REMOTE BISTATIC RECEIVER SYNCHRONIZATION USING DLL TECHNIQUES

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INTRODUCTION

A bistatic radar can be formed using a pulsed monostatic radar as transmitter and an omnidirectional remote receiver (1). In this case the target location is obtained from the azimuth angle of transmitter antenna, the baseline between transmitter and receiver sites, and the time interval ΔT between transmission of the pulses and reception of the target echoes.

The performance of a bistatic radar depends on the quality of the synchronization of the transmitter and receiver (2). Synchronization techniques are usually done with a direct link between sites (3), or via two high stability clocks previously synchronized. An alternative method, known as *hitchhiking* (1), is based on the synchronization of the necessary signals (Azimuth Reference Pulse, emitted Pulse Repetition Frequency, and phase and frequency of emitted signal) in the short period of time when the radar transmitted beam directly illuminates the receiver site.

At the U.P.C. a bistatic receiver is being developed which uses a S-band 2-D, monostatic Airport Surveillance Radar as transmitter, installed at the Airport of Barcelona, 11 Km away from receiver site. The receiver uses the hitchhiking method to synchronize the transmitted signal, which is a 6 PRF, pulse to pulse, staggered sequence.

Pulse to pulse staggering in the Pulse Reference interval (P.R.I), usually used to increase the radar unambiguous range and MTI blind speeds (3), complicates notably the synchronization of the pulsed waveform. A free running open loop technique may be used for this purpose, adjusting a stable clock at the same frequency as the transmitted pulses (4), which is synchronized by the received sequence during direct illumination. When the received signal can be contaminated by interferences, noise, or multipath effects, a more robust closed loop approach is desirable (5). This paper presents a closed loop solution to the synchronism process, based on a Delay-Lock Loop (DLL) configuration (5), using the special properties of the pulse to pulse staggered signal, that can be considered as a digital pseudorandom code modulation with a period equal to the P.R.I.

DLL DESCRIPTION

The Delay-Lock Loop has been described as an optimal device for tracking the delay difference between two correlated waveforms, and it is a nonlinear feedback system, which employs a form of cross-correlation in the feedback loop to control the delay of two signals, in the same manner that a phase-lock loop (PLL) tracks the phase of a sinusoidal signal (figure 1). DLL is systematically used in Spread-Spectrum satellite communications, to synchronize the digital pseudorandom reference sequence, achieving a reduction of the effects of interferences due to other users and intentional jamming.

The DLL is based on a VCO as clock, which generates an internal pseudorandom sequence, similar to the sequence to be recovered, and a correlator block, which detects the delay between sequences as the phase detector in a PLL detects the phase error. Synchronization between received and internal sequence is based on varying the control voltage of the VCO, this control voltage is an error signal consisting in the filtered subtraction of the correlations between the received modulation and the $\tau/2$ advanced and delayed versions of the internal sequence, where τ is the pulse duration, figure 2 shows the substraction of correlations as a function of the time delay between sequences.

Assuming no delay exists between sequences (corresponding to point A_1 in the subtracted correlations in figure 2), if the internal sequence delays, the control voltage moves to B, the VCO is excited with a voltage that increases the output frequency, thus the internal sequence is accelerated and synchronized. The voltage tends to A_1 again, which is a stable equilibrium point. Examining the control signal we can see that there are other stable equilibrium points (marked as A_i), which may cause an undesirable constant delay (false lock) and must be inhibited. Figure 2 shows also that for some delay ranges, deadzones appear where no active VCO control is applied. These lost control time intervals enlarges considerably the synchronization time.

PROPOSED STAGGERED PRF SYNCHRONIZER

Figure 3 presents the proposed staggered PRF synchronization system, which solves the false locks and deadzone problems. We can distinguish two different parts, a presence and coarse alignment detector block, and the fine alignment block, the first one detects when the incoming signal is present (Presence line), and if it is close enough to the internal generated sequence (Alignment line), the second block, based on

the DLL configuration, performs the fine sequence alignment.

The system operates under two different modes: acquisition and tracking. In the acquisition mode no coarse alignment exists (alignment=0) during the illumination window, the internal sequence is progressive delayed until the delay is less than $\tau/2$, in order to inhibit false locks. During the acquisition the VCO is controlled with a constant voltage (V_{ref}) that ensures the progressive delay. The tracking mode operates when the delay is less than $\tau/2$ (marked by a high correlation between sequences, alignment=1) to make the fine delay adjust. The VCO control voltage in tracking mode is the filtered signal at the output of the delay detector. The synthesized staggered PRF generation is maintained when no illumination window is present by the Track & Hold block, which preserves a constant VCO control voltage.

Special characteristics of the system

Progressive delay in acquisition mode cannot be more than τ between two consecutive illuminations, in order to ensure synchronization in a direct illumination, this limitation implies a range restriction of the VCO constant control voltage.

To improve the synchronization the pulse width τ has been extended, reducing the acquisition time. Pulse extension aids the track process too, because the linear interval of the correlation is larger than with the original pulse and the deadzones are reduced. However there is a restriction in pulse enlargement, because the correlation sidelobes increase which can cause false locks.

The filter F(s) in figure 3 includes the correlator and the loop filters, and its design is very critical, its parameters control the loop performance synchronization time in track mode, which must be less the illumination time. A convenient method of performance analysis in order to choose the loop filter parameters consists in linearizing the different parts, supposing that the output signal of the correlator is directly the delay time error. Then the input signals to the delay detector are directly the initial received and internal generated pulse time variations, T and $\bar{T}$ respectively (6)(7), their relationship can be expressed by their Laplace transform as follows:

$$\epsilon_T(s) = \frac{1}{s + K_d K_{GI} F(s)} T(s)$$

$$\epsilon_T(s) = \bar{T}(s) - T(s)$$

Where K_d is the equivalent delay detector constant, measured in volt/sec, and K_{GI} is the VCO and Internal Generator constant, in sec/(sec·volt).

System error sources, noise and multipath effects

The ideal system performance is predominantly affected by the quantization error in the A/D process, the possible different expansions of the received and the internal generated pulses, and the correlator implementation.

The VCO sensitivity and number of bits in the A/D-D/A converter are very critical parameters. There is a compromise between VCO frequency range an number of bits, large frequency range needs large number of A/D-D/A bits in order to minimize the quantization control voltage error, large errors represent a large accumulated delay error. Narrow frequency range allows a few number of bits, but it is not possible to ensure that the DLL works in linear regime, which increases the synchronization time.

Different expansion of pulses introduce an imperfect delay detection, because the maximum amplitudes of the correlations are different. This problem is reduced introducing a constant offset voltage into the loop filter, which is adjusted in the calibration procedure of the system.

Filter parameters determine the control voltage amplitude ripple, due to the non-ideal characteristic of the correlators. Large ripple represents a high uncertainly in the sampled & held control voltage, which determines the synchronization quality, measurable with the accumulated delay between sequences when no direct illumination is present.

Assuming that the signal at the input is the envelop detection of the received signal plus noise, the Gaussian band limited white noise becomes a Rayleigh process. This noise introduces a random time shift or Jitter in the detected pulses (8), with a nonzero mean value, which depends on the receiver bandwidth. Thus a biased misalignment appears, and a random time varying error is introduced into the loop. The VCO control voltage is contaminated by a highpass filtered version of this random error, that supposes an introduction of a time estimation jitter. Their effects can be studied using the linearization of the system response:

$$C(s) = \frac{sF(s)K_d}{s + K_d K_{GI} F(s)} \left[E_T(s) - T(s)\right]$$

Where C(s) is the VCO control voltage, and E_T is the random error of the pulse arrival. A degradation of the quality of synchronization must be added to preceding effects due to the random variation of the VCO control voltage, that increases the VCO control voltage

uncertainly value in A/D conversion.

Specular multipath effect on the system produces in the received signal a superposition of two identical sequences with a constant time delay between them (7). A false pulse acquisition can result if the coarse alignment detector block cannot distinguish the true sequence. Pulse expansion eliminates these effects if the width is larger than the multipath delay.

EXPERIMENTAL RESULTS AND CONCLUSIONS

An experimental Staggered PRF synchronizer, based on a DLL, has been tested using a transmitter signal simulator that simulates the staggering sequence windowed by the antenna beam. The measured system performance ensures synchronization with a 30 ms direct illumination, with an accumulated delay error in the order of the resolution cell positioning error in range, using low cost 8 bit A/D-D/A converters and 1MHz $\pm$ 40Hz VCXO.

An artificial time expansion of the received pulses is performed in order to reduce the acquisition time synchronization, this modification supposes a reduction of the multipath effects too.

A bistatic radar synchronization method, based on DLL, has been developed. The system has been analyzed by linearization of the different parts and signals involved. The parameters that degrade system performance are obtained, and some solutions are presented in order to minimize their effects. Received noise degradation effects in this particular system are been studied too, where the most important are the time estimation jitter and a constant alignment error.

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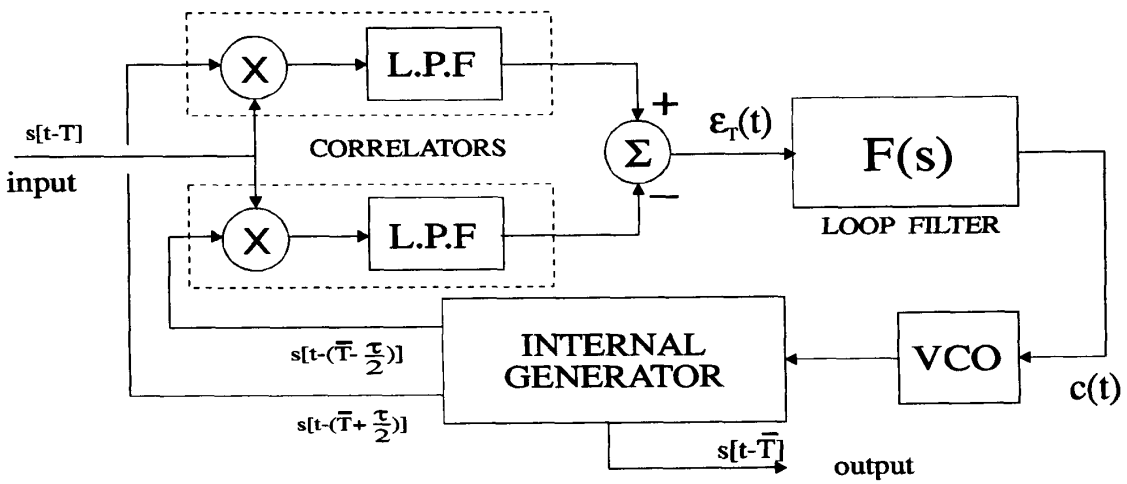

figure 1. Schematic diagram of the DLL

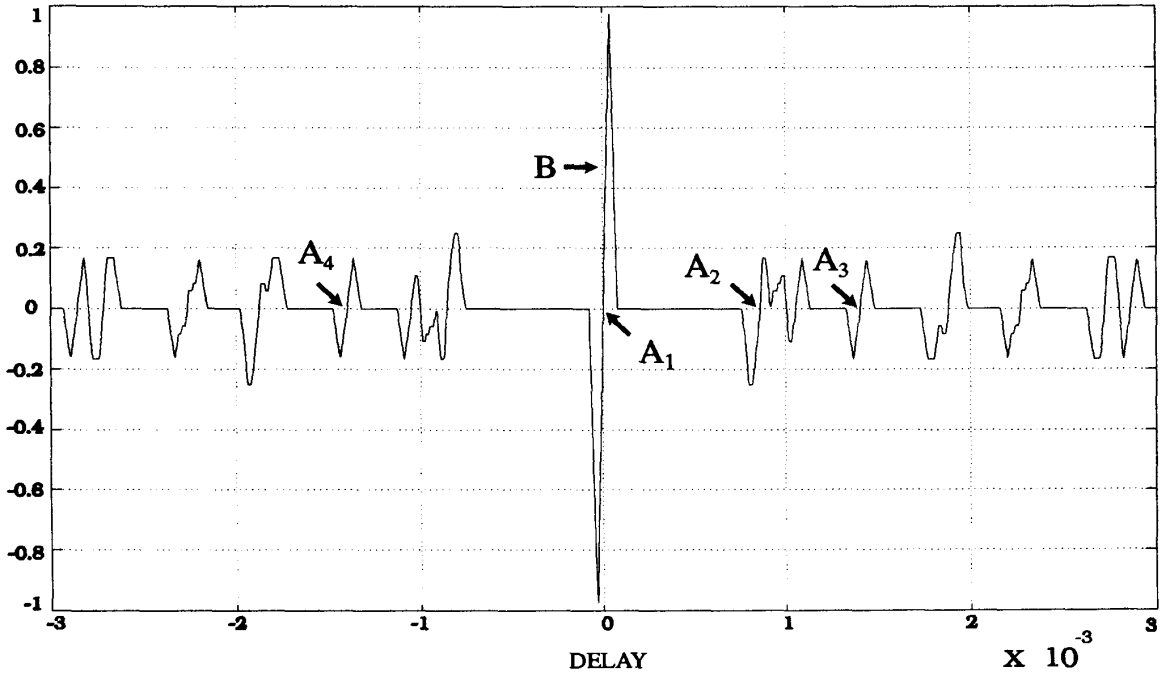

figure 2. Substracted correlation signal at the input of the loop filter.

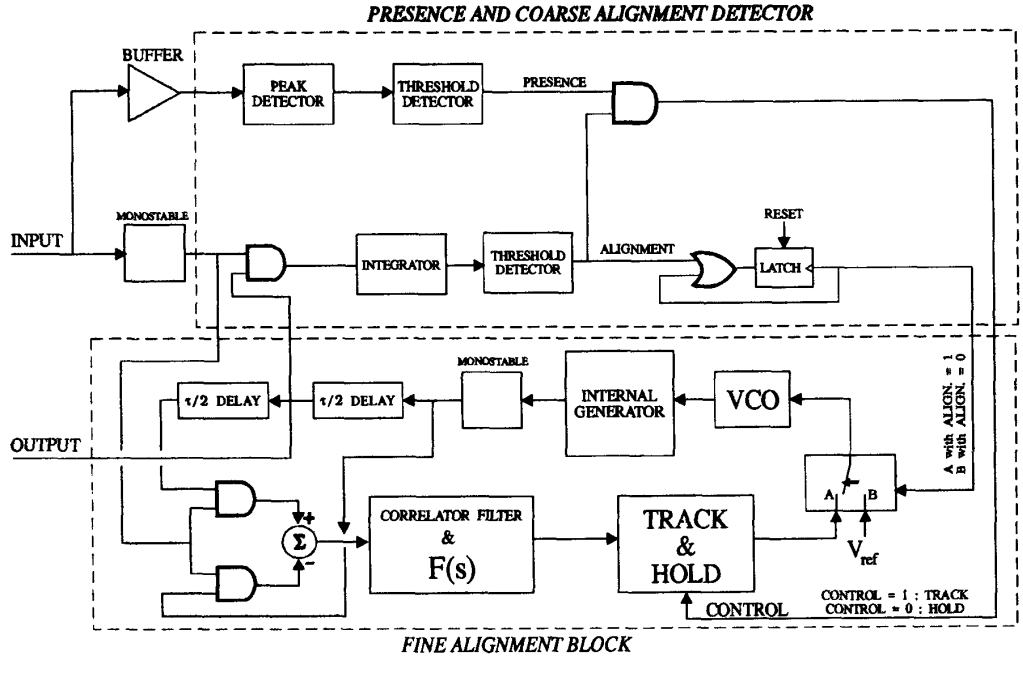

figure 3. Proposed staggered PRF synchronism circuit.