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A PULSED CARRIER RECOVERY USING A DISCRETE CONCEPTION OF THE PLL

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ABSTRACT

A bistatic Radar system needs an accurate synchronization between the transmitter and a the remote receiver, in order to achieve a correct coherent target detection and positioning [1]. This paper presents an unlinked receiver carrier phase/frequency synchronization method, from the radiated pulsed signal of a remote radar transmitter when its antenna beam illuminates the receiver. A modified discrete conception of the PLL technique is used, based on the special properties of the signal to be recovered.

INTRODUCTION

Coherent target detection and processing is used in modern radar systems to reject static clutter echoes and estimate target velocities from the doppler frequency shift of the scattered signals. Coherent detectors require precise phase and frequency references of the transmitted pulses [2]. In conventional monostatic systems both emitter and receiver share the same reference oscillators. This is not the case for bistatic or multistatic systems in which a remote receiver must use dedicated links to achieve coherent operation. An alternative is to synchronize a high stability oscillator from the radiated signals by the transmitter when the antenna is in the receiver direction. A typical radar signal consists of a basic rectangular RF pulse of 1 μs width which is repeated with a period of 1ms. The transmitter antenna rotation speed and beamwidth limits the availability of the signal from the receiver to windows of around 30 ms every 4.5 s (figure 1). Thus the synchronism technique proposed must acquire the phase of the signal in the short visibility time and maintain the coherence until the next antenna scan. Similar synchronization problems with limited access to reference are encountered in other important areas like TDMA and mobile communication systems [3].

Phase and frequency recovery are usually based on PLL techniques [4][5] (figure 2), where the synchronized signal is obtained with a VCO controlled with the filtered phase error between the reference signal and its output. PLL systems have been extensively studied for incoming continuous wave (CW) signals, this is not the case when the signal has a pulsed characteristic like the transmitted radar signal, which has an extremely low duty cycle, on the order of 10^{-3}. A discrete-time PLL technique is proposed to achieve the synchronization of pulsed signals considering the pulse modulation as a temporal sampling.

THE PLL AS A PULSED CARRIER SYNCHRONIZER

A second order PLL with a perfect integrator loop filter (figure 2) is able to maintain the synchronism when the reference signal has an amplitude modulation, whenever the Acquisition process has been done, and the system is under Tracking mode. The best way to use the property of immunity to amplitude modulation is to perform the acquisition process during just one received pulse, and ensure it has been completed when signal vanishes. However, the non ideal performance of the loop filter and the VCO, in the PLL, reduce considerably this characteristic. It can be seen a reduction of the loop bandwidth, that increases the acquisition time, and the appearance of a peak at the cut-off frequency, that implies a potential source of unstabilities. Thus a PLL designed for large bandwidth, is not a well solution to synchronize pulsed signals.

At the closed-loop, For low duty cycle rectangular amplitude modulation, the output signal from the phase detector is the sampled version of the phase error when the incoming signal has CW characteristic, with a sampling interval T equal to the modulating signal. From this consideration, it is possible to reach the synchronization making use of the whole burst of pulses in the received signal window. We must use theories usually employed in discrete and digital system. In the

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loop filter (figure 2), y(t) can be expressed as:

$$y(t) = y[(n-1)T] + \frac{\tau_2}{\tau_1}x(t) + \frac{1}{\tau_1}\int_{(n-1)T}^{t} x(t)\,dt \;;\; for\; t \geq (n-1)T \quad \textbf{(a)}$$

And at the VCO, we have:

$$\theta_0(nT) = \theta_0((n-1)T) + K_0\int_{(n-1)T}^{nT} y(t)\,dt \quad \textbf{(b)}$$

using (a) and (b) the output phase of the VCO, at the instant of sampling, can be written as:

$$\theta_0(nT) = \theta_0((n-1)T) + K_0\left[Ty((n-1)T) + \left[\frac{\tau\tau_2}{\tau_1} + \frac{T\tau}{\tau_1} - \frac{\tau^2}{2\tau_1}\right]x((n-1)T)\right]$$

where τ is the received pulse duration. Last expression represents the evolution of the VCO phase at the instants of sampling, as a function of the signals at previous instants. We can use the Z-transform in order to obtain the relationship between signals:

$$\theta_0(z) = \theta_0(z)z^{-1} + K_0[Ty(z)z^{-1} + Kx(z)z^{-1}]$$

$$where\; K = \frac{\tau\tau_2}{\tau_1} + \frac{T\tau}{\tau_1} - \frac{\tau^2}{2\tau}$$

We can express y(nT) with its Z-transform as:

$$y(z) = \frac{\tau}{\tau_1}\frac{z^{-1}}{1-z^{-1}}x(z)$$

Then, the VCO phase is:

$$\theta_0(z)(1-z^{-1})^2 = K_0\left[K + \left(\frac{T\tau}{\tau_1} - K\right)z^{-1}\right]x(z)z^{-1}$$

Where $x(z) = K_d[\phi(z)]$, and $\phi(z) = \theta_i(z) - \theta_0(z)$. After some operations we get the phase error evolution as:

$$\phi(z) = \frac{(1-z^{-1})^2}{1-[2-KK_0K_d]z^{-1} + \left[1 + K_0K_d\left(\frac{T\tau}{\tau_1} - K\right)\right]z^{-2}}\theta_i(z) \quad \textbf{(c)}$$

Using Z-transform theory, the system is stable if the denominator has its roots with a module less than 1. And using the last value theorem [6], it is seen that phase error tends to zero for step and ramp variation of the input phase θ_i. The loop transfer function is the eq.(d).

Loop filters parameters must be modified respect to values obtained for analog PLL in order to ensure loop stability and acquisition velocity, a well method to calculate them is to obtain the equivalent analog system

$$H(z) = \frac{\theta_0(z)}{\theta_i(z)} = \frac{K_0K_d\left[K + \left(\frac{T\tau}{\tau_1} - K\right)z^{-1}\right]z^{-1}}{1-[2-KK_0K_d]z^{-1} + \left[1 + K_0K_d\left(\frac{T\tau}{\tau_1} - K\right)\right]z^{-2}} \quad \textbf{(d)}$$

by replacing z by $(1+j\omega T)$ [7], if the equivalent analog bandwidth B_L is $B_L << 1/T$, and calculate them for a fixed natural frequency and damping factor of the loop transfer function.

However the system is still under technological limitations and the system cannot maintain the coherence between two consecutive signal windows, because the real O.A reduces the ideal integrator performance of the loop filter.

FIRST APPROXIMATION TO SOLUTION

Next step is to seek some solutions to avoid these limitations, that degrades the system performance. The best way to do this is to replace analog loop filter by a digital conception filter, because it permits an easy implementation of integration performance better than with an A.O. Using Z-transform, the PLL can be represented as in figure 2, replacing F(s) and V(s) by F(z) and V(z), which are the loop filter and VCO transfer function in Z domain. The Closed-Loop Transfer Function and Phase Error, in linear regime, are:

$$H(z) = \frac{K_dF(z)V(z)}{1 + K_dF(z)V(z)}$$

$$\phi(z) = \frac{1}{1 + K_dF(z)V(z)}\theta_i(z)$$

If we design a loop filter with a relation in time domain as:

$$y(t) = y((n-1)T) + K_f[x(nT) - ax((n-1)T)] \quad for \quad nT \leq t < (n+1)T$$

that implies in the Z-domain:

$$F(z) = \frac{y(z)}{x(z)} = \frac{K_f(1-az^{-1})}{1-z^{-1}}$$

In the VCO we have:

$$\theta_0(nT) = \theta_0((n-1)T) + K_0 T y((n-1)T)$$

$$V(z) = \frac{\theta_0(z)}{y(z)} = \frac{K_0 T z^{-1}}{1 - z^{-1}}$$

Obtaining:

$$H(z) = \frac{K_0 K_d K_f T(1 - az^{-1})z^{-1}}{1 - (2 - K_0 K_d K_f T)z^{-1} + (1 + aK_0 K_d K_f T)z^{-2}}$$

$$\phi(z) = \frac{(1 - z^{-1})^2}{1 - (2 - K_0 K_d K_f T)z^{-1} + (1 + aK_0 K_d K_f T)z^{-2}} \theta_i(z)$$

These expressions for Loop Transfer Function and Phase Error evolution, are similar to (c) and (d), which tell us that this configuration is able to synchronize the VCO to the phase and frequency of the pulsed carrier. And it is similar to the general baseband model of a Digital PLL (DPLL)[7].

Systems which are described by the Z-transform can be easily simulated numerically. Using the properties of discrete time signals, the general expressions relating the PLL signals can be written as:

$$\begin{aligned} x(n) &= K_d \sin[\theta_i(n) - \theta_0(n)] \\ y(n) &= y(n-1) + K_f(x(n) - ax(n-1)) \\ \theta_0(n) &= \theta_0(n-1) + K_0 T y(n-1) \end{aligned} \qquad \text{(e)}$$

System simulation using these expressions allows to calculate loop filter parameters in order to reach stable performance, and optimize the phase and frequency acquisition time.

frequency acquisition uncertainty

It can be seen that the system possibly acquires the reference phase and frequency with an error always multiple of the sampling frequency. It can be explained observing the signal from the phase detector in two different situations, when the VCO phase close to the input phase, and VCO phase with a frequency shift multiple to the sampling frequency, the input signal to the loop filter cannot be distinguished under these two situations, and the loop acts at the same manner. This behavior is encountered in all discrete systems where there is a periodic spectral performance. However this frequency discrete ambiguity is not a handicap in the specific case where we use it, since the radar processor compensates internally this frequency shifts.

THE PULSED CARRIER SYNCHRONIZER

Figure 3 shows a hardware solution that implements the proposed loop filter, based on Sample & Hold circuits acting as delay tapped lines, that maintain constant the necessary signals between two consecutive pulses. The sampling is synchronized to the instants of pulse reception.

Several measured results of the loop performance are presented in figures 4 and 5, that can be compared with the simulation results using the expressions (e), for the same VCO, phase detector and loop filter parameters, and similar initial conditions. It is shown that the measurements are very close to simulation. In these figures are shown that, for small frequency errors, the process can be considered as linear (Sinus operand of the phase detector is approximated by its angle), and a pull-in process is observed for large frequency errors.

This configuration theoretically solves the coherency maintenance when no direct illumination is done. However the drift of the Sample & Hold circuit as a controller of the VCO produces a progressive frequency drift, unacceptable for this application.

The discrete consideration of the system allows to use A/D-D/A converters and digital registers as delay lines, to implement the loop filter transfer function. A loop filter using digital-analog converters has been developed, based on a D/A input-output PC card (figure 6), and it has seen that it is able to be used (figure 7). Using this loop filter, the frequency drift due to the non-ideal integrator performance is solved, but a quantization error effect appears as a limitation of performance, because the VCO control voltage is restricted to the finite range of digitized levels. It can be reduced using large number of bits for a defined discretization window.

CONCLUSIONS

A PLL technique suitable to periodic pulsed signals has been presented, based on a discrete-time treatment of the involved signals. This consideration allows an easy and realistic simulation of the PLL acquisition and tracking processes. At the same time, the loop filter may be implemented by delay tapped lines. Two experimental loop filters has been implemented, one based on S&H circuits, and another on D/A and digital registers, that show a close agreement between simulated and actual performance. The proposed approach can be applied to pulsed signal synchronization for radar and communication coherent systems.

ACKNOWLEDGEMENT

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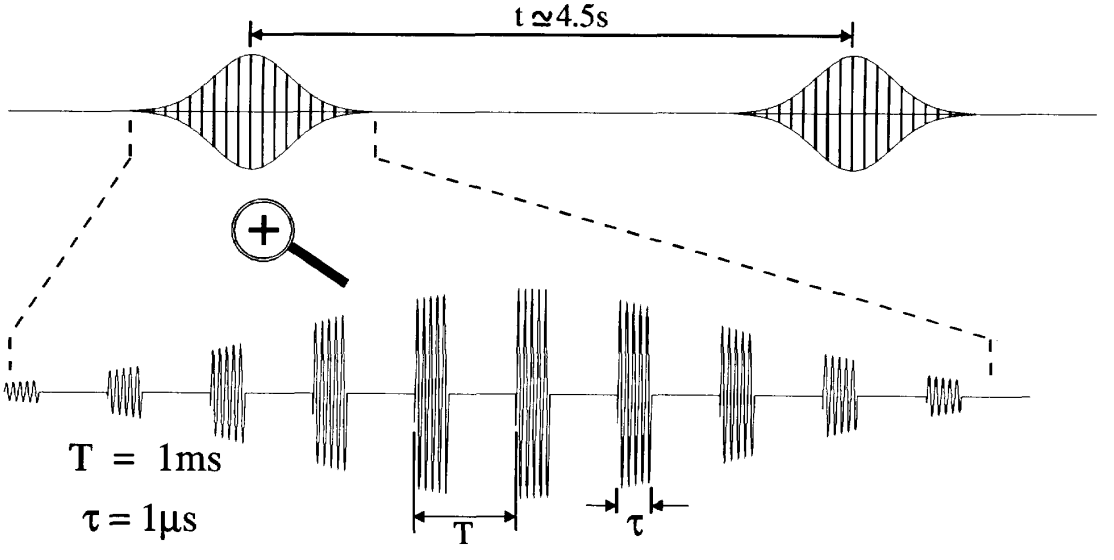

figure 1. Received signal aspect.

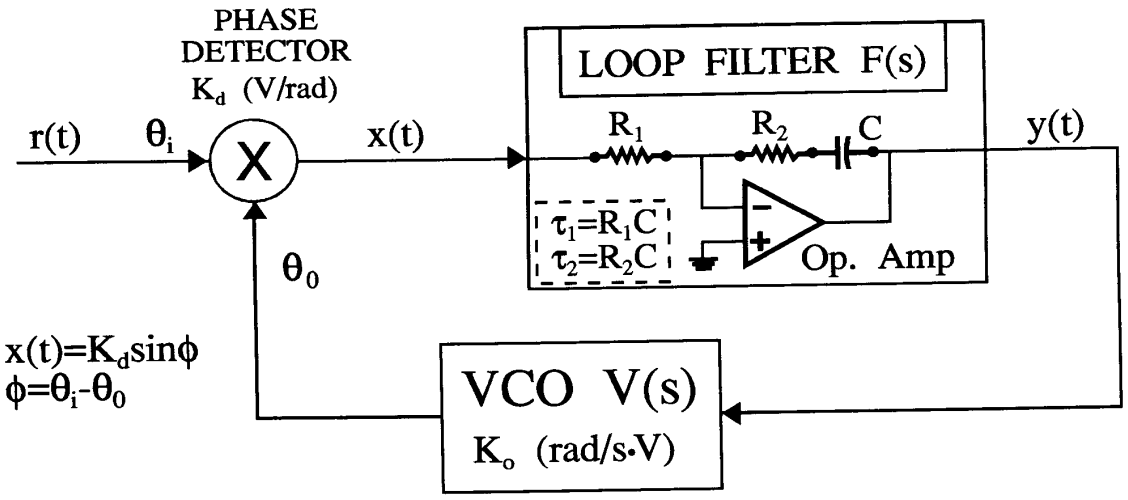

figure 2. General diagram of the Phase-Locked Loop.

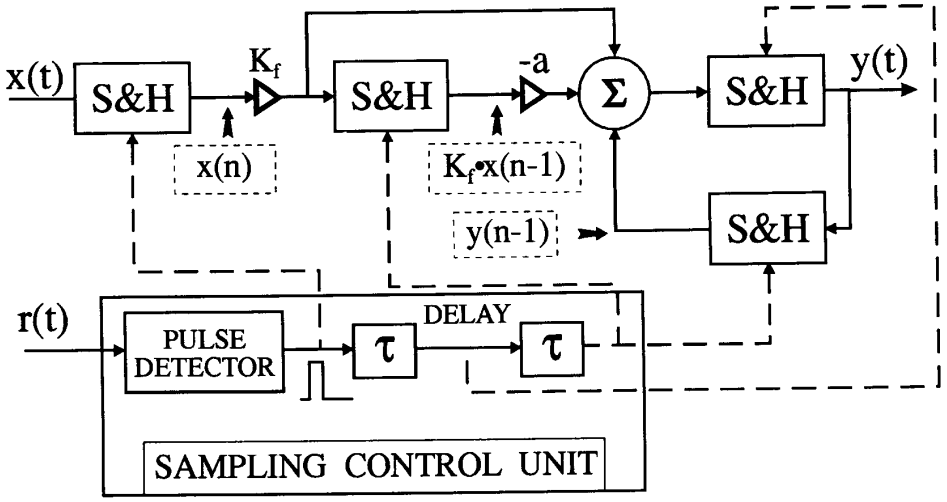

figure 3. Proposed new Loop Filter, based on Sample and Hold circuits.

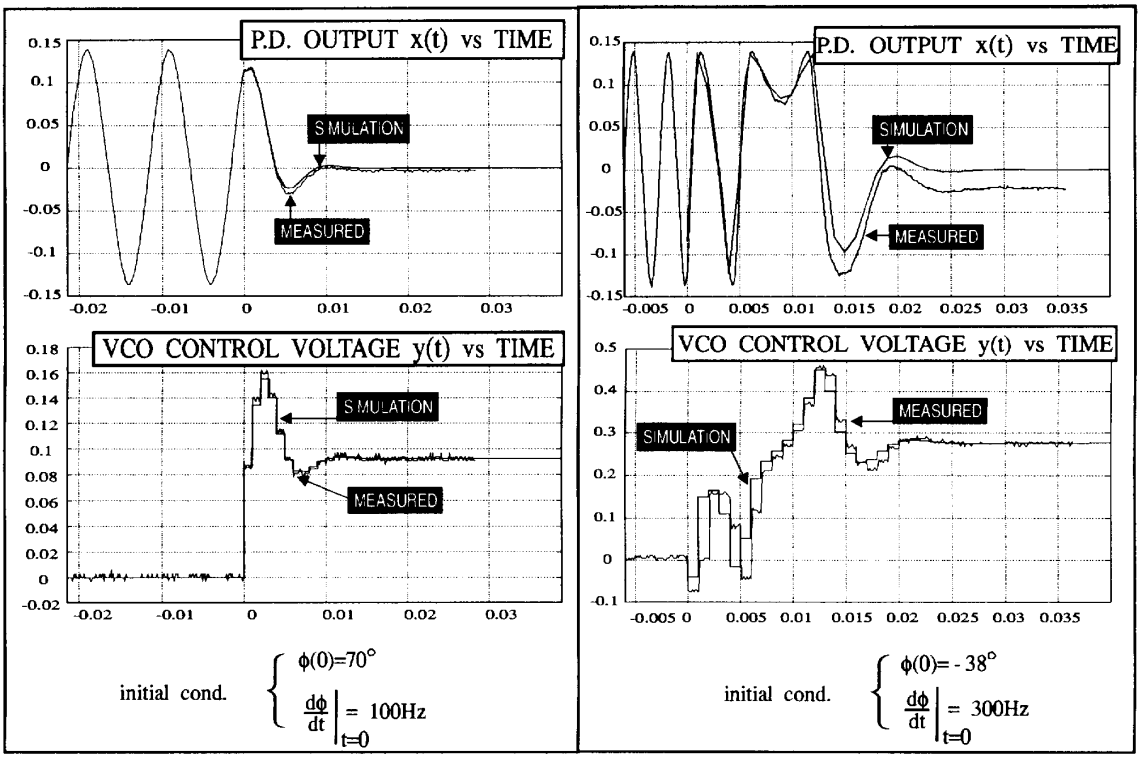

figure 4 and 5. Measurement and simulation results. K_0=6800 rad/s·V, K_d=0.1375 V/rad, K_f=1, a= 0.6, f=30MHz.

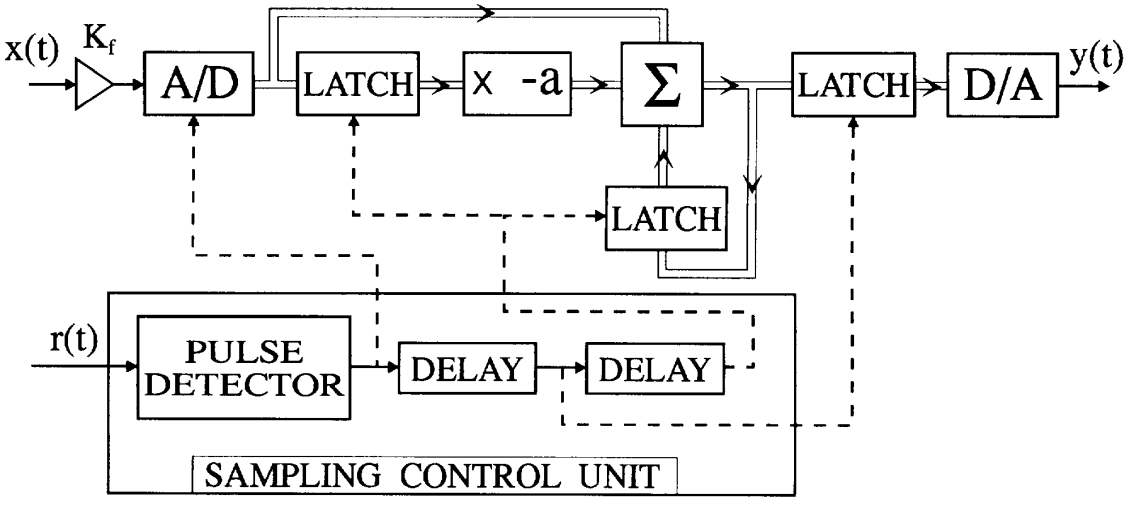

figure 6. Proposed All-Digital Loop Filter.

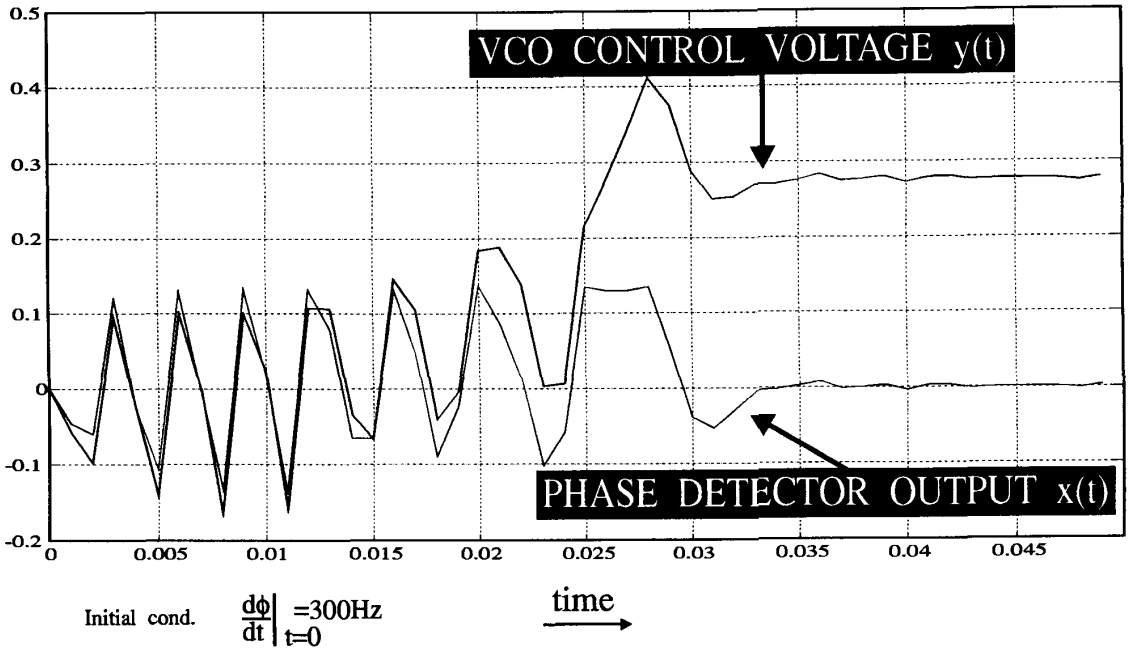

figure 7. System response with the Loop Filter of fig. 6. Same loop parameters.