High Efficiency Reconfigurable Class-F Power Amplifier at 2.4 GHz in CMOS-MEMS Technology

Mitra Gilasgar[1], Antoni Barlabé[1], Lluís Pradell[1], Maher Bakri-Kassem[2], Raafat Mansour[3]

[1]Technical University of Catalonia, TSC Dep., Campus Nord UPC, 08034 Barcelona, Spain
e-mail: mitra.gilasgar@tsc.upc.edu

[2]American University of Sharjah, Electrical Engineering Dep., Sharjah, United Arab Emirates

[3]University of Waterloo, Electrical and Computer Engineering Dep., Waterloo, Ontario, Canada

***Abstract* — A novel reconfigurable CMOS class-F power amplifier is proposed in this paper which can adapt to load variations resulted from the hand effect on a mobile phone. Reconfigurability is achieved by using MEMS switches that are integrated monolithically in the CMOS technology along the rest of the circuit, reducing the cost and size. This structure integrates MEMS varactor inside CMOS technology that are built through a mask-less post-processing technique. Designed for 2.4GHz, for a load impedance of 50Ω, simulations results show that the power amplifier achieves a power added efficiency of 32.8% and a power gain of 12.9 dB, while delivering peak output power of 18.2 dBm. Simulation results for different load variations have been performed showing a great improvement in efficiency and output power by using the proposed structure. The total size of the fabricated chip is 1.6 mm x 1.6 mm.**

I. Introduction

Power Amplifiers (PAs) are critical blocks of transceivers due to their high power consumption. It is necessary to design high efficiency PAs [1] in order to increase the battery life time of the device. In addition to high efficiency, small size and low cost are also demanded. Traditionally, PAs have been implemented in technologies such as GaAs and InP HEMT. With the growth of complexity in RF frontends there is a great need to integrate the PAs with other devices. CMOS technology offers low cost and high integration level, and most handset components are built using CMOS technology. However PA is still considered the most difficult block to implement in CMOS due to the low breakdown voltage, the conductive substrate, and the high sheet-resistance of the poly silicon that limit the output power and efficiency of the PA. Switching power amplifiers [1] have a minimum overlap between drain voltage and current waveforms, resulting in low power consumption and high efficiency. Class-E PA has a simple load network consisting of one resonator while class-F uses multiple resonators in its output matching network (OMN) to obtain a drain half-sine current and a square voltage waveform, increasing the complexity of the design. However Class-E suffers from voltage stress on the device output. The voltage swing on the drain for a class-E PA can reach up to 3.6 V_{DD}, while only 2 V_{DD} is possible for a class-F PA. Therefore, for the implementation of high efficiency PAs on low breakdown technologies such as CMOS, a class-F PA is more suitable. There are very few class-F PAs reported in CMOS technologies [2]-[3]. The control of load impedances for a limited amount of harmonics allows class-F PA to obtain high efficiency at high frequencies. In theory class-F can achieve 100% efficiency [4] but this figure is lowered in practice due to the limited number of harmonics that can be tuned through the OMN. A comprehensive study of class-F PA was developed in [5]-[6].

In addition to high efficiency, it is desired that the PA could adapt to different conditions in wireless applications, such as the impedance change of the antenna when a user holds a mobile phone. The strong interaction between head, hand and antenna causes a change in antenna impedance which leads to a reduced performance [7]-[8]. Impedance tuners can be used to overcome this problem. Tunable matching networks (MN) have been demonstrated based on single-stub, double-stub, triple-stub, quad-stub or load line techniques [9] using varactors [10]-[11]. RF MEMS varactors are particularly attractive for the tuner integration because they have low insertion loss compared to MOS varactors and better linearity. Integrated RF MEMS tunable MNs are presented for adaptive amplifiers in CMOS technology [12]-[14] and GaAs technology [15].

In this work, the effect of load variation is compensated by reconfiguring the CMOS class-F PA output load matching using an impedance tuner. This tuner integrates two RF-MEMS variable capacitors in CMOS and can adapt to different load impedance values. The proposed class-F PA topology is explained in section II. The structure of the MEMS varactor is shown in section III. Load-pull and source-pull analysis are explained in section IV following with the simulation results in section V and the conclusions in section VI.

II. Proposed Topology

In class-F PAs, the load impedance seen by the power transistor should be a short circuit (sc) at even harmonics, an open circuit (oc) at odd harmonics and the optimized value at fundamental frequency:

$$Z_1 = R_{optimal}, \quad Z_{2n} = 0, \quad Z_{2n+1} = \infty \qquad (1)$$

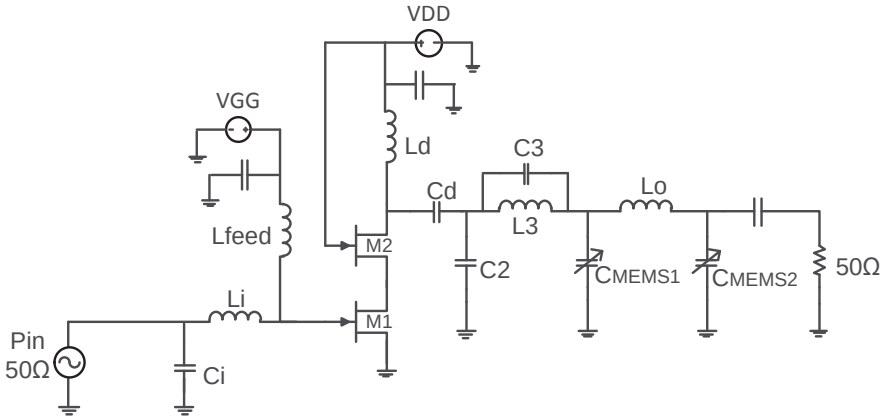


Fig. 1. Reconfigurable class-F PA designed in CMOS-MEMS technology.

The schematic diagram of the proposed integrated PA is shown in Fig. 1. It is designed using the TSMC 0.18 µm CMOS technology at 2.4 GHz. The input matching network (IMN) consists of a capacitor (Ci) and an inductor (Li) to match the power device to 50 Ω input impedance for a high power transfer. In the OMN, fundamental matching and harmonic termination is done using lumped capacitors and inductors, tank L3C3 provide the open circuit for 3rd harmonic and C2 provide the 2nd harmonic short circuit. C_d is used for DC block as well as for matching at fundamental frequency. Impedance reconfiguration is achieved by two MEMS varactors. The design process of these capacitors is explained in section III. A cascode structure ensures that the circuit works under stable conditions and reduces the voltage stress on the CMOS transistor. High-Q inductors are required in the output of a PA to match to 50Ω and their implementation is very difficult in CMOS. The implementation of the inductors in the IMN and OMN is explained in section III.

III. MEMS Analogue Continuous Varactors

The utilized RF MEMS devices are designed using the CMOS Back-End-Of-Line (BEOL) metallization. The cross section of the metallization layers is illustrated in Fig. 2 (a) and the proposed MEMS varactor is illustrated in Fig. 2(c). This structure integrates the MEMS capacitor inside CMOS technology and uses a mask-less post-processing technique. In order to meet the design rules of the CMOS 0.18 µm technology, special attention is paid to the metal layers for plates of capacitor, mask and sacrificial layer. As it is demonstrated in Fig. 2(b), Metal 5 is used as the top layer of the MEMS capacitor and metal 3 is used as the bottom layer of the capacitor. Metal 6 is used as the mask and metal 4 is used as the sacrificial layer. Metal 6 extends 2 µm over metal 5 and metal 3 to protect the capacitor's plates from being etched away.

A special post processing technique that can be applied to CMOS technology is used to release the MEMS capacitors [12]-[14]. The post-processing steps are: 1) 1st dry etching; 2) wet etching; and 3) 2nd dry etching. A trench of 100 µm is created in the silicon substrate to improve the quality factor of the capacitor and enhance the RF performance.

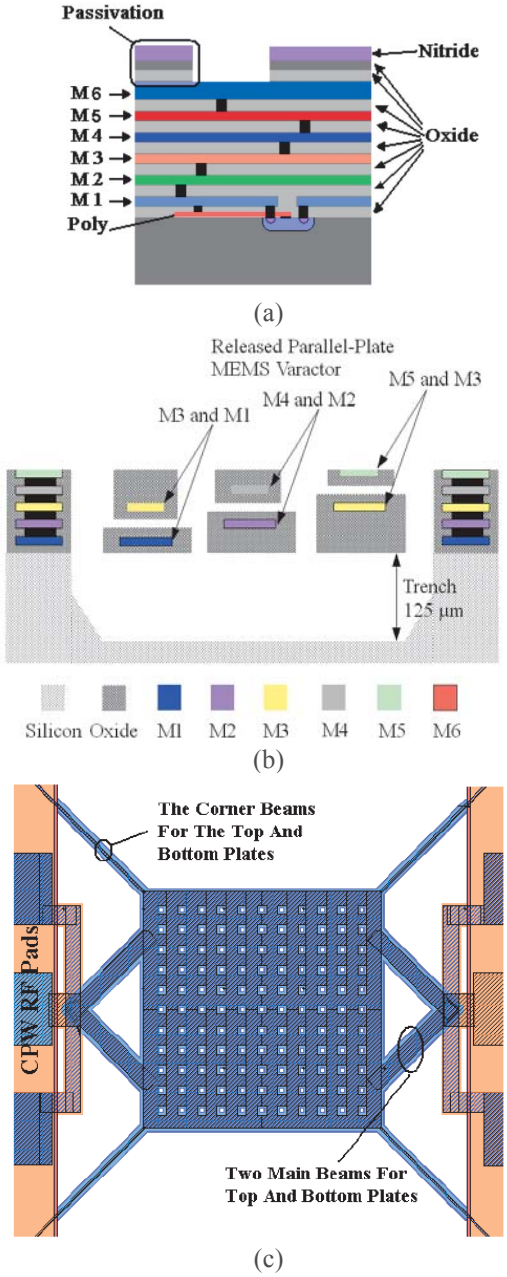


Fig. 2 (a) The cross sectional view of the CMOS 0.18 µm technology from TSMC, (b) Cross-section of MEMS-CMOS post-processing technique in TSMC 0.18 µm CMOS process and (c) Proposed analog MEMS continuous capacitor.

Two different sizes of the MEMS analogue continuous capacitor [12] are designed to achieve targeted values of 0.9-1.8 pF for CMEMS1 and 0.9-1.5 pF for CMEMS2. The quality factor at 2.4 GHz exceeds 100 [12]. On chip inductors in the IMN and OMN are implemented using a stacked structure from Metal 1 to Metal 4 to increase the Q factor. Using the post processing technique, a trench will be created beneath to further increase the Q and decrease the losses from the substrate. Electromagnetic simulation results show that a Q of 7.3 for L3, 10 for Ld, 7.8 for Li, and 10.7 for Lo are achieved.

IV. Load-Pull Analysis

In practice, due to nonlinearities and parasitics of the active device, ideal short and open circuits at harmonic frequencies do not necessarily lead to the best results. Therefore, to achieve the best performance, an accurate load matching for the output of transistor at fundamental and harmonic frequencies is required. Calculated from Load-Pull analysis, Z_{L1}, Z_{L2} and Z_{L3} are load impedances that result in an optimum performance at fundamental, second and third harmonics respectively. The calculated values are given in Table 1 and the OMN shown in Fig 1 is designed to give these optimum impedances at the desired frequencies.

V. Simulation Results

To evaluate the performance of the proposed PA design, simulations are performed using Keysight ADS and Cadence Spectre RF. The simulated drain voltage and current waveform of the PA are shown in Fig. 3. The power spectrum for the case of 50 Ω load impedance is shown in Fig. 4. The proposed PA achieved a 2nd and 3rd harmonic rejection of 26.9 dBc and 44.8 dBc respectively.

The simulated results of power-added efficiency (PAE) and efficiency versus input power are shown in Fig. 5. Output power and gain simulation results vs. input power are shown in Fig. 6. For an output load impedance of 50Ω and an input power of 7 dBm, a peak PAE of 32.8 %, a drain efficiency of 34.6% and a gain of 12.9 dB are obtained while delivering an output power of 18.2 dBm.

Values of CMEMS1 and CMEMS2 are 1.7pF and 1pF for this case. To test the effect of load variation, other impedance values are considered for the load and the MEMS capacitors are tuned accordingly. Then the results are compared to a case where there has not been any tuning (meaning that the CMEMS1 and CMEMS2 remain the same values of 1.7 pF and 1 pF respectively). The results are shown in Table 2. In all of the cases a higher PAE and a higher output power are achieved by tuning the circuit. Fig. 7 shows a picture of the manufactured PA chip before the post-processing. The fabricated chip is under the post-processing and will be measured soon.

	Load impedance (Ω)
Z_{L1} (@ 2400 MHz)	14.138 + j·20.194
Z_{L2} (@ 4800 MHz)	- j·65.268
Z_{L3} (@ 7200 MHz)	-j·6.367

Table 1. Load Impedances for fundamental, second and third harmonic from load-pull analysis.

Load impedance	PAE	Pout	
50Ω	32.8	18.2	Default
50 + j75 Ω	24	16.7	Tuned
	17.4	15.8	Not-Tuned
75 + j50 Ω	29.8	17.5	Tuned
	23.3	17	Not-Tuned
75 + j100 Ω	20.4	16.4	Tuned
	13.8	15.1	Not-Tuned
100 Ω	27	17.7	Tuned
	24	17.3	Not-Tuned
100 + j50 Ω	26.1	17.6	Tuned
	21.1	16.8	Not-Tuned
30 + j75 Ω	21	16	Tuned
	13.6	14.7	Not-Tuned

Table 2. Simulation results of the load variation effect. The corresponding PAE and output power are shown for both cases of tuned and not-tuned circuit.

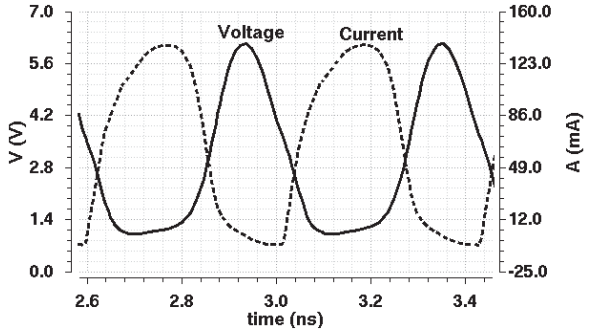


Fig. 3 Drain voltage (solid) and current waveforms (dash) of the proposed class-F PA.

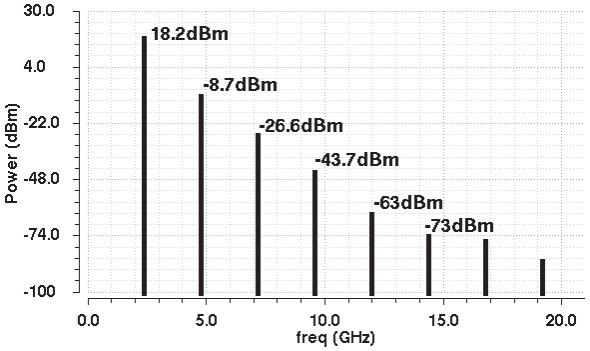


Fig. 4 Output power spectrum for 50 Ω load impedance. It shows a 2nd and 3rd harmonic rejection of 26.9 dBc and 44.8 dBc respectively.

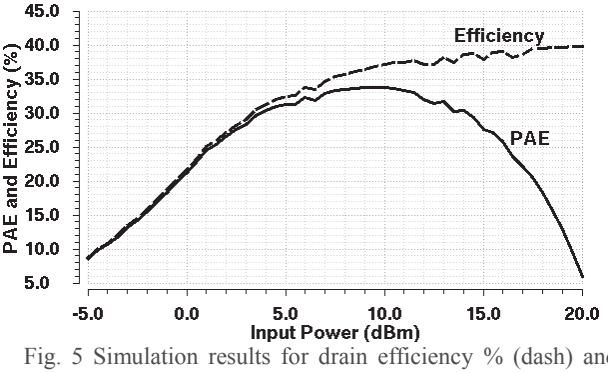
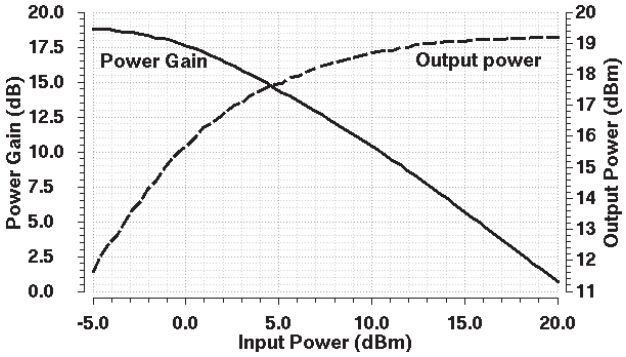


Fig. 5 Simulation results for drain efficiency % (dash) and PAE % (solid) versus input power.



(b)

Fig. 6 Simulation results for delivered output power (dash) and power gain (Solid) versus input power.

VI. Conclusion

In this work, a novel reconfigurable CMOS class-F power amplifier is proposed which can adapt to load variation caused by hand and body effect on the antenna. The load variation effect is compensated by using an impedance tuner in the load matching network. This tuner integrates two RF-MEMS variable capacitors in CMOS. The MEMS structure is integrated inside a CMOS technology and uses a mask-less post-processing technique. The power amplifier achieves a simulated drain efficiency of 34.6% and power gain of 12.9 dB, while delivering peak output power of 18.2 dBm for load impedance of 50Ω. The effect of load variations on PAE and output power are studied by simulating different load impedance values and in all of the cases a higher PAE and higher output power is achieved by the reconfigurable circuit. The total size of the die is 1.6 mm x 1.6 mm.

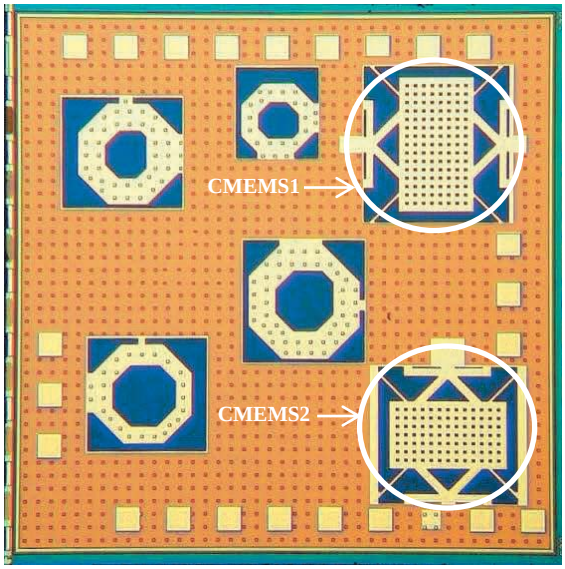


Fig. 7 Manufactured chip before post-processing. Chip dimensions are 1.6 mm x 1.6 mm.

Acknowledgement

This work was supported by the Spanish Government Project TEC2013-48102-C2-1-P and grant BES-2011-051305. The authors wish to thank the HIPICS research group of UPC, for their support to access the 0.18 µm CMOS technology and Cadence Software.

References

[1] S. C. Cripps, "RF Power Amplifiers for Wireless Communications," Artech House, 1999.

[2] T. C. Kuo, B. Lusignan, "A 1.5W Class-F RF Power Amplifier in 0.2µm CMOS Technology," *IEEE International Solid-State Circuits Conference, Digest of Technical Papers, ISSCC*, pp.154 – 155, Feb 2001.

[3] J.Carls, F. Ellinger, U. Joerges, M. Krcmar, "Highly-efficient CMOS C-band class-F power amplifier for low supply voltages," *Electronics Letters*, vol.45, no.24, pp.1240 – 1241, Nov 2009.

[4] F. Raab, "Class-F power amplifiers with maximally flat waveforms," *IEEE Transactions on Microwave Theory & Techniques*, vol. 45, no. 11, pp. 2007–2012, Nov 1997.

[5] M. Gilasgar, A. Barlabe, L. Pradell, "A very low distortion high efficiency class-F power amplifier at 900 MHz," *XXVIII Simposium Nacional de la Unión Científica Internacional de Radio* (URSI), Santiago de Compostela, Spain, 2013.

[6] M. Gilasgar, A. Barlabe, L. Pradell, "Highly Efficient Class-F RF Power Amplifiers with Very Low Distortion," *The Radio Science Bulletin*, (ISSN 1024-4530), no 347, pp. 21–31, Dec 2013.

[7] K. Boyle, M. Leitner, "Mobile phone antenna impedance variations with real users and phantoms," *2011 IEEE International Workshop on Antenna Technology (iWAT)*, Hong Kong, pp. 420-423, 2011.

[8] K. R. Boyle, Y. Yun, L. P. Ligthart, "Analysis of Mobile Phone Antenna Impedance Variations with User Proximity," *IEEE Transactions on Antennas and Propagation*, vol.55, no.2, pp.364–372, Feb 2007.

[9] T. Vähä-Heikkilä, K. V. Caekenberghe, J. Varis, J. Tuovinen, G. M. Rebeiz, "RF MEMS impedance tuners for 6–24 GHz applications," *International Journal of RF and Microwave Computer-Aided Engineering*, Volume 17, Issue 3, pages 265–278, May 2007.

[10] Z. Zhen, K. L. Melde, "Frequency Agility of Broadband Antennas Integrated with a Reconfigurable RF Impedance Tuner," *IEEE Antennas and Wireless Propagation Letters*, vol.6, no., pp.56 – 59, 2007.

[11] Y. Lu, L.P.B. Katehi, D. Peroulis, "High-power MEMS varactors and impedance tuners for millimeter-wave applications," *IEEE Transactions on Microwave Theory and Techniques*, vol.53, no.11, pp.3672 – 3678, Nov 2005.

[12] M. Bakri-Kassem, S. Fouladi, R. Mansour, "Novel High-Q MEMS Curled-Plate Variable Capacitors Fabricated in 0.35µm CMOS Technology," *IEEE Transactions on Microwave Theory & Techniques*, Vol. 56, No. 2, pp. 530–541, Feb 2008.

[13] S. Fouladi, M. Bakri-Kassem, R. Mansour, "MEMS Based RF Components with Vertical Motion and Parallel-Plate Structure and Manufacture Thereof Using Standard CMOS Technologies," *USA Patent US 7,858,423*.

[14] S. Fouladi, M. Bakri-Kassem, R. Mansour, "An Integrated Tunable Band-Pass Filter Using MEMS Parallel-Plate Variable Capacitors Implemented with 0.35 µm CMOS Technology," *IEEE MTT-S Int. Microwave Symposium Digest, Hawaii, USA*, pp.505 – 508, June 2007.

[15] M. Ben Hammouda, F. Domingue, M. Ahmed-Ouameur, "MEMS based tunable microwave amplifier design for reconfigurable PCS1900 mobile application," *2011 11th Mediterranean Microwave Symposium (MMS)*, pp.106 – 109, Sep 2011.