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Efficient Production Binning Using Octree Tessellation in the Alternate Measurements Space

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***Abstract*—Binning after volume production is a widely accepted technique to classify fabricated ICs into different clusters depending on different degrees of specification compliance. This allows the manufacturer to sell non optimal devices at lower rates, so adapting to customer's quality-price requirements. The binning procedure can be carried out by measuring every single circuit performances, but this approach is costly and time consuming. On the contrary, if alternate measurements are used to characterize the bins, the procedure is considerably enhanced. In such a case, the specification bin boundaries become arbitrary shape regions due to the highly non linear mappings between the specifications space and the alternate measurements space. The binning strategy proposed in this work functions with the same efficiency regardless of these shapes. The digital encoding of the bins in the alternate measurements space using octrees is the key idea of the proposal. The strategy has two phases, the training phase and the binning phase. In the training phase, the specification bins are encoded using octrees. This first phase requires sufficient samples of each class to generate the octree under realistic variations, but it only needs to be performed once. The binning phase corresponds to the actual production binning of the fabricated ICs. This is achieved by evaluating the alternate measurements in the previously generated octree. The binning phase is fast due to the inherent sparsity of the octree data structure. In order to illustrate the proposal, the method has been applied to a band-pass Butterworth filter considering three specification bins as a proof of concept. Successful simulation results are reported showing considerable advantages as compared to a SVM based classifier. Similar bin misclassifications are obtained with both methods, 1.68% using octrees and 1.83% using SVM, while binning time is 5X times faster using octrees than using the SVM based classifier.**

***Index Terms*—Production Binning, Specification Binning, Quality Binning, Alternate Test, Analog and Mixed-Signal Test, Quadtrees, Octrees, Classifiers, Feature Selection, Signature Selection, Quality Metrics, Analog Filter, Butterworth Filter.**

I. Introduction

FABRICATED ICs may present different degrees of specification compliance due to manufacturing process variations. Some devices exhibit excellent performance, therefore they are closer to nominal specifications, while others present worse performance, indicating they are far away from nominal specs. Specification based binning has been used as an efficient way of increasing production profit for digital circuits [1]–[5]. To this purpose, several binning goals are considered, traditionally, power consumption and speed [6], [7]. Similar concept has been applied for binning analog and mixed-signal circuits [6], [8].

Production testing of analog and mixed-signal circuits is an increasingly challenging task due to the presence of statistical variations related with the manufacturing process which directly affect circuit specifications [9], [10]. High amount of resources are solely dedicated to test and diagnose such devices to ensure that only specification compliant circuits are shipped to customers [10], [11]. One possible option to reduce these costs is to perform a specification based binning [6]. This allows the manufacturer to classify devices according to a quality criterion depending on how close the circuit is to nominal specifications [6].

Binning of mixed-signal circuits can be achieved by simply measuring the specifications as in classic specification based testing or by performing alternate measurements that correlate to actual specifications [12], [13]. Alternate testing techniques require a mapping between the specification space and the measurements space in order to allow the test decision to be performed. Artificial intelligence [14] and regression techniques [13], [15], [16] have been used with successful results to this purpose, as well as using octrees to represent the pass/fail regions [17], [18]. In this paper, octree data structures are used to encode the specification bins in the alternate measurements space.

The rest of paper is organized as follows. Section II presents the procedure for binning mixed-signal circuits using octrees in the alternate measurements space. Also, and due to the novelty of the application of octrees in this field, a brief introduction to the generation of octrees and their application to encode the bins in the measurements space is given. Section III defines some efficiency metrics to evaluate the resulting octree in terms of binning time estimation, incurred global bin escapes and noise impact. Section IV focuses on the application of the previously presented methodology to bin a 4th order Butterworth filter using alternate measurements [17], [19]. A criterion to select an adequate set of alternate measurements to avoid redundancy is presented. Section V reports the simulation results and presents the efficiency of the binning procedure using the previously defined quality metrics. The octree binning technique is compared to a state of the art classifier based on support vector machines. Finally, section VI summarizes the work and concludes the paper.

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II. Specification Based Binning of Mixed-Signal Circuits

The procedure of binning analog and mixed-signal circuits after volume production can be formalized as the classification of any candidate circuit into a cluster, according to certain circuit performances, among several possible disjoint bins. Such clustering is performed according to parameters of different nature.

The most common space for binning mixed-signal circuits is the *specifications space* in which circuit performances are directly measured and binned accordingly. Process variations may cause some circuits to violate or not fulfill the set of functional specifications related to certain bins. The effect of the uncertainties in the manufacturing process are modeled in this work by the statistical distributions offered by technology's process design kit in the *components space*. Direct measurement of circuit specifications is difficult and time consuming [10]. To overcome these drawbacks, the use of alternate measurements is widely adopted as an indirect and effective solution to test analog and mixed-signal ICs [13]. In this work, the term *measurements space* will be used to designate the alternate measurements which will facilitate the binning process. Fig. 1 sketches these three spaces and the bin boundaries defined according to certain specification levels.

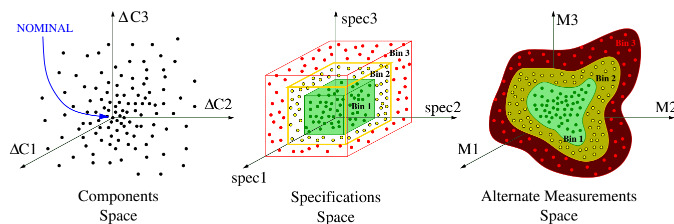

Fig. 1. Sketch of the three spaces considered in this work. Components space variability induce deviations in the specifications space as well as in the alternate measurements space in which the binning process takes place.

The proposed production binning methodology is performed in two phases, namely, training and binning phases. First, the training phase encodes the specification bins in the measurements space using octrees relying on circuit samples obtained by simulation, model evaluation or actual production data. After the training phase, the production binning is achieved by evaluating the alternate measurements of a candidate circuit in the previously trained octree data structure.

A. Training Phase

In order to encode the bins in the measurements space, a considerable amount of representative data need to be generated. This can be done entirely relying on simulations, circuit models or by using available data on the production run with already binned ICs. Of course, accelerating techniques for obtaining representative bin border circuits can also be used, such us statistical blockade [20], stratified sampling [21], copula theory [22] or estimating the probability density function using kernels [23]. The defined bins in the specification space will map to arbitrary regions in the measurements space which will be used for binning the forthcoming circuits.

As an example of circuit data generation in the measurements space, 10^4 Monte Carlo circuit samples of a 4th order band-pass Butterworth filter have been generated relying on HSPICE simulations. Fig. 2 shows these circuits in the measurements space where green points encode circuits fulfilling the specifications (bin 1), yellow points indicate circuits presenting marginal specifications (bin 2) and red points indicate circuits not satisfying all the specifications (bin 3). Further explanations on circuit specifications and bin definitions will be given in section IV.

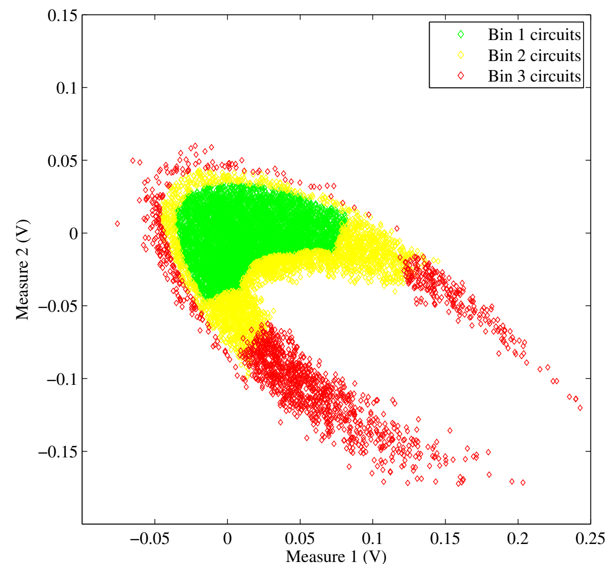

Fig. 2. Monte Carlo samples of a 4th order band-pass Butterworth filter in the measurements space. The circuit has been designed and simulated using an industrial 65 nm CMOS technology.

Once circuit data are generated, they need to be digitally encoded using an octree data structure. This data structure presents the advantage of being able to represent arbitrary n-dimensional regions and the capability of controlling its resolution by just limiting the maximum depth level. Such tree structures can be digitally represented and are easily evaluated using recursion. Next section describes how octrees can be created using circuit data samples.

B. Octree Encoding

Octrees have been extensively used in the field of computer graphics since they were proposed in [24]. Their main applications include texture rendering, image color quantization, object identification, and data clustering. In this work, octrees will be used to encode the specification bins in the alternate measurements space.

An octree data structure of dimension n is a tree in which each node has exactly 2^n children or none. Octrees are a particular case of k-ary trees, where $k = 2^n$. Octrees usually represent a geometric partition of a three dimensional space,

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hence each node has exactly 8 children, what gives its name. For the case of two dimensional applications, they also receive the name of quadtrees since each node has exactly 4 children. The concept can be easily generalized to n-dimensional spaces where sometimes are referred as 2^n-ary trees, or simply n-dimensional octrees, which is the term used in this work.

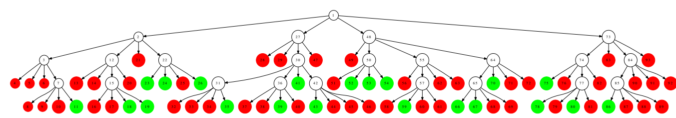

Fig. 3. Graph representation of the quadtree depicted in Fig. 4. For illustration purposes, only two bins have been considered, i.e. green and red. The resulting tree is 4 levels deep and has 93 nodes.

As an example of data encoding using octrees, consider the set of two dimensional alternate measurements shown in Fig. 4. The color of each pair of measurements indicate they belong to bin 1 (green) or bin 2 (red). Initially, and also during the whole process, the theoretical boundary separating both bins is unknown, so the presented algorithm is solely based on the alternate measurements. The encoding algorithm starts with the definition of a square cell (root node) including all the data to be considered in the training phase. Then, the square is tessellated in 4 equal regions by halving each dimension. Each of these 4 generated regions is further examined. If it exclusively contains single bin measurements, the square is tagged accordingly to that class and no further partitioning is needed. Otherwise, the square is marked as decision pending (white parent nodes in Fig. 3) and the tessellation/labeling procedure continues until all the generated squares only contain equal class measurements.

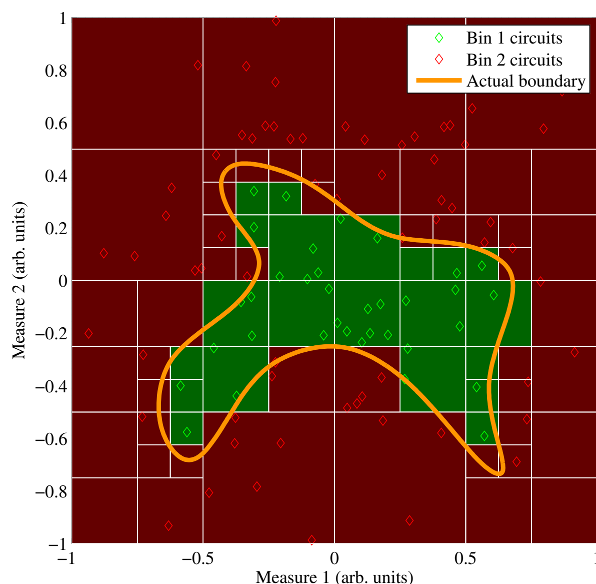

Fig. 4. Example of a quadtree generated using 100 bivariate Gaussian samples and two bins. The actual boundary separating both bins is represented by the thick orange line. The resulting quadtree is 4 levels deep and has the graph representation depicted in Fig. 3.

Depending on the underlying statistical distributions of the available alternate measurements, octree cells containing no data may occur in deep levels. In this case, unknown octree cells are labeled accordingly to the bin assigned to the majority of their neighboring cells.

C. Binning Phase

As mentioned earlier, the binning phase corresponds to the actual production binning of the fabricated ICs using the octree data structure encoded in the former training phase. The binning procedure is time efficient due to the sparsity of the octree as will be shown later.

Consider a pair of alternate circuit measurements, (M_1, M_2), corresponding to a fabricated circuit aiming to be binned using, for instance, the octree depicted in Fig. 4. The binning procedure is performed using the graph of Fig. 3. Assuming the pair of alternate measurements are within the initial square box (root node), the binning algorithm computes to which of the four quadrants the measurements belong to by performing one comparison per coordinate. This decision brings the candidate circuit to a new bound hence a new and deeper octree level is achieved. If the current node is labeled, the circuit is mapped to that bin and the evaluation finishes. If not, the evaluation algorithm repeats the comparison operation through the graph until a labeled node is found (tree leafs) and the circuit is binned. The pseudocode of the binning algorithm using octrees is listed in Fig. 5.

```
1:  function EVALMEASUREMENTS(N, M)
2:      Precond: N is an octree node data structure
3:      Precond: M is a vector of alternate measurements
4:      if N.label ≠ NULL then
5:          return N.label
6:      else
7:          idchild ← compare(M, N.center)
8:          N ← N.child[idchild]
9:          return EVALMEASUREMENTS(N, M)
10:     end if
11: end function
```

Fig. 5. Pseudocode of a recursive implementation of the binning process using octrees in the alternate measurements space. Octree evaluation is efficient since only one comparison per coordinate and level is required.

III. Efficiency Metrics

A. Binning Complexity Estimation

The process of binning analog and mixed-signal circuits using octrees can be formalized as an application between the n-dimensional alternate measurements space and natural numbers. That is, for any vector of alternate measurements, $M \in \mathbb{R}^n$, the octree maps it to a bin $b = \mathcal{O}(M) \in \mathbb{N}$,

$$\begin{aligned} \mathcal{O} : \mathbb{R}^n &\to \mathbb{N} \\ M &\mapsto b \end{aligned} \tag{1}$$

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Similarly, let $h(M)$ be the application mapping any vector of alternate measurements, $M \in \mathbb{R}^n$, to the maximum octree depth (or height) at that exact location. Under such definitions and according to the concepts and algorithm exposed in previous section, the number of comparisons, N_c, to bin a circuit using a vector of alternate measurements, M, turns to be $N_c = n\,h(M)$, i.e. one comparison per coordinate and level traversed. Moreover, if $\mathcal{P}(M)$ denotes the joint probability density distribution in the alternate measurements sample space $\Omega \subset \mathbb{R}^n$, the average number of comparisons to bin a circuit using the octree data structure is,

$$\widetilde{N_c} = n \int_{\Omega} h(M)\,\mathcal{P}(M)\,dM \ll n h_{\max} \tag{2}$$

Despite of the fact that the number of nodes of a sparse 2^n-tree grows exponentially with the dimensionality of the measurements space, is because of such inherent sparsity [17] that the average number of required comparisons is far below the theoretical upper bound $nh_{\max}$. This fact makes octree evaluation time efficient and easy to be digitally implemented as the algorithm listed in Fig. 5 clearly states.

B. Bin Escapes

As pointed before, the binning phase consists on the evaluation of a candidate circuit in the octree generated in the training phase, $b = \mathcal{O}(M)$, according to previously introduced notations. Certain circuits may be incorrectly binned due to insufficient octree resolution or noise in the measurements. Similarly to test escapes and test yield loss, a new metric to measure the quality of the binning procedure needs to be defined. Here forth, these circuits will be referred as *bin escapes*. In order to quantify this metric, let p denote the number of bins and let us define a $p \times p$ matrix $E = (e_{ij})$ referred from now on as the *bin escapes matrix*. Element e_{ij} in *bin escapes matrix* indicates how many circuits certainly belonging to bin i have been clustered into bin j. Then, the *global bin escapes* metric can be naturally defined as the sum of all the misclassified circuits as follows,

$$\mathrm{GBE} = \sum_{\substack{i,j=1 \\ i \neq j}}^{p} e_{ij} \tag{3}$$

Then, it is clear that the circuits accounted in the diagonal of the bin escapes matrix correspond to correctly binned circuits. On the contrary, circuits accounted above or below the diagonal of the bin escapes matrix are circuits that have been misclassified. Circuits above the diagonal are circuits classified in a worse performance bin than the actual circuits. On the contrary, elements located below the diagonal correspond to circuits classified in a bin being representative of better circuit performances than the actual circuit. Bin escapes matrix is being used in section V to evaluate the efficiency of the proposed binning procedure.

C. Noise Impact

Under realistic conditions, any circuit measurements is subjected to certain level of uncertainty, mainly due to the noise present in the measurements. Assume a voltage range V_{range} and a maximum uncertainty level in the measure of V_{noise}, what gives the dynamic range of the measurement, $\mathrm{DNR} = V_{\text{range}}/V_{\text{noise}}$. Since each octree level halves the range, it is clear that the resolution is $V_{\text{range}}/2^{h_{\max}}$, being $h_{\max}$ the maximum octree height. Given the previous definitions, it is clear that the maximum required octree depth under the mentioned noise conditions is $h_{\max} = \lceil \log_2 \mathrm{DNR} \rceil$.

If octree computation is stopped at level $h_{\max}$, even when circuit data is available to continue tessellating the space beyond level $h_{\max}$, the impact of noise can be quantified as the ratio of the decision pending cells hypervolume and the root node hypervolume. Of course, bin escapes will also reflect the noise impact since the values located above and below the diagonal of bin escapes matrix will increase. In the subsequently presented case study the impact of noise in the binning efficiency is also explored.

IV. Case Study: 4th Order Band-Pass Butterworth Filter

A. Specifications Space and Alternate Measurements Space

In order to show the viability of the proposed binning methodology using octrees, it has been applied to bin a 4th order band-pass Butterworth filter in the alternate measurements space. The Butterworth filter has been designed and simulated in an industrial 65 nm N-well bulk CMOS technology from ST-Microelectronics [25] as illustrated in the schematic shown in Fig. 6. The used topology corresponds to a multiple feedforward implementation [26] according to the design specifications shown in Table I.

The designed Butterworth filter has been tuned at 1 MHz with a 500 kHz bandwidth. Circuit components have been chosen to meet the aforementioned specifications and implemented using technology specific passive components as illustrated in Fig. 6. Resistors have been implemented using fixed width high resistance polysilicon resistors and capacitors using metal-insulator-metal capacitors. The sheet resistance of the used polysilicon resistors is approximately, $R_s = 6$ kΩ/□, while the capacitance of the used metal-insulator-metal capacitors is about 5 fF/μm^2.

TABLE I
Butterworth Filter Design Specifications

Design Specification	Symbol	Value	Units
Filter order	n	4	
Center frequency	f_0	1	MHz
Bandwidth (-3 dB)	BW	500	kHz
Band-pass gain	G	-3	dB

Even though the presented methodology can be naturally extended to an arbitrary number of bins, in this work only

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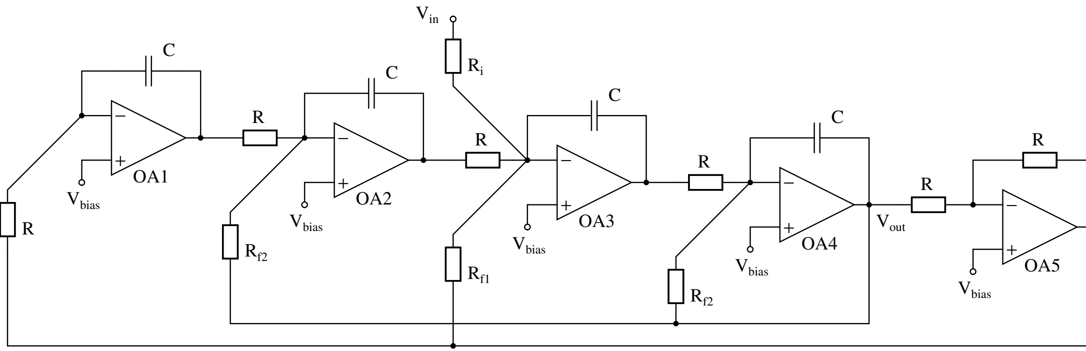

Fig. 6. Schematic of the 4th order band-pass Butterworth filter used as case study. The chosen topology corresponds to a multiple feedforward implementation [26]. The filter has been designed and simulated using a low-power standard-Vt 65 nm CMOS technology from ST-Microelectronics. Passive elements correspond to fixed width high resistance polysilicon resistors (rhiporpo) and metal-insulator-metal capacitors (mim). Components values are $R = 10$ kΩ, $R_i = 4R$, $R_{f1} = 0.444R$, $R_{f2} = 1.414R$ and $C = 15.9$ pF. Power supply for this technology is 1.2 V.

three bins have been considered as a proof of concept. Table II defines bin boundaries based on frequency/gain performances of every sample circuit. For instance, a circuit will be classified in bin 1 if and only if all the following conditions are satisfied: (1) the filter presents a gain less than -1.8 dB within the 262.8 kHz band-pass bandwidth, (2) it attenuates no more than -4.2 dB within the 262.8 kHz band-pass bandwidth and (3) it attenuates more than -49.0 dB at the stop-band corner frequencies (9.9 MHz bandwidth). Analogous reasoning applies for bins 2 and 3 according to the information shown in Table II.

TABLE II
BUTTERWORTH FILTER BIN LIMITS

Specification	Bins 1–2	Bins 2–3	Units
Pass-band bandwidth	262.8	530.8	kHz
Stop-band bandwidth	9.9	14.9	MHz
Max pass-band gain	−1.8	−1.4	dB
Min pass-band gain	−4.2	−10.8	dB
Min stop-band gain	−49.0	−56.0	dB

Circuit excitation is achieved by applying a single 3 tone input stimulus. The chosen tones correspond to filter's center frequency, an octave lower and an octave higher. The input-output composition can be considered as an analog signature characterizing the filter and its level of specification compliance [27]–[29]. Fig. 7 shows the input-output Lissajous composition for a nominal filter when it is excited using the aforementioned 3 tone stimulus as well as the Lissajous trace when the stimulus is applied to a filter affected by process variability. As demonstrated in previous works [27], Lissajous compositions serve as an indicator of circuit parametric deviations in linear analog filters.

Continuous trace information is compacted to a set of 10 evenly spaced (in time) voltage samples of filter response to the mentioned multitone stimulus as Fig. 7 illustrates. The selection of such points allows an easy and systematic approach facilitating further data processing while keeping most of the Lissajous trace information available to the forthcoming measurements selection criterion [30]. The actual alternate measurements correspond to the difference of the samples of the deviated response with respect to the nominal response.

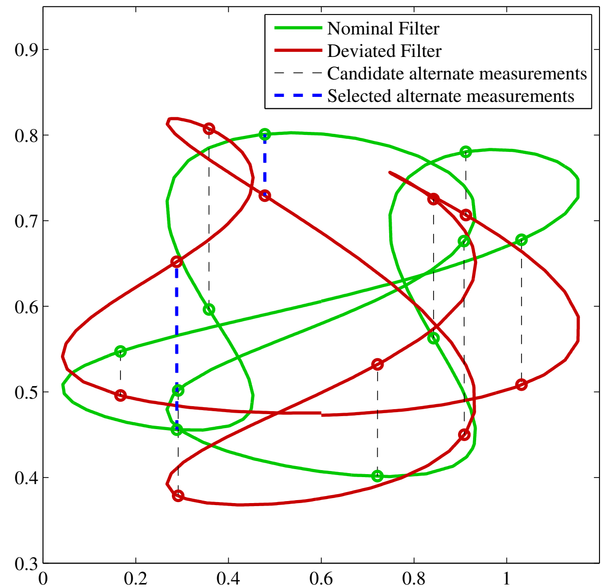

Fig. 7. Input-output composition when a 3 tone signal is applied to the band-pass Butterworth filter. Evenly spaced (in time) voltage samples form the candidate set of alternate measurements to be used in the binning process.

B. Alternate Measurements Selection Criterion

Last section defined the set of possible alternate measurements to be used during the binning procedure. As Fig. 7 illustrates, there are a total of 10 candidate alternate measurements to be considered.

It is quite clear that a set of alternate measurements to be used for binning purposes has to satisfy two main properties: (1) the measurements need to reflect circuit's performances variability in order to allow the binning to be performed efficiently and (2) an adequate set of measurements should not be redundant to avoid incurring in extra binning costs [31]–[33]. The first condition is achieved by means of a sensitivity analysis of candidate alternate measurements. Regarding the second condition, Kendall's Tau rank correlation coefficient [34] is used to rate the most adequate pair of measurements with the aim of reducing redundant information [35]. Kendall's

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Tau rank correlation coefficient computed between all the possible alternate measurements pairs of the Butterworth filter under study is shown in Fig. 8. The minimum absolute value of Kendall's Tau is 0.1126, highlighted in a white border and corresponds to measurements ids 9 and 7. Here forth, these measurements will define the alternate measurements space for the case study.

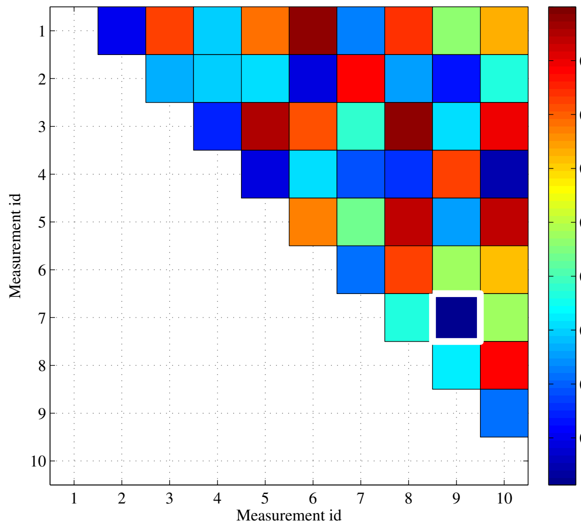

Fig. 8. Kendall's Tau rank correlation coefficients between all the possible pairs of candidate alternate measurements. The minimum absolute value is highlighted in white. Warm colors indicate high correlation while cold colors indicate low correlation.

The previous procedure has selected a pair of alternate measurements since two measurements are enough for characterizing the variability in this work. Despite of that, the method can be naturally generalized if more than two alternate measurements are needed. The proposed heuristic maintains the same criterion of minimizing the overall correlation within the target alternate measurements set. This can be achieved by minimizing the sum of the absolute values of Kendall's Tau of the chosen pairs.

Let N be the total number of candidate alternate measurements and $k \geq 2$ the number of alternate measurements to be selected for binning/testing purposes. Let T represent the absolute value of Kendall's Tau rank correlation matrix between all the possible pairs among the N candidate alternate measurements, i.e. $N(N-1)/2$ different elements. Then, apply the following greedy algorithm,

1) Choose the first pair of measurements in matrix T among the $N(N-1)/2$ different pairs presenting the minimum Kendall's Tau value.
2) Choose the next pair among the remaining pairs presenting the next minimum Kendall's Tau value, taking into account it will add one extra measurement if the chosen pair lies in the rows/columns of previously selected pairs and will add two extra measurements otherwise.
3) Continue applying the same procedure until the required alternate measurements are obtained to form the target set consisting of, at least, k measurements.

C. Training Phase

The proposed binning strategy using octrees has been applied to bin a 4th order band-pass Butterworth filter under the presence of process variations. As mentioned earlier, the circuit has been designed using and industrial 65 nm CMOS technology and simulated using HSPICE simulator. Monte Carlo simulations have been conducted relying on technology's process design kit (statcrolles corner) [25]. The set of obtained circuits clearly present different degrees of specification compliance. Fig. 9 shows in detail the obtained magnitude Bode plots together with the bin boundaries defined in Table II.

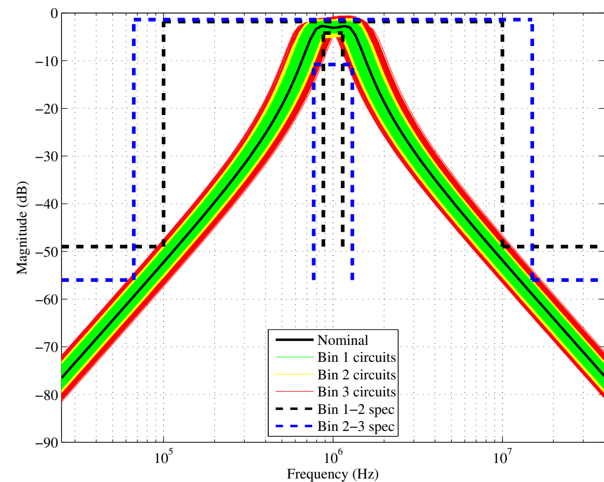

Fig. 9. Detail of the magnitude Bode plots generated using HSPICE Monte Carlo simulations of the Butterworth filter used as case study. The specifications boundaries defining each of the bins are also shown using discontinuous traces.

The training phase uses the measurements selected in previous section to encode the bins in the alternate measurements space using octrees. Fig. 10 shows the resulting encoding of the circuits shown in Fig. 2. Green, yellow and red octree cells correspond to bin 1, bin 2 and bin 3, respectively. The resulting octree has 14 levels in depth, i.e. $h_{\max} = 14$.

The resulting levels distribution for the encoded octree representing the alternate measurements space of the Butterworth filter is shown in Fig. 11. As can be appreciated, the vast majority of nodes correspond to levels 6, 7, 8, and 9 despite the maximum node level is 14. Further details will be given in the forthcoming sections, but this fact implies a considerable advantage in terms of binning time since a considerable amount of circuit samples will be binned without achieving a deep recursion level.

V. Simulation Results

A. Specification Based Binning Using Octrees

In order to evaluate the binning procedure using octrees, a new set of 50×10^3 Butterworth filters has been generated using Monte Carlo simulations and evaluated in the octree

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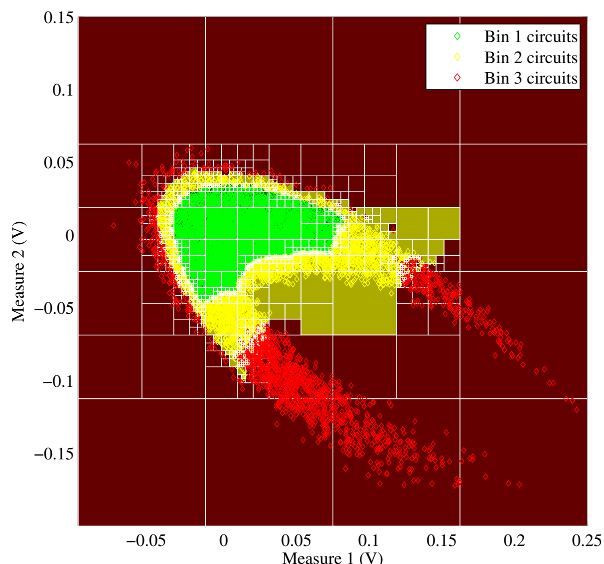

Fig. 10. Resulting octree after the application of the training phase to the set of 10^4 Butterworth filter samples shown in Fig. 2. As can be appreciated, high octree levels concentrate in bin boundaries, where a refinement is needed.

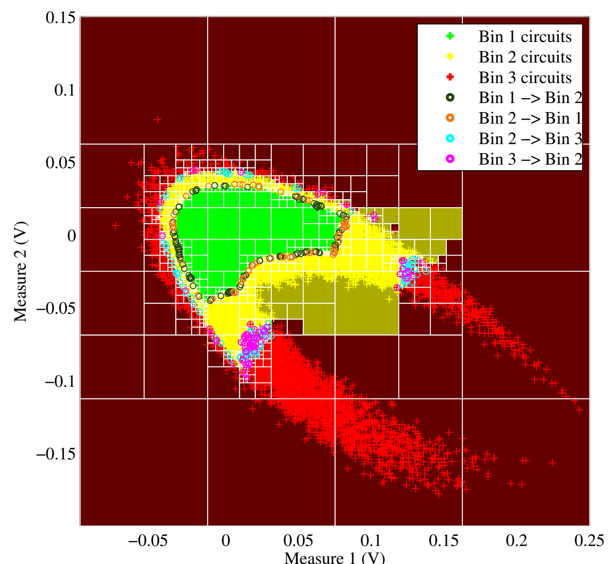

Fig. 12. Binning results using the testing set of 50×10^3 Monte Carlo circuit samples by means of the octree illustrated in Fig. 10 and generated in the former training phase. Misclassified circuits concentrate in bin boundaries.

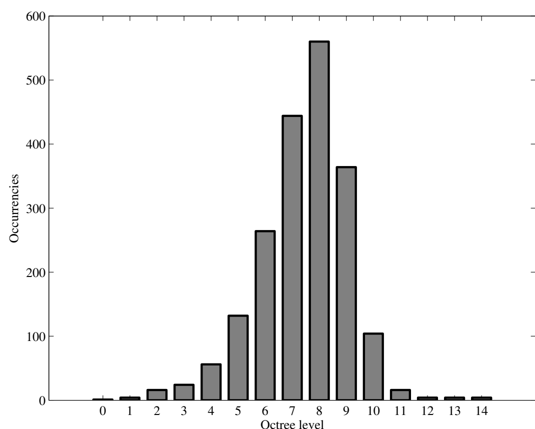

Fig. 11. Levels distribution for the octree shown in Fig. 10. Despite the maximum octree level is 14, the vast majority of octree cells correspond to levels 6, 7, 8, and 9, what greatly facilitates its evaluation in terms of binning efficiency.

TABLE III
BIN ESCAPES MATRIX FOR OCTREES BASED BINNING (%)

	Without noise			Gaussian noise $\sigma = 3$ mV		
	Bin 1	**Bin 2**	**Bin 3**	**Bin 1**	**Bin 2**	**Bin 3**
Bin 1	56.580	0.494	0.000	53.970	3.084	0.020
Bin 2	0.328	26.750	0.436	2.288	23.902	1.324
Bin 3	0.000	0.418	14.994	0.004	1.006	14.402
GBE	1.676%			7.726%		

generated in the training phase. The results of the evaluation can be observed in Fig. 12. Correctly binned circuits are drawn using green, yellow and red colors, which respectively correspond to bins 1, 2, and 3. Circuits that have not been correctly binned are circled using different colors according to the legend shown in Fig. 12. Table III reports the data characterizing the bin escapes matrix for the case study. As expected, the vast majority of bin escapes takes place between contiguous bins. Global bin escapes for this case study is 1.676% out of the 50×10^3 that form the binning set. The worst adjacent bin misclassification is 0.494%.

In order to study the time efficiency of evaluating the octree presented in section IV, all the required comparisons have been stored for the generated set of 50×10^3 circuits. Fig. 13 shows the cumulative percentage of binned circuits as a function of the required number of comparisons at a certain level. As can be observed, about 95% of the circuits are clustered by just performing 7 two-dimensional comparisons despite the octree is 14 levels deep. As suggested earlier, this implies a considerable benefit in terms of binning time since the octree data structure adapts its shape to the irregular bin boundaries generated in the alternate measurements space, only where a refinement is needed.

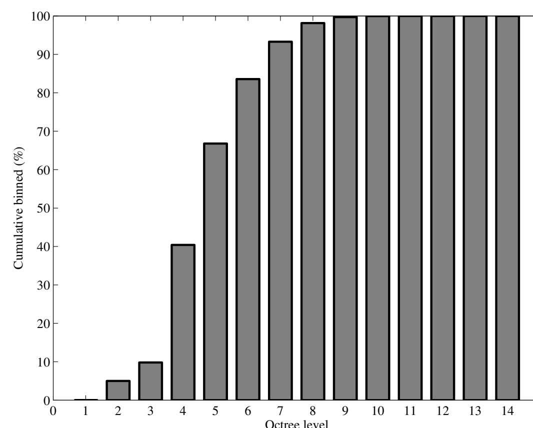

Fig. 13. Cumulative percentage of binned circuits as a function of the achieved octree level for the binning phase using 50×10^3 Butterworth filters. As can be observed, about 95% of the circuits are binned by just performing 7 comparisons.

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It has been mentioned that there are two main sources of bin escapes, namely, finite octree resolution and noise. The former issue has already been studied and simulation results have been reported. It basically depends on the required resolution which is also related with the number of samples used in the training phase. The latter issue, noise, is also of crucial importance thus resolution strictly depends on the DNR in a real world application. When noise is added, similar results to those presented in Fig. 12 are obtained, but numbers get degraded. Table III also reports information on a noisy binning scenario, where Gaussian noise has been added to the alternate measurements. In this case, the global bin escapes rises up to 7.726% being the worst adjacent bin misclassification 3.084% out of the total set of considered circuits.

Binning results for different noise levels added to the alternate measurements and different sizes of the training set are reported in Fig. 14. Global bin escapes is considerably affected when noise levels are increased, clearly showing a direct relationship between noise and GBE. Training set size also plays a noticeable role with respect to bin escapes. For the presented case study, if the training set consists of 10^3 circuits, the resulting octree represents the alternate measurements space poorly what translates in high GBE. On the contrary, if sample size is in the order of 10^4 or larger, the octree is sufficient to encode the bins in the measurements space.

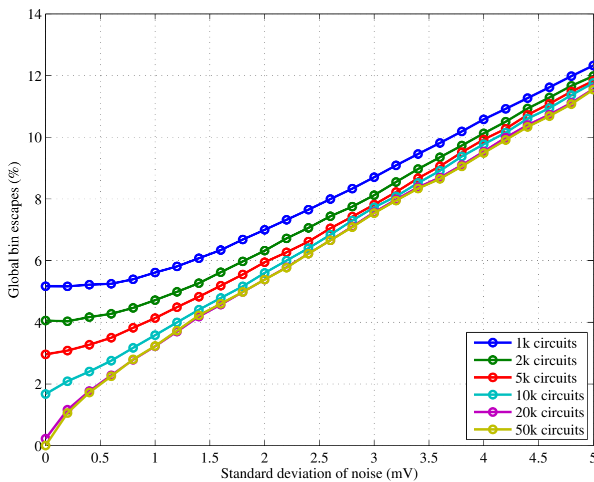

Fig. 14. Global bin escapes as a function of the number of circuit samples used in the training phase and the noise present in the alternate measurements. As expected, global bin escapes metric increases as noise level increases.

B. Comparison with Support Vector Machines Classifiers

In order to compare the proposed method for binning mixed-signal ICs with state of the art tools and techniques, a support vector machine (SVM) classifier has been trained using exactly the same set of circuits used for octrees which is depicted in Fig. 2. The training procedure has been carried out using MATLAB and the sequential minimal optimization training method. The kernel used in the procedure is a radial basis function (RBF), which is a standard choice in the field [36]–[38]. The SVM training has been carried out using a 5-folds cross validation together with a grid search to determine the optimum kernel spread, σ, as well as the optimum soft margin parameter, C. A single SVM classifier is capable of dealing with two classes only, so for binning circuits in p bins, $p-1$ support vector machines need to be trained. In this work, two SVM classifiers have been trained, one for separating bins 1-2 and one for separating bins 2-3. The results for the grid search can be seen in Fig. 15.

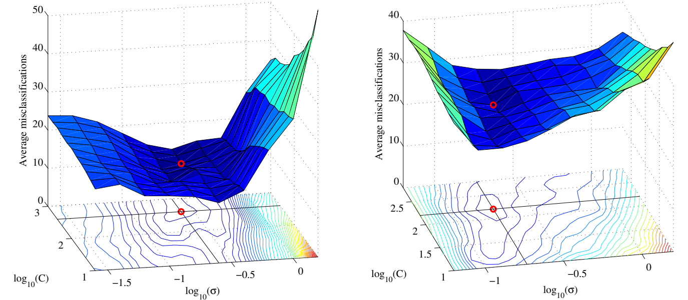

Fig. 15. Results of the grid search in the (σ, C) space using 5-fold cross validation technique with the training set presented in Fig. 2. The plot on the left corresponds to the SVM between bins 1-2 while the plot on the right corresponds to the SVM between bins 2-3.

The cross validation procedure together with the grid search method to determine the best σ and C parameters yields to the optimum support vector machines to be used. Table IV reports the training results for the two SVM classifiers trained using the same training set as used with octrees (10^4 samples). The whole SVM training process takes 1.5 h. The resulting optimum SVM classifiers boundaries are shown in Fig. 16.

TABLE IV
SVM CLASSIFIERS TRAINING INFORMATION

Aspect	SVM 1-2	SVM 2-3	Units
Training set size	10k	10k	ckts
Number of grid search points	110	100	
Cross validation folds	5	5	
Optimum σ parameter	0.2512	0.1848	
Optimum C parameter	398.1	158.5	
Average misclassification	12.6	25.0	ckts
Number of support vectors	180	623	
Single SVM training time	6.64	6.44	s
Total training time	53.7	38.7	min

Table V summarizes the results of the comparison between the production binning using octrees and using support vector machines. Regarding the training phase, the training using SVM is considerably longer, specially if the cross validation and grid search needs to be performed. The global bin escapes for octrees and SVM are similar, accounting for 1.676% if octrees are used and 1.828% if SVM classifiers are used. The time needed to achieve the binning for the 50×10^3 circuits was around 5 times faster using octrees than support vector machines classifiers. This strictly depends on the number of support vectors resulting after the training phase for the case of SVM classifiers while it only depends on the average octree level for the case of octree classifiers.

Table VI reports the bin escapes matrix for the binning procedure using the trained SVMs. The left hand side table

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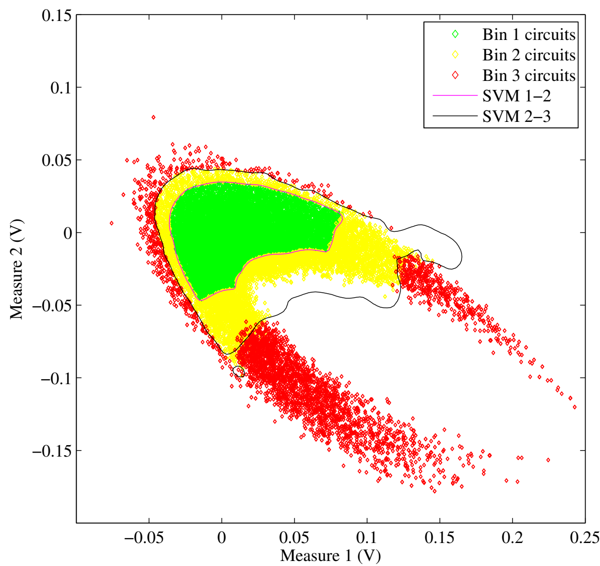

Fig. 16. Best SVM classifiers using the training set of 10^4 circuits shown in Fig. 2. The SVM has been trained using sequential minimal optimization method and radial basis functions (RBF) kernels.

TABLE V
COMPARISON BETWEEN OCTREES AND SUPPORT VECTOR MACHINES

Aspect	Octree	SVM
Grid search and cross validation time	not needed	1.5 h
Single classifier training time	1.3 s	13 s
Production binning time	19.2 s	99.8 s
Global bin escapes	1.676 %	1.828 %

corresponds to the ideal classification with no noise while the right hand side table reports the bin escapes matrix when Gaussian noise is added. Under the presence of noise, octree global bin escapes represent the 7.726% out of the total circuits while SVM wrongly bins the 7.660%, showing almost equivalent performances. It is important to note that non linear support vector machines rely on a minimization algorithm which may not converge immediately. Furthermore, SVM classifiers depend on several tuning parameters which require specific parameter selection and may result in non optimal classifiers. On the contrary, the octree encoding algorithm is straightforward to implement and solely relies on the available data.

TABLE VI
BIN ESCAPES MATRIX FOR SVM CLASSIFIER (%)

	Without noise			Gaussian noise $\sigma = 3$ mV		
	Bin 1	**Bin 2**	**Bin 3**	**Bin 1**	**Bin 2**	**Bin 3**
Bin 1	56.688	0.3860	0.000	54.078	2.980	0.016
Bin 2	0.204	26.234	1.076	2.244	23.464	1.806
Bin 3	0.000	0.162	15.250	0.004	0.610	14.798
GBE	1.828%			7.660%		

VI. CONCLUSIONS

A specification based binning strategy for mixed-signal circuits using octrees in the measurements space has been proposed. The method comprises two phases, training and binning. The training phase digitally encodes the specification bins in the measurements space using octrees. It is based on a set of circuits obtained from Monte Carlo simulations, model evaluation or available data on the production run. The generation of the octree in the training phase may be computationally intensive but it only needs to be performed once. Its size, i.e. the number of tree nodes, grows exponentially with the number of alternate measurements used (n). Our experiments show acceptable tree sizes for low dimensionalities ($n = 2, 3$). The binning phase performs circuit binning according to the octree generated in the previous phase taking advantage of the inherently sparse octree data structures.

In order to show the viability of the proposal, a Butterworth filter has been designed in an industrial 65 nm CMOS technology and binned using octrees. Monte Carlo simulations have been conducted to evaluate the bin escapes as a function of several parameters such as the training set size and noise levels. Simulation results reveal that worst adjacent bin misclassification is 0.494% out of the total set of circuits when no noise is considered. The octree binning procedure has been compared against state of the art support vector machines classifiers revealing considerable advantages in terms of evaluation complexity showing a speedup of 5X and slightly better misclassification results for the considered two-dimensional case study, therefore assessing the viability of the proposal for circuit binning based on a small number of alternate measurements.

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