FPGA DEVELOPMENT FOR MEASURING DIFFERENTIAL PHASE IN REAL TIME

A Thesis Presented

by

CRISTINA LLOP VALLVERDÚ

Submitted to the Graduate School of the
University Politecnic of Catalunya ETSETB in partial fulfillment
of the requirements for the degree of

MASTER OF SCIENCE IN ELECTRICAL ENGINEERING

June 2015

Electrical and Computer Engineering

FPGA DEVELOPMENT FOR MEASURING DIFFERENTIAL PHASE IN REAL TIME

A Thesis Presented

by

CRISTINA LLOP VALLVERDÚ

Approved as to style and content by:

Paul R. Siqueira, Chair

To my husband, mom and dad

Nothing in life is to be feared,
it is only to be understood.

Marie Curie

COLLABORATION

This project was started in March 2009 at the University of Massachusetts at Amherst −UMASS− (Amherst, Massachusetts, USA) and funded by the Advanced Component Technology program, NASA´s Earth Science Technology office.

The research involved in this thesis was conducted at the Mircowave and Remote Sensing Laboratory (MIRSL) at UMass.

From October 2011 to August 2012 this project has been continued by the author of the current thesis, Cristina Llop Vallverdú (cristinallv@gmail.com) and under the supervision of Dr. Paul Siqueira.

ACKNOWLEDGMENTS

I would like to extend my sense of gratitude to my husband Marc, parents Mª Dolors i Ramon and family for their encouragement and support to pursue the last part of my Master at UMass Amherst. I would like to thank to my advisor, Dr. Paul Siqueria for his continuous guidance and support, for giving me the opportunity to go through this learning process in both my personal and professional life; perhaps more for his guidance, patience and confidence in my abilities. The process of learning, better yet, the process of learning to learn and to appreciate things- small and big, simple and intricate have left a gratifying feeling in me. Also I would like to thank Dr. Stephen Frasier for giving me the chance of being here working at the Microwave Remote Sensing Lab, I have had an enjoyable and rewarding time being part of this group. I would like to acknowledge the help and the incredible patience of Justin Lu and the Latino corner, Jorge Salazar, Jorge Trabal and Rafael Medina.

Finally, I would like to thank all professors from UPC specially to professors Lluis Prat, Josep Colomines and Ramon Alcubilla and labmates with whom I have shared numerous technical discussions, long days and long nights in the lab. Thanks to Miquel, Tery, Àlex, Santi and Roger for all these good memories without you it would had never been the same.

And the last but not the least I would like to mention all the people that I meet during this great experience, people of the MIRSL, Mr. Chen, Haçer and Nina.

ABSTRACT

FPGA DEVELOPMENT FOR MEASURING DIFFERENTIAL PHASE IN REAL TIME

JUNE 2015

CRISTINA LLOP VALLVERDÚ

B.E., UNIVERSITY POLITECNIC OF CATALUNYA - ETTAC

M.Sc., UNIVERSITY POLITECNIC OF CATALUNYA - ETSETB & UNIVERSITY OF MASSACHUSETTS

M.S.E.C.E., UNIVERSITY OF MASSACHUSETTS AMHERST

Directed by: Professor Paul R. Siqueira

Technology assessment and proof of concept prototypes are necessary first step before any new concept and idea can be deployed as a fully proved on-board system. In this approach a radar cross-track interferometer has been constructed along with an integrated digital processing system capable of monitoring temperature and other operating conditions in order to design and test a new generation of radar systems with higher resolution level and a wider swath.

Cross-track interferometry is a remote sensing technique that relays on the measurement of phase difference between two data channels to infer characteristics about the target being observed. This type of radars are primarily sensitive to phase and changes in the transmitter characteristics where small differences in temperature can affect the overall performance of the system. Particularly, this thesis is based on the RF receive system of a radar that operates at a frequency of 35.75 GHz (wavelength (λ) of 8.4 mm). High frequency means that small fluctuations on the temperature in the two receive channels will manifest themselves as changes in the electrical path length. In this instance, phase differences not related with the measured topographic height will appear, possibly lading to significantly- increased error in the overall system.

To address the thermally-induced phase error issue, an adaptive digital receive system have been implemented into a Filed-Programmable Gate Array (FPGA) capable, not just, of measuring and monitoring continuously the phase but also identifying the accuracy of the

RF front-end's performance as a function of temperature and compensate these thermally-induced errors in real time.

The complete system, the combination of RF and the adaptive digital receive system has been designed and constructed as part of the National Aeronautics and Space Administration (NASA) Surface Water Ocean Topography (SWOT) initiative.

RESUM

FPGA DEVELOPMENT FOR MEASURING DIFFERENTIAL PHASE IN REAL TIME

JUNE 2015

CRISTINA LLOP VALLVERDÚ

B.E., UNIVERSITY POLITECNIC OF CATALUNYA - ETTAC

M.Sc., UNIVERSITY POLITECNIC OF CATALUNYA - ETSETB & UNIVERSITY OF MASSACHUSETTS

M.S.E.C.E., UNIVERSITY OF MASSACHUSETTS AMHERST

Directed by: Professor Paul R. Siqueira

L'avaluació tecnològica i la prova de prototips conceptuals és el pas previ necessari per l'implementació final del disseny en un sistema. Seguint aquest enfocament s'ha dissenyat una primera versió d'un radar cross-track interferometer, el qual incorpora un sistema de processat digital integrat capaç de controlar les fluctuacions de temperatura sobre el hardware del sistema de recepció RF i altres condicions de funcionament del sistema.

Cross-track interferometry és una tècnica de teledetecció basada en la mesura de la diferència de fase entre dos canals de dades per inferir característiques de l'objectiu. Aquest tipus de tècnica és principalment sensible a la tempreatura, on petites variacions d'aquesta en l'etapa de transmissió o recepció poden provocar canvis en la mesura de fase i el rendiment global del sistema. En particular, aquesta tesi es basa en l'etapa de recepció RF d'un radar que opera a freqüència 35,75 GHz (longitud d'ona (*lambda*) de 8,4 mm). El funcionament a freqüències elevades provoca que, petites fluctuacions de temperatura en l'etapa de recepció del senyal, es manifestin com canvis en la longitud del camí elèctric. En aquest cas, la diferència de fase no és deguda a l'açada topogràfica del terreny, provocant un increment significatiu en l'error sobre tot el sistema global.

Per abordar aquest problema s'ha dissenyat un sistema adaptatiu digital implementat sobre una Filed-Programmable Gate Array (FPGA) capaç, no tant sols de mesurar i monitoritzar la fase sinò també de compensar en temps real els errors sobre aquesta produïts per les fluctuacions de temperatura.

El sistema complet, la combinació del subsistema RF i el subsistema de recepció digital adaptable ha estat dissenyat i construït com a part del projecte Surface Water Ocean Topography (SWOT) iniciativa de la National Aeronautics and Space Administration (NASA).

RESUMEN

FPGA DEVELOPMENT FOR MEASURING DIFFERENTIAL PHASE IN REAL TIME

JUNE 2015

CRISTINA LLOP VALLVERDÚ

B.E., UNIVERSITY POLITECNIC OF CATALUNYA - ETTAC

M.Sc., UNIVERSITY POLITECNIC OF CATALUNYA - ETSETB & UNIVERSITY OF MASSACHUSETTS

M.S.E.C.E., UNIVERSITY OF MASSACHUSETTS AMHERST

Directed by: Professor Paul R. Siqueira

La evaluación tecnológica y prueba de prototipos conceptuales es el paso previo necesario para la implementación final del diseño en el sistema. Siguiendo este enfoque se ha diseñado una primera versión de un radar cross-track Interferometer el cual incorpora un sistema de procesado digital integrado capaz de controlar las fluctuaciones de temperatura sobre el hardware del sistema de recepción y otras condiciones de funcionamiento del sistema.

Cross-track interferometry es una técnica de teledetección basada en la medida de la diferencia de fase entre dos canales de datos para inferir característcas del objetivo. Este tipo de técnica es principalmente sensible a la tempreatura, donde pequeñas variaciones de esta en la etapa de transmisión o recepción pueden provocar cambios en la medida de fase y el rendimiento global del sistema. En particular, esta tesis se centra en la etapa de recepción RF de un radar que opera a la frequencia de 35,75 GHz (longitud de onda (λ) de 8,4 mm). El funcionamiento a elevadas frequencias provoca que, pequeñas fluctuaciones de temperatura en la etapa de recepción de la señal recepciónó se manifestó a sí mismos como cambios en la longitud del camino eléctrico. En este caso, las diferenciasé cias de fase que no están relacionados con la altura topográfica grabe a fico medida se muestra, posiblemente embarque para incrementado significativamente-error en el sistema global.

Para abordar este problema se ha diseñado un sistema digital adaptativo implementado sobre una Filed-Programmable Gate Array (FPGA) capaz, no sólo de medir y monitorizar la fase sinó también de compensar en tiempo real los errores sobre esta producidos debido

a las fluctuaciones de temperatura.

El sistema completo, la combinación del subsistema RF y el subsistema de recepción digital adaptable ha sido diseñado y construido como parte del proyecto Surface Water Ocean Topography (SWOT) iniciativa de la National Aeronautics and Space Administration (NASA).

CONTENTS

Page

LIST OF TABLES

Table **Page**

LIST OF FIGURES

Figure **Page**

CHAPTER 1

INTRODUCTION

1.1 Surface Water and Ocean Topography mission of NASA

The Surface Water Ocean Topography (SWOT) mission is one of five second-tier Earth Observing Missions recommended by the National Research Council (NRC) Earth Science Decadal Survey published,*"Earth Science and Applications from Space: National Imperatives for the Next Decade and Beyond"* recommended the SWOT mission [6] in 2007. SWOT is a collaborative mission involving NASA and the French space agency, Centre National d'Études Spatiales (CNES) with a lunch date determined prior to 2015, but around 2020 [7].

The general idea of this mission is bring together the hydrology and oceanography communities toward a better understanding of the worlds oceans and its terrestrial surface waters. The synergies between this communities will lead to a new understanding of the ocean surface boundry layers and the deep ocean and, the distribution and dynamics of fresh water bodies. This knowledge will be fundamental to improve our understanding of the ocean's role in climate change.

The technical goal is provide high-resolution centimeter level accuracy measurements of ocean and fresh-water topography over a wider swath than what is currently available through more traditional altimetric methods which tend to be narrow-swath, and hence more difficult to generate mid- to large-scale for the target dynamics over both short and extended periods of time. For SWOT mission a wide-swath mapping instrument utilizes near-nadir fan-beam to perform radar interferometry which results in high-resolution and wide swath measures of topography.

To achieve the accuracies required by SWOT mission a Ka-band (35 GHz; 200 MHz bandwidth) cross-track interferometer, KaRIN, capable of provide single-look resolutions on the order of 5 meters in azimuth and 10-70 m in ground range is used. Measures of topography at these resolutions will be averaged to achieve 1 km_2 topographic estimations with accuracies of the order of centimeters in vertical height.

This instrument has two Ka-band Synthetic Aperture Radar (SAR) antennas placed at opposite ends separated by a fixed baseline of 10m yielding 50m spatial resolution over land and 1km spatial resolution over oceans with 10cm and 1cm height accuracies, respectively. The system measures in two swaths of 60-70km with an incident angle of $4_{\circ}$ and operates in ping-pong, or double-baseline mode, which alternates the transmission of high-power microwave energy between the two antennas that make up the interferometric baseline.

The block diagram in Figure 1.1 outlines the system that will be employed.

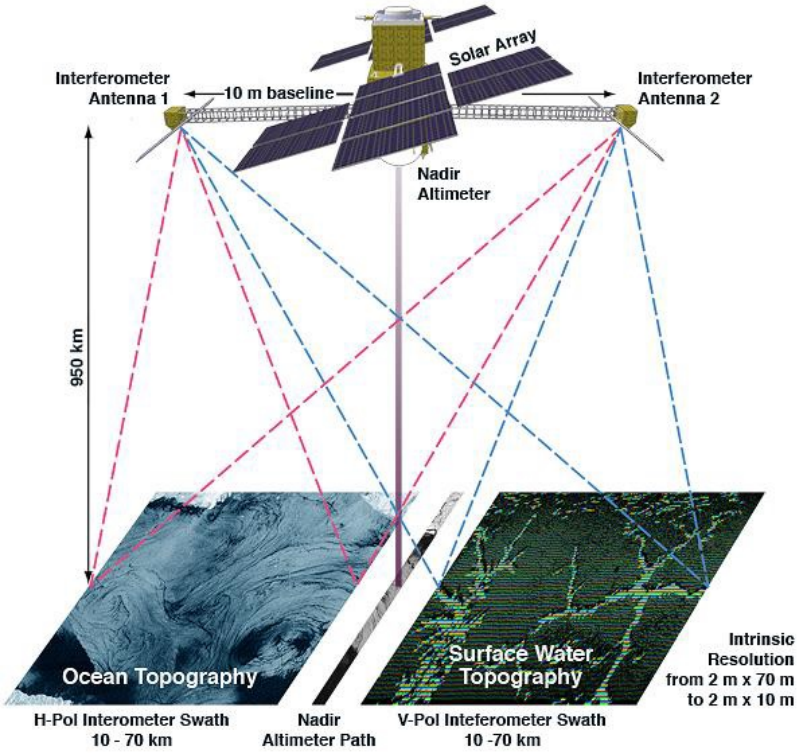

Figure 1.1. SWOT KaRIN Ka-band Radar Interferometer

Because the sensitivity of a radar interferometry to the topographic height is governed by the ratio of interferometric baseline to frequency, single-pass interferometric instruments are more compact (and able to fly on a single platform) compared to their lower frequency counterparts (e.g. L- or C-band interferometers), thus eliminating the error source associated with temporal decorrelation or the high cost of flying two satellite platforms simultaneously. With the advantage of flying a compact instrument on a single platform, comes an increased sensitivity of the interferometric phase to the mechanical and thermal aspects that govern the interferometer's observational geometry.

The technological challenges that Microwave Remote Sensing Laboratory (MIRSL) faces regards this project are:

- Design and construct a Ka-band downconverter with a 200 MHz bandwidth and digital output system capable of compensate the thermal variations that affect the bandpass performance.
- Minimize the power consumption while maintaining overall performance in terms of phase and amplitude stability over the passband as a function of temperature.
- Achieve a high-fidelity phase measurement implemented with a low computational overhead phase stability calculations.

To achieve the challenges described previously Figure 1.2 illustrate a high-level block diagram of the system proposed and designed. The on board computer transmit the information to the control, timing and waveform generator through the spacecraft bus and

this subsystem is responsible, among other things, to send the information to the processing and data storage and to control the transmit/receive switch. In order to send the required signal through the antenna subsystem, the RF upconversion subsystem translates this signal generated to Ka-band frequency.

On the receiver side, the signal received by the antenna subsystem is converted from Ka-band to L-band or baseband by the RF-downconverter circuitry and fed a high speed Data Acquisition System (DAS). The information processed is sent back to the on board computer through a communication bus.

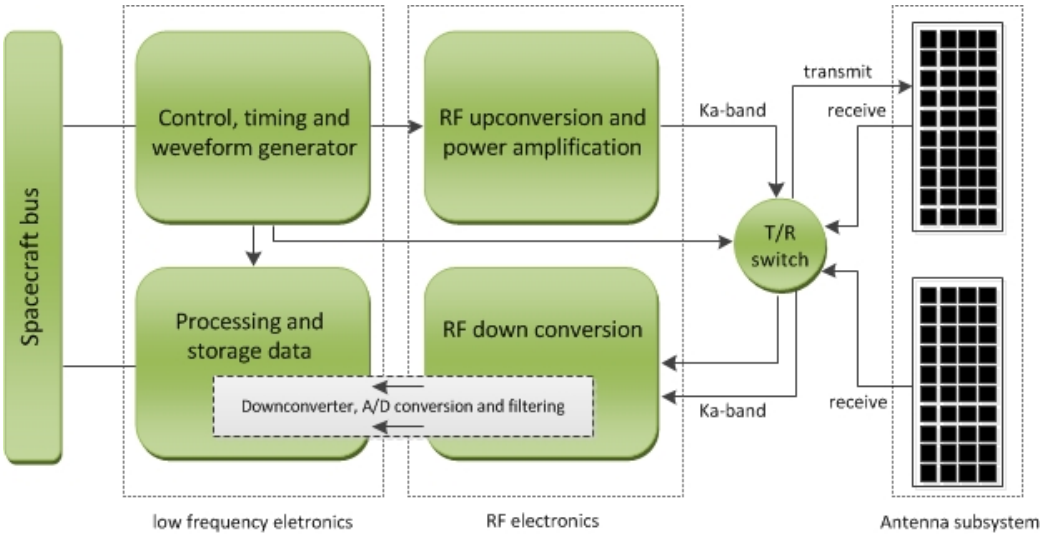

Figure 1.2. KaRIN System block diagram

1.2 Goal

This project builds upon the research from the "Real-Time Differential Signal Phase Estimation for Space-based Systems Using FPGAs" [3] and will continue the work done in [13], [9] and [11]. The primary goal of this thesis is to establish the communication between the temperature sensors located in the Ka-band dual downconverter, RF part, and the data acquisition system board. To attain the principal goal, the following objectives have been accomplished.

- Create the physical communications between the digital board and the RF boards within the constraints of the exiting hardware interface.
- Design a software algorithm to read data from the thermal sensors located on the downconverter in real-time and provide the capability to compensate for possible temperature deviations in the RF system.
- Adapt the existing phase detection algorithm and include taking into account the hardware limitations.
- Send the data collected to the storage resources. These can be to the hard drive through the SATA bus and/or serial port.

One outcome of this thesis will be an improvement on the data collected using a limited microcontroller, and integrate the digital system board created specially for this project. This will provide an opportunity to measure the overall system behavior, performance and accuracy but also limitations.

1.3 Summary of chapters

This thesis documents the description of the communications system between the RF dowconverter and the data acquisition system board and the temperature characterization of the RF downconverter system. The first chapter of thesis is an introduction to this thesis and the overall SWOT project. Chapter 2 contains the principle concepts of the radar interferometry field. Chapter 3 will consider a detailed description of the software and user interface used for programing the FPGA. Chapter 4 provides a better description of the communication system, the characteristics of the SPI protocol and its problems The general data acquisition ssystem is described in chapter 5. Finally, chapter 6 concludes with a summary of the work completed and provide some recommendations for future work.

CHAPTER 2

FUNDAMENTALS OF RADAR INTERFEROMETRY

Microwave Radar interferometry is an imaging remote sensing technique which can, in part, be used to measure surface topography, its changes over time, and other changes in the detailed characteristics of the surface. By exploiting the phase of a coherent radar signal, interferometry has transformed radar remote sensing from a largely interpretive science to a quantitative tool, with applications in cartography, geodesy, land cover characterization, vegetation estimation, and natural hazards.

Radar interferometers can be divided in two types based on the geometric configuration of the baseline vector as is shown in Figure 2.1.

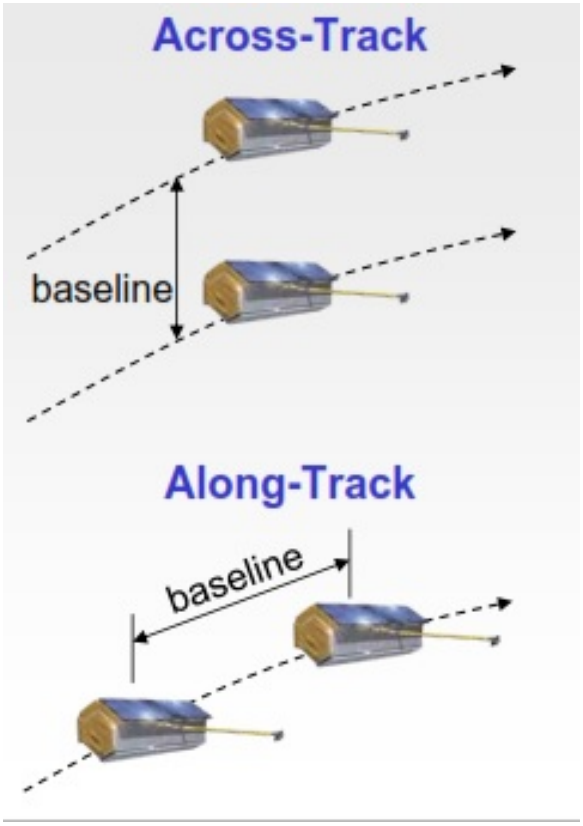

Figure 2.1. Depiction of the spatial extent of a resolution element giving geometric decorrelation

If the spatial baseline is oriented perpendicular to the flight track of the aircraft or spacecraft, in other words if the antennas are nominally separated in the cross-track direction

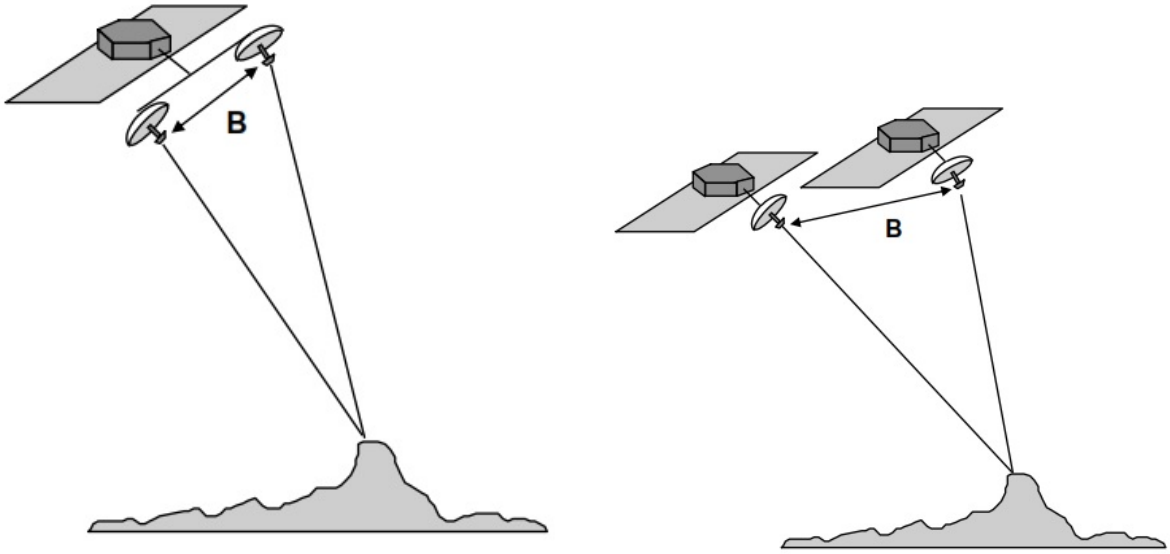

Figure 2.2. Single track configuration and Repeat track configuration

the interferometer is called **Cross-Track interferometer**. This configuration is used for topographic and surface deformations measurements. When the baseline is oriented parallel to the flight track, in other words the antennas are separated in the along-track direction, is called **Along-Track interferometers** and this type of configuration is used to measure radial velocity.

Depending on the application, radar interferometers can have different configurations. Figure 2.2 shows the Single Pass Interferometry (SPI) configuration where both radars (antennas) are located on the same platform and separated by the baseline distance which means, both antennas acquire data at the same time. The Repeat Pass Interferometry (RPI) configuration where the two radars (antennas) acquire data from different vantage points at different times. The time interval may range from seconds to years.

The two antennas can be configured in two modes of data collection. For Single Pass, the two modes of data collection are:

1. **Normal mode.** When only one of the antennas transmits and both receive.

2. **Ping-pong mode.** When each antenna transmits and receives its own echoes alternatively in time. Using this mode, the transmitted high-power microwave energy is alternated between antennas, improving the high accuracy of the interferometric measurements but also brings the phase stability of the transmit and receive systems in the overall height error.

These different instrument configurations can be used to achieve different functionalities. Cross-track single-pass and repeat-pass interferometers can be used to estimate topography and single pass along-track interferometers can be used to estimate the speed of water currents and mobile terrestrial targets. Specifically, the system explained in this thesis, SWOT, is a single pass across-track interferometer that operates in a ping-pong or double-baseline mode. [1]

2.1 Phase Estimation

Interferometry is a family of techniques where radio waves, usually electromagnetic waves, are superimposed in order to extract information about the relative changes in wave properties. Concretely, radar interferometry use the interference occurred when the phase measurements of two different waves are not aligned to reconstruct three-dimensional topography,as well as small changes to topography.

Each scattered single-channel radar signal can be represented by a complex scalar, equation 2.1 where a is the amplitude, ϕ the phase and λ is the carrier wavelength.

$$s_1 = a_1 e^{-i\frac{2m\pi}{\lambda \times 2R_1} + \phi_{S1}} s_2 = a_2 e^{-i\frac{2m\pi}{\lambda \times 2(\Delta R + R)} + \phi_{S2}} \tag{2.1}$$

The phase of the signal in Eq.2.1 has been decomposed in two parts: the first one corresponds to the propagation phase that depends on the distance between the radar and the scattering point R. The second part is the scattering phase that depends on the detailed nature of the scattering process.

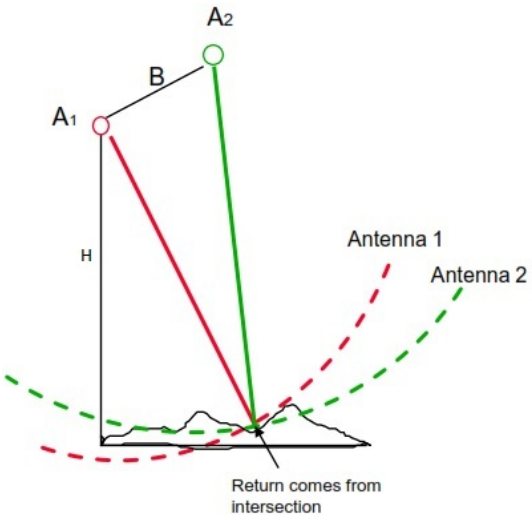

Figure 2.3. Geometry of an interferometry radar

Given the Figure 2.3, the two antennas A_1 and A_2 at an elevation h are separated by a baseline B and oriented at an angle α respect to local horizontal. The complete list description of key interferometry parameters are specified in Table 2.1.

The returning echo of the signal can be considered as a plane wave since the value of the range R is usually larger than the baseline distance B. The phase difference between observations can be written as 2.2

$$\Delta\phi = k\Delta R = \frac{2\pi\Delta R}{\lambda} \tag{2.2}$$

The interferometric phase variation $\Delta\phi$ is then proportional to ΔR divided by the transmitted wavelength λ or proportional to the free-space wavenumber, k.

Parameter	Description
θ	Look-angle with respect to nadir
θ_0	"Flat Earth" look-angle with respect to nadir
α	Baseline tilt angle
A_1	Antenna #1
A_2	Antenna #2
B	Baseline vector
R_1	Range to target from Antenna #1
ΔR	Range to target from Antenna #2
H	Height of the radar assembly
h	elevation of the terrain
Z(y)	Observation point
$P(\theta_0)$	"Flat Earth" observation point
r	Slant distance between Z(y) and $P(\theta_0)$

Table 2.1. Interferometric parameters

When two signals collected at the same point in space but with different polarization are combined to form an interferogram* the scattering phase term is canceled† and keep the geometrical phase, obtaining a signal phase that only depends on the difference in range phase between the two positions.

$$s1s_2^* = Ae^{-i(\frac{2m\pi}{\lambda}\Delta R)} \tag{2.3}$$

The factor m takes into account whether the range difference is only due to the receive path or due to both the transmit and the receive paths. In that case m is equal to 2 due too the ping-pong configuration.

This phase difference can be estimated by the coherence γ, which is the result of the cross-correlation between the complex coefficient of the electric field of two signals received at the two antennas, A_1 and 2.

$$\gamma = \frac{\langle V_1 V_2 * \rangle}{\sqrt{\langle |V_1|^2 \rangle \langle |V_2|^2 \rangle}} = \gamma_0^{-j\phi} \tag{2.4}$$

2.2 Height Estimation

Interferometric height reconstruction is the determination of the height of a scattering point *Z(y)*, h (see Figure 2.4) based on geometric expressions, knowledge of the components listed in table 2.1, and the interferometric phase. This phase-to-height conversion was the original motivation for the development of radar interferometry.

The height of the target in $Z(y)$ can be expressed as the result of applying the cosine law to the triangle $Z(y)A_1A_2$ shown in Figure 2.3.

*An interferogram is the result of the cross-correlation between the complex coefficient of the electric field of the two signals received at the two antennas.

†is a good approximation in practice assume that they are the same

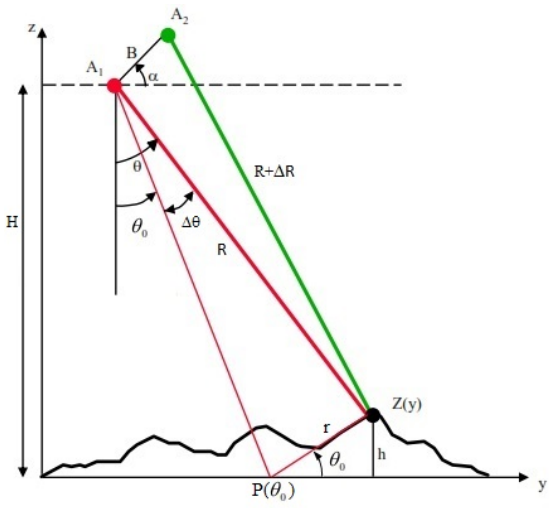

Figure 2.4. Geometry of an interferometry radar

$$h = H - R\cos(\theta) \tag{2.5}$$

Assuming far-field approximation for R, where baseline distance is smaller than the range $B << R$, it can be assumed that parallel plane waves are incident at both antennas and using the law of cosines based on the Figure 2.4 an approximate expression for the ΔR can be found

$$sin(\theta - \alpha) = \frac{(R + \Delta R)^2 - R^2 - B^2}{2BR} \Rightarrow \Delta R \approx -B\sin(\theta - \alpha) \tag{2.6}$$

By substituting (2.6) into (2.2), the expression for the interferometric phase in terms of the look angle holds:

$$\Delta\phi = k\Delta R = \frac{-2\pi B\sin(\theta - \alpha)}{\lambda} \tag{2.7}$$

Regrouping the terms of the expression (2.7(, θ can be expressed as,

$$\theta = \alpha - \sin^{-1}(\frac{\Delta\phi}{kB}) \tag{2.8}$$

From (2.8), a relationship between look-angle, θ, interferometric phase, ϕ, and baseline separation, B, can be shown. Thus, by substituting (2.8) into (2.5), a formula for height as a function of the measured interferometric phase can be expressed as,

$$h = H - R\cos(\alpha - \sin^{-1}(\frac{\Delta\phi}{kB}) \tag{2.9}$$

2.2.1 Interferogram flattening

The height estimated in (2.9) from the Figure 2.4 depends, among other parameters, on the ground topography and the local appearance of the Earth's surface from the prospective of the radar. As a result, the measured interferometric phase, shown in (2.7), can be written

as a sum of the phase quantities representing effects by both the ground topography and the "flat-Earth" look-angle (θ_0). Since these quantities are measured simultaneously by the radar. Can be expressed as

$$\Delta\phi = \phi_{topography} + \phi_{flat-Earth} \tag{2.10}$$

The look angle to a point on a "flat-Earth" is represented by θ_0. Then, θ can be written as $\theta = \theta_0 + \Delta\theta$. Based on that, equation 2.6 can be rewritten as follow

$$\sin(\theta - \alpha) = sin(\theta_0 + \Delta\theta - \alpha) \approx \sin(\theta_0 - \alpha) + \cos(\theta_0 - \alpha)\Delta\theta \tag{2.11}$$

In terms of the interferometric phase, the expression expands into the following form,

$$\Delta\phi \approx -\frac{2\pi}{\lambda} B \sin(\theta_0 - \alpha) - \frac{2\pi}{\lambda} B \cos(\theta_0 - \alpha)\Delta\theta \tag{2.12}$$

where the first term represents the phase difference measured for the "flat earth", i.e. in the absence of any topography. The operation to remove the phase difference due to the Earth's surface is called interferogram flattening and, as a result, it generates a phase map proportional to the relative terrain altitude leaving

$$\Delta\phi_{topography} = -\frac{2\pi}{\lambda} B \cos(\theta_0 - \alpha)\Delta\theta \tag{2.13}$$

2.2.1.1 Sensitivity of height with respect to phase

As shown in (2.9), the height of a certain point is obtained by triangulating range data collected from $Z(y)A_1A_2$. The altitude between two adjacent discontinuities is called the *altitude of ambiguity* (symbol h_a). This concept is defined as the elevation change required to change the flattened phase difference by one cycle, 2π, after interferogram flattening. The ambiguity height is computed from the interferometer parameters and is defined as follow,

$$h_a = \frac{\lambda R \sin(\theta_0)}{B_n \cos(\theta_0 - \alpha)} \tag{2.14}$$

Where B_n is the component of the baseline perpendicular to the look direction.

If the elevation in the scene varies by more than the ambiguity height, the phase will be "wrapped". The ambiguity height decreases when the baseline length increases. Having a small ambiguity height means good sensitivity to topography and increasing the frequency of the interferometer allows proportional reduction of the baseline, keeping the value other variables. The resolution in the cross-track direction is proportional to the bandwidth and high frequencies allowing higher bandwidth, achieving better resolution.

The altitude ambiguity is inversely proportional to the perpendicular baseline. The relationship between phase and target height is known as the *phase sensitivity*,σ_ϕ. The accuracy of the phase estimated, and therefore the height estimated obtained from it, is inversely proportional to the correlation between the two channels

$$\sigma_\phi^2 = \frac{1}{2N_L} \frac{1 - \gamma_2}{\gamma_2} \tag{2.15}$$

where N_L is the number of independent samples used to derive phase and γ is the measure of the correlation between the two channels.

2.3 Temperature dependence of differential phase

As probed in equation (2.12), signals can be decorrelated due to various factors listed below,

- Thermal and processor noise.
- Differential geometric and volumetric scattering.
- Rotation of the viewing geometry.
- Random motion over time.

One of the point's study of SWOT project at UMass is the temperature dependence of the phase and how compensate the phase deviations due to the temperature fluctuations. The concurrent measurements of the temperature and differential phase have shown a strong dependence between them.

Based on the previous thermal analysis of the RF downconverter system can be concluded that,

- Changes in the physical path length due to thermal expansion/contraction, will cause changes in the signal phase as well as temperature imbalances in active components.
- A one degree phase change is equivalent to 23 mm of electrical path length change. Integrated over 5 cm of total path length, this is equivalent to a 0.05% expansion coefficient, or 5 parts in $10,000$.
- Thermal imbalances between the two interferometric paths will thus induce a temperature dependent phase error.
- The temperature point measurements, shown in Figure 2.5,are unlikely to be sufficient to characterize the phase error, as they do not take into account the temperature distributions of the system or the thermal inertia of the chassis.

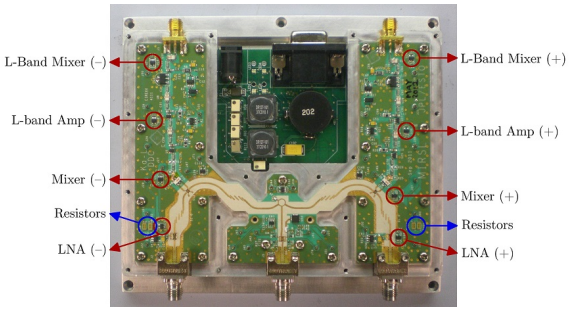

Figure 2.5. Location of temperature sensor in the downconverter phase

The temperature measurements are taken "on-board" which means, the phase error may be monitored in real-time and corrected in the digital stage.

CHAPTER 3

MICROBLAZE AND EMBEDDED DEVELOPMENT TOOLS

This chapter describes briefly the environment used to establish the software communication between the FPGA and the RF downconverter.

3.1 MicroBlaze Soft Processor

The main part of the overall system architecture is the soft microprocessor MicroBlaze supported by the Xilins XC4VFX140 Virtex-4 FPGA. The processor has high-speed instruction and data buses to guarantee access to instructions and data simultaneously. The relevant characteristics of the MicroBlaze are the 32-bit general purpose registers, the 32-bit instruction word with three operands and two addressing modes. Moreover the 32 bit address bus and the single issue pipeline.

In addition to these features, the soft core offers several configuration options in order to adapt its functionality to the requirements of the application to be developed [14].

The memory architecture of the microprocessor is called the "Harvard type", which indicated that the access to instructions and data are carried out in separate address spaces. Each address space has a range of 32 bits. Access to input / output, the processor has the same address space for memory and the input / output (i.e. devices input / output are mapped to memory). The processor has three interfaces for memory accesses:

- Local Memory Bus (***LMB***): The LMB is a synchronous bus used primarily to access on-chip block RAM. All operations on the LMB are synchronous to the MicroBlaze core clock. It uses a minimum number of control signals and a simple protocol to ensure that local block RAM are accessed in a single clock cycle.
- Processor Local Bus (***PLB***): The PLB is a fully synchronous bus that gives access to processor peripherals. The MicroBlaze PLB interfaces are implemented as byte-enable capable 32-bit masters.
- On-Chip Peripheral Bus (***OPB***). The MicroBlaze OPB interfaces are implemented as byte-enable capable masters.

The bus interface used in this project is the Processor Local Bus (***PLB***). Regarding the programming model of the microprocessor, one of the relevant aspects of the architecture are the usage of the bank registers and the internal mechanisms to deal with interruptions. In addition, MicroBlaze microprocessor specifies certain memory locations to treat interrupts and exceptions as:

- Reset hardware: 0x00000000
- Exception: 0x00000008
- Interruption: 0x00000010

3.1.1 Description of the OS. uC/OSII

μC / OS-II real-time operating systems, multi-tasking, scalable, portable, deterministic and priority scheme. Its most important features are:

- Multi-tasking: The operating system can handle up to 256 different tasks. Each task is assigned a unique priority, so there are a total of 256 priority levels.
- Scalable: It has been designed so that they use only the services that are needed for a particular application. This can reduce the amount of memory (ROM and RAM) that is needed by the operating system depending on the type of application.
- Portable: Most operating system is written in ANSI C, and only a small part (the need for access to records and to enable and disable interrupts) includes assembly code specific to a particular microprocessor.
- Deterministic: It is always possible to know how long the execution of a function or service. This is because the running time of most operating system services do not depend on the number of tasks that constitute an application.
- Outline priority (preemptive) operating system always executes the highest priority task that is ready to run.

3.2 Embedded Development Tools

An embedded system design is a complex task since it consists of the hardware and the software portions. Getting these portions of an embedded design to work are projects in themselves. In order to simplify the design process, several sets of tools are offered to assist in all phases of the embedded design. The tools available, at the time of this thesis, to simplify the process are shown in Figure below.

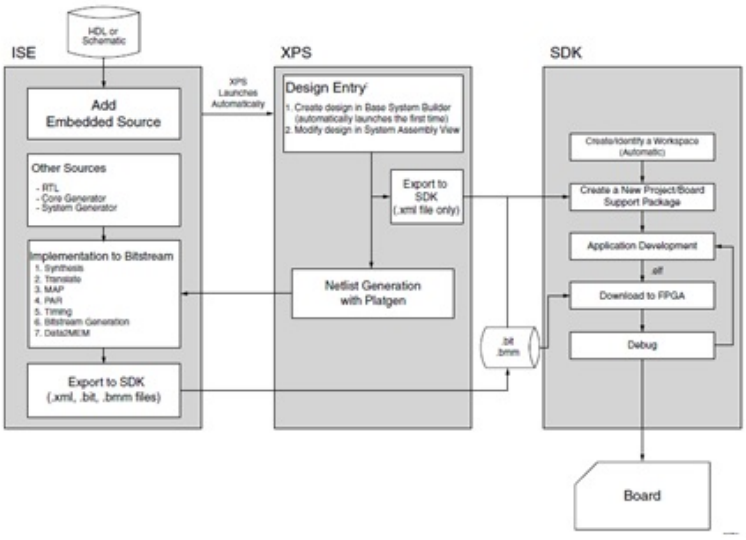

Figure 3.1. Flow diagram of an embedded design

Each one of these tools available used to develop this work are explained in the following sections.

3.2.1 Integrated Software Environment (ISE)

The Xilinx ISE [16] is the foundation for Xilinx FPGA logic design which controls all aspects of the design flow. Is used for design implementation, process of translating, synthesizing, mapping, place and route, optimization, timing and power analysis, and generating a bitstream file for a given embedded design as well as support for real-time in-circuit debugging of the programmed FPGA. The ISE can also be considered the bridge between the complete design and the FPGA device.

3.2.2 Embedded Development Kit (EDK)

The Xilinx embedded development kit (EDK) [15] is a suite of tools and collections of ready-to-use Intellectual Properties IP's (although some IPs can be modified to suite some specific use and/or application) used to design a complete embedded processor system for implementation in a Xilinx FPGA. The term IP here refers to commercially available capabilities that can be purchased individually. EDK allows designers to build a complete processor system on Xilinx's FPGAs. The systems that can be produced using EDK ranges from a simple single processor architecture to a complex multi-processor system with multiple hardware accelerators. The tool mainly supports two types of processors:

- ***PLB*Power-PC** which is a hardcore processor implemented in some FPGAs.
- ***PLB*MicroBlaze** which is a reconfigurable soft-core processor.

Depending on the FPGA chip used, multiple Microblazes and Power-PCs can be integrated together in a single design.

The development of any specific application by the MicroBlaze microprocessor consists of two distinct phases, the definition of the hardware platform system and the application software development. The first phase is carried out using the tool Xilinx Platform Studio (XPS), while the second is performed using the tool Software Development Kit (SDK).

Besides, using ISE, it is possible to perform several types of simulations for the generated architectures which allows the estimation of both the performance and the power consumption of the architecture.

3.2.2.1 Xilinx Platform Studio (XPS)

The Xilinx Platform Studio (XPS) is the development environment for designing the hardware portion of the embedded processor system. It allows customization of the logic platform hardware aspects such as processors, peripherals connected to the buses, and buses. Besides the standard IP cores available in the IP catalog, the XPS allows the creation of custom peripherals that can be included in the system.

XPS maintains the hardware platform description in a high-level form, known as the Microprocessor Hardware Specification (MHS) file. The MHS is an editable text file, is the principal source file representing the hardware component of your embedded system. XPS synthesizes the MHS source file into Hardware Description Language (HDL) netlists ready for FPGA place and route.

- Design environment for processor subsystem.
- Xilinx Microprocessor Project (XMP) file.
- Microprocessor Hardware Specification (MHS) file.
- Bus Functional Model (BFM) Simulation.
- ChipScope Pro logic analyzer integration.

3.2.2.2 Software Development Kit (SDK)

The Xilinx Software Development Kit (SDK) provides an environment for development, compilation and verification of C/C++ embedded software portion of the embedded system. It includes user-customizable drivers for all supported Xilinx hardware IPs, profiling tools that help to identify bottle necks in the code that might occur due to the interaction of functions that are executed within the programmable logic, and functions executed on the processor.

The SDK helps developing software for the hardware system defined in XPS. A Software Platform is the lowest level of the software stack that includes all the drivers and libraries components of the embedded system. Note that many applications can share the same software platform and the hardware platform must be imported into SDK prior to creation of software application and BSP.

CHAPTER 4

COMMUNICATION SYSTEM SPECIFICATIONS

4.1 Description of the overall RF system

The receiver part of the communication system consist in a two channel (I and Q) single-stage downconverter from Ka-band to L-band. The measures that have been taken to improve hardware isolation and thermal management towards thermal changes are

(i) each stage use a different PCB board, one for the low-frequency power and another for the telemetry sensors; (ii) both channels are highly symmetric in order to minimize the differences between channels to increase the phase stability; (iii) include a set of isolation cavities on the RF side which that cover the region with board with the microstrip filters, one-quarter inch wide via strips additionally separate the two interferometric channels (top and bottom) from the common LO distribution and power conditioning portion of the Ka-band downconverter board (middle section of Figure 4.1); (iv) incorporate a mechanical housing made to mate with these via-strips using a compressible conductive "shock", which forms a sufficient electric connection with the ground plane and to improve electromagnetic isolation between critical regions of the downconverter's architecture; (v) increase the number of telemetry sensors on board; (vi) include a method for actively influencing the temperature of the of the two down-conversion channels.

The different layers are shown in below Figure 4.1.

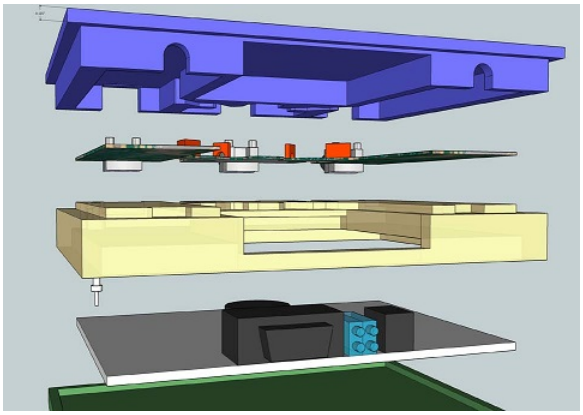

Figure 4.1. Closeup of the different layers of the Ka-band to L-band downconverter design. The RF board connects to the DC telemetry and power board through a set of Tusonix feed-through connectors. Different functional blocks of the downconverter (two channels and LO distribution) are isolated from one another by a set of drop down walls that mates with the lower part of the chassis

The following image 4.2 shows the Ka-band to L-band downconverter with all the layers mounted. It can be observed some of the improvements made. For example, the isolation cavities, the symmetry between channels or the mechanical housing.

Figure 4.2. Real image of the Ka-band to L-band downconverter

As explained before, interferometric measurement are sensitive to phase, electrical path length variations and changes in the transmitter/receiver characteristics will have a big impact on the derived science products. In order to monitor the variations of these values different temperature locations, current and voltage sensors have been mounted on the channel Ka-band receiver.

The Integrated circuit (I.C.) used to sense the temperature board on the different spots is the MAX6612 [4]. This sensor provide a voltage output proportional to temperature. Two of the important parameters of this sensor are the accuracy and the sensitivity. In terms of accuracy, the sensor provide a $\pm 1.2\,^{\circ}\mathrm{C}$ (max) at $+25\,^{\circ}\mathrm{C}$, $\pm 3.0\,^{\circ}\mathrm{C}$ (max) from $T_A = 0\,^{\circ}\mathrm{C}$ to $+70\,^{\circ}\mathrm{C}$, and $\pm 5.5\,^{\circ}\mathrm{C}$ (max) from $T_A = -10\,^{\circ}\mathrm{C}$ to $+125\,^{\circ}\mathrm{C}$. Regarding sensitivity, the output voltage to temperature is a high $19.53 mV/\,^{\circ}\mathrm{C}$.

For the current measure it had been used the LT6170 [2]. The values of the main characteristics of this sensor are the wide operating temperature range, between 2.7V to 44V with a maximum offset of $250\mu V$ and 40nA of maximum input bias current. Finally, the i.c. CHE1270-QAG [10] measure LO power signal. The principal characteristics are the sensitivity of 50 mV/dBm and 15 dBm as minimum input power.

The location on the board of each sensor and the temperature resistor is shown in Figure 4.3. Based on previously thermal studies [8] it has been proved that the amount of temperature sensors located in the board is not enough for the mainly purpose but it has helped to provide an idea of the thermal distribution through the RF system.

As it can be seen in the previous image, the temperature sensors are located along the paths of each channel (I and Q channel) and the two temperature control resistors are next to the LNA temperature sensor of each channel. The printed circuit board PCB layout can be found in Appendix A. The specific schematic location, description of the signal measured, type of sensor and which ADC is responsible to convert the value and the exact pin input is described in the Table 4.1.

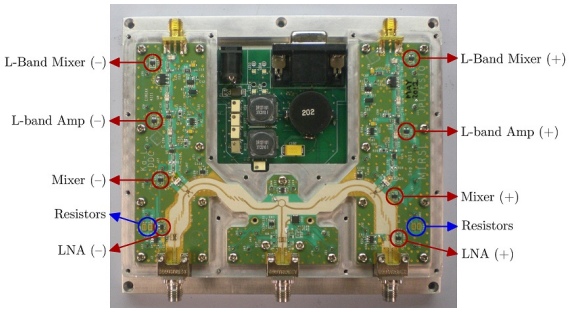

Figure 4.3. Temperature sensors locations and Temperature control resistors of the RF downconverter

4.2 Analog to Digital Converter. ADC

To transmit the information of the temperature, current and power sensors to the DAS it has been used the Analog to Digital Converter (ADC) MAX1168 [5].

The main 4 digital output signals of the i.c., corresponding with the main SPI communication bus, are the clock signal, *SCLK*, that drives the conversion process and clocks data out. The serial data output is *DOUT* (*MOSI* signal). This signals keep in high impedance when $\overline{CS}$ is high. The *DIN* is the serial data input used to communicate with the command/configuration/control register (it is considered the *MISO* signal). To show the end of conversion $\overline{EOC}$ is set low, it will remains high in the other steps of conversion. Finally, the active-low chip-select $\overline{CS}$ activates the normal operating mode after the initial transition form high to low and remains low for the entire conversion process.

Signals between AIN0 to AIN7 are corresponding with the analog value of each sensor. The rest of the signals does not concern this thesis because at the moment of this thesis, the physical implementation is already done and it does not affect the software part of the transmittion.

Regarding the operational modes offered by the ADC, due to the hardware characteristics available of the RF downconverter, the configuration used for this application is the $16-bit-wideData-transferandscanmode$. The scan mode configuration allows multiple channels to be scanned consecutively or one channel to be scanned eight times. With this mode, the conversion results are stored in memory until the completion of the last conversion in the sequence. Using the maximum word length available, 16-bit mode, provides a better resolution of the conversion. Once the ADC has been power-up, it has to be set up the register that contains the command/configuration and control information. The following Table 4.2 shows in detail each bit.

The first three bits, BIT7, BIT6 and BIT5 indicate the channel number to do the conversion. In this project, every time that one specific sensor has to be read, the register will be update with the sensor number. The information regarding the options of scan mode are set in BIT4 and BIT3. To set the power down mode with an internal reference and the reference buffer off between conversions is used BIT2 and BIT1. The last bit, BIT0, refers to the clock mode and the value "1" means that the will set by the internal clock. That way it will improve the functionality of the overall conversion. The power-up state is the default state of the ADC. Every time the ADC turn off the device resets the register to the power-on reset default state and the register has to be configured again if this default

PCB location	Signal description	Sensor type	ADC	Pin ADC
U45	Temperature LO AMP	MAX6612	ADC1	0
U50	Temperature LO FILT (-)	MAX6612	ADC1	1
U52	Temperature LO FILT (+)	MAX6612	ADC1	2
U57	Temperature DC BOARD	MAX6612	ADC1	3
U36	Temperature LNA (+)	MAX6612	ADC2	8
U37	Temperature MIXER (+)	MAX6612	ADC2	9
U38	Temperature L–BAND AMP (+)	MAX6612	ADC2	10
U39	Temperature L–BAND OUPUT (+)	MAX6612	ADC2	11
U16	Temperature LNA(–)	MAX6612	ADC2	12
U17	Temperature MIXER (–)	MAX6612	ADC2	13
U18	Temperature L–BAND AMP (–)	MAX6612	ADC2	14
U19	Temperature L–BAND OUTPUT (–)	MAX6612	ADC2	16
U53	LO PWR	CHE1270-QAG	ADC1	4
U65	Current SENSE LO	LT6107	ADC1	5
U61	Current SENSE RX (+)	LT6107	ADC1	6
U69	Current SENSE RX (–)	LT6107	ADC1	7

Table 4.1. Description and location of each sensor located on the RF downconverter

COMMAND	BIT7(MSB) CH SEL2	BIT6 CH SEL1	BIT5 CH SEL0	BIT4 SCAN1	BIT3 SCAN0	BIT2 REF PD SEL1	BIT1 REF PD SEL0	BIT0(LSB) INT EXT CLK
Power-Up STATE	0	0	0	0	0	1	1	0
CONFIG	0	0	0	0	0	0	1	1

Table 4.2. Content of the command, configuraion and control register

state is not what is needed for the application. For an extended explanation of this register consult the datasheet [5].

The way that the ADC works is explained as follow:

The falling edge of CS wakes the analog circuitry and allows SCLK (external clock. This signal comes from the FPGA) to clock in data (information stored in signal DIN). At the same time, signal DOUT changes from high-Z to logic low after CS is brought low and the input data (DIN) latches on the rising edge of SCLK.

The command/configuration/control register begins reading DIN on the first SCLK rising edge and ends on the rising edge of the 8th SCLK cycle. Once the ADC is configured as needed, the internal clock signal (INTERNAL CLK) is activated 125ns after the rising edge of the 16th SCLK cycle. The external clock has to be turned off due to the incompatibility of both clock signals and ensures lowest noise performance during acquisition. At that point, the acquisition begins on the 2nd rising edge of the internal clock and the c.i. selects the proper channel for conversion at the rising edge of the 3rd SCLK cycle and ends on the falling edge of the 18th internal clock cycle.

Each bit of the conversion result shifts into memory as it becomes available. Is important to note that the conversion result is available (MSB first) at DOUT on the falling edge of EOC. Upon completion of the last conversion in the sequence, EOC transitions from high to low to indicate the end of the conversion and shuts down the internal oscillator. Use

the EOC high-to-low transition as the signal to restart the external clock (SCLK). DOUT provides the conversion results in the same order as the channel conversion process. The MSB of the first conversion is available at DOUT on the falling edge of EOC. Figure 4.4 shows the timing diagram for 16-bit-wide data transfer in scan mode.

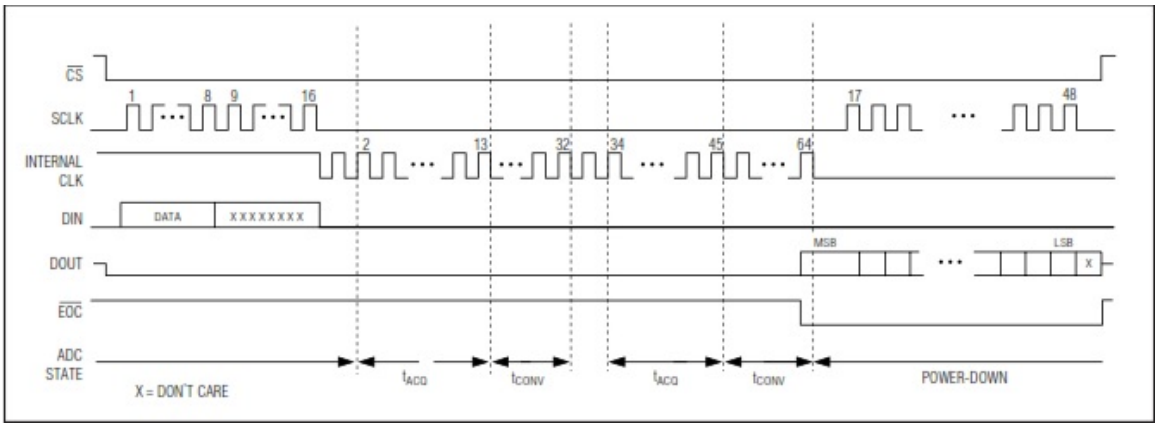

Figure 4.4. Conversion timing for the SPI internal clock mode, 16-bit Data-transfer mode.

Some of the considerations described in the datasheet have been taken into consideration. For example:

- As a software consideration, in order to obtain a maximum throughput force $\overline{CS}$ high after the conversion result is read and force $\overline{CS}$ low again to initiate the next conversion immediately after the specific minimum time.
- As a hardware consideration, force $DSPR$ high and $DSEL$ low for the $SPIQSPIMICROWIRE$ interface mode.

The output data in DOUT signal is straight binary where the nominal transfer function is unipolar. The value of Less Significant Bit, LSB, is $LSB = +62.5\mu V$ or $V_{REF}/2^{16} = +4.096V/65536V$.

The protocol that the ADC uses to transmit the information is the Serial Parallel Interface (SPI) protocol. Due to the importance of this protocol for the performance of the telemetry system, the details of it are explained in section 4.2.1.

4.2.1 SPI communication protocol

The SPI is a serial bus standard communication protocol established by Motorola and supported in silicon product from various manufacturers. This protocol allows a master device initiate communication and data exchange with one or more slave devices. It is a synchronous serial data link that operates in full duplex*. Devices communicate using a master/slave relationship, in which the master initiates the data frame. The frequency used is less than or equal to the maximum frequency the slave device supports and is commonly in the range of 10 kHz – 100 MHz. For this application, the frequency target of this study is 200kbps.

The four logic signals used to establish the communication are:

*signals carrying data go in both directions simultaneously

- **SCLK**: Is the serial clock signal generated by the Master to synchronize data transfers between the master and the slave.
- **MOSI**: Is the output signal for the master and input for the slave.
- **MIS0**: Is an input signal for the master and an output signal for the slave device.
- **SS**: This signal is generated by Master to select individual slave/peripheral devices. The SS/CS is an active low signal.

Among these four logic signals, two of them MOSI and MISO can be grouped as data lines and into the other two SS and SCLK as control lines.

The communication is initiated by the master all the time. The master first arranges the clock by using a frequency, which is less than or equal to the maximum frequency that the slave device supports. Now, this SPI master controls the data transfer by generating the clock signal (SCLK).The master then select the desired slave for communication by pulling the chip select (SS) line of that particular slave-peripheral to "low" state and activates the particular slave it wants to communicate with by using slave-select signal (SS). Once slave is selected then receives or transmits data via the two data lines. A master, usually the host micro controller, always provides clock signal to all devices on a bus whether it is selected or not. The slaves on the bus that has not been activated by the master using its slave select signal will disregard the input clock and MOSI signals from the master, and must not drive MISO. That means the master selects only one slave at a time.

The data may be transferred in either or both directions simultaneously. In fact, as far as SPI is concerned, data are always transferred in both directions. It is up to the master and slave devices to know whether a received byte is meaningful or not. So a device must discard the received byte in a "transmit only" frame or generate a dummy byte for a "receive only" frame.

Slaves can be thought of as input/output devices of the master. SPI does not specify a particular higher-level protocol for master-slave dialog. In some applications, a higher-level protocol is not needed and only raw data are exchanged. An example of this is an interface to a simple codec. In other applications, a higher-level protocol, such as a command-response protocol, may be necessary. Note that the master must initiate the frames for both its command and the slave's response. SPI is a common technology used nowadays for communication with peripheral devices where we want to transfer data speedily and with in real time constraints.

This bus can offer a higher throughput due to the the lack of device addressing which means less overhead. The size of message, content and purpose can be choose arbitrary and there is no 8-bit word limit. There is no need of transceiver and because the signals are unidirectional allows an easy Galvanic isolation. Extremely simple hardware interfacing. SPI does not have an acknowledgement mechanism to confirm receipt of data. In fact, without a communication protocol, the SPI master has no knowledge of whether a slave even exists. SPI also offers no flow control. The protocol not just have useful characteristics, it also has some disadvantages. The most relevant are the lack of flow control by the slave and the slave acknowledgment. This can cause that the master delay the next clock edge slowing the transfer rate or could be transmitting to nowhere and do not know it. Also, only handles short distances compared to other communications protocols and generally prone to noise spikes causing faulty communication. These last facts have to be taken into account during the design of the FPGA algorithm to read the telemetry data and the wire to connect both boards.

The SPI bus can operate with a single master device and with one or more slaves devices. When a single slave device is used, the SS signal may be fixed to logic low if the slave permits it. Some slaves require a falling edge of the chip select signal to initiate an action. With multiple slave devices, an independent SS signal is required from the master for each slave device to control with which device is establishing the communication. The Figure 4.5 show a typical SPI-bus configuration with one SPI-master and multiple slaves/peripherals.

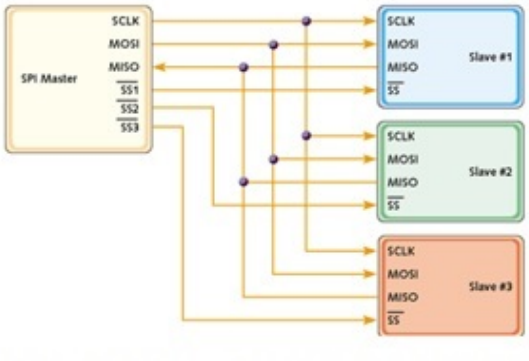

Figure 4.5. SPI communication mode for a single master and multiple slave devices

The configuration used in this thesis to establish the communication between boards is a single master with two slaves, one for each ADC.

4.3 I/O Connector

This section explain the physical connection between the DAS board and the RF downconverter.

In order to establish the connection between the two boards, an specific wire with a different type of connector on each extrem has been made. The RF downconverter side connector corresponds to a db15 male type. For the other extreme of the wire, DAS board side, is used two different kind of connectors due to the constraints of the hardware architecture. More details about this can be found on section 5.2.

The result of having three different types of connectors, two in one of the extremes, is shown in Figure 4.6.

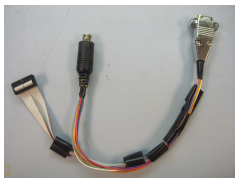

Figure 4.6. Wire that connects the DAS board with the RF downconverter

The description of the RF downcponverter connector pinout number, the corresponding color and signal name is shown in Figure 4.7 and Table4.3.

The input signal from the point of view of the DAS board are connected through the "header 20" connector and the output signal are connected through the "9 pin mini din"

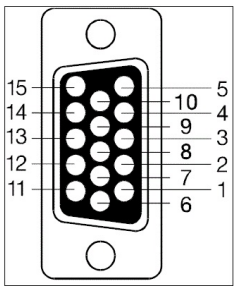

Figure 4.7. DB15 male connector for the telemetry signals of the RF downconverter

db15 PIN NUMBER	WIRE COLOR	SIGNAL NAME
9	white	SCLK
4	green	DIN
11	grey	CS1
12	orange	CS2
14	red	+SHDN
15	purple	-SHDN
10	blue	EOC
3	brown	DOUT
6	black	ground

Table 4.3. DB15 pinout with their own signal and wire color

connector. This last connector is not as common as it may be db9 connector. These two types of connectors are shown in Figure 4.8 and 4.9 and the detailed description is shown in Table 4.4

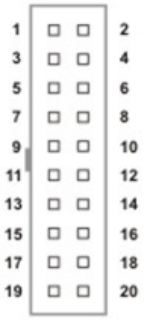

Figure 4.8. 20 header connector

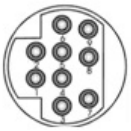

Figure 4.9. 9 pin mini din connector

Signal name	Connector type	Pin number
GROUND	20-pin header	5
DIN	20-pin header	4
EOC	20-pin header	8
+SHDN	9-pin din	6
-SHDN	9-pin din	7
CS1	9-pin din	8
CS2	9-pin din	9
SCK	9-pin din	5
DOUT	9-pin din	1

Table 4.4. Connectors 20 header and 9 pin mini din pinout description

CHAPTER 5

DATA ACQUISITION SYSTEM

The DAC system is responsible to measure and monitor the differential phase of the analog signal from the communication system. It is also capable of receiving the information from the telemetry sensors (power, current and voltage corresponding of the temperature) located on the RF downconverter board. Thus, the two interferometric data streams can be combined with the telemetry data, to characterize and ultimately compensate the possible thermal deviations of the sensitive components of the analog downconversion process.

The end goal would be use the DAC system to monitor and to perform a low-level check in order to detect errors or problematic data and to record intermediate products that can be saved and sent to the ground for further analysis.

5.1 Description of the overall DAC system

The output of the RF downconverter analog signal is fed into two analog-to-digital converters provided by National Semiconductor ADC8D1520 and configured to sample at 3 GSamp/sec. The implementation of this system includes also a high capacity Xilinx Data processing FPGA device, XC4VFX140 and lower capacity Xilinx communications FPGA, XC4VL25 suitable for interfacing with the PCI bus.

The data processing FPGA is responsible to implement a Real-Time phase detection algorithm. This algorithm is based on the theory explained in section 2.1 and 2.2 and is used to calculate not only the phase variation of a single channel but also the relative phase difference between the two downconverted input channels. Also, identifies the accuracy of the RF front-end's performance relative to temperature and then adjusts sampled and downconverted results in real time to rectify the effects of temperature signal fluctuations. This FPGA is in charge to establish the communication with other components over JTAG, SATA and serial interfaces.

5.1.1 System architecture

b) fpga architecture and program system. program the device through JTAG. c) hyper-terminal characteristics.

The overall architecture is shown in Figure 5.1 below. The Xilinx MicroBlaze processor is instantiated in the system for high level procedure control.

The Xilinx Microblaze processor is instantiated in the system for high level procedure control. The PLB system bus is connects peripheral to micro processor. UART is used for communication between PC and MicroBlaze. ADC controller is a finite state machine which can configure ADC parameters. PhaseCalc hardware is our main design which implements the phase detection algorithm. Both interfaces to the PLB to ADC controller and the PhaseCalc are implemented using Xilinx SDK.

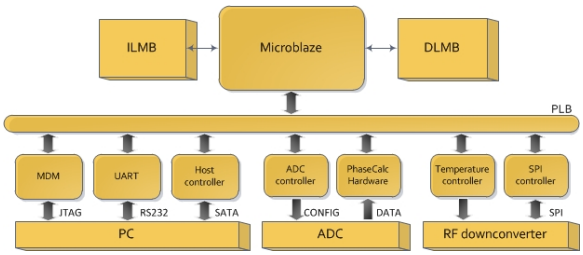

Figure 5.1. Overall architecture of phase detection system

5.1.2 Signals description

In order to establish the communication between the data acquisition system board and the downconverter, a group of signals is used to allow this communication. The table 5.1 shows the description and direction of each signal. Due to the hardware configuration, the available I/O interface and the number of inputs and outputs signals needed the hardware configuration for the communication between the RF downcoverter and the FPGA is as follow:

* Buffer U48 set in the direction A to B. For that, buffer signals are set OE1 = '0' and DIR = '1' * Buffer U50 and U51 set in the direction B to A. For that, signals OE3 = OE4 = DIR3 = DIR4 = '0'. * The signals are connected in the following order:

Signal name	Pin down-converter	Connector	Pin connector	Pin FPGA
GROUND	6	20-pin header	5	ground
xps_spi_0_MOSI_O	3	20-pin header	4	N34
temp_reg_0_EOC	10	20-pin header	8	D36
temp_reg_0_SHDN_p	14	9-pin din	6	R33
temp_reg_0_SHDN_n	15	9-pin din	7	N35
temp_reg_0_CS1	11	9-pin din	8	H32
temp_reg_0_CS2	12	9-pin din	9	L34
xps_spi_0_SCK	4	9-pin din	5	D35
xps_spi_0_MISO	9	9-pin din	1	M35

Table 5.1. Interferometric parameters for the LGRC deployment

The hardware interfaces available for thermal and timing information consist of three different connectors. Two of them are located on the data acquisition board and are a 20-pin header and a 9-pin DIN connector. In the other side of the communication, located on the downconverter there is a db15. In total there are available 29 pins but 10 of the 20 pins header are connected to ground, the rest of the 19 pins available are connected to the fpga through 4 different SN74LVC245A buffers. The SMA connector J22 is also connected to the fpga through the buffer U49. This signal is an input of the FPGA, which means the buffer is set in the direction A to B and also, the signals H5 to H10 from the 20-pin header have to be set in this direction too.

5.1.3 Power supply

To provide the power supply to the DAS board is used an 3U extender card as shown in Figure 5.2. The values used are 5.0V and 3.3V corresponding with the input voltage of the switching power regulators used to generate core voltages, I/O voltages and the auxilary voltages for the Data FPGA and PCI FPGA [12].

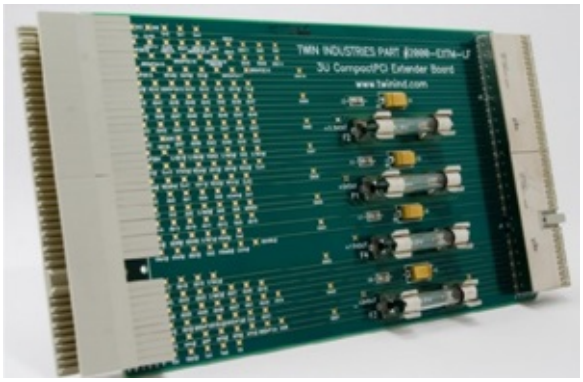

Figure 5.2. 3U Extender card used to provide power supply to the DAS board.

5.2 Design Methodology

The hardware components of the embedded system are designed using XPS and the software application is developed using SDK as explained in section X. The software application is developed using C. The custom hardware logic in the FPGA is designed in Verilog, and the embedded system designed in EDK is instantiated as a module in the main Xilinx ISE project.

Software and hardware codesign strategy is adopted in FPGA implementation.

5.3 Standard Xilinx IP Cores

The Xilinx IP cores facilitate ease of design and integration into the system. This section describes the various IP blocks that have been used to design the system on the Formatter FPGA.

5.3.1 UART Core

A UART is used for logging system information and transmitting results to an attached PC.

A UART is a Univeral Asynchronous Receiver and Transmitter - it is an electronic circuit which handles communication over an asynchronous serial interface - very often an RS232 interface.

The Xilinx UART core is used for communicating with the Host Computer. It has an adjustable baud rate and experiments are conducted at a rate of 115 Kbps.

The UART core is used for implementing serial communication with the Host Computer. All the APIs are defined in the header file xuartlite.h which is added in this application. The functions, Xuartlite SendByte(Base Address, Data) and Xuar- tlite RecvByte(Base

Address), are used for for sending and receiving a byte of data using the UART core. The processor recognizes the argument Base Adress as the memory-mapped base address of the UART. Alternatively, the xil printf function can also be used for sending a stream of data bytes to the computer. The UART core is the default STDIO for the processor system, and hence, this function can be used for sending data to the Host Computer.

5.4 Custom IP Peripheral (temp_reg)

The Custom Peripheral, called **temp_reg** in this system, is added to facilitate communication between the processor and the rest of the custom hardware Verilog modules TR modules (T/R Module Interface, Transceiver Interface and Timing State Machine and the tempreature sensors). In order to add a custom peripheral to the PLB of the MicroBlaze system, the Custom Peripheral wizard is used in Xilinx XPS. This wizard also generates the necessary device drivers that are used in developing the software application for the MicroBlaze processor. After creating this peripheral, the Xilinx PLB interface modules are automatically included in the HDL files. These PLB interface modules take care of all bus transactions between the processor and the peripheral. As mentioned before, the bus is flexible enough to adapt its own characteristics to a specific application. In order to establish the communication between boards, the SPI bus has to be modified to adapt the characteristics of the ADC communication SPI protocol. The difference between the standard SPI protocol and the once that ADC uses is mainly the slave transmitting step.

Check Figure 5.3.

5.5 Board operating rules

Due to the configuration and hardware characteristics the usage of the DAS has to follow a certain operation rules described below,

- The ADC's sample range is configured to work at 800 mV peak to peak. Due to this voltage range the input signal's peak to peak values should be less than 800mV and greater than 600 mV to effectively use all quantization bits.
- Regarding the clock signal, this signal has been hard coded in the hardware at a frequency of 1.5 GHz. This means that the sample rate cannot be changed without change the source code and re-synthesize it. The voltage value of the clock signal is 600 mV.
- Extreme care has to be taken while handling the board, anti-static straps have to be used o ensure that the static charges discharge to ground and do not affect the components present on the board.

To turn on the whole system the following set of steps has to be follow to avoid damages in the DAS board.

1. First of all, the values of the power supply have to be verified before connecting to the DAS board. The input voltages will be provided only after double-checking the voltage levels from the power supply to avoid any mishaps due to voltage fluctuations.

2. Power up the board at the voltage specified in the board. The power supply values are 5.0 V and 3.3 V. Figure 5.2 in section 5.1.3 shows the two power supply points used in this project.

3. Open the a hyperterminal window with the configuration specified in section 5.3.1.

4. Load the configuration file, x and x into the IMPACT software.

5. When it is successfully configured, the hyperterminal will ask to introduce two characters.

6. Turn on the clock signal ($IADC_CLK$) once the FPGA is configured. Do not feed clock signal into ADC until FPGA is configured. Is important NOT TO feed clock signal into DAS board until FPGA is configured.

7. Press two characters on the keyboard. The way that the design is configured, it can be whatever two characters.

8. Activate the trigger signal. This will enable the WE_EN signal of the FIFO and asserts the CLR signal of the BUFR. Provide the trigger signal through a SMA connector J22.

9. The next step is to start the signal generator.

At this point both parts of the system, hardware and software, are set up and the system will begin to work.

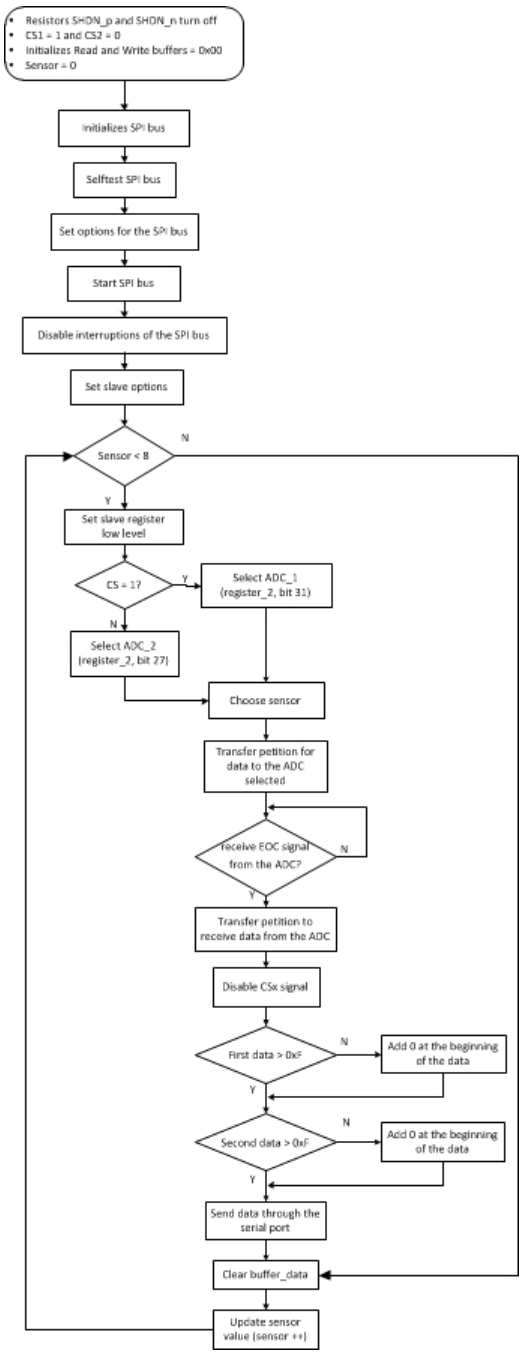

Figure 5.3. Diagram bloc of the algorithm implemented into the FPGA to acquire data from the telemetry system and send it through the serial port

CHAPTER 6

CONCLUSIONS

6.1 Summary of work

The main goal of this thesis is to explain the technology of combining millemeterwave engineering with thermal analysis, to make the system more robust, balanced, and predictable. In order to achieve this goal, a set of objectives were set and explained through the thesis. The creation of a the physical communications between the digital board and the RF boards within the constraints of the exiting hardware interface in order to stablish the communication betweeen boards. There was no existing interface at the beggining of this project and to solve this issue and test the algorithm created for temperature reading, an specific HW interface was created.

The next step was to design a software algorithm to read data from the thermal sensors located on the downconverter in real-time and provide the capability to compensate for possible temperature deviations in the RF system to follow with the adaptation this algorithm with the existing phase detection algorithm and taking into account the hardware limitations.

6.2 Recommendations for future work

This section presents recommendations for future work on the current radar that pop-up during the realization of this thesis.

1. Due to the lack of the FPGA logic resources it was not possible to establish a Real-Time FPGA hardware in the loop simulation enviroment in order to deal with liability and stability of the system. In future project it should be taken into consideration this kind of tests.

2. The subsystem explained in this thesis have been developed in standard condition but the end goal is to lunch this radar. Is it well known FPGA are radiation vulnerable, which is a challange for the realization of the space application of the reconfigurable FPGAs. To do so, EMC test and radiation effects on FPGA should be consider for future project phases.

3. Regarding the temperature sensors used on the RF downconverter, it should be consider replacing the resistors used. The resistors consume a lot of power, 0,625W each resistor, which can produce bigger interferences to phase difference than the small temperature changes by themselves.

4. Moreover, it should be necessary to perform a study to identify a better location for the temperature sensors, choose a better type of sensor and also increase the presence of them on the more sensitive areas of the RF downconverter.

5. For future applications, the input HW interface should be adapted to the output RF downcoverter in order to aboud having different types of connector at the same wire end. Also, more robust HW interface should be designed to avoiud having cross-talk problems within the signal lines.

6. Increase the logic resources of the FPGA in order to improve the way that the system adjust the temperature variations based on the information available from tempreature sensors.

APPENDIX A

RF DONCONVERTER PCB LAYOUT

A.1 RF downconverter. RF part

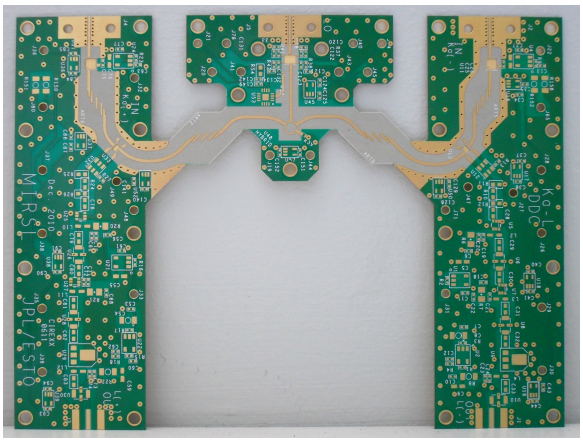

Figure A.1. PCB layout corresponding to the RF part of the downconverter

A.2 RF downconverter. DC part bottom view

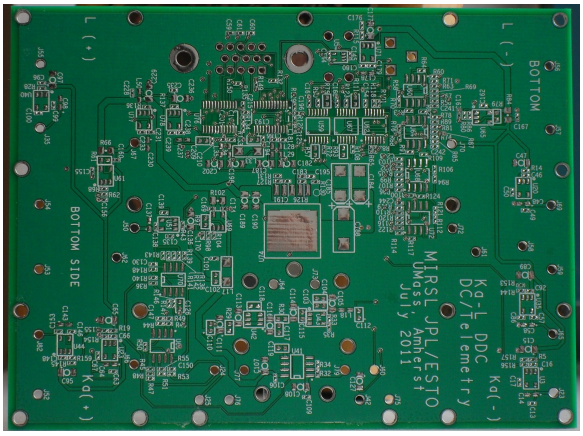

Figure A.2. PCB layout corresponding to the bottom DC part of the downconverter

APPENDIX B

IMAGES OF THE OVERALL SYSTEM

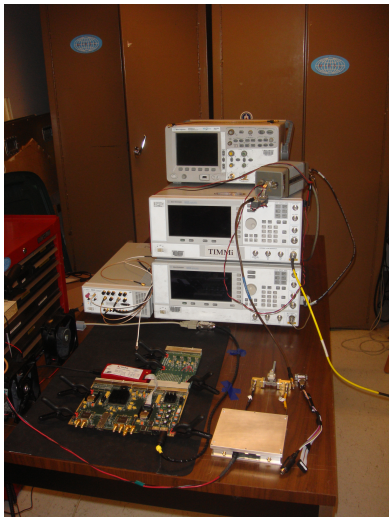

Figure B.1. View of the overall system mounted. Osccilloscope, arbitrary function generator, 35 GHz waveform generator and RF downcoverter connected to DAS system.

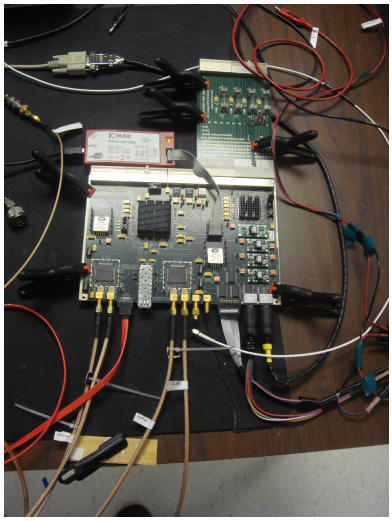

Figure B.2. Closer view of the DAS system with all signals connected.

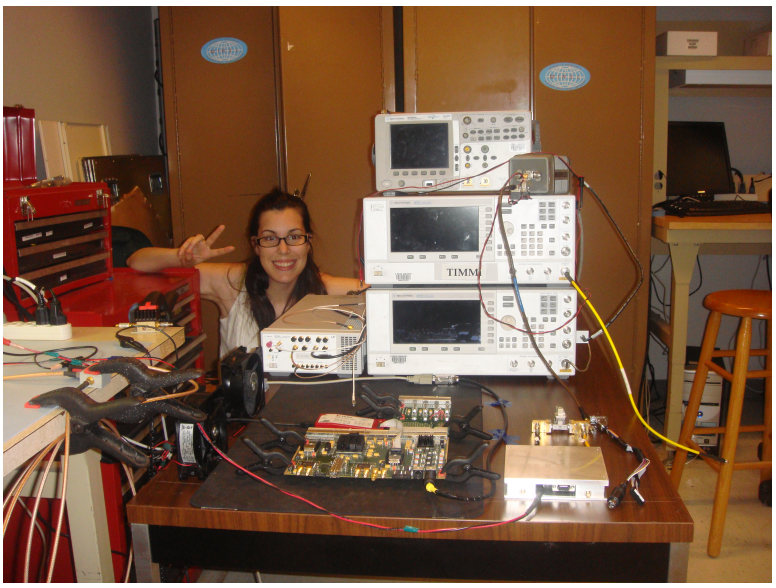

Figure B.3. Me feeling proud of the job done :)

BIBLIOGRAPHY

[1] Cloude, R.S. *Polarisation. Applications in remote sensing.* Oxford University Press, 2010.

[2] Linear Technology. *LT6107 - High Temperature High Side Current Sense Amp in SOT-23*, June 2008.

[3] Lu, Shiting J., Siqueira, P., Vijayendra, V., Chandrikakutty, H., and Tessier, R. Real-time differential signal phase estimation for space-based systems using fpgas. *IEEE Transaction on Aerospace and Electronic Systems 49*, 2 (2013), 1192 – 1209.

[4] Maxim Ingrated. *MAX6612. High-Slope, Low-Power, Analog Temperature Sensor in an SC70 Package*, March 2008.

[5] MAXIMr. *Multichannel, 16-bit, 200ksps Analog-to-Digital Converter*, October 2009.

[6] on Earth Science, Committee, from Space: A Community Assessment, Applications, and Strategy for the Future, National Research Council. National imperatives for the next decade and beyond. Tech. rep., National Research Council, 2007.

[7] organization, The Global Climate Observing System (GCOS). Nasa future missions cgms-38 white pape. Tech. rep., National Research Council, November 2010.

[8] P. Siqueira, R. Tessier, A. Swochak K. Fu D. Esteban-Fernandez B. Heavey. A single-stage, two-channel ka-band to digital, thermal compensating receiver for swot.

[9] Swochak, Anthony F. Development, implementation, and characterization of a ku band interferometer. Master's thesis, University of Massachusetts Amherst, August 2011.

[10] United Monolithic semiconductor. *5-44GHz Detector*, November 2010.

[11] Vedantham, Harish. Design and development of a ka-band interferometer for cryospheric applications. Master's thesis, University of Massachusetts Amherst, February 2009.

[12] Vedantham, Harish. Design and testing of a prototype high speed data acquisition system for nasa. Master's thesis, University of Massachusetts Amherst, December 2010.

[13] Venkatasubramanian, Karthik Srinivasan. Design and development of timmi an interferometric radar. Master's thesis, University of Massachusetts Amherst, September 2007.

[14] Xilinx Corportation. *MicroBlaze Processor Reference Guide*, August 2004.

[15] Xilinx Corportation. *EDK Refernce Guide*, December 2009.

[16] Xilinx Corportation. *ISE In-Depth tutoria*, March 2011.