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Novel charge pump converter with Tunnel FET devices for ultra-low power energy harvesting sources

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***Abstract*—Compared to conventional technologies, the superior electrical characteristics of III-V Tunnel FET (TFET) devices can highly improve the process of energy harvesting conversion at ultra-low input voltage operation (sub-0.25V). In order to extend the input voltage/power range of operation in conventional charge pump topologies with TFET devices, it is of the major importance to reduce the band-to-band tunneling current when the transistor is under reverse bias conditions. This paper proposes a new charge pump topology with TFET devices that attenuate the reverse losses, thus improving the power conversion efficiency (PCE) in a broader range of input voltage values and output loads. It is shown by simulations that compared with the conventional gate cross-coupled charge pump and considering an input voltage of 640 mV, the proposed topology reduces the reverse losses from 19 % to 1 %, for an output current of 10 µA. For this case, the PCE increased from 63 % to 83 %.**

Keywords—Charge Pump; Energy Harvesting; Switched-Capacitor; Thermo-generator; Tunnel FET; Ultra-Low Power.

I. INTRODUCTION

The interest in power supply circuits that are able to harvest energy from the surrounding environment for powering portable and wearable low-power systems has been increasing over the last years [1-4]. Energy harvesting (EH) sources such as micro-photovoltaic cells (PV) [1-2] and thermo-electric generators (TEG) [3-4] are characterized by extremely low output voltage and power values, thus preventing their immediate usage.

Charge pump or switched-capacitor converters have been widely considered to boost the output voltage of EH sources in order to meet the minimum supply voltage requirements of electronic systems [2, 4]. Besides the inherent switching losses that characterize these converters, the main difficulty in achieving a good power conversion performance at low input voltage (sub-0.25 V) and low power levels (sub-µW) is related to the high conduction losses of conventional transistors applied in the conversion process [5]. Thermionic injection transistors as MOSFETs and FinFETs are characterized by a minimum subthreshold-slope swing of 60 mV/dec (room temperature). This characteristic limits the required current at low voltage values in passive DC-DC converters.

The steep subthreshold slope Tunnel FET (TFET) device has been shown to increase the efficiency of the gate cross-coupled (GCC) converter shown in Fig. 1 at low input voltage levels (sub-400 mV) compared to the use of FinFET technology [6]. Under reverse bias conditions, Tunnel FET devices present two main distinct mechanisms of current injection: Band-to-band tunneling (BTBT) and drift-diffusion (DD). These two mechanisms limit the power conversion efficiency (PCE) of the charge pump due to the consequent reverse losses. The first and second injection mechanisms are respectively presented at low and high reverse bias conditions. While the second is inevitable, the first mechanism can be attenuated by a new topology (forcing the V_{GS} of the reverse biased transistors to 0 V. This is the purpose of this paper: a charge pump that attenuates the reverse current of TFETs, thus increasing the PCE in a wider range of operation.

The structure of this work is as follows: section II presents the conventional gate cross-coupled (GCC) charge pump topology, its regions of operation and the perspectives and problems of using TFET devices in the conversion process. Section III proposes a novel charge pump topology to be used with TFET devices. Section IV compares by simulation the performance of the proposed charge pump with the GCC counterpart. The conclusions are presented in Section V.

II. GATE CROSS-COUPLED CHARGE PUMP

In Fig. 1, the gate cross-coupled (GCC) charge pump topology is presented. This topology has been proved to present better conversion performance at low input voltage values compared to other DC-DC converter topologies [5].

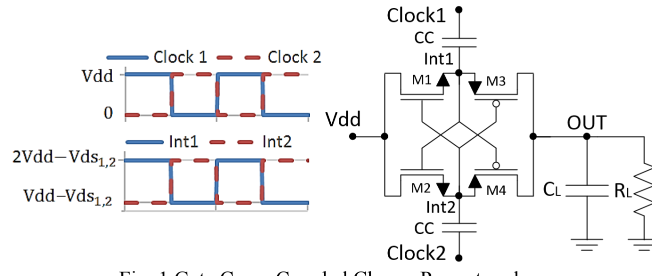

Fig. 1 Gate Cross-Coupled Charge Pump topology

A. *First region of operation (Int1 > Int 2)*

The principle of operation of the GCC converter can be divided into two regions. In the first, the low to high transition of Clock 1 increases the voltage node "Int1" to $2V_{DD}$-V_{DS2}. At the same time, the voltage node of "Int2" is reduced to V_{DD}-V_{DS2}. In this region, the transistors M1 and M4 are reverse biased (off state) and transistors M2 and M3 forward biased (on state). The bias characteristics in this region, considering steady state conditions are presented in Table I:

Table I Bias conditions of the GCC converter in region I

Reg. I	State	Vgs	Vds
M1 (n)	Off	Int2 − Int1 = −Vdd	Vdd − Int1 = −Vdd + Vds1
M2 (n)	On	Int1 − Int2 = Vdd	Vdd − Int2 = Vds2
M3 (p)	On	Int2 − Int1 = −Vdd	Vout − Int1 = −Vsd3
M4 (p)	Off	Int1 − Int2 = Vdd	Vout − Int2 = Vdd − Vsd3

B. *Second region of operation (Int1 < Int 2)*

During the second region of operation, the high to low (low to high) transition of Clock 1 (Clock 2) and consequent reduction (increase) of voltage in node "int1" (int2) results in a forward bias condition of transistors M1 and M4 and reverse bias in M2 and M3. The bias conditions of the transistors are presented in Table II:

Table II Bias conditions of the GCC converter in region II

Reg. II	State	Vgs	Vds
M1 (n)	On	Int2 − Int1 = Vdd	Vdd − Int1 = Vds1
M2 (n)	Off	Int1 − Int2 = −Vdd	Vdd − Int2 = −Vdd + Vds2
M3 (p)	Off	Int2 − Int1 = Vdd	Vout − Int1 = Vdd − Vsd4
M4 (p)	On	Int1 − Int2 = −Vdd	Vout − Int2 = −Vsd4

C. *Tunnel FET in Charge Pumps*

Unlike the conventional MOSFET device, the TFET is designed as a reverse biased gated *p-i-n* diode. For an n-TFET the source region is highly doped with a p-type semiconductor and the drain with a highly doped n-type as shown in Fig. 2. For this configuration, the source region has the lowest voltage compared to the gate and drain and the tunneling effect is produced at the source-channel interface. For the p-TFET the drain is highly doped with a p-type semiconductor and the source with an n-type. In contrast with the n-TFET, this configuration has the drain region with the lowest voltage and the current is allowed by tunneling at the drain-channel interface.

In Fig. 3 (a), the current-voltage characteristic of an Heterojunction TFET device is presented [7-8]. The structure of the HTFET is as follows: Lg=40 nm, P^+ GaSb, N_A=4x10^{19} cm^{-3}, N^+ InAs, N_D=2x10^{17} cm^{-3}, T_{CH}=5 nm, T_{OX} =2.5 nm (HfO2), EOT=1 nm, Φ_M=4 eV.

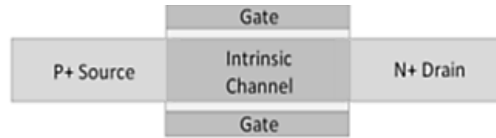

Fig. 2 Double-gate n-TFET structure

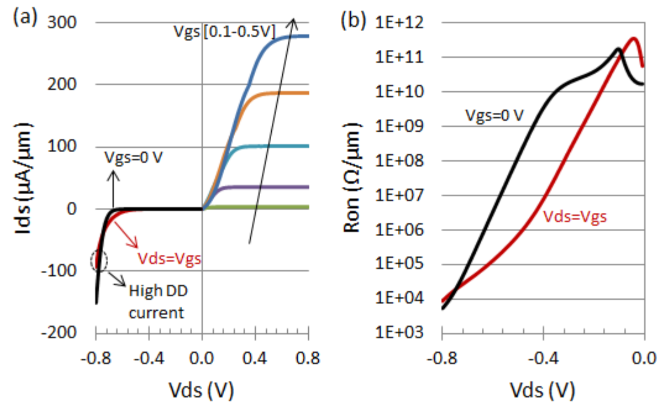

Fig. 3 (a) n-TFET current in function of Vds. (b) n-TFET internal resistance

According to Tables I and II, and considering no losses in the transistors, the reverse bias condition (off state) is always characterized by a V_{GS}=V_{DS}. For n/p types Tunnel FETs, and considering large reverse bias conditions ($|V_{DS}| > 0.7$ V), the reverse current is generated due to the drift diffusion (DD) mechanism, independent on the V_{GS} value applied as shown in Fig. 3 (a). Under this bias condition, the consequent high reverse current degrades the PCE of the charge pump due to high reverse losses, thus limiting the use of TFET devices in charge pumps at low voltage operating ranges. In contrast, under lower bias conditions ($|V_{DS}| < 0.7$ V), the reverse current due to BTBT mechanism can be attenuated if the V_{GS} of the reverse biased transistors is forced to be 0 V.

In [6], the authors presented a slightly different TFET GCC charge pump topology that redirects the gate control signals of the two p-type transistors to the bottom of the two coupling capacitors. This solution forces the V_{GS} of M3 and M4 to respectively V_{DS1} and V_{DS2} (approx. 0 V at low output current) when the transistors are reverse biased. However, the higher the required current, the higher will be V_{DS1} and V_{DS2} and consequently the reverse losses. Also, the reverse current of M1 and M2 (under reverse bias conditions) is not solved. In the next section, a different topology that attenuates the reverse current of all the transistors during their off state condition is presented.

III. Proposed Solution

In Fig. 4, the proposed charge pump is presented. Compared to the GCC converter, it presents two auxiliary transistors and two auxiliary capacitors:

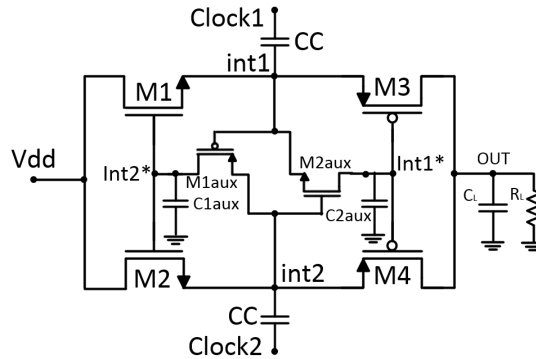

Fig. 4 Proposed charge pump with Tunnel FET devices

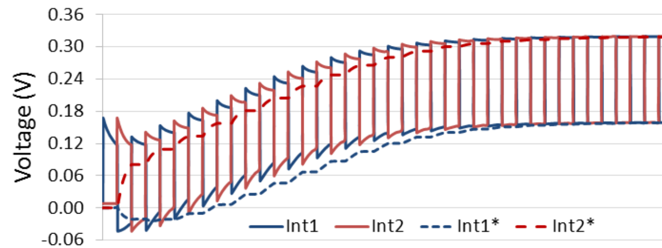

Fig. 5 Voltage nodes in the proposed charge pump

In the proposed charge pump, the auxiliary transistors $M1_{AUX}$ and $M2_{AUX}$ and the auxiliary capacitors $C1_{AUX}$ and $C2_{AUX}$ are required to maintain a fixed gate voltage value in M1-M4 transistors independent of the region of operation.

During start-up, and considering the second region of operation, the auxiliary transistors are forward biased and the "int1*" and "int2*" nodes will present a voltage value of $int1\text{-}V_{SD_M2_aux}$ and $int2\text{-}V_{SD_M1_aux}$ respectively. As the voltage drop between the regions of the auxiliary transistors is negligible, it is assumed that the gate voltages of M1 and M2 are the same as the node "int2" and the gate voltages of M3 and M4 the same as the node "int1". Therefore, the bias conditions presented in Table II present the same V_{GS} and V_{DS} values for the forward biased transistors. In contrast, the reverse biased transistors present a V_{GS} value equal to 0 V, reducing the reverse losses.

During the first region of operation, the auxiliary transistors are reverse biased (off state) and the voltage values at the nodes "int1*" and "int2*" are retained. Therefore, during this region the V_{GS} value of the reverse biased transistors is equal to 0 V while the forward biased transistors remain with the same values of V_{GS} and V_{DS} of Table I.

In Fig. 5, the transient simulation for the above mentioned nodes is presented. As an example, the input voltage is 160 mV. As presented, the node "int1*" presents 160 mV (same value of node "int1" in steady-state) and the node "int2*" presents 320 mV (2*V_{DD}, same value of node "int2").

IV. SIMULATION RESULTS

In this section, the conventional gate cross-coupled (GCC) charge pump is compared with the proposed solution. The clock signals are simulated with a frequency of 100 MHz. In both topologies, the Tunnel FET characteristics are those presented in Fig. 3 (a).

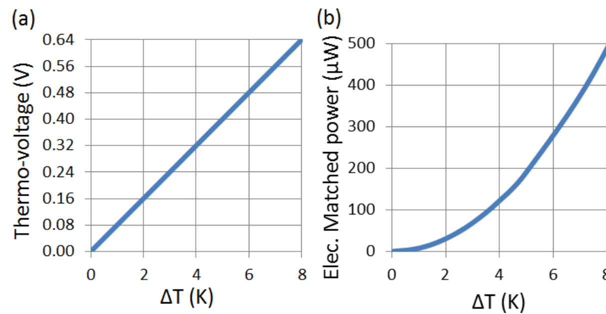

Fig. 6 Electrical characteristics of the MPG-D655. U=80 mV/K (Tamb=25ºC). Rth=22 K/W, Relec = 210 Ω

In both converters, the transistors M1-M4 present channel widths of 1 µm. In the proposed converter, the auxiliary transistors present 0.1 µm width. The coupling capacitors in both converters present a capacitance of 1 pF. The auxiliary capacitors in the proposed converter present 0.1 pF. Finally, the output capacitor has a value 10 pF. The input power supply voltage of both charge pumps is simulated with the characteristics of a commercial ultra-low thin-film thermo-generator, in particular the MPG-D655 from Micropelt [9]. It presents a Seebeck coefficient of 80 mV/ K. The electrical characteristics are presented in Fig. 6.

In Fig. 7, the power conversion efficiency (PCE) in function of the output current for different ΔT values in the thermo-generator is presented. It is observed that for low input voltage values (sub-320 mV, ΔT < 4 K) both the GCC charge pump (dashed lines) and the proposed charge pump (solid lines) present a similar performance. However, when the input voltage of the converter increases (equivalent ΔT of 6 K and 8 K) the proposed converter presents a higher PCE in the entire range of current considered.

In Fig. 8 it is shown that the decrease of the reverse losses enables the proposed charge pump to achieve higher output voltage values at a wider variation of temperatures. Compared to the GCC charge pump and at low ΔT (2 K and 4 K), the proposed converter also allows for higher output voltage at higher output current.

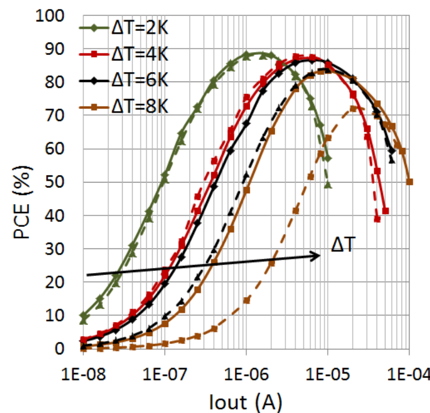

Fig. 7 Power Conversion Efficiency in function of output current. Dashed lines: GCC charge pump. Solid lines: Proposed charge pump

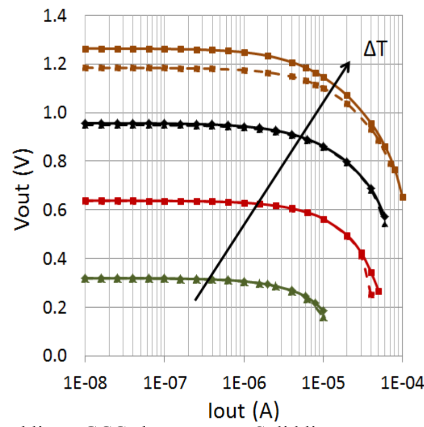

Fig. 8 Output voltage in function of output current. Dashed lines: GCC charge pump. Solid lines: proposed charge pump

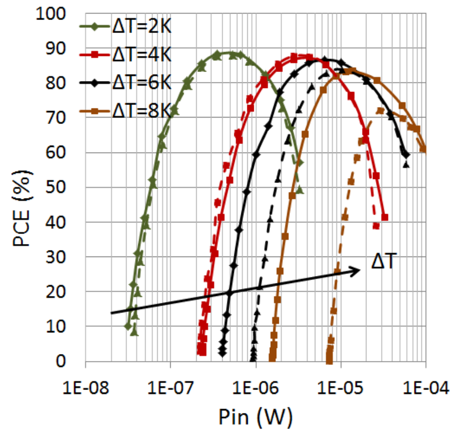

Fig. 9 Power Conversion efficiency in function of input power. Dashed lines: GCC charge pump. Solid lines: proposed charge pump

In Fig. 9, it is shown that compared to the conventional GCC charge pump, the proposed solution allows for higher power conversion efficiency at lower input power values when the thermo-generator is subjected to ΔT with values higher than 4 K (320 mV). At higher input power supply voltage values, the higher reverse current of the transistors in the "off" state in the conventional GCC topology limits the PCE of the converter due to the increase of the reverse losses.

In order to estimate the reverse losses of both converters, a power distribution comparison of losses is presented in Fig. 10. The output current considered is 10 µA for two variations of temperature, ΔT of 4 K and 8 K. It is observed that for both charge pump converters, the losses considering a ΔT in the thermo-generator of 4 K (320 mV) are mainly due to switching and forward losses (of forward biased transistors). At a ΔT of 4 K, the reverse losses of both converters are negligible. However, when increasing the input power supply voltage to 640 mV (ΔT = 8 K), the reverse losses of the GCC converter represent 19 % of the total input power. At the same conditions, the reverse losses and auxiliary circuitry of the proposed converter are respectively 1 % and 2 % of the total input power.

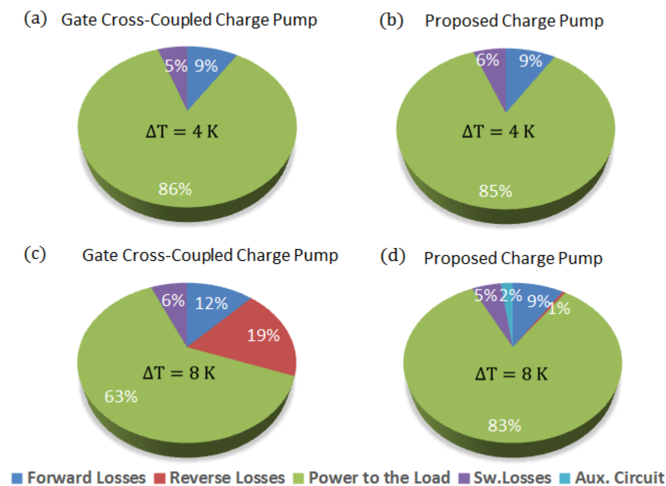

Fig. 10 Power distribution for an output current of 10 µA

In the proposed converter, the extra area of the auxiliary transistors and capacitors are presented as a drawback. In the simulations, sizes of 1/10 the main transistors and coupling capacitors were considered. However, these sizes can be further reduced as long as the gate voltage values of the main transistors are kept at the predefined level during the entire regions of operation.

V. Conclusions

In this work, a novel charge pump topology for the application of TFET devices is proposed. It is shown by simulation that the proposed charge pump reduces significantly the reverse losses by forcing the V_{GS} of the reverse biased transistors to 0 V. To achieve this, an auxiliary circuitry is required to keep the gate voltage of the main transistors at a fixed voltage. This behavior results in higher PCE and output voltage values at a wider range of output current. It is shown by simulations that when considering the conventional GCC converter with an input power supply voltage of 640 mV (I_{OUT} = 10 µA), 19 % of the power losses are due to the reverse current of reverse biased Tunnel FETs. With the proposed solution, these losses are reduced to 1%.

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References

[1] D. Brunelli, C. Moser and L. Thiele, “Design of a solar-harvesting circuit for batteryless embedded systems,” *IEEE Trans. on CAS part I*, Vol. 56, No. 11, pp. 2519-2528, 2009

[2] S.W. Hsu, E. Fong, V. Jain, T. Kleeburg and R. Amirtharajah, "Switched-capacitor boost converter design and modeling for indoor optical energy harvesting with integrated photodiodes," *Low Power Electronics and Design (ISLPED), 2013 IEEE International Symposium on* , pp.169-174, 2013.

[3] L. Mateu, C. Codrea, N. Lucas, M. Pollak, P. Spies, "Human body energy harvesting thermogenerator for sensing applications," *International Conf. on Sensor Tech. and App.*, pp. 366-372, 2007.

[4] G. Bassi, L. Colalongo, A. Richelli and Z. Kovacs-Vajna, "A 150mV- 1.2V fully-integrated DC-DC converter for Thermal Energy Harvesting," *Power Electronics, Electrical Drives, Automation and Motion (SPEEDAM), 2012 Int. Symposium on*, pp. 331-334, 2012.

[5] O.Y. Wong, H. Wong, W. S. Tam and C.W. Kok, “A comparative study of charge pumping circuits for flash memory applications,” Microelectronics Reliability, vol. 52, no-4, pp- 670-687, 2012.

[6] U.Heo, X. Li, H. Liu, S. Gupta, S. Datta and V. Narayanan, "A High-Efficiency Switched-Capacitance HTFET Charge Pump for Low-Input-Voltage Applications," *VLSI Design (VLSID), 2015 28th International Conference on* , pp.304,309, 2015.

[7] V. Saripalli, A. Mishra, S. Datta and V. Narayanan, “An energy-efficient heterogeneous CMP based on hybrid TFET-CMOS cores,” *Proceedings of the 48th Design Automation Conference (DAC)*, pp.729-734, 2011.

[8] V. Saripalli, S. Datta, V. Narayanan and J.P. Kulkarni, “Variation tolerant ultra low-power heterojunction tunnel FET SRAM design”, *IEEE/ACM International Symposium on Nanoscale Architectures*, pp.45-52, 2011.

[9] “MPG-D655 Thin Film Thermogenerator Preliminary Datasheet,” Accessed January 2014, http://micropelt.com/downloads/datasheet_mpg_d655.pdf.