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Design, implementation, and verification of an FPGA-based control system for a permanent-magnet motor drive built upon a three-phase four-level active-clamped inverter.

A Master's Thesis

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by

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MASTER IN ELECTRONICS ENGINEERING

Advisors: Emili Lupon i Rosés, Joan Nicolás Apruzzese

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Title of the thesis: Design, implementation, and verification of an FPGA-based control system for a permanent-magnet motor drive built upon a three-phase four-level active-clamped inverter.

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Abstract

The present work summarizes the work and knowledge acquired by the author during its Masther's Thesis in the Research Group in Power Electronics, GREP. The development is based on the Multilevel Active-Clamped (MAC) power converter prototype, that was initially developed by GREP. Serving as a great introduction to the multilevel converter state-of-the-art, the prototype was tested and it was proved the need for a custom FPGA-based control platform board to drive a PMSM. The design of the board is then performed following the requirements established by the research group and the results obtained from the initial tests. Issues as power decoupling, signal conditioning and grounding strategies are discussed in the following chapters.

A todas mis *patas*, las que me mantienen en pie.

Acknowledgements

This thesis was supported in great extent by the Research Group in Power Electronics, GREP, at the Technical University of Catalonia. The initial prototype developed by this group is described in [1].

I would like to thank Dr. Sergio Busquets who gave me the opportunity to become part of this group and offer me this thesis, and its support during its development.

An extensive part of the project was developed in collaboration and supervision by Dr. Joan Nicolas Apruzzese, whose dedication and on-going support made this project feasible. As one of the main precursor of the initial prototype, he became an essential help to understand the problems and requirements of the project.

The initial version of the project was developed in collaboration between the GREP and Dr. Emili Lupon i Rosés, who is responsible of the FPGA's configuration. It has to be emphasized its support while debugging the system behaviour and many inquiries regarding the system's logic.

Dr. Miguel J. García was consulted and provided valuable support in the analog and mixed signal early design stages. His insights and clarifications were very helpful toward building a successful project in terms of signal integrity, noise and EMC.

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1. Introduction

1.1. Project content and structure

This thesis work summarizes the experimental tests performed on a Multilevel Active-Clamped (MAC) power converter prototype, initially developed by GREP. The prototype was tested and it was proved the need for a custom platform board, mainly to solve coupled and conducted noise issues. The original control system is based on the DE0 board from Terasic/Altera, which includes a Field Programmable Gate Array (FPGA) Cyclone III. The following work consists in designing a new FPGA-based control system to substitute the original control system used to control the three-phase four-level active-clamped inverter. The novel control system consists of a single board containing a new FPGA device more suitable for the specific application, sensors circuitry, the analog-to-digital converters, conditioning signal processing circuitry and user interface circuitry.

This thesis is organized as follows. Chapter 1 presents a brief introduction of the work done, the objectives and the work plan. Chapter 2 reviews the state-of-the-art of the technology involved in the whole system architecture: power converter topology, FPGA implementation and control structure; mostly based on research publications by GREP members. Chapter 3 reviews the initial experimental tests performed with the original prototype and covers the electrical circuit and layout design of the new prototype. To conclude the thesis, an economical review of the costs of the new prototype is presented.

1.2. Motivation

As part of the research activities of the GREP, the development of new modulation strategies is one of the main ones. In this context, the multilevel modulation “The Nearest Three Virtual Space Vector PWM”, described in [2], was developed initially for three level power converter and further extended in [3] for converters consisting of four levels and in [4] for the generic case of *m* levels.

The research concept, in this case a modulation scheme, is first tested and simulated into a numerical software solution, such as Matlab/Simulink that provides the simulation environment and is commonly used in many research areas and departments. This aims to test the feasibility of the theoretical concepts and its mathematical implementation.

This implementation can be translated into a hardware based solution, such as dSpace hardware or other custom hardware, where the mathematical algorithm extracted from the simulator interacts with the real hardware (the power converter), providing a real response of the system.

However, depending on the algorithm complexity and the system requirements, this approach is not always feasible as it cannot meet the design constraints or may seriously limit the theoretical study of the system, normally implying a limitation in the control loop by the simulator response time.

For this reason, together with the interest of the group to move into more industrial prototypes, an initial implementation of the modulation algorithm was performed by the GREP in collaboration with Emili Lupon [1]. This implementation covers the PWM modulation of four-level case of a Multilevel Active-Clamped (MAC) topology explained in [3] and will be further discussed in chapter 2.

A significant research's goal is to implement a closed-loop controller where the relevant variables are updated as close as possible to the update of the switching cycle. In other words, to obtain the update of the modulation periods with the latest system variables. However, this is not the target of the implementation described in [1], as it is a first step towards this objective, and the controller is implemented in open loop.

As it will be described later, the necessity of a robust platform arises immediately: proper ground planes and shielding must be used to overcome numerous noise issues as well as ground issues. As a mixed signal system, the digital signals can overcome the analog ground causing noticeable errors on the small analog signals.

Also, the current state of the system does not provide enough reliability, as many connections are employed that are just not properly fixed or stable. This leaded to day-to-day problems that required large amount of time to investigate, delaying planned tasks and tests.

1.3. Methods and procedures

The scope of the current thesis work starts at this point, where the open loop controller is implemented and tested. This system is implemented in a DE0 board from Terasic/Altera, based on a Field Programmable Gate Array (FPGA) Cyclone III, and a custom stripbard containing the ADC and the required interfaces. This setup is driving a permanent-magnet motor (described also in chapter 2) by a custom four-level power converter board developed previously by GREP.

The FPGA implementation [1] has been revised completely for the closed loop control, being not tested at the start of the thesis: nor the new closed loop algorithm, nor the open loop algorithm.

1.4. Global system description

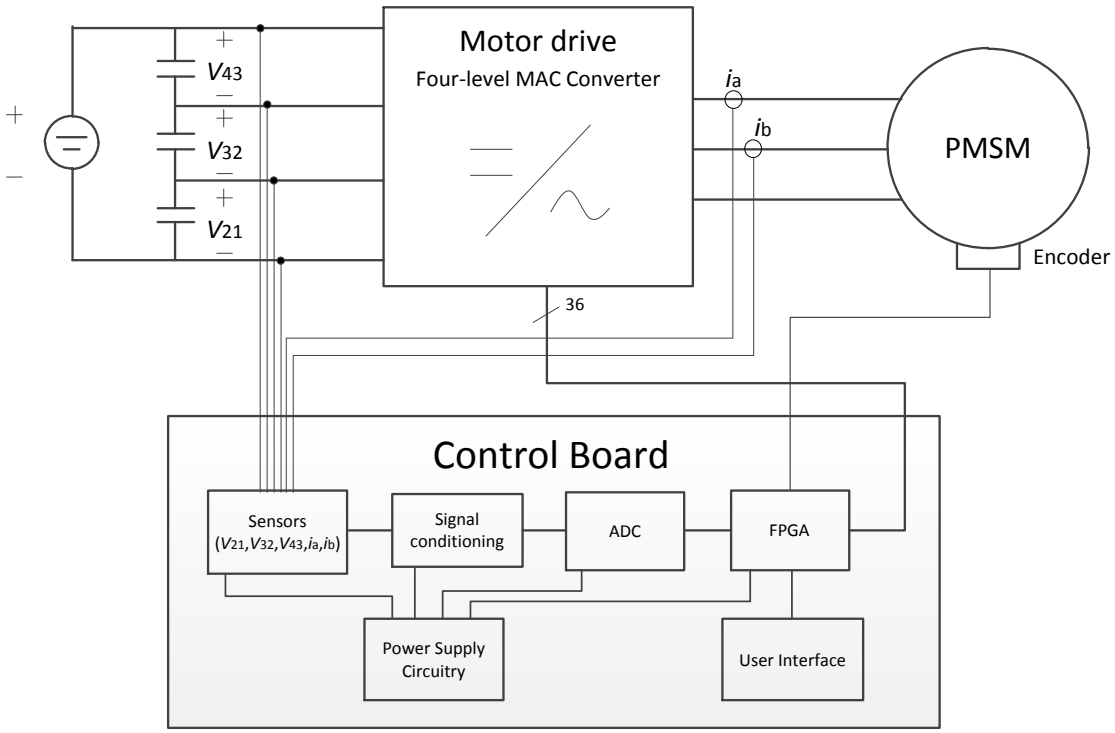


Figure 1. Global system diagram.

As it can be seen in Figure 1, the system is composed by a DC-bus voltage that consists of three independent voltage sources in series. These voltage sources may be a capacitor voltage divider (in order to get the intermediate voltages), a set of batteries or a set of voltage sources.

These voltages are fed to a four-level three-phase MAC converter that will be detailed in chapter 2. The function of this block is to convert the dc voltages into a three phase ac voltages of the appropriate magnitude, phase and frequency for a permanent magnet synchronous motor.

The control logic that rules the MAC converter (including the modulation scheme and the control algorithm) is calculated and is implemented in a single device, an FPGA. The system requires the motor phase current and the dc capacitor/battery voltages, as well as the motor angle.

The final prototype board should be composed of the FPGA, the required power supplies, user interface, interface with the encoder and analog sensors and signal conditioning.

1.5. Objectives

The main objectives could be summarized as follows:

- Study and understand the technology involved in the project.
- Analyze the state of the initial version of the control system, which is based on the DE0 board from Terasic/Altera.
- Be involved in and understand the system test performed with the initial prototype.
- Select a suitable FPGA for the application.

- Design the electronic circuit of the new FPGA-based control system, which comprises the new selected FPGA, the analog-to-digital converters, a suitable user interface, and additional circuitry.
- Design the layout of the printed-circuit board of the new FPGA-based control system.
- Assemble a prototype of the FPGA-based control system.
- Update the design implemented within the FPGA, including changes from the current version, as for example the modification of the type of communication between the FPGA and the analog-to-digital converters (parallel instead of series), the optimization of the instant at which the input signals are acquired and computed with the purpose of enhancing the control of the inverter, and the support of the new user interface.

A brief overview of the initial prototype system has been accomplished in the previous chapter. As it has been outlined, the requirements to get a fully working closed-loop prototype are more demanding.

The objectives pursued by the new electrical circuit are:

- Reduce radiated noise in the analog circuitry. Radiated noise from the power converter couples into the relatively-long wires used in the bread board.
- Reduce conductive noise. Because of improper analog-digital isolation, the current peaks in the digital part affect the signal ground and distort it.
- Improve system robustness.
- Reduce system connection complexity
- Simplify the system configuration and debugging capabilities.
- Allow room for more processing capabilities. The closed loop algorithm is known to be compact enough, about 8000 logic elements, but collaboration with other departments is studied and can result in more complex algorithms.

The reasons for these requirements are extracted from the preliminary test driven in chapter 3.1 and the demands from the research group.

1.6. Work plan

The image bellow describes the initial schedule describing the project tasks as a Gantt diagram, later reviewed in 1.7. The milestones are shown in italics.

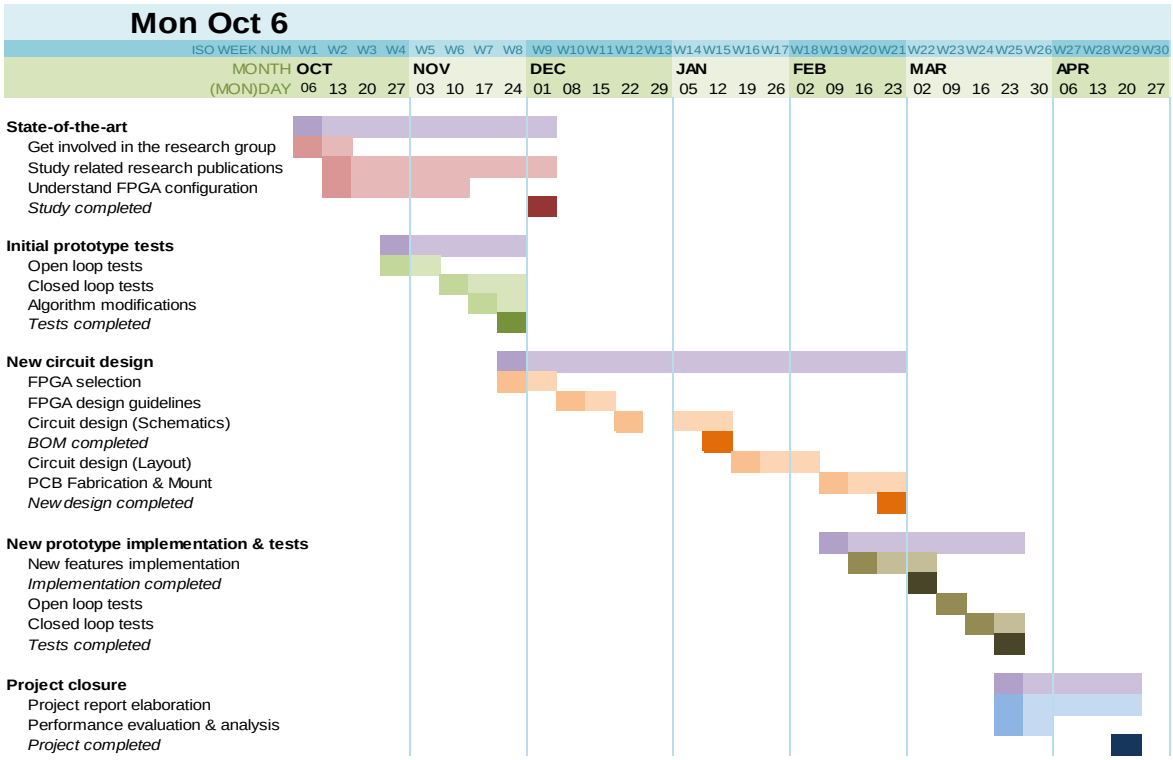


Figure 2. Inital work plan

1.7. Deviations from the initial plan

The initial plan proved to be too far ambitious for the scope of a master thesis, principally due to unexpected drawbacks during the initial experimental tests and the underestimation of the design complexity of a state-of-the-art FPGA device. Also, no previous experience in high-density PCB design, neither from the author of this thesis nor from the research group, made very difficult to estimate the actual effort required for the design.

The actual schedule is reviewed in **¡Error! No se encuentra el origen de la referencia.**

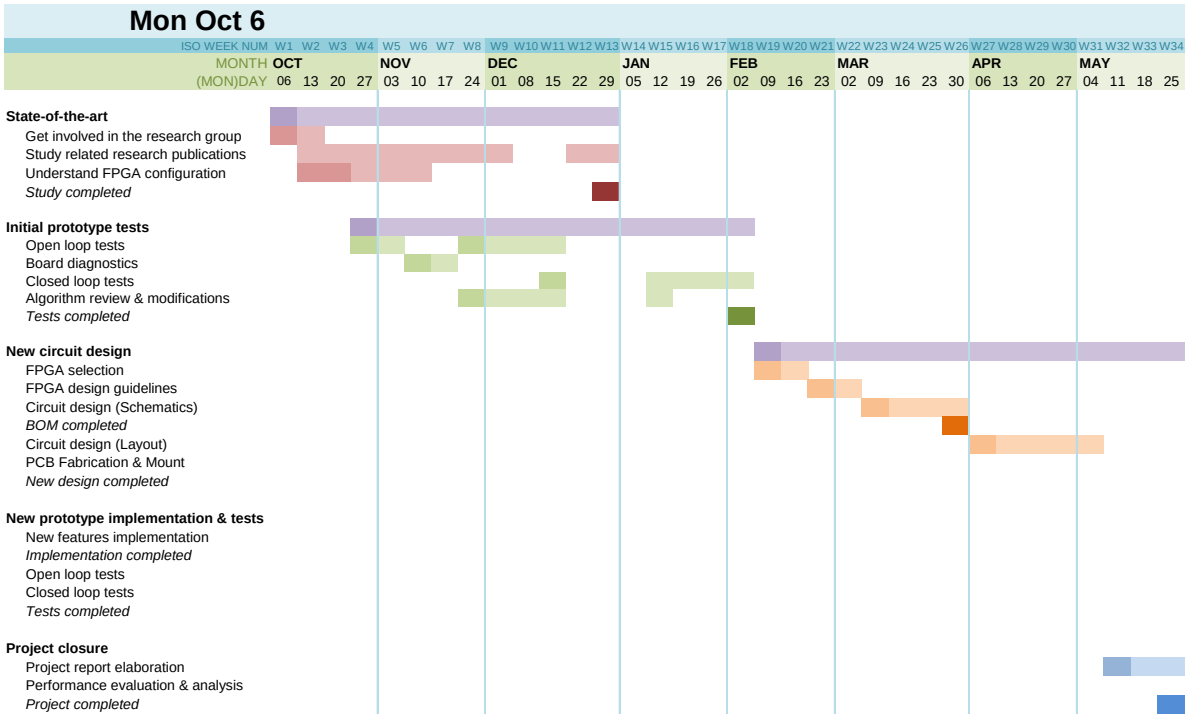


Figure 3. Actual work plan

As can be seen in the Gantt diagram, the initial tests were expected to last one month, serving as introduction to the project and team working habits. The reality turned out to be far more difficult to accomplish, and as will be detailed in chapter 3, the tests were tediously to perform and requires constant re-checking of the system.

The needing for a debugging system required FPGA reconfiguration and study of SignalTap II debugging tool. Some modifications not initially considered were also performed.

These tests extended well until February 2015, delaying the entire project and making impossible to accomplish the planned schedule.

On other side, the tools used to successfully develop a modern FPGA mixed signal board (Altium Designer, PDN calculator) have a stepper learning curve than expected. The learning basis of the cad tools were not considered in a first timing study. In the same context, the design constraints required constant updating between the manufacturer, the components involved in the design and the board layout. The initial test showed the needing for deeper investigation in noise ground treatment and new circuit parts were introduced.

The system requirements forced us to use a BGA-type FPGA package, requiring the study of specific issues related with this kind of package. Also, the board is preferred to be built only in four layers to keep costs down and required carefully study of FPGA pin-planning.

This made it necessary, unwillingly, to reduce the project scope not making possible to accomplish the latter objectives of the project. This covers mainly the FPGA configuration update and performance improvements checks.

2. State of the art of the technology used in this thesis

This chapter will review the existing work and literature involved in the project development, mainly based on research papers produced by the members of the GREP research group that can be found at the bibliography.

2.1. Power converter

The project evolves around a four level Active-Clamped Converter (MAC). As a multilevel converter, it has several advantages over the traditional two-level converters that have lead them towards high power applications, such as reduced voltage rating of semiconductors, lower harmonic distortion and increased efficiency [5]83. On the other side, a larger number of semiconductor is used and the modulation strategies becomes complex. However, they are gaining popularity in mid to low power conversion as processing capabilities are increasing.

The MAC converter is a multilevel power topology described in [6], extended from the popular three-level active neutral-point-clamped topology, which is built upon a single semiconductor device. This single semiconductor device can be a power transistor (with the typical antiparallel diode), a thyristor, etc.

In the generalized multilevel topology, a so called “basic cell” is formed by two pair of switches with an antiparallel diode and a flying capacitor. However, in the Active-Clamped Converter, the flying capacitor is removed, remaining only the dc link capacitor and leading to a simplified topology.

These basic cells are arranged in a triangular connection. The topology is formed by $\frac{1}{2} \cdot m \cdot (m-1)$ basic cells, being *m* the number of levels of the converter. This way, each basic cell has to withstand a voltage equal to the dc link divided by the number of levels -1.

In the particular case of this project, a four-level three-phase MAC converter is used. Each MAC phase is formed by 6 six basic cells, 12 power MOSFET in total. The converter is used to drive a permanent magnet motor where the three output phases are connected to the motor windings.

A basic modulation scheme [6] is first presented and studied in this text, but afterwards presents an improved modulation scheme developed by GREP [7].

To allow the connection of the dc-link bus voltages to the output, a set of *m* switching states is defined by a set of *m-1* independent control variables (c_k). For the example studied in this thesis of a four-level converter, there are 3 independent variables.

The converter topology can be seen in the next image:

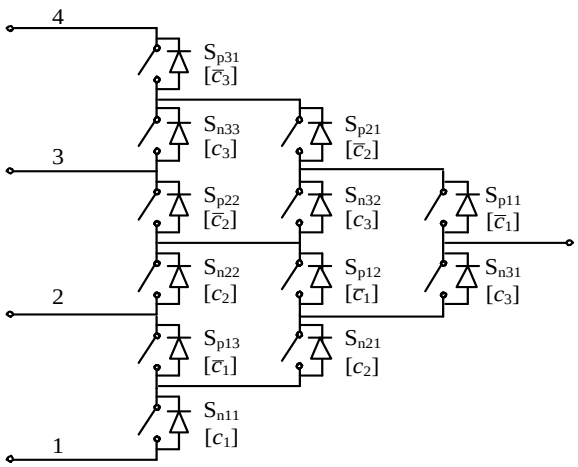


Figure 4. Power converter. 1 leg.

To connect the output terminal *o* to the input terminal *k*, the control values (always following the notation from [6]) is as follows:

$$c_j = 0 \ (j < k)$$

$$c_j = 1 \ (j \geq k)$$

It is important to notice that following this notation scheme, the blocking voltages of each device will be preserved: the devices not carrying any current are also switched on to preserve the devices blocking voltage to $\frac{V_d}{m-1}$.

The number of independent variables is different from the number of required output control pins from the FPGA controller, as while each MOSFET is not controlled independently, the implementation details require small modifications to these control independent variables in each individual control pin, as stated in [6] and studied deeply in [7]. This fine control is required in the transition between switching states to first turn off the required devices and, after a blanking time, turn on the required ones. Also, the switching loses concentrate in the last device being turned off, and can be modified to distribute the loses between devices.

The modulation strategy is further developed in [2] and [3] for three and four level topology respectively, receiving the name of “nearest-three virtual-space-vector PWM”. This modulation guarantees the dc-link capacitor voltages on any operating condition, provided that the addition of the three phase currents equals zero (as is in the PMSM load case). This modulation is an advance over the traditional PMW strategies based on the nearest-three space vectors that cannot guarantee a stable and balanced dc-link voltage under all operating conditions and loads. The balancing problem arises from the occurrence of non-zero currents at inner dc-link points that will either discharge the upper capacitors or the lower ones. This is, of course, unavoidable for every instant but can be avoided in average by hardware or software solutions.

The space-vector diagram can be studied only on the first sextant, as the others can be extrapolated because of its symmetry, and the redundant switching states are selected so

that the midpoint currents, in the case of study i_2 and i_3, the average value is zero in every switching cycle. As said, this fact guarantees the DC-link voltage balancing, which is not possible for original modulation patterns for high modulation indexes and high load angle.

This improvement is achieved by the introduction of a set of new virtual vectors that are product of a linear combination of vectors corresponding to other switching states that permits an average output current equal to zero.

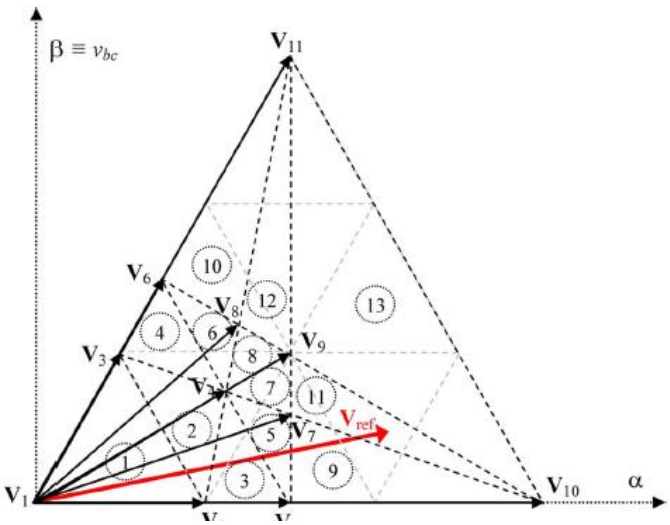


Figure 5. Virtual vector representation. Image from [3]

For the FPGA implementation the proposed simplification of the modulation proposed in [3] is employed, using values of x5, x6, x9 = 0.5 as suggested and can be found in the aforementioned paper, significantly simplifying computations.

2.2. Control strategy

In this section, two different control strategies co-exist in the current implementation of the controller: An improved dc-link voltage control and the actual motor control, represented in blue and yellow respectively in the image below.

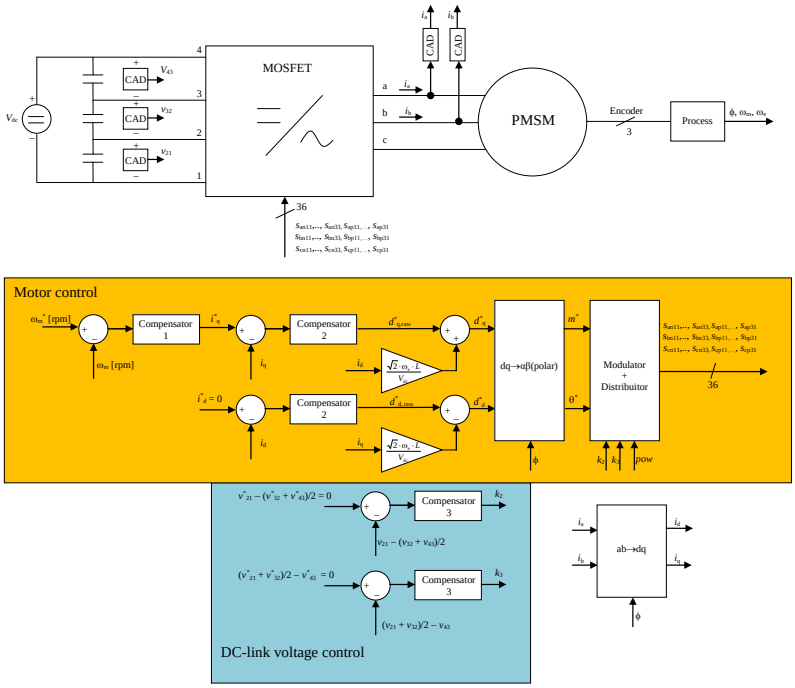


Figure 6. Control diagram. Yellow, speed and current control. Blue, voltage balance control

2.2.1. DC-link voltage

Although the modulation presented in [2] and [3] avoids the balancing dc-link capacitor problem theoretically, a closed loop control becomes necessary to avoid any unbalances and non-linarites occurring due to a non-ideal system.

In [8] a control strategy for the active-clamped topology of any type of base modulation, any number of levels or any number of legs is proposed, so the balance is preserved for the whole modulation index range, (0, 1). It achieves this stability by intentionally perturbing the phase duty-ratio waveforms. However, with the control proposed, the associated small signal model is complex and unknown, preventing an optimum control to be found. This work is further evolved in [9], which presents a simpler symmetric formulation modification of the previous control that permits the definition of the small signal model. As reported in the paper, the main difference is that while the first implementation represents an offset in the leg duty ratios in order to produce an offset in the leg voltages, this latter work represent a per unit increase on the leg duty ratios, rather than a fixed value.

This control requires the calculation of the power flow direction, as the control should vary the leg duty-ratios values accordingly.

As this latter work is employed in the implementation of the closed loop controller, it is important to notice the following paragraph from [9] that establishes one of the main design constraints:

"T_{ds} is the delay due to the sampling of the capacitor voltages or k_y prior to the beginning of the switching cycle. **If fast analog-to-digital converters** and a field-programmable gate array (FPGA) are used in the implementation, T_{ds} can be reduced to a small

percentage of the switching cycle. In the following, it will be assumed that $T_d = T_s$ for simplicity."

For this sentence to be valid, the project will employ 6 parallel ADC working near max frequency in parallel mode as well as an FPGA to reduce the computational time.

2.2.2. Motor control

The system implements an industry-standard field-oriented control (FOC) motor control algorithm formed by two loops: two fast current control loop (inner) and the angular slow control loop (outer).

The modulation described in 2.1 requires the target reference vector to extract the leg duty cycles. This target reference vector is defined by its length, noted as *m**, and its angle *θ** in αβ coordinates. Note that this is coherent with the modulation definition on abc plane, as its axis are equivalent for αβ coordinates. This reference vector is the output of the FOC motor control and is used as the input for the simplified algorithm of the modulation exposed in 2.1.

The current is feed by two analog sensors. As the three phase system (the permanent magnet motor) does not have a neutral connection, the third current can be calculated as a linear combination of the other two. These currents are the instant value of phase currents, in abc coordinates.

The control can be studied in abc coordinates, the system variables are not constant values even for a constant torque on the motor (unless its angular velocity is zero). Though possible, successful implementations have been approached by nonlinear control techniques, the control becomes complex.

In this case, the current is converted to dq components by the direct (Clarke & Park) transformation:

$$\begin{bmatrix} i_d \\ i_q \end{bmatrix} = \sqrt{2} \cdot \begin{bmatrix} \sin\left(\theta + \frac{\pi}{3}\right) & \sin(\theta) \\ \cos\left(\theta + \frac{\pi}{3}\right) & \cos(\theta) \end{bmatrix} \cdot \begin{bmatrix} i_a \\ i_b \end{bmatrix}$$

This simplifies the control design as the current axes moves at an angular speed equal to the electrical speed of the motor. This way, the i_q current is the inducted current perpendicular to the motor axis and responsible of the torque of the motor; while the i_d current is the inducted current aligned with the axis, causing the magnetization of the rotor.

Thus the torque can be expressed in dq coordinates by:

$$T_e = \frac{3}{2} \cdot P \cdot \left[\psi_m i_q + i_d i_q \left(L_d - L_q\right)\right];\ \psi_m: \text{depends on motor}$$

In case of $i_d = 0$:

$$T_e = \frac{3}{2} \cdot P \cdot \psi_m i_q$$

The control implemented is formed by a pair of identical PI algorithm and two different decoupling terms. The decupling term introduces a small term depending on i_q and i_d for d_d and d_d terms respectively. This is because the motor model introduces a cross dependence from the voltages in d and q coordinates [10]:

$$\begin{bmatrix} v_d \\ v_q \end{bmatrix} = R_s \cdot \begin{bmatrix} i_d \\ i_q \end{bmatrix} + \begin{bmatrix} L_d s & -L_q \omega_e \\ L_d \omega_e & L_q s \end{bmatrix} \cdot \begin{bmatrix} i_d \\ i_q \end{bmatrix} + \psi_m \omega_e \begin{bmatrix} 0 \\ 1 \end{bmatrix}$$

In the case of interest, the compensator is multiplied by the square root of two because the variables d_d^* and d_q^* are multiplied by the square root of two as it simplifies the

The angular controller enables the system to move at a target angular speed. It forms an outer loop composed of a PI controller.

The DC-link control voltage explained in 2.2.1 is implemented in the FPGA as two independent compensators, at the present time only proportional control is implemented. The DC-link voltage bus is sensed each one independently, leading to the voltages v_{12}, v_{32}, v_{43}; ordered from lower bus to the upper one. As the control presented in [9], and due to the fact that the capacitor voltage difference only depends on the non-zero inner currents from the dc-link bus (current directly flowing from levels 2 and 3), only needs two input variables k_2 and k_3 that compensates these differences. k_2 aims to minimize the voltage difference between v_{12} and the arithmetic mean of the other voltages; whereas k_3 does the same for v_{43}.

2.3. FPGA implementation

It is the purpose of this chapter to review the implementation that drives the initial prototype on the Cyclone III device as of February 2015. An exhaustively review of all the implementation details is not carried out, as is out of the scope of the present document, but to focus on the technologies applied and highlight some special features.

The FPGA implementation was revised for the closed loop operation (the initial configuration is described in [1]), receiving a major revamp.

The flexibility of reprogrammable hardware allows implementing highly parallel structures that reduces dramatically the required processing time. Also, as it will be described later on this same chapter, allows to specifically design the system and bus widths to the required resolution of the input variables.

Variable values and calculations are performed in fixed-point to reduce hardware needs, carefully designing the variable range and number of bits to fulfil the control requirements. This often implies the identification of symmetries, offset values and variable scales in [1]. The ADC resolution chosen for this application is 12 bit wise, which defines the initial scale of the internal variables.

This implementation is responsible for:

- User interface. 10 slider switches, 3 buttons, 10 LEDs and 4 1-digit 7-segment displays. Allows showing and modifying the system variables and parameters.
- Process the signal from the encoder.
- Interface with and process ADC signals.
- Implement the desired control and modulation algorithm.
- Implement safety measures.

A general view of the structure and system blocks is described in the Figure 7:

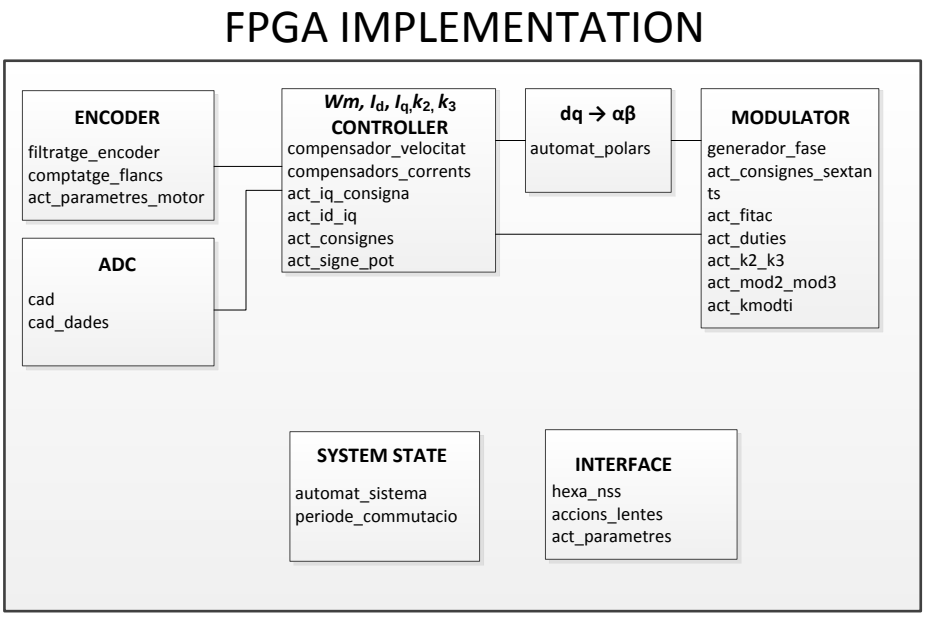


Figure 7. FPGA implementation diagram

In this figure the blocks are only stated for representation purpose, it is not an actual implementation division: the implementation is highly optimized, signals and timings from different blocks are often re-used to reduce the number of elements used. The names inside the blocks are different modules or process implementations, organized by functions identified in previous chapters.

2.3.1. Modes of operation

The operator can select 3 modes of operation: mode 0, mode 1 and mode 2. This corresponds to the number of control loops used. In mode 0, there is no controller other than the dc-link voltage stabilized. Is also referred to as “open loop”, where the sinusoidal frequency is fixed to 50.05 Hz and the modulation index is directly selected by the used, thus controlling the amplitude of the output signal.

In mode 1 the user selects the target current i_q, making the current controller active. This leads to a constant current output whose frequency is determined by the encoder angle.

Mode 2 refers to the full speed closed loop controller. When this mode is selected, the outer control loop is enabled. It is the purpose of this controller to establish a constant speed on the motor. The output frequency, current and modulation index is dynamically adjusted depending on motor variables.

2.3.2. Time unit

The system is fed by a 50 MHz clock that is used as basic time unit (20 ns) that fixes the maximum time resolution achieved by the system.

With this unit in mind, the blanking time, tb, is set to 40 TU (800 ns); the delay time, td, is set to 2 TU (40 ns) and the swithing time, ts, is set to 10.000 TU (200 us).

The ADC is also operated around this clock input, whereas its clock signal is only activated when the ncs pin is active at ¼ the clock frequency, 12.5 MHz (the maximum frequency for the AD7658 device is 18 MHz).

The encoder signals, explained later in this chapter, are also filtered at a lower sample rate (6.25 MHz).

2.3.3. Low frequency modules

There are two modules that operate at a lower input frequency: the button inputs and the 7-segments display.

The button inputs do not require a high update rate and by reducing its sampling frequency to 25 Hz, much of the "bouncing" effect is solved and a single clean pulse of one TU is generated each time the button is pressed.

This does not apply to the reset button, which generates the reset signal independently.

The 7-segment display is updated at even lower frequency, 3 Hz, as otherwise it will not be possible to distinguish any value by the human eye. Three times a second, the configuration updates the display content with data from either the operation mode, modifiable parameters or non-modifiable parameters.

The hexadecimal data is decoded into 7-segment format by a special purpose component, hexa_nss.

Note that when the data to visualize is fed from the analog to digital converter, it can happen that a wrong value is shown during a small amount of time. This is due to the fact that, in the implementation of the analog to digital serial data buffer, the data is not registered before passing into the internal variable (v_{21}, v_{32}, v_{43}, i_a, i_b) as it would require an extra clock time that will delay the processing time. The internal variable is actually a shift register.

As the 7 segment visualizes the data from the internal registers independently from the ADC conversion input, it is feasible that the visualization takes place while the shift register is feeding its data.

2.3.4. Error handling

The implementation includes safety measures to prevent the power converter from being damaged.

As explained in [7], the converter cannot be switched off or switched on in any order; one cannot simply disconnect all the driver signals as not all the power transistors will behave exactly in the same manner, causing higher blocking voltages than they are designed for. Instead, an explicit order must be followed that is implemented as an independent state machine in the *"automat_sistema"* process. This generates a signal, *"estat_sistema"*, which higher bits represent the enable column signal for the converter. That is, the fourth bit of *"estat_sistema"* represents the enable signal for the column closer to the dc-link voltages (formed by 6 devices); the third bit the second column and the second bit the last column (closer to the output). This latter "and" function is implemented in *"generador_fase"* component.

For this reason, the operator should never remove the power from the control logic while in on state before the power converter voltages.

The error signal is enabled when any of the error led signal is enabled (current overflow, encoder error, etc) and is held enabled until the system is restarted.

2.3.5. Encoder

3 signals are generated by the encoder: *A, B, INDEX0.* A motor rotation (mechanical, 360 degrees) generates 1024 pulses over *A* and B square-wave signals. One signal is delayed ¼ of a pulse regarding the other, which provides 4096 edges (12-bit resolution) and the rotation direction.

INDEX0 provides a pulse each time the rotor is at a certain position, that has a constant relationship with the motor windings that establish the abc coordinates reference plane.

Figure 8 is used to clarify these signals:

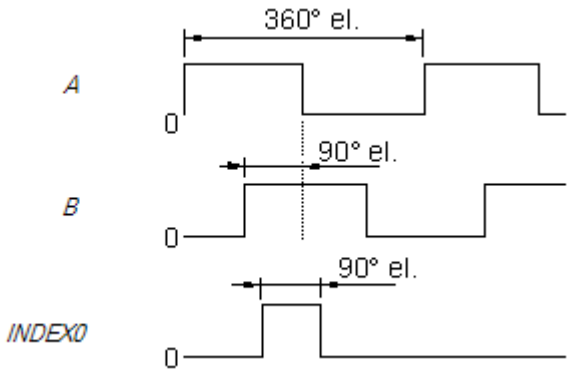


Figure 8. Encoder signal example.

The delay between these two signals allows to determine the direction of rotation and another pulse, *INDEX0,* determines when the rotor is at a certain position. This position has a constant relationship with the inductance that establishes the abc coordinates of the system.

This constant relationship is referred to as *c_angle_offset* and for this particular motor is established as 385 pulses. The electrical angle is required for the modulation scheme, takes this offset into account and increases its value every new pulse is obtained from the encoder. Also, the number of poles of the motor has to be taken into account, for this case a full mechanical rotation corresponds to four electrical rotations.

The signals coming from the encoder are sampled at 6.25 MHz and are checked to be constant for 8 or more samples. This reduces the noise or bouncing errors caused by the encoder signals.

The angular speed is then calculated with the filtered values of the encoder signals, once every 2.5 ms. To reduce the measured uncertainty, 4 values are stored in memory and averaged each new sample, achieving 1.5 rpm precision [11].

2.3.6. ROM Memory

Complex mathematic operations as sines, tangents, etc. are implemented as Look-Up Tables (memory). This memory is accesed by the logic module provided by Alterea

altsyncram, parametrized dual-port synchronous RAM, as single port ROM blocks (except the block containing the sines and cosines of ϕ, that is implemented in a single dual-port block). The input (address of the memory) is the input of the desired function while the output of the memory is the result of the operation. This is a very fast implementation of complex math functions, at the cost of memory block that otherwise would not be used.

As part of the altera_mf library (Altera Megafunctions), the Altera Cyclone III 3C16 [14] device contains 56 M9K blocks that each can be configured from 8192 positions of 1 bit to 256 positions of 36 bits each one.

As an example, the memory that stores the sine and cosine of ϕ and $(\phi + 60º)$ is configured as 1024 positions of 26 bits. These 26 bits contains the sine, 13 higher bits, and the cosine, 13 lower bits.

The content of this memory is generated by a c console program that generates an Altera compatible *.mif initialization file. This is done for every memory block contained in the project.

2.3.7. Target vector calculation

For the conversion of the target duty cycles into the reference vector for the modulation, a dq to αβ coordinates conversion (equivalent to a Cartesian to Polar conversion) must be performed:

$$m^* = \sqrt{(d_d{}^*)^2 + \left(d_q{}^*\right)^2}$$

$$\theta^* = \tan^{-1}\left(d_d{}^*, d_q{}^*\right) + \emptyset$$

This operation requires two square operations, an addition and a square root of the result for the case of m*; and an arctangent operation between two input vectors for the case of the reference vector angle.

For both operations (the square root and the arctangent) a successive approximation algorithm is employed. A memory room containing two input variables, in the case of 10 bit each one, would require 1,048,576 positions of 10 bits output, much more than available.

In the particular case of the m* calculation, this algorithm compares the product of the result and the result minus 1 with $(d_d{}^*)^2 + \left(d_q{}^*\right)^2$, modifying the result value according to this comparison.

In the case of the arctangent, the result is feed to a memory block that performs the tangent operation. Then this value (that is the result of tangent angle) is scaled with the maximum of $|d_d{}^*|$ and $\left|d_q{}^*\right|$ and compared to the minimum of them. This is done so the arctangent range is always lower than 1, so the resolution can be optimized:

$$\frac{y}{x} = \tan\theta = \frac{\sin\theta}{\cos\theta} < 1$$

$$y = x \cdot \tan\theta$$

Where x and y are $\max(|d_d{}^*|,\ \left|d_q{}^*\right|)$ and $\min(|d_d{}^*|,\ \left|d_q{}^*\right|)$ respectively.

2.4. Electric Motor

The power converter is intended to drive a permanent magnet synchronous motor (PMSM), model 1FT6105-8SB71-2AAD. This an 8 Pole (4 pair), Force-Ventilated, 1500 rpm rated speed motor.

The main advantages of this type of motor are high efficiency (no rotor currents), smaller rotor diameters, high torque per ampere constant and low rotor inertia. On the other side, as a synchronous machine, requires the rotor position sensing. The back EMF shape in this type of motors is sinusoidal.

Other relevant information for this project is the winding inductance (7.5 mH), winding resistance at 20 ºC (0.35 Ω), torque constant (2.97 Nm/A), voltage constant (189 V/1000 rpm) and optimum power (9.27 kW).

Other technical parameters are represented in the next image:

Technical data 1FT6, rated speed 1500 RPM

n_N [RPM]	M_0 [Nm]	M_N [Nm]	M_N 1) [Nm]	Motor type 1FT6–	I_0 [A]	I_N [A]	Connector size 2)	Cross-section 3) [mm²]	Cable type 4) 5) 6FX□002– 6)	Terminal box 2)
Non-ventilated										
1500	27.0	24.5	22.05	102-8AB7 □	8.7	8.4	1.5	4 x 1.5	5□S21-1 □□0	gk130
1500	50.0	41.0	36.9	105-8AB7 □	16.0	14.5	1.5	4 x 2.5	5□S31-1 □□0	gk130
1500	70.0	61.0	54.9	108-8AB7 □	22.3	20.5	1.5	4 x 4	5□S41-1 □□0	gk130
1500	75.0	62.0	55.8	132-6AB7 □	21.6	19	1.5	4 x 4	5□S41-1 □□0	gk230
1500	95.0	75.0	67.5	134-6AB7 □	27.0	24	1.5	4 x 4	5□S41-1 □□0	gk230
1500	115.0	88.0	79.2	136-6AB7 □	34.0	27	1.5	4 x 10	5□S61-1 □□0	gk230
Forced ventilation										
1500	65.0	59.0	53.1	105-8SB7 □	21.9	21.7	1.5	4 x 4	5□S41-1 □□0	gk130
1500	90.0	83.0	74.7	108-8SB7 □	30.0	31	1.5	4 x6	5□S51-1 □□0	gk130
1500	110.0	102.0	91.8	132-6SB7 □	36.0	36	3	4 x 10	5□S13-1 □□0	gk230
1500	140.0	130.0	117.0	134-6SB7 □	44.0	45	3	4 x 10	5□S13-1 □□0	gk230
1500	175.0	160.0	144.0	136-6SB7 □	55.0	55	3	4 x 16	5□S23-1 □□0	gk420
1500	425	385	347	163-8SB7 □ 8)	151	136	—	—	—	gk630
1500	600	540	486	168-8SB7 □ 8)	194	174	—	—	—	gk630
Water cooling										
1500	119.0	116.0	116.0	108-8WB7 □	43.0	43	3	4 x 10	5□S13-1 □□0	gk230
1500	155	150	150	132-6WB7 □ 8)	58	58	—	—	—	gk630
1500	200	190	190	134-6WB7 □ 8)	73	67	—	—	—	gk630
1500	240	230	230	136-6WB7 □ 8)	92	90	—	—	—	gk630
1500	300	290	290	138-6WB7 □ 8)	112	112	—	—	—	gk630
1500	450	450	450	163-8WB7 □ 8)	160	160	—	—	—	gk630
1500	700	690	690	168-8WB7 □ 8)	225	221	—	—	—	gk630

Figure 9. Motor technical characteristics.

3. Project development

3.1. Preliminary Tests

These tests were initially thought as an introduction to become familiar with the system. They were expected not to extend over the first month, performing a second row tests after the new design is completed, but due to time limitations this second row could not be repeated with the new designed circuit within the thesis work.

3.1.1. Initial prototype description

The initial prototype consists of an Altera DE0 board, a prototype bread board (containing the board the ADC, the encoder interface and power supply connection), a set of 3 voltage sensor boards and 2 current sensor boards and laboratory power supplies.

This setup is summarized, not including the power supplies, in the image below:

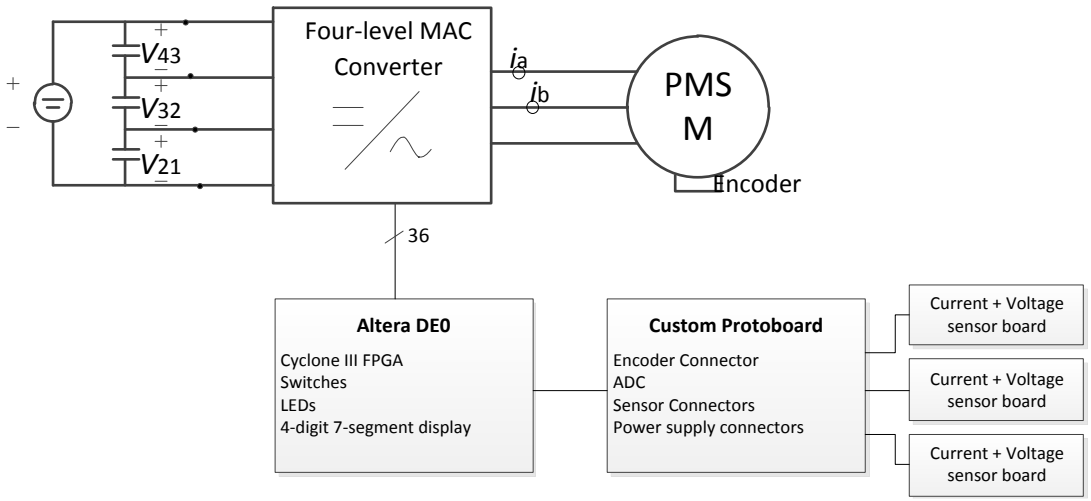


Figure 10. Initial prototype overview

As the DE0 board does not contain any analog to digital converter, a prototype bread board was developed that enclose an ADC, the interface to the motor encoder and the board power input connections. The connection to the DE0 board is made by two parallel shielded cables that interface to the two GPIO ports on the DE0 board.

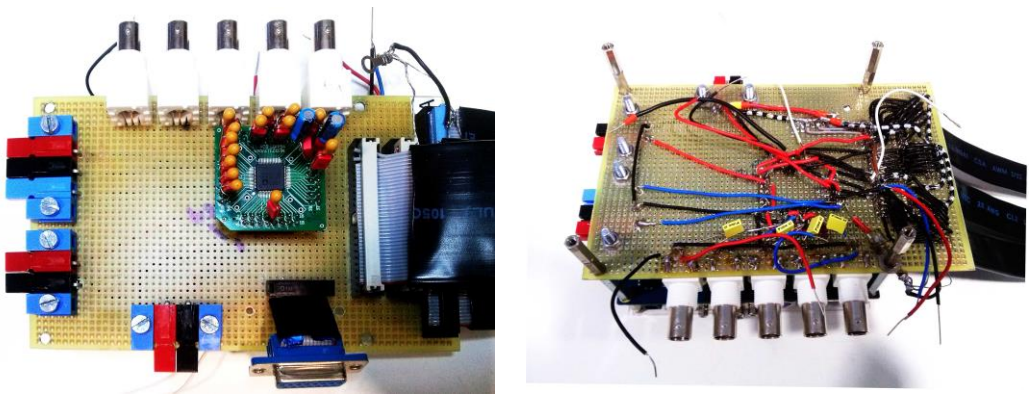


Figure 11. Prototype bread board. Top and bottom view

The ADC chip selected was the AD7656BSTZ, from Analog Devices Inc., that contains six 12 bit bipolar successive approximation (SAR) ADC modules. It is important to clarify that this chip does perform 6 analog to digital conversions at the same time, compared to other devices that contain more than one “analog channels”, but may only operate one at a time (they actually contain only one analog to digital converter module that multiplexes their input channel). That feature was explicitly required, as it is intended to update the system variables simultaneously and once at a time next to the duty cycle update.

This device is provided in a 64-lead LQFP (Lead Low Profile Quad Flat Package), package with 0.5 mm pitch between leads. That means that it cannot be directly interfaced to the 2.54 mm pitch bread board used in the first prototype, so a SMT breakout board was employed. The required decoupling capacitors suggested in the datasheet were soldered directly to this breakout board and a complex wiring has been performed below the breadboard, as shown in Figure 12.

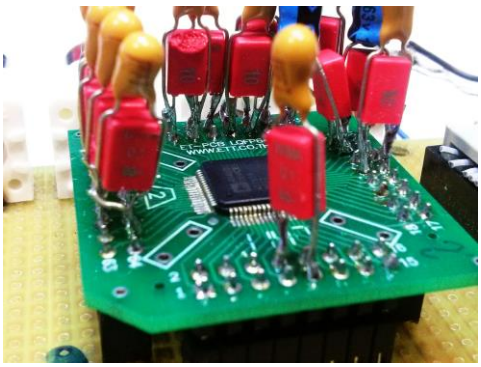


Figure 12. ADC board detail.

For this early stage, the power required for the ADC and the encoder comes from the standard laboratory power supplies. The ADC requires ±15 V, +5 V for the analog circuitry and +5V for the digital interface. Also, a 3.3 V voltage is required to “drive” the digital signals (the voltage at which the FPGA IO operates).

As the ADC datasheet suggests, as well as in reference [12],the ADC signal and digital grounds can be tied together with a small performance decrease in devices with low digital currents: “the analog plane is not corrupted because the small digital transient currents flow in the small loop between Vd, the decoupling capacitor, and DGND” [5]. This is the solution chosen in the initial prototype, but as it will be studied in chapter 2, resulted in poor performance and critical errors in the analog values.

Furthermore, the analog signals were measured by means of current and voltage sensors mounted on external individual boards (already available by GREP) , shown in Figure 13, that also required analog power supplies. The prototype does not include any ground plane nor any separation between analog and digital ground, so when connecting the reference point for the sensors it is very likely that the signal will get corrupted.

These boards contains isolated current and voltage sensors from LEM, and their output frequency components are limited by a low pass filter of cut-off frequency $f_s/10$, where f_s refers to the power converter update frequency and is fixed to 5 kHz; so the filter cut-off frequency is 500 Hz. This way, the filter also acts as anti-aliasing filter for the analog to digital converter as well.

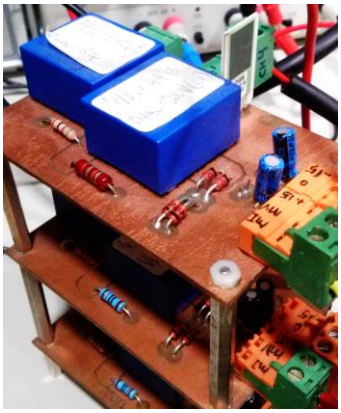


Figure 13. Sensor boards.

The ADC can be interfaced as 1, 2 or 3 channel serial mode or 12 bit parallel interface. Due to the IO constraints on the DE0 board, the 3 channel serial mode was employed. The ADC captures the 5 input variables at the same time and stores this conversion result until it is obtained by the serial communication channel.

The reference voltage V_{REF} can be configured to 5 V, 2.5 V or externally, so the signals that can be fed to the ADC are $\pm 2 \cdot V_{REF}$. The initial prototype was fixed to 2.5 V internal reference voltage, so the range is ±5V. The selected ADC has 12 bits resolution, the current sensor has a configured nominal range of ±12.5 A (±5 V), so the resolution is 6.1 mA. For the voltage sensors, the resolution is 0.108 V as the range is configured for ±222.2 V.

This module (ADC) was later replaced in the final prototype by the AD7656-1BSTZ, as it requires less decoupling capacitors at the price of slightly less bandwidth. A more detailed description is enclosed in chapter 3.2

3.1.2. Tests performed

3.1.2.1. Open loop, RL load

The system is tested first with a RL load that models a PMSM motor with zero angular velocity. A three phase balanced RL load is connected to the three phase converter outputs.

This allows checking the waveforms of the MAC converter MOSFET gate signals. Due to the DC-link balance controller, the system tries to rectify the duty cycles to balance the DC-link voltages. This behaviour can be shown when, for a constant target modulation index, m^*, depending on the DC-link voltages the duties are modified.

It can happen that, depending on the target modulation index, the output is never connects to the outer rails (V_4 and V_1), contrary to the inner rails mandatory connection [3].

In the image bellow, an example were the modulation is connecting to the four possible levels is shown (blue line). The red, green and pink lines represent the DC-link voltages, scaled at a different voltage. It can be seen that the proposed implementation does balance the DC-link voltages actively.

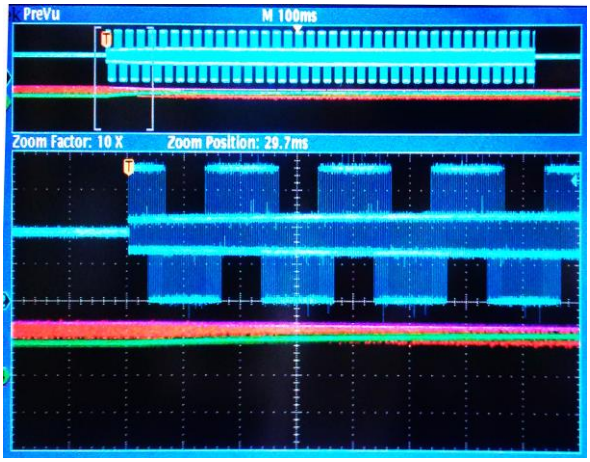


Figure 14. 1 Leg output not filtered, DC-link bus voltages

The stability of the voltage controller was checked with different compensator constant, k_{p3}. First, it is checked the correct operation with and without load when the compensator constant is zero. Then, the compensator constant is increased while the target modulation index is fixed to 0.36. The results are shown in the table below and in Figure 15:

k_p3	v21 (V)	v32 (V)	v43 (V)	Stable
Stop	70.5	44	78.9	y
1	67.2	53	72.3	y
3	66	56.9	71.1	y
5	65.8	58.6	65	y
7	65.3	59.9	64.3	y
9	64.8	60.6	63.9	y
11	64.7	61.1	63.7	y
13	64.4	61.6	63.3	y
15	64.3	62.1	63.2	y
17	64.2	62.3	63.2	y
19	64.1	62.5	62.8	y
21	64.1	62.8	62.6	y
23	63.9	62.9	62.8	y
25	63.8	62.9	62.8	y
27	63.8	62.9	62.7	y
29	63.8	63.2	62.4	y
32	63.7	63.2	62.4	y
48	63.5	63.7	62.3	y
64	63.4	63.9	62	y
80				n

Table 1. Voltage balance controller results

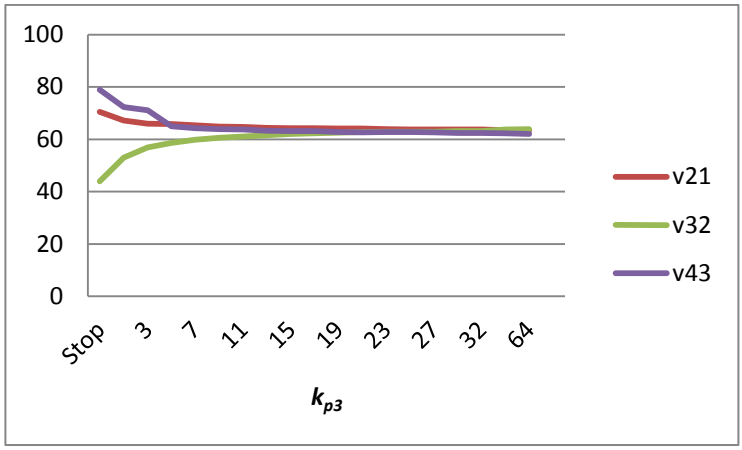


Figure 15. Voltage bance controller results.

As expected, the difference between the voltages decreases as the proportional term increases. There is no integral term, so this error is maintained. The response of the controller is relatively fast, being stable in less than 3 electrical cycles (50 Hz) yet in the lowest values of k_{p3}. The system became instable for values bigger than 80.

This unstable behaviour can be seen in the figure below:

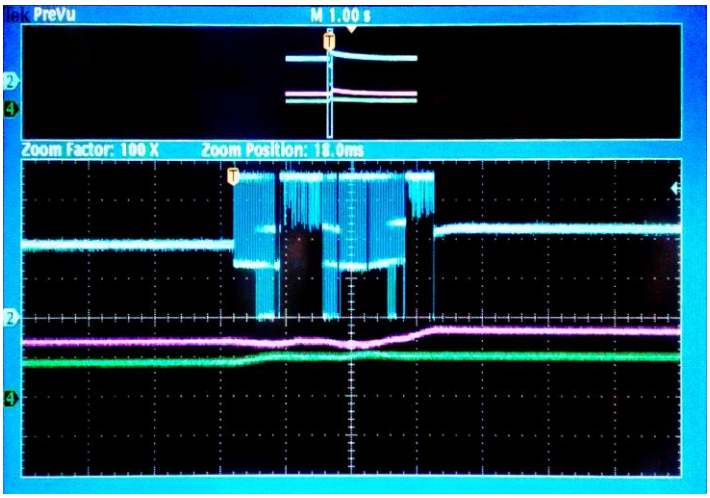


Figure 16. Unstable DC-link voltages

3.1.2.2. Open loop, motor load

When the current controller behaviour is checked, a series of tests are performed on the real motor.

Initially, the motor is fed with a three-phase 50.05 Hz sinusoidal current with modifiable amplitude. This open loop speed resulted in a system not able to synchronize with the rotor, as its rotor inertia required to ramp from 0 Hz to the required speed. Note that this frequency is referred to the electrical frequency, the actual motor speed is four times inferior (the motor presents four pole pairs).

For this reason, the open-loop controller was modified setting the electrical frequency to 2.5 Hz, so a complete rotor turn is completed in 1.6 seconds, much more feasible. This modification is described in the “FPGA configuration modifications” chapter.

With this angular speed, the control performed as expected. However, there is no user-control on the current being feed to the motor (especially at the initial states when it is stopped); the only control is related with the modulation index, the rotor speed (back EMF) and the motor winding inductance. The control loop is active, but resulted that was too aggressive and forced a current close to the current limits, so an over current error arose because of the current ringing and coupled noise into the measure. Only with very low modulation index we were able to correctly make the motor rotate.

3.1.2.3. Current closed loop, motor load

In this case, care must be taken as there is no limitation in the rotor final speed. Theoretically, it will be increased indefinitely only limited by its own friction.

When performing the test, the motor got stuck in 8 constant points. The motor started to move, and suddenly stopped. If forced to move on, then the rotor goes on until the next point.

This behaviour was incorrectly interpreted as an error in the control loop or in the system variable feed. Investigating this error, the encoder angle was checked and modified to ±45º with no positive results. Also the algorithm equations were revised and checked.

Finally, the problem was tracked to the power converter output sequence that resulted to be not aligned with the motor phases. In a PMSM motor, the abc components require to be in the exact physical position as the controller implements them, so all the dq and αβ transformations are correctly interpreted. Otherwise, as it was happening, the rotor will start moving according to phase a-b-c sequence, and stuck in the frontiers of them (sequence b-a-c for example)

When correctly sequenced, the current control algorithm performed as expected.

3.1.2.4. Angular speed closed loop, motor load

The outer loop, which controls the motor speed, requires the encoder input and can only be tested with the motor load.

As in the open loop example, the current required to start the rotor at a very high speed exceeds the possible values. Although the current is limited, the noise in the system prevented to use values close to the maximum ones.

For this reason, the motor was started using very low speed values and then speeded up manually with the control interface.

The motor, employing this power controller, can act as a generator but there is no provision on the dc side for this mode of operation. Any energy recovered from the motor will be stored in the capacitors or absorbed by the power supplies, so it is not recommended to suddenly stop the rotor with the controller, but instead slow down progressively until stopped.

The angular speed controller was tested also in different load scenarios: with no load and with a torque braked.

3.1.3. Problems encountered

Numerous problems rose during this phase. The main ones are exposed in this section.

3.1.3.1. AD7656

The ADC showed two problems not referred in its datasheet.

The first one was related to initialization. The first conversion value does not take into consideration the range pin voltage, so the range is ±10 V instead of ±5 V. The behaviour of the FPGA configuration was changed so that the first conversion after reset is discarded.

The second one was that the ADC showed random wrong values (for the sensed currents and voltages) that are being repeated from time to time. These values are generally the same: 0x4000, 0xBFFF, etc (hexadecimal codification). This problem is tracked to either noise issue on the input or wrong ground topology.

As it is a SAR ADC, it can happen that a very high noise peak on the input makes the first (and most significant value) bit to be incorrectly identified and the other bits set to the complementary values to compensate for this error.

However, it must happen at the exact time on all the inputs and only in the first bit, which considering the sample time (3.5 us), it is unlikely to happen so often.

Other users have reported similar problems with this chip [15], “A common mode choke used between digital and analog ground allows noise spikes from the power supply to show up across analog and digital ground. The issue does not appear when the common mode choke is removed/shorted.” For this reason, in the final prototype the analog and digital ground planes are split but room for an inductor has been reserved.

This latter problem prevented the system to start eventually, as in the first switching cycles an error took place and required a complete system restart.

3.1.3.2. DC-link off voltages

When the power converter is in off state, each DC-link voltage is connected to different number of transistors [7]. As a MOSFET in off state can be modelled as a high value resistance, then the DC-link capacitor voltages became unbalanced. Also, other components as the drivers supply have a non-linear response and contribute to this unbalance.

This unbalance situation is mitigated by the inclusion of compensation resistors that aims to equalize the voltages, but does not solve it completely.

This forced us to use values of about 170 V in the DC-link bus. Less voltage would make the driver self-power circuitry stops working (as requires at least 30 volts at each DC-link capacitor [7]). Higher voltage is dangerous for the MOSFET, as in this case are 100 V rated.

3.1.3.3. Noise issues

The system presents sporadic noise peaks in the analog sensor outputs that propagate to the ADC conversion values. It is also present in the DC-link voltages, with amplitude of 2 V. However, it represents a small fraction when compared to the DC-link voltages, that, when measured after the sensor, its value is comparable with the DC-link sensed values.

The noise was investigated but a clear propagation channel could not be established. The detected frequency is near 15 ns period and its weight depends on the modulation

index. This can be due to the fact that the ADC sample time may match in time with the power transitions.

If the driver digital power source (that comes from the prototype board) is disconnected, the noise is not coupled anymore. It is clear then that is not caused by any external source.

An additional input filter (cut-off frequency of 500 Hz) was placed in the ADC conversion inputs that should mitigate the noise if it is radiated into the sensor cables. However, the result was not as positive and only a small part of the noise was removed.

As the system is only composed by a single ground connection (not a ground plane, nor analog only plane), it is feasible that the noise can be conductively coupled from the power converter.

To be able to test the system, 3 independent power supplies were used instead of a capacitor divider improving the noise margin in the sensed voltage.

3.1.3.4. Open loop speed

As previously stated, the open loop frequency was excessive without a proper speed-up ramp.

3.1.4. FPGA configuration modifications

Small modifications were performed into the FPGA code.

The open loop speed was modified by the *delta_fita_0* variable that is the amount of angle that is increased each time. The output frequency is calculated as:

$$freq_0 = 5^8 \cdot \frac{delta\_fita\_0}{128 \cdot ts\_4tck}\ Hz$$

Each time an error caused by the noise or an ADC error (explained previously) the system needed a full restart, that would remove the motor rotor synchronization angle and any custom values entered (k_p, ω^*, etc). This resulted in a time-consuming task, so the configuration was modified to perform “soft-restart” that only resets the current and voltage errors if the error was caused by a voltage o current overflow and a “full-restart” otherwise.

No debugging capabilities were defined in the initial states of the project, but as project evolved it resulted evident that a debugging method was imperative. The Altera SignalTap II was selected for the task [17], as is already included in Altera Tools and can be included in a design without changing the implementation (does consume logic elements, it is not a hard-IP block). Among other features, enables to visualize internal variables of the FPGA though the JTAG port in a Logic Analyser in the computer (.

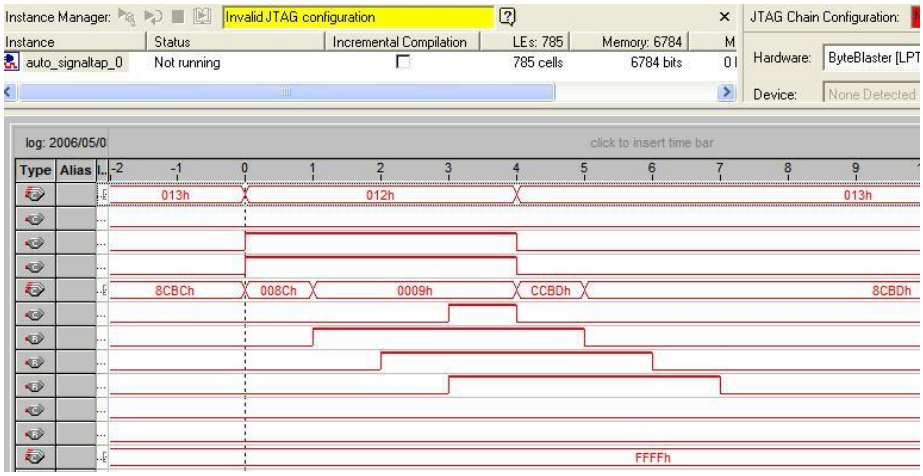


Figure 17. Example of SignalTap II waveform inspector

It also can output variables to the output port, feature used to synchronize a mixed-oscilloscope and capture the serial data, control lines and input waveform at the exact moment an overflow occurred. This way we obtained a precise information of what was happening when an error occurred, storing the current, voltage or other system variables.

3.2. Electrical Design

3.2.1. System overview

A PCB custom board will be developed taking into account lessons learned in the testing phase. It will consist on a single board that includes all the possible circuit elements, including the FPGA, analog to digital converter, encoder interface and analog sensors and signal conditioning circuits.

It is important to remember the main objectives of this design: reduce conductive and radiated noise in the analog circuitry and improve the system robustness (reducing power connections, among others).

Also, the circuit will contain configuration jumpers and extra components (initially not populated) that make the board more versatile and can enable the possibility to test new features of the circuit.

Full schematics can be found in the Annexes.

The design is fully hierarchical, employing separate ground labels for each sheet. The local ground and power labels are then connected to the desired global label, generally in the lower left corner of the sheet. This is done in this way to keep a total control over the sheet power rails, preventing errors due to incorrect global label selected (as it is much clearer this way). An example of this notation can be seen in the image:

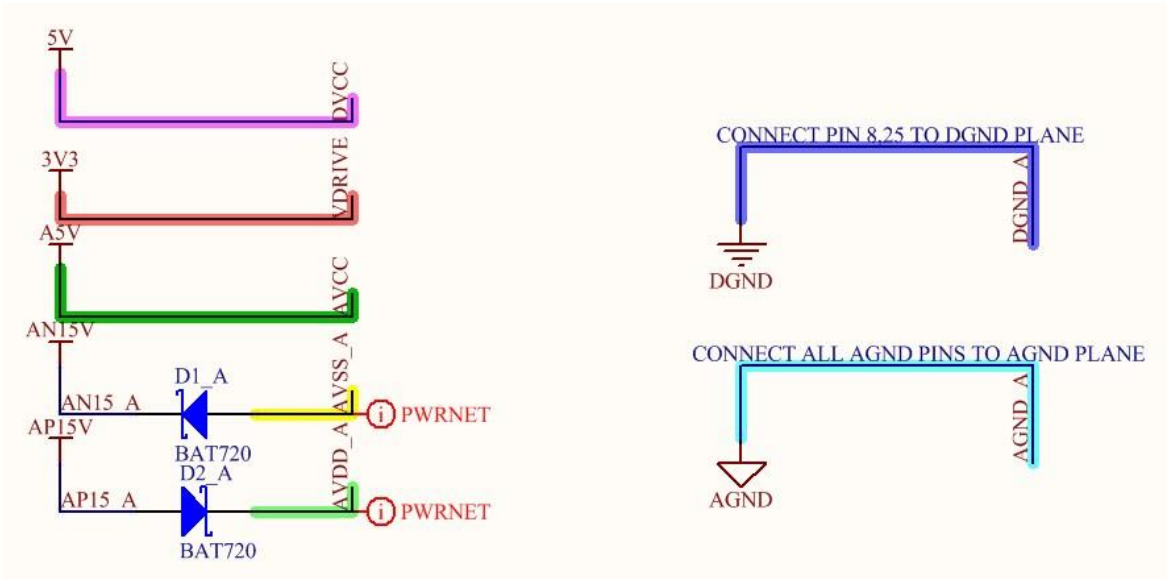


Figure 18. Power nets on schematics

Note that the power nets are tinted in each schematic for easier reading. The colours exposed in the image below are maintained over all schematics (they represents the same power net unless otherwise stated).

As will be detailed in the power supply chapter, the design employs two different ground planes: DGND and AGND. DGND, digital ground, is used in the FPGA and all the digital components. AGND, analog ground, is used only in the ADC analog parts and analog sensors and signal conditioning circuits.

3.2.2. FPGA Selection

Several FPGA manufacturers are reviewed to compare the state-of the-art in FPGA devices. However, it is not always easy to compare different families from different manufacturers. A more deeply comparison should port the current configuration to each attractive family and compare the timing, power consumption and resources reports generated by each FPGA manufacturer tool. This is not feasible nor in the scope of the current thesis.

The requirements for the FPGA are, mainly, the number of logic elements available (but this can vary depending on the manufacturer logic element definition), the memory available, the number of user configurable input/output pins and the device speed grade. The latest parameter is the hardest part to evaluate, as it depends on the specific technology and architecture of the chip.

The former implementation uses 101 pins, 7.305 logic elements. 299.520 memory bits, 76 embedded 9-bit multipliers and requires a speed grade -6 from Altera (the fastest) to run on a Cyclone III at 50 MHz. No PLL are used for this purpose, but it is possible that other applications (as grid power conversion in αβ plane) do require at least one. There are no requirements on differential pairs, high speed memory controller or high speed transceivers so those FPGAs including those elements are not taken into account.

The new implementation will require 123 pins as a new user interface is used as well as parallel ADC connection. The number of logic elements is expected to increase as new functionalities are included into the FPGA, or new algorithms from other research groups are included. As an example, a white paper example implementation from Altera [16] states that the required resources for a FOC controller are much higher than our implementation:

	VVC Controller	DTFC-SVM IPM Motor Controller	FOC Generator Controller	Complete Design	Cyclone FPGA Resources
LEs	2,344	19,560	7,976	29,880	39,600
Multipliers (18 x 18)	34	59	20	113	116
M9K Memory	—	27	17	44	126
f_{MAX}	—	101 MHz	98.4 MHz	98.4 MHz	—

Figure 19. FOC control implementation resources.[16]

Also the FPGA package is an important feature, as defines the technology required to fabricate the printed circuit board and the number of user input output. Note that while BGA offers a wide number of user IOs, there is a limited amount of them that can be acceded from a routing point of view, depending essentially on the number of layers used in the board and its technology.

3.2.2.1. Lattice Semiconductor

Lattice offers three product families whose specifications match the desired ones, FE2M, XP2 and LFE3.

LFE2M50E-5FN484C: 48k Le, 4147 kb RAM, 8 PLL, 260 user IO and 88 Multipliers 18 bit. Retail price: 118.66€ (as of 2014/02/01).

The downside of this device is that the package is 484 FPBGA, with pitch size lower than 1mm. Also, it is not the fastest speed grade available for this manufacturer.

LFXP2-17E-6QN208C: 17k Le, 276 kb RAM, 4 PLL, 146 user IO, 20 Multipliers 18 bit and 5 SysDsp. Retail price: 41.25€ (as of 2014/02/01).

This device is shipped in 208-PQFP that can be soldered with conventional equipment, however 20 multipliers and 5 “SysDsp” may not be enough and further investigation is required.

LFE3-35EA-7FTN256C: 33k Le, 327 kb RAM, 4 PLL, 133 user IO, 64 Multipliers 18 bit. Retail price: 68.42€ (as of 2014/02/01).

This device offers more multipliers and logic elements. It is shipped in standard 256 BGA package (1mm ball-pitch).

3.2.2.2. Xilinx Inc.

Xilinx, as well as Altera, is supported by “FPGA Design and Codesign Resources” from Matlab. This includes HDL Coder and HDL Verifier that enables the generation of HDL code from Matlab and Simulink models. It is not used in this project, but may represent an interesting feature in the future.

Only the families Artix 7 and Spartan 6A are evaluated, other higher end families exceeds the cost budget.

XC7A35T-2FTG256I: Artix 7. 32 kLe, 1800 kb RAM, 5 PLL, 170 user IO, 90 DSP Block. Retail price: 43.04€ (as of 2014/02/01).

Each DSP block contains a 25x18 bit multiplier, an adder and an accumulator. This device is speed grade -2, and also contains a 12 bit ADC. This is shipped in standard 256 BGA package (1mm ball-pitch).

XC6SLX25-2FTG256C: Spartan 6A. 24 kLe, 936 kb RAM, 2 PLL, 186 user IO, 38 DSP Block. Retail price: 32.23€ (as of 2014/02/01).

This device only contains 38 DSP blocks, may fall too short for the application.

3.2.2.3. Altera Inc.

The Cyclone III device, yet not obsolete, family is not anymore supported by Quartus II Software.

The MAX 10 family looks appealing, as does not require a configuration memory and can be operated from a single supply which simplifies a lot the board design and reduce costs Also contains a 12bit 1 Msps SAR ADC with up to 18 analog input channels. This is not a six channel parallel ADC as the one used in the initial design, but is 4 times faster and does not require external connection. The major drawback this ADC is single-ended (not bipolar) and would require a major revamp of the sensing circuitry.

As of February 2015, only the device with 8 kLe is available only containing 24 18x18 bit multiplier. For this reason, this family was discarded.

Similarly to Xilinx, only the lower cost families are evaluated: Cyclone V and Cyclone IV. As in this case we do have access to the timing requirements, each device is checked with Quartus timing reports. This analysis showed that, independently of the FPGA family, it is required a -6 speed grade device to fulfil the timing specifications for 50 MHz.

As of February 2015, only the Cyclone IV family was available as -6 speed grade at the distributors available.

EP4CE22F17C6N: Cyclone IV. 22 kLe, 594 kb RAM, 4 PLL, 153 user IO, 66 18x18 bit multiplier. Retail price: 63.10€ (as of 2014/02/01).

Packaged in standard 256 BGA package (1mm ball-pitch), this device is similar to the EP3C16F484C6 device being currently used but improving it performance.

3.2.2.4. Selected device

Taking into consideration all the factors described, the EP4CE22F17C6N device is selected as the best suited for the application. It represents a major step-forward from the current generation, allowing room enough for future algorithm changes whereas keeping the porting effort low.

In this device, the closed-loop implementation takes up to 32% of the logic elements, 80% of the user IO pins, 33% of the total RAM blocks and 32% of the embedded multipliers. The worst case timing analyser result shows a 58.03 MHz max frequency for this design in the Cyclone IV device.

However, this device is the biggest-size in terms of number logic elements that is produced with the BGA256 packaging. This is a restriction of the design, as we will not be able to change only the FPGA if more processing power is required (process known as migration).

Only the XC7A35T-2FTG256I device seems suited for the application, but the speed grade uncertainty and the porting effort required to change from one vendor to another does not make it the best option for this design.

3.2.3. FPGA design

3.2.3.1. Configuration memory

This subchapter covers the EPCS (Configuration Memory) – FPGA connection. This connection allows the FPGA configuration each time it is powered up.

The amount of storage memory required for the full FPGA configuration is listed in [18], for the specific case of the EP4CE22, is 5,748,552 bits. However, it is very unlikely that the implementation make use of all the resources of the FPGA (as the maximum frequency will decrease) and also, because the configuration scheme selected, the configuration data can be stored compressed.

The configuration scheme is selected to be “Single-Device AS Configuration”. MSEL pins are set according to [18] so they describe: “AS configuration scheme, standard POR delay, 3.3 Configuration Voltage Standard”. The electrical connection for this scheme is described in the image:

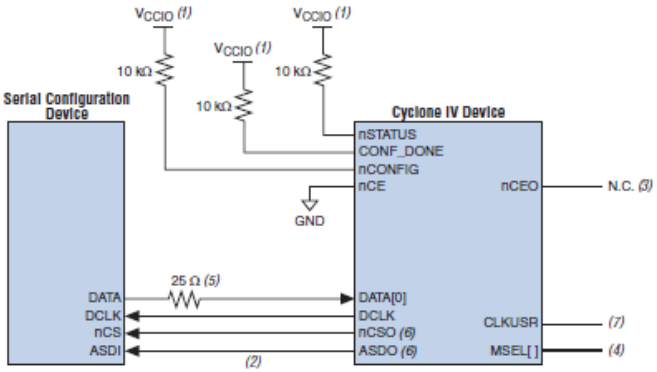


Figure 20. EPCS schematic from [18]

According to [18], the EPCS DCLK input frequency must be between 20 MHz and 40 MHz. The Cyclone IV device uses DCLK and DATA [1] pins to send operation commands and read address signals to the EPCS device. The EPCS device provides data on its DATA pin, connected to DATA[0] input on the Cyclone IV device. After configuration, these pins are set as input tri-stated.

If it is required, the remaining free-space of the configuration device can be used as static memory to store information/variables that will be preserved even after power off.

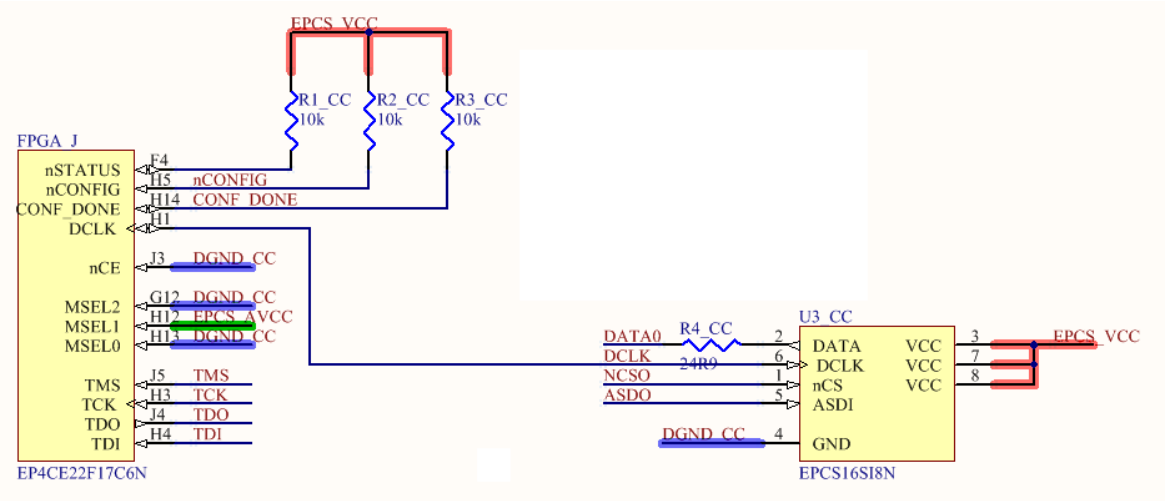


Figure 21. Actual EPCS schematic.

The layout is showed in Figure 21. Note the 24.9 Ω resistor matching near the EPCS device, as recommended by the EPCS datasheet. This is done as the output resistance of the DATA pin is about 25 Ω, so the generator is adapted to the transmission line (if 50 Ω transmission line used).

Also, the layout should comply the recommendations from the EPCS device specifications: DATA0, DCLK, nCSO, ASDO maximum length of 254mm; maximum capacitance of 30 pF (15 pF for DATA0).

3.2.3.2. FPGA configuration

This subchapter covers the PC – Board connection. This connection allows the user to configure the device.

Most evaluation boards include an on-board JTAG compatible with Altera tools. This device is based on a USB transceiver and a MAX II EPM240 CPLD, similar to USB-Blaster device from Altera. The configuration of this device is not publically available and cannot be used without licensing from Altera.

Some open source alternatives have been developed [19], but the compatibility with Altera tools is not guaranteed. As the project make extensive use of SignalTap II in-system debugging, fully compatibility between the board and Altera Tools is critical.

For these reasons, a JTAG header in combination with Altera USB-Blaster (USB based JTAG adaptor) cable is used.

According to [18] there are 3 possible interface schemes:

- Only 1 JTAG connection directly to EPCS device. This will configure the EPCS device. This configuration will be non-volatile (is preserved after power disconnection). A hot/fast/volatile configuration is not possible (configure directly the FPGA from the JTAG interface. The debug tools will not be available as there is no JTAG connection to the FPGA.
  The result schematic is as follows:

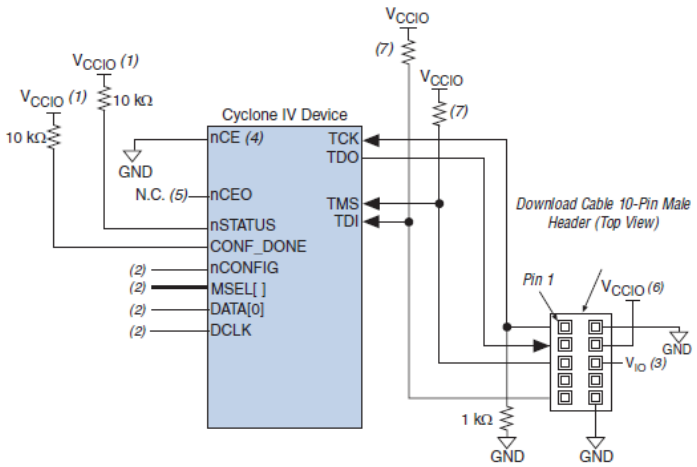


Figure 22. JTAG option 1

- Use 2 independent JTAG, one connected to the EPCS memory and one connected to the FPGA. This is the more versatile solution, but requires two JTAG headers and extra components. Also, can be confusing for the end-user.
  The result schematic is as follows:

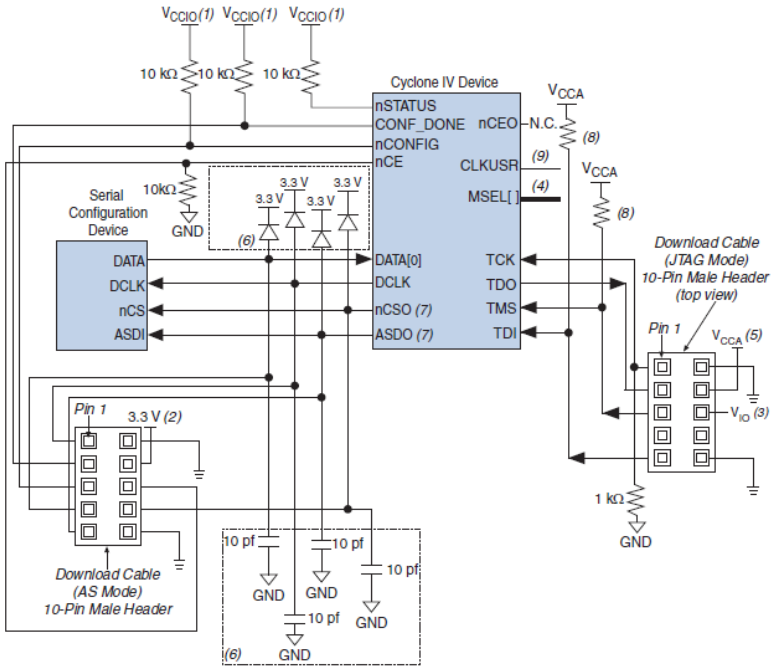


Figure 23. JTAG option 2

- 1 JTAG connected only to the FPGA. The serial configuration device can be programmed in a non-volatile way by the SFL (Serial FlashLoader) method [20]. By means of an IP block, the FPGA acts as a bridge between the JTAG interface and the EPCS device. This method is a bit slower, as requires configuring the FPGA to act as a bridge, but has all the benefits of the two-JTAG method without its drawbacks. It is also possible to use SignalTap II or other debug methods with this scheme.
  The result schematic is as follows:

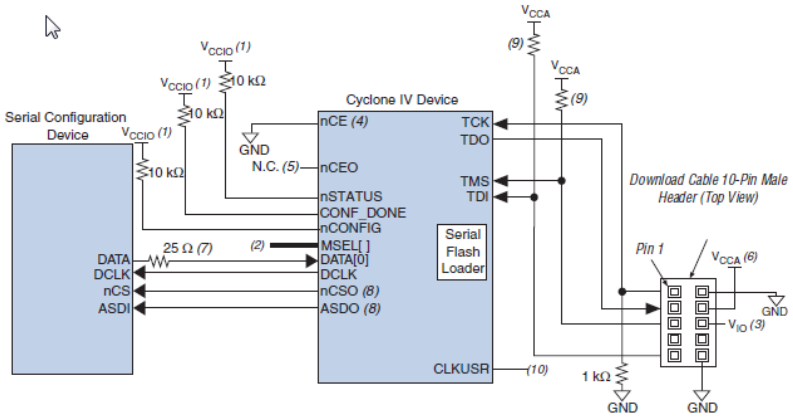


Figure 24. JTAG option 3

The latter is selected as the best-fit architecture for our project: only one JTAG header is required, simpler connection and is able to debug the FPGA.

3.2.3.3. Clock

GCLKs drive throughout the entire device, feeding all device quadrants. All resources in the device (I/O elements, logic array blocks (LABs), dedicated multiplier blocks,and M9K memory blocks) can use GCLKs as clock sources. Use these clock network resources for control signals, such as clock enables and clears fed by an external pin. Internal logic can also drive GCLKs for internally generated GCLKs and asynchronous clears, clock enables, or other control signals with high fan-out.

The clock signal is generated by a 50 MHz crystal oscillator connected the global clock input CLK6. This input is selected amongst other global clock input because the layout is simplified. Also, it is recommended that the reset input signals and other high fan-out input signals to be connected in these global clock input ports.

3.2.3.4. Power decoupling

The FPGA must be properly decoupled to operate correctly. For this specific task, Altera provides the “PDN Tool” (Power Delivery Network Tool) [21].

An estimation of the FPGA power consumption is needed. This can be generated by the PowerPlay Early Power Estimator or with the Altera Quartus II PowerPlay Power Analyser. The first one is an estimator to be used in the early stages of development, where you have a rough idea of the resources that will be used. Then, the tool generates an estimation on the minimum current requirements for all the power supply rails.

In our case, as the algorithm was already implemented, the VHDL project was ported to Cyclone IV in Quartus II. The power consumption reports from PowerPlay Power Analyser are used as they are expected to be closer to the real values.

The basic element of the PDN Tool is the target voltage rail impedance, calculated as follows:

$$Z_{target} = \frac{VoltageRail \cdot \left(\frac{\%Ripple}{100}\right)}{MaxTransientCurrent}$$

Also, the tool suggest a frequency for PCB decoupling, $F_{effective}$. Beyond this frequency, the PCB decoupling does not result in a system PDN profile improvement.

To be able to decouple every frequency below this frequency ($F_{effective}$), a set of parallel capacitors must be employed. This is due to the self-resonant frequency of each capacitor:

$$F = \frac{1}{2} \cdot \pi \cdot \sqrt{LC}$$

Were L represents the equivalent series inductance. As can be seen in the chart below, this term limits the effective frequency that is able to act as a capacitor. Beyond the resonant frequency, the capacitor acts as an inductor.

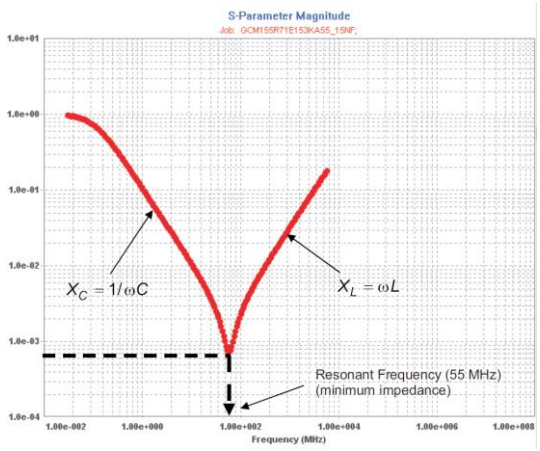


Figure 25. Capacitior Impedance over frequency.

All the voltage rails will be driven to 3.3 V, as all the peripherial devices works at this voltage. The PLL digital supply, as the specifications recommends, is shared with core 1.2 V supply with proper isolation filters. The 3.3 V, 1.2 V and 2.5 V voltage rails are generated independently one from another. This system voltage rails information is configured in the PDN tool:

		Group #	1	2	3	4
		Regulator / Separator	switcher	switcher	filter	linear
		Parent Group	none	1	2	1
Rail	Voltage	I max				
VCCA1	2.5	0.01				x
VCCA2	2.5	0.01				x
VCCA3	2.5	0.01				x
VCCA4	2.5	0.01				x
VCCD_PLL1	1.2	0.002			x	
VCCD_PLL2	1.2	0.002			x	
VCCD_PLL3	1.2	0.002			x	
VCCD_PLL4	1.2	0.002			x	
VCCINT	1.2	0.2		x		
VCCIO1	3.3	0.116	x/related			
VCCIO2	3.3	0.116	x/related			
VCCIO3	3.3	0.016	x/related			
VCCIO4	3.3	0.016	x/related			
VCCIO5	3.3	0.016	x/related			
VCCIO6	3.3	0.016	x/related			
VCCIO7	3.3	0.016	x/related			
VCCIO8	3.3	0.016	x/related			

Figure 26. PDN Tool. Voltage rail configuraion.

Also, the board stackup information from the board manufacturer is defined (Explained in chapter 3.3). In this case, all the dielectric material is made up from FR4, being the centre of the board the core of 1.2 mm:

Full Stackup					
Layer	Material	Dk	Thickness	Type	Pwr Planes
1	Copper		2.755	Signal	
	pre-preg	FR4	6.889	pre-preg	
2	Copper		2.755	Power	target
	pre-preg	FR4	47.24	pre-preg	
3	Copper		2.755	Power	reference
	pre-preg	FR4	6.889	pre-preg	
4	Copper		2.755	Signal	

Figure 27. PDN Tool. Layer stackup

Other board details, like capacitor ESR and ESL values and a small plane capacitor below the FPGA are introduced to the calculator.

Then, by looking at the impedance response of each rail, the capacitors are selected:

Decoupling Caps				Rail Group Quantity			
Value (µF)	Footprint	Layer	Orientation	1	2	3	4
0.001	0603	BOTTOM	VOS	0	0	0	0
0.0022	0603	BOTTOM	VOS	0	2	0	0
0.0047	0603	BOTTOM	VOS	0	2	0	0
0.01	0603	BOTTOM	VOS	0	2	0	0
0.022	0402	BOTTOM	VOS	0	0	0	0
0.047	0603	BOTTOM	VOS	0	0	0	0
0.1	1206	BOTTOM	VOS	8	8	4	4
0.1	0603_X2Y	BOTTOM	VOS	0	2	0	0
0.47	0603	BOTTOM	VOS	2	2	0	0
1	0603	BOTTOM	VOS	0	0	0	0
2.2	1206	BOTTOM	VOS	0	0	0	0
4.7	1206	BOTTOM	VOS	0	0	0	0
10	1206	BOTTOM	VOS	0	0	1	1
100	Custom	BOTTOM	VOS	1	1	0	0
0	0603	BOTTOM	VOS	0	0	0	0
0	0201	BOTTOM	VOS	0	0	0	0

Figure 28. PDN Tool. Capacitor selection.

Note that this is the result of numerous iteration loops between the tool and the final layout. The smallest size for the components selected is 0603, as a smaller size makes it very difficult to hand-solder.

The capacitor ESL depends on the mounting inductance, and should be considered when designing the layout.

In the designer system, special purpose capacitors have been used for the highest frequencies decoupling (near 50 MHz):

- 0306. Labelled as Low Inductance Capacitors, it shape is different from the traditional 0603 capacitor where the connections are on the narrow side, in a 0306 the connections are placed in the wider side decreasing the effective ESL and ESR. The image shows the capacitor selected:

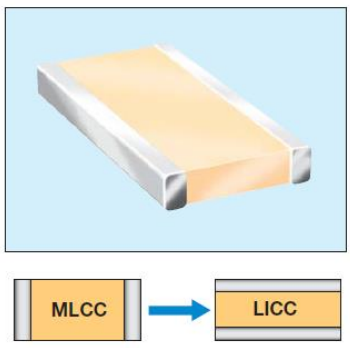


Figure 29. 0306 capacitor from AVX.

- X2Y. This special purpose capacitor is a four terminal device that has two separate capacitors connected to a common pair of ground terminals. This capacitor can provide superior high frequency decoupling compared to conventional ceramic capacitors.

Figure 30. X2Y capacitor image and mounting circuit

The resulting impedance chart response for each rail is shown below. The equivalent impedance of all the capacitors in each rail is shown in red:

- 3.3 Voltage rail:

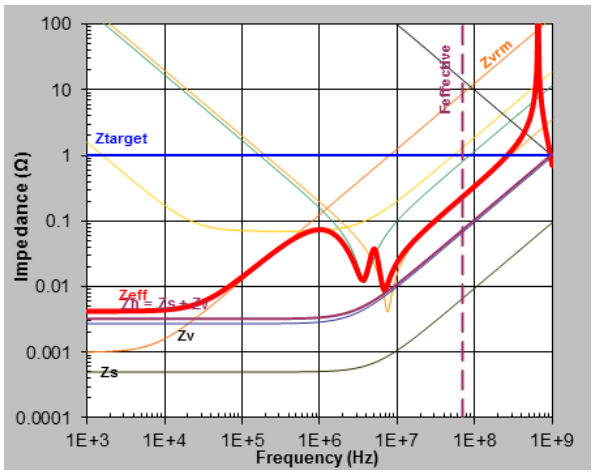


Figure 31. 3.3 Voltage rail.

- 1.2 Voltage rail

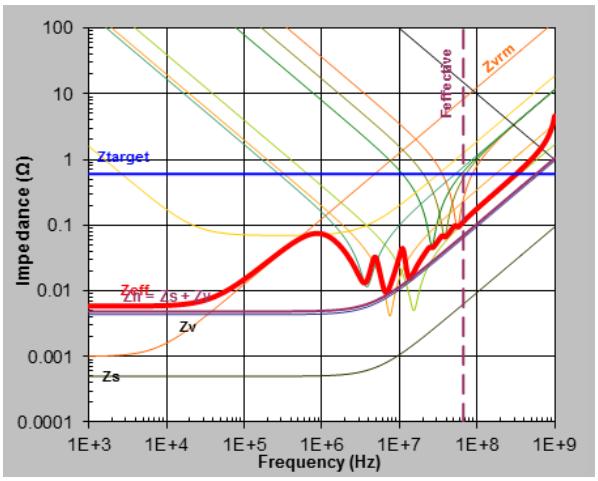


Figure 32. 1.2 Voltage rail.

- 1.2 PLL Voltage rail

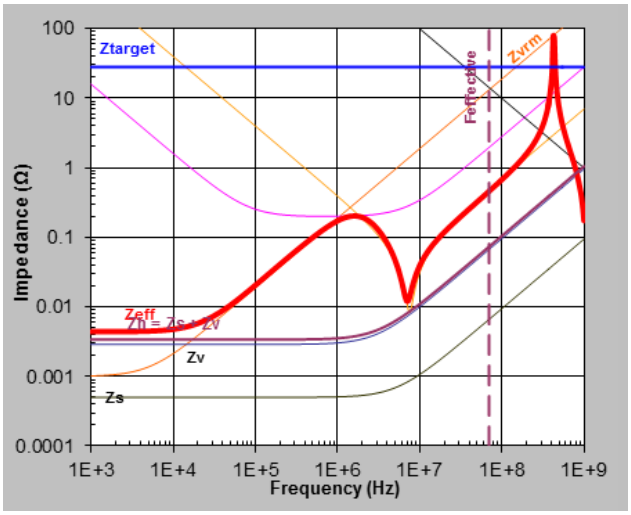


Figure 33. 1.2 PLL Voltage rail

- 2.5 Analog PLL voltage rail

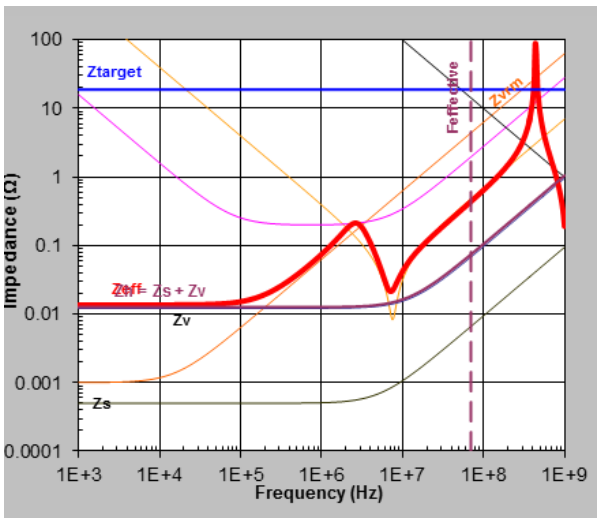


Figure 34. 2.5 Analog PLL voltage rail

The PLL, tough not used in this design, it is required to be properly powered.

3.2.3.5. PIN assignment

All the pin assignments are double check with Altera Pin Planner Tool. This tool allows checking if the FPGA pin is able to perform the task required (input only, input output, differential pair, etc). All the IO Banks are 3.3 V powered.

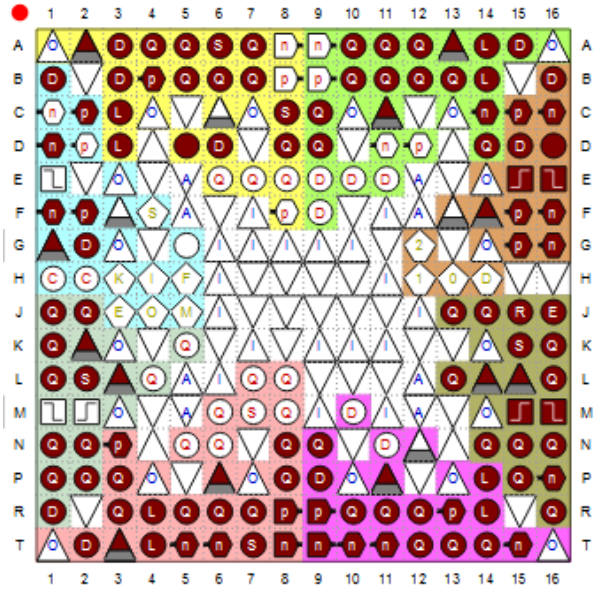


Figure 35. Cyclone IV E. EP4CE22F17C6. Top View.

The assignment is done so the board can be routed only in four layers, being only used for signals the external ones. For these reason, only the two outer rows of user IO are used in the placement, except in the centres (lines 8-9) that more pins can be accessed with only two layers.

The unused pins can be tied to ground or left unconnected [22]: “To improve signal integrity, set the unused pins as outputs that drive ground and tie them directly to the ground plane on the board. (…) To reduce power dissipation, set the clock pins to drive ground and set the other unused I/O pins as inputs that are tri-stated. If you set a reserved state for the unused pins, you must not connect those pins to other devices on the board”

All I/O pins specified as GND can either be connected to ground to improve the device’s immunity to noise or left unconnected.

3.2.4. Mixed signal circuit

The ADC is the only device that has analog circuitry and digital circuitry. As previous experiences proven, it is critical to carefully implement this component

3.2.4.1. Ground design

A split plane is decided to be used in the board. The digital ground plane will take care of most of the board consumption, and analog ground plane will only cover the analog part of the ADC, the signal conditioning circuit and the sensors.

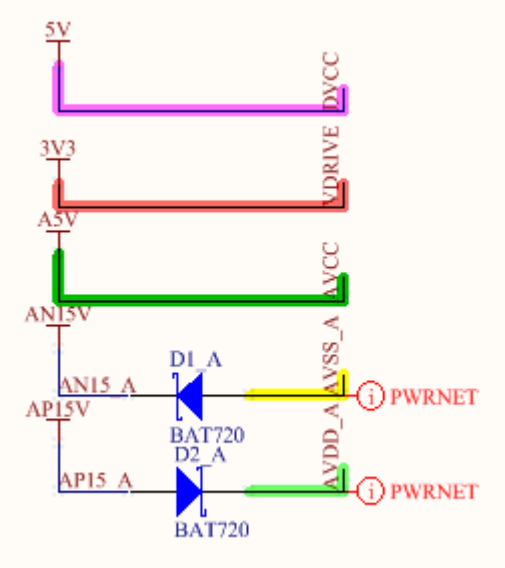
For convenience, the external sensor and power connection are shielded to this analog ground. However, in case of heavy radiated noise, the analog ground can be corrupted. For this case, all the shielding have a disconnection jumper that can be used to shield the signal against the metal case of the prototype or the digital ground.

Also, the ADC ground planes should not have a voltage difference bigger than 0.3 V. It is very unlikely to happen as the circuit is designed, but room for an inductor that joins the analog and digital ground in DC is reserved. This inductor will not be populated unless necessary.

3.2.4.2. ADC

The ADC selected was the AD7656-1BSTZ in contrast to the AD7656 used in the initial prototype, as it requires less decoupling capacitors at the price of slightly less bandwidth (4.5 MHz vs. 12 MHz).

5 Voltage sources are used to power the ADC:



Two independent 5 V voltage sources provide power to the analog and digital circuitry. As this ADC is bipolar, the same voltages as the sensors are used. The Schottky diode on AVDD and AVSS prevents the sensor, in case of being powered before the ADC, to power the ADC.

The ADC can operate in “hardware” or “software” mode, and in serial or parallel mode. In hardware mode the ADC is configured using it pins (like REFIN, RANGE), while in software mode a set of registers is used. This allows more flexibility as the different ranges can be selected for channels 1-2, 3-4, 5-6 but requires multiplexing the data bus, which is required to be input/output. This feature is not particularly attractive for our application, so hardware mode was selected as being simpler.

The electrical system is designed so the ADC can be operated both in serial or parallel mode (only changing a jumper). All these options were studied in the table below, so the design is as much versatile as possible:

Pin	Serial Mode. HW.					Parallel Mode. HW.				
	Used	Static/	Directi	Value	Description	Used	Static/	Directi	Value	Description
CONVST A	1	F	O	X	Start Conversion	1	F	O	X	Start Conversion
CONVST B	1	I	X	X	Can be tied with CONVSTA	1	I	X	X	Can be tied with CONVSTA
CONVST C	1	I	X	X	Can be tied with CONVSTA	1	I	X	X	Can be tied with CONVSTA
_CS	1	F	O	X	Required	1	F	O	X	Required
_RD	0	FF	O	0	Tie to gnd when serial	1	F	O	X	_RD. Enables the output bus
_WR/REF (EN/_DIS)	1	S	X	1	Enable internal reference	1	S	X	1	Enable internal reference
BUSY	1	F	I	X		1	F	I	X	
REFIN/REFOUT	0	S	X	X	Should be decoupled	0	S	X	X	Should be decoupled
SER/_PAR SEL	1	S	X	1	Serial Mode	1	S	X	0	Parallel
DB0. SEL A	1	FF	O	1	Enable input A	1	F	I	X	Parallel bit 0
DB1. SEL B	1	FF	O	1	Enable input B	1	F	I	X	Parallel bit 1
DB2. SEL C	1	FF	O	1	Enable input C	1	F	I	X	Parallel bit 2
DB3	0	FF	O	0	Daisy chain not enabled	1	F	I	X	Parallel bit 3
DB4	0	FF	O	0	Daisy chain not enabled	1	F	I	X	Parallel bit 4
DB5	0	FF	O	0	Daisy chain not enabled	1	F	I	X	Parallel bit 5
DB6. CLK	1	F	O	X	Required for serial mode	1	F	I	X	Parallel bit 6
DB7. HBEN. DCEN	0	FF	O	0	Daysy chain not enabled	1	F	I	X	Parallel bit 7
DB8. DOUT A	1	F	I	X	Serial data FPGA input A	1	F	I	X	Parallel bit 8
DB9. DOUT B	1	F	I	X	Serial data FPGA input B	1	F	I	X	Parallel bit 9
DB10. DOUT C	1	F	I	X	Serial data FPGA input C	1	F	I	X	Parallel bit 10
DB11	0	FF	O	0	Tie to gnd when serial	1	F	I	X	Parallel bit 11
DB12	0	FF	I	0	Contain leading 0	1	FF	I	0	Contain leading 0
DB13	0	FF	I	0	Contain leading 0	1	FF	I	0	Contain leading 0
DB14. REFBUF(_EN/DIS)	1	FF	O	0	Enable internal ref buffer	1	FF	I	0	Contain leading 0
DB15	0	FF	I	0	Contain leading 0	1	FF	I	0	Contain leading 0
RESET	1	F	O	X		1	F	O	X	
RANGE	1	S	X	1	x2 Range	1	S	X	1	x2 Range
_STBY	1	S	X	1	Tied to 1 = Normal operat.	1	S	X	1	Tied to 1 = Normal operat.
_H/S SEL	1	S	X	0	VSTB, CONVTSC, REF, REFBUF	1	S	X	0	Hardware mode
_W/B	1	S	X	0	Word length	1	S	X	0	Word length

Figure 36. ADC pin configuration.

The resulting circuit implemented:

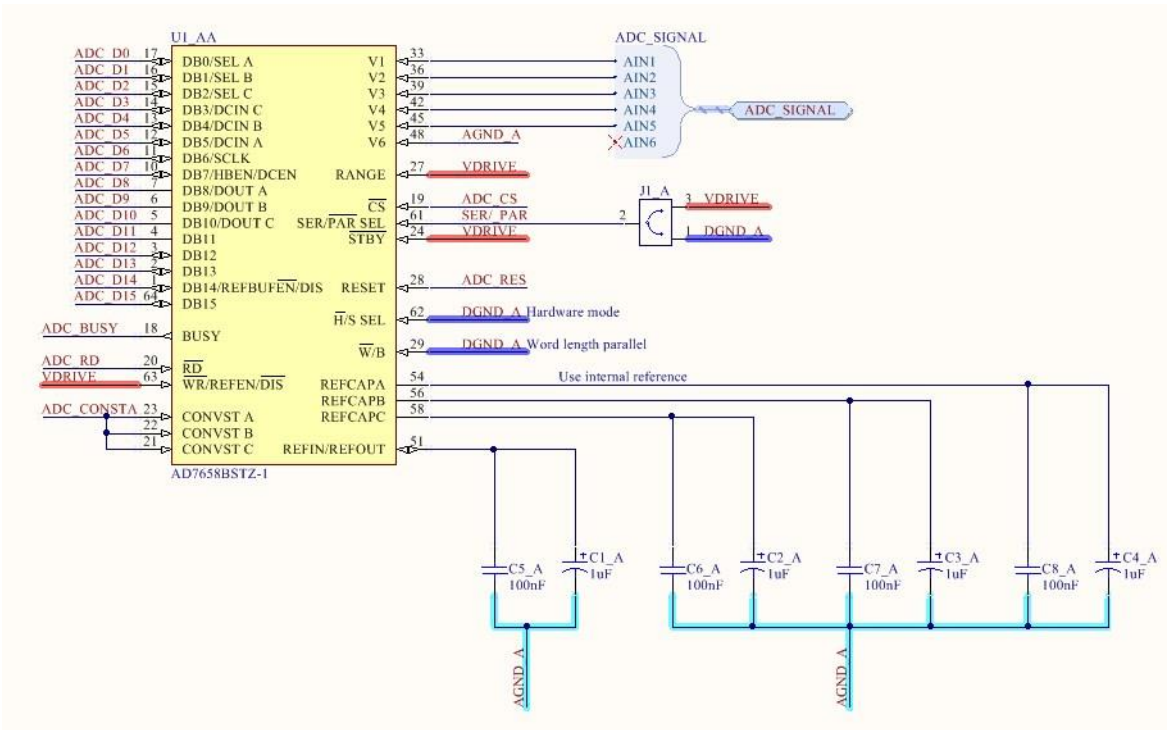


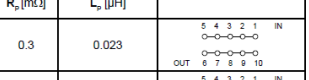
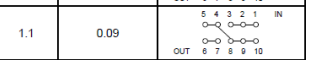
Figure 37. Implemented ADC circuit.

3.2.4.3. Sensors

Two current sensors and three voltage sensors are required by specifications. As high voltage is employed in the power converter, they should be isolated for safety reasons.

There are several isolated topologies available, but the current sensor LA-25NP1 and the voltage sensor LV-25P from LEM manufacturer were already available at GREP and they have much experience working with them, so they were the first option to consider.

The LA-25NP1 is Hall Effect compensated current transducer. The output is a current source of 25 mA when the current flowing though it is 5/6/8/12/25 A (depending on configuration). In the board designed, it can be configured for 12 or 25 A range:

Number of primary turns	Primary current		Nominal output current	Turns ratio	Primary resistance	Primary insertion inductance	Recommended connections
	nominal	maximum					
	I_{PN} [A]	I_P [A]	I_{SN} [mA]	K_N	R_P [mΩ]	L_P [µH]	
1	25	36	25	1 / 1000	0.3	0.023	
2	12	18	24	2 / 1000	1.1	0.09	

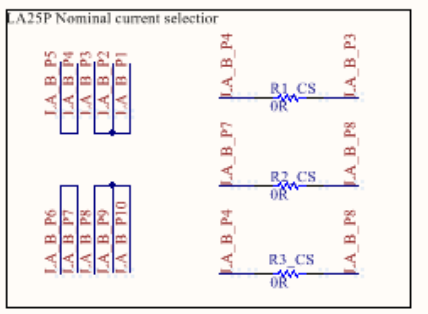


Figure 38. Current sensor configuration options.

Also, an external current sensor can be used instead of these one mounted on the board. This external current sensor should be the LA 55-P, which is similar in operation but does not require cutting the current path (as it have a hole where the wires goes though it). Rated for 50 A nominal current, can be uses as a drop-in replacement as its output nominal current is double the LA-25NP1 for double current)

This option was studied because the MAC Converter output legs contain high-frequency high-power harmonics that can be coupled into the circuit. By moving away these output connections, the capacitive coupling should be removed.

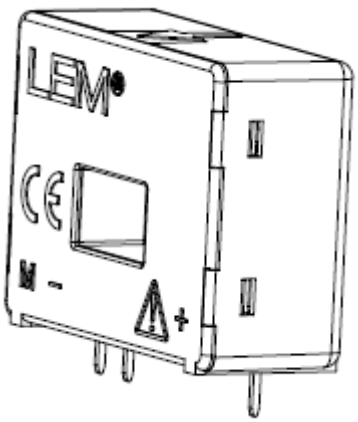


Figure 39. LEM LA 55-P

The design is planned so the current output from the sensor is not translated into voltage until it arrives to the board. This is done to reduce the noise coupling on the cables, as any induced current coupled into the signal should be converted also to voltage by the relatively-low transducer resistor. If done just next to the sensor, and then feed the

voltage to a high input impedance circuit, any coupled current will translate into much higher voltage noise.

The DC-link voltages are sensed on the board, as they are supposed to be a constant DC value. A differential filter is used on the board to filter the high voltage source. This differential filter has a cut-off frequency of 500 Hz, 10 times lower than the switching cycle.

Note in the image below how external connections CNX_VS allows to change the voltage sensing circuit. By removing R4_VS and R7_VS, the user has access to the individual voltage sensor inputs.

The input resistor R2 (20 kΩ) is calculated so the current flowing though the sensor is 10mA when 200 V is applied to the input voltage. This resistor will dissipate 2W in this case.

The schematic is showing in Figure 40.

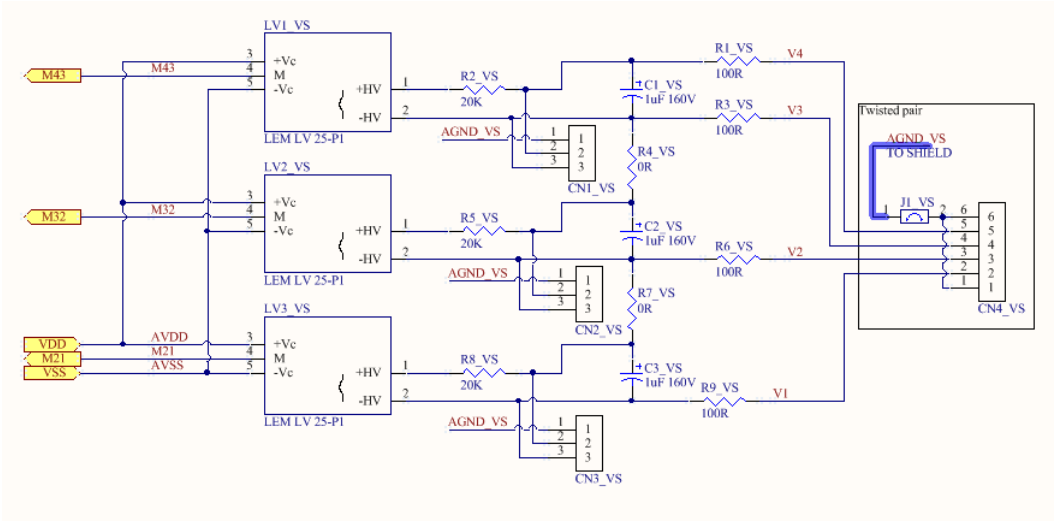


Figure 40. Voltage sensors circuit.

The output from both current and voltage sensors are processed in a similar way, only differing from the sensing resistor that must be different for each case.

This resistor value is 200 Ω for the voltage sensor and 180 Ω for the current sensors. Note that the maximum value for LA-55P is 160 Ω, but this difference will only make its range smaller and is not expected to influence in the sensor linearity.

This resistor is in parallel with a capacitor that acts as a low-pass current filter with cut-off frequency of 500 Hz. After the current-to-voltage conversion, another low-pass voltage filter is placed just before the operational input. Note that in total, this is a 3rd order 500 Hz low pass filter, placed so high order because the deep noise problems arisen in the initial tests. If, after proper testing, it is proven that there is less filtering constraints they can be easily removed.

The resulting circuit is shown in Figure 41.

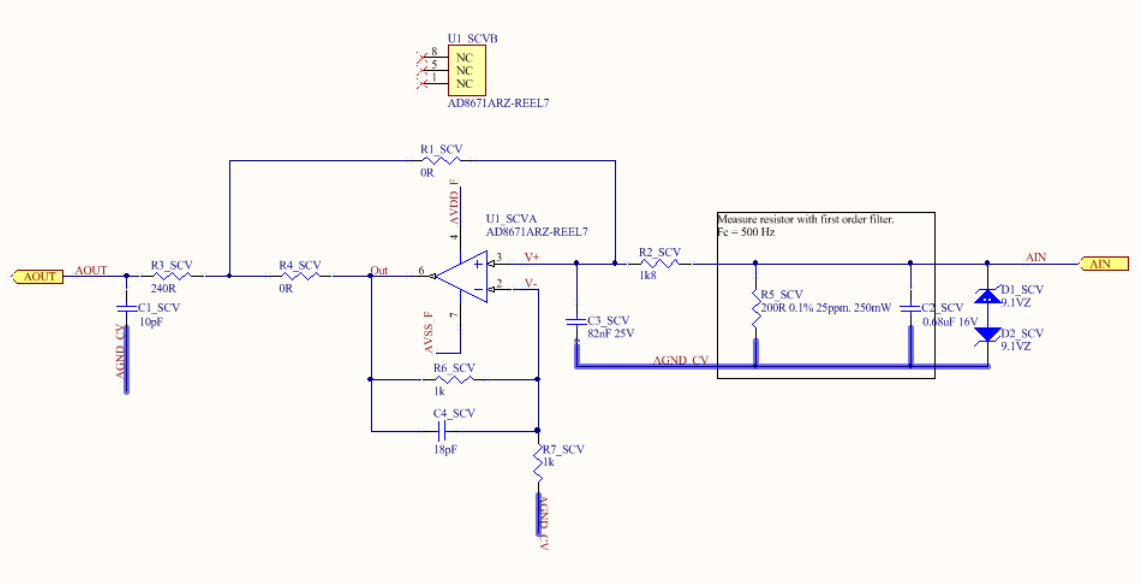


Figure 41. Signal conditioning circuit.

As the measured current/voltage is sampled in a SAR ADC, which has a series of capacitors that must be charged very fast (the opening time is 3.5 us), so it requires an operational amplifier. As amplification is not desired, it is only working as voltage follower. The operational amplifier is selected then with these requirements in mid. The input signal does not contain any high-frequency of interest, so the only requirements for the operational amplifier are unity-gain stability, low input current and noise and great output capabilities. The AD8671 is selected as being suited for the application and offer a great relationship between price-features.

This device input stage is populated with back-to-back diodes, thus the use of a feedback resistor (1 kΩ in this case) is recommended to avoid having the amplifier load the sensor. However, this resistor together with the input capacitance pin introduces a pole in the feedback loop that can lead to instabilities. A parallel capacitance to the feedback resistor is placed to compensate this effect.

The operational inverting pin can be populated with a resistor to ground that converts the device to a non-inverting amplifier.

The AD8671 is unity-gain stable and can drive large capacitance loads. However, according to datasheet, “very large loads can cause unwanted ringing or instability”. For this reason, the output is decoupled by the 240 Ω resistor.

The power rails for the AD8671 is filtered by a small 10 Ω RC filter in order to prevent signal transfer between different stages that can lead to intermodulation distortion, crosstalk and instability (not shown in Figure 41).

The amplifier can be bypassed populating R1 and removing R4.

3.2.5. Power supply

The board power requirements are summarized in the image below:

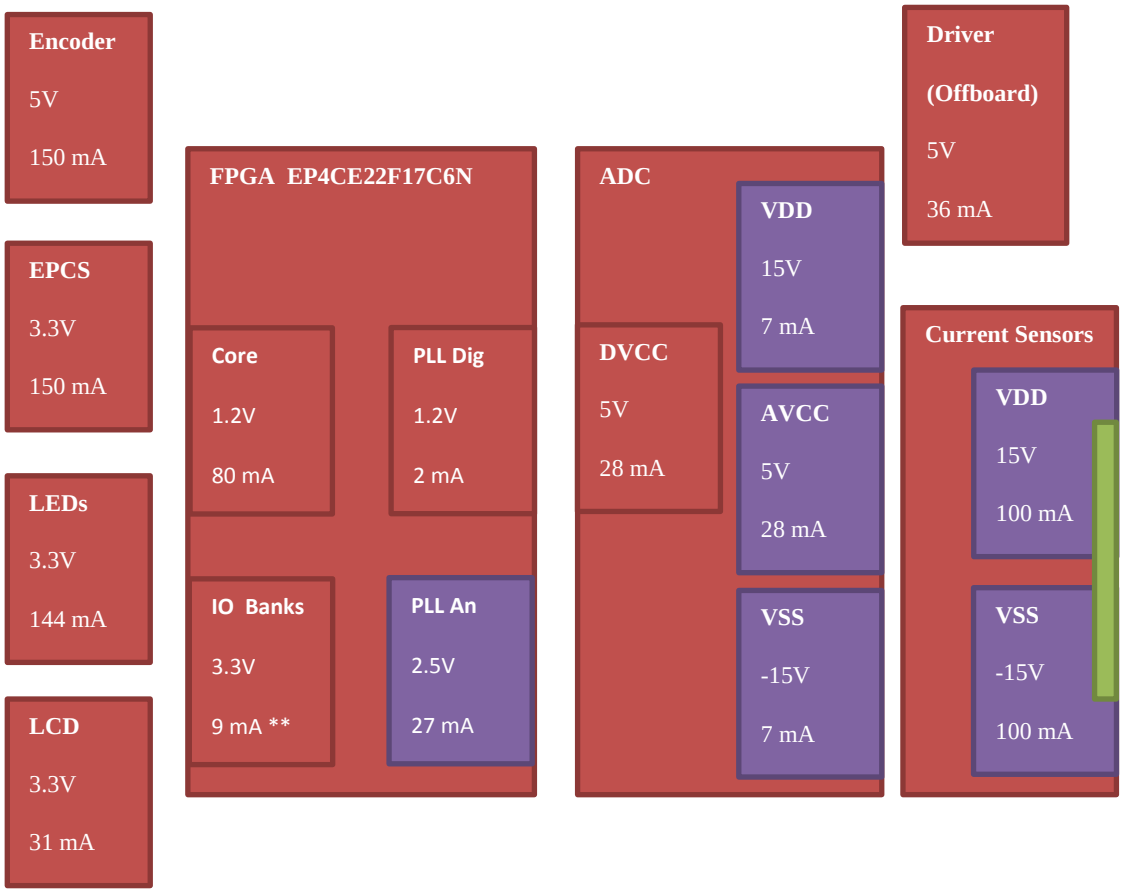


Figure 42. System power requirements.

The general power architecture is designed with the aid of “WEBENCH® Power Architect” from Texas instruments. This way we obtain an easy evaluation of the system performance and efficiency of different configuration schemes, mainly different voltage rail structures.

The desired power rails are configured as DC power that fed to the board via a commercial AC-DC converter, providing 7.5 V DC, then a switinchg power converter that creates a 3.3 voltage rail. From this voltage rail, a switching power converter is used to obtain the 1.2 V used for the FPGA core and a linear regulator that supply the 2.5 V supply for the FPGA PLL:

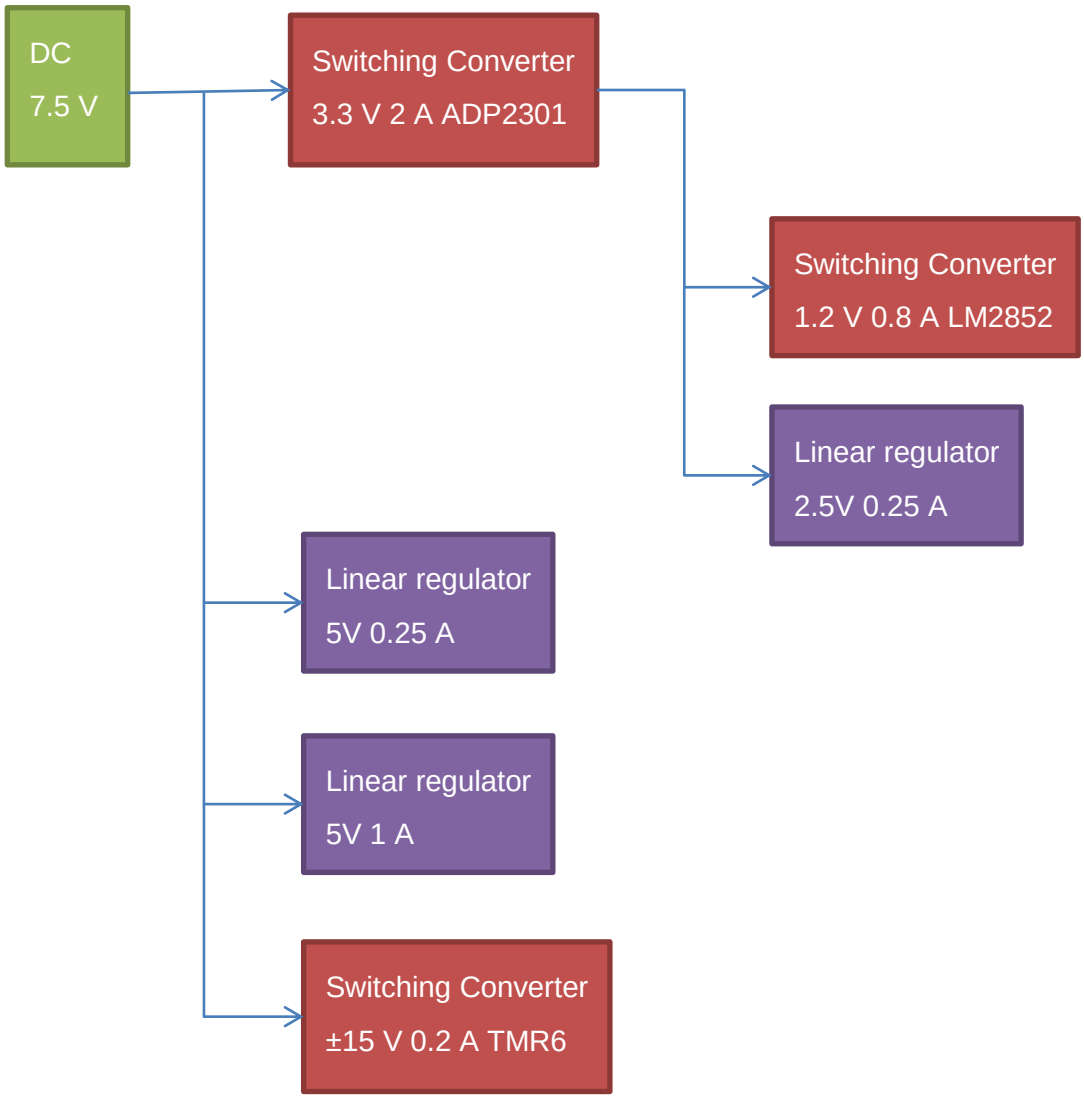


Figure 43. Voltage rails.

The design also allows connecting an external power source and disconnecting the on-board power supplies, except in the case of 1.2V supply and 2.5V supply.

3.2.5.1. ADP2301

This device is designed with the spread sheet provided by analog devices that mainly eases the calculations exposed in the datasheet. The device works as a buck step down converter from 7.5 V to 3.3 V, 1 A maximum output with 1% voltage ripple.

Two variants of the same circuit exists, a 1.4 MHz switching one (ADP2301) and a 700 kHz one (ADP2300). Using the conversion limitation curve in Figure 44, we can see that both options are feasible. However, faster transient response is preferred for the circuit over higher efficiency of the 700 kHz switching version.

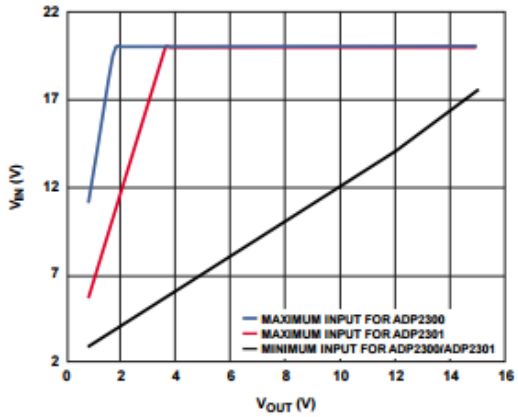


Figure 44. Voltage Conversion Limitations

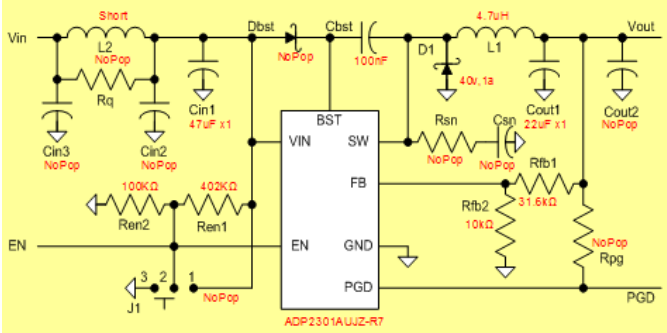
Figure 44. ADP230X Conversion limits.

The device is configured to output 3.3 V. The output is not enabled until the power source is above 2/3 of 7.5 V, by the EN pin: “Generally, the EN pin can be easily tied to the VIN pin so that the device automatically starts up when the input power is applied. However, the precision enable feature allows the ADP2300/ ADP2301 to be used as a programmable UVLO by connecting a resistive voltage divider to VIN, as shown in Figure 46. This configuration prevents the start-up problems that can occur when VIN ramps up slowly in soft start with a relatively high load current.” (From datasheet). The next image shows the output from the spread sheet for this configuration:

ANALOG DEVICES

ADP230x Buck Designer

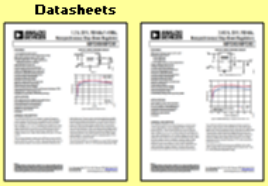
Revision v.1.39 DB20150402



Enter Inputs | Order Eval Board

Bill of Materials
Efficiency
Bode Plot
Transient Response
230x Demo Schematic
230x Demo Board Pictures
230x Demo Board Layout

Datasheets



No Errors To Display

Bill of Materials | Enter Inputs | Advanced Settings | Go to Top

Item#	Desc	Mfg	Part Number	Component Specs	Pkg	Part Qty	Area(mm²)	Hgt(mm)	Cost($)
Totals:						10	51.6	1.60	$1.54
1	U1	ADI	ADP2301AUJZ-R7	Switcher IC - ADJ	TSOT6	1	8.1	1.00	0.810
2	L1	Coilcraft	PFL4514-472MEB	4.7uH, 220mΩ	Shielded	1	16.7	1.40	0.320
3	D1	DiodesInc	1N5819HW	1A, 40V	SOD123	1	6.6	1.45	0.081
4	Cout1	Murata	GRM21BR60J226M	22uF, 6.3v	805	1	2.50	1.25	0.069
5	Cout2			NoPop		0	0.00	0.00	0.000
6	Cin1	Taiyo Yuden	LMK316 BJ476ML-T	47uF, 10v	1206	1	5.1	1.60	0.195
7	Cin2			NoPop		0	0.0	0.00	0.000
8	Rfb1	Vishay	1% Tolerance E96	31.6KΩ, 1%	805	1	2.50	0.50	0.010
9	Rfb2	Vishay	1% Tolerance E96	10KΩ, 1%	805	1	2.50	0.50	0.010
10	Cbst	Vishay	5% Tolerance	100nF >6.3v X7R	805	1	2.50	1.25	0.020
11	Ren1	Vishay	1% Tolerance E96	402KΩ	805	1	2.50	0.50	0.010
12	Ren2	Vishay	1% Tolerance E96	100KΩ	805	1	2.50	0.50	0.010
13	Csn		No Snubber Selected	NoPop		0	0.00	0.00	0.000
14	Rsn		No Snubber Selected	NoPop		0	0.00	0.00	0.000

Figure 45.ADP230X Configuration result.

The feedback resistors, capacitance and inductor are chosen to match the manufacturer recommendations. The recommended circuit is then placed in the design:

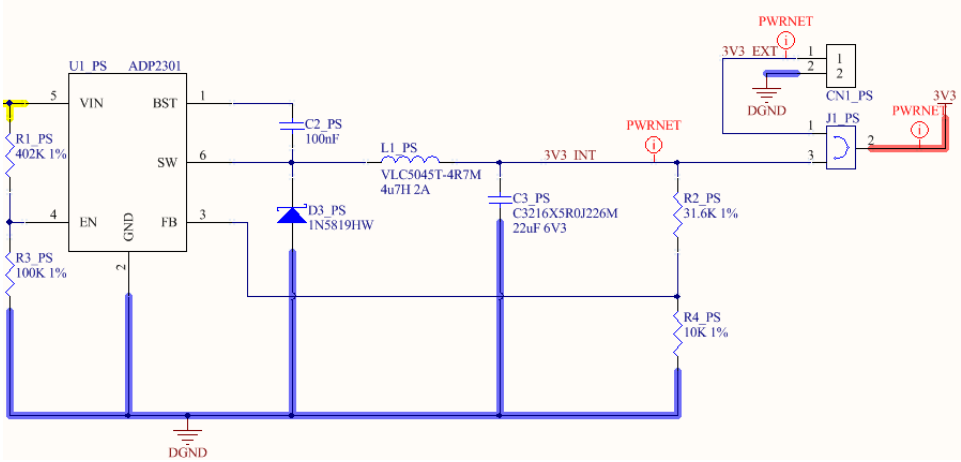


Figure 46. ADP2301 shematic circuit.

3.2.5.2. LM2852

One of the critical features stated by [18] is that the power supply must be monotonical (see image below). This subject is studied in [23], recommending the use of switching power supplies to provide power to the FPGA.

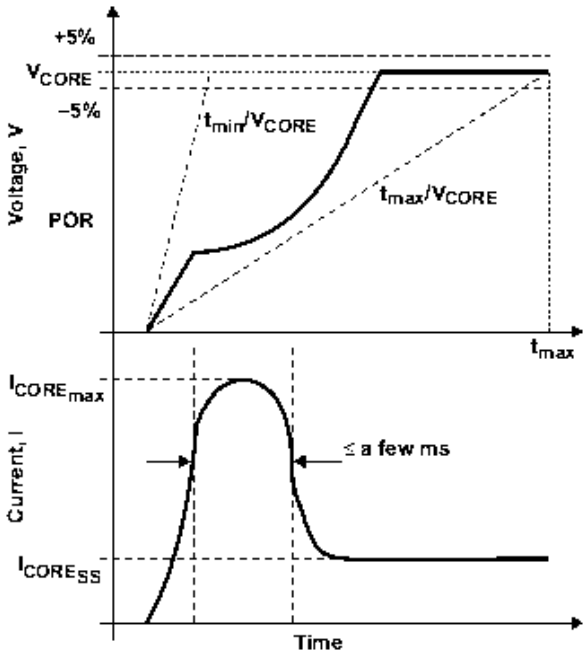


Figure 47. Monotonical power supply, current peak. [23]

In terms of performance, it would be superior to connect the converter directly to the 7.5 V DC bus, but there was no device capable of this operation (with the mentioned features).

The LM2852 is specifically designed for Point-Of-Load microprocessor and FPGA power supply. The circuit design is helped by the “WEBENCH® Power Architect” tool. The main configuration panel is shown in the image:

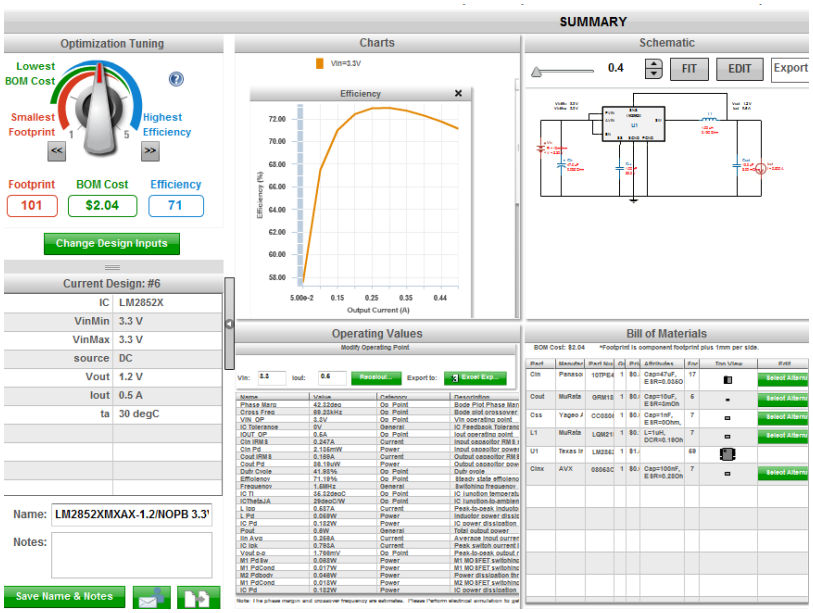


Figure 48. WEBENCH® Power Architect

This tool allows to perform simulations that can be used to obtain the frequency response to study the stability of the converter, the efficiency for the selected configuration, etc. :

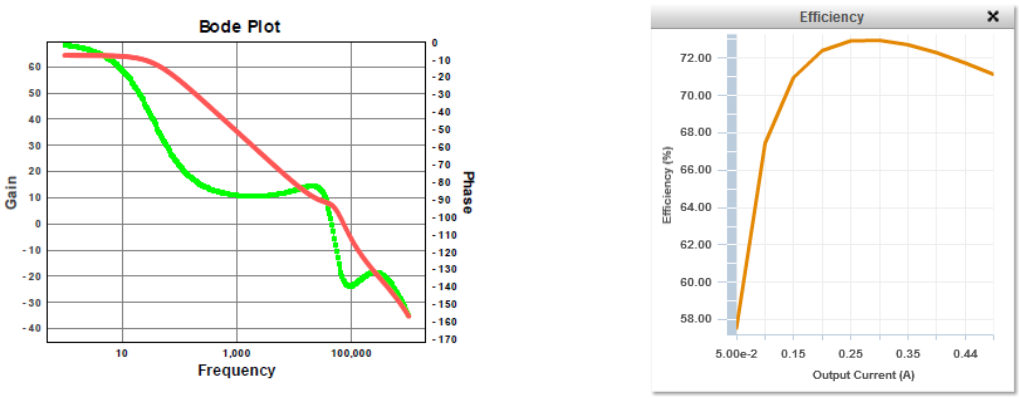


Figure 49. WEBENCH simulation result for LM2852.

As in the previous case, the selected components match the recommended values from the manufacturer. The designed circuit is represented in the image:

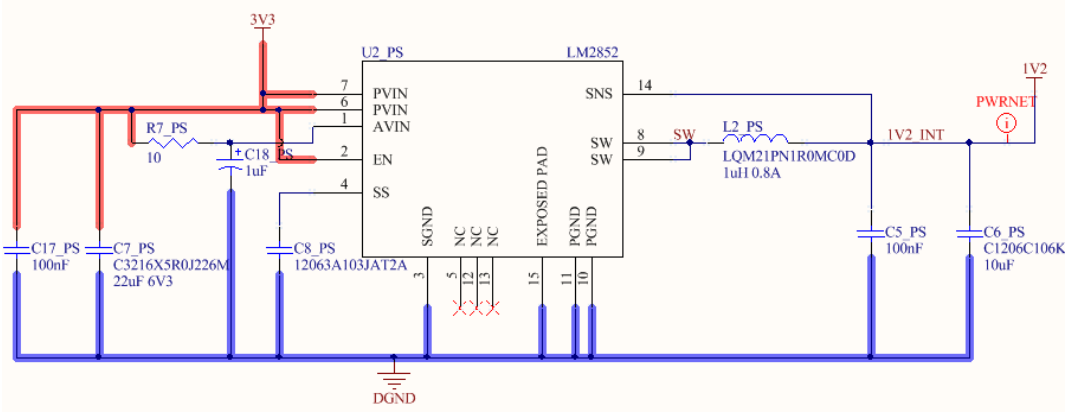


Figure 50. LM2852 schematic circuit.

3.2.5.3. TMR6

For sake of simplicity, a power converter block from TRACOPOWER™ is used to provide the ±15 V rails. The circuit is based on the application note for this device:

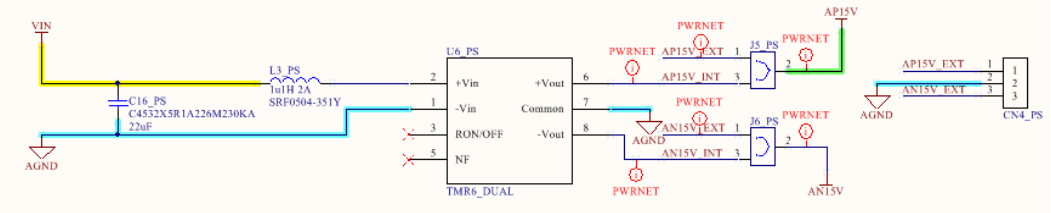


Figure 51. TMR6 shematic circuit.

In this case the yellow line represents the input voltage from the DC-AC adaptor.

3.2.5.4. ADP3303

This linear regulator generates the 5 V analog voltage rail. A 100 nF noise reduction capacitor, C4, is used to reduce the noise by 6 dB to 10 dB according to device datasheet. The power circuit is shown below:

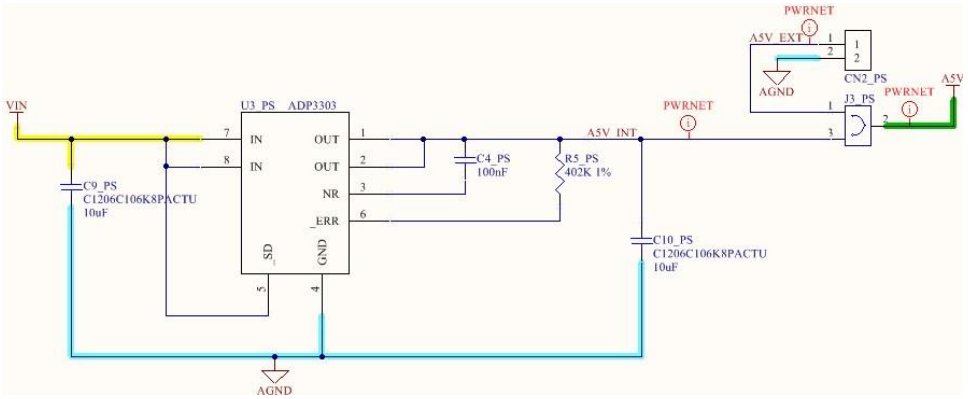


Figure 52. AP3303 shematic circuit.

3.2.5.5. LP2992

Low noise regulator that provides the 2.5 Voltage rail required for the FPGA PLL. Although it is an analog circuit, there is no analog split plane provided for the FPGA.

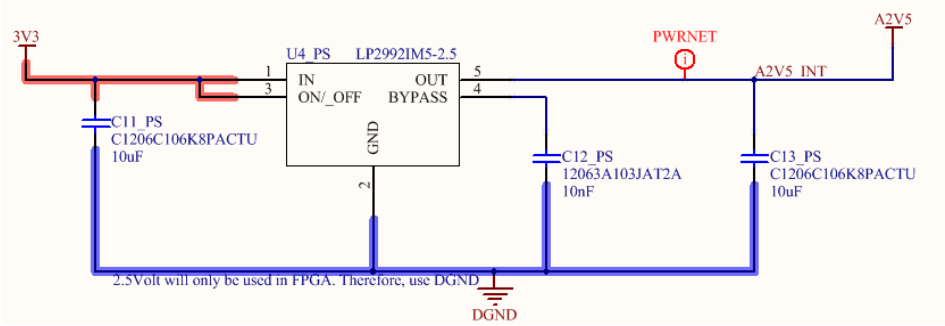


Figure 53. LP2992 schematic circuit

3.2.6. User Interface

The user interface received a major revamp with respect to the original prototype.

A 16-characters 3-lines LCD panel replaces the four digit seven-segment displays, a matrix keyboard is included as well as the same 12 slider switches. The LEDs proven to be a rapid way to identify errors produced in the device so their number is increased up to 12 in this prototype.

The LCD panel model is EADOGM163-A from ELECTRONIC ASSEMBLY. Can be powered by a single 3.3V power supply, The LCD logic is driven by a ST 7036 controller that can be interfaced with a 4-bit or 8-bit parallel interface or by SPI.

It is available in different liquid crystal technologies, being “STN pos. yellow/green reflective” the most suitable for the application, as the finest readable technology without needing backlight.

Nevertheless, the design is compatible with other liquid crystal technologies that shares the same footprint and led backlight limited resistor, albeit not populated, is included.

3.2.7. Encoder

The encoder interface is similar to the initial prototype. The encoder signals are feed from a shielded cable that connects with the board with a DB15 connector.

The encoder facilitates the three signals of interest (A, B, INDEX0) and its bit-complementary (A_INV, B_INV, INDEX0_INV). The latter are not used by the control logic so, in order to reduce the number of user IO pins required for the FPGA, they were removed.

The encoder is powered by the on-board digital 5V regulator. The cable shield is tied to digital ground, and can be disabled by resistor R1_E removal, as can be derived from the circuit:

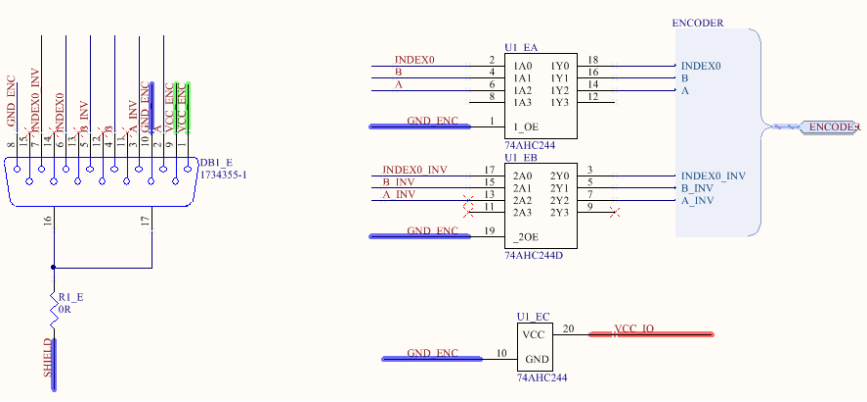


Figure 54. Encoder circuit schematic

Not in the original encoder circuit, an octal non inverting buffer/line driver (74AHC244) is connected to the encoder outputs, working as non-inverting buffer. Its main function is to convert the 5 V digital signals from the encoder into 3.3 V.

According to [18], "If VCCIO is between 3.0-V and 3.6-V and the PCI clamping diode (not available on EP1C3 devices) is enabled, the voltage at point B in Figure 11–3 is 4.3-V or less. To limit large current draw from the 5.0-V device, R2 should be small enough for a fast signal rise time and large enough so that it does not violate the high-level output current (IOH) specifications of the devices driving the trace. The PCI clamping diode in the Cyclone device can support 25mA of current (…) Because 5.0-V device tolerance in Cyclone devices requires use of the PCI clamp (not available on EP1C3 devices), and this clamp is activated during configuration, 5.0-V signals may not be driven into the device until it is configured".

The 74AHC244 is supplied with 3.3V but can accept voltages higher than its supply voltages before the FPGA is configured.

Furthermore, this device inputs have a Schmitt-trigger action that helps recovering the signal and prevents from some noise and bounces.

3.2.8. GPIO

An additional general purpose eight-signal header has been included in the design.
The main propose on the board are:

- Include a general purpose IO that covers future needs.
- Be able to output debugging signals, in conjunction with SignalTap.
- Have a backup mechanism that may mitigate any error in the board. As the first iteration of new board design, 100% error-free board is unlikely.

3.3. Layout Design

3.3.1. General characteristics

A brief review of the design parameters is performed in this chapter. Only FR4 dielectric material is considered, as the cost of different material is not justified for this application.

3.3.1.1. Stack type

The manufacturer selected provides only “Foil Lamination” stack types. This stack is made by a core dielectric in the center of the board, and several prepregs at the outer layers separation. A prepreg is made of the same material of the core, but has not been yet cured, which is done in the fabrication stage.

The minimum layer count is defined by the complexity of the board. In this case, the limitation factor is the FPGA routing. As explained, by carefully chose each pin function the

3.3.1.2. Trace width and clearance

Trace width and clearance should initially be at least 0.05mm larger than the smallest width and clearance for that technology. The best practice to obtain the optimum values is to attempt to route the densest pattern, in this case the PFGA BGA package. This way, the components are the ultimate responsible of the board technology.

3.3.1.3. Core thickness

The core thickness influences in the physical stability of the board and the minimum inductance of the vias. For bigger boards, it is required to increase the core thickness to improve the torsion resistance of the board.

The thicker the core, bigger the vias; leading to an increase in the inductance of the vias which can result critical for power decoupling applications.

Using the PDN Power tool from Altera, we can estimate the effect of core thickness:

- For 0.8mm. 0.5 FR4 Core. Prepeg 2116 (0.105mm) . 35/35
  Results, impedance chart and values.

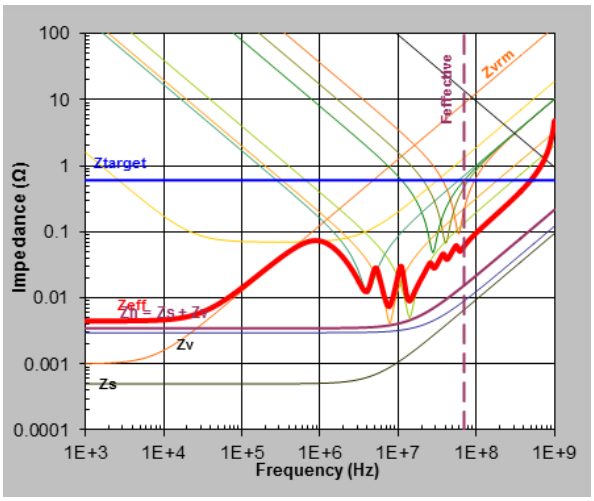


Figure 55. 1.2 V rail impedance with 2116 prepeg 0.8 mm

Device		
BGA Via	70.4pH	0.7 mΩ
Plane Capactince	373.6 pF	1.3 mΩ
Feffective	70 MHz	

Table 2. Effect of core thickeness. Results for 2116 prepeg.

- For 1.6mm. 1.2mm FR4 Core. Prepeg 7628 (0.175mm) 35 / 35

Results, impedance chart and values.

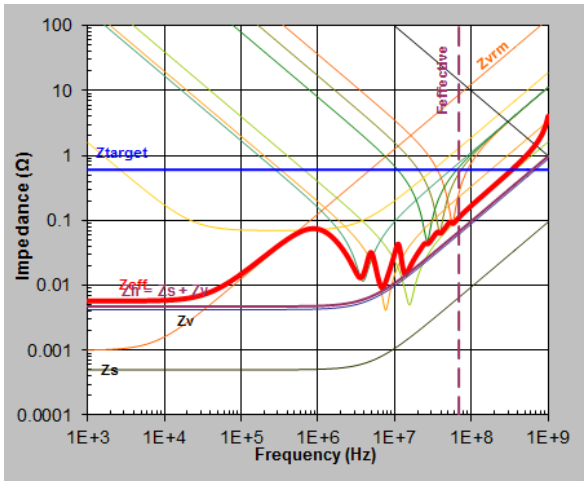


Figure 56. 1.2 V rail impedance with 7628 prepeg 0.8 mm

Device		
BGA Via Inductance	140.2pH	1.3 mΩ
Plane Capactince	159.6 pF	1.3 mΩ
Feffective	69.1 MHz	

Table 3. Effect of core thickeness. Results for 7628 prepeg.

3.3.1.4. Prepeg thickness

The main influence is the capacitance between layers (crosstalk) and its influence in characteristic line impedance. This can be calculated for a ustrip-line as in the following image:

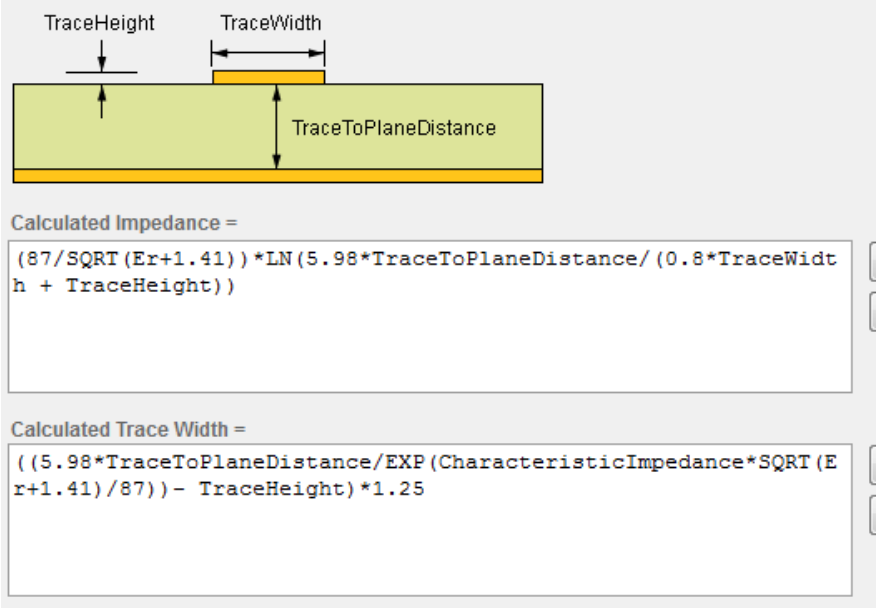


Figure 57. uStrip line characteristic Impedance

This board only contains a few signals that are high-speed, but the characteristic impedance it is not a critical parameters as in memory interfaces or transceivers.

Only the standard prepeg thickness is considered in this Thesis, as the use of non-standard stack-ups increases the board cost and manufacturing time.

3.3.1.5. Copper thickness.

The copper thinness influences three areas: current capability, plane capacitance, characteristic impedance, fabrication constraints.

The study will determine the feasible values of copper thickness and characteristic impedance, then determine the minimum copper thickness for the desired current, study its effects in plane capacitance and last, check the fabrication constrains.

There is a limitation in maximum characteristic impedance that can be achieved in the board, that for a given copper thickness and prepeg is determined by the minimum width. In the case of interest, the minimum with is 0.2 mm while the minimum required characteristic impedance is 50 Ω.

A set of copper thickness is introduced in computational models and determined that only thickness below 70 um were able to create the desired characteristic impedance. In the case of 35 um, this impedance is archived with 0.29 mm. width.

Thus, it imperative to determine 35 um can handle the maximum board currents.

The current capability is given by the PCB manufacturer, as the image below:

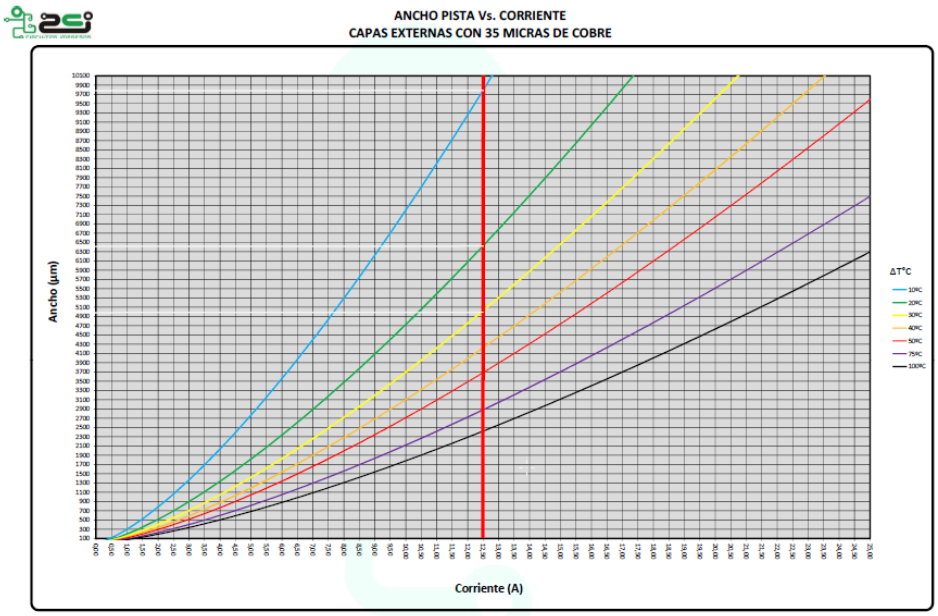


Figure 58. Line width - Current for several temperature increases. For 35 um

In our mixed signal board, the maximum current is defined by the on-board current sensors that will be able to measure up to 25 Amperes. The graph from the manufacturer is for a single layer copper board, and we intended to use both top an bottom. There is no study on this field that establishes simple relationship for the number of layers and maximum current capability (only studies based on finite-states calculations [24]). However, as the copper has positive temperature coefficient (can be used in parallel), the current of two similar conductors will be about a half of the total current, but its dissipation coefficient will not be the same as if two separate conductors are used. These give us a best-case and worst-case scenario. In the graph, 12.5 A is marked in red. The best case scenario tells us that the temperature rise in the board will be 10 ºC for 9.77mm width, 6.4 ºC for 6.4mm witdh and 30 ºC for 5 mm witdh.

According to these results, the use of 35 um thickness is feasible form a current capability point of view.

Using the PDN Power tool from Altera, in an example of a power plane composed of a 3 layer plane capacitor GND-VCC-GND, size equivalent to the PFGA FBGA 256 package size, the effect of the copper thickness is studied, showing no significant differences.

The copper thickness also influences the minimum trace with and separation. To be able to route the internal FPGA layers, 0.2 mm trace width and separation is required. This forced us to use thickness lower or equal to 35 um, that was the final chosen thickness.

3.3.1.6. Manufacturer constraints.

The manufacturer constrains are presented, highlighted for 35 um thickness.

Min width and separation:

Outter layers:

Copper Thickness	Min width (Tw)	Min separation (Ts)
18u	0.125mm	0.150mm
35u	0.200mm	0.200mm
70u	0.250mm	0.250mm

Table 4. Min width and separation.Outter layers

Inner layers:

Copper Thickness	Min width (Tw)	Min separation (Ts)
18u	0.125mm	0.150mm
35u	0.150mm	0.180mm
70u	0.250mm	0.250mm

Table 5. Min width and separation.Inner layers

Drill size:

Dill type	Min diameter	Tolerance
Plated	0.250mm	+0.1mm/-0.05mm
Non plated	0.350mm	+0.1mm/-0.05mm
Bluried via	0.500mm	

Table 6. Drill size

Aspect ratio:

The material thickness determines the minimum drill size. The fab establishes a max aspect ratio of 6. This way, for a 1.6mm standard material thickness the minimum drill size is 0.26mm.

Min Crown size:

Metal	Min crown
External. +18um	0.150mm
Extenal. +35um	0.200mm
Internal.	0.2

Table 7. Min crown size

The minimum crown was not enough to be able to fan-out the FPGA pins, so it was asked to the fabric if 0.165mm is feasible, obtaining a positive response.

Solder mask:

Mask color	Min clearance	Min trace thickness
Green	0.075mm	0.1mm
Other	0.075mm	0.15mm

Table 8. Solder mask constrains.

Screen:

Mask color	Min clearance	Min trace thickness
White	0.1mm	0.125mm
Black	0.1mm	0.180mm

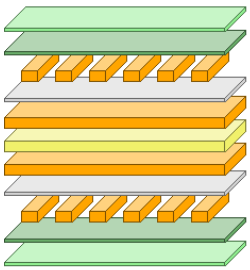
Table 9. Screen constrains

Drill size:

0.25 mm to 1.4 mm

3.3.1.7. Final stack-up

The stack up was designed to be a standard one which the manufacturer offers that accomplishes the requirements:



Layer Name	Type	Material	Thickness (mm)	Dielectric Material	Dielectric Constant	Pullback (mm)	Orientation
Top Overlay	Overlay						
Top Solder	Solder Mask/Co...	Surface Material	0.01016	Solder Resist	3.5		
Top	Signal	Copper	0.035				Top
Dielectric1	Dielectric	Prepreg	0.175	FR-4	4.2		
Plane 1	Internal Plane	Copper	0.035			0.5	
Dielectric2	Dielectric	Core	1.2	FR-4	4.2		
Plane 2	Internal Plane	Copper	0.035			0.5	
Dielectric3	Dielectric	Prepreg	0.175	FR-4	4.2		
Bottom	Signal	Copper	0.035				Bottom
Bottom Solder	Solder Mask/Co...	Surface Material	0.01016	Solder Resist	3.5		
Bottom Overlay	Overlay						

Figure 59. Final stack-up

3.3.2. General view

A completed image is attached:

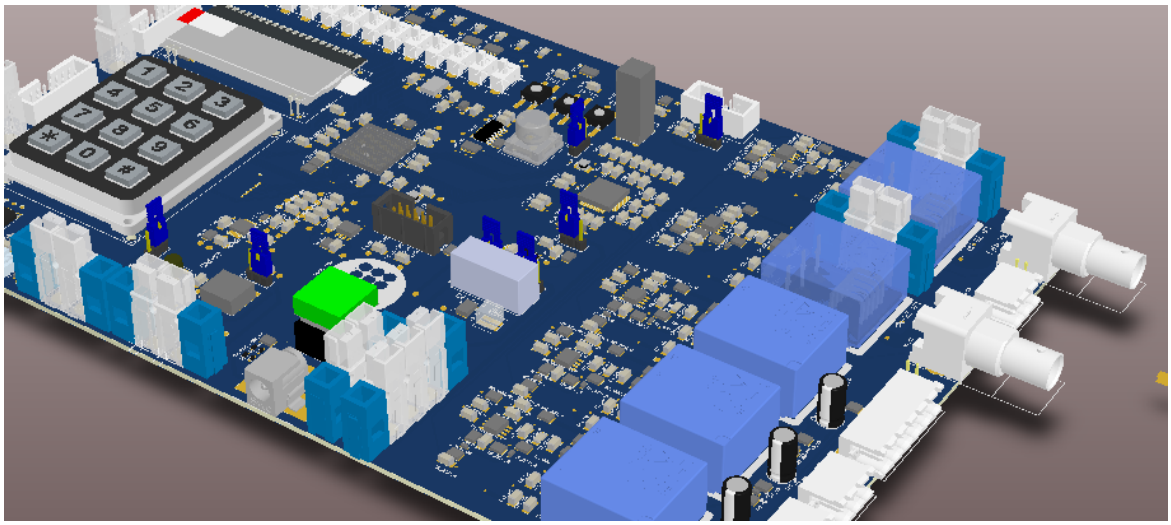


Figure 60. 3D representation of the board

3.3.3. FPGA routing

The BGA-256 packaged was fan-out by only 2 signal layers an 2 power layers. As can be seen in the image, only a very few pins were available on the outer rows:

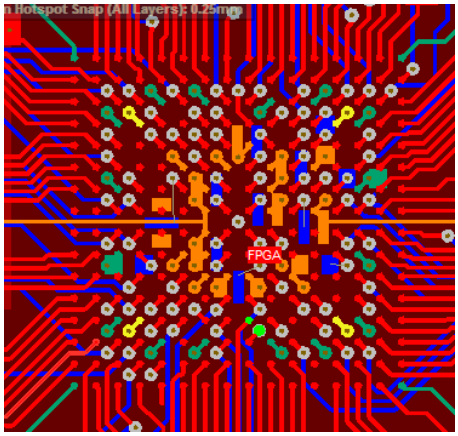


Figure 61. FPGA fanout

The design was optimized so each pin is extracted directly as a bus-like type and no cross occurs between them. Depending on the bus, is routed on the top side or in the bottom side. An example can be seen in the image, controller output bus is routed in the top layer (red) and the LCD data lines in the bottom layers (blue):

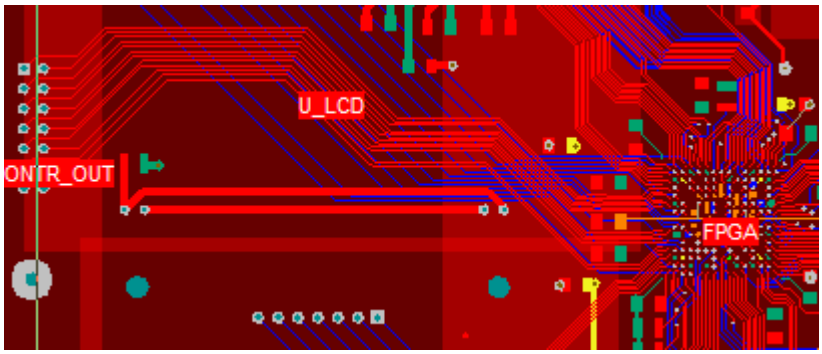


Figure 62. Example of bus topology

The decoupling capacitors are placed around the FPGA and below it (near the supply pins are placed the high-frequency-special-purpose capacitors:

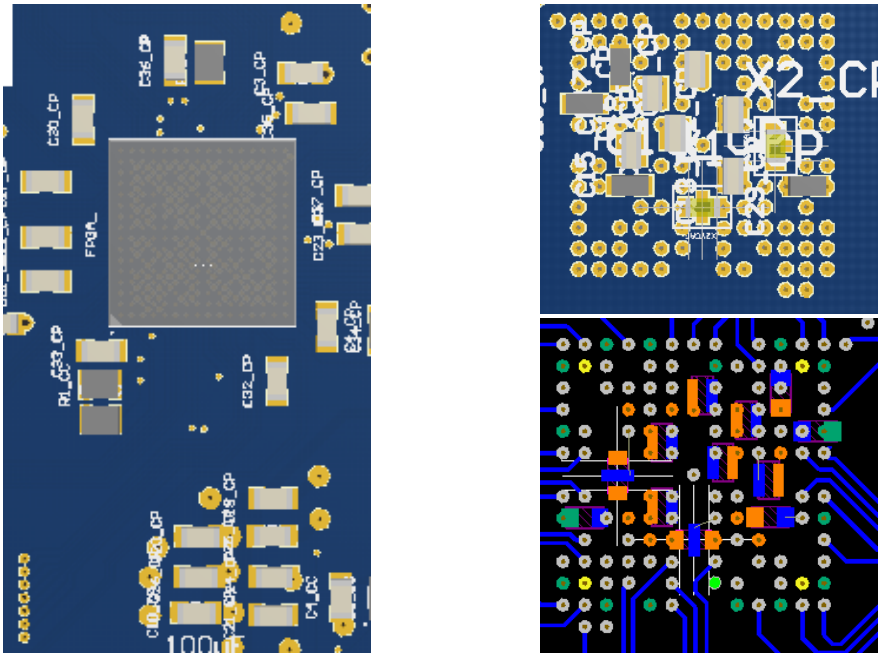


Figure 63. Decoupling capacitors.

3.3.4. Analog signals

The signal coming from the BNC connector is fed to the input circuitry by means of a 50 Ω transmission line (uStrip) to minimize reflections. This can be seen in the image bellow as the line is thinner than the 0.4mm used in other connections, but still wider than the 0.2 mm minimum specifications by the manufacturer.

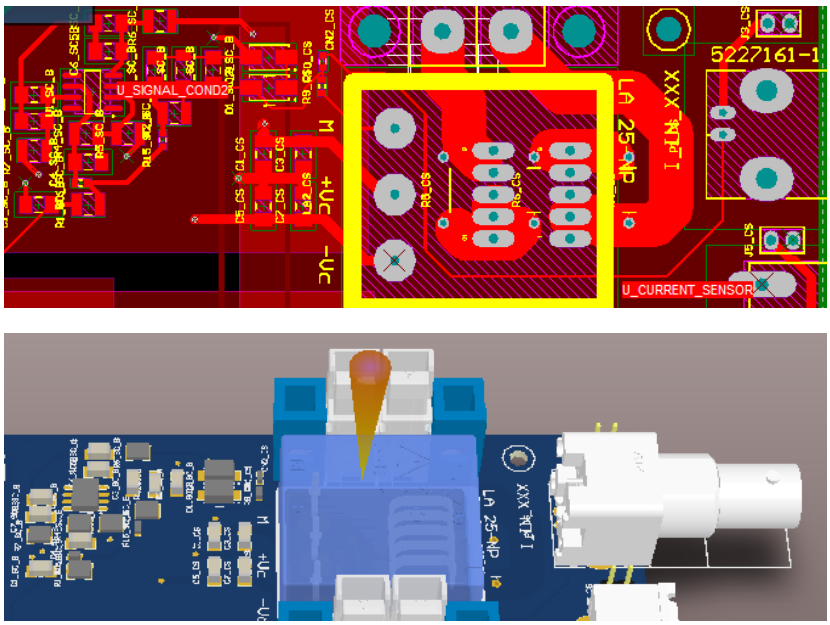


Figure 64. Current measurement circuit

3.3.5. Power planes

The system includes a layer only for power supply purposes:

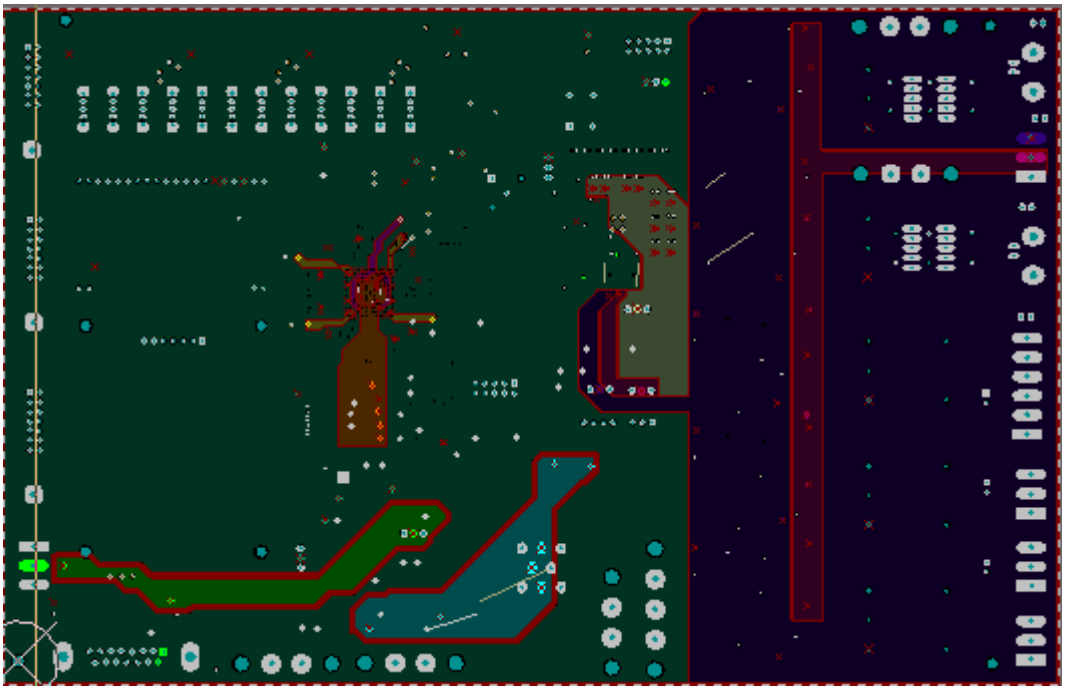


Figure 65. Power plane

In the image, the analog circuits (right) is mainly covered by -15 V power supply (dark blue) and a small portion of +15V. The zone in gray near the ADC is the analog 5 V voltage rail.

The dark gray, mostly all the board as is used as the main bus, is +3.3 V. In the lower side, the light-blue is the input voltage that feeds the power converters, and the digital +5V is represented a is left in green.

The FPGA zone requires a zoom-in:

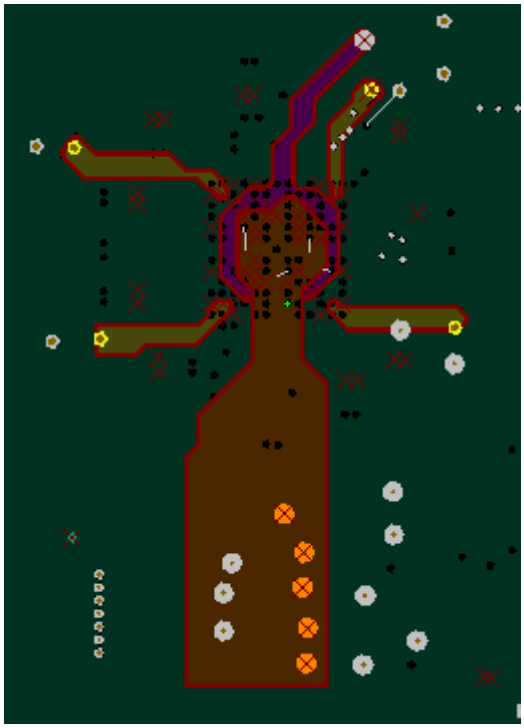


Figure 66. Power plane FPGA

The FPGA main voltage, 1.2 V, is represented in brown. The vias for the decoupling capacitors on top layer are the yellow circles. This power is feed to the center of the FPGA, were the power pins are placed. Arround it, the PLL analog 2.5 V source is represented in purple, while the digital PLL supply is represented in light green.

3.3.6. Ground planes

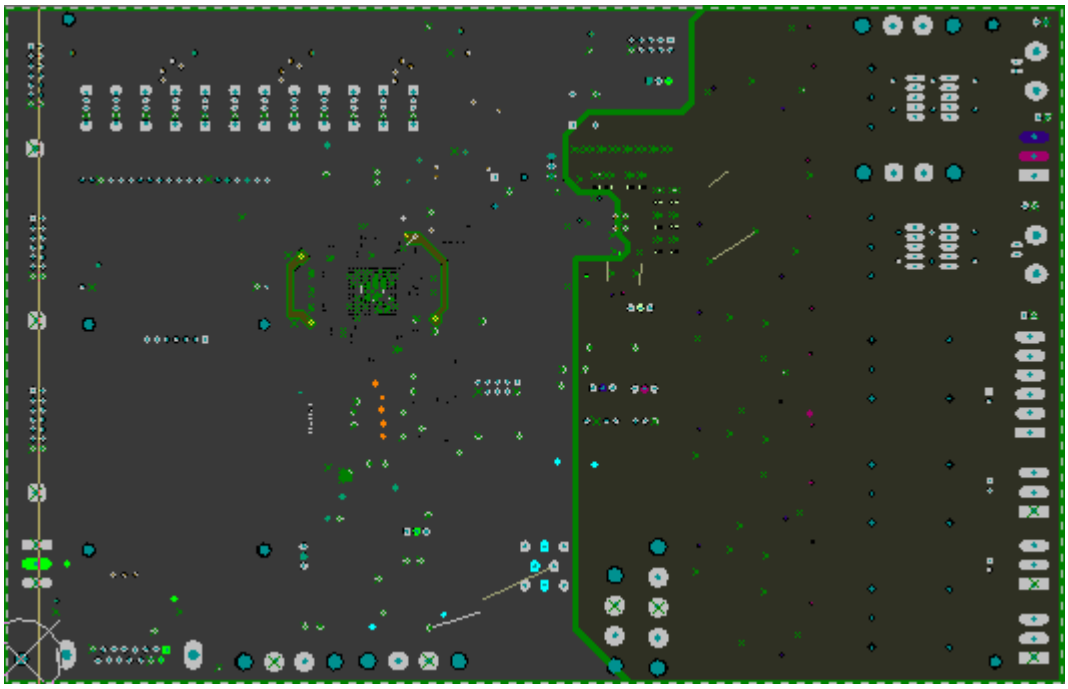


Figure 67. Ground plane

Two separate grounds are used, analog (right, green) and digital (left, gray).The union between them is done near the analog power supplies to create a star-like distribution topology. This union is done in top layer to further control its placement; it can be modified if necessary.

Near the FPGA, a small path to output the PLL digital power supply pins is created:

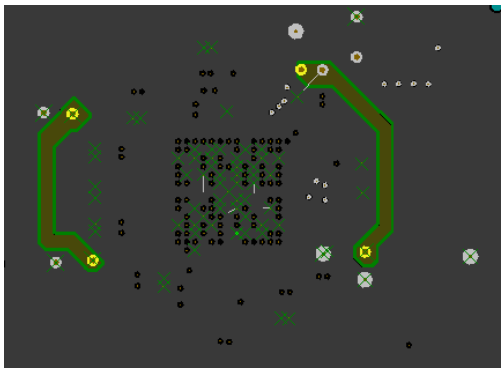


Figure 68. Ground plane FPGA detail.

As suggested by the design guide, all the vias connection is done by a solid pad, not a thermal one (increases inductance).

4. Budget

4.1. Component costs

The following table contains all the components included in the prototype, its unitary price and total price. Note that some general-purpose components were already available at GREP and no cost is associated with them.

Value		Part Reference	Package	Q	Ref/Price		
					Referencia	1 unit	total(eur)
FPGA	FPGA	EP4CE22F17C6N		1	544-2821-ND	68.18	68.18
	Configuration memory	EPCS16SI8N		1	989-EPCS16SI8N	17.36	17.36
	Cap 2.2nF Low ESL	LLL185R71H222MA01L	0306	2	81-LLL185R71H222MA01L	0.317	0.634
	Cap 4.7nF Low ESL	LLL185R71H472MA01K	0306	2	81-LLL185R71H472MA1K	0.297	0.594
	Cap 10nF 16V low ESL High freq	LLL185R71C103KA01L	0306	2	81-LLL185R71C103KA01	0.287	0.574
	Capacitor 0.47 uF 0603 (4)	0603ZD474KAT2A	0603	5	581-0603ZD474KAT2A	0.102	0.51
	Capacitor 0.1 uF 1206 (26)	VJ1206Y104KXQCBC	1206	24	77-VJ1206Y104KXQCBC	0.061	1.464
	Capacitor 0.1 uF 0603	6R3X14W104MV4T	0603	5	605-6R3X14W104MV4T	0.553	2.765
	Capacitor 10 uF 1206 (1)	TCJA106M10R300	1206	4	581-TCJA106M10R300	1.09	4.36
	Capacitor 100 uF 1210 (2)	TCJB107M6R70	1210	4	581-TCJB107M6R70	1.27	5.08
	Oscilator	KC7050A50.0000C3GE00		1	581-KC7050A50.C3GE	1.84	1.84
	Cap 10nF 16V low ESL High freq	LLL185R71C103KA01L	0306	2	81-LLL185R71C103KA01	0.287	0.574
	Cap 4.7nF Low ESL	LLL185R71H472MA01K	0306	2	81-LLL185R71H472MA1K	0.297	0.594
	Cap 2.2nF Low ESL	LLL185R71H222MA01L	0306	2	81-LLL185R71H222MA01L	0.317	0.634
	Capacitor 0.1 uF 1206 (26)	VJ1206Y104KXQCBC	1206	2	77-VJ1206Y104KXQCBC	0.061	0.122
	Capacitor 1uF, 16 V	77-VJ1206Y105MXJTBC	1206	2	77-VJ1206Y105MXJTBC	0.061	0.122
	Capacitor 0.01 uF, 25 V	12063A103JAT2A	1206	1	581-12063A103J	0.102	0.102
	Resistor 10kohm, 1%	CRCW121010K0FKEA	1210	5	71-CRCW1210-10K-E3	0.297	1.485
	Resistor 1kohm, 1%	CRCW12101K00FKEA	1210	1	71-CRCW1210-1.0K-E3	0.297	0.297
	Resistor 24.9ohm, 1%	CRCW121024R9FKEA	1210	1	71-CRCW1210-24.9-E3	0.297	0.297
	Inductance 10nH	1210AS-010K-01	1210	1	434-1210AS-010K-01	0.756	0.756
ADC	ADC	AD7658BSTZ-1	ST-64-2	1	584-AD7658BSTZ-1	16.13	16.13
	Diode Zener Vss, Vdd	BAT720	SOT23	5	8734569	0.164	0.82
	Capacitor 0.1uF, 10 V	VJ1206Y104KXQCBC	1206	14	77-VJ1206Y104KXQCBC	0.061	0.854
	Capacitor 1uF, 16 V	77-VJ1206Y105MXJTBC	1206	14	77-VJ1206Y105MXJTBC	0.061	0.854
	Inductance 10 nH	1210AS-010K-01	1210	1	434-1210AS-010K-01	0.756	0.756
	Capacitor	CC1206KKX5R8BB105	1206	2	603-	0.297	0.594

	decoupling 1 uF, 25 V				CC126KKX5R8BB105		
	Capacitor decoupling 0.1 uF, 25 V	CC1206KRX7R8BB104	1206	2	603-CC206KRX7R8BB104	0.246	0.492
	Jumper						0
SENSORS	Op Amp	AD8671ARZ	SOIC-8	5	1143298	2.59	12.95
	Voltage Sensor	LV 25-P		3	1617416	52.31	156.93
	Current Sensor	LA 25-NP		2	1617404	18.21	36.42
	Current Sensor (hole)	LA 55-P		2	1617405	24.15	48.3
	Diode Zener 9.1 V	SMAZ9V1-13-F	SMA	20	621-SMAZ9V1-13-F	0.272	5.44
	Capacitor 0.82uF (RC parallel filter)	GRM219R71E824KA88D	0805	5	81-GRM219R71E824KA8D	0.338	1.69
	Resistors 200 ohm (Rm)	TNPW1206200RBEEA	1206	3	71-TNPW1206200RBEEA	0.563	1.689
	Resistors 180 ohm (Rm)	TNPW1206180RBEEN	1206	2	71-TNPW12061800BEEN	0.87	1.74
	Capacitor 0.082uF (RC parallel filter)	VJ0805Y823JXXPW1BC	0805	5	77-VJ0805Y823JXXPBC	0.102	0.51
	Capacitor decoupling 10 uF, 25 V	CC1206MKX5R8BB106	1206	20	603-CC126MKX5R8BB106	0.297	5.94
	Capacitor decoupling 0.1 uF, 25 V	CC1206KRX7R8BB104	1206	20	603-CC206KRX7R8BB104	0.246	4.92
	Resistors 100 ohm (filter V)	FCR1206J10R	1206	4	279-FCR1206J10R	1.67	6.68
	Resistor 0ohm, 1%	SR06X000 PTL	0603	18	791-SR06X000PTL	0.108	1.944
	Resistor 20 kohm (filter V)	PCF1206R-20KBT1	1206	3	756-PCF1206R-20KBT1	0.328	0.984
	Capacitor electrolítico 1 uF, 400 V	ECA-2GM010		3	667-ECA-2GM010	0.262	0.786
	Capacitor 0.68 uF, 16 V (RC parallel filter)	CC1206KKX7R7BB684	1206	5	603-CC126KKX7R7BB684	0.328	1.64
	Capacitor 0.082uF, 100 V (2nd. RC filter)	VJ1206Y823MXBTW1BC	1206	5	77-VJ1206Y823MXBTBC	0.061	0.305
	Resistor 1.8 kohm (2nd. RC filter)	ERJ-14NF1801U	1210	5	667-ERJ-14NF1801U	0.262	1.31
	Capacitor 18pF, 50 V (real.)	VJ1206A180KXAAC	1206	5	77-VJ1206A180KXAAC	0.082	0.41
	Resistor 1 kohm (real.)	SG73S2ETTD102J	1210	10	660-SG73S2ETTD102J	0.194	1.94
	Capacitor 10pF, 10 V (3rst. RC filter)	VJ1206A100JXQCW1BC	1206	5	77-VJ1206A100JXQCBC	0.102	0.51
	Resistor 240 ohm (3rst. RC filter)	ERJ-14NF2400U	1210	5	667-ERJ-14NF2400U	0.262	1.31
	Resistor 10 ohm (decoupling filter)	ERJ-14YJ100U	1210	10	667-ERJ-14YJ100U	0.262	2.62

LED	LED	SML-LX1206SOC-TR	1206	12	696-SML-LX1206SOC	0.44	5.28
	red de 4 Resistors 330 ohm	CRA12E083330RJTR		3	71-CRAE12-330/R	0.235	0.705
LCD	LCD Display	EA DOGM163L-A		1	790-EADOGM163LA	16.6	16.6
	Capacitor 0.1 uF, 10 V	VJ1206Y104KXQCBC	1206	1	77-VJ1206Y104KXQCBC	0.061	0.061
	Capacitor 1uF, 16 V	77-VJ1206Y105MXJTBC	1206	2	77-VJ1206Y105MXJTBC	0.061	0.122
	Capacitor 10 uF, 10 V	C1206C106K8PACTU	1206	1	80-C1206C106K8P	0.348	0.348
Teclado	Matrix Keyboard 3x4	ECO.12150.06		1	1130805	10.89	10.89
	4-Resistor Network 1kohm	CRA12E0831K00JTR		1	71-CRA12E-J-1K	0.235	0.235
SWITCH	Switches	0S102011MS2QN1		12	611-OS102011MS2QN1	0.44	5.28
	Hex Smitch Trigger (buttons)	74ALVC14D,112	SOT-108	1	771-ALVC14D112	0.464	0.464
	Button ON/OFF	UB16SKG03N		1	UB16SKG03N-ND	7.45	7.45
	Reset Button	ESE20C343		1	2079610	0.807	0.807
	3 Button	1571634-2		3	506-1571634-2	0.29	0.87
	Button Start	1241.1082.3		1	693-1241.1082.3	2.36	2.36
	red de 4 Resistors 1kohm	CRA12E0831K00JTR		3	71-CRA12E-J-1K	0.235	0.705
	red de 4 Resistors 100kohm	CRA12E083100KJTR		1	71-CRA12E-J-100K	0.235	0.235
	red de 4 Resistors 10kohm	CRA12E08310K0JTR		1	71-CRAE12-10K/R	0.235	0.235
	Resistor 10kohm, 1%	CRCW121010K0FKEA	1210	1	71-CRCW1210-10K-E3	0.297	0.297
	Resistor 100 kohm, 1 %	CRCW1210100KFKEA	1210	1	71-CRCW1210-100K-E3	0.297	0.297
	Capacitor 0.1 uF, 10 V	VJ1206Y104KXQCBC	1206	6	77-VJ1206Y104KXQCBC	0.061	0.366
	Capacitor 1uF, 16 V	77-VJ1206Y105MXJTBC	1206	1	77-VJ1206Y105MXJTBC	0.061	0.061
Encoder	8-Channel Buffer	74AHC244D,118	SOIC-20	1	771-AHC244D118	0.407	0.407
	Resistor 0ohm, 1%	SR06X000 PTL	0603	1	791-SR06X000PTL	0.108	0.108
	Capacitor 0.1uF, 10 V	VJ1206Y104KXQCBC	1206	2	77-VJ1206Y104KXQCBC	0.061	0.122
	Capacitor 10 uF, 10 V	C1206C106K8PACTU	1206	1	80-C1206C106K8P	0.348	0.348
	Capacitor 1uF, 16 V	77-VJ1206Y105MXJTBC	1206	1	77-VJ1206Y105MXJTBC	0.061	0.061
EXT GPIO	Capacitor 0.1uF, 10 V	VJ1206Y104KXQCBC	1206	1	77-VJ1206Y104KXQCBC	0.061	0.061
	Capacitor 1uF, 16 V	77-VJ1206Y105MXJTBC	1206	1	77-VJ1206Y105MXJTBC	0.061	0.061
Conectores	Conector Encoder D-SUB 15	1734355-1		1	718-3590	4.03	4.03
	Conector Jack, opción 1 (2 mm)	RASM722X	SMD	1	502-RASM722X	1.15	1.15
	Conector BNC	5227161-1		8	571-5227161-1	3.29	26.32

	Conector Anderson +-15V			2			0
	Conector Idc 10 pins EXTGPIO			1			0
	Conectores Idc 14 pins OUT			2			0
+/- 15 V	TRACOPOWER 6W +15V,-15V	TMR 6-0523		1	755-3532	20.6	20.6
	Capacitor 22 uF TRACO	C4532X5R1A226M230KA	1812	1	810-C4532X5R1A226M	1.05	1.05
	Inductance 1.1uH BOURNS	SRF0504-351Y	1210	1	652-SRF0504-351Y	1.31	1.31
3,3 V	Voltage regulator	ADP2301AUJZ-R7	TSOT-6	1	584-ADP2301AUJZ-R7	2.14	2.14
	Diode zener Schottky	1N5819HW-F	SOD-123	1	621-1N5819HW-F	0.522	0.522
	Inductance 4.7 uH	VLC5045T-4R7M	5045 (mm)	1	810-VLC5045T-4R7M	0.481	0.481
	Capacitor 10 uF, 16 V	GRM31CR71C106KA12L	1206	1	81-GRM31CR71C106KA12L	0.297	0.297
	Capacitor 22 uF, 6.3 V	C3216X5R0J226M	1206	1	810-C3216X5R0J226M	0.491	0.491
	Capacitor 0.1 uF, 10 V	VJ1206Y104KXQCBC	1206	1	77-VJ1206Y104KXQCBC	0.061	0.061
	Resistor 31.6 kohm, 1 %	CRCW121031K6FKEAHP	1210	1	71-CRCW121031K6FKEAH	0.072	0.072
	Resistor 10kohm, 1%	CRCW121010K0FKEA	1210	1	71-CRCW1210-10K-E3	0.297	0.297
	Resistor 402 kohm, 1 %	CRCW1210402KFKEA	1210	1	71-CRCW1210402KFKEA	0.297	0.297
	Resistor 100 kohm, 1 %	CRCW1210100KFKEA	1210	1	71-CRCW1210-100K-E3	0.297	0.297
2.5 V	Voltage regulator LDO	LP2992IM5-2.5/NOPB	SOT-23-5	1	926-LP2992IM525NOPB	1.11	1.11
	Capacitor 0.01 uF, 25 V	12063A103JAT2A	1206	1	581-12063A103J	0.102	0.102
	Capacitor 10 uF, 10 V	C1206C106K8PACTU	1206	2	80-C1206C106K8P	0.348	0.696
1.2 V	Switching Voltage Converter	LM2852XMXA-1.2/NOPB	TSSOP-EP-14	1	926-LM2852XMXA12NOPB	4.1	4.1
	Inductance 1 uH	LQM21PN1R0MC0D	0805	1	81-LQM21PN1R0MC0D	0.297	0.297
	Capacitor 22 uF, 6.3 V	C3216X5R0J226M	1206	1	810-C3216X5R0J226M	0.491	0.491
	Capacitor 0.1 uF, 10 V	VJ1206Y104KXQCBC	1206	1	77-VJ1206Y104KXQCBC	0.061	0.061
	Capacitor 0.01 uF, 25 V	12063A103JAT2A	1206	1	581-12063A103J	0.102	0.102
	Capacitor 10 uF, 10 V	C1206C106K8PACTU	1206	1	80-C1206C106K8P	0.348	0.348
5 V ana	Linear Voltage regulator	ADP3303ARZ-5	SOIC-8	1	584-ADP3303ARZ-5	2.65	2.65
	Capacitor 10 uF, 10 V	C1206C106K8PACTU	1206	2	80-C1206C106K8P	0.348	0.696
	Capacitor 0.1 uF, 10 V	VJ1206Y104KXQCBC	1206	1	77-VJ1206Y104KXQCBC	0.061	0.061
	Resistor 402 kohm, 1 %	CRCW1210402KFKEA	1210	1	71-CRCW1210402KFKEA	0.297	0.297
5 V dig	Linear Voltage regulator	L4940D2T5-TR	DPAK-3	1	511-L4940D2T5-TR	1.49	1.49
	Capacitor 10 uF, 10 V	C1206C106K8PACTU	1206	2	80-C1206C106K8P	0.348	0.696

Other	Diode zener	PMEG2010AEB,115	SOD-523	4	771-PMEG2010AEBT/R	0.369	1.476
	Resistor 390ohm	CRCW1210390RJNEA	1210	1	71-CRCW1210J-390-E3	0.246	0.246
	Button ON-OFF	UB26SKW035FJF-RO		1	633-UB26SKW035FJF-RO	10.56	10.56

TOTAL	**Total component price**						**565.542**

Table 10. Components budget.

The next image represents the total component price by its price. Note that the main costs are related with the sensors. Most part of the sensors, like current and voltage sensors were already available at GREP and does not represent a real cost to the prototype, but were included to represent the actual cost of the board.

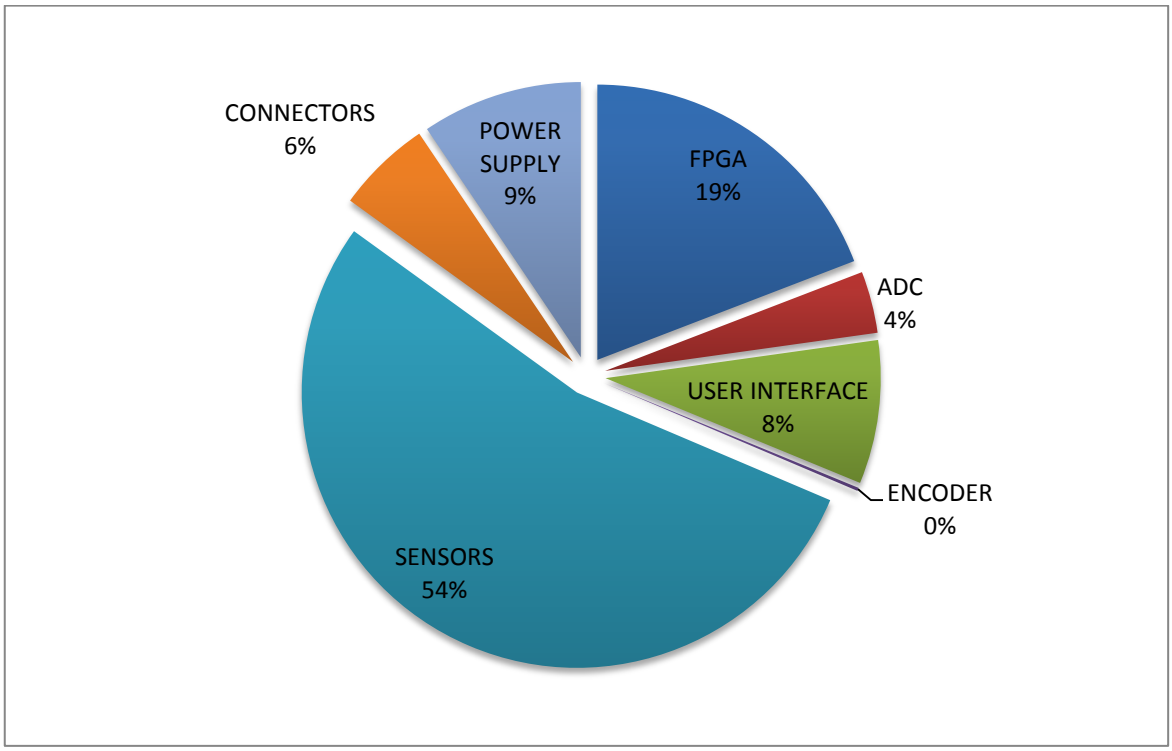


Figure 69. Components price by function.

4.2. Total prototype costs

Description	Quantity/Hrs	Price	Total (Eur)
Project manager, supervisor	300	40	12000
Project elaboration	900	30	27000
PCB Fabrication (EUROCIRCUITS, STD 4 Layer)	1	233.45	233.45
Special components soldering (BGA, TQFN)	1	98.09	98.09
TOTAL			**39331.54**

Table 11. Total prototype costs.

5. Conclusions and future development

The work elaborated during the thesis development has been presented. The project methodology allowed acquiring a deep knowledge in current multi-level technology and its actual implementation in a prototype by means of a FPGA. The preliminary tests are presented and prototype problems were described, specially noise-related problems that revealed the importance of ground design in mixed signal circuits.

An insight into the details and complexity on the design of a state-of-the art FPGA has been presented as well as board implementation and component selection.

In order to improve the board design, PCB design software allows performing signal integrity analysis that takes into account the actual board line characteristics (Characteristic impedance, length, etc) so the high-speed signals are optimized in the design. This is only required for a small number of lines, like the *DATA0* (Serial output from EPCS device) or the ADC data lines and clocks.

Also, both Altera and Xilinx have developed communication channels with MATLAB/SIMULINK. As GREP work is first tested in these simulation environments, it is worth investigating the connection possibility between the prototype board and SIMULINK models that would easier the project development and result obtaining.

The relative sensor cost in the prototype costs is more than 50% of the total component costs. A balance between robustness, easiness of use, safety and cost must be obtained. This is especially true for voltage sensors in the sensors. As this work presens a one-run fabrication, safety and previous experience made us chose hall-effect sensors but for a larger run, a revision in this side must be considered

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Glossary

GREP. Power Electronics Research Group at the University of Catalonia.

PWM. Pulse Width Modulation. Simple modulation scheme.

EMC. Electro-Magnetic compatibility. Studies the unintentional generation, propagation or reception of electromagnetic enegergy.

dSpace. Digital signal processing and control engineering. In the text is used to refers to the control units fabricated by this manufacturer.

MAC. Multilevel Active-Clamped Converter. Multilevel topology whose basic cell is composed only by a diode and a transistor.

FPGA. Field Programmable Logic Array. Device with configurable logic which is used to implement the control and converter algorithm.

CPLD. Complex Programmable Logic Device. In contrast with a FPGA, make use of a interconnexion matrix and are normally smaller than them.

LQFP. Low-profile Quad Flat Package. Refers to a surface-mount component package.

SMT. Surface-mount technology. Technology in which the components are placed directly to the surface of the board.

Duty cycle. In Power Electronics Design, refers to the amount of time a signal is high or active. Normally expressed as a relation between the on and off time of the signal.

PMSM. Permanent Magnet Synchronous Motor.

THD. Total Harmonic Distortion. Measurement that evaluates the harmonic distortion of a signal over its fundamental component.

TU. Time Unit. In the text is used to stabilise the minimum unitary time that the FPGA can distinguish.

ADC. Analog to digital converter.

Hard-IP Block: Signal Tap II. In contrast with a soft-IP block, the hard-IP block is defined by a hardware present on a device, rather than on a software that can be configured.

JTAG. Joint Test Action Group. Comunication standard, “Standard Test Access Port and Boundary-Scan Architecture”, IEEE Std. 1149.1-1990.

SPI. Serial Peripherial Interface. 4 line communication standard.

LCD. Liquid Crystal Display.

LED. Light-Emiting Diode