Design of Low Noise Readout Amplifiers for Monolithic Capacitive CMOS-MEMS Accelerometers

Author: Josep Maria Sánchez Chiva

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Supervisors: Jordi Madrenas Boadas & Piotr Jozef Michalik

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Acronyms

A/D	Analog-to-Digital Converter
AC	Alternating current
AM	Amplitude Modulation
ASIC	Application Specific Integrated Circuit
BW	BandWidth
CAD	Computer-Aided Design
CDS	Correlated Double Sampling
CMFB	Common-Mode Feed Back
CMOS	Complementary Metal Oxide Semiconductor
CSA	Charge Sensitive Amplifier
CTC	Continuous-Time Current
CTV	Continuous-Time Voltage
DC	Direct Current
EMI	ElectroMagnetic Interference
EKV	Enz-Krummenacher-Vittoz
FoM	Figure of Merit
FPGA	Field Programmable Gate Array
GNU	GNU's Not Unix
IC	Inversion Coefficient
IHP	Innovations for High Performance (German Company)
LHP	Left-Half Plane
MEMS	Micro Electro Mechanical System
MEMSoC	Micro-Electro-Mechanical-System on Chip
MIM	Metal-Insulator-Metal
MOS	Metal Oxide Semiconductor
NMOS	N-type Metal Oxide Semiconductor

opamp	Operational Amplifier
OTA	Operational Transimpedance Amplifier
PCB	Printed Circuit Board
PM	Phase Margin
PMOS	P-type Metal Oxide Semiconductor
PSRR	Power Supply Rejection Ratio
RC	Resistor-Capacitor
RHP	Right-Half Plane
SC	Switched Capacitor
SEM	Scanning Electron Microscope
SI	Strong Inversion
SiGe	Silicon Germanium
SNR	Signal-to-Noise Ratio
SR	Slew Rate
TIA	TransImpedance Amplifier
UGB	Unity-Gain Bandwidth
WI	Weak Inversion

Ackowledgements

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Abstract

This thesis report describes the design process, the implementation and the simulation and measurement results of two different readout circuits to be used with two monolithic MEMS accelerometers fabricated by post-CMOS surface micromachining based on isotropic wet etching in IHP SiGe 0,25 μm technology. The first design is used with a 50 fF z-axis sensor and the second design with a 200 fF sensor as well as the first sensor.

The approach used has been the Continuous Time Voltage (CTV) sensing implemented in two ways. The first readout circuit implements a CTV sensing utilising an open-loop topology whereas the second design implements a CTV sensing with a closed-loop amplifier and low duty-cycle reset. In both designs, chopper stabilisation has been implemented to get rid of DC offset and Flicker noise, making both designs to work beyond the noise corner frequency to obtain the lowest achievable noise floor: thermal noise.

The target during the design of both circuits has been to design amplifying circuits with a thermal noise equal or below the Brownian-noise of the capacitive sensor in order to make the noise from the sensor to be dominant. This has been possible by means of a deep study of noise and the optimisation of the transistor dimensions ratio that have the highest noise influence: input pair transistors. In both cases, equations that relate input node capacitance with noise have been found and final values have been obtained by fine tuning using the design software following the hypothesis found in the derived equations.

The first design has been fabricated and total noise using opamp measured noise shows a noise floor of $238\,\mu g/\sqrt{Hz}$, a lower noise value than designs with sensors having a similar sensitivity found in the literature. Second design has not been fabricated yet, but simulations also show a good noise performance of $20\,\mu g/\sqrt{Hz}$ with the second sensor. However, differences in measured and simulated noise in the first design shows that the total noise of the second design using the second sensor may be lower than the simulated value due to a rather pessimistic noise model used by the software.

Resum

Aquesta tesi descriu el procés de disseny, la implementació i els resultats de les simulacions i les mesures de dos circuits de condicionament de senyal per ser usats amb dos sensors d'acceleració monolítics fabricats en el procés *post-CMOS surface micromachining* basat en *isotropic wet etching* en tecnologia IHP SiGe 0,25 µm. El primer disseny s'ha implementat amb un sensor de 50 fF de *z-axis*, mentre que el segon s'ha implementat, a més a més d'aquest mateix sensor, amb un segon sensor de 200 fF.

El mètode utilitzat ha sigut el de sensat de Voltatge en Temps Continu (CTV) implementat de dues maneres. El primer disseny implementa el sensat CTV utilitzant una topologia en llaç obert, mentre que el segon disseny implementa el sensat CTV mitjançant un amplificador en llaç tancat i un reset amb baix *duty-cycle*. En ambdós dissenys, s'ha usat estabilització *chopper* per a eliminar *offset* DC i soroll *Flicker*, fent treballar els dos dissenys per sobre de la freqüència colze de soroll per tal d'obtenir el mínim soroll: soroll tèrmic.

L'objectiu durant el disseny dels dos circuits ha sigut el de dissenyar dos circuits de condicionament amb un soroll tèrmic igual o menor al soroll Brownià del sensor capacitiu per tal de fer que el soroll dominant sigui el provinent del sensor. Això ha sigut possible gràcies a un profund estudi del soroll i l'optimització de les dimensions dels transistors que tenen una major influència: el parell de transistors d'entrada. En els dos casos, s'han elaborat equacions que relacionen la capacitat al node d'entrada amb el soroll, i els valors finalment usats han sigut obtinguts utilitzant el *software* de disseny seguint les hipòtesis marcades per les expressions obtingudes.

El primer disseny ha sigut fabricat i el soroll total usant el soroll mesurat de l'amplificador és de $238\,\mu g/\sqrt{Hz}$, un soroll més baix que dissenys trobats a la literatura amb sensors amb una sensitivitat similar. El segon disseny no s'ha fabricat encara, però les simulacions mostren un bon valor de soroll de $20\,\mu g/\sqrt{Hz}$ amb el segon sensor. Malgrat tot, les diferències trobades entre el soroll mesurat i el simulat per al primer disseny fan creure que el soroll del segon disseny amb el segon sensor podria ser menor degut a que els models usats pel *software* semblen ser pessimistes pel que fa al soroll.

Resumen

Esta tesis describe el proceso de diseño, la implementación y los resultados de las simulaciones y las medidas de dos circuitos de acondicionamiento de señal para ser usados con dos sensores de aceleración monolíticos fabricados mediante el proceso *post-CMOS surface micromachining* basado en *isotropic wet etching* en tecnología IHP SiGe 0,25 µm. El primer diseño se ha implementado con un sensor de 50 fF de *z-axis*, mientras que el segundo se ha implementado, además de con éste mismo sensor, con un segondo sensor de 200 fF.

El método utilizado ha sido el de sensado de Voltage en Tiempo Continuo (CTV) implementado de dos maneras. El primer diseño implementa el sensador CTV utilisando una topología en lazo abierto, mientras que el segundo diseño implementa el sensado CTV mediante un amplificador en lazo cerrado y un reset con bajo *duty-cycle*. En ambos diseños, se ha usado la estabilizació *chopper* para eliminar el *offset* DC y el ruido *Flicker*, haciendo trabajar ambos diseños por encima de la frecuencia codo de ruido para obtener el riudo mínimo: ruido térmico.

El objetivo durante el diseño de los dos circuitos ha sido el de diseñar dos circuitos de acondicionamiento con un ruido térmico igual o inferior al ruido Browniano del sensor capacitivo de modo que el ruido dominante sea el que proveniente del sensor. Ésto ha sido posible gracias a un profundo estudio del ruido y la optimizacion de las dimensiones de los transistores que tienen una mayor influencia: el par de transistores de entrada. En los dos casos, se han elaborado equaciones que relacionan la capacidad en el nodo de entrada con el ruido, y los valores finalmente usados han sido obtenidos mediante el *software* de diseño siguiendo las hipótesis marcadas por las expresiones obtenidas.

El primer diseño ha sigdo fabricado i el ruido total usando el ruido medido del amplificador es de $238\,\mu g/\sqrt{Hz}$, un ruido más bajo que el de diseños encontrados en la literatura con sensores con una sensibilidad similar. El segundo diseño aún no se ha fabricado, pero las simulaciones muestran un buen ruido de $20\,\mu g/\sqrt{Hz}$ con el segundo sensor. Sin embargo, las diferencia encontradas entre el ruido medido y el simulado del primer diseño hacen creer que el ruido del segundo diseño con el segundo sensor podria ser menor debido a que los modelos usados por el *software* parecen ser pesimistas respecto al ruido.

1 INTRODUCTION

In the last decades, MEMS (Micro Electro Mechanical Systems) have allowed the miniaturization of sensors up to the point where sensors are fabricated in CMOS compatible processes that allow electronics to be fabricated within the same die area [1][2][3][4][5]. This process has brought an improvement in batch fabrication, higher yield, smaller size, lower power and lower cost [5]. Furthermore, the use of capacitive MEMS sensors such as accelerometers and gyroscopes present advantages over piezoelectric sensors, as capacitive sensors present higher sensitivity, lower power dissipation, lower temperature coefficient, lower noise and lower fabrication cost [3][6][7][8][9][10].

As a consequence, the MEMS market has grown in the last years thanks to the inclusion of MEMS sensors in a wide range of devices. Automotive applications, biomedical applications, in consumer applications such as smartphones and tablet PC's, robotics, shock detection systems and military applications are some examples [1][2][4][11][12].

However, with the mentioned improvement in MEMS sensors, optimised readout circuits and techniques have also been developed in order to meet the demanding performances expected for the aforementioned applications.

In that way, this Master Thesis is focused in the development of two readout circuits for capacitive CMOS-compatible MEMS accelerometers with important constraints in terms of sensing capacitance, parasitic capacitances and, most important, noise added by the circuit and its power consumption.

1.1 State of the art

There exist two main fabrication processes for capacitive MEMS accelerometers: Bulk micromachining and surface micromachining [4][10]. In the former, sensors have a greater proof mass and therefore they have bigger sensing capacitance and sensitivity, but the main drawback of this process is the need of wafer bonding [4]. On the other hand, surface micromachining allows capacitive sensors to be fabricated in the same die that the electronics, providing lower interconnect parasitics between the sensor and the electronics but a much lower sensing capacitance [4][10].

Surface micromachined sensors can achieve sub-100 fF sensing capacitances that present

new challenges to designers due to the lower sensor sensitivity [10] and electromagnetic interference (EMI) because their sensing node has high impedance [4]. Furthermore, with such small sensing capacitance, the readout circuit parasitics present a greater impact.

As a direct consequence, readout circuits must be designed carefully in order to avoid further degradation of the sensor performance: parasitics added by the electronics must be minimized and the circuit has to be capable to deal with such lower sensitivity sensors. Moreover, in order to avoid deteriorating the SNR of the system, the noise added by the electronics must be kept at the level of the sensor thermal-mechanical Brownian noise or below [7]. Finally, circuits are also expected to have a low power consumption while meeting all the specifications explained above.

In order to deal with the previously explained challenges, different approaches have been used in order to design readout and amplifying circuits for capacitive MEMS sensors: switched-capacitor (SC) charge integration, continuous-time current (CTC) sensing and continuous-time voltage (CTV) sensing [7][10].

Switched-capacitor charge integration readout circuits present a virtual ground at the input and a robust biasing, making the circuit parasitic insensitive, robust and accurate. Correlated double sampling (CDS) is a variation of SC circuits that provides the suppression of low-frequency noise and offset [7][8]. However, both SC and CDS readout circuits still presents an important noise folding and switch noise as well as a more complex clock and switching circuitry, making, in general, their noise performance worse than that of continuous time circuits [10].

Continuous-time current sensing circuits [14] are implemented as transimpedance amplifiers (TIA) that present a virtual ground at the input node and thus a removal of input parasitic capacitance and a robust DC biasing at the sensing node through a feedback resistor. However, this feedback resistor generates a pole that reduces the bandwidth and the output noise is mainly dominated by thermal noise of this resistor [8] that is somehow compensated by a reduction of the switch noise compared to SC topology. However, opamp noise removal is not completely compensated by this topology because the gain is proportional to the resistor value.

To overcome this relationship between gain and noise, continuous-time voltage sensing is used. CTV sensing can be implemented with an open-loop or capacitively fed back amplifier. This topology presents the main drawback of a lack of DC biasing at the sensing node and, consequently, a challenge with this node parasitics and biasing. In this case, there is no

noise from any resistor, but as it will be observed in following sections, there may be a reduction in SNR if circuits are not accurately designed: open-loop CTV has a signal attenuation at the sensing node due to the voltage divider formed by the sensor and its parasitic capacitance; on the other hand, closed-loop CTV suffers opamp noise modulation proportional to the capacitance hanging at its input node. However, this topology has been reported to present the best noise performance [10].

Furthermore, continuous-time topologies make use of chopper stabilization in order to reduce Flicker noise and DC offset by working beyond the noise corner where Flicker and thermal noise meet [8][9][10][15].

1.2 Motivation

This Master Thesis project is enclosed in the Micro-Electro-Mechanical System on Chip (MEMSoC) — Spanish National Research project TEC2011-06116 with the purpose of the design and fabrication of a readout circuit for two MEMS capacitive accelerometers. During the project, two readout circuits have been designed, the former has been already fabricated in IHP SiGe 0,25μm technology and the second one has been recently taped out and it is going to be fabricated in the coming months using the same technology.

Both circuits have been designed to be low-power and low-noise in order to compare the performance between both topologies with the existing ones in the literature.

2 SENSORS CHARACTERISTICS

Two different z-axis out-of-plane MEMS capacitive accelerometers have been used that are part of Mr. Piotr Michalik's PhD thesis, currently under development. The first sensor has been fabricated in post-CMOS surface micromachining process based on isotropic wet etching applied to IC's manufactured in IHP SiGe 0,25 μm technology [12] in the same die area that the electronics. The second sensor has been taped out recently and it is expected to be fabricated on the same technology in the coming months.

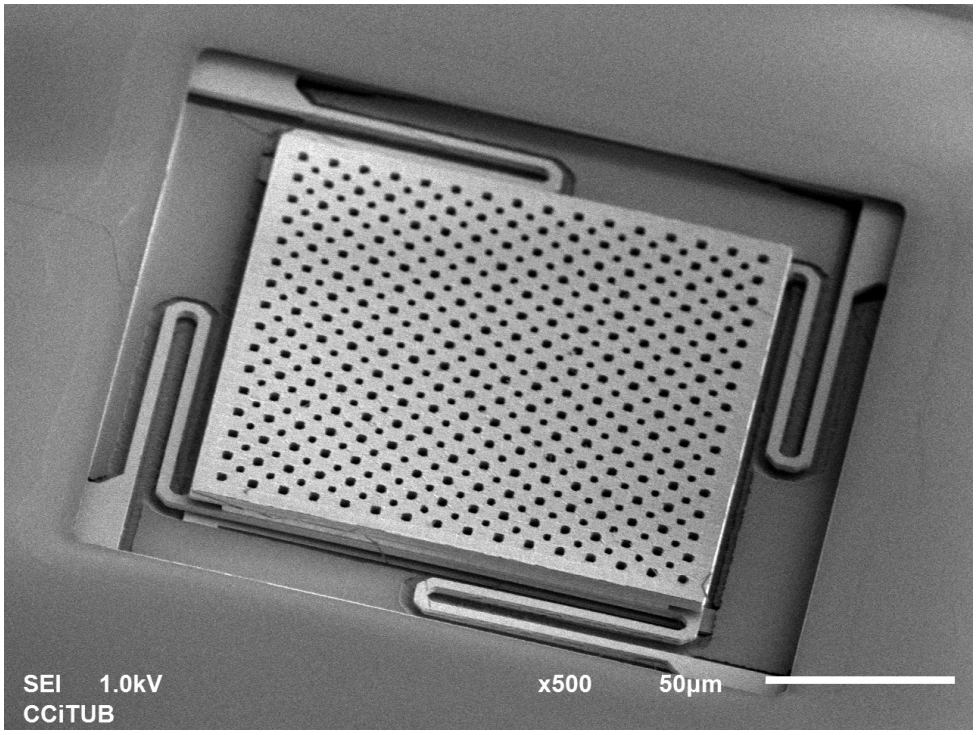

Figure 2.1: SEM image [13] of a prototype 50 fF sensor.

The characteristics of each sensor are presented in Table 2.1:

	Sensor 1	Sensor 2
Resonant frequency [kHz]	20	6,6
Sensing capacitance [fF]	50	200
Sensitivity [fF/g]	0,013	0,25
Dynamic range [fF]	±5	±20
Mass [ug]	0,6	5
Input parasitic capacitance [pF]	1	3,16
Output parasitic capacitance [fF]	200	630

Table 2.1: Characteristics of the sensors [13].

In Table 2.1, sensing capacitances values have been obtained by estimating it from layout, mass is a rough estimation and input and output parasitic capacitances have been obtained from parasitic extraction using Assura tool configured to give C only extraction for selected nodes. Moreover, the quality factor *Q* has been impossible to obtain as it depends on packaging pressure, so a very conservative value will be used, $Q=0,5$, that is the lowest practical value for an open-loop sensor in order to obtain the worst case noise value.

In order to set a noise specification for the readout circuits, it is important to know the thermal noise present at the sensor. The noise of such type of sensors has its origin in the thermal noise of the sensor molecules at a given temperature. This thermal noise produces an agitation of the sensor through a Brownian motion process. The equivalent acceleration noise due to the agitation of the sensor can be equated with equation (Eq. 2.1) [16].

$$\frac{\overline{a_n}}{\Delta f}=\sqrt{\frac{4k_B T \omega_r}{mQ}} \tag{2.1}$$

Where $k_B \approx 1,38065 \cdot 10^{-23} m^2 kg\ s^{-2} K^{-1}$ is the Boltzmann constant, $T=300\,K$ is the room temperature, ω_r is the sensor resonant frequency, *m* is its mass and *Q* is its quality factor.

Acceleration noise values calculated with figures from Table 2.1 and the *Q* factor approximation are presented in Table 2.2:

	$\frac{\overline{a_n}}{\sqrt{\Delta f}}[\mu g/\sqrt{Hz}]$
Sensor 1	268,81
Sensor 2	16,58

Table 2.2: Brownian noise of the sensors.

It is important to take into account, however, that the noise values calculated in Table 2.2 are just rough estimations of the real thermal-Brownian noise of the sensors as several estimated and worst case approximated values have been used.

In order to be able to deal with the noise value during the design of the readout circuit, it is important to have the Brownian-noise of the sensor in units used during this design. In this case, it is useful to convert noise into $F/\sqrt{Hz}$ units. This is possible taking into account that the sensitivity *S* can be expressed as in equation (Eq. 2.2).

$$S = \frac{\Delta C}{\Delta a} \tag{2.2}$$

Where ΔC is the variation of capacitance and Δa the corresponding acceleration. This expression can be used for noise as the term $\sqrt{Hz}$ from both terms in noise units is eventually removed, making *S* to have F/g dimensions. So modifying equation (Eq. 2.2), it is possible to obtain the equivalent sensor noise in capacitance units using equation (Eq. 2.3):

$$\frac{\overline{\Delta C_n}}{\sqrt{\Delta f}} = S \frac{\overline{\Delta a_n}}{\sqrt{\Delta f}} \tag{2.3}$$

So now using the sensitivity in Table 2.1 and noise in acceleration units from Table 2.2 it is possible to obtain the noise in capacitance units in Table 2.3:

	$\frac{\overline{\Delta C_n}}{\sqrt{\Delta f}}[F/\sqrt{Hz}]$
Sensor 1	$3{,}5 \cdot 10^{-21}$
Sensor 2	$4{,}1 \cdot 10^{-21}$

Table 2.3: Sensors noise in capacitance units.

2.1 The proposed approach

The characteristics of the MEMS accelerometer presented in the previous section presents several challenges in terms of sensitivity, sensing capacitance, sensor parasitics and Brownian noise floor that makes the design of the readout circuits challenging. For this reason, two different readout circuits have been designed in order to be used with the sensors and to compare their performance.

Continuous-time voltage-mode amplifiers have been designed due to their reported better noise performance [10]. However, both open-loop and capacitively feedback topologies have been designed as they present different noise and gain characteristics in order to test both topologies and compare both performances.

Both circuits make use of chopper stabilization in order to avoid DC offset and to work in a frequency well beyond the noise corner frequency. Fully differential topology is also employed in order to increase common-mode noise rejection from the driving voltage and a better performance on power supplies noise rejection. Furthermore, fully differential topology

allows an increase of the output voltage swing.

Both have been designed to make the readout amplifier noise to have the lower impact as possible in the final total noise. In other words, to make the thermal-Brownian noise to be the dominant noise source of the circuit. Doing so, the lowest measurable acceleration is set mainly by the sensor and not the readout circuit, and thus maximizing the resolution of the system.

3 OPEN LOOP AMPLIFICATION APPROACH

3.1 Introduction

The design of the first readout circuit started in a time constrained scenario, so a simple and robust schematic was desired with a straightforward to do layout. This simplicity was also desired when designing the biasing of the input nodes, so a Common-Mode FeedBack (CMFB) amplifier was immediately discarded. Instead, a simpler strategy to bias the inputs of the opamp was needed. Moreover, a high Signal-to-Noise Ratio (SNR) was expected, so the maximisation of this figure of merit through the design of the opamp was a must.

In Figure 3.1 the view of the full implemented system design is shown in which the proposed readout circuit is included.

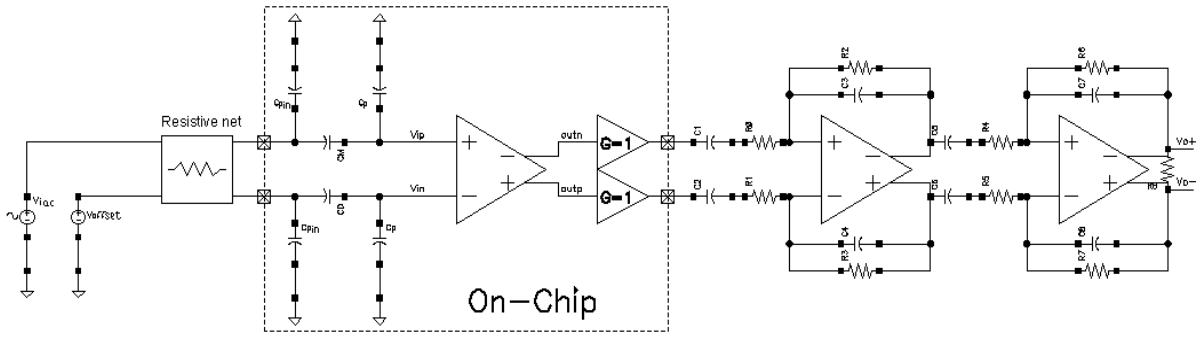

Figure 3.1: View of the system level design for the first readout circuit.

In Figure 3.1, the On-Chip amplifier that will be thoroughly explained in the following chapters is followed by unity gain amplifiers made with source followers in order to isolate the opamp from pad capacitances. Off-Chip, a resistive and filtering net is used previous to the input in order to be able to control the AC signal amplitude driven at each input in order to overcome the different gain of each capacitive voltage divider. Besides, the input DC offset can also be tuned. At the output of the chip, the signal is followed by two charge sensitive amplifiers (CSA) that provide a certain gain and filtering. The off-chip circuit and PCB design are detailed in [17].

In order to meet all the simplicity needs and noise requirements, a continuous-time voltage-mode (CTV) readout amplifier was designed using a fully-differential topology in open-loop configuration and chopper stabilisation.

Open-loop voltage-mode configuration provides an easy to design and robust readout circuit

with a reduced design time compared to closed-loop topologies: The open-loop configuration amplifies the output voltage from the voltage divider formed by the MEMS sensor and its output parasitic capacitance. To implement this in a fully differential topology, a working MEMS sensor and a dummy unreleased sensor where used.

Open-loop CTV configuration adds an important amount of capacitance at the input of the opamp, while CTC amplification through a TIA lacks from this capacitance issue as the input node is a virtual ground. However, open-loop CTV was chosen over CTC for two main reasons: first, CTV has been reported to have the best noise performance [7][10], mainly because CTV lacks from the noise added by the feedback resistor, and second, because an optimization strategy has been derived in order to maximise easily the SNR of this topology through input transistor dimensions tuning, being able to restrict the affectation of the input parasitic capacitance.

Finally, a fully-differential topology was used in order to easily increase the SNR as this topology reduces common-mode noise and improves supply voltage and ground PSRR. Also, a simple technique for input voltage biasing has been designed that biases the inputs of the opamp in a fashion that simplifies the design. Besides, chopper stabilization has been implemented in order to avoid Flicker noise and to work at frequencies where white noise dominates.

3.2 Top level circuit study

In Figure 3.2, the top level schematic of the readout circuit proposed is shown:

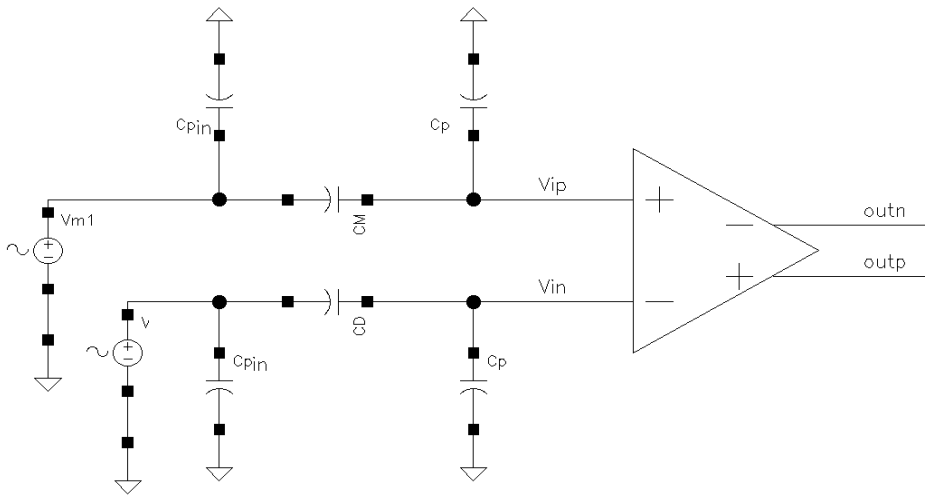

Figure 3.2: Top level schematic of the first readout circuit.

Where C_M is the sensor, C_D is the unreleased sensor used as a dummy sensor and C_p are the parasitic capacitances at the output of both sensors. C_{pin} are the input capacitances of the sensors.

The parasitic capacitance C_p at the output of the sensors have been used to create a capacitive voltage divider that is used to convert the variation of capacitance due to acceleration into a variation of voltage at the input of the operational amplifier. Besides to this C_p, the parasitics of the input stage of the opamp, C_{opamp}, must be taken into account as it is a main concern because the higher the parasitic capacitance, the higher the loss of the voltage divider and the SNR as it can be seen in equation (Eq. 3.1):

$$V_{ip} = V_{m1} \frac{C_M}{C_M + C_p + C_{opamp}} \tag{3.1}$$

Where V_{ip} is the voltage at the input of the opamp, V_{m1} is the driving voltage, C_M is the capacitance of the MEMS sensor and C_p is its parasitic capacitance.

In order to boost the gain of the given voltage divider, the sensor node with the higher parasitics ($C_{p\,in} = 1\,pF$ as it can be seen in Table 2.1) has been connected at the driven node. Doing so, the high parasitic capacitance remains connected to a low impedance node and has no effect in frequency nor attenuation. The output parasitic of the sensor (*200fF* as it can be seen in Table 2.1) has been the one used in the voltage divider. Moreover, cascoding has been utilised in the opamp in order to reduce Miller effect capacitance and thus reduce C_{opamp}.

As a released and an unreleased sensors have been used, different capacitances are expected due to the different permittivity coefficient of air and silicon dioxide. This mismatch may also be present in the sensor parasitic capacitance. In order to make sure that this capacitance mismatch is corrected, an off-chip driving voltage correction by means of a resistive net [17] has been implemented on the test PCB in order to tune the voltage injected at each path so that the amplitude at the inputs of the opamp without excitation of the sensor is the same.

The driving DC voltage to be used at the input of the sensor is set to have the same value that at the input of the opamp. Doing so, the voltage drop across the MEMS sensor is set to zero and no displacement of the movable plate of the accelerometer due to the electrostatic attractive force between plates [18] is produced and therefore no offset is generated.

Finally, two unity gain source followers (not shown in Figure 3.2) have been used to drive the output signals to the pads of the chip and thus reducing the output capacitive load of the opamp and boosting the frequency response of the opamp.

For simplicity, there will be assumed that both driving voltages are matched ($V_m = V_{m1} = V_{m2}$) as well as sensor capacitances and parasitics. This is an unrealistic case, but the tuning of driving voltages allows to make such simplifications as chopping signal at each input of the opamp is matched (when the sensor is not excited). Hence, it is possible to analyse the circuit in Figure 3.2:

$$V_{\text{ip}} = V_{m1} \frac{C_M}{C_M + C_p + C_{opamp}} \tag{3.2}$$

$$V_{\text{in}} = V_{m2} \frac{C_D}{C_D + C_p + C_{opamp}} \tag{3.3}$$

So that in the case without acceleration each modulating signal must make $V_{ip} = V_{\text{in}}$:

$$V_{m1} \frac{C_M}{C_M + C_p + C_{opamp}} = V_{m2} \frac{C_D}{C_D + C_p + C_{opamp}} \tag{3.4}$$

Where C_M is the unreleased sensor capacitance, C_D is the dummy capacitance and C_p is the parasitic capacitance at the output of both MEMS. With the assumption made before, the sensor capacitance C_M value is $C_M = C_D + \Delta C$, where the driving voltage tuning to match both paths has been translated into an equivalent $C_M = C_D$ without acceleration.

Then, given a gain *G* at the differential amplifier, the output voltage is:

$$V_o = G(V_{\text{ip}} - V_{\text{in}}) = V_m G \left(\frac{C_D + \Delta C}{C_D + \Delta C + C_p + C_{opamp}} - \frac{C_D}{C_D + C_p + C_{opamp}} \right) \tag{3.5}$$

As the sense capacitance is both in the numerator and the denominator, a non-linearity should be expected in this topology. However, as the dynamic range of the sensor is reduced ($\pm 5 fF$), an approximation can be made: $\Delta C \ll C_D + C_p + C_{opamp}$. Finally, equation (Eq. 3.5) is simplified in equation (Eq. 3.6):

$$V_o \approx V_m G \left(\frac{\Delta C}{C_D + C_p + C_{opamp}} \right) \tag{3.6}$$

So the sensed acceleration ΔC will generate a proportional amplitude modulation (AM).

With a single ended topology, output voltage would have had an offset component as it can be derived from equation (Eq. 3.5) that would have reduced the output maximum voltage swing; however, with a fully differential topology, differential output has no offset component and the output voltage swing is doubled.

3.3 Operational Amplifier Choice

In order to decide the topology of the opamp, some aspects and needs of the top level design should be taken into account. First of all, the opamp needs to be able to work at quite high frequencies because chopping stabilization is going to be used in order to avoid Flicker noise. Consequently PMOS transistors have been used at the input stage instead of NMOS in order to easily obtain a lower corner frequency due to the lower Flicker noise of PMOS over NMOS transistors [19]. Simulations for this technology confirmed it. Secondly, noise floor is the main concern, so white noise needs to be reduced by proper sizing of input transistors. Thirdly, a low added non-linearity can be allowed due to the open loop topology to be used. Finally, the design was carried out in a time constrained scenario.

With all this design constraints in mind, the schematic of the opamp was designed and it is shown in Figure 3.3.

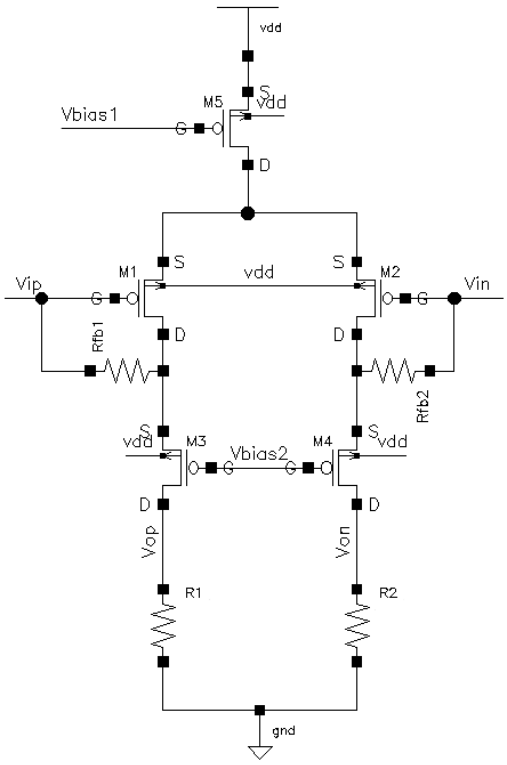

Figure 3.3: Schematic of the first design amplifier.

Resistors have been used instead of active NMOS loads as they allow an easier control of the open loop gain of the operational amplifier because of their known and low values. Doing so, the open-loop gain is much lower than the gain normally found in general purpose opamps in order to avoid output voltage saturation. Moreover, the frequency response is easily improved with a low resistance load.

A single stage opamp has been used instead of a two-stage opamp for several reasons. Firstly, having just an stage reduces design time. Secondly, it requires less current. Thirdly, single stage opamp increases unity-gain bandwidth (UGB) due to the lack of second stage and compensation, because the main purpose of compensation is to move the low frequency pole to lower frequencies by means of pole-splitting compensation while looking for stability [20]. Instead, a high UGB has been obtained by using a relatively low value resistor and by using unity gain buffers between the outputs of the opamp and the pads of the chip. Doing so, a low capacitive and resistive (compared to the channel resistance of an active load) node is present at the output of the opamp and thus boosting its frequency performance.

The biasing of the inputs has been done by using high value resistors. These resistors are connected between the inputs and the cascode nodes of the opamp. As these cascode nodes are low impedance nodes, signal gain is also reduced, so the Miller effect is

importantly reduced and the input referred resistor is also minimized. These high value resistors used are resistive fuses further detailed in coming sections.

3.4 Small signal analysis for low frequencies

From the schematic circuit of Figure 3.3, the equivalent small signal single-ended circuit has been drawn in order to obtain the DC open loop gain of the opamp.

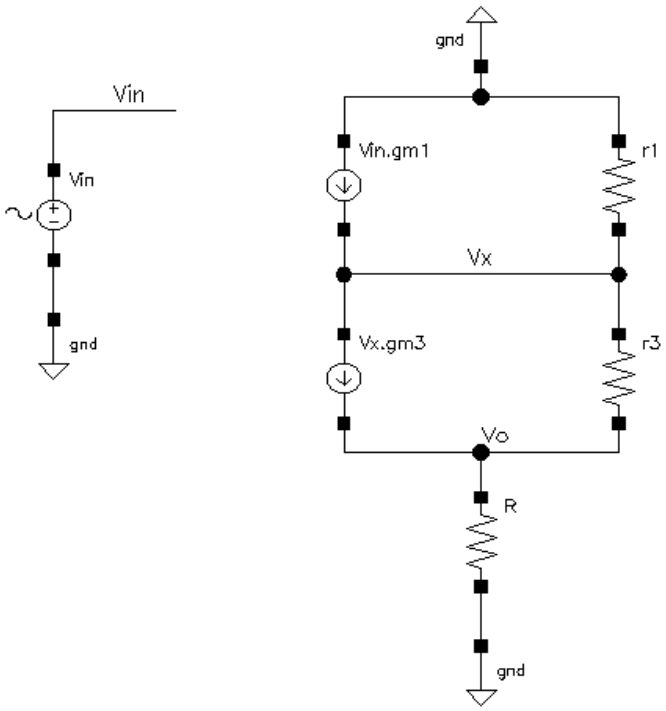

Figure 3.4: Equivalent small signal single-ended circuit from the opamp on Figure 3.3.

Where r_1 and r_3 are the channel resistances of transistors M1 and M3 and V_x is the cascode node where biasing resistor is connected (this resistor has not been added in Figure 3.4 because it has no influence in the gain at low frequencies). Finally, R corresponds to R_1=R_2

The schematic on Figure 3.4 can be redrawn for convenience as:

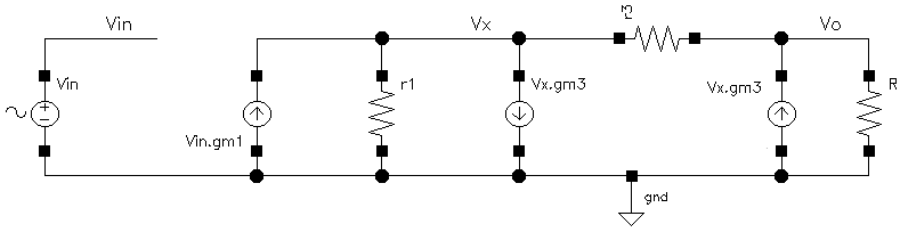

Figure 3.5: Modified small signal circuit from Figure 3.4.

Where the voltage-controlled current source of transistor M3 connected to intermediate node V_x is equivalent to a resistor of value $1/gm_3$. As this resistor is much lower than the channel resistor of transistor M1, it dominates. Moreover, as r_3, that models the channel length modulation of transistor M3, tends to be very high compared to the value of R, the equivalent circuit in Figure 3.5 can be further modified to the one shown in Figure 3.6:

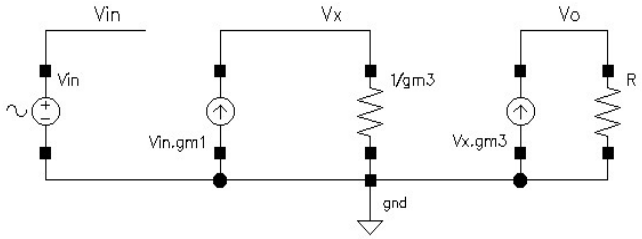

Figure 3.6: Simplified small signal circuit from Figure 3.5.

From Figure 3.6, it is possible to equate node voltages:

$$V_x \approx V_{in} \frac{gm_1}{gm_3} \tag{3.7}$$

$$V_{out} = R\, V_x\, gm_3 \tag{3.8}$$

And finally the gain:

$$G = \frac{V_{out}}{V_{in}} = R\, gm_1 \tag{3.9}$$

From equation (Eq. 3.9), the use of resistor R can be justified as it is an easy way to control the gain of the opamp.

3.5 Small signal analysis for medium to high frequencies

To make a frequency study of the opamp used, an small signal schematic with the capacitances as well as the feedback capacitor included has been drawn in Figure 3.7.

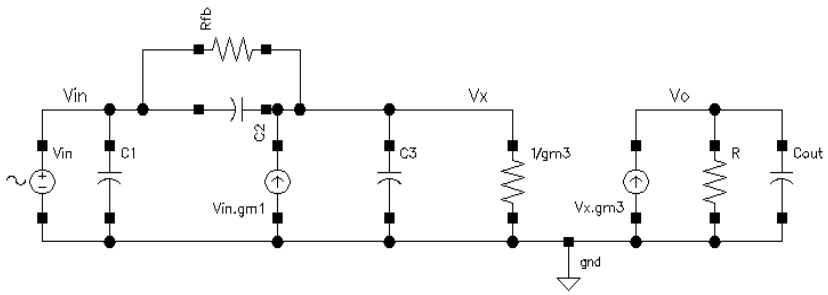

Figure 3.7: Single-ended small signal circuit of the opamp with parasitic capacitances included.

In Figure 3.7 there can be seen all the capacitances that may affect the performance of the opamp. They are detailed below.

$$C_1 = C_{gs1,2} + C_{gb1,2} \tag{3.10}$$

$$C_2 = C_{gd1,2} \tag{3.11}$$

$$C_3 = C_{db1,2} + C_{sg3,4} + C_{sb3,4} \tag{3.12}$$

$$C_{out} = C_{db3,4} + C_{dg3,4} + C_{load} \tag{3.13}$$

Where C_{load} is the input capacitance of the source followers connected at the output of the opamp and the remaining ones are the typical parasitic capacitances of MOS transistors.

The feedback resistor is included now because it is affected by the Miller effect [21]:

$$Z_{\text{in}} = \frac{Z_{fb}}{1 - A_v} \tag{3.14}$$

$$Z_{\text{out}} = \frac{Z_{fb}}{1 - \frac{1}{A_v}} \tag{3.15}$$

Where in equations (Eq. 3.14) and (Eq. 3.15) A_v is a negative value and Z_{fb} is the feedback impedance.

As the feedback resistor is connected between the input and a low impedance node, the voltage gain between these two nodes is expected to be much lower than unity, so by Miller effect C_2 is added to C_1 as well as the feedback resistor without any modification as it can be seen in Figure 3.8. At V_x node, resistor is not added because even though it is divided by a great value, it is expected to have a resistance around *1* to *10GΩ*, much higher than

$1/gm_3$. Regarding capacitance C_2, its value is negligible, so is its equivalent at node V_x.

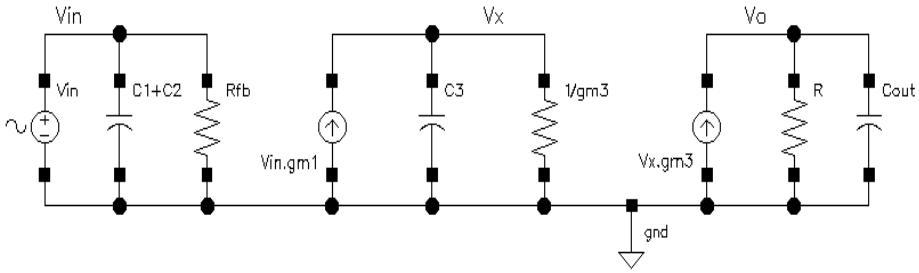

Figure 3.8: Simplified small signal circuit from Figure 3.7.

From Figure 3.8, it is possible to equate the expressions of the two poles of the system:

$$p_1 = \frac{1}{R\,C_{out}} \tag{3.16}$$

$$p_2 = \frac{gm_{3,4}}{C_3} \tag{3.17}$$

As p_2 is formed by a low value resistor $1/gm_{3,4}$ and a capacitor C_3 that is expected to be around several hundred femto Farad because it is mad of transistors parasitics (Eq. 3.12), it can be considered a very high frequency pole. The pole p_1 is composed by a relatively low-value lumped resistor and an output capacitance with an approximated value of a hundred femto Farad, consequently this pole is also expected to be a high frequency pole, but not so high as p_2. This is good because as we want to work at a chopping frequency in the range of some MegaHertz, the low frequency pole must be placed several MegaHertz above this value. However, and in order to avoid instabilities and to obtain an acceptable phase margin, p_2 will be placed above the UGB by correct design of gm_3 parameter in coming chapters.

It also must be taken into account that the inputs of this opamp are going to be connected to a capacitive net that will modify the final frequency response of the opamp. The input net can be seen in Figure 3.9:

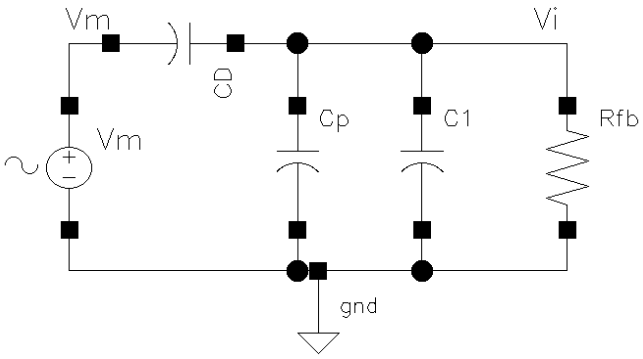

Figure 3.9: Equivalent circuit at opamp input.

Where $V_i = V_{\text{in}} = V_{ip}$, as both inputs have the same equivalent circuit. Capacitance C_2 is not taken into account because its low value compared to C_1: C_2 is a gate-to-drain parasitic capacitance, that is much lower than the gate-to-source capacitance in C_1.

In Figure 3.9 a high pass filter is easily seen that is described by equation (Eq. 3.18):

$$\frac{V_i}{V_m} = \frac{\dfrac{C_D}{C_D + C_1 + C_p} s}{s + \dfrac{1}{R_f (C_D + C_1 + C_p)}} \tag{3.18}$$

So a final band-pass filtering is going to be obtained in the overall circuit. This equation gives us a constrain to choose the feedback resistor value.

3.6 Noise considerations

The design target for this opamp has been to make the added noise from the opamp to be lower or at least to have a similar value than the Brownian-noise from the sensor in order to avoid deteriorating its performance and to keep the resolution of the system as close as the resolution limited by the sensor noise. Following such target makes the total output noise to be dominated by the sensor thermal-Brownian noise as noise is added quadratically as shown in equation (Eq. 3.19):

$$\overline{V_{n\,out}^2} = \overline{V_{n\,out\,opamp}^2} + \overline{V_{n\,out\,sensor}^2} \tag{3.19}$$

In Table 2.3, a noise value with capacitance units was obtained, but this value has to be

converted to voltage at the input of the opamp by modifying equation (Eq. 3.2) for noise purposes:

$$\frac{\overline{V_{i\,sensor}}}{\sqrt{\overline{\Delta f}}} = V_m \frac{\frac{\overline{\Delta C_{n1}}}{\sqrt{\overline{\Delta f}}}}{C_D + C_p + C_{opamp}} \tag{3.20}$$

As it can be seen in equation (Eq. 3.20), noise is inversely proportional to the MEMS capacitance without excitation C_D, its parasitic capacitance C_p and the opamp input stage parasitic capacitance C_{opamp}. From these parameters, the only one that can be controlled during the design of the readout circuit is the input pair capacitance. Hence, it will be important to size input transistors so that they do not increase too much the noise at the same time that they provide enough open-loop gain for the opamp.

However, from equation (Eq. 3.20), an issue arises: it is not possible to compute a single noise value to be used as a target for noise in optimisation stages because it depends on C_{opamp}, a value that depends on the sizing of the input stage. Consequently, an optimisation strategy that tracks variations of noise at the same time that input stage sizing varies will be needed.

3.6.1 Analysis of components noise

In order to minimise noise, it is important to know which is the noise contribution from every component of the circuit. In Figure 3.10, the schematic of the opamp can be seen where equivalent noise sources have been added to each of the components:

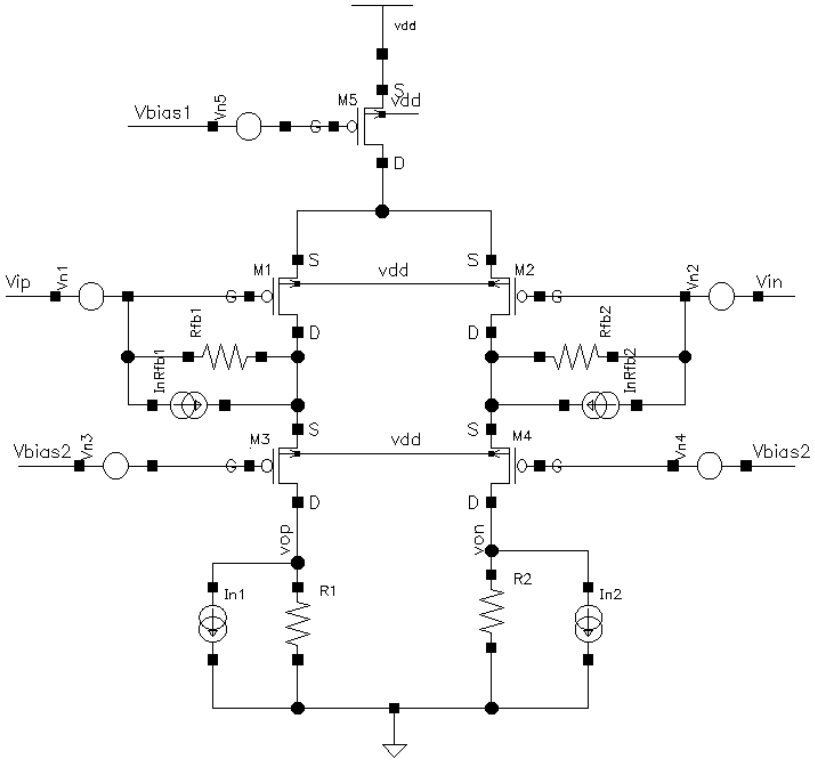

Figure 3.10: Opamp circuit with components' equivalent noise sources.

Where it can be seen that all transistors have a gate referred noise source and resistors have an equivalent noise current source.

Noise from transistor M5 is a common mode noise that will be easily removed by the fully differential topology.

As it will be shown in coming chapters, feedback resistors have been implemented using two sub-threshold MOS transistors. Doing so, the layout area compared to a lumped resistor has been drastically reduced. Seen at the input, the noise of this feedback resistor can be approximated to equation (Eq. 3.21) if all the current is assumed to flow through M1 and M2, this is, the very worst case in terms of noise:

$$\frac{\overline{V_{iRfb1,2}}}{\sqrt{\overline{\Delta f}}} = \frac{\overline{i_{nRfb1,2}}}{gm_{1,2}} \tag{3.21}$$

Where, divided by M1/M2 transconductance is further reduced.

The contribution of noise from cascode transistors is usually negligible [22] and in this case it has been confirmed because the output referred noise has been equated to be:

$$\frac{\overline{V_{o3,4}}}{\sqrt{\Delta f}} \approx gm_{3,4} R_{1,2} \overline{V_{n3,4}} \left(1 + \frac{gm_{3,4} r_{1,2}}{1 - gm_{3,4} r_{1,2}} \right) \tag{3.22}$$

And as $|1 - gm_{3,4} r_{1,2}| \gg 1$, the expression between parenthesis tends to zero, so noise from cascode transistors can be approximated to be negligible.

White noise from load resistors can be referred to the input as expressed in equation (Eq. 3.23):

$$\frac{\overline{V_{iR1,2}}}{\sqrt{\Delta f}} = \frac{i_{nR1,2}}{gm_{1,2}} \tag{3.23}$$

Finally, the noise from the input transistors is the one that should dominate the overall noise because it is directly connected at the input.

The overall noise of the differential opamp has contributions of components of each half of the opamp quadratically added, so the final input referred noise expression, that gathers equations (Eq. 3.21), (Eq. 3.23) and input transistors noise can be found in equation (Eq. 3.24):

$$\frac{\overline{V_{iopamp}}}{\sqrt{\Delta f}} \approx \sqrt{2\overline{V^2_{n1,2}} + 2\frac{\overline{i^2_{nR1,2}}}{(gm_{1,2})^2} + 2\frac{\overline{i^2_{nRfb1,2}}}{(gm_{1,2})^2}} \tag{3.24}$$

Where, for symmetry, noise from components of both branches is the same.

Noise from transistors has two main components: Flicker noise, also known as 1/f noise due to its dependency with frequency; and white noise [19]. Noise component of resistors comes mainly from white noise. From [23], noise for MOS transistors can be modelled as below:

$$\frac{\overline{V^2_{w\,MOS}}}{\Delta f} = \frac{8 k_B T}{3 gm} \tag{3.25}$$

$$\frac{\overline{V^2_{1/f\,MOS}}}{\Delta f} = \frac{K_f}{W L C'_{ox} f} \tag{3.26}$$

Where K_f is the Flicker noise constant, and it is dependent on device characteristics and biasing with a typical value of 10^{-28} C^2/m^2 [19][24] for PMOS transistors and a higher value for NMOS; k_B is the Boltzmann constant, T the room temperature, f the frequency, W and L the width and length respectively and C'_{ox} the oxide per unit area of the transistor. White noise from resistors [19] is shown in equation (Eq. 3.27):

$$\frac{\overline{i_R^2}}{\Delta f}=\frac{4k_BT}{R} \tag{3.27}$$

So finally, total input referred noise can be written using equations (Eq. 3.25) and (Eq. 3.27), and just white noise is taken into account as this is the parameter that is wanted to minimize, while Flicker noise will be removed by chopping at frequencies above the corner frequency.

$$\frac{\overline{V_{i\,opamp}}}{\sqrt{\Delta f}}=\sqrt{2\frac{8k_BT}{3\,gm_{1,2}}+2\frac{4k_BT}{R_{1,2}(gm_{1,2})^2}+2\frac{\overline{i^2_{nRfb\,1,2}}}{(gm_{1,2})^2}} \tag{3.28}$$

In order to simplify equation (Eq. 3.28) and to allow a much straightforward minimisation of total noise, noise from feedback resistors is removed from equation (Eq. 3.28) because it is divided by the transconductance of input transistors, a very large value, and hence it can be considered that its contribution to noise is small. The same is made for the noise from load resistors, as it is also divided by the resistor value:

$$\frac{\overline{V_{i\,opamp}}}{\sqrt{\Delta f}}\approx\sqrt{\frac{16k_BT}{3\,gm_{1,2}}} \tag{3.29}$$

3.6.2 Optimization of noise

At this point, an approximated expression for the input referred noise of the opamp has been derived in equation (Eq. 3.29) from a more complete equation (Eq. 3.28). Besides, equation (Eq. 3.20) allows us to compute the input referred noise from the sensor shaped with the capacitances connected at the input node. In order to minimise the noise from the opamp, a glance should be taken to both expressions. Equation (Eq. 3.20) is inversely proportional to the parasitic capacitance of the input stage of the opamp. This capacitance, denoted as C_1 in equation (Eq. 3.10) can be detailed as in equation (Eq. 3.30):

$$C_1=C_{gs\,1,2}+C_{gb\,1,2}=\frac{2}{3}W_{1,2}L_{1,2}C'_{ox}+C'_{ox}W_{1,2}L_{ov} \tag{3.30}$$

Where L_{ov} is the overlap length between gate and source. Moreover, $C_{gb1,2}=0$ because the channel works as a shield that isolates gate from bulk. So finally, expressions (Eq. 3.30) and (Eq. 3.20) can be merged in equation (Eq. 3.31):

$$\frac{\overline{V_{isensor}}}{\sqrt{\Delta f}} = V_m \frac{\frac{\overline{\Delta C_{n1}}}{\sqrt{\Delta f}}}{C_D + C_p + \frac{2}{3} W_{1,2} L_{1,2} C'_{ox} + C'_{ox} W L_{ov}} \tag{3.31}$$

Where the overlap length value is $L_{ov} = 40{,}17\,nm$ for PMOS transistors [25]. Expression (Eq. 3.31) shows that the noise seen at the input will be shaped by the parasitics at the input of the opamp similarly as the gain of the voltage divider does for signal coming from the sensor.

Similarly, equation (Eq. 3.29) can be further detailed by introducing the transconductance of input transistors:

$$\frac{\overline{V_{iopamp}}}{\sqrt{\Delta f}} \approx \sqrt{\frac{16 k_B T}{3\sqrt{2 \mu_P C'_{ox} \left(\frac{W}{L}\right)_{1,2} I_{D1,2}}}} \tag{3.32}$$

Where the transconductance used is the first order model for the strong inversion saturation region as, for simplicity in the time constrained scenario, input transistors has been designed to work in that region.

Taking a look at equations (Eq. 3.32) and (Eq. 3.31), it is straightforward to see that the only parameters that both expressions share that allows us to tune the noise is the sizing of input transistors. Hence, a sweep of width will be performed in simulations in order to find the final value. Equations derived above have been used to have a sense of what is expected to happen at the various gains and noises and to check which values should be tuned in order to perform the minimisation of noise. However, simulations will be used due to its higher precision versus the simplified models and expressions used above.

3.7 Components values and transistors sizing

Due to the time constrained scenario in which the circuit was designed, some initial simplifications where made. First of all, DC tail current flowing through the OTA was fixed to $100\mu A$ and the load resistors were fixed to $16 k\Omega$ in order to have a DC output voltage of $0{,}8\,V$, enough to keep both input and cascode transistors in strong inversion saturation while providing sufficient output voltage swing. The length of input transistors has been arbitrarily set to $L_{1,2} \equiv 1\,\mu m$ in order to make the optimisation easier and, as well, to avoid

nonlinearities in the gain thanks to a greater channel length modulation of the transistors [26].

With the values above, a sweep of input transistors width has been carried out in order to check the performance of the sensor noise and the opamp noise. In simulations, the sensor has been modelled as a capacitor of *50fF* and its noise has been modelled with a parallel capacitor with the noise value in capacitance units in Table 2.3. In Figure 3.11, white noise of input stage and sensor noise, both referred at the input of the opamp have been plotted.

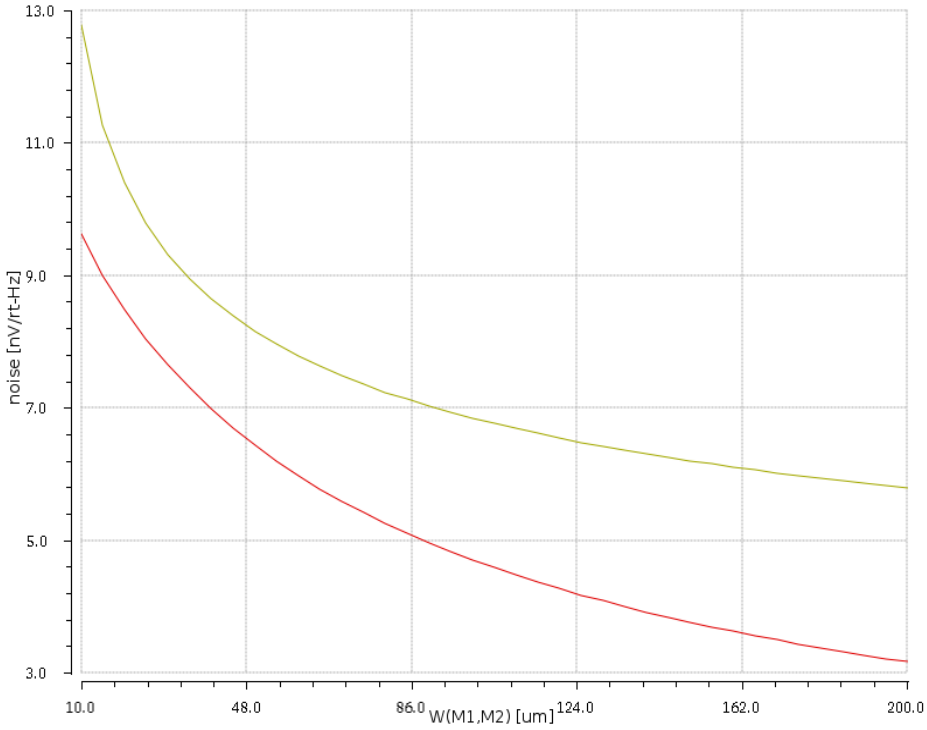

Figure 3.11: Opamp input stage white noise (yellow) and sensor noise (red) versus input pair width.

As it can be seen in Figure 3.11, opamp noise is higher than sensor noise in all the range, however, the difference is small and has its minimum of $1{,}65\,nV/\sqrt{Hz}$ in the range between $35\,\mu m$ and $40\,\mu m$. This range seems to be an acceptable range of input transistor widths in order to optimise noise as well as having an small input stage that also reduces the gain drop of the voltage divider on equation (Eq. 3.2).

Moreover, the input stage width has a control over the open-loop gain of the opamp through the transconductance of M1 and M2 as seen in equation (Eq. 3.9). Even though width values that minimise noise are quite short, they provide and opamp open-loop gain between $5{,}5\,V/V$ and $5{,}8\,V/V$ for $35\,\mu m$ and $40\,\mu m$ respectively. Even though this values are small (as they are proportional to the relatively small lumped resistor load) compared to the values found in general purpose opamps, they provide a controlled gain without

saturating the opamp.

However, the main indicator of performance for the readout circuit is the signal-to-noise ratio (SNR). This parameter can be computed using equation (Eq. 3.33):

$$SNR = 20\log\frac{V_{o\,max}}{V_{o\,TOTAL}} \tag{3.33}$$

This parameter has been simulated for an equivalent acceleration of *5fF* (the maximum allowed by the sensor), a bandwidth of *400kHz* and performing a sweep of the input pair width as seen in Figure 3.12.

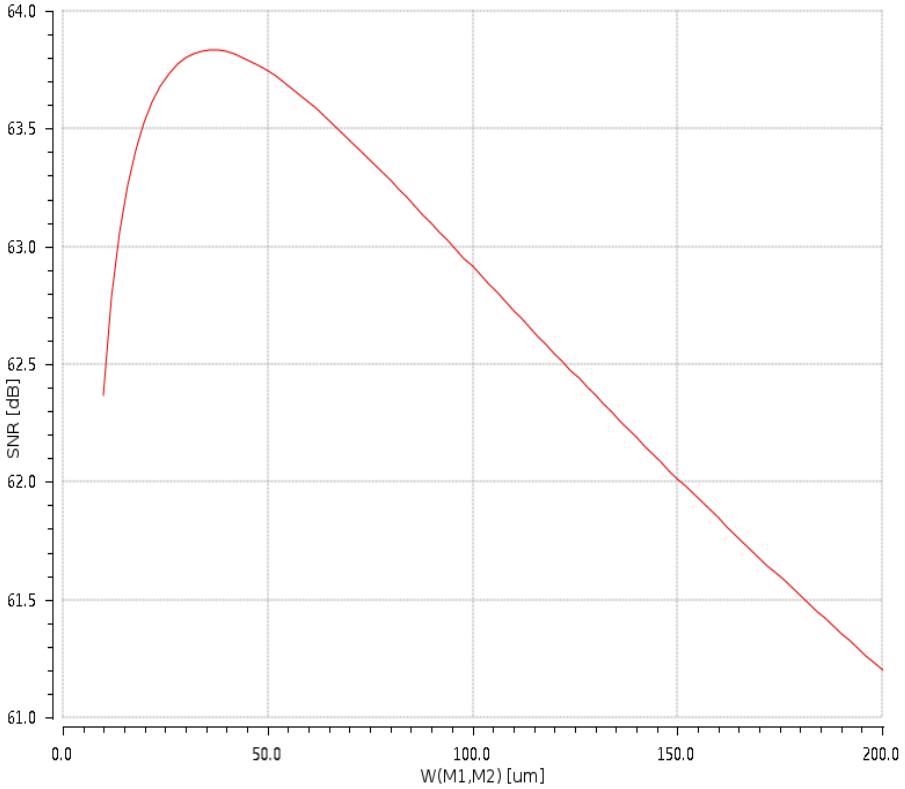

Figure 3.12: SNR of the system versus input pair width.

Where the maximum SNR is found at $36\,\mu m$. However, for simplicity in the layout stage, a width of $W_{1,2} = 40\,\mu m$ that provide a simulated $SNR(40\,\mu m) = 63{,}82\,dB$, extremely close to the maximum $SNR(36\,\mu m) = 63{,}83\,dB$.

Cascode transistors (M3 and M4) gate voltages have been fixed with a current mirror that provides a gate voltage of *0,7V*. However, this voltage can also be fixed off-chip through a potentiometer on the PCB with no worries for noise added as it would be common-mode noise. The source voltage of the cascode transistor is fixed by its gate-to-source voltage and set to $1{,}7\,V$, also setting the input DC voltage. Doing so we ensure that there is enough

source-to-drain voltage at M3, M4 and M1, M2 so that they are always working in the saturation region.

In order to obtain such M3 and M4 source voltage, $V_{gs3,4}$ must have a value of $1V$. In order to obtain this value, the sizing ratio can be calculated from equation (Eq. 3.34), that has been derived from the strong inversion saturation region channel current:

$$\left(\frac{W}{L}\right)_{3,4}=\frac{2I_{3,4}}{\mu_p C'_{ox}(V_{gs3,4}-|V_{TP}|)^2} \tag{3.34}$$

Where μ_p is the mobility of carriers (in this case, holes) close to the silicon surface, C'_{ox} is the oxide capacitance for unit area, $I_{3,4}$ is the DC current flowing through M3 and M4 and $|V_{TP}|=0,65\,V$ is the threshold voltage of PMOS transistors in this technology. Moreover, $\mu_p C'_{ox}=32\,\mu A/V^2$. With this parameters, the ratio of M3, M4 can be calculated:

$$\left(\frac{W}{L}\right)_{3,4}=25,5 \tag{3.35}$$

However, using simulations this ratio has been finally set as *200* with a width of $W_{3,4}=100\,\mu m$ and a length of $L_{3,4}=0,5\,\mu m$. This important difference is a consequence of the first order theoretical model used to calculate this ratio, that does not take into account the variation of the threshold voltage with the source-to-bulk voltage as shown in (Eq. 3.36) obtained from [24]:

$$V_{th}=V_{T0}+\gamma\left(\sqrt{2|\Phi_F|+V_{SB}}-\sqrt{2|\Phi_F|}\right) \tag{3.36}$$

Where γ is the bulk threshold parameter, Φ_F is the strong inversion surface potential, V_{SB} is the source-to-bulk voltage drop and V_{T0} is the zero bias threshold voltage.

Moreover, an even more accurate equation takes into account the channel length modulation as shown in (Eq. 3.37):

$$\frac{W}{L}=\frac{2I_3}{\mu_p C'_{ox}(V_{gs3}-|V_{TP}|)^2(1+\lambda V_{DS})} \tag{3.37}$$

Where λ is the channel length modulation parameter.

Finally, transistor M5 has been sized with $L_5=1\,\mu m$ and $W_5=100\,\mu$ in order to provide a correct mirroring from the reference current. Moreover, this length value boosts channel

resistance of the current mirror and provides an overdrive voltage of $0{,}2\,V$ as recommended in [27].

3.7.1 Input pair biasing

In order to avoid the use of a CMFB amplifier and thus reduce the power consumption of the circuit and its design complexity, high value feedback resistors have been used. However, to avoid big area lumped resistors, a resistive fuse was implemented using two sub-threshold PMOS transistors [28]. Using transistors working in the weak inversion region it is possible to obtain a much greater channel resistance. Moreover, implementing a high range variable resistor has been found to be a good strategy to correct the time delay of each path generated by the RC network at the input of the opamp, that may generate a different delay due to the mismatch of parasitic capacitance and sensor value.

As it can be seen in Figure 3.13 (a), the fuse resistor [28] consists in two serial PMOS transistors with the same dimensions and both sources connected to the voltage V_{mid}. V_{mid} voltage is the common-mode voltage of the resistor and is sensed in order to generate a voltage between V_{mid} and V_g that is constant and independent on variations of the common-mode voltage. Doing so, the biasing voltage is kept constant and so the total resistance between V_1 and V_2 because the bias point of transistors remains constant.

In order to avoid current leakage out the opamp, the bulk of the PMOS transistors in the resistor have been connected to its source.

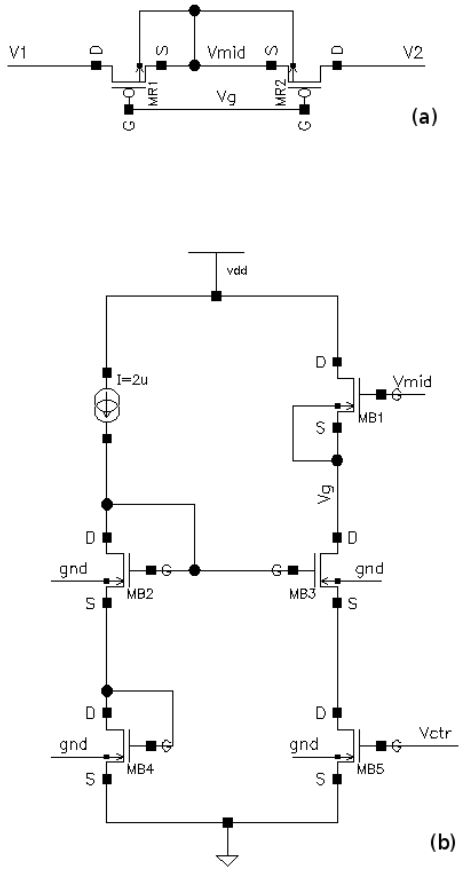

Figure 3.13: a) The resistor schematic formed by two subthreshold PMOS transistors. b) Biasing circuit of the resistor in (a).

The voltage that biases the transistors in the resistor is generated by the biasing circuit shown in Figure 3.13 (b). The basic purpose of this biasing circuit is to generate an externally tunable V_g voltage that tracks the variations of the sensed V_{mid} voltage in order to keep the voltage drop $V_{mid} - V_g$ constant.

This is obtained mainly by the right half of the circuit: gate voltage V_{ctr} of transistor MB5 is biased off-chip. This voltage tunes the gate-to-source voltage of MB5 and allows to control the working region and current of this transistor. With a voltage below its threshold voltage $|V_{tp}|$, the transistor works in the subthreshold region, following the equation (Eq. 3.38) [23]:

$$I_{DB5} \approx I_{D0}\left(\frac{W}{L}\right) e^{(q V_{GSB5} / n k_B T)} \tag{3.38}$$

Where $I_{D0} = 2 n \beta v_{th}^2 e^{\frac{-V_{T0}}{n v_{th}}}$ [19], n is the inverse of the slope of the current versus the gate-to-source voltage in the weak inversion region, q is the charge of the electron and

$v_{th}=k_B T/q$ is the thermal voltage. Increasing the V_{ctr} voltage increases the current of this transistor and thus the current of MB3 and MB1. Transistor MB3 is used as a cascode transistor that helps boosting the source voltage of MB1 and thus reducing its gate-to-source voltage in order to help keeping it below the threshold voltage. It is done by setting the gate voltage of MB3 to approximately *1,2V* using MB2 and MB4.

The tuning of current at MB5 is translated in a tuning of gate-to-source voltage at MB1, and thus a control of $V_{mid}-V_g$ voltage drop that biases the PMOS transistors that form the variable resistor.

Taking into account that $I_{DB5}=I_{DB1}$, it is possible to equate the controlled $V_{mid}-V_g$ voltage depending on V_{ctr}:

$$(V_{m2}-V_g)=\frac{n\,k_B T}{q}\ln\frac{(W/L)_1}{(W/L)_5}+V_{ctr} \tag{3.39}$$

As it can be seen, the voltage generated by the biasing circuit V_g is dependant on the sensed voltage V_{mid}, so any variation or noise in the sense voltage is directly translated to V_g and the gate-to-source voltage of the transistors in the resistor is kept constant.

With a given biasing voltage V_{ctr}, it is possible to know which is the resistance that can be obtained. In reference [29], the conductance of a PMOS transistor working in the weak inversion region for the purpose of implementing a high value resistance is shown. There, the conductance of the transistor is equated from the EKV model. In our case, and given that the resistor is going to be placed such that no DC current is going to flow through the resistor, the voltage drop across the variable resistor is expected to be zero. Consequently, and for two PMOS in series it can be assumed that:

$$R_{fb}=2\frac{v_{th}}{I_0}e^{(-V_{sg}/n|V_{tp}|)} \tag{3.40}$$

Where in this model $I_0=2n\mu_p C'_{ox}(W/L)|V_{tp}|^2 e^{(-|V_{T0}|/n|V_{tp}|)}$. Simulations performed and available in following chapters show that resistance value obtained ranges easily from hundreds of MegaOhms to hundreds of TeraOhms with a sweep of *600 mV*.

Transistors MB2, MB3, MB4 and MB5 has been sized equally with the aid of simulations in order to generate the desired voltage at the gate of MB3. For simplicity, length have been set to $L_{B2,B3,B4,B5}=1\,\mu m$. Finally $W_{B2,B3,B4,B5}=100\,\mu m$. Transistors MR1 and MR2 has been

sized $W_{R1,R2}=1\,\mu m$ and $L_{R1,R2}=100\,\mu m$ in order to boost the resistance obtained. Finally, MB5 has been sized also with the aid of simulations in order to obtain high enough resistance values: $W_{B5}=50\,\mu m$ and $L_{B5}=1\,\mu m$.

3.8 Simulations and measurements

The design presented in section 3 has been laid out and fabricated in IHP SiGe 0,25µm technology. In Figure 3.14, a confocal profiler image of a die with the already fabricated electronics and the MEMS sensors is shown.

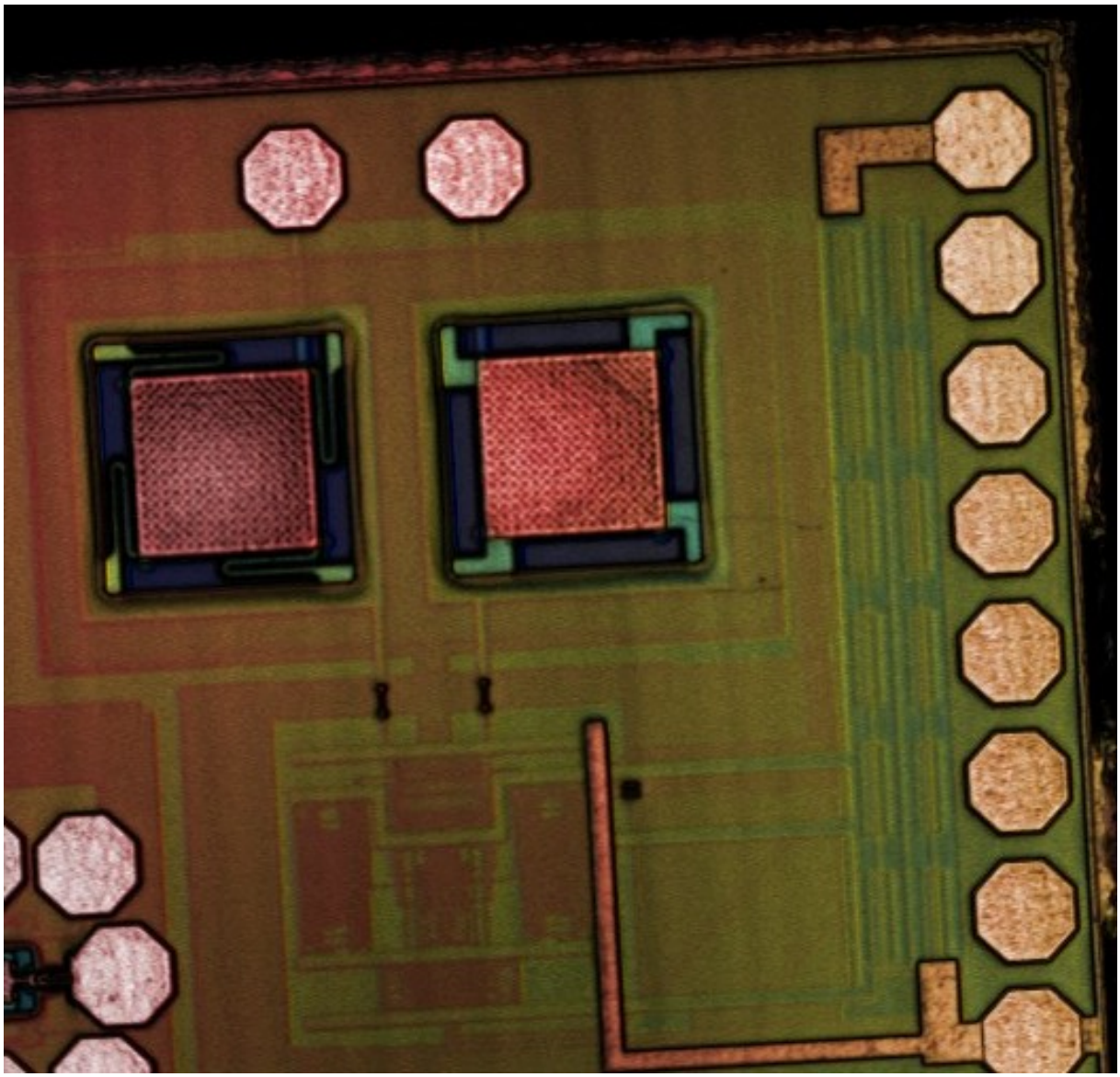

Figure 3.14: A confocal profiler image of a die [13]. On the top the MEMS sensor (left) and the unreleased sensor (right) and the circuit at the bottom.

In this section, simulations and measurements values will be shown as well as theoretically obtained values with previously derived equations in order to compare and check that derived equations meet reality.

3.8.1 Small signal and frequency performance

Equation (Eq. 3.9), repeated below for convenience, described the open-loop gain of the opamp. With the component values set in section 3.7, it is possible to compute its value:

$$G=\frac{V_{out}}{V_{in}}=R_{1,2}\,gm_{1,2}=R_{1,2}\sqrt{2\,I_{1,2}\left(\frac{W}{L}\right)_{1,2}\mu_P C'_{ox}}=5{,}72\frac{V}{V} \tag{3.41}$$

Where $R_{1,2}=16\,k\Omega$, $I_{1,2}=50\,\mu A$ is half the tail current, $(W/L)_{1,2}=(40\,\mu m/1\,\mu m)$ and $\mu_P C'_{ox}=32\,\mu A/V^2$.

Simulation gain value is really close to the obtained using equation (Eq. 3.41): $G=5{,}77\frac{V}{V}$.

Unfortunately, it has not been possible to obtain this parameter by measuring the fabricated samples because there is no access to the input nodes of the opamp because unity gain buffers have not been laid out connecting this nodes to the output in order to avoid increasing the capacitance at this node and consequently, the noise.

The simulated bandwidth of the opamp is $BW=74{,}53\,MHz$. This value is also close to the one obtained using equation's (Eq. 3.16) p_1. Expanding equation (Eq. 3.16) with equation (Eq. 3.10):

$$f_{p1}=\frac{1}{2\pi R_{1,2}\left(A_d C_{jd}+P_d C_{j-sw}+C'_{ox} W_{3,4} L_{ov}+C_{load}\right)} \tag{3.42}$$

Where L_{ov} is the overlap channel length, A_d and A_s are the areas of the drain and source junctions respectively, C_{jd} and C_{js} are the depletion capacitances of the drain and source junction respectively, P_d and P_s are the drain and source perimeter and $C_{j\text{-}sw}$ is the sidewall capacitance per unit area. C_{load} is the capacitance load added by the source follower, that is expected to be dominant as it is a source-to-gate capacitance. Hence, equation (Eq. 3.42) can be simplified and computed using the strong inversion saturation region small signal model for the input capacitance:

$$f_{p1}=\frac{1}{2\pi R_{1,2}\frac{2}{3}C'_{ox}W_{SF}L_{SF}}=59{,}7\,MHz \tag{3.43}$$

Where $L_{SF}=1\,\mu m$, $W_{SF}=100\,\mu m$ are the dimensions of the source followers. The obtained value is quite close to the one obtained by simulations. However, both values would be closer if the more complete expression (Eq. 3.42) would have been used. This value also gives a maximum value for the chopping frequency.

The high frequency pole, generated by the cascode transistor as seen in equation (Eq. 3.17), is placed at very high frequencies:

$$f_{p2}=\frac{gm_{3,4}}{C_{3,4}}\approx\frac{\sqrt{2\,I_{3,4}\mu_P C'_{ox}\frac{W_{3,4}}{L_{3,4}}}}{2\pi\left(\frac{2}{3}C'_{ox}W_{3,4}L_{3,4}\right)}=1{,}53\,GHz \tag{3.44}$$

Where $W_{3,4}=100\,\mu m$, $L_{3,4}=0{,}5\,\mu m$, $I_{3,4}=50\,\mu A$. However, in simulations, this second pole is expected to be close (but at a lower frequency) to the UGB frequency as the phase margin is close to the *45º* that means that UGB and the second pole are in the same frequency [20]. Simulations show that $UGB=230{,}4\,MHz$ with a phase margin of $PM=39{,}8^{o}$. This difference is mainly due to the approximated transconductance model and capacitance simplification. This performance, however, is slightly modified by the source followers, as they modify slightly the bandwidth of the opamp.

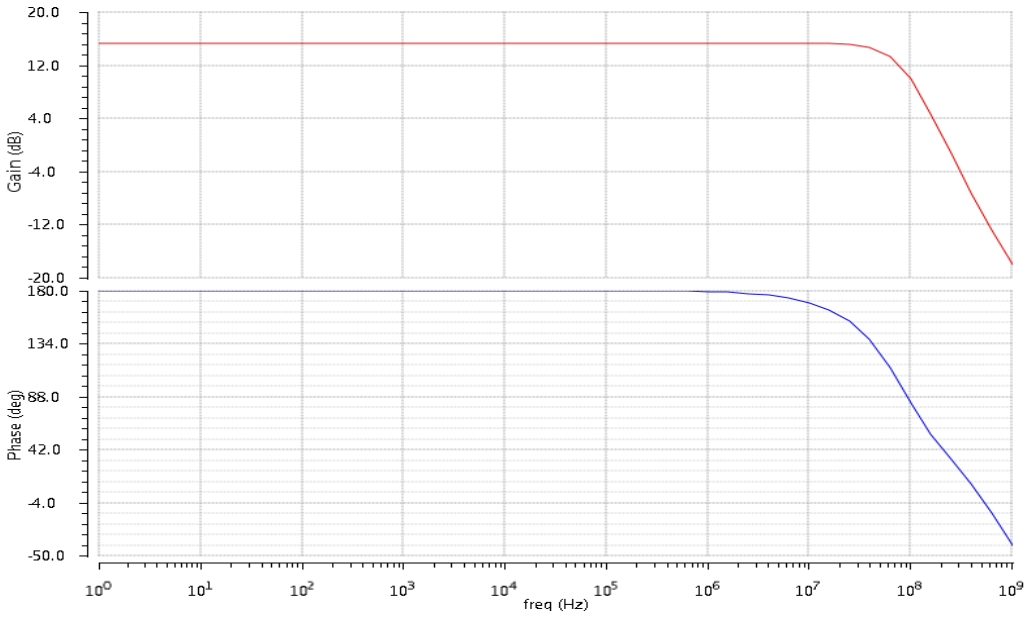

Figure 3.15: Open-loop gain and phase of the opamp.

Moreover, as shown in equation (Eq. 3.18), the input RC network works as a high-pass filter that makes the entire system to have a band-pass behaviour. From expression (Eq. 3.18), it is possible to obtain the cut-off frequency of the filter:

$$f_{HP}=\frac{1}{2\pi}\frac{1}{R_f(C_D+C_1+C_p)} \tag{3.45}$$

Approximating C_1 as the gate-to-source capacitance of input transistors, expression (Eq. 3.45) tracks correctly the cut-off frequency. This frequency depends directly on the feedback resistance that may be a concern if set to low values. Simulations show that in order to have a behaviour such the one described in the equations derived along this report, the feedback resistance should have a value above $1G\Omega$; otherwise, the approximation made when equating the low frequency pole stops being true.

3.8.2 Noise

In section 3.6.2 a detailed study of opamp noise has been carried out with the objective of setting the values for the input stage. That study focused on white noise while relying that Flicker noise would be negligible thanks to chopping stabilisation. Moreover, noise from the rest of the opamp was neglected in order to simplify the study. In Figure 3.16, these noises are now shown.

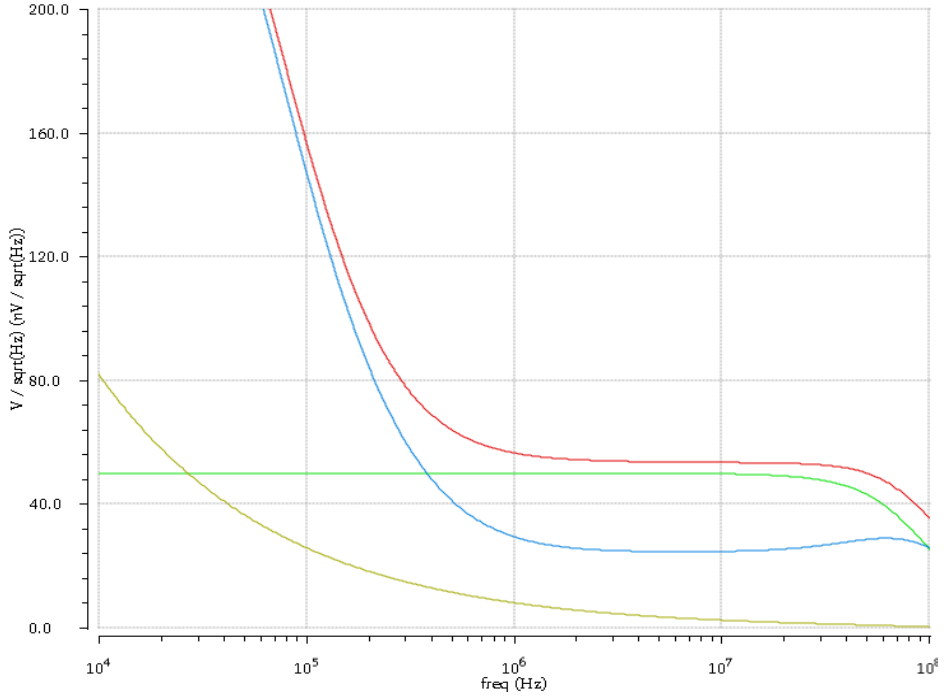

Figure 3.16: Comparison of noises. Input pair white noise (green), input pair Flicker noise (yellow), rest of transistors noise (blue) and total noise (red) with $V_{ctr}=0{,}4V$.

In Figure 3.16 it is possible to see that Flicker noise of the input pair is not a problem because it starts to be lower than thermal noise at around $27\,kHz$. However the noise of the rest of the opamp is much higher than Flicker noise and is mainly generated by the transistors in the feedback resistors. The noise coming from feedback resistors have two sources: first, white noise from the biasing transistors of this block that is somehow seen at the input of the opamp. Second, high frequency induced gate noise from transistors in the feedback resistor. This last noise is much higher with higher gate voltages in the subthreshold region [30]. However, this noise is just the remains of filtered out noise performed by the RC low pass filter seen by the equivalent noise source in series with the feedback resistor in Figure 3.9.

Total output noise generated by the opamp is approximately constant starting from 1MHz with a value of $56{,}5\,nV/\sqrt{Hz}$ until it starts to drop rapidly when approaching the cut-off frequency of the opamp, however a maximum chopping frequency bound is set at the frequency where opamp gain is reduced a 1% from the DC gain: $14{,}93\,MHz$, where the noise is $53{,}4\,nV/\sqrt{Hz}$.

The simulated noise, as well as the noise computed using derived equation (Eq. 3.32) and measurements from two available samples are compared in Table 3.1.

	Amplifier output noise @ 1 MHz $[nV/\sqrt{Hz}]$
Computed from derived equation (Eq. 3.32)	45,3
Simulated	53,4*
Measured sample #1	37,2
Measured sample #2	40,8

Table 3.1: Output referred noise from different sources.(* Minimum measured noise)

From the values in Table 3.1, it is possible to make some statements. First, that the noise from the approximated theoretical equation is really close to the measured value, validating the model and checking that the approximation made saying that most of the opamp noise comes from the input stage is true. Second, that both the theoretical expression (Eq. 3.32) and the PDK model for this technology are pessimistic with noise.

Now that opamp noise study has already been performed, it is important to compare it with the output referred noise of the sensor. This noise is shown in Figure 3.17 and has a flat response between the low and high cut-off frequencies due to the input RC high-pass filter

and the drop of gain of the opamp low frequency pole.

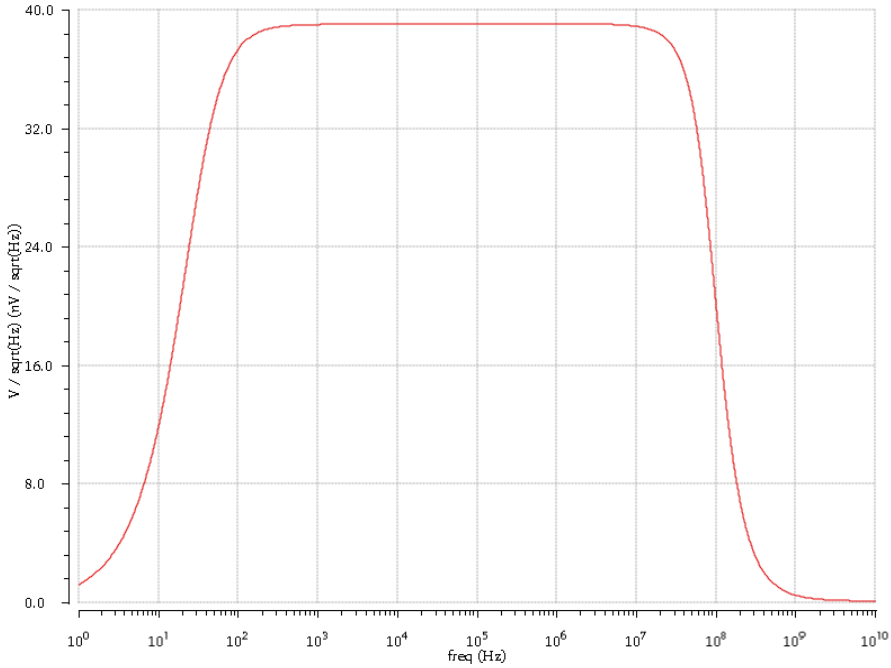

Figure 3.17: Brownian-noise of the sensor referred at the output.

Its maximum value is $39{,}0\,nV/\sqrt{Hz}$, and as it is uncorrelated with the noise from the opamp, both are quadratically added:

$$\overline{V_{o\,TOTAL}} = \sqrt{\overline{V^2_{o\,sensor}} + \overline{V^2_{o\,opamp}}} = 66{,}1\,\frac{nV}{\sqrt{Hz}} \tag{3.46}$$

In equation (Eq. 3.46), total output noise using the simulated opamp noise is calculated, however, the same figure can be computed using a mean value of the two available samples shown in Table 3.1: $\overline{V_{o\,TOTAL\,sample}} = 55{,}2\,\frac{nV}{\sqrt{Hz}}$.

In order to easily compare this figure with the noise generated by the sensor with acceleration units, sensitivity equation (Eq. 2.2), output voltage of equation (Eq. 3.6) and noise in equation (Eq. 3.46) have been merged in equation (Eq. 3.47):

$$\frac{\overline{\Delta a}}{\sqrt{\Delta f}} = \frac{\overline{V_{o\,TOTAL}}}{\sqrt{\Delta f}}\,\frac{C_1 + C_p + C_D}{V_m\,G\,S_1} = 284{,}5\,\frac{\mu g}{\sqrt{Hz}} \tag{3.47}$$

However, using measured noise $\frac{\overline{\Delta a_{measured}}}{\sqrt{\Delta f}} = 237{,}6\,\frac{\mu g}{\sqrt{Hz}}$.

Where sensitivity is found in Table 2.1 $S_1 = 0{,}013\, fF/g$, $C_1 \approx \frac{2}{3} C'_{ox} W_{1,2} L_{1,2}$, $C_p = 200\ fF$, $C_D = 50\ fF$, $V_m = 1\,V$ and $G = 5{,}77\,V/V$. Note that in equation (Eq. 3.47), driving voltage V_m has been set to *1V* for simplicity. From now on, this value will be kept in order to obtain normalised values for the driving voltage. The value obtained in expression (Eq. 3.47) can be used to compute the resolution of the system. Assuming that the value on equation (Eq. 3.47) is constant along the desired *100 Hz* signal bandwidth, the equivalent noise acceleration is found to be $2{,}85\,mg$ ($2{,}38\,mg$ with the measured noise), fixing the minimum resolution and the LSB in acceleration units. Taking into account that the range of variation of the sensor is *10 fF*, and using the sensitivity equation (Eq. 2.2), the range of measurable acceleration can be computed:

$$\Delta a_{max} = \frac{\Delta C_{1\,max}}{S_1} = 769{,}23\, g \tag{3.48}$$

That means 269906 levels with the simulated noise and 323206 with the measured noise, so an A/D of 18 and 19 bits have to be used respectively.

3.8.3 Resistor

The feedback resistor has been simulated in order to check the resistor values obtainable with a sweep of the V_{ctrl} voltage.

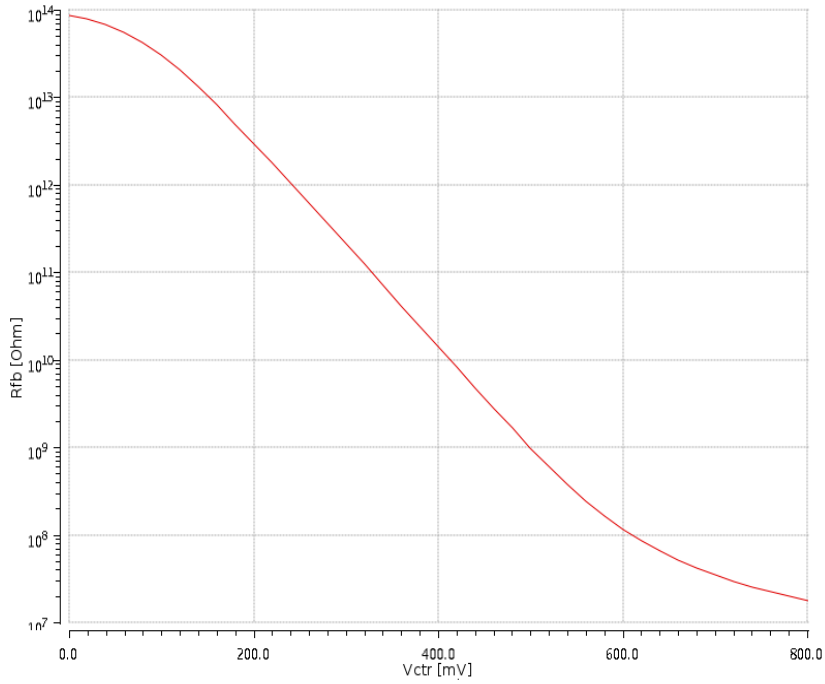

Figure 3.18: Feedback resistors value with a sweep of its control voltage V_{ctr}.

Note that in Figure 3.18 the y-axis is in logarithmic scale. In Figure 3.18 it is possible to see that a large set of resistor values can be set by tuning the control voltage V_{ctr}. However, it is important to take into account the resistor values obtainable that do not add too much induced gate noise to the circuit as explained in the previous section. For that reason, total noise generated by the resistor and its biasing circuit has been plotted in Figure 3.19.

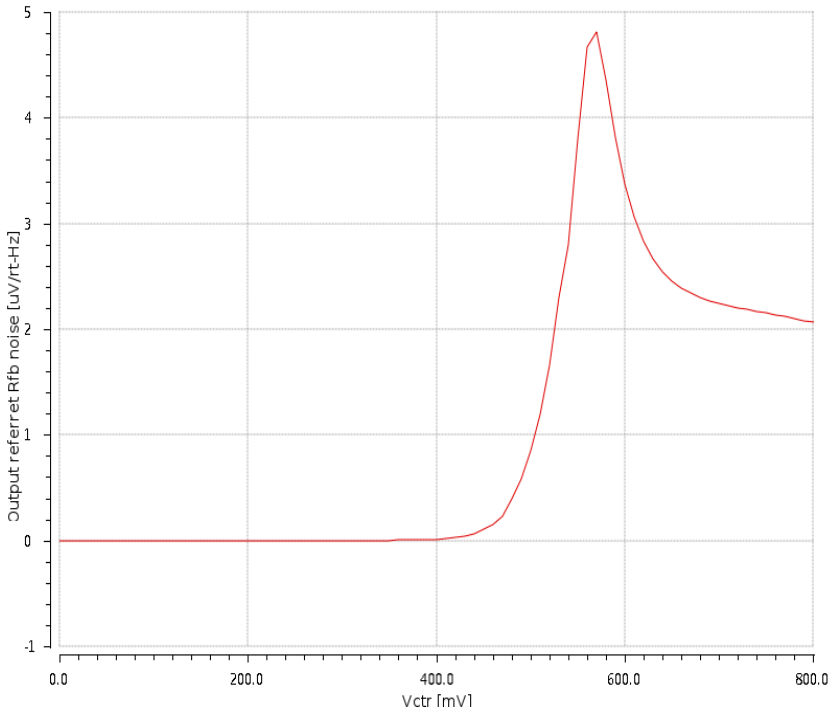

Figure 3.19: Output referred noise generated by feedback resistors depending on its control voltage.

As it can be seen, noise at *400 mV* starts to increase due to both thermal noise and induced gate noise. Hence, and in order to avoid the noise from this block, $V_{ctr} = 400\,mV$ is set as the maximum usable value, that makes the resistors to have a minimum simulated value of $R_{fb} = 14{,}1\,G\Omega$. To make sure that noise is not underestimated, al noise simulations and measurements have been performed with the aforementioned control voltage.

3.8.4 Large signal

Equation (Eq. 3.6) allow us to compute the output voltage swing that the readout circuit will have in all the range of variation of the sensor: $\Delta C_M = \pm 5\text{fF}$ from Table 2.1. Utilising (Eq. 3.6) to compute the maximum and minimum output voltage swing is shown in equation (Eq. 3.49):

$$\left(\frac{V_o}{V_m}\right)_{max} \approx G\left(\frac{\Delta C_{max}}{C_D + C_p + C_{gs1,2}}\right) = \pm 90{,}32\,\frac{mV}{V} \tag{3.49}$$

Note that output voltage is normalised with the driving voltage. Where component values used are the obtained by computing the equations derived above in the report: $G = 5{,}72\,V/V$, $\Delta C_{max} = \pm 5\text{fF}$, $C_D = 50\,fF$, $C_p = 200\,fF$, $C_{gs1,2} = (2/3)C'_{ox} W_{1,2} L_{1,2}$.

However, simulations previously showed that the gain was slightly underestimated. Besides, $C_{gs1,2}$ is overestimated in the equated model as simulations show a maximum voltage of $V_{o\,max} = \pm 106\,mV$ with a sensitivity of $S_{readout\,1} = 21{,}55\,mV/fF$. Using equation of sensor sensitivity (Eq. 2.2) it is possible to obtain the sensitivity of the overall system in acceleration units:

$$S_{readout\,1}\left[\frac{V}{g}\right] = \frac{V_{o\,max}}{\Delta a_{max}} = \frac{S_{readout\,1}\left[\frac{V}{F}\right]\Delta C_{max}}{\frac{\Delta C_{1\,max}}{S_{sensor\,1}}} = S_{readout\,1} S_{sensor\,1} = 280{,}1\,\frac{\mu V}{g} \tag{3.50}$$

Unfortunately it has not been possible to measure both the output voltage swing nor the sensitivity of the entire readout circuit because the PCB with the reference sensor is still not available at the time this report is written.

Finally the power consumption has been simulated. Current consumption is $I_{total\,1} = 363\,\mu A$ so with a supply voltage between *3V* and *0V* the total power consumption is $P_{total\,1} = 1{,}09\,mW$.

4 CLOSED-LOOP AMPLIFICATION APPROACH

4.1 Introduction

With the experience obtained during the design of the first readout circuit a second circuit has been designed in order to overcome the disadvantages found: Firstly, the measurement of the acceleration should be made independent of sensor parasitic capacitance due to these capacitance variations between the two paths of the fully differential topology and between the released and the unreleased sensor. Secondly, open-loop topology makes the design easy, but the variability of the open-loop gain with temperature and fabrication variation is not desirable in a commercial ASIC, so a closed-loop topology is a better strategy to control the gain. Thirdly, it would be interesting to be able to correct sensor and dummy sensor capacitance mismatch on-chip accurately. Finally, SNR should be improved in order to design the opamp in order to avoid worsening this figure. This means that SNR should be set by the sensor and the electronics should keep this value almost unchanged.

The optimisation of noise for this second readout circuit was performed for the first sensor (*50±5 fF*) even though the second sensor is going to be used instead (*200±20 fF*). The decision of using the second sensor was done in advanced stages of the design, so it was not feasible to optimise the noise of the circuit for the second sensor. For this reason, the simulations of this design will be performed for both sensors in order to 1) show the optimisation of noise for the first sensor and 2) to shown the final performance using the second sensor.

The full ASIC schematic is shown in Figure 4.1, where a closed-loop CTV topology has been used:

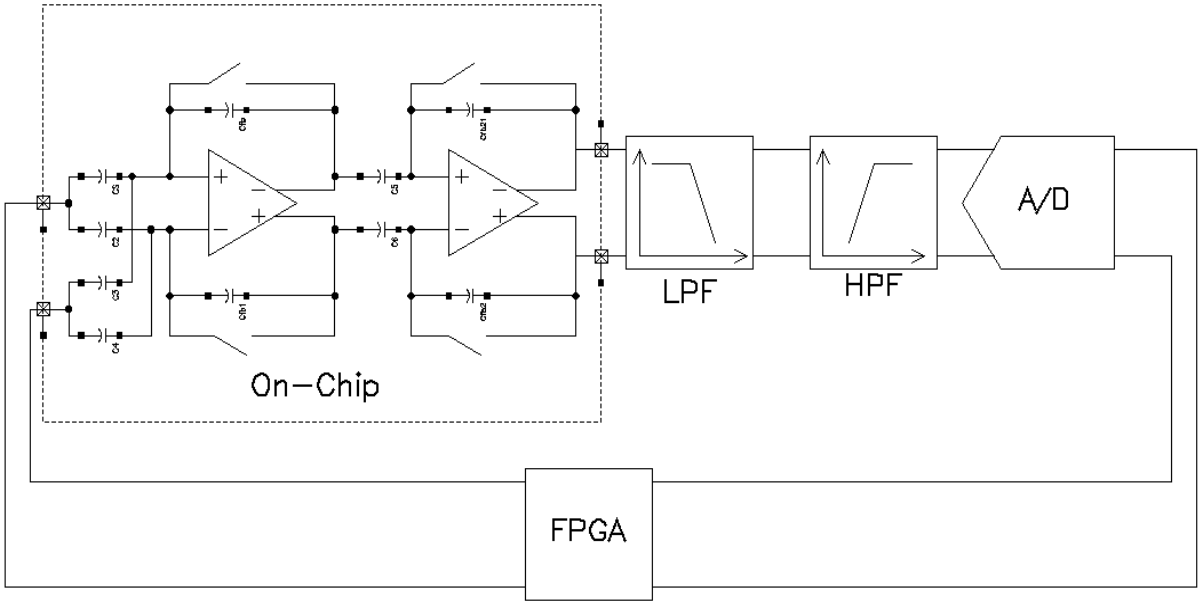

Figure 4.1: View of the system level design of the second readout circuit. Sensor parasitics have not been included.

Where it can be seen that the full schematic of the design includes the capacitive bridge and the opamp under design. Afterwards, another opamp configured as a CSA is going to be used in order to boost the signal amplitude and to overcome noise issues at the output node of the chip and keep SNR high. From now on, we will refer only to the first opamp (the left most opamp in Figure 4.1). Right after, off-chip, two high order anti-aliasing filters, one high pass and one low pass, are going to be used in order to filter out undesired frequency components and to provide a bandwidth of 400 kHz, even though the final desired signal bandwidth is *100 Hz*. Two filters instead of a band-pass notch filter are going to be used to avoid undesired phase changes. Finally, an A/D converter will be used to convert signals into the digital domain to be processed by an FPGA, that also generates the input driving signal.

In this case, the gain of the opamp is needed to be high in order to avoid non-linearities in the closed-loop topology, so a minimum targeted DC gain is between *40dB* and *60dB*.

Regarding the SNR, a tradeoff between opamp first stage transconductance and its input parasitic capacitance has been found providing the minimum achievable opamp noise by the optimization of input transistors dimensions. This optimization has been carried out for a CTV closed-loop topology with low duty cycle reset of opamp input nodes such as in [10]. Chopper stabilization and fully differential topology have also been implemented in order to reduce Flicker noise, DC offset, common-mode noise from the modulating voltage and from rails.

4.2 Top level circuit study

From the full ASIC schematic of Figure 4.1, a simplified version is shown in Figure 4.2.

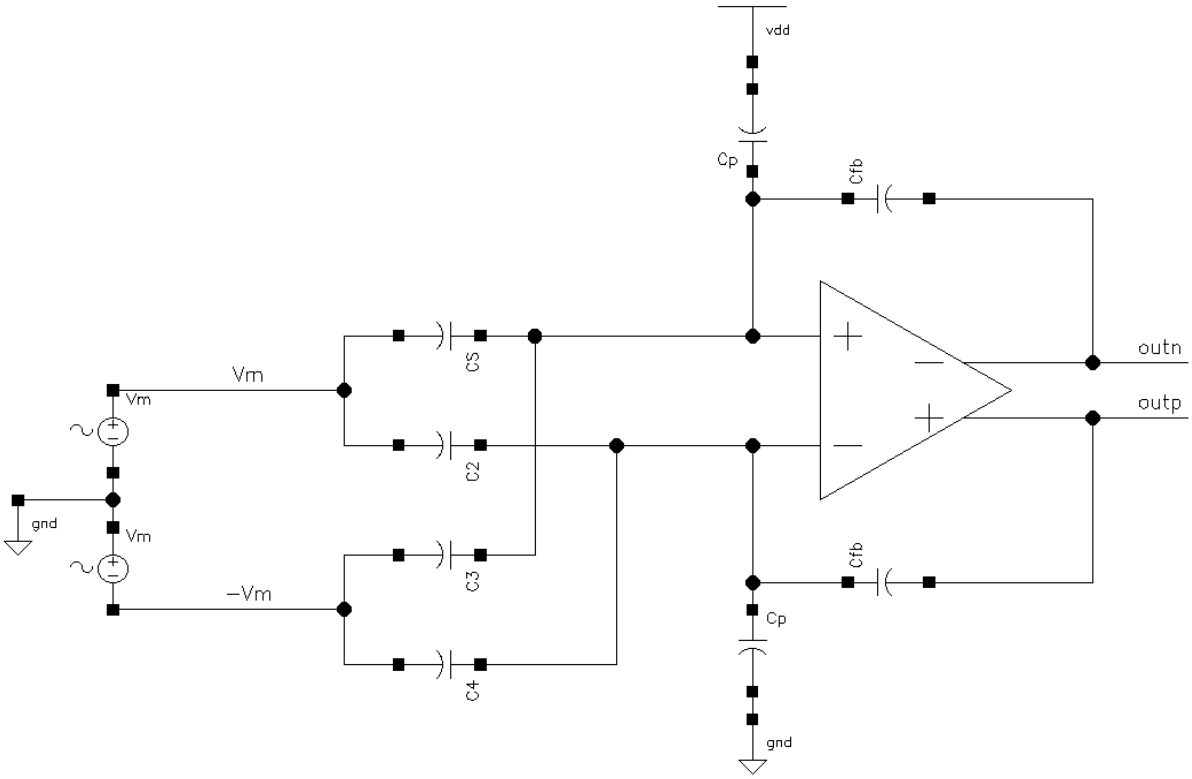

Figure 4.2: Top level schematic of the second readout circuit.

Where C_p are the output parasitics of the MEMS sensors, C_s is the sensor, C_2 is the unreleased sensor with the programmable capacitor (not shown in Figure 4.2 because it is considered to be matched with the rest of the capacitors), C_3 and C_4 are MIM capacitors matched with C_s and C_2. The closed loop topology has been done by using feedback capacitances (C_{fb}) and hence resulting in a charge sensitive amplifier (CSA): variations of sensor capacitance are translated in variations of charge that flow through the feedback capacitance. Even though this approach is similar to the CTC implementation with a transimpedance amplifier, the noise added by the resistor is avoided.

Moreover, utilising a closed loop amplifier provides a virtual ground at the inputs of the opamp. This virtual ground gives us important benefits compared to the first design. First of all, the overall gain is parasitic capacitance insensitive as these capacitances are connected between ground an a virtual ground, effectively removing them from the gain expression. Secondly, the gain of the readout circuit can be tightly controlled because it is not a direct function of the open-loop gain of the opamp but the feedback capacitance. Consequently,

temperature and doping variations are no longer a concern.

Finally, AC offset can be removed as a set of programmable capacitances is used to match MEMS sensor with the dummy sensor (C_2), compensating the different capacitance between released and unreleased sensor.

Opamp output DC voltage have been set using a CMFB amplifier. However, and in order to avoid voltage drift at input high impedance DC floating nodes, a low duty cycle is going to be used in order to reset the DC value at these nodes such as in [10]. Even though a low duty cycle reset is used, the circuit is still considered to be continuous-time because reset has no measurement purpose. The span of this report, tough, is focused in the design of the opamp circuit, so no more details about the low duty cycle are going to be explained.

With the circuit in Figure 4.2, it is possible to equate its output expression:

$$V_o^+ = V_m \frac{C_1 - C_3}{C_{fb}} \tag{4.1}$$

$$V_o^- = V_m \frac{C_S - C_2}{C_{fb}} \tag{4.2}$$

If $C_S = C_D + \Delta C$ is the MEMS sensor and $C_1 = C_2 = C_3 = C_D$ are matched, it is possible to equate the final differential output voltage:

$$V_o = V_m \frac{\Delta C}{C_{fb}} \tag{4.3}$$

Where in this case no nonlinearity due to the conditioning circuit is added. Moreover, the output voltage depends on the feedback capacitances, and as they are implemented on-chip and close to each other on layout, a precise matching is expected to be obtained.

In order to make the gain to be the higher the better, feedback capacitance has to be as small as possible. For this reason, this capacitance has been fixed to the arbitrary value of *100 fF*. This value is a tradeoff between a low value capacitance but high enough so that layout parasitics and process variations are much lower than the value set.

4.3 Operational Amplifier Choice

The schematic of the operational amplifier used is shown in Figure 4.3.

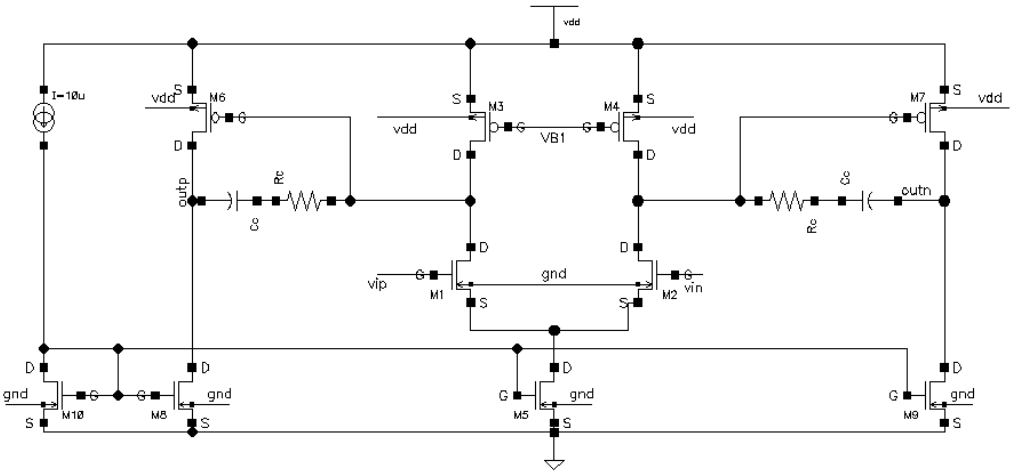

Figure 4.3: Schematic of the opamp used in the second design.

In this case an NMOS input stage has been used because, even though standalone PMOS transistors have been simulated to be less noisy in this technology for low to medium frequencies, an interesting trade-off between transistors noise and its transconductance has been derived, concluding in a better noise performance of NMOS transistors in this topology that will be explained in detail in section 4.6.1.

In this case, an active PMOS load has been used, and therefore the output voltage has to be kept within a given range in order to avoid moving this transistor out of the saturation region. This problem was not present in the previous design, where the use of a resistor allowed a degree of freedom in the output voltage swing. Due to this reason and the fact that the threshold voltage of the transistors in this technology is pretty high ($V_{TN}=0,6\,V$ and $|V_{TP}|=0,65\,V$), cascode transistors have not been used in order to be able to allow a high output voltage swing at the same time that all transistors are kept in the saturation region.

In this design, a CMFB has been used. This CMFB senses the output voltage and feeds back the variations through the bias voltage V_{B1}, that is the source-to-gate voltage of M3 and M4.

As it can be seen in Figure 4.1, driving voltage is expected to come from an FPGA, that means an square-wave driving voltage. Due to the fast edges of such signals, the opamp should have a sufficient phase margin in order to avoid instabilities and peaking at the edges. Hence the compensation in this design is an important specification. In [20] a phase margin of *60º* is said to have a peaking of *0,2dB*, and in [23] a phase margin of *65º* is proposed because it has ideally no peaking. For this reason and taking into account that some peaking can be allowed, a phase margin target of at least *60º* is set.

For this purpose, a nulling resistor compensation net has been used because it gathers the benefits of the Miller compensation with its pole-splitting in order to separate the low and high frequency poles, and the assistance of the nulling resistor, that placed in series with the capacitor provides a zero that can be used to compensate the high frequency pole and hence boost the phase margin.

Finally, a two-stage opamp has been designed in order to increase further the gain of the opamp and to improve its closed-loop operation. The second stage has been designed to be loaded with a second opamp (that will be the same design). This second stage is expected to be a CSA with an equivalent input capacitance of *100 fF*.

4.4 Small signal analysis for low frequencies

From the schematic of Figure 4.3, the equivalent small signal single-ended circuit can be drawn in order to equate the DC gain. In Figure 4.4, the final equivalent small signal circuit is derived:

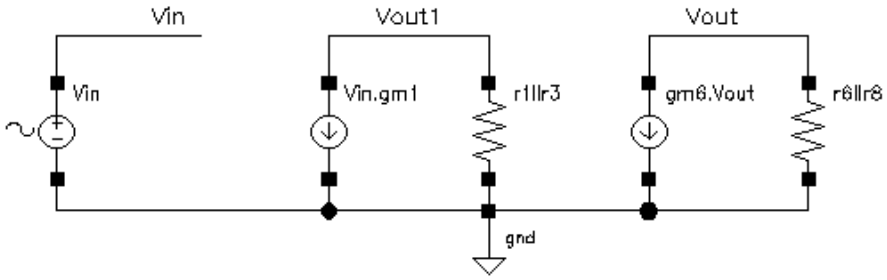

Figure 4.4: Equivalent single-ended small signal circuit of circuit in Figure 4.3.

Where the compensation has not been included as its effect starts at much higher frequencies.

The DC gain is equated in (Eq. 4.4):

$$\frac{V_o}{V_i} = gm_1 gm_6 (r_1 \| r_3)(r_6 \| r_8) \tag{4.4}$$

Where gm_1 and gm_6 are the transconductances of M1/M2 and M6/M7 respectively and r_1, r_3, r_6, r_8 are the channel resistances of M1/M2, M3/M4, M6/M7 and M8/M9.

4.5 Small signal analysis for medium to high frequencies

For an study of the frequency operation, the small signal equivalent circuit of Figure 4.4 is redrawn in Figure 4.5 but in this case, including the equivalent capacitances of the circuit. Note that the compensation net has not been included:

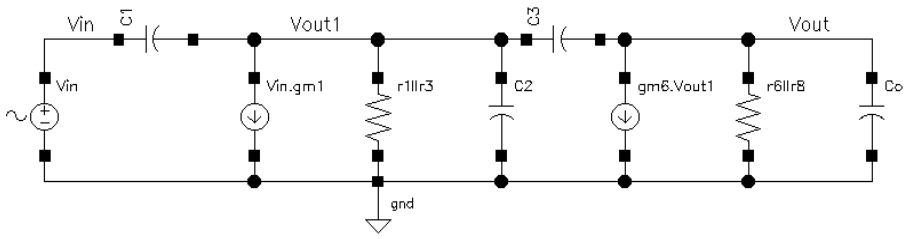

Figure 4.5: Small signal circuit from the opamp in figure 4.3 including capacitances.

Where the value of each capacitance is detailed below:

$$C_1 = C_{gd1,2} \tag{4.5}$$

$$C_2 = C_{gs6,7} + C_{gb6,7} + C_{dg3,4} + C_{db3,4} + C_{db1,2} \tag{4.6}$$

$$C_3 = C_{gd6,7} \tag{4.7}$$

$$C_o = C_{db6,7} + C_{dg8,9} + C_{db8,9} + C_{load} \tag{4.8}$$

Where MOS transistors parasitic capacitances are taken into account and the equivalent input capacitance of the second stage, that as mentioned before is $C_{load} = 100\text{fF}$.

From Figure 4.5, it is possible to make a two-pole simplification removing C_3 and C_1 capacitances. Capacitor C_3 is the gate-to-drain parasitic capacitance of transistor M6/M7, and due to the low value of this capacitance the zero that it generates is at very high frequencies. Besides, its Miller effect equivalents have a lower value than C_o and C_2. Capacitor C_1 can be split using the Miller effect into two capacitances. The equivalent capacitance at the input can be removed because is in parallel with a voltage source, and the equivalent capacitance at the output can assumed to be equal to C_1 by Miller effect in equation (Eq. 3.15). However, its value is much smaller than C_2 and hence is removed.

The final small signal circuit is shown in Figure 4.6:

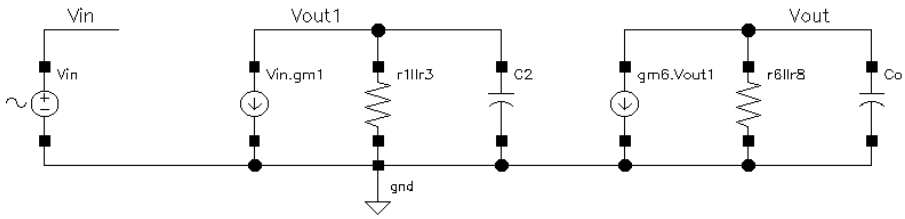

Figure 4.6: Simplified small signal circuit from Figure 4.5.

From which it is possible to derive the two poles generated:

$$p_1 = \frac{-1}{(r_1 \| r_3) C_2} \tag{4.9}$$

$$p_2 = \frac{-1}{(r_6 \| r_8) C_o} \tag{4.10}$$

In order to control the position of these two poles and to be able to tune the phase margin of the opamp when working in open-loop, a nulling resistor compensation has been used, not shown in Figure 4.5 in order to make the pole derivation more straightforward. The nulling resistor compensation, consisting in a resistor (R_c) and a capacitor (C_c) in series, is connected between V_{out1} and V_{out}. This strategy provides the benefits of pole-splitting from Miller compensation, at the same time that the right-half plane (RHP) zero generated by the Miller capacitance can be tuned.

Pole-splitting is a direct consequence of the compensation capacitance, also known as Miller capacitance. As this capacitance is connected between the input and the output of an amplifying stage, by Miller effect it can be separated into two capacitances. The equivalent input capacitance is added to C_2 and has a value proportional to the stage gain. Doing so, this capacitance is importantly increased and consequently the pole is moved to lower frequencies. The equivalent output capacitance is added to C_o with a value inversely proportional to the stage gain, so little modification is made on this pole as the gain is large. Equations that follow this input and output equivalent capacitances have already been shown in equations (Eq. 3.14) and (Eq. 3.15). The final result is a pole split that helps boosting the phase margin when the separation between poles is sufficient.

However, there is a drawback in the Miller compensation: the generation of a RHP zero. This zero increases the gain at the same time that reduce the phase [24], so it is important to get rid of it by means of moving it to frequencies where its effect is minimized or by means of converting it into a left half plane (LHP) zero, where it can be used to compensate a pole.

This conversion is possible thanks to the nulling resistor.

The expressions of the final poles and zero are shown below [24]:

$$p_1 = \frac{-1}{((r_1 \| r_3) C_c)(1 + gm_6(r_6 \| r_8))} \tag{4.11}$$

$$p_2 = \frac{-gm_6 C_c}{C_2 C_o + C_o C_c + C_2 C_c} \approx \frac{-gm_6 C_c}{C_o C_c + C_2 C_c} \tag{4.12}$$

$$z = \frac{1}{C_c(1/gm_6 - R_c)} \tag{4.13}$$

As it can be seen, and as it was advanced above, it is possible to adjust both poles position with the compensation capacitor, and the RHP zero with the compensation capacitor and resistor. Two approximations have been made in (Eq. 4.11): C_c is going to be a value relatively much higher than C_2 and C_o, as taking into account that these two capacitances can be approximated to $C_2 \approx C_{gs6}$ and $C_o \approx C_{load}$. Moreover, the zero expression is valid as far as compensation resistance is much lower than $(r_1 \| r_3)$ and $(r_6 \| r_8)$, that will be true because the channel resistance seen at the drain for strong inversion MOS transistors is expected to be several tens of kilo Ohms.

At this moment of the design, an important approach is taken: compensation capacitor is chosen in order to split the poles and put the low frequency pole so that open-loop gain at *1MHz* is within the specified range of $60\,dB > gain > 40\,dB$. Doing so it is possible to assure that at very high frequencies where chopping is going to be carried out, the open loop gain will still be kept high and will reduce the nonlinearity of the closed-loop gain due to a non-infinity open-loop gain. A low frequency pole at lower frequencies does not guarantee that the open-loop gain will be enough to avoid nonlinearities due to a low gain at that frequency, while a pole at higher frequencies makes difficult the design for the targeted phase margin because poles would be closer.

Next, and in order to reduce further the effect of the high frequency pole, the zero is moved from the RHP to the LHP and situated at its same frequency. Doing so, it is possible to reduce the phase effect of this second pole on the low frequency pole position and hence to boost the phase margin. In equation (Eq. 4.14), $p_2 = z$ is made in order to be able to isolate the component value:

$$R_c = \frac{C_o + C_2 + C_c}{C_c\, gm_6} \tag{4.14}$$

4.6 Noise considerations

The noise budget for this opamp can be obtained from the Brownian-noise generated by the sensor in Table 2.3. However, it is necessary to know this value with voltage units in order to be able to be compared with the noise generated by the components of the opamp. Hence, taking equation (Eq. 4.3), it is possible to obtain the noise budget referred at the output (because in this closed-loop topology is more comfortable as the gain is known) of the opamp. Properly modifying the equation (Eq. 4.3) for noise and normalising for modulating signal:

$$\frac{\overline{V_o}}{V_m\sqrt{\Delta f}} = \frac{\overline{\frac{\Delta C_{n2}}{\sqrt{\Delta f}}}}{C_{fb}} \tag{4.15}$$

Where $\overline{\Delta C_{n1}}/\sqrt{\Delta f} = 3{,}5 \cdot 10^{-21}\, F/\sqrt{Hz}$ and $\overline{\Delta C_{n2}}/\sqrt{\Delta f} = 13{,}4 \cdot 10^{-21}\, F/\sqrt{Hz}$ and $C_{fb} = 100\text{fF}$. With these conditions the noise budget at the output is $35\, nV/\sqrt{Hz}$ for the first sensor and $134\, nV/\sqrt{Hz}$ for the second sensor.

As previously noted, the noise of this circuit depends on the capacitance hanging at the input node of the opamp even though that in terms of signal it is a virtual ground. This behaviour can be better understood if the circuit is studied from Figure 4.7, where the total noise of the opamp is input referred with a voltage source:

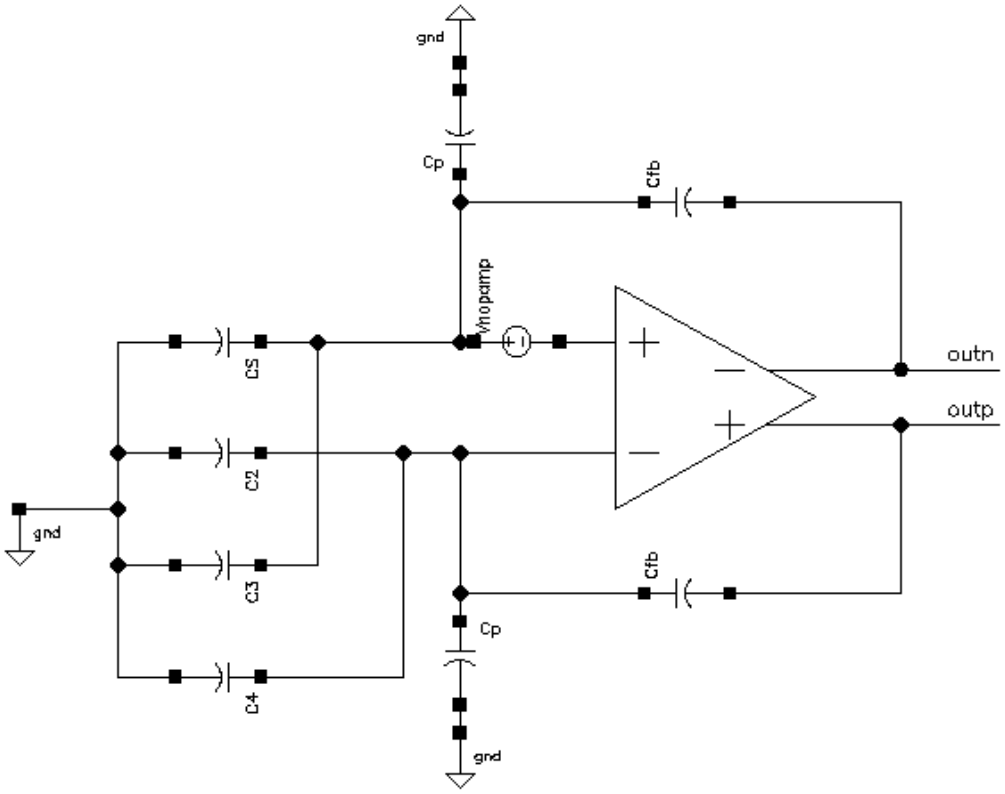

Figure 4.7: Top level schematic with an input equivalent noise source of the opamp.

Analysing the circuit it is possible to equate the output noise dependant on the input referred noise of the opamp:

$$\overline{V_o} = \overline{V_{i\,opamp}} \left(1 + \frac{C_S}{C_{fb}} + \frac{C_3}{C_{fb}} + \frac{C_p}{C_{fb}} + \frac{C_{gs1}}{C_{fb}} \right) \tag{4.16}$$

From equation (Eq. 4.16), three straightforward strategies to reduce noise come to mind easily. First of all, increasing feedback capacitance may seem that reduces directly the noise. However, this solution also reduces the overall gain of the CSA (Eq. 4.3) that at the same time reduces the noise budget as seen in equation (Eq. 4.15). The second potential solution may be reducing the $C_{gs1,2}$ capacitance by means of reducing the input stage gate area, mainly by tuning devices width. However, this solutions comes into conflict with the third solution: reducing the white noise $\overline{V_{i\,opamp}}$ by means of increasing the transconductance of input transistors.

However, this two last potential solutions can be merged to obtain an equation that can be used to find a tradeoff to find the input transistors width that minimizes noise added by the opamp.

4.6.1 Analysis of components noise

Previous to deriving the equation that optimizes transistors sizing to minimize noise, it is important to make and study of whether a PMOS or NMOS transistor pair should be used at the input stage in this specific case where noise depends on input opamp capacitance.

Traditionally, PMOS transistors have been reported to be less noisy than NMOS transistors, mainly due to the lower Flicker noise that they present. However, in this design where chopper stabilization is used, white noise is more important. As it can be seen in equation (Eq. 3.25), white noise is inversely proportional to the transconductance, a parameter that is greater in NMOS transistors. Moreover, as NMOS transistors have a greater transconductance than PMOS, they need less gate area to obtain the same transconductance, making the input gate capacitance smaller, a positive fact taking into account that it is proportional to gain.

At this point, a figure of merit has been used to compare the gain versus parasitic capacitance of NMOS and PMOS transistors taking into account the aforementioned values:

$$FoM = \frac{C_{gs}}{gm} \tag{4.17}$$

Where the input parasitic capacitance is going to be approximated as the gate-to-source capacitance of input transistors and the transconductance with the first order strong inversion model. Equation (Eq. 4.17) has been derived from equation (Eq. 4.16), getting rid of parameters that do not depend on transistor dimensions, where C_{gs} is in the numerator and gm in the denominator. Hence the lower the *FoM* the lower the noise. Traditionally, a *FoM* should be as high as possible, but in this case it has been used as an illustrative figure.

Equation (Eq. 4.17) can be detailed with the first order model of C_{gs} and *gm* mentioned before:

$$FoM = \frac{L}{3}\sqrt{L}\sqrt{\frac{2W C'_{ox}}{\mu I_D}} \tag{4.18}$$

To compare the value of the figure of merit for NMOS and PMOS, the same width, length and current must be used for both transistors so that:

$$FoM_{NMOS} = \sqrt{\frac{1}{\mu_N}} < \sqrt{\frac{1}{\mu_P}} = FoM_{PMOS} \tag{4.19}$$

As the oxide per unit area is the same for both transistors, it is possible to find that *FoM* for NMOS transistors is lower than for PMOS transistors as the mobility for electrons is better than for holes and therefore the use of NMOS transistors is justified.

The circuit in Figure 4.3 can be redrawn in order to introduce the equivalent noise sources of their components:

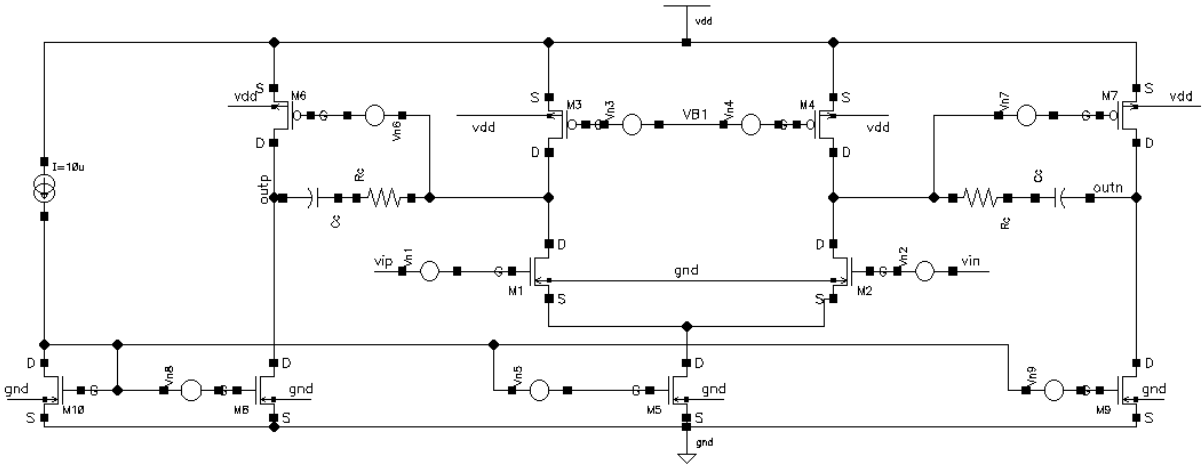

Figure 4.8: Opamp circuit with components noise.

And the equivalent input referred noise can be equated similarly as done for the first design:

$$\frac{\overline{V_{iopamp2}}^2}{\sqrt{\Delta f}} = 2\overline{V_{n1,2}}^2 + 2\overline{V_{n3,4}}^2\left(\frac{gm_{3,4}}{gm_{1,2}}\right)^2 + 2\overline{V_{n6,7}}^2\left(\frac{1}{(r_{1,2}\|r_{3,4})gm_{1,2}}\right)^2 + 2\overline{V_{n8,9}^2}\left(\frac{gm_{8,9}}{gm_{6,7}(r_{1,2}\|r_{3,4})gm_{1,2}}\right)^2 \tag{4.20}$$

Where $\overline{V_{i,j}}$ is the equivalent noise source of transistors i and j, taking into account that the circuit is symmetrical and that both transistors have an identical noise characteristic.

In equation (Eq. 4.20), noise of all transistors have been expressed referred at the input of the opamp. Transistors M1 and M2 noises are already at the input, M3 and M4 noise is first multiplied by its transconductance in order to convert the voltage noise in current noise flowing through the first stage and afterwards it is converted again into voltage by dividing by M1 and M2 transconductance. Noise from M6 and M7 have been converted to current by dividing by the impedance of the first stage output and afterwards converted to voltage as made with M3 and M4. A similar procedure has been carried out with noise from M8 and M9.

Noise from compensation resistor has not been taken into account as its noise has a path

towards the input from the zero that the compensation net generates. At this frequency, the compensation capacitance has a very low impedance and hence a path towards the input is available for compensation resistor noise. However, this noise is still not considered because the zero is placed at frequencies well above the working frequency, concretely, at the high frequency pole.

In order to simplify noise expression, a quick glance at equation (Eq. 4.20) shows that input referred noise from transistors M6, M7, M8 and M9 is divided by high values and therefore is considered to be negligible. Consequently, (Eq. 4.20) has been simplified.

$$\frac{\overline{V_{iopamp2}{}^2}}{\sqrt{\Delta f}} = 2\,\overline{V_{n1,2}{}^2} + 2\,\overline{V_{n3,4}{}^2}\left(\frac{gm_{3,4}}{gm_{1,2}}\right)^2 \tag{4.21}$$

Where transistors M1 and M2 are going to be the dominant noise sources from the opamp while transistors M3 and M4 are going to be second noise sources in importance due to the division by the high value transconductance $gm_{1,2}$. As M1 and M2 noise is going to dominate, noise optimization is focused on this input stage by making a final approximation in the total noise expression (Eq. 4.21):

$$\frac{\overline{V_{iopamp2}}}{\sqrt{\Delta f}} \approx \sqrt{2\,\overline{V^2_{n1,2}}} = \sqrt{\frac{16\,k_B T}{3\mathrm{gm}_{1,2}}} \tag{4.22}$$

Even though this expression is a very rough approximation of final noise, it is just going to be used to simplify the noise optimization as just first stage is going to be optimized.

4.6.2 Optimization of noise

The steps done until this point in order to minimize the noise of this second design have been: first, deriving the *FoM* and demonstrating in equation (Eq. 4.19) that in this specific design the overall noise will be lower if the input stage is designed with NMOS rather than PMOS transistors. Second, the total input referred noise of the opamp has been derived in equation (Eq. 4.20) and has been simplified in equation (Eq. 4.22) in order to optimize the input stage characteristics to minimize the overall noise, as input stage is the main contributor to noise in the system. Third, output noise equation (Eq. 4.16) has been derived with the opamp considered as a black box with the noise referred at the input.

At this point, equations (Eq. 4.22) and (Eq. 4.16) can be merged into equation (Eq. 4.23),

which will provide the equation that will allow us to finally optimize the input stage.

$$\overline{V_o} = \sqrt{\frac{16 k_B T}{3 gm_{1,2}}} \left(1 + \frac{C_S + C_3 + C_p + C_{gs1,2}}{C_{fb}} \right) \tag{4.23}$$

Note that as chopper stabilization is used, Flicker noise has not been taken into account but just white noise.

In order to optimize input stage to minimize noise, current has not been considered as a tunable variable because it is possible to reduce noise quite straightforwardly by increasing indefinitely the current. This approach is not an optimum approach in the design of low power ASIC's, so the remaining degree of freedom is the W/L ratio of input transistors from which the length has been arbitrarily chosen to be very small $L = 0{,}3\,\mu m$, so the only parameter left is the width. This short channel approach may not be optimum to obtain a high gain, but is does to obtain a low input capacitance.

From equation (Eq. 4.23), some observations can be made in order to make an hypothesis of what will happen when tuning the mentioned width. First of all, total output noise is inversely proportional to the square-root of the transconductance of input devices. At the same time, in the strong inversion saturation region transconductance is proportional to the square-root of transistor width and current (as seen in equation (Eq. 4.24)), and in weak inversion transconductance is directly proportional to channel current and independent (in the first order model) of the width as shown in equation (Eq. 4.25):

$$gm_{si} = \sqrt{2 \mu C'_{ox} \frac{W}{L} I_D} \tag{4.24}$$

$$gm_{wi} = \frac{I_D}{n v_{th}} \tag{4.25}$$

Hence, with a given fixed current, the transconductance of an MOS transistor in strong inversion increases while increasing the width. At a given point, the increase of width makes the transistor to enter the moderate and eventually the weak inversion region, where the transistor reaches the maximum transconductance. This can be easily seen if the all region EKV model for transconductance is used instead [31]:

$$gm \approx \frac{\kappa I_D}{v_{th}} \frac{2}{1 + \sqrt{1 + 4\,IC}} \tag{4.26}$$

Where κ is the subthreshold gate coupling coefficient, that is equivalent to *1/n*, where *n* has been considered to range from 1,2 to 2 in [19], from 1 to 1,5 in [26] and 0,67 in [31]. Besides, κ is a parameter that is not usually found in process specifications documents [32]. *IC* is the inversion coefficient, calculated as:

$$IC = \frac{I_D}{I_S} \tag{4.27}$$

That indicates the inversion region at which the transistor operates: If $IC < 0{,}1$ the transistor is in the weak inversion region, if $IC > 10$ is in the strong inversion region and moderate inversion otherwise.

I_S is the moderate inversion characteristic current [31]:

$$I_S = \frac{2\mu C'_{ox} v_{th}^2}{\kappa} \frac{W}{L} \tag{4.28}$$

Using the mathematical software GNU Octave it is possible to plot EKV transconductance in order to demonstrate that the transconductance increases while going from strong inversion to weak inversion by sweeping transistor width:

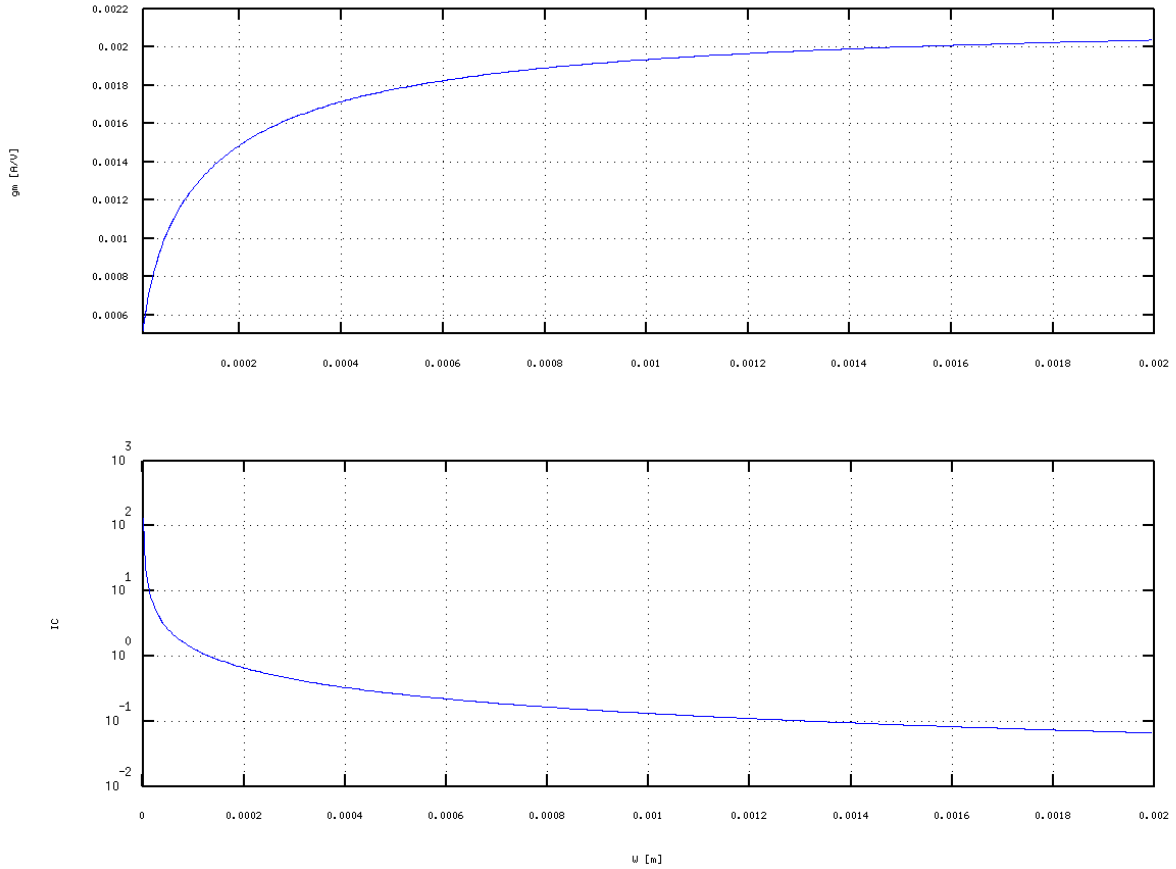

Figure 4.9 : Where the transistor works in weak inversion from approximately $W = 1{,}3\ mm$ and above, in the strong inversion from $W = 13\ \mu m$ and below and in the moderate inversion otherwise.

Where parameters values used to plot Figure 4.9 have been: $I_D = 80\ \mu A$, $1\ \mu m \leq W \leq 2\text{mm}$, $L = 0{,}3\ \mu m$, $\kappa = 0{,}7$, $v_{th} = k_B T / q$, where $q = 1{,}602 \cdot 10^{-19} C$ is the electron charge and $C'_{ox} = 95\mu\text{A}/V^2$ has been obtained by simulation of this technology.

Consequently, it may seem a good idea to make input transistors to work closer to the weak inversion region rather than in the strong inversion region, as the larger the transconductance the lower the noise. Even though, it is important to take into account

Besides, the other parameter that directly affects the noise performance is the gate-to-source capacitance of the MOS transistor:

$$C_{gs\,SI} = \frac{2}{3} W L C'_{ox} + W L_{ov} C'_{ox} \tag{4.29}$$

$$C_{gsWI} = W\, L_{ov}\, C'_{ox} \tag{4.30}$$

Where L_{ov} is the overlap length between the gate and the source, that has been found to be *41,37nm* in the NMOS model [25].

As parameter L_{ov} has a very small value, the strong inversion region has a much greater gate-to-source capacitance than the weak inversion region for a given width. However, in our approach of tuning the width in order to minimize noise, weak inversion region is achieved at very large values for width as it can be seen in Figure 4.9. Hence, the initial benefits of working in the weak inversion region in terms of transconductance are spoiled by the overlap capacitance, that may be a large value.

An intermediate working region exist though, that may offer a working point for transistors that offer the tradeoff between a relatively low parasitic capacitance and high transconductance. This intermediate region is the moderate inversion region. As this region is the transition between weak and strong inversion regions, considering weak and strong inversion region models to be adjacent results in a large error computing capacitances, and an all-region model have to be used instead [26]. Due to the complexity of such all-region models for computing the capacitance, simulations have been used in order to fine tune and optimize input transistors to minimize noise.

A first simulation to fix the width of the input pair has been performed by using the final circuit of the opamp with the characteristics that will be explained in the next section. Tail current of the first stage has been swept in a generous range at the same time that input transistors width. Output referred thermal noise for input transistors has been measured in order to obtain Figure 4.10:

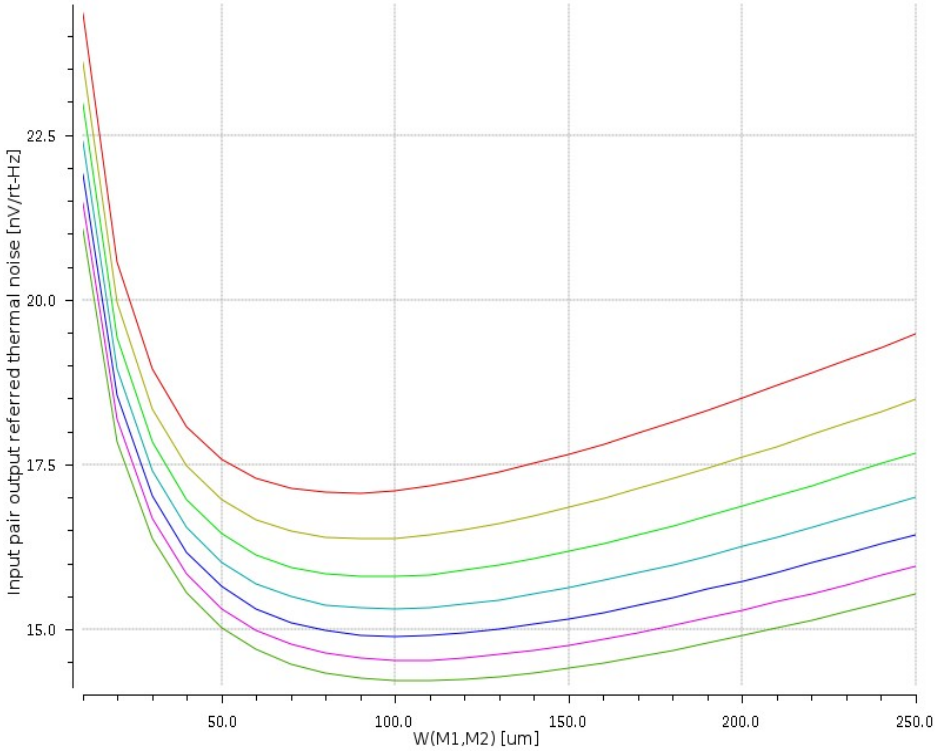

Figure 4.10: Thermal noise for different tail currents while performing a sweep of transistors width. Red is 140μA, below rest of currents with increasing steps of 10μA until light green (260μA).

In all the cases, input transistors have been found to be working in the moderate inversion region. Where input transistors width have been swept while keeping input transistors length fixed at *0,3 μm*. Such value is very close to the minimum allowed by the technology, and has been chosen because it maximises the ratio of input transistors at the same time that minimizes transistors area and consequently the parasitic capacitance. In this second design, such an small length has been used because in the closed-loop approach, open-loop nonlinearities for such small length are not expected to be an issue.

In Figure 4.10, the shape predicted before can be identified: for small widths, the transistor approaches the strong inversion operation region and hence the transconductance decreases and C_{gs} capacitance increases, boosting the input pair noise. On the other side, when the width is importantly increased, the transistors approach the weak inversion operation region at the same time that C_{gs} linearly increases due to the large width, that makes the noise increase also linearly. In the middle, input pair works in moderation region, that harvests the best of both weak and strong inversion: relatively low parasitic capacitance and a not so low transconductance.

4.7 Components values and transistors sizing

At the beginning, the optimization of noise of the input stage for this second design was carried out to be implemented with the first sensor. The second sensor was confirmed to be used in advanced design stages, so the final design could not be adjusted for it. Fortunately, the second sensor has a greater noise budget due to its larger sensitivity, so the noise contribution of the opamp is finally much lower than the noise budget even though the minimum opamp noise of the opamp for the second sensor is not finally obtained.

As the opamp and sensor noises are uncorrelated, they are added up quadratically:

$$\overline{V_o} = \sqrt{V^2_{sensor} + V^2_{AO}} \tag{4.31}$$

But in order to add a bound to help optimize not just the width but also the tail current of the input stage, a good design strategy is to limit the amount of added noise that the design can afford and that is added by the opamp. At the beginning of section 4.6 the noise budget was computed. This value is wanted to be increased just a given percent (denoted by *p*) by the opamp noise, setting the limit in equation (Eq. 4.32):

$$\overline{V_o} \leq \overline{V_{sensor}} \left(1 + \frac{p[\%]}{100\%} \right) \tag{4.32}$$

Hence, merging equations (Eq. 4.31) and (Eq. 4.32), the noise allowed at the output due to the opamp can be computed:

$$\overline{V_{o\,AO}} \leq \sqrt{\left[\left(1 + \frac{p[\%]}{100\%} \right)^2 - 1 \right] \overline{V^2_{sensor}}} \tag{4.33}$$

Now, output referred white noise of the input stage of the opamp is limited to increase just a *10%* the calculated total output noise of the sensor, that means a total output noise of $38{,}5\,nV/\sqrt{Hz}$ for the first sensor. Doing so, and using equation (Eq. 4.33), opamp output referred noise is limited to $16{,}0\,nV/\sqrt{Hz}$. Figure 4.10 in the previous section shows the optimization sweep of tail current and input transistors width, where it can be seen that using a tail current of $I_{tail} = 200\,\mu A$ (light blue line) and a width of $W_{1,2} = 90\,\mu A$ input stage white noise is minimised so that its final output value is below the target: $15{,}8\,nV/\sqrt{Hz}$. Moreover, these parameters make input transistors to work in the moderate inversion region. It is important to take into account that with this strategy, white noise has been minimised

until meeting the specification set by choosing a proper current and transistors width. However, this minimisation has not taken into account Flicker noise, that might have increased as it is inversely proportional to transistors width and current. In order to get rid of 1/f noise, chopping at higher frequencies is proposed in order to work below the noise corner and in a frequency where Flicker noise impact is further minimised.

Transistors M3 and M4 have been sized with $W_{3,4}=8\,\mu m$ and $L_{3,4}=1\,\mu m$. With this configuration, and half the tail current, its overdrive voltage is around *0,88 V*, that provide a wide range of voltage to avoid the CMFB amplifier to move this transistor out of the strong inversion region. Moreover, transistors lengths have been set to *1 μm* in order to have a great channel resistance, as the opamp open-loop gain is proportional to it as it can be seen in equation (Eq. 4.4). Channel resistance of an MOS transistor is shown in equation (Eq. 4.34) [23]:

$$r_{DS}=\frac{1}{\lambda I_D} \tag{4.34}$$

Where *λ* is the channel length modulation parameter [20], that at the same time is inversely proportional to the length [23], so finally, channel resistance is proportional to transistor length.

Transistors M6 and M7 have been sized width $W_{6,7}=40\mu\mathrm{m}$ and $L_{6,7}=0{,}5\,\mu m$. The bounds used to set this values have been: first, the overdrive voltage has been set to *0,2 V* as recommended in [27]; second, these transistors V_{sg} are used to set the biasing voltage at the output of the first stage so that the voltage swing is enough in order to keep both M1 and M2 in the moderate region and M3 and M4 in the strong inversion regions along time; and third, current flowing through transistors M6 and M7 set the slew-rate (SR) of the output stage.

Hence, taking into account the SR equation in (Eq. 4.35):

$$SR=\frac{I_{6,7}}{C_o} \tag{4.35}$$

Where C_o was derived in equation (Eq. 4.8) and that can be approximated to $C_{load}=100\mathrm{fF}$. As chopping frequency used will range from *1MHz* to *10MHz* approximately and an square wave will be used, it is important to have enough SR to avoid slow edges. An arbitrary bound is set so that the output rising edge at *10MHz* is limited to the *10%* of half the period. This

means a rising edge of *5ns*. Considering for simplicity that the output voltage can swing up to the supply voltage of *2,5V*, this means a SR rate of *500 V/µs* from the definition of SR [23]. Consequently, with equation (Eq. 4.35) current of this second stage is calculated to be $I_{6,7,8,9}=50\mu A$.

Using this current for the second stage it is possible to calculate the transistor ratio in order to obtain a $V_{sg\,6,7}=0,2\,V$ with equation (Eq. 4.36):

$$\frac{W}{L}=\frac{2\,I_{6,7}}{\mu_p C'_{ox}}\frac{1}{(V_{sg\,6,7}-|V_{tp}|)^2}=78,1\approx 80 \tag{4.36}$$

Where equation (Eq. 4.36) result has been rounded in order to easily lay out M6 and M7 transistors.

With these parameters, transistors transconductance is calculated with the strong inversion equation:

$$gm_{6,7}=\sqrt{2\mu_p C'_{ox}\frac{W}{L}\,I_{6,7}}=505,1\,\mu A/V \tag{4.37}$$

That is a quite high value that will boost the open-loop gain in equation (Eq. 4.4) and reduce the compensation resistor value needed in equation (Eq. 4.14). Finally, the DC voltage that transistors M6 and M7 set at the output of the first stage can be calculated with equation (Eq. 4.38), that is the drain current where V_{sg} has been isolated from drain current expression:

$$V_{dd}-V_{sg\,6,7}=\sqrt{\frac{2\,I_{6,7}}{\mu_p C'_{ox}}\frac{L}{W}}+|V_{tp}|=1,65\,V \tag{4.38}$$

Finally, transistors M5, M8 and M9 have been sized so that they provide the target current at each branch of the opamp from a current mirror of *10 µA* coming from a bandgap reference circuit. All these transistors have a length set to 2µm in order to boost its drain resistance and improve its performance as current sources. Besides, this length value provide an overdrive voltage of *0,2V* for all transistors, that have been sized as $W_5=200\,\mu m$ and $W_{8,9}=50\,\mu m$.

4.7.1 Compensation net

As explained in previous sections, compensation net has been designed in order to make the

opamp to have an open-loop gain within the specifications gain range. In order to do so with equations (Eq. 4.11) and (Eq. 4.14), channel resistances of various transistors should be computed. However, these resistances depend on the channel length modulation *λ*, that is proportional to the variations of the depletion layer width and hence it is difficult to compute and simulations are needed [20]. Hence, a different strategy has been used consisting in a sweep of values for the compensation capacitance without the compensation resistor. Once a value for the compensation capacitance has been obtained, a compensation resistor value has been calculated with equation (Eq. 4.14). Afterwards, fine tune of both resistor and capacitor values have been performed using simulations until phase margin is found to be greater than *60º* for various corners and temperatures among Monte Carlo simulations.

Finally, the values set for the compensation net have been:

$$C_c = 2{,}7\ pF \tag{4.39}$$

$$R_c = 2{,}7\,k\Omega \tag{4.40}$$

4.8 Simulations

The design presented in section 4 has been laid out in IHP SiGe 0,25μm technology and has been recently taped out. As explained previously, the design and optimisation of this second design was carried out to fit the first *50 fF* sensor because the design was at advanced stages when the second sensor was decided to be used. Even though, in the simulation results both sensors will be used in order to show that, the design is correctly optimised to minimise first sensor noise but that the second sensor has an acceptable performance with the current design.

As both sensors will share the same electronics in the next simulations, the power consumption of both cases will be the same. Current consumption is $I_{total2} = 450\,\mu A$, so with a supply voltage between *2,5V* and *0V* the total power consumption is $P_{total2} = 1{,}12\,mW$.

4.8.1 Small signal and frequency performance

Open-loop DC gain of the opamp was equated in (Eq. 4.4), where each parameter can be further detailed using the EKV model for transconductances (Eq. 4.26) and a simple first

order model for channel resistances (Eq. 4.34).

$$\frac{V_o}{V_i} = gm_{1,2}\, gm_{6,7} (r_{1,2} \| r_{3,4})(r_{6,7} \| r_{8,9}) = \\ = \frac{\left(\frac{2\kappa}{v_{th}}\right)^2}{\left(1+\sqrt{1+4\,IC_{1,2}}\right)\left(1+\sqrt{1+4\,IC_{6,7}}\right) I_{D3,4}\left(\frac{\lambda_{3,4}}{I_{D1,2}} + \frac{\lambda_{1,2}}{I_{D3,4}}\right) I_{D8,9}\left(\frac{\lambda_{8,9}}{I_{D6,7}} + \frac{\lambda_{6,7}}{I_{D8,9}}\right)} \tag{4.41}$$

However, this value is difficult to compute because, as explained in previous sections, the channel length modulation (λ) is a parameter that depends on the effective channel of the transistor and the variations of the depletion layer [20]. Moreover, expression (Eq. 4.41) depends on different lengths values (and for both PMOS and NMOS transistors) in which there is also a short channel length. In an accurate analysis, different lengths mean different channel length modulation, so expression (Eq. 4.41) is difficult to obtain manually as lots of simulations must be done in order to obtain all λ values. For this reason, the design has been designed aided by the CAD tool in order to avoid going into too many details and focus on the gain of each stage and the final total gain. For this reason, no theoretical gain figure has been computed, even though the equation has helped in the design flow. The same will be applied when computing the poles and zero frequencies.

The simulated open-loop DC gain of the opamp is $G_{DC} = 72{,}24\,dB$ with a $-3\,dB$ bandwidth of $BW = f_{p1} = 30{,}25\,kHz$. The product of these two values is not exactly the unity-gain bandwidth simulated value of $UGB = 211{,}49\,MHz$ because as it can be seen, the frequency response of the opamp is not exactly a single-pole system, as a pole-zero pair near the UGB is visible in Figure 4.11.

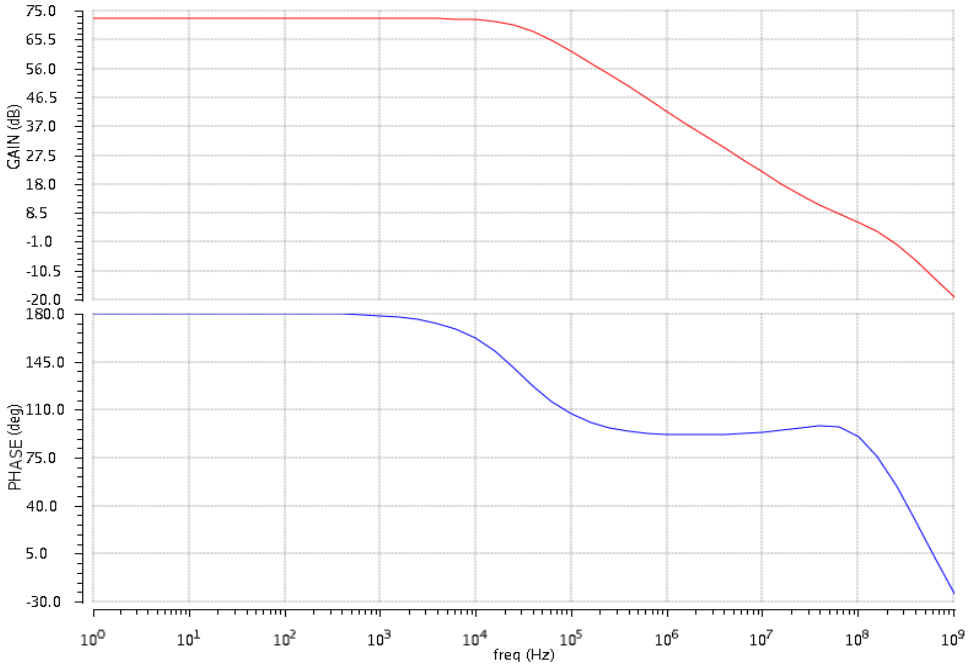

Figure 4.11: Opamp open loop gain and phase.

This pole-zero pair is the result of tuning the nulling resistor from the RC compensation net in order to place the LHP zero at a frequency very close to the high frequency pole as predicted by equation (Eq. 4.14). In this case, the zero has been placed at slightly lower frequencies than the second pole. Doing so, an small increase in phase takes place until the second pole and higher frequency poles reduce rapidly both phase and gain. This small bump in phase allows the increase of the phase margin by compensating the effect of the high frequency pole. The simulated phase margin is $PM = 63{,}16^{o}$, that meets the criterion set in section 4.3. Moreover, the frequency range where open-loop gain of the opamp is within specifications is between $f_{G=60\,dB} = 123{,}03\,kHz$ and $f_{G=40\,dB} = 1{,}27\,MHz$. However, if noise allows it, chopping can be done at lower frequencies as a gain higher than the specifications is not a problem.

4.8.2 Noise

First sensor (50 fF ± 5 fF)

In section 4.7, input pair width and tail current was set in order to meet noise budget for the opamp, however, this minimisation was done only for white noise relying it would be dominant. Flicker noise should also be taken into account as it fixes the minimum frequency at which chopping can be done. In Figure 4.12, white noise and Flicker noise have been plotted referred at the output in order to check which is the corner frequency of noise.

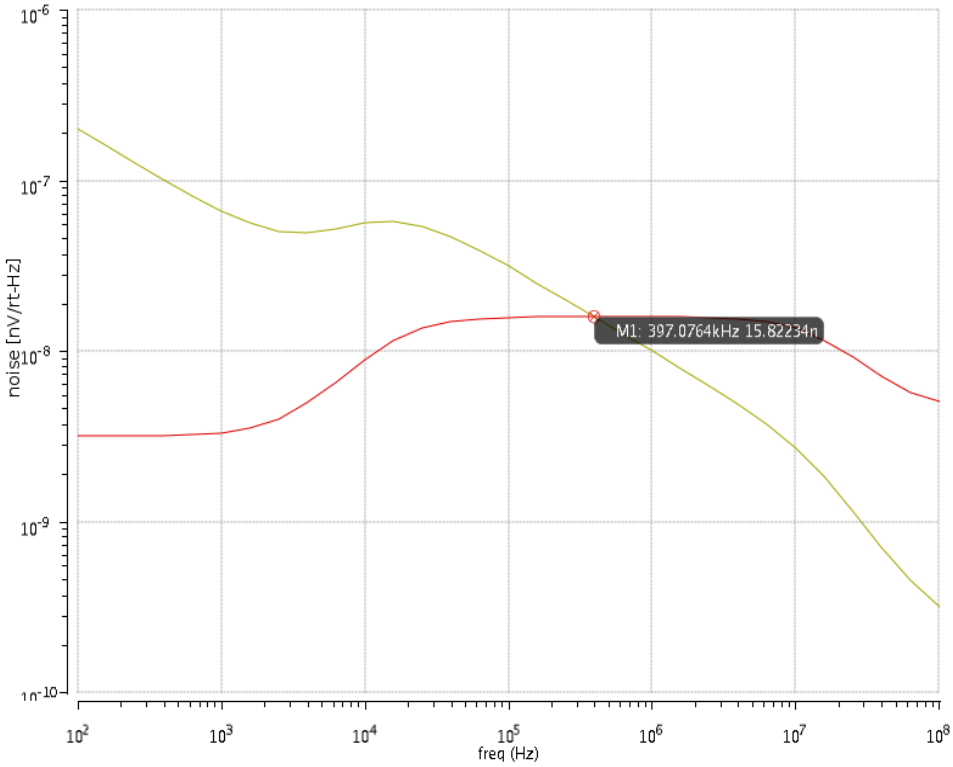

Figure 4.12: Input pair white noise (red) and Flicker noise (yellow).

Where a hump can be seen in both noises due to the band-pass filtering produced by the circuit. Noise corner frequency is found at $f_{corner} = 397{,}08\,kHz$. Compared to the previous design, this corner frequency is found one order of magnitude above due to the higher Flicker noise of NMOS transistors used in this second design.

However, once the circuit gets rid of Flicker noise of the input pair, the rest of the opamp also contributes to the output noise even thought the first stage is the dominant contributor of this block. In Figure 4.13, noise contributors have been plotted separately:

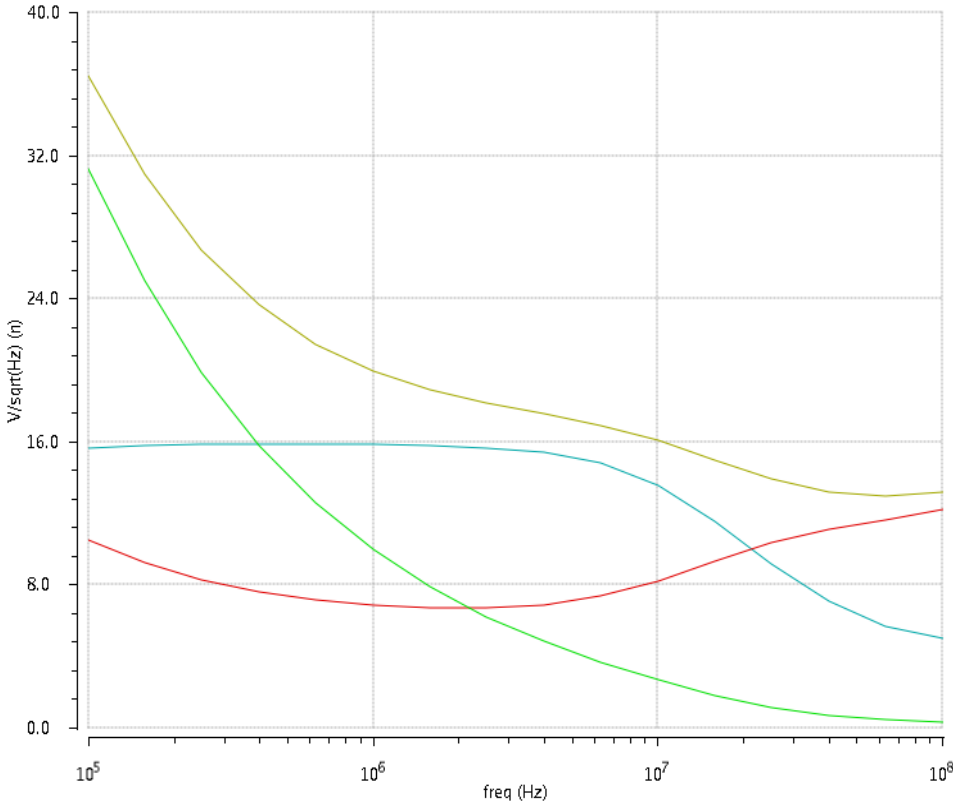

Figure 4.13: Comparison of noise. Input pair white noise (light blue), input pair Flicker noise (green), rest of transistors noise (red) and total noise (yellow).

Where it can be seen that at frequencies above the corner frequency thermal noise from input stage is the dominant (validating approximation in noise equation (Eq. 4.22)), followed by Flicker noise until it is reduced below the noise from the rest of the opamp. With this noise performance, chopping frequency range set by specified gain is updated adding as a lower bound the corner frequency of input pair. Within this range, output referred noise from the opamp is $\overline{V_{o\ opamp2}(397{,}08\,kHz)} = 23{,}16\,nV/\sqrt{Hz}$ and $\overline{V_{o\ opamp2}(1{,}27\,MHz)} = 18{,}67\,nV/\sqrt{Hz}$.

In equation (Eq. 4.23), repeated below for convenience, an approximated equation for output opamp noise was obtained that approximated the total output noise of the opamp to be just white noise due to the input stage shaped with some capacitances.

$$\overline{V_o} = \sqrt{\frac{16\,k_B T}{3\,gm_{1,2}}}\left(1 + \frac{C_S + C_3 + C_p + C_{gs1,2}}{C_{fb}}\right) \tag{4.42}$$

Where the transconductance can be further detailed using EKV model equation (Eq. 4.26) and gate-to-source capacitance of equation (Eq. 4.29) in strong inversion as a worst case approximation because the input pair works in moderate inversion.

Computing derived equation (Eq. 4.42) an output referred opamp noise of $\overline{V_{o\ opamp}} = 18{,}10\,nV/\sqrt{Hz}$ is obtained, a value higher than the simulated $15{,}8\,nV/\sqrt{Hz}$ white noise in section 4.7. This difference is mainly due to the strong inversion approximation of capacitance, however in this case this "worst case" approximation makes the computed white noise to be closer to the total output noise.

Sensor noise seen at the output is shown in Figure 4.14.

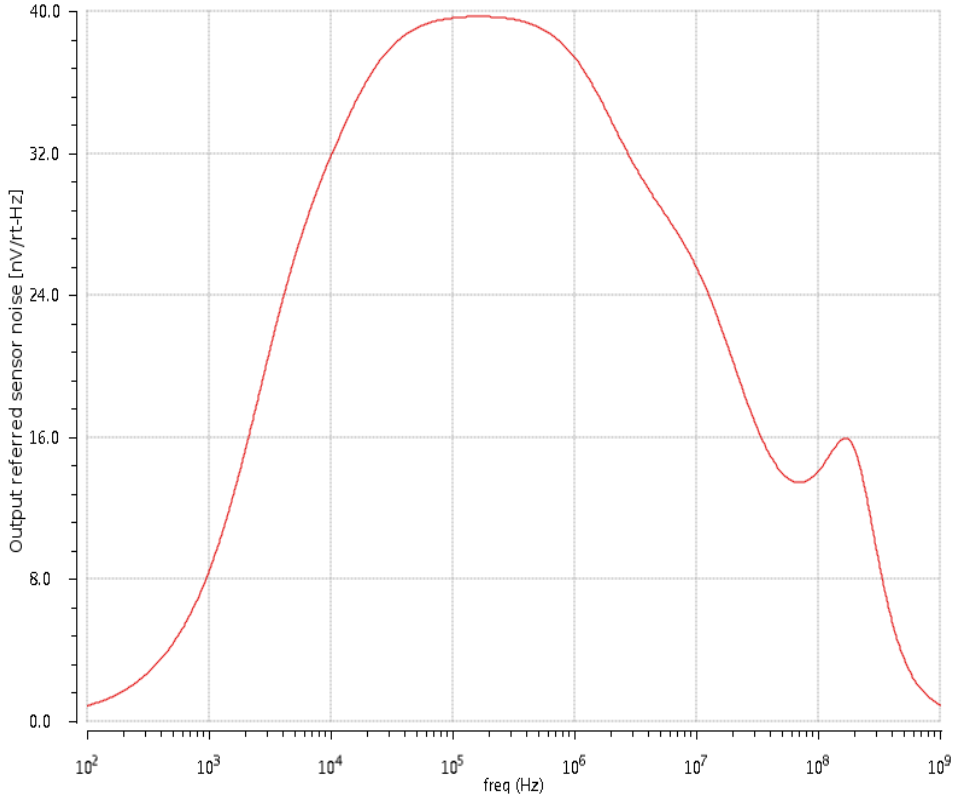

Figure 4.14: Sensor noise seen at the output.

Where in this case bandwidth is much limited due to the higher capacitance at the input due to the full bridge. The strange bump between *100 MHz* and *1 GHz* is due to the closed-loop gain of the opamp and its very high frequency poles and zeros. Its value ranges from $\overline{V_{o\ sensor\,1}(397{,}08\,kHz)} = 39{,}33\,nV/\sqrt{Hz}$ to $\overline{V_{o\ sensor\,1}(1{,}27\,MHz)} = 36{,}33\,nV/\sqrt{Hz}$.

Now, it is possible to know the total output noise adding quadratically the noise from the opamp and the sensor in the two bound set previously: $\overline{V_{o\,total}(397{,}08\,kHz)} = 45{,}64\,nV/\sqrt{Hz}$ and $\overline{V_{o\,total}(1{,}27\,MHz)} = 40{,}85\,nV/\sqrt{Hz}$. So finally, chopping will be done at *1,27 MHz*, the frequency that provides the lower total noise.

To obtain the noise in acceleration units, sensitivity equation (Eq. 2.2) and output voltage equation (Eq. 4.3) can be merged to derive the acceleration noise:

$$\left(\frac{\Delta a}{\sqrt{\Delta f}}\right)_{1,27\,MHz} = \frac{\overline{V_{o\,total}(1,27\,MHz)}}{\sqrt{\Delta f}} \frac{C_{fb}}{V_m S} = 314,23\,\frac{\mu g}{\sqrt{Hz}} \tag{4.43}$$

Where $C_{fb} = 100\,fF$ and sensitivity from Table 2.1 is $S = 0,013\,fF/g$.

Assuming the value in equation (Eq. 4.43) to be constant over a bandwidth of *100 Hz* an equivalent acceleration noise of $3,14\,mg$ can be computed. This resolution is translated into the existence of *244799* levels, so an A/D of 18 bits is needed.

Second sensor (200fF ± 20 fF)

In the case of using the second sensor, the noise at the corner frequency is $\overline{V_{o\ opamp}(480,2\,kHz)} = 35,5\,nV/\sqrt{Hz}$ and the minimum value is again found at the maximum frequency set by the opamp: $\overline{V_{o\ opamp}(1,27\,MHz)} = 29,6\,nV/\sqrt{Hz}$, where white noise is dominant from a corner frequency of $f_{corner} = 480,2\,kHz$. Due to the higher capacitance hanging at the input node compared with the other chip, opamp noise is higher at the output as predicted by equation (Eq. 4.23). This kind of noise offset for this second design can easily be seen in Figure 4.15 compared to the first sensor Figure 4.13. In this second chip case, the corner frequency is different from the use of the first one, event though, the difference is relatively small as the shape of noise has been changed identically both for Flicker and thermal noise due to the change of input node capacitance.

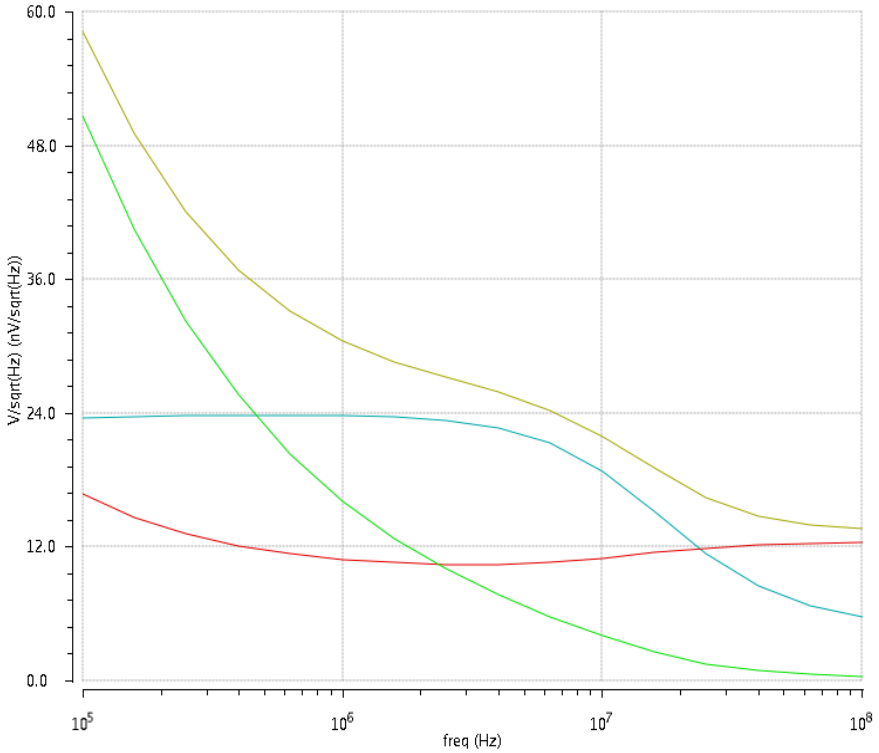

Figure 4.15: Comparison of noise. Input pair white noise (light blue), input pair Flicker noise (green), rest of transistors noise (red) and total noise (yellow).

The output noise for the second sensor can be computed utilizing the equivalent capacitance variation in Table 2.3 and output voltage equation (Eq. 4.3) for the second design.

$$\overline{V_{o\,sensor\,2}} = V_m \frac{\overline{\frac{\Delta C_{n2}}{\sqrt{\Delta f}}}}{C_{fb}} = 41{,}0 \frac{nV}{\sqrt{Hz}} \tag{4.44}$$

The noise budget for this second sensor is higher than for the first sensor, so in this case the noise from the sensor is dominant and opamp noise will have a lower impact in the total noise.

The final output total noise including simulated opamp and second sensor noise is quadratically added and found to be $\overline{V_{o\,total}(480{,}2\,kHz)} = 54{,}2\,nV/\sqrt{Hz}$ and $\overline{V_{o\,total}(1{,}27\,MHz)} = 50{,}6\,nV/\sqrt{Hz}$. Finally, similarly to equation (Eq. 4.43), noise is converted to acceleration units in equation (Eq. 4.45) for the best noise case:

$$\left(\frac{\Delta a}{\sqrt{\Delta f}}\right)_{1{,}27\,MHz} = \frac{\overline{V_{o\,total}(1{,}27\,MHz)}}{\sqrt{\Delta f}} \frac{C_{fb}}{V_m S} = 20{,}2 \frac{\mu g}{\sqrt{Hz}} \tag{4.45}$$

Where in this case sensitivity is $S = 0{,}25\,fF/g$. Even though that the absolute output

voltage noise is higher in this design that using the first sensor, the noise in acceleration units is much lower thanks to the higher sensitivity of the sensor.

Assuming the value in equation (Eq. 4.45) to be constant over a bandwidth of *100 Hz* an equivalent acceleration noise resolution of $202{,}4\,\mu g$ can be computed. Finally, similarly to equation (Eq. 3.48), a total span of acceleration for this sensor is found to be $160\,g$, that means having *790514* quantization levels and the need of a 20 bit A/D.

4.8.3 Large signal

First sensor (50fF ± 5 fF)

Using equation (Eq. 4.3), the maximum ratings of output voltage are:

$$\left(V_o\right)_{max} = V_m \frac{\Delta C_{max}}{C_{fb}} = \pm 50\,mV \tag{4.46}$$

That is almost half the output voltage than the first design due to the fabrication mismatch and parasitics that limit the feedback capacitance. However, this value is tightly controlled thanks to the reduced variability of the closed-loop gain, so simulated value results in the same range. The simulated sensitivity of the readout circuit is $S_{readout} = 9{,}74\,mV/fF$, smaller than with the first readout circuit. Finally, similarly to equation (Eq. 3.50), in equation (Eq. 4.47) sensitivity is computed to be in acceleration units.

$$S_{readout2}\left[\frac{V}{g}\right] = S_{readout2}\,S_{sensor1} = 126{,}7\,\frac{\mu V}{g} \tag{4.47}$$

Once noise and maximum output voltage are known, the best SNR case can be computed for this second design and this sensor:

$$SNR\left(1{,}27\,MHz\right) = 20\log\frac{V_{o\,max}}{V_{o\,TOTAL}} = 101{,}8\,dB \tag{4.48}$$

Second sensor (200fF ± 20 fF)

For the second sensor, theoretical output range obtained from formula (Eq. 4.3) and confirmed by simulations is $\pm 200\,mV/fF$. The sensitivity of the readout circuit is the same than in the previous section and sensitivity of the sensor is presented in Table 2.1, so the total sensitivity of the system is:

$$S_{readout}\left[\frac{V}{g}\right]=S_{readout}\,S_{sensor}=2{,}44\,\frac{mV}{g} \tag{4.49}$$

Once noise and maximum output voltage are known, the best SNR case can be computed for this second design and this sensor:

$$SNR\left(1{,}27\,MHz\right)=20\log\frac{V_{o\,max}}{V_{o\,TOTAL}}=99{,}9\,dB \tag{4.50}$$

5 CONCLUSIONS

Once simulations and measurement (when available) have been shown, a comparison of both designs should be carried out in order to know to advantages and disadvantages of each design, the drawbacks and the cases where one design or the other may perform better.

First of all, a straightforward concept, not found in the literature, may be reviewed because its conclusions should be taken into account during the design and, more concretely, during the choice of whether a PMOS or NMOS input stage should be implemented. PMOS transistors have been always considered to be less noisy than NMOS transistors, and this is true for Flicker noise (and hence, for low frequencies) as observed along the report. In equation (Eq. 3.26) Flicker noise is shown to be proportional to the Flicker noise constant, that has been reported to be higher in NMOS than in PMOS transistors [19][24]. However, in high frequency applications where white noise is the dominant at the working frequency, PMOS transistors tend to have a greater noise than NMOS transistors because their lower transconductance for the same dimensions and biasing current, a constant that is inversely proportional in the noise equation (Eq. 3.25). Besides, this noise performance makes the corner noise of PMOS transistors to be at much lower frequencies than in NMOS transistors. Hence, a designer facing a similar design should think about the priorities in his design: On one hand, using a PMOS input stage provides a much lower corner frequency and a lower exigency on the frequency response of the amplifying circuit at the cost of a greater noise floor or the need of a more accurate compensation to keep it to levels similar to NMOS. On the other hand, using an NMOS input stage provides a lower floor noise at the price of having the noise corner frequency at a much higher frequency and the need of an accurate design of the high frequency response of the amplifying stage. Otherwise, an important limitation of the maximum chopping frequency arises.

Another important thing to take into account during the design is to avoid focusing the design keeping input transistors in the strong inversion saturation region because in readout circuits with demanding specifications, important improvements may appear when studying other working regions. Focusing on the strong inversion saturation region when anything limits the design (such as in our case, a time constrain design scenario) may end up with lower performances. Consequently, a detailed study of this issue is recommended as well as the use of all-regions models and simulations are highly recommended.

Now it has arrived the time to compare the two designs presented along this report in order

to clarify which one is best (if there is one) or which one fits better or worse for some cases. To do so, the final figures for the two designs using the first sensor will be very useful. Finally, the benefits and disadvantages of using the first or second sensor in the second design will be reviewed.

In Table 5.1, a comparison of the main figures for both designs utilising the first sensor are shown.

	1st design	2nd design
Open loop gain [*dB*]	15,2	72,2
Bandwidth [*Hz*]	74,5 M	30,3 k
UGB [*Hz*]	230,4 M	211,5 M
PM [º]	39,8	63,2
Noise corner frequency [*Hz*]	27,0 k	397,1
Amplifier added noise* [$nV/\sqrt{Hz}$]	53,4	18,7
Total noise* [$nV/\sqrt{Hz}$]	66,1	40,9
Total noise in aceleration units [$\mu g/\sqrt{Hz}$]	284,5 (232,0**)	314,2
SNR [dB]	104,3	101,8
Total sensitivity $\mu V/g$	280,1	126,7
Voltage Supply [V]	3	2,5
Current Consumption [μA]	363	450

Table 5.1: Comparison of both designs using the first sensor. Figures shown has been obtained by simulations. (*Output referred noise (circuit and sensor noise), **Using opamp measured noise of sample #1)

In Table 5.1 it can be seen that in terms of output referred noise, the second design is better than the first one. However, looking at the equivalent acceleration noise the first design has a better performance. This is due to the different gain and total sensitivities of each design. In the literature several documents have been found that rely on the absolute output noise, however, the equivalent acceleration noise is recommended to be used instead.

The SNR of the first design can be observed to be higher. This issue is due to the fact that the maximum voltage swing of the second sensor (with the same chopping frequency voltage amplitude V_m) is lower than the first sensor, concretely it has almost half the voltage swing, and so can be observed in the SNR. The same can be said of the sensitivity. This difference may be reduced by using a NMOS input stage in the first design, making both circuits quite flexible and able to meet noise specifications.

Even though low noise and a high sensitivity were the two main specifications for the designs, the fact that the second design has a lower performance on them may seem that it is worse than the first design. However, both the SNR and the sensitivity can be easily improved and made much better that the first design if the amplitude of the chopping voltage (V_m) is increased. Contrarily, some important disadvantages that the first design present cannot be removed so easily such as the input node sensitivity to parasitics (versus the AC ground of the second design), its potential non-linearity issues for high sensitive sensors (due to the approximation made in equation (Eq. 3.6)), its difficult-to-control gain variations with fabrication variations (versus the variation of the second sensor, just sensitive to variations of the feedback capacitor), its low precision matching in the capacitive input voltage divider and a potential high attenuation at this voltage divider due to a large parasitic sensor and/or opamp capacitance not present in the closed-loop design.

To be fair, the first design has a much easy to do layout, a higher bandwidth due to the lack of compensation and an easy way to increase its open-loop gain (versus the limited value of the feedback capacitance in the closed-loop approach, dependant on the feedback capacitors) and output voltage swing than the second design, but if removal of parasitics, reduction of fabrication variations and a robust frequency compensation are a must, the closed-loop design should be used.

Another important aspect that benefits the closed-loop design is the fact that the optimisation of the input stage for noise do not affect the overall closed-loop noise of the readout circuit, while in the first design the gain is fixed by the parameters set in the input pair for noise optimisation. This is also important in the case where the gain of the circuit is set in order to have a given output voltage range to send to the next circuit.

When comparing the results of the second design using the first and second sensor, it is possible to see that, even though the second sensor noise referred at the output is similar to the one provided by the first sensor, the design has a lower noise in acceleration units. This is due to the higher sensitivity of this second sensor, that quantifies the fact that even though a readout circuit with demanding characteristics is important, having a sensor with a good sensitivity and, for some designs, low parasitics is also a key factor for a good performance or a less demanding circuit design.

Finally, a comparison with the literature is a must if we want to make fair conclusions of the quality of our design. In order to do that, a comparative table has been completed with some of the most recent and relevant articles of readout circuits with sensor sensitivities close to

the sensitivity of our sensors. However, it has been difficult to find recent articles utilising sensors with similar sensitivities because the actual trend is to increase it as much as possible. The criteria of organisation of the table has been to arrange the papers with the sensor sensitivity in the x-axis and the total noise in $\mu g/\sqrt{Hz}$ units in the y-axis. Comparing the noise like that it is possible to easily compare which implementation will have a better resolution when the noise is integrated with the same bandwidth. Besides, as we saw in the second design used with the second sensor, the absolute output or input referred noise in voltage unit does not provide a good value to compare noise because the sensitivity of the sensor may or may not improve this figure in acceleration units (the final wanted measurement); due to that, lower sensitivities tend to have higher noise than higher sensitivities.

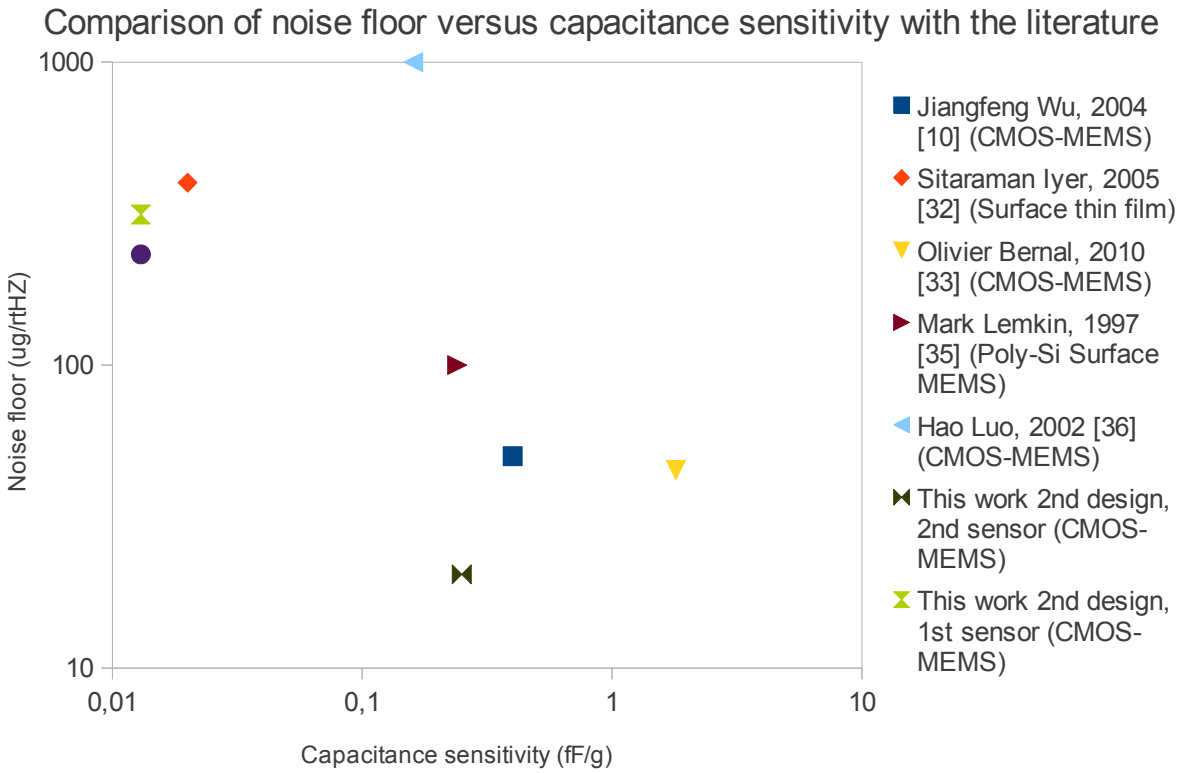

Figure 5.1: Comparison of floor noise of the designs presented in the report with the literature.

As it can be seen in Figure 5.1, the two designs using the first sensor have relatively high noises, but taking into account their sensitivity they have good noise values, and even lower noise than [33] although it has a higher sensitivity. The performance of the second sensor on the second design has also a good performance, with a lower noise than sensors with a similar sensitivity. Consequently, it is possible to conclude that the noise performance of the designs presented along this document have figures lower than similar designs present in

the literature.

6 FUTURE WORK

Future work should have an important focus on the closed-loop design. A very limiting time constrained scenario took us to start with an important amount of initial conditions as well as a bunch of things of the design could not be studied and tested as thoroughly as desired.

Hence, in this design a more complete optimisation taking also into account the biasing current should be carried out. Besides, work on all the nonidealities and drawbacks explained all along the report and specially in the conclusions chapter is also a good strategy in order to make the actual open-loop approach more attractive.

Another issue may be studied in depth that affects the two presented circuits: up to this point, the noise minimisation has been focused on white noise as chopping makes the circuit to work at frequencies well below Flicker noise is dominant. However, minimising thermal noise might increase Flicker noise. An strategy that minimises both noises may be interesting to be carried out in order to obtain two main benefits: avoiding the increase of the noise corner frequency and reduce the remnant Flicker noise at frequencies where it is not dominant. This approach is specially interesting to be used with a NMOS input pair because of the observed noise corner frequency that they present over PMOS. Doing so, more relaxed frequency specifications could be used or a wider usable bandwidth.

Finally, timing conditions made the second circuit to be optimised for the first sensor even though it is finally going to be used with the second sensor. Performance of this closed-loop approach with the second sensor is more than acceptable, even though better noise figures may be obtained if an optimisation for the second sensor is applied.

References

[1] P. Michalik et al. *"Technology-portable Mixed-signal Sensing Architecture for CMOS-integrated z-axis Surface-micromachined Accelerometers"* in *17th Int. Conf. Mixed Design of Integrated Circuits and Systems (MIXDES 2010)*, Wroclaw, Poland, 2010, pp. 431-435.

[2] R.S. Payne et al. *"Surface Micromachining: From Vision to Reality to Vision."* in *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers,* San Francisco, CA, 1995, pp. 164-165.

[3] J. Wu. *"Sensing and Control Electronics for Low-Mass Low-Capacitance MEMS Accelerometers."*, Doctoral Dissertation, Carnegie Mellon Univ., 2002.

[4] N. Yazdi et al. *"Micromachined Inertial Sensors."* in *Proc. IEEE*, vol. 86, pp. 1640-1659, Aug. 1998.

[5] C. Lu, M. Lemkin, B.E. Boser. "*A Monolithic Surface Micromachined Accelerometer with Digital Output."* in *IEEE J. Solid-State Circuits,* vol. 30, pp. 1367-1373, Dec. 1995.

[6] University of California, Berkeley. Berkeley Sensor & Actuator Center. B.E. Boser. *"Electronics for Micromachined Inertial Sensors.",* Berkeley, CA., 1997.

[7] M. Lobur, A. Holovatyy. "*Overview and Analysis of Readout Circuits for Capacitive Sensing in MEMS Gyroscopes (MEMS Angular Velocity Sensors)."* in *5th Int. Conf. Perspective Technologies and Methods in MEMS Design (MEMSTECH 2009)*, Zakarpattya, Ukraine, 2009, pp. 161-163.

[8] N. Yazdi, H. Kulah, K. Njafi. *"Precision Readout Circuits for Capacitive Microaccelerometers."* in *Proc. IEEE Sensors,* vol. 1, pp. 28-31, Oct. 2004.

[9] C. Zhang et al. *"A Large Dynamic Range CMOS Readout Circuit for MEMS Vibratory Gyroscope."* in IEEE Sensors Conf., Lecce, Italy, 2008, pp. 1123-1126.

[10] J. Wu, G. Fedder, L.R. Carley. *"A Low-Noise Low-Offset Capacitive Sensing Amplifier for a 50-µg/rtHz Monolithic CMOS MEMS Accelerometer."* in IEEE J. Solid-State Circuits, vol. 39, no. 5, May 2004.

[11] InvenSense. S. Nasiri. *"A Critical Review of MEMS Gyroscopes Technology and Commercialization Status."*, Santa Clara, CA.

[12] P. Michalik et al. *"An Approach to MEMS smart sensor design using CMOS BEOL."* in

14th Int. Conf. MEMSWAVE, Postdam, Germany, 2013.

[13] Information provided by Mr. Piotr Michalik. Not published.

[14] G. Fedder. *"Simulation of Microelectromechanical Systems"*, Doctoral Dissertation, University of California at Berkeley, 1994.

[15] H. Sun et al. *"A Low-Power Low-Noise Dual-Chopper Amplifier for Capacitive CMOS-MEMS Accelerometers."* in IEEE J. Sensors, vol. 11, no. 4, April 2011.

[16] B.E. Boser, R.T. Howe. *"Surface Micromachined Accelerometers."* in Proc. IEEE Int. Conf. Custom Integrated Circuits (CICC), Santa Clara, CA, 1995, pp. 337-344.

[17] N. Somasundaram. *"Measurements device for CMOS-MEMS accelerometer"*, Bachelor Thesis, Sastra University and Universitat Politècnica de Catalunya, 2014.

[18] C. Goldsmith et al. *"Characteristics of micromachined switches at microwave frequencies"* in IEEE MTT-S Microwave Symposium Digest, San Francisco, CA, 1996, vol. 2, pp. 1141-1144.

[19] Universitat Politècnica de Catalunya. Departament d'Enginyeria Electrònica. Jordi Madrenas. *"Analog Integrated Design (DAI). Device Models."* Class notes, Barcelona, Spring 2013.

[20] P.R. Grey, R.G. Meyer et al, *"Analysis and Design of Analog Integrated Circuits"*, 5th edition, Chichester: John Wiley, 2009.

[21] B. Razavi, *"Fundamentals of microelectronics"*, 1st edition, Chichester: John Wiley, 2008.

[22] Universitat Politècnica de Catalunya. Departament d'Enginyeria Electrònica. Jordi Madrenas. *"Analog Integrated Design (DAI). Basic Blocks."* Class notes, Barcelona, Spring 2013.

[23] D.A. Johns, K. Martin, *"Analog Integrated Circuit Design"*, 1st edition, Chichester: John Wiley, 1997.

[24] P.E. Allen, D.R. Holberg, *"CMOS Analog Circuit Design."*, 2nd edition, Oxford: Oxford University Press, 2002.

[25] SG25_H1_H3_H3P_process_spec.pdf → technology file

[26] Y. Tsividis, C. McAndrew, *"The MOS Transistor"*, Int. 3rd edition, Oxford: Oxford University Press, 2012.

[27] W. Sansen, *"Analog Design Essentials"*, 1st edition, Springer, 2007.

[28] J. Madrenas, D. Fernández, J. Cosp. *"Resistive Trans-Fuse and Differential Resistor for Common-Mode-Tolerant Nonlinear Space Filtering"* in 24th Conf. Design of Circuits and Integrated Systems (DCIS 2006), Barcelona, 2006.

[29] A. Tajalli, Y. Leblebici, E.J. Brauer. *"Implementing ultra-high-value floating tunable CMOS resistors"* in Electronics Letters, vol. 44, no. 5, Feb. 2008.

[30] K. To. *"High Frequency Noise Characteristics of RF MOSFETs in Subthreshold Region"* in IEEE Radio Frequency Integrated Circuits (RFIC) Symposium, June 2003.

[31] R.R. Harrison, C. Charles. *"A Low-Power Low-Noise CMOS Amplifier for Neural Recording Applications"* in IEEE J. Solid-State Circuits, vol. 38, no. 6, June 2003.

[32] University of Utah. R.R. Harrison, *"MOSFET Operation in Weak and Moderate Inversion."* Clas Notes, Utah.

[33] S.V. Iyer et al. *"A 0,5 mm² Integrated Capacitive Vibration Sensor with Sub-10 zF/rt-Hz Noise Floor."* in Proc. IEEE Int. Conf. Custom Integrated Circuits (CICC), San José, CA, 2005.

[34] O.D. Bernal et al. *"A Low-Power High-Performance Accelerometer ASIC for High-End Medical Motion Sensing."* in 32nd IEEE Ann. Int. Conf. Engineering & Biology Society (IEEE EMBS), Buenos Aires, Argentina, Sept. 2010, pp. 190-193.

[35] M.a. Lemkin et al. *"A 3-axis Force Balanced Accelerometer Using a Single Proof-Mass."* in Int. Conf. Solid-State Sensors and Actuators (TRANSDUCERS '97), Chicago, June 1997, pp. 1185-1188.

[36] H. Luo et al. *"A Post-CMOS Micromachined Lateral Accelerometer."* in J. Microelectromechanical Systems, vol. 11, no. 3, June 2002, pp. 188-195.