UNIVERSITAT POLITÈCNICA DE CATALUNYA
BARCELONATECH

DESIGN OF A CAMERA FOR THE IMAGE STABILIZATION SYSTEM FOR THE SOLAR ORBITER PROJECT

A Master's Thesis

Submitted to the Faculty of the

Escola Tècnica d'Enginyeria de Telecomunicació de Barcelona

Universitat Politècnica de Catalunya

by

DAVID ROMA DOLLASE

In partial fulfilment

of the requirements for the degree of

MASTER IN TELECOMMUNICATIONS ENGINEERING

Advisor: JOSÉ M. GOMÉZ CAMA

Barcelona, March 2014

Abstract

The Correlation Tracking Camera (CTC) is a high frame rate low resolution camera. It is used by the Image Stabilization System (ISS), which function is to detect and correct the jitter introduced by the spacecraft. The CTC provides images which are processed by the ISS using a correlation tracking algorithm and it detects displacements with subpixel resolution. Based on its results a mirror is tipped and tilted, in order to stabilize the image position for the FPA (Focal Plane Assembly) image cameras. The FPA will provide high-resolution and full-disk measurements of the photospheric magnetic field, goal of the Polarimetric and Helioseismic Imager (PHI) instrument of the Solar Orbiter mission.

Acknowledgements

I would like to express my special appreciation and thanks to the entire ISS team, working at the University of Barcelona (UB), the Kiepenheuer-Institut für Sonnenphysik (KIS) and SENER. I want to thank them especially for their patience and guidance and for all the work they have done and all they have teach me. Without them, the development of the CTC will have been impossible.

From the UB:

- José M. Gómez Cama: principal investigator (IP).
- José Bosch: co-principal investigator (CoIP).
- Manuel Carmona: project manager.
- Manuel López de Miguel: quality and product assurance manager.
- And all my coworkers: Tomás Carrasco, Josep Sabater and Albert Casas.

From KIS: Reiner Volkmer, Thorsten Maue and Eiji Nakai.

From SENER: Xavi Llamas and Laura Diez.

And finally also thanks for the people from the workshop of the Electronics Department at UB.

Revision history and approval record

Revision	Date	Purpose
0	24/02/2014	Document creation
1	10/03/2014	Document revision

Written by:		Reviewed and approved by:	
Date	24/02/2014	Date	10/03/2014
Name	David Roma Dollase	Name	Manuel Hernandez Pajares
Position	Project Author	Position	Project Supervisor

Table of contents

List of Figures

List of Tables:

1. Introduction

1.1. Solar Orbiter

The Solar Orbiter (SO) main objective is to address how does the sun create and control the heliosphere. The Solar was first discussed on March 1998, but it was not proposed until 2007 [1]. Several studies over objectives and feasibility were undertaken and the mission formally started at 2008. The four top-level scientific questions being addressed by Solar Orbiter are:

- How and where do the solar wind plasma and magnetic field originate in the corona?
- How do solar transients drive heliospheric variability?
- How do solar eruptions produce energetic particle radiation that fills the heliosphere?
- How does the solar dynamo work and drive connections between the Sun and the heliosphere?

To answer these questions, it is essential to make in-situ measurements of the solar wind plasma, fields, waves, and energetic particles close enough to the Sun that they are still relatively pristine and have not had their properties modified by subsequent transport and propagation processes. This is one of the fundamental drivers for the Solar Orbiter mission, which will approach the Sun to 0.28 AU.

Relating these in-situ measurements back to their source regions and structures on the Sun requires simultaneous, high-resolution imaging and spectroscopic observations of the Sun in and out of the ecliptic plane. The resulting combination of in-situ and remote-sensing instruments on the same spacecraft, together with the new, inner-heliospheric perspective, distinguishes Solar Orbiter from all previous and current missions, enabling breakthrough science which can be achieved in no other way.

The baseline mission is planned to start in January 2017 with a launch on a NASA-provided launch vehicle from Cape Canaveral, placing the spacecraft on a ballistic trajectory that will be combined with planetary gravity assist maneuvers (GAM) at Earth and Venus. The second Venus GAM places the spacecraft into a 4:3 resonant orbit with Venus at a perihelion radius of 0.284 AU. The first perihelion at this close distance to the Sun is reached 3.5 years after launch. This orbit is the start of the sequence of resonances 4:3-4:3-3:2-5:3 that is used to raise gradually the solar inclination angle at each Venus GAM. The resulting operational orbit has a period of 168 days during the nominal mission with a minimum perihelion radius of 0.28 AU. The end of the nominal mission occurs 7 years after launch, when the orbit inclination relative to the solar equator reaches 25°. The inclination may be further increased during an extended mission phase using additional Venus GAMs, to reach a maximum of 34° for the January 2017 baseline and 36° for a launch in March 2017.

1.1.1. Scientific Payload

The in-situ instruments [2]**:**

- The Solar Wind Analyser (SWA) instrument suite (C. J. Owen, PI, UK) will fully characterize the major constituents of the solar wind plasma (protons, alpha particles, electrons, heavy ions) between 0.28 and 1.4 AU.

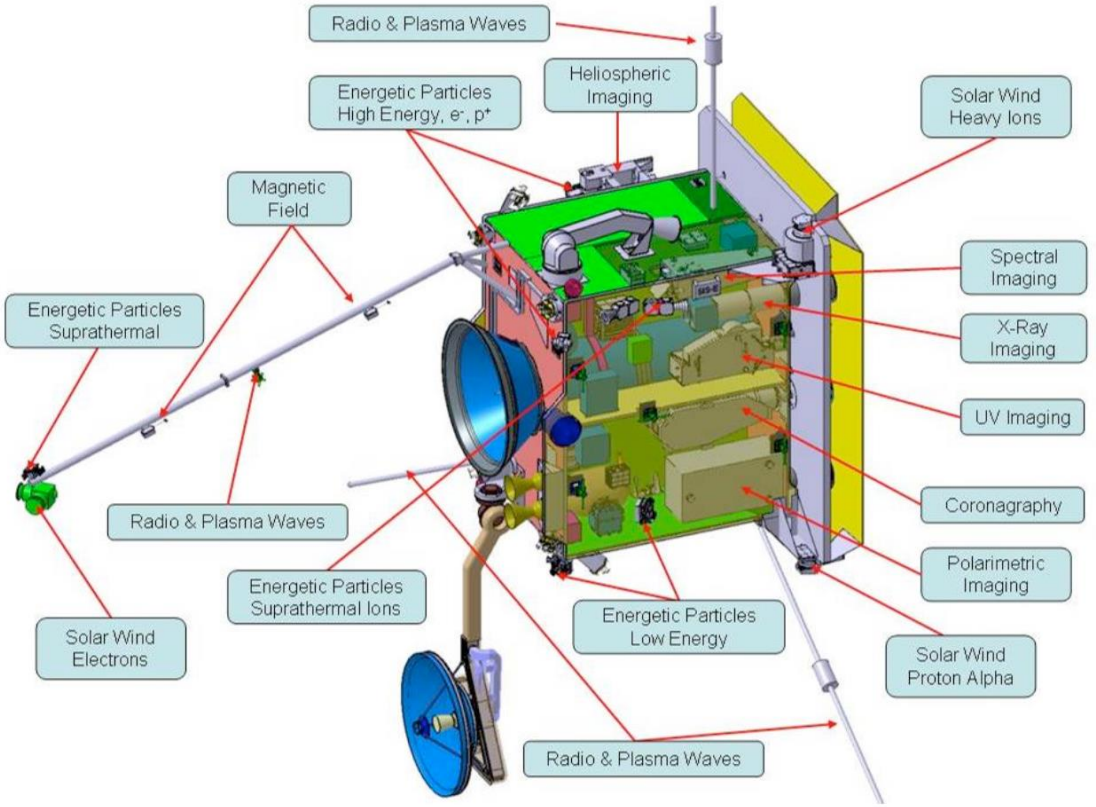

FIGURE 1-1 SOLAR ORBITER SCIENTIFIC PAYLOAD [1]

- The Energetic Particle Detector (EPD) experiment (J. R. Pacheco, PI, Spain) will measure the properties of suprathermal ions and energetic particles in the energy range of a few keV/n to relativistic electrons and high-energy ions (100 MeV/n protons, 200 MeV/n heavy ions).
- The Magnetometer (MAG) experiment (T. S. Horbury, PI, UK) will provide detailed in-situ measurements of the heliospheric magnetic field.
- The Radio and Plasma Waves (RPW) experiment (M. Maksimovic, PI, France) will measure magnetic and electric fields at high time resolution and determine the characteristics of electromagnetic and electrostatic waves in the solar wind from almost DC to 20 MHz.

The remote-sensing instruments:

- The Polarimetric and Helioseismic Imager (PHI, S. K. Solanki, PI, Germany) will provide high-resolution and full-disk measurements of the photospheric vector magnetic field and line-of-sight velocity as well as the continuum intensity in the visible wavelength range.
- The Extreme Ultraviolet Imager (EUI, P. Rochus, PI, Belgium) will provide image sequences of the solar atmospheric layers from the photosphere into the corona.
- The Spectrometer/Telescope for Imaging X-rays (STIX) (A. O. Benz, PI, Switzerland) provides imaging spectroscopy of solar thermal and non-thermal X-ray emission from ~4 to 150 keV.
- The Multi Element Telescope for Imaging and Spectroscopy (METIS) Coronagraph (E. Antonucci, PI, Italy) will perform broad-band and polarized imaging of the visible K-corona, narrow-band imaging of the UV and EUV corona and spectroscopy of the most intense lines of the outer corona.

- The Solar Orbiter Heliospheric Imager (SoloHI, R. A. Howard, PI, U.S.) will image both the quasi-steady flow and transient disturbances in the solar wind over a wide field of view by observing visible sunlight scattered by solar wind electrons.
- A European-lead extreme ultraviolet imaging spectrograph with contributions from ESA member states and ESA. This instrument will remotely characterize plasma properties of regions at and near the Sun, based on the previously selected Spectral Imaging of the Coronal Environment (SPICE) investigation. For simplicity, this payload element will be referred to as SPICE in this document.

1.2. Polarimetric and Helioseismic Imager

PHI will provide high-resolution and full-disk measurements of the photospheric vector magnetic field and line-of-sight (LOS) velocity, as well as the continuum intensity in the visible wavelength range at a cadence of one set of observables per minute. The LOS velocity maps will have the accuracy and stability to allow detailed helioseismic investigations of the solar interior, in particular of the solar convection zone.

The PHI instrument consists of two telescopes, a High Resolution Telescope (HRT) that will image a fraction of the solar disk at a resolution reaching ~200 km at perihelion, and a Full Disk Telescope (FDT) to image the full solar disk at all phases of the orbit. PHI will carry out measurements with a narrow-band filtergraph at several wavelength positions in a Zeeman-sensitive photospheric spectral line, and in the nearby continuum. At each spectral position, the polarization state of the incoming light will be analyzed. From the observables (the four Stokes parameters that fully describe an electromagnetic wave), a number of solar physical quantities will be retrieved: the LOS flow velocity (v_{LOS}) and the three components of the vector magnetic field (field strength, inclination, and azimuth). From these quantities, the LOS component and the transverse component of the magnetic field vector (B_{LOS} and B_{Trans}) can be derived. Together with the continuum intensity I_c (a proxy for the plasma temperature, which also provides the image context for the other variables), spatial maps of these variables constitute the main data products of the instrument. The off-axis Ritchey-Chrétien HRT will image a fraction of the solar disk at a resolution reaching ~200 km at minimum perihelion distance (0.28 AU).

The FDT provides a FOV of 2° with a pixel size of ~720 km (at 0.28 AU), giving a complete view of the solar disk during all orbital phases. The implementation of an off-pointing mechanism (OPM) is being assessed. The OPM would allow the FDT to continue observing the whole solar disk while the spacecraft, including the HRT, is pointing off the solar disk centre. Continuous observations of the full solar disk by the FDT are needed to allow precise sensing of the solar limb and provide stable pointing. PHI will have its own image stabilization system (ISS) that compensates spacecraft jitter and other disturbances. This system is composed of a correlation tracking camera sensor, a control algorithm and rapid tip-tilt mirrors.

In order to limit the amount of light entering the instrument, two entrance windows, one for each telescope, are mounted on the spacecraft's heat shield. These windows act as heat rejection filters with a transmission band of about 30 nm width centered on the science wavelength, such that the total transmittance does not exceed 4% of the total incident energy.

Each telescope has its own polarization modulation package (PMP), located early in the optical path to minimize polarization cross-talk effects. Each PMP consists of two liquid crystal variable retarders (LCVRs) followed by a linear polarizer. Spectral analysis is

performed by a Fabry-Pérot filtergraph system (FG) consisting of two lithium niobate ($LiNbO_3$) etalons which extract a spectral portion of the Fe I 6173 Å absorption line and at a nearby continuum point. The FG provides a tuning range of ±0.6 Å, which is required for compensating the spacecraft radial velocity of ±30 km/s plus the range required to scan the spectral line (~400 mÅ, depending on the observing mode).

A digital processing unit (DPU) performs image accumulation, pre-processing, and calculation of physical variables (Stokes inversion and data compression), and controls the instrument interfaces with the spacecraft.

1.3. Image Stabilitzation System

The Image Stabilization System goal is to detect the jitter introduced by the spacecraft (S/C) and correct it using a Tip-Tilt Mirror (TTM). The system is based Correlation Tracking algorithm, which detects displacements with subpixel resolution.

The main ISS objective is providing a stability of 0.1arcsec in 10sec at 10Hz if the pointing jitter of the S/C is below 1arcsec in 10sec. This translates to ISS leads to 1/16th pixel resolution and precision of 1/8th pixel at the CT camera within 10sec and a bandwidth of 30Hz.

The ISS has four main functional blocks as shown in Figure 1-2.

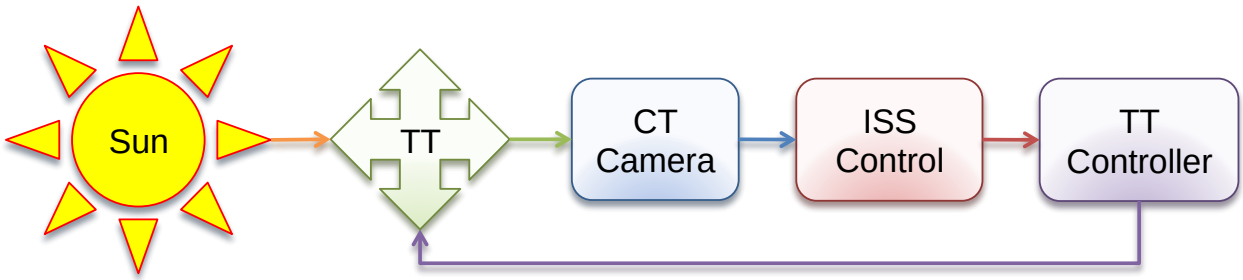

FIGURE 1-2 ISS BLOCK DIAGRAM

The High Resolution Telescope (HRT) receives the Sun light, and it is reflected by the M2 Mirror, which is controlled by the Tip-Tilt Controller (TTC). Part of this light is focalized on the CT camera sensor forming an image. This image is sent to the ISS control algorithm, which compares this image with a reference one. Based on the results, the ISS control gives a signal to the TT Controller, which moves the TT Driver and as a result the M2 Mirror. The whole system works in close-loop, allowing a precise control.

1.4. Correlation Tracking Camera

The Correlation Tracking Camera main function is to provide images at a high frame rate (nominal frame rate of 300 fps) and a resolution of 8 bits to the ISS. Also, the CTC power consumption and mass budget must be kept as low as possible. It's most important elements are an image sensor and a FPGA (Field Programmable Gate Array) that will control the sensor, preprocess the images and send them to ISS Control.

1.5. State of art of sensors

The two following technologies can be found for camera sensors: CCD (Charge Coupled Device) and APS (Active Pixel Sensor).

The main advantages of using CCD camera are:

- Well known: CCDs have been used since decades and therefore it's a proven, reliable and well known technology.
- Less noise: CCDs have less dark noise tan APS sensors.
- Quality: The radiometric response of CCDs is better. This is not true anymore for commercial sensors, but still for the space qualified parts.

The advantages of APS sensors are:

- Consumption: APS have power consumption up to 100 times less than CCD equivalent parts.
- Cost: Since APS sensors are built with a standard CMOS fabrication process, its cost is much lower.
- Radiation hardened: APS sensors are much more radiation tolerant thanks to its CMOS process than CCDs.
- Readout speed: the frame rate provided by APS sensors is much higher than for CCDs.
- Blooming: The APS sensors have a very high anti-blooming tolerance.

For this project the key parameters are consumption, radiation tolerance and readout speed, therefore an APS sensor has been used.

1.6. Scheduling

At the moment of writing this document, the development phase (PDR and CDR) has been concluded with a fully functional breadboard. The STM and EFM model are manufactured and the next millstone will be the QM manufacturing. Figure 1-3 shows the scheduling for the ISS. The project started at 2007, but the developing of the subsystems started at 2010.

1.7. Document structure

The design of the CTC is divided in two parts. The first part corresponds to the hardware: the electrical interfaces, the requirements, the implemented design and the schematics generated. The second part corresponds to the firmware design, following the European Cooperation for Space Standardization (ECSS) applicable standards.

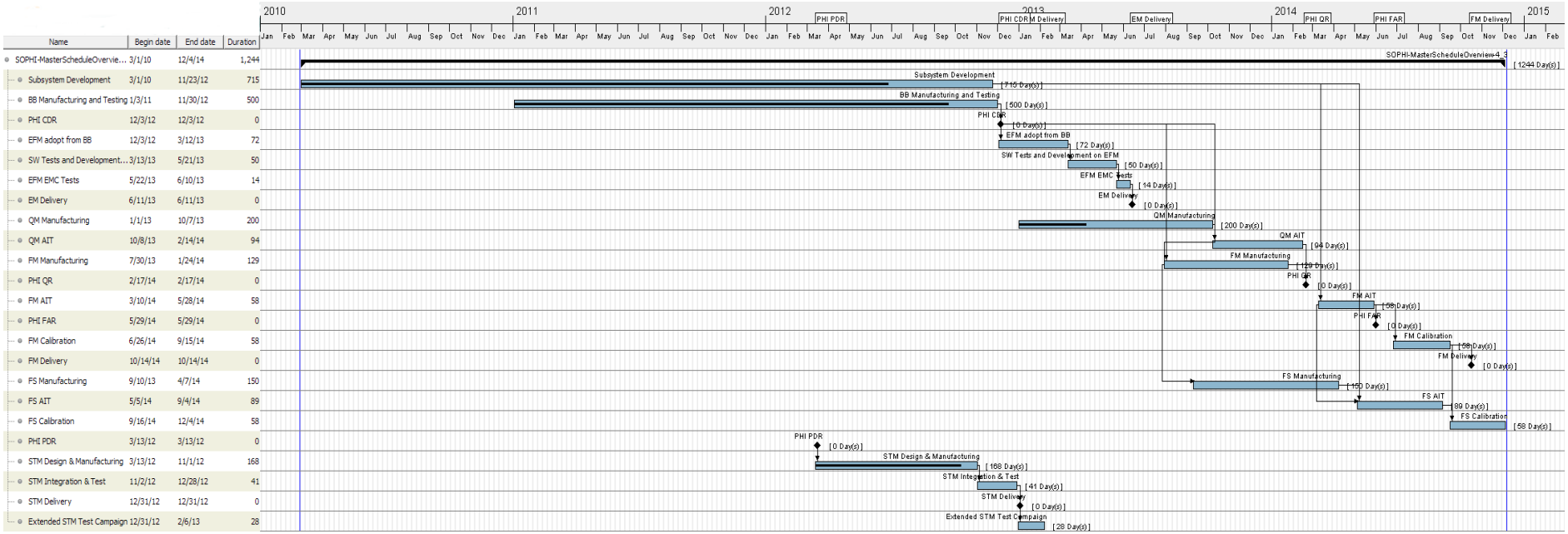

FIGURE 1-3 PROJECT SCHEDULING

2. Electronic Interface

There are two interfaces: the power supply (J107S connector) and the data interface (J105S connector).

2.1. EMC classes

The following EMC classes are defined [3]:

Class 1: Power lines and Heater Lines

Class 2: Digital lines (TM/TC) and Non-sensitive analog lines (except RF)

Class 3: Pyro Mechanisms

Class 4: Low_level sensitive lines

Class 5: RF

2.2. Data interface

The CTC data interface shall be connected to the DPU with a LVDS interface [4].

2.2.1. LVDS interface

The LVDS interface follows a scheme as shown in Figure 2-1.

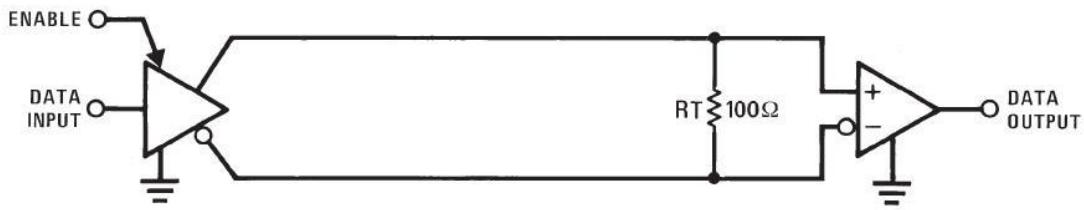

FIGURE 2-1 LVDS_OUT DRIVE (LEFT) AND LVDS_IN RECEIVER (RIGHT)

The LVDS characteristics are shown in

Parameter	Conditions	Min	Typ	Max	Units
Differential Output Voltage	RL = 100Ω	250	350	450	mV
Output Voltage High			1.38	1.6	V
Output Voltage Low		0.90	1.03		V
Input Voltage High		2.0		VCC	V
Input Voltage Low		GND		0.8	V
Rise time			1.5		ns
Fall time			1.5		ns

Table 2-1 [4].

Parameter	Conditions	Min	Typ	Max	Units
Differential Output Voltage	RL = 100Ω	250	350	450	mV
Output Voltage High			1.38	1.6	V
Output Voltage Low		0.90	1.03		V
Input Voltage High		2.0		VCC	V
Input Voltage Low		GND		0.8	V
Rise time			1.5		ns
Fall time			1.5		ns

TABLE 2-1 LVDS ELECTRICAL CHARACTERISTICS

The LVDS driver used shall be the 5962R9865103VYC and the LVDS receiver shall be the 5962R9865203VYC.

2.2.2. J105S connector

The connector used shall be a micro-D 25 female according to [3] with part number MDA225SBSPG1 [3].

2.2.3. Pin assignment

The pin assignment of the data interface shall be as shown in Figure 2-2 and Table 2-2 according to [3].

Source pin	Signal Designation	Line Type	EMC cat.	I/F circuit	Comments
1	CTC_DPU_MISO_P	True	2	LVDS_IN	Control Link data output
2	CTC_DPU_MISO_N	Comp	2	LVDS_IN	Control Link data output
3	CTC_DGND	SH		N/A	Connected to CTC DGND
4	DPU_CTC_SCLK_P	True	2	LVDS_IN	Control Link clock
5	DPU_CTC_SCLK_N	Comp	2	LVDS_IN	Control Link clock
6	CTC_DGND	SH		N/A	Connected to CTC DGND
9	CTC_DGND	SH		N/A	Connected to CTC DGND
14	CTC_DGND	SH		N/A	Connected to CTC DGND
15	CTC_DPU_IDAT_P	True	2	LVDS_OUT	Image Link data
16	CTC_DPU_IDAT_N	Comp	2	LVDS_OUT	Image Link data
18	CTC_DPU_CCLK_P	True	2	LVDS_OUT	Image Link clock
19	CTC_DPU_CCLK_N	Comp	2	LVDS_OUT	Image Link clock
21	CTC_DPU_SINT_N	Comp	2	LVDS_OUT	Control Link interrupt
22	CTC_DPU_SINT_P	True	2	LVDS_OUT	Control Link interrupt
24	DPU_CTC_MOSI_N	Comp	2	LVDS_IN	Control Link data input
25	DPU_CTC_MOSI_P	True	2	LVDS_IN	Control Link data input
7,8, 10, 11, 12, 13, 17, 20, 23	N/C				Spare pins

TABLE 2-2 J105S PIN ALLOCATION

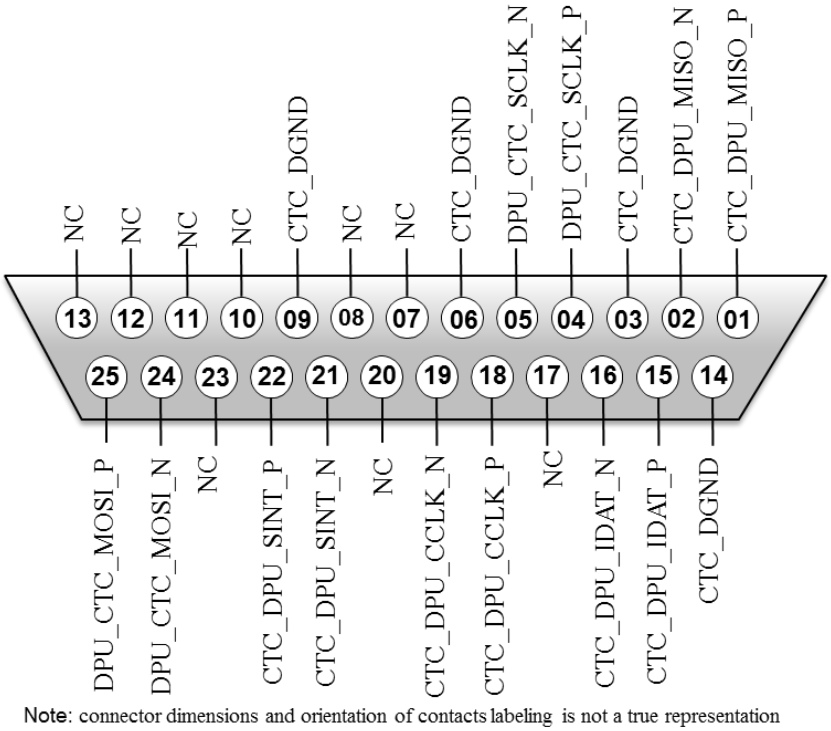

FIGURE 2-2 J105S PINS DISTRIBUTION

2.3. Power Supply

The CTC will get the power supply lines from the Camera Power Converter (CPC).

2.3.1. Power supply interface

The power supply interface follows a scheme as shown in Figure 2-3. The only exception shall be the -5V_CPC supply since it's only used at the analog circuit. Therefore, the bottom circuit (digital supply) shall be not present.

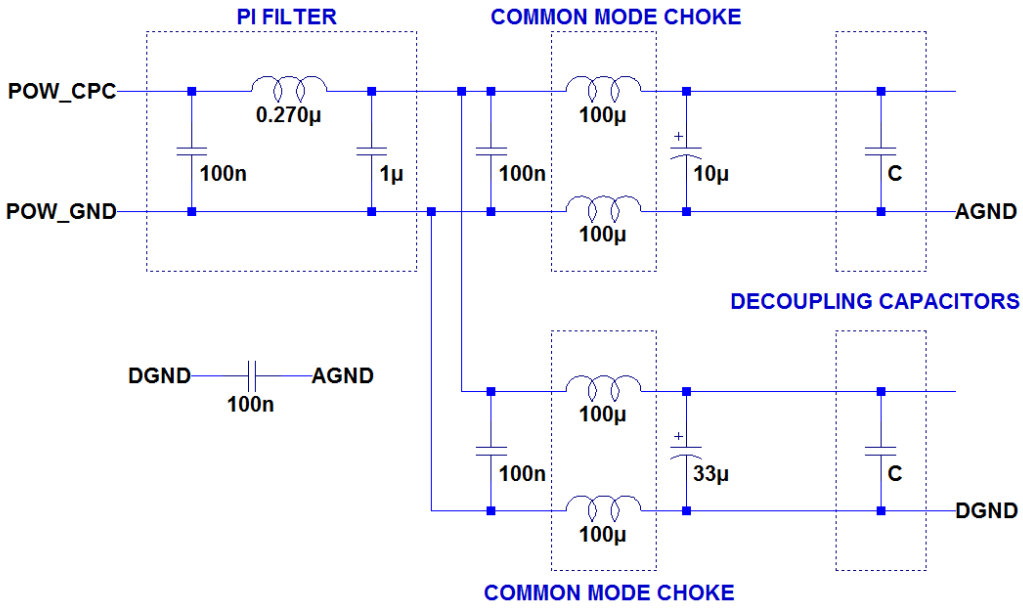

FIGURE 2-3 POWER SUPPLY INTERFACE

The power supply electrical characteristics shall be according to [5] as shown in Table 2-3.

Signal	Output Voltage (V)	Maximum Current (mA)
+3.3V_CPC	3.3 ± 0.165	158
+2.5V_CPC	2.5 ± 0.125	313
+5V_CPC	5.15 ± 0.25	56
-5V_CPC	-5.15 ± 0.25	25

TABLE 2-3 POWER SUPPLY ELECTRICAL CHARACTERISTICS

2.3.2. J107S Connector

The connector used shall be a nano-D 25 female according to [3] with part number (A42459-001 [3]).

2.3.3. Pin assignment

The pin assignment shall be as show in Figure 2-4 and Table 2-4 according to [3].

Source pin	Signal Designation	Line Type	EMC cat.	I/F circuit	Comments
1	CPC_CT_VCCD	Pow	1	POW_CPC	Voltage +3.3V
2	CPC_CT_VCCD	Pow	1	POW_CPC	Voltage +3.3V
5	CPC_CT_VCCA	Pow	1	POW_CPC	Voltage +2.5V
6	CPC_CT_VCCA	Pow	1	POW_CPC	Voltage +2.5V
9	CPC_CT_VSSI	Pow	1	POW_CPC	Voltage -5.15V
10	CPC_CT_VSSI	Pow	1	POW_CPC	Voltage -5.15V
12	CPC_CT_VCCI	Pow	1	POW_CPC	Voltage +5.15V
13	CPC_CT_VCCI	Pow	1	POW_CPC	Voltage +5.15V
14	CPC_CT_GND	Ret	1	POW_GND	CT PWR Return
15	CPC_CT_GND	Ret	1	POW_GND	CT PWR Return
16	CPC_CT_GND	Ret	1	POW_GND	CT PWR Return
19	CPC_CT_GND	Ret	1	POW_GND	CT PWR Return
20	CPC_CT_GND	Ret	1	POW_GND	CT PWR Return
21	CPC_CT_GND	Ret	1	POW_GND	CT PWR Return
3, 4, 7, 8, 11, 17, 18, 22, 23, 24, 25	NC				Spare pins

TABLE 2-4 J107S PIN ALLOCATION

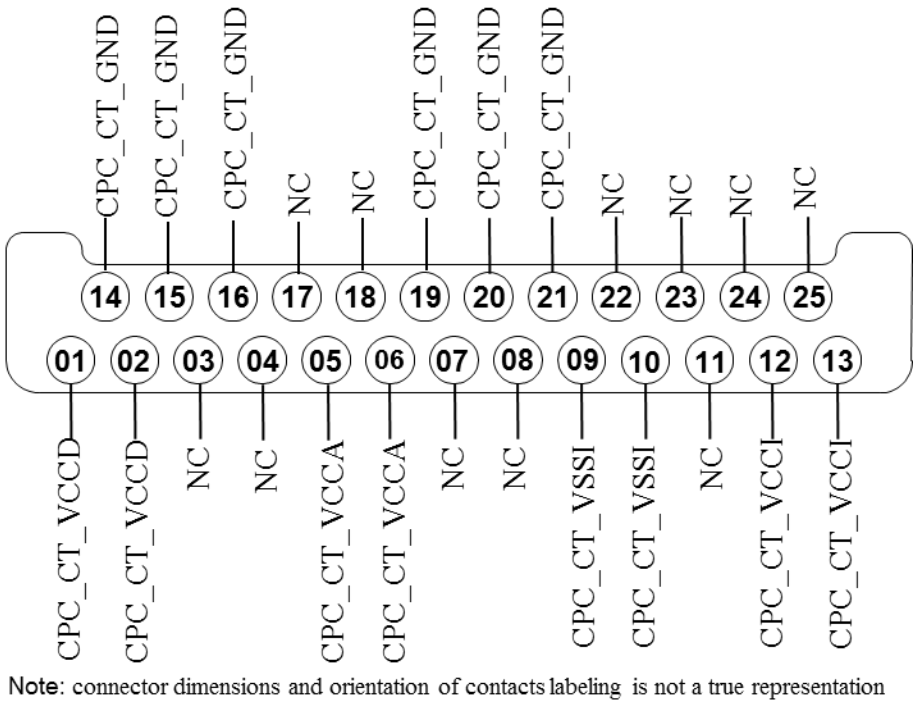

FIGURE 2-4 J107S PINS DISTRIBUTION

3. Requirement Specification

3.1. Annotations

The following section explains the fields of the requirements tables in agreement with [6].

Identification

Identification of the CTC requirement. Format: CTC-R-number_id

Abbreviation of Requirement Types

The requirements table contains a column which includes an identifier that reflects the requirement type. In Table 3-1 the abbreviation of requirement types are listed.

CO	Configuration Requirement
DE	Design Requirement
EC	EMC Design Requirement
EL	Electrical Requirement
EV	Environmental Requirement
FU	Functional Requirement
HA	Handling Requirement
HF	Human Factor Requirement
IF	Interface Requirement
IL	Identification and Labelling Requirement
LA	Location and Alignment Requirement
LS	(Integrated) Logistic Support Requirement
MC	Mechanical Requirement
MI	Mission Requirement
OP	Optical Requirement
OR	Operational Requirement
PA	Product Assurance Induced Requirement
PY	Physical Requirement
SW	Software Requirement
TH	Thermal Requirement
VE	Verification Requirement

TABLE 3-1 ABBREVIATION OF REQUIREMENTS TYPES

Verification Method

The requirements table contains a column labelled VM and includes the Verification Method. This column could contain the letters R, A, I, and T, which are the abbreviations of the following verification methods listed in Table 3-2.

R	Review of Design
A	Analysis
I	Inspection
T	Test

TABLE 3-2 ABBREVIATION OF VERIFICATION METHODS

Parent

The parent is the origin of the requirement.

Remarks

Additional information concerning the requirement.

3.2. CTC Requirements

3.2.1. Data interface

Identifier	RT	Requirement	VM	Parent	Remarks
CTC-R-100	IF	The CTC shall include two links with the DPU: the control link and the image link.	R	[5]	
CTC-R-102	IF	All signals between the DPU and the CTC shall be LVDS.	R	[5] R-0070	
CTC-R-103	IF	CTC electronics connector type and pin-out for data interface shall be according to section 2.	R		
CTC-R-105	IF	CTC electronics shall tolerate the DPU interfaces being active while in the OFF state. The CTC components shall remain within the specified derating limits under this circumstance.	R		

3.2.2. Control Link

Identifier	RT	Requirement	VM	Parent	Remarks
CTC-R-110	IF	The CTC shall include a four signal communication over LVDS with the DPU.	R	CTC-R-102	
CTC-R-111	IF	The CTC shall work as slave and the DPU as master for the Control Link communication.	R	[5]	
CTC-R-112	IF	The control link nominal bit rate shall be 1 Mbps.	R	[5]	
CTC-R-113	IF	The control link interface shall comply with the requirements in	R	[5]	

3.2.3. Image Link

Identifier	RT	Requirement	VM	Parent	Remarks
CTC-R-120	IF	The Image Link consists of two output LVDS signals to the DPU.	R	CTC-R-102	
CTC-R-121	IF	The nominal bit rate for data transmission on the Image Link shall be 100 Mbps.	R	[5]	
CTC-R-122	IF	The image link interface shall comply with the requirements in section 0.	R		

3.2.4. Power supplies

The CTC is powered by the CPC. Four supply lines are provided:

- +3.3V_CPC: 3.3V nominal
- +2.5V_CPC: 2.5V nominal
- +5V_CPC: 5.15V nominal
- -5V_CPC: -5.15V nominal

These four supply lines are provided to the CTC via individual and dedicated connector. Connector type, pin-out and location are described in the respective [NR07] and [NR08].

Identifier	RT	Requirement	VM	Parent	Remarks
CTC-R-200	EL	The operation of the CTC electronics shall be compatible with the following characteristics of the +3.3V_CPC supply line: a) +3.3V_CPC output voltage: 3.3V +/- 0.165V b) +3.3V_CPC ripple and noise: 20 mVpp max. (@1MHz) c) +3.3V_CPC rise time: 5ms minimum	A,T	[7]	
CTC-R-201	EL	The operation of the CTC electronics shall be compatible with the following characteristics of the +2.5V_CPC supply line: a) +2.5V_CPC output voltage: 2.5V +/- 0.125V b) +2.5V_CPC ripple and noise: 20 mVpp max. (@1MHz BW) c) +2.5V_CPC rise time: 5ms minimum	A,T	[7]	
CTC-R-202	EL	The operation of the CTC electronics shall be compatible with the following characteristics of the +5V_CPC supply line: a) +5V_CPC output voltage: 5.15V +/- 0.25V b) +5V_CPC ripple and noise: 20 mVpp max (@1MHz BW) c) +5V_CPC rise time: 5ms minimum	A,T	[7]	
CTC-R-203	EL	The operation of the CTC electronics shall be compatible with the following characteristics of the +5V_CPC supply line: a) -5V_CPC output voltage: -5.15V +/- 0.25V b) -5V_CPC ripple and noise: 20 mVpp max (@1MHz BW) c) -5V_CPC rise time: 5ms minimum	A,T	[7]	
CTC-R-204	EL	The maximum current consumption of the CTC electronics shall be: a) +3.3V_CPC: 158 mA b) +2.5V_CPC: 313 mA c) +5V_CPC: 56 mA d) -5V_CPC: 25 mA	R		
CTC-R-205	IF	CTC electronics connector type and pin-out for power supply lines shall be according to section 2	R		
CTC-R-206	IF	CTC electronics location for power supply lines shall be according to [8]	R	[8]	

3.2.5. Physical requirements

Identifier	RT	Requirement	VM	Parent	Remarks
CTC-R-230	MC	The CTC electronics mass shall be below 165 g.	T	[8]	This mass budget does not include mechanical fixation (screws,

					washers spacers etc) and thermal fixation (heat spreaders) means
CTC-R-231	MC	The CTC Detector board shall have a surface of 125 by 55 mm.	T	[8]	
CTC-R-232	MC	The CTC FPGA board shall have a surface of 80 by 60 mm.	T	[8]	
CTC-R-233	MC	The maximum height of the two boards shall be 32.25 mm.	T	[8]	
CTC-R-234	MC	The CTC electronics mechanical design shall comply with [NR08]	R	[8]	

3.2.6. Environmental requirements

Identifier	RT	Requirement	VM	Parent	Remarks
CTC-R-240	EV	The CTC FPGA board temperature working range shall be from -20 ºC to 80 ºC.	R	[9]	
CTC-R-241	EV	The CTC Sensor board temperature working range shall be from -20 ºC to 60 ºC.	R	[9]	
CTC-R-242	EV	The CTC electronics shall withstand a TID radiation level of shall be 25 krad without degradation of functionality.	R	[10]	

3.2.7. H/K

Identifier	RT	Requirement	VM	Parent	Remarks
CTC-R-250	FU	The CTC electronics shall provide housekeeping data of: a) FPGA temperature b) Sensor temperature c) Internal voltage references d) -5 V, +5 V and 2.5 V power supply lines	T	[5] R-1370	
CTC-R-253	FU	The CTC housekeeping data shall have accuracy better than 5 %.	R		

3.2.8. Functional requirements

The CTC images are the input of the ISS to correlate and compensate the jitter of the spacecraft. Therefore, fast data acquisition with slow delay to close the loop and low image quality is required.

Identifier	RT	Requirement	VM	Parent	Remarks
CTC-R-260	FU	The FPGA should have four working mode: - Idle mode: no images are taken and only in this mode the configuration parameters can be change. - Continuous mode: sending continuously images to ISS Control. This mode is only left when ISS Control sends an Idle Mode command. - Single mode: only one image is send to ISS Control. Then the working mode is automatically changed to Idle Mode.	R	[5]	

		- Test mode: same as continuous mode but the analog output of the image sensor is change to a fixed pattern. Used to test the analog chain without the sensor.			
CTC-R-261	FU	The nominal pixel readout frequency shall be 10 MHz	T		
CTC-R-262	FU	The image sensor used shall be the STAR 1000.	R		
CTC-R-263	FU	The FPGA used shall be an RTSX72SU.	R		
CTC-R-264	FU	The camera shall have 10 bit minimum resolution of the sensor signal.	T	[5] R-1320	
CTC-R-265	FU	The S/N ratio of the acquired image shall be better than 8bit.	T	[5] R-1325	

4. Design Report

This document explains the hardware elements (its behaviour and functionalities) and shows the analysis done to meet the requirements of the CTC.

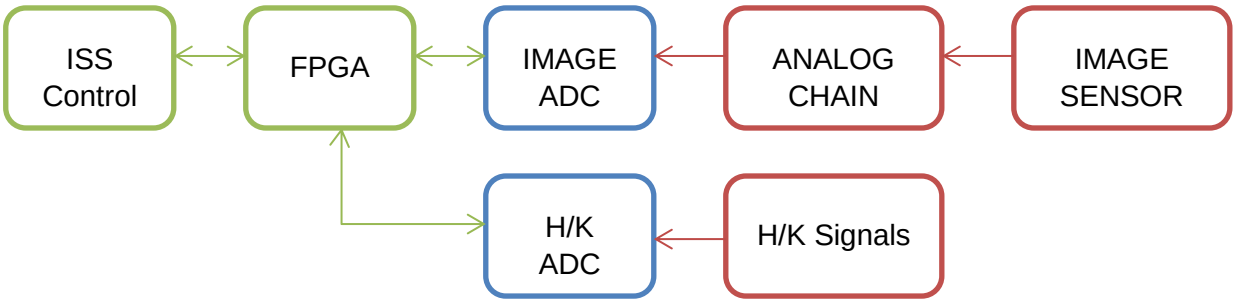

FIGURE 4-1 CTC BLOC DIAGRAM

4.1. Overview

The hardware of the CTC has the following main elements (Figure 4-1):

- FPGA: FPGA that controls the image sensor and the ADCs. It has two communication links with ISS Control: Image Link, unidirectional link dedicated to send the images read and Control Link, bidirectional SPI variant used by ISS Control to change the working mode of the firmware.
- Image Sensor: image sensor capturing the images of the CTC.
- Analog chain: operational amplifiers used to adapt the analog output of the sensor to the ADC input.
- Image ADC: ADC used to convert the analog pixel value to the digital value used by the FPGA.
- H/K ADC: ADC used to convert the H/K signals and controlled by the FPGA.

4.2. Hardware

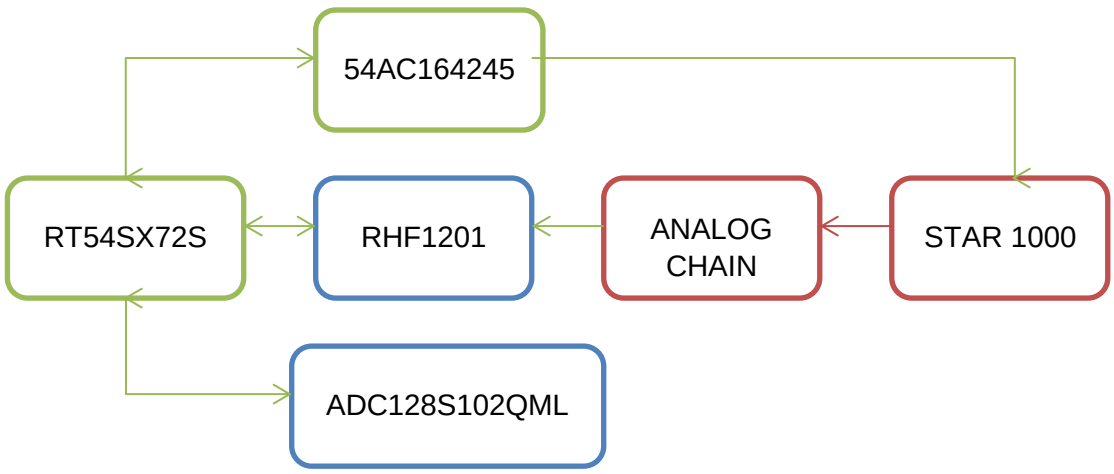

FIGURE 4-2 HARDWARE BLOC DIAGRAM

4.2.1. FPGA

The FPGA device selected for managing the CT Camera functionalities is the Microsemi (Actel) RTSX72SU [CTC-R-263] in CQFP208 package version. It's an antifuse FPGA with a 0.25 um CMOS technology, allowing low power consumption. All its registers are D-type flip-flops with asynchronous SEU robustness (Figure 4-3) and SEL immunity. The used power supply is 2.5V for the core and 3.3V for the I/O.

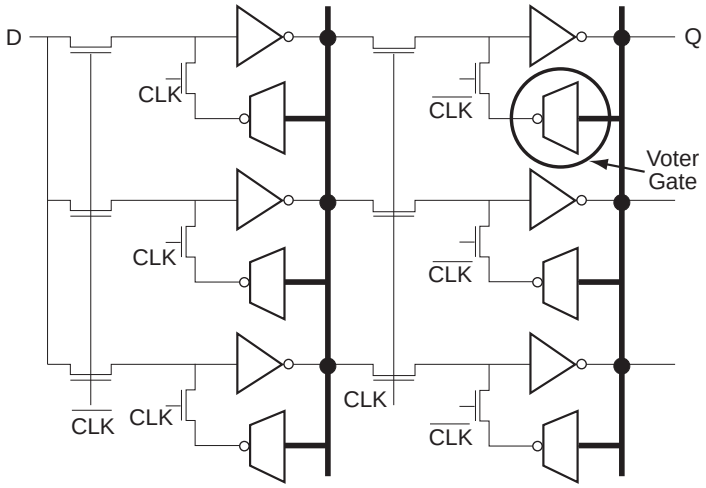

FIGURE 4-3 D-TYPE FF WITH SEU ROBUSTNESS

It works with a QS188LD9S-100.000M, a 100 MHz oscillator [CTC-R-121]. The internal working of the FPGA is explained in the firmware sections.

The communication with the ISS Control is LVDS [NR02 CTC-R-102]. The conversion from 3.3V to LVDS is done by an UT54LVDS031LVUCA [IR16], a 400 Mbps driver [CTC-R-121]. The conversion from LVDS to 3.3V is done by an UT54LVDS032LVTUCA, a 400 Mbps receiver. The receiver tolerates, even when not powered, 3.9 V at their inputs and the LVDS maximum output voltage high is 1.6 V. Therefore, there is no problem with the DPU LVDS driver working when the CTC is not powered [CTC-R-105].

4.2.2. Level shifter

The 54AC164245 is a Schmitt trigger 16-bit bidirectional CMOS transceiver [IR07]. It uses two power supplies: 3.3V used for the input or output signals of the FPGA and 5V for the input signals of the sensor. It's also used to perform the power up reset of the FPGA. This is done with a RC network connected between the 5 V supply and one input of the level shifter. Since the level shifter has internal trigger Schmitt, a clean high slew rate reset is sent to the FPGA.

4.2.3. Image sensor

The STAR 1000 [CTC-R-262] is a CMOS APS 1 Mpixel sensor with a 15 um by 15 um pixel size. It has an internal ADC, but its high power consumption (maximum of 47.3 mA at 5 V) and low resolution (maximum of 10 bits) make it unsuitable for our purpose.

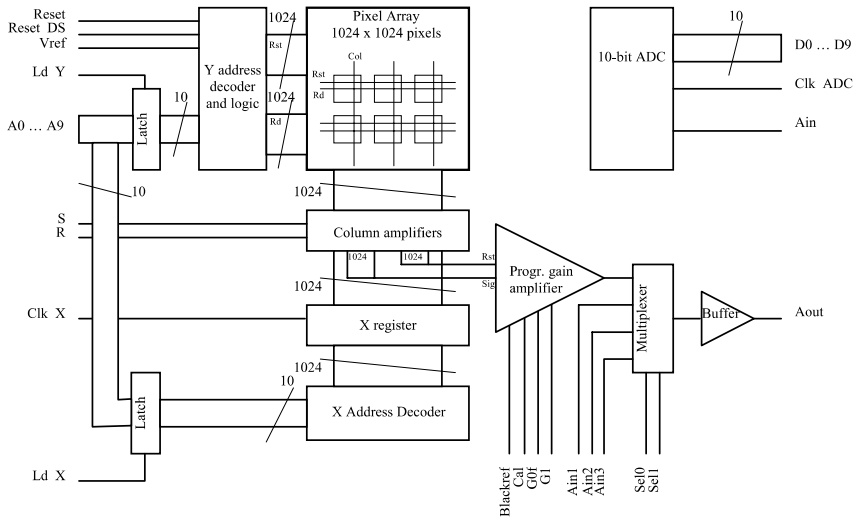

FIGURE 4-4 STAR 1000 INTERNAL BLOCK DIAGRAM

4.2.3.1. Signals

The power supply signals are as follow:

- VDDA: analog 5V supply.
- GNDA: analog ground.
- VDDD: digital 5V supply.
- GNDD: digital ground.

All power supply signals for the internal ADC are connected to the ground via a 100 KΩ resistance. All high-level supply pins have a 100 nF type-II capacitor and a 1 nF type-I capacitor connected.

The input signals are the following:

- A0 to A9: bus with the column (X) or row (Y) to read. A9 is the LSB and A0 the MSB.
- LD_Y: acquisition signal of the row latch. The steady state of this signal is set to 5 V by the FPGA.
- LD_X: acquisition signal of the column latch. The steady state of this signal is set to 5 V by the FPGA.
- RESET: signal to reset a row. It's used to control the integration time of the sensor.
- RESET_DS: signal used for dual slope integration. As it's not used, it's connected to ground.
- G1 and G0: signals to select the analog gain of the output. G1 is the MSB. The analog gain value is shown in Table 4-1. This gain multiplies not only the pixel signal, also the BLACKREF and the dark offset voltage.

Value (G1 G0)	Analog gain
00	x1
01	x2
10	x3
11	x4

TABLE 4-1 ANALOG GAIN

- S and R: signals to control the row read.
- A_SEL1 and A_SEL0: signals controlling the output multiplexer, allowing to select between the STAR 1000 output and a 5 MHz test signal generated by the FPGA when in Test Working Mode.
- CLK_X: clock signal used for the column readout. At its rising edge, the selected pixel value is at the analog output. To prevent an internal damage of the sensor if the firmware hangs, it's connected with a 100 KΩ pull-up to VDDD. This clock is always enabled except when loading a row to the column amplifiers,
- CAL: calibration signal. Used to have at the analog output the BLACKREF voltage.
- BLACKREF: 1.5V offset added to the analog output, used to ensure the output amplifier works in the lineal region. This voltage level is generated from an LM4050-2.5V voltage reference and a voltage divider. To ensure that this signal has enough current, a RH1078M in follower configuration is put between the voltage divider and the BLACKREF input.
- VREF and VRES: logic level for the reset signal and the dual slope reset, both are connected to VDDD with two capacitors each (one type-I 1 nF capacitor and a 100 nF capacitor). These signals are used as voltage reference of the pixel matrix.
- GND_AB: anti-blooming drain control voltage. It is applied 1 V for improved anti-blooming with a voltage divider and two capacitors (470 nF and 10 nF).
- NBIAS_DEC and NBIAS_OAMP: polarization voltages connected with a 100 KΩ to VDDA and a 100 nF capacitor as indicated by the datasheet.
- NBIAS_ARRAY: polarization voltage connected with a 1 MΩ to the VDDA and a 100 nF capacitor as indicated by the datasheet.
- PBIAS and PBIASDIG2: polarization voltage connected with 20 KΩ to GNDA and a 100 nF capacitor as indicated by the datasheet.

All electro-optical evaluation signals are connected with a 100 KΩ pull down.

4.2.3.2. Analog output

The analog output of the STAR 1000 comes from the addition of three voltages:

- Pixel value: has a range of 0 V to maximum 1.24 V. It's the signal range of interest.
- Dark reference offset: has a range from 0 V to maximum 0.93 V. This value will change with temperature and aging of the sensor.
- BLACKREF: is fixed to 1.5 V to ensure the internal output amplifier is always in the lineal working region.

With these values, the analog output range of the STAR 1000 goes from 1.5 V to 3.67 V. These values take into account the output change from temperature and device aging. Therefore, even in the expected worst conditions, the output of the image sensor will be in the operational range of the ADC.

4.3. Analog Chain

The analog output of the STAR 1000 has 100 Ω output impedance and is current limited during the transition of pixels. For this, a high bandwidth operational amplifier in follower configuration is used behind the sensor (AD8041S). Then, the analog single ended signal

is transformed to differential with a fully differential amplifier (AD8138A). This allows archiving a better SNR. This signal is finally fed into the ADC (Figure 4-5).

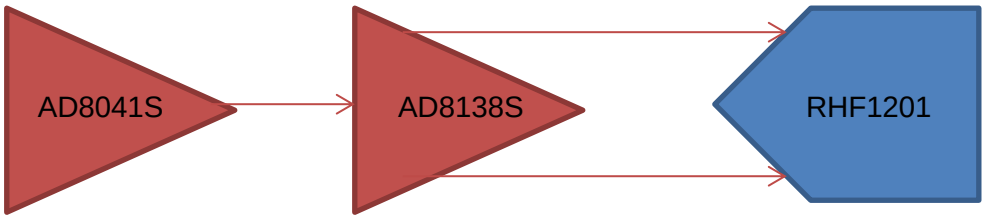

FIGURE 4-5 ANALOG CHAIN ADAPTATION OF THE STAR 1000 OUTPUT

4.3.1. Voltage follower

The AD8041S is a 160 MHz GBW rail-to-rail low noise amplifier. It adds a maximum offset of 8 mV to the signal. This signal is fed in the fully differential stage through the V_{IN-} input.

4.3.2. Voltage reference

To compensate the offset and have a more symmetrical differential signal, a 2.5 V voltage reference is used. This signal is fed in the fully differential stage through the V_{IN+} input.

4.3.3. Fully differential amplifier

The AD8138A is a fully differential amplifier used to drive the ADC. Its function is to convert the single-ended signal to differential, in the appropriate margins for the ADC. The preferred configuration is analysed in section 4.4.

4.3.4. Image ADC

The RHF1201 is a 12 bit [CTC-R-264] low consumption ADC that allows up to 50 Msps. A maximum rate of 7 Msps will be used. The ADC conversion has a 5.5 clock cycles delay between the analog input and the digital output.

4.3.4.1. Signals

- VIN and VINB: differential analog inputs. Its working range is between -0.2 V and 1.6 V. The full-scale input is set to 2 Vpp.
- INCM: input common mode of the differential input. It's used as an output from the RHF1201 to the AD8138S.
- VREFM: lower reference voltage. It is tied to the analog ground.
- VREFP: upper reference voltage. It can be externally forced between 0.5 V and 1.4 V or used its internal value between 0.79 V and 1.16 V. To improve the SNR, this voltage is externally forced to 1 V. This is done with a voltage divider from the LM4050-2.5. Between the input and the voltage divider, the circuit shown in Figure 4-6 is used. This circuit is used because a voltage follower has proven not to be sufficient since it is not able to give enough instantaneous current, producing oscillations on the VREFP signal.

- CLK: 10 MHz input clock signal [CTC-R-261]. With the rising edge of this signal a conversion starts. This signal is not 3.3V compatible; therefore a voltage divider is put between the FPGA output and the RHF1201 input.
- OE (output enable): digital input. When set to high level the output is set to high impedance. It's tied to the digital ground with a 10 KΩ resistance.
- Data Ready (DR): digital output. This output is a delayed copy of the CLK signal with its rising edge synchronized with the most stable point of the digital output.
- D11 (MSB) to D0 (LSB): digital output value.
- DFSB (Data Format Select): digital input. When set to a low level, the output is the two's complement of the digital value. When set to high level it provides a standard binary output. It is set to high level. It's tied to the 2.5 V power supply with a 10 KΩ resistance.

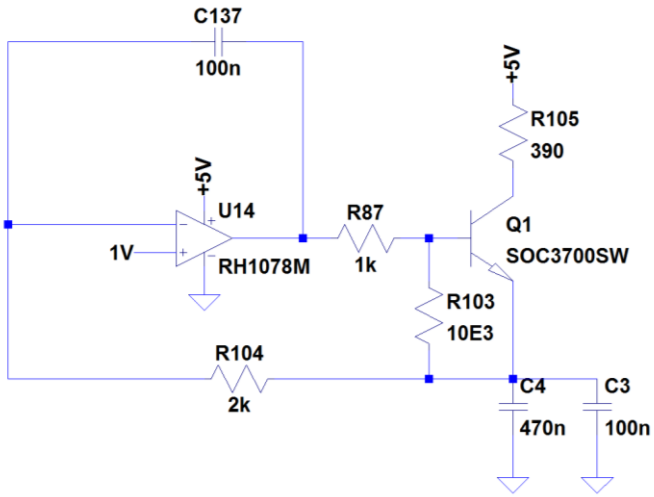

FIGURE 4-6 VREFP CIRCUIT

- SRC (Slew Rate Control): digital input. When set to high level the output current is limited, reducing the digital noise but increasing the fall and rise time. It's tied to the digital ground with a 10 KΩ resistance.
- VCCBE and VCCBI: power supplies of the digitals output buffers. Both of them are connected to the 2.5 V power supply.
- GNDBI and GNDBE: digital grounds of the output buffers. They're connected to the digital ground.
- AVCC: analog power supply, 2.5 V.
- AGND: analog ground. It is connected to the analog ground.
- IPOL: analog polarization current. To optimize power consumption around 10 Msps it is connected with a pull down of 91 KΩ to the analog ground.

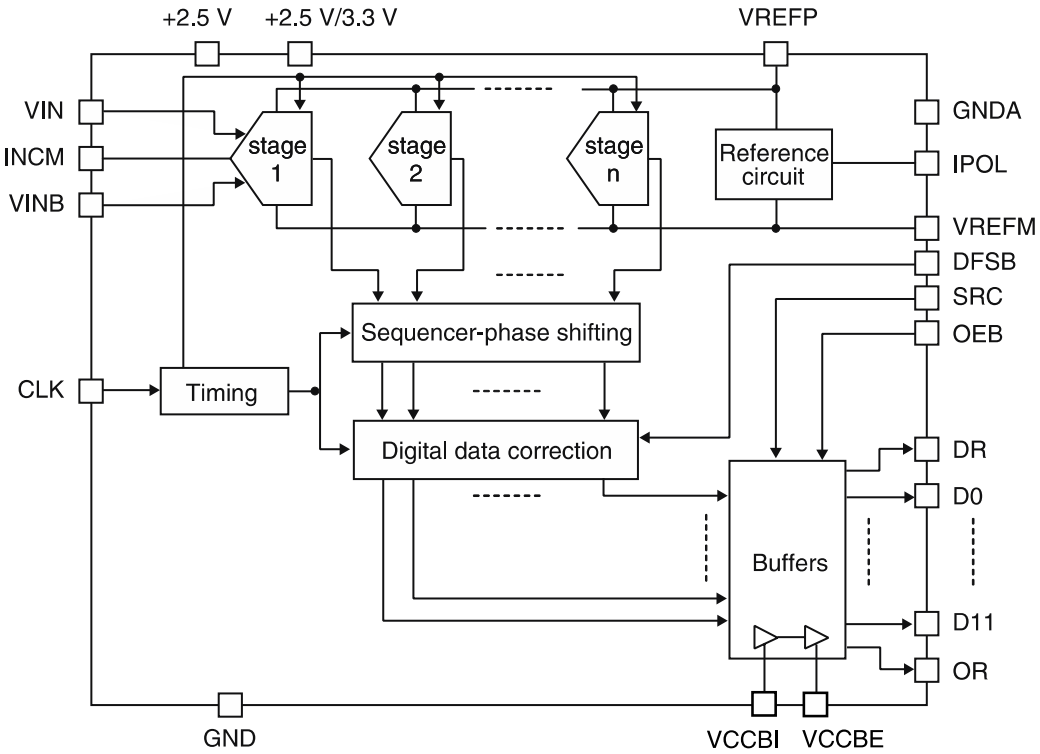

FIGURE 4-7 RHF1201 BLOCK DIAGRAM

- DVCC: digital power supply. It is connected to 2.5 V.
- DGND: digital ground.

4.3.5. H/K ADC

The ADC128S102QML is a 12-bit SAR ADC with 8 analog inputs, low power consumption and 1 Msps. The data transfer and control with the FPGA is done via an SPI link. The following H/K data is measured [CTC-R-250]:

- Temperature of the STAR 1000 and the FPGA: this is done via two ISL71590SEH (temperature transducers). To compensate the temperature offset the temperature transducer is connected to -5 V.
- Voltage reference 2.5 V and 1V signal: used for calibration. The 2.5 V signal comes from an LM4050-2.5V voltage reference and the 1 V signal from a voltage divider from the same voltage reference.
- Power supplies: the analog power supplies of -5 V and 2.5 V and the digital power supplies of 5 V and 3.3 V are also measured.

Pin	Signal	Pin	Signal
IN0	-5 V analog	**IN4**	3.3 V analog
IN1	2.5 V analog	**IN5**	5 V digital
IN2	STAR 1000 temp	**IN6**	1 V reference
IN3	FPGA temp	**IN7**	2.5 V reference

TABLE 4-2 H/K DATA

4.3.6. H/K ADC values conversion to physical values

1. First, all the H/K ADC values are read. The ADC value of the reference voltage more similar to the expected one is selected. From this value, using eq. (**1** the real value of the 3.3 V power supply is calculated. This voltage corresponds to the reference voltage of the H/K ADC.

$$V_{3V3} = V_{ref\ Voltage} \frac{2^{10}}{ADC_{ref\ voltage}} \quad \textbf{(1)}$$

2. Knowing the reference voltage value, we calculate the voltage at the input of the different ADC input channels using eq. (**2**.

$$V_{INX} = ADC_{INX} \frac{V_{3V3}}{2^{10}} \quad \textbf{(2)}$$

3. If we suppose that no current is flowing in to the H/K ADC and only through the resistors, the following equations can be used to known the power supplies voltage:

$$V_{-5V} = \frac{V_{IN0} - V_{3V3} R_P}{1 - R_P}; R_P = \frac{R_{33}}{R_{34} + R_{33}} \quad \textbf{(3)}$$

$$V_{2.5V} = V_{IN1} \frac{R_{29} + R_{30}}{R_{30}} \quad \textbf{(4)}$$

$$T_{STAR\ 1000} = \frac{V_{3V3} - V_{IN2}}{R_{25} I_{Temp\ Sensor}} - 273.15\ [ºC] \quad \textbf{(5)}$$

$$T_{FPGA} = \frac{V_{3V3} - V_{IN3}}{R_{26} I_{Temp\ Sensor}} - 273.15\ [ºC] \quad \textbf{(6)}$$

$$V_{5Va} = V_{IN4} \frac{R_{27} + R_{28}}{R_{28}} \quad \textbf{(7)}$$

$$V_{5Vd} = V_{IN5} \frac{R_{57} + R_{56}}{R_{56}} \quad \textbf{(8)}$$

4.4. Analog chain analysis

The analog circuitry of the CTC converts the single-ended analog output signal from the STAR 1000 sensor to a differential signal in the operational range of the ADC.

4.4.1. STAR 1000 analog output

The output of the STAR 1000 consists of the sum of three signals:

- BLACKREF: external DC signal set to 1.5 V with a voltage divider from a voltage reference (LM4050-2.5V). This signal exists to add a DC level to the output to ensure that the internal output amplifier of the STAR 1000 works in the lineal region. The voltage of 1.5 V is used, as recommended by OnSemi to obtain a very good image quality and to ensure the correct biasing of the internal logic.

- Dark reference offset: internal DC level in the range from a few hundred millivolts to 0.93 V. This signal changes with aging and temperature but, from datasheet data, it will be always in this range.
- Pixel voltage output: internal AC signal in the range from 0 V to 1.24 V. This signal is the one containing the information about the pixel illumination.

In summary, the analog output of the STAR 1000 will be between 1.5 V and 3.67 V, with a minimum of 0.99 V of useful information. This means that at least 0.93 V (maximum of the dark reference offset) of input range is not used. But with this we can ensure that the output of the STAR 1000 sensor will be in range of the analog chain, independently of the working temperature of the sensor or other degradations that can appear. The pixel readout frequency is 10 MHz.

4.4.2. Voltage follower

The AD8041 is used as voltage follower for the inputs of the differential stage. This is done because the output impedance of the STAR 1000 analog output is high and with the voltage follower we ensure the correct isolation of the signal from the sensor and the differential stage.

The AD8041 is a rail-to-rail amplifier with a 160 MHz cutoff frequency and adds only a maximum of 8 mV of offset voltage.

4.4.3. Fully differential Amplifier

The circuit of the fully differential stage is represented in Figure 4-8.

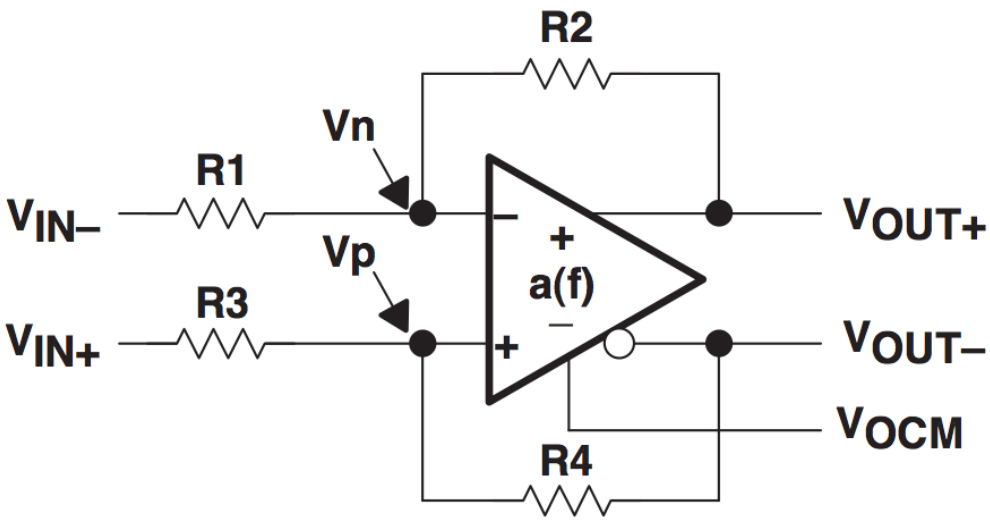

FIGURE 4-8 FULLY DIFFERENTIAL STAGE

We use the fully differential amplifier in balanced mode (R1=R3 and R2=R4) as noise immunity is greater and the behaviour is less temperature dependent.

In this case, the following variable is defined (equation 9):

$$\beta = \frac{R_1}{R_1 + R_2} = \frac{R_3}{R_3 + R_4} \quad \textbf{(9)}$$

With these change, the voltage at the outputs of the differential stage results in equation 10.

$$V_{OUT+} = \frac{(V_{IN+} - V_{IN-})(1-\beta)}{2\beta} + V_{OCM}$$

$$V_{OUT-} = \frac{(V_{IN-} - V_{IN+})(1-\beta)}{2\beta} + V_{OCM} \quad \textbf{(10)}$$

And the differential voltage between them is (equation 11):

$$V_{OD} = V_{OUT+} - V_{OUT-} = (V_{IN+} - V_{IN-})\frac{(1-\beta)}{\beta} \quad \textbf{(11)}$$

With these equations in mind, the following conditions must be met:

- The operating range of the ADC differential inputs is from -0.2 V to 1.6 V.
- The differential signal peak-to-peak value must be less than 2*(VREFP-VREFM). With VREFM set to ground and VREFP to 1 V with a resistive divider from an external voltage reference (LM4050-2.5V), this means the differential signal maximum peak-to-peak value is 2 V. The VREFP signal is set to 1 V since the ADC datasheet [13] recommends this value as it gives the best SNR. The internal voltage reference is not used because it is more temperature dependent as the LM4050 voltage reference.
- The common mode voltage (V_{OCM}) is generated internally in the ADC and is in the range from 0.4 V to 0.67 V [13].
- The V_{IN-} working range value goes from 1.5 V to 3.67 V, although the absolute maximum value can rise up to 4.5 V. This is because when increasing the programmable analog gain of the sensor, the internal output amplifier from the sensor gets the maximum output voltage limits.
- We need at least 8 bits of resolution [CTC-R-265]. This issue is discussed in chapter 4.5.
- The fully differential amplifier recommends using R_1 and R_3 equal to 499 Ω.

They are only two degrees of freedom: the V_{IN+} and the feedback resistance (since we're working in symmetric configuration R_2=R_4). The maximum signal amplification is achieved when the output voltage is fully symmetrical. This can be done changing V_{IN+} or BLACKREF. The V_{IN+} value is set with a voltage reference at 2.5 V. There is no other voltage reference available for the CTC working conditions (power supplies and radiation conditions) than the LM4050-2.5V. Using directly a voltage reference ensures the high instantaneous current needed with a very low noise, low temperature dependency and low power consumption in front of the voltage divider solution. But, for a BLACKREF value of 1.5 V the ideal V_{IN+} value is 2.585 V. This is not possible for the CTC, since it will require a voltage reference higher than 2.5 V.

The other solution is to lower the BLACKREF value to 1.415 V. This will allows us to increase the feedback resistances. In the most favourable case, this change will increase the useful range of the digital output (the range corresponding to the analog pixel value without the dark reference offset) from the actual 537 to 585, an increment of 48 symbols

(9%). This solution will be tested in the future with the entire optical setup since it can affect the sensor behaviour. For this reason, the baseline will be keep as 1.5 V.

With these values and from equation 11, selecting $R_2 = R_4 = 422\ \Omega$ allows the maximum possible voltage output range. The differential output, which is independent from the common mode voltage, goes from 0.846 V to -0.989 V. This gives a peak-to-peak differential output from 1.835 V.

The theoretical output is shown in Table 4-3 for the datasheet range of the common mode signal. Notice that in all possible cases all the voltages are in the operative range of the ADC, independently of the dark reference offset of the sensor or the ADC internal common mode voltage reference.

V_{OCM} (V)		**0.4**		**0.52**		**0.67**
V_{OUT+} (V)	0.823	-0.095	0.943	0.025	1.093	0.175
V_{OUT-} (V)	-0.023	0.895	0.097	1.015	0.248	1.165

TABLE 4-3 DIFFERENTIAL OUTPUT VOLTAGE RANGE

If the output of the sensor goes up to 4.5 V, the output to the ADC is below the absolute maximum values, but out of the operative range. This ensures if the analog gain is set to a wrong value and the sensor output goes to its maximum value, the signal to the ADC will be out range but no permanent damage will be done to it.

4.5. Noise analysis

4.5.1. Conditions

- The most relevant noise source is temperature. In this sense, only the thermal noise will be considered for the passive components. For active components, the total noise near 65º [CTC-R-241] will be taken if specified by the datasheet. If this condition is not found, worst temperature conditions will be used.
- Any parasitic capacitance will act as a low pass filter reducing noise, so the following calculus will be a worst case.
- We consider that all noise present at the BLACKREF pin of the STAR 1000 will be also present at the analogue output of the sensor.
- Noise at the common mode input of the fully differential driver is not relevant in balanced mode, as it doesn't add differential noise at the output.
- Noise coming from the power supplies is not taken into account. The power supply requirements are set from the results of this analysis in order that the noise coming from them allows the design to meet the 8 ENOB requirement [CTC-R-265].

4.5.2. Basic noise Equation

The main noise equations are:

- Resistance: Every resistance acts like a noise source following equation 12 power spectral density.

$$\overline{v_n^2} = 4\, k_B T\, R \qquad \textbf{(12)}$$

- Capacitor: A capacitor acts as a low-pass filter and so it reduces noise. Equation 13 shows the power spectral density of thermal noise in a simple RC network.

$$\overline{v_n^2} = \frac{k_B T}{C} \quad \textbf{(13)}$$

For this analysis, we will take into account the root mean square (RMS) of the voltage noise. The conversion is done with equation 14, where Δf refers to the equivalent noise bandwidth of the system.

$$v_n = \sqrt{v_n^2 \, \Delta f} \quad \textbf{(14)}$$

For the equivalent noise bandwidth (ENB) of the different subsystems we use a simple one-pole low pass filter, as it's the worst-case model. The equivalent noise bandwidth of a one-pole low pass filter is shown in equation 15. The used cut-off frequency will be of 10 MHz as it's the image sampling frequency or the cut-off frequency of the circuit, whichever is the smaller.

$$\Delta f = 1.57 \, f_{3dB} \quad \textbf{(15)}$$

The addition of different RMS noise sources, as they're Gaussian and uncorrelated, is done with a sum of squares, as shown in equation 16.

$$v_n = \sqrt{v_{n1}^2 + .. + v_{ni}^2} \quad \textbf{(16)}$$

4.5.3. Noise at the analog circuitry

4.5.3.1. RH1078M output noise

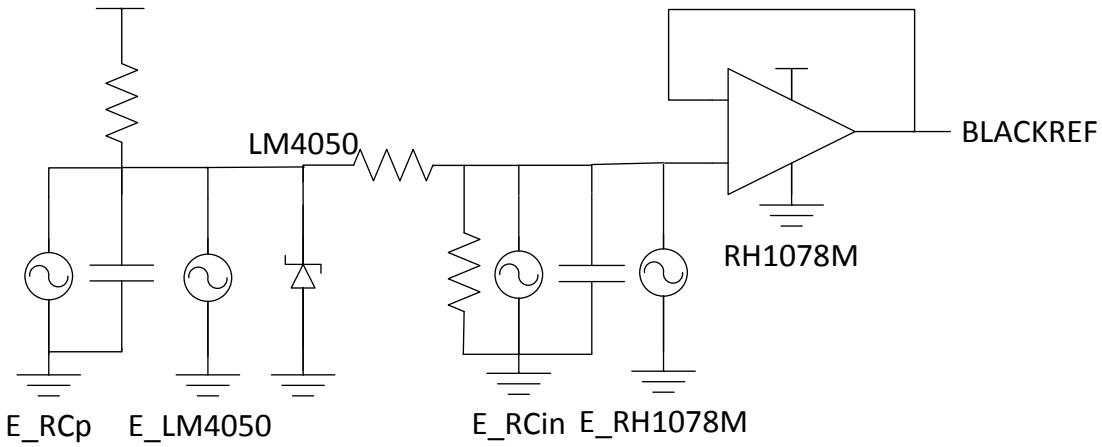

FIGURE 4-9 BLACKREF INPUT NOISE

The bandwidth of the RH1078M is 200 KHz and with equation 15 we find an ENB of 306 KHz.

The noise sources at the BLACKREF input are:

- LM4050: this part adds 50 µV, but the voltage divider reduces this noise to 24.6 µV RMS voltage noise.
- R-Cp: the 2KΩ resistor and the three capacitor with a total capacitance of 570 nF add a noise of 30 µV using equation 13 and taking into account the ENB of 21 Hz from the subsequent RC.
- R-Cin: the voltage divider and the capacitance of 3.9 nF adds a total noise of 605 µV.
- RH1078M: the RH1078M has an input voltage noise density of 25 nV/√Hz, which leads to a total input noise of 14 µV.

Noise Source	RMS Noise Voltage (µV)
LM4050	30
R-Cp	30
R-Cin	605
RH1078M Input	14

TABLE 4-4 BLACKREF NOISE SOURCES

From these values and equation 16 we find that the total noise at the RH1078M output is 607 µV.

4.5.4. IN- input noise

The noise sources at the input of the AD8041 are:

- Blackref input noise: the blackref input is connected directly to the RH1078M output and so the RMS voltage noise present at blackref is 607 µV.
- STAR 1000 output noise: the datasheet specifies a 2.37 mV RMS voltage noise for a temperature of 85 ºC and a 10 MHz clock rate and 1.13 mV RMS voltage noise for a temperature of 25 ºC. Since the noise depends linearly with temperature, the supposed noise at 65 ºC results in 1.96 mV of RMS voltage noise.
- AD8041: the AD8041 has an input voltage noise density of 16 nV/√Hz, which leads to a total input noise of 63 µV. No information of how the input voltage noise density changes with temperature or radiation is present in the datasheet.

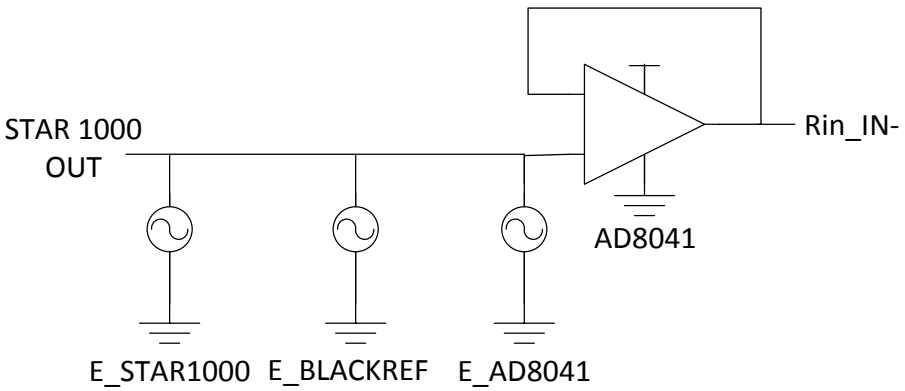

FIGURE 4-10 IN- INPUT NOISE

Noise Source	RMS Noise Voltage (µV)
BLACKREF	460
STAR 1000	1957
AD8041 Input	63

TABLE 4-5 IN- INPUT NOISE

From these values and equation 16 we find that the total noise at the RH1078M output is 2.050 mV.

4.5.5. IN+ input noise

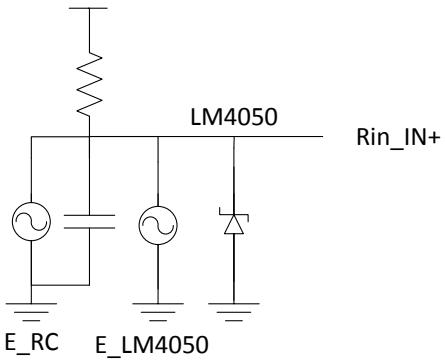

FIGURE 4-11 IN+ INPUT NOISE

The noise sources at the input of the AD8041 are:

- LM4050-2.5: 50 µV RMS voltage noise.
- RC: the 1KΩ and the two capacitor with a total capacitance of 571.5 nF generate a noise of 24 µV using equation 13 and taking into account that the ENB is set by the 10 MHz sampling frequency.

Noise Source	RMS Noise Voltage (µV)
LM4050-2.5	50
RC	24

TABLE 4-6 IN+ INPUT NOISE

From this values and equation 16 we find that the total noise at the RH1078M output is 55 µV.

4.5.5.1. AD8138

The bandwidth of the AD8138 used is 10 MHz, since it's the sampling frequency of the ADC.

The following noise sources exist in the fully differential amplifier stage:

- The four resistances contribute with thermal noise following equation 12.

- The input current noise density of the AD8138 (2 pA/√Hz) generates a voltage noise due the presence of the resistances. The total resistance seen by this current source is shown in equation 17, with $R_i = R_1 = R_3$ and $R_f = R_2 = R_4$.

$$R_{eq} = \frac{R_i R_f}{R_i + R_f} \quad \textbf{(17)}$$

- The voltage noise at the output of the two AD8041 is amplified in this stage in a factor of $1+R_i/R_f$ = 1.85
- The input voltage noise density of the AD8138 (5 nV/√Hz).
- The presence of the two series resistance at the output also generates thermal noise following equation 12.
- As the fully differential amplifier is used in balanced mode, the noise at the common mode input doesn't generate any differential noise at the output.

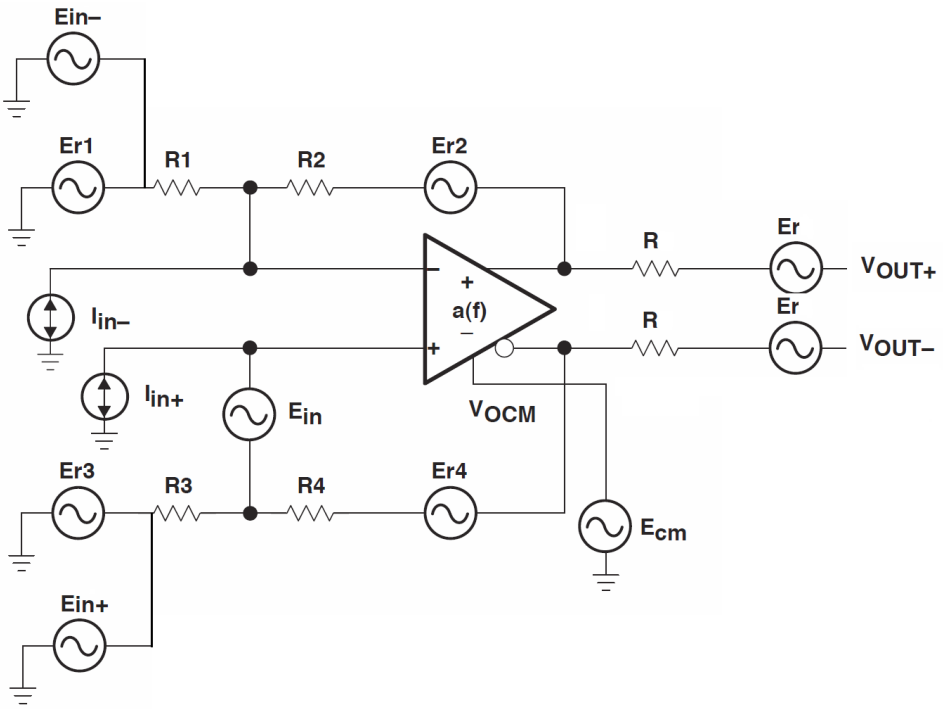

FIGURE 4-12 FULLY DIFFERENTIAL AMPLIFIER

The values of the generated noise are shown in Table 4-7.

Using again equation 16 we find a total differential noise at the analog output of 3.783 mV. This is equivalent to 443 electrons from the sensor, and using the 30% quantum efficiency of the STAR 1000, this represents a total of 1478 photons.

Noise Source	RMS Noise Voltage (µV)
R_{in}	12
R_f	11
Input current noise	8
Input voltage noise	20
R_{ser}	4

IN- Noise	2050
IN+ Noise	55

TABLE 4-7 FULLY DIFFERENTIAL AMPLIFIER OUTPUT NOISE

4.5.6. Noise at the Analog-to-Digital Converter

The full-scale voltage of the RHF1201 is set to 2 V peak to peak and the minimum SNR (Signal to Noise Ratio) with an input signal of 15 MHz is 58 dB. With these values and equation 18 we find that the ADC adds 2.244 mV RMS voltage noise.

$$SNR = 20\log\left(\frac{Signal_{RMS}}{Noise_{RMS}}\right) \quad \textbf{(18)}$$

So, the total noise of the system is 4.103 mV and the total SNR is 43.186 dB. This noise is equivalent to 9 DNs at the ADC and taking in to account a quantum efficiency of 30% and an electron to DN conversion factor of 55.43 e^-/DNs, this is equivalent to a total of 1663 photons at the sensor.

Then, taking into account the maximum total harmonic distortion (THD) of 64 dB with a 15 MHz input signal, we find with equation 19 a value of SINAD (Signal to Noise and harmonic distortion ratio [IR03]) of 43.150 dB. Since the sampling frequency is low (10 MHz), the contribution of the harmonic distortion is irrelevant as expected.

$$SINAD = -10\log\left(10^{-SNR/10} + 10^{-THD/10}\right) \quad \textbf{(19)}$$

Finally, the SINAD allows us to find the ENOB (Effective Number Of Bits) with equation 20.

$$ENOB = \frac{SINAD - 1.76\ dB - 20\log(Input\ Amplitude/Full\ Scale\ Amplitude)}{6.02} \quad \textbf{(20)}$$

So, the resulting ENOB for input signal amplitude of 0.99 V (minimum of the saturation voltage of the STAR 1000) is 8.13 bits.

4.5.7. Conclusions

In the worst case, we have 8.13 bits of effective resolution. The analysis also shows that the most significant source of noise, making almost irrelevant all the others, is the STAR 1000 itself. This noise can only be lowered reducing the noise gain of the differential stage at the expense of reducing the differential output gain and so at the end a worst signal to noise ratio can be achieved.

4.6. Power supply

All supplies are provided by the CPC. The power supply interface is defined in section 2.

4.6.1. CPC harness

The harness to the CPC and the connector used are defined in section 2 .

4.6.2. Power supplies requirements

The only power supply critical from the noise point of view is the 5 V supply. This is due to the image sensor. The STAR 1000 uses the power supply as voltage reference for the pixel reset and readout. This makes that any noise present at the 5 V power supply will be also present at the pixel voltage.

4.6.2.1. +5V

4.6.2.1.1. Nominal value

The recommended power supply for the +5V devices is shown at Table 4-8.

Device	Min (V)	Max (V)
STAR 1000	-	5.5
54AC164245	4.5	5.5

TABLE 4-8 RECOMMENDED OPERATIVE CONDITIONS FOR THE +5V POWER SUPPLY

Also, the recommended value for the AD8041S and is AD8138S is 5 V but no recommended operating conditions are found at the datasheet. Therefore, using a 5% margin, the needed nominal values should be between 4.75 V and 5.25 V.

4.6.2.1.2. Ripple

Table 4-9 shows the PSRR of the different components using the +5V power supply.

Component	PSRR (dB)
AD8041S	68
AD8138A	50
RH1078M	100
STAR 1000	1

TABLE 4-9 +5V COMPONENTS PSRR

Due to the absent of PSRR at the STAR 1000, this is the only component taken into account for the allowed ripple calculus at +5V. From the Noise analysis at section 4.5, we found that the maximum noise allowed at the STAR 1000 to achieve an ENOB of 8 is 2.2 mV. Since the internal noise of the sensor and the noise from the power supply coming through the sensor are supposed to be uncorrelated, the addition of the total noise is done by the sum of squares. With a worst case noise of the STAR 1000 of 1.96 mV, the maximum allowed ripple at the power supply is 1 mV. This value is not frequency dependent from the electronics side, but from the image correlation. Since the renewal of the reference image is done at 1 Hz, the 1 mV ripple should be lower than this frequency.

4.6.2.2. –5V

4.6.2.2.1. Nominal value

No precise value is required for the AD8138S. Taking in to account derating of this component, this value is increased with two diodes to near - 3.6 V.

4.6.2.2.2. Ripple

Taking into account the 50 dB PSRR, the maximum ripple allowed is 0.59 Vrms. But, to ensure the power supply voltage is always near the operative voltage, the limit for the ripple is set to a 5%, 0.25 Vrms.

4.6.2.3. 3.3 V

4.6.2.3.1. Nominal value

The operative range for the 3.3V devices are shown in Table 4-10.

Device	Min (V)	Max (V)
54AC164245	2.3	3.6
UT54LVDS031LVE	3.0	3.6
UT54LVDS032LVE	3.0	3.6
RHF1201	3	3.4
ADC128S102QML	2.7	3.6
RT54SX72S	3.0	3.6

TABLE 4-10 RECOMMENDED OPERATIVE CONDITIONS FOR THE 3.3 V POWER SUPPLY

From the previous table the nominal value range is from 3.0 V to 3.6 V, but for lower delays at the FPGA a nominal value range from 3.15 V to 3.45 V is needed.

4.6.2.3.2. Ripple

Since this voltage doesn't affect the analog chain of the sensor, no special severe requirements exist for this voltage. Therefore, the maximum ripple is required to ensure that the voltage is always in the operative range of the devices. Hence, the maximum ripple should be lower than 0.15 Vrms.

4.6.2.4. 2.5 V

4.6.2.4.1. Nominal value

The recommended power supply for the 2.5V devices is shown in Table 4-11.

Device	Min (V)	Max (V)
RHF1201	2.3	2.7
RT54SX72S	2.25	2.75

TABLE 4-11 RECOMMENDED OPERATIVE CONDITIONS FOR THE 2.5 V POWER SUPPLY

From the previous table the nominal value range is from 2.3 V to 2.7 V, but for better timing characteristics at the FPGA a nominal value range from 2.35 V to 2.65 V is needed.

4.6.2.4.2. Ripple

The RHF1201 PSRR is 93 dB and therefore ripple at this voltage is not relevant for the analog chain noise. So, the maximum ripple is required to ensure that the voltage is

always in the operative range of the devices. Hence, the maximum ripple should be lower than 0.15 Vrms.

4.6.2.5. Summary of the power supply requirements

Table 4-12 summarizes the previous requirements.

Supply	DC Min (V)	DC Max (V)	Ripple (mVrms)
+ 5 V	4.75	5.25	1
- 5 V	-3.40	-3.80	250
+ 3.3 V	3.15	3.45	150
+ 2.5 V	2.35	2.65	150

TABLE 4-12 POWER SUPPLY REQUIREMENTS

4.6.3. Pi filter

Since the maximum ripple allowable at the +5V power supply is 1 mVrms and the ripple provided by the CPC is 4 mVrms @ 600 KHz, a filter is needed. The minimum attenuation of this filter at 610 KHz must be 12 dB. This can be achieved with a simple pi filter consisting of two capacitors and one inductance as shown in Figure 4-13.

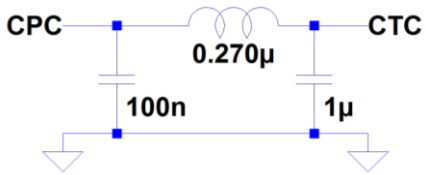

FIGURE 4-13 PI FILTER

The inductor used is the MS21423-18 with 0.270 µH, Q minimum of 80, SRF minimum frequency of 280 MHz and maximum DCR of 0.10 Ω. The input capacitance is a type-I 100 nF ceramic capacitor and the output capacitor is a type-II 1 µF ceramic capacitor. With this pi filter, the common mode choke and the expected output load of the +5V power supply, the expected attenuation at 610 KHz is 29 dB (Figure 4-14).

From simulation it's also found that noise coming from the other power supplies can be an issue at the analog ground. This happens since the different power supplies share the same analog ground, splitted from the CPC ground via the common mode chokes, but above certain frequencies the common mode chokes seems to be not working anymore.

Therefore some measurements have been done at the laboratory, but without the CPC it has not been possible to test if this will be a problem with the final power supply. For the commercial power supply used (ripple should be below 4.5 mV, similar to CPC) Table 4-13 shows the results of the different tests.

Parameter	Without filters, with capacitor between grounds	With filters, with capacitor between grounds	With filters, without capacitor between grounds	Without filters, without capacitor between grounds
Minimum ENOB	9.25	9.46	9.42	9.33

TABLE 4-13 PI FILTER TEST

From these results, the best signal quality is achieved with all the power supplies filtered and the capacitor placed between the analog and the digital ground.

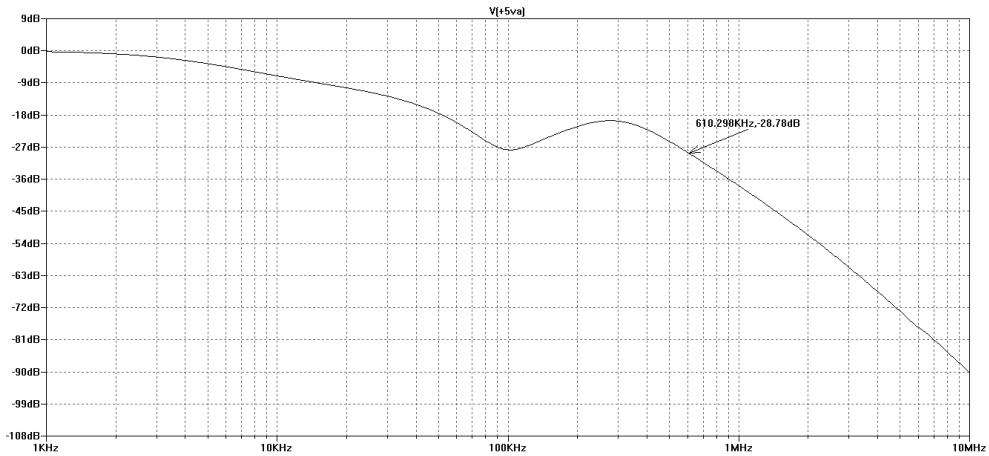

FIGURE 4-14 +5V ATTENUATION

4.6.4. Grounding

The ground of the CPC is splitted into analog ground and digital ground via the common mode chokes. This is done to reduce the noise between the digital signals and the analog electronics. The two grounds are connected through a 1 nF capacitor near the image ADC.

4.7. Power consumption

Three different cases have been studied for the power consumption: worst case (125 ºC), typical (25 ºC) and minimum. No safety margins have been added to the results.

- Worst case: worst case values are shown in Table 4-14. All values are the maximum from standard microcircuit drawings at 125 ºC, except for the STAR 1000 (datasheet maximum value at 85 ºC), for the FPGA (from Actel Power Calculator) and for the 54AC164245 and ADC128S102QML (from datasheet at 125 ºC). The dynamic currents are the maximum possible at continuous frame mode. The total power consumption in this case is 1.549 W.

Component	Voltage (V)	Quiescent Current (mA)	Dynamic Current (mA)	Total Power (mW)
STAR1000	5	13.9	0.0	69.5
AD8041S	5	6.1	4.0	50.5
AD8138S	5	24.0	0.5	122.5
AD8138A	-5	24.0	0.5	122.5
RH1078M	5	0.1	0.2	3.0
RHF1201	2.5	13.0	2.4	38.5
	2.5	60.0	0.0	150.0
UT54LVDS031LV/E	3.3	35.0	10.0	148.5
UT54LVDS032LV/E	3.3	15.0	3.0	59.4
54AC164245	5	0.2	0.0	2.1
	3.3	0.2	0.0	1.3
QT188LD9S-100MHz	3.3	40.0	2.0	138.6
RTSX72SU	3.3	10.6	0.9	37.9
	2.5	5.8	217.2	557.5
LM4050-2.5	5	1.0	3.0	20.0
LM4050-2.5	5	2.8	0.0	14.0
ADC128S102QML	3.3	0.0	1.5	5.0

TABLE 4-14 WORST CASE POWER CONSUMPTION

- Typical: typical values are shown in Table 4-15. All values are the typical found at datasheets at 25 ºC except for the FPGA, which values are obtained from the Actel power calculator. The total power consumption is 1.167 mW.

Component	Voltage (V)	Quiescent Current (mA)	Dynamic Current (mA)	Total Power (mW)
STAR1000	5	12.8	0.0	64.0
AD8041S	5	5.2	4.0	46.0
AD8138A	5	20.0	0.5	102.5
	-5	20.0	0.5	102.5
RH1078M	5	0.1	0.2	2.8
RHF1201	2.5	0.5	0.0	1.3
	2.5	18.0	2.4	51.0
UT54LVDS031LV/E	3.3	18.0	10.0	92.4
UT54LVDS032LV/E	3.3	15.0	3.0	59.4
54AC164245	5	0.0	0.0	0.3
	3.3	0.0	0.0	0.1
QT188LD9S-100MHz	3.3	30.0	2.0	105.6
RTSX72SU	3.3	7.0	0.5	24.8
	2.5	3.0	194.0	492.5
LM4050-2.5	5	1.0	0.0	5.0
	5	2.8	0.0	14.0
ADC128S102QML	3.3	0.0	0.9	3.0

TABLE 4-15 TYPICAL CASE POWER CONSUMPTION

- Minimum: minimum current consumptions are shown in Table 4-16. These are the minimum currents found at datasheets except for the FPGA, which values are obtained from the Actel power calculator. The dynamic current is the minimum possible for the design. The total power consumption is 1017 mW.

Component	Voltage (V)	Quiescent Current (mA)	Dynamic Current (mA)	Total Power (mW)
STAR1000	5	12.8	0.0	64.0
AD8041S	5	5.2	0.6	29.0
AD8138A	5	18.0	0.1	90.4
	-5	18.0	0.1	90.4
RH1078M	5	0.1	0.2	2.8
RHF1201	2.5	0.5	0.0	1.7
	2.5	15.0	0.0	37.5
UT54LVDS031LV/E	3.3	18.0	0.1	59.7
UT54LVDS032LV/E	3.3	15.0	0.0	49.5
54AC164245	5	0.0	0.0	0.1
	3.3	0.0	0.0	0.1
QT188LD9S-100MHz	3.3	0.0	30.0	99.0
RTSX72SU	3.3	7.0	1.0	26.4
	2.5	3.0	176.0	447.5
LM4050-2.5	5	1.0	0.0	5.0
	5	2.8	0.0	13.8
ADC128S102QML	3.3	0.0	0.0	0.0

TABLE 4-16 MINIMUM POWER CONSUMPTION

Table 4-17 shows the currents needed from the different power supplies for the different cases.

	-5 V	2.5 V	3.3 V	5 V
Worst Case	25	299	121	56
Typical	21	218	86	47
Minimum	18	195	71	41

TABLE 4-17 CURRENT CONSUMPTION FOR THE DIFFERENT POWER SUPPLIES

Finally, Table 4-18 summarizes the different cases for the different elements of the CTC design.

	Worst Case (mW)	Typical (mW)	Minimum (mW)
CTC Detector	70	64	64
CTC Detector Board	524	325	271
CTC FPGA Board	955	778	682
Total	1549	1167	1017

TABLE 4-18 POWER CONSUMPTION OF THE DIFFERENT CASES

Using the values of the previous tables and doing a linear adjustment of the quiescent consumption, the following power consumptions for the PHI operational modes A and B are found (Table 4-19 , A1 and A2 and B1 and B2 are equivalent for the CTC).

Operational Mode	**A (A1 & A2)**		**B (B1 & B2)**	
	Operative temperature (ºC)	Average power (W)	Operative temperature (ºC)	Average power (W)
CTC Detector	56	0.070	-15	0.064
CTC Detector Board	80	0.430	14	0.308
CTC FPGA Board	79	0.833	8	0.756
Total		1.331		1.227

TABLE 4-19 POWER CONSUMPTION FOR THE DIFFERENT PHI OPERATIONAL MODES

4.8. Mass budget

The CTC consists of two boards: the CTC Detector Board, with a surface of 125 by 55 mm; and the CTC FPGA Board, with a surface of 80 by 60 mm. The two boards use a polyimide 8 layers stack up with a total thickness of 1.6 mm. The external layers have a copper thickness of 70 um and the internal of 35 um. For the copper a density of 8940 Kg/m^3 has been used and for the polyamide (Arlong 85N) a density of 1600 Kg/m^3. With these values, the mass of the boards is shown in Table 4-20.

Board	**Mass (g)**
CTC Detector Board	35
CTC Sensor Board	25

TABLE 4-20 CTC BOARDS MASS

The CTC mass is shown at Table 4-21 and is below the required 165g (CTC-R-230).

Part Number	Item	Q	Mass [g]	Total [g]
RTSX72SU	Actel FPGA	1	15.50	15.50
STAR1000	Image sensor	1	7.90	7.90
RHF1201	12bit ADC	1	2.50	2.50
AD8041S	Video amplifier	1	0.35	0.35
AD8138S	Fully differential amplifier	1	0.35	0.35
ADC128S102	ADC	1	0.70	0.70
UT54LVDS032	LVDS Receiver	1	0.70	0.70
UT54LVDS031	LVDS Transmitter	1	0.70	0.70
54AC164245	Level Shifter	2	0.70	1.40
CM103	Common-Mode Chokes	7	5.00	35.00
LM4050QML	Precision Micropower Shunt Voltage Reference	2	0.24	0.48
RH1078	OP-AMP	2	0.35	0.70
AD590	Temp. Sensor	2	1.20	2.40
SOC3700SW	NPN Transistor	1	0.03	0.03
QT188LD9	Oscillator	1	5.00	5.00
Tantalum Capacitor	Capacitor AVX TAJ-C	6	0.17	1.00
Tantalum Capacitor	Capacitor AVX TAJ-E	3	0.51	1.54
Resistors	R0603	1 12	0.00	0.22
Capacitors 0805	C0805	1 28	0.01	0.70
Capacitors 1206	C1206	1	0.01	0.01
Capacitors 1810	C1810	5	0.03	0.17
Omnetics 25 Plug	Connector: MNPO-25-VV-M-ETH	3	0.62	1.86
Omnetics 25 Socket	Connector: MNSO-25-VV-M-ETH	4	0.53	2.12
Micro-D 25 Socket	Connector: MDA225SBSPG1	1	5.50	5.50
PCB Board	(125mmx55mm)+(80mmx60mm), 8 layers	1	60.00	60.00
MS21423-18	Inductor	4	0.50	2.00
			Total	**148.83**

TABLE 4-21 MASS BUDGET

5. Firmware Development Plan

This section provides the overall Design, Development and Verification principles, approach and structure for the CT Camera FPGA design. This document includes in accordance with [11]:

- Documentation to be generated
- Development team and assignment of major responsibilities
- Identification of the baseline FPGA technology, device family and package.
- Verification and stimuli generation approach.
- Identification and versions of all design tools to be used.
- Identification of programming equipment.
- Design flow, e.g. for design description, logic synthesis, etc.
- Validation and verification approach.
- Specification of a configuration management system.
- Risks analysis and mitigation technics.

5.1. CT Camera FPGA Overview

The CT Camera FPGA controls the Image Sensor and the Analog to Digital Converter that reads the sensor signals. It also includes the interface between the CT Camera and the DPU, and the housekeeping acquisition.

5.1.1. Device selection

The FPGA device selected for managing the CT Camera functionalities is the Microsemi (Actel) RTSX72SU with speed grade -1 in CQFP208 package version. This device has been selected for the following reasons:

- Adequate number of I/O´s and low pinout dimension
- Robustness in radiation environment
- All register are TMR
- Low power consumption
- Extensive usage in space applications

5.1.2. Prototype solution

For prototyping the commercial equivalent part will be used, the A54SX72A with speed grade -1 and PQFP208 package version.

5.2. FPGA Design Flow

The CT Camera FPGA development shall follow the design flown shown in the Figure 5-1 in accordance with [11].

5.2.1. Definition phase

The goal of this activity is to define the CTC FPGA specifications. These specifications shall be documented within the FPGA Requirement Specifications. This document shall include a minimum set of items according to the [11] (sec 5.3 and Annex H), as:

- Definition of FPGA interfaces
- Power-up and initialization state

- Environmental constraints: thermal and radiation
- Physical constraints
- Functional requirements
- System configurations and operating modes
- Applicable algorithms
- Interface protocols

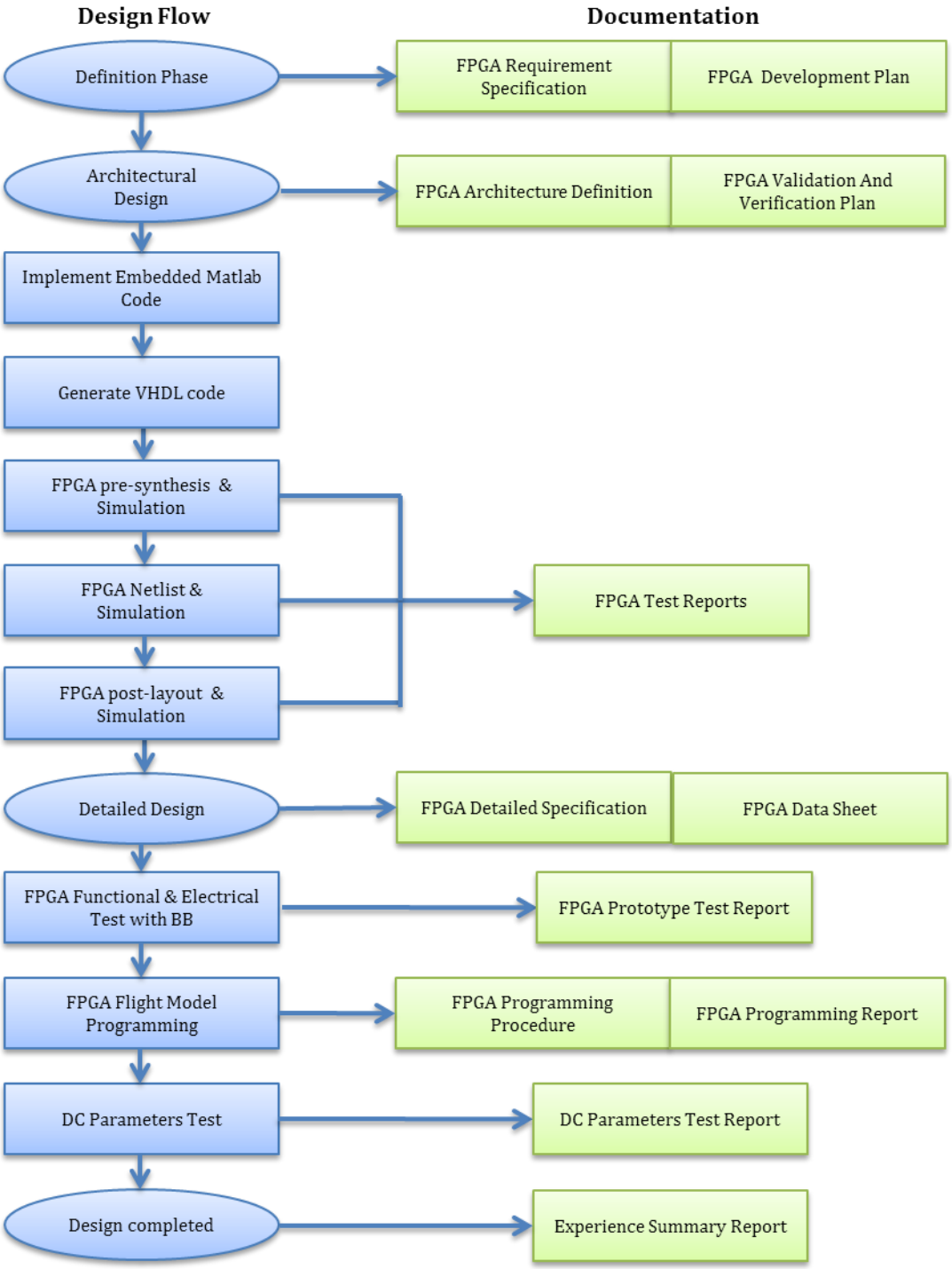

FIGURE 5-1. CT CAMERA FPGA DESIGN FLOW

5.2.2. Architectural design

The objective of this phase is to define the architectural definition and the verification and validation plan.

The architectural definition ([11] sec 5.4) shall include at least:

- Subdivide the design in blocks and identify their functionalities and interactions.
- Define the state machines and their transitions of the different blocks.
- Define the architecture down to the level required to fulfil the requirements.
- Identify asynchronous parts of the design.
- Select IP cores in case they are needed.
- Identify technology specific cells needed for the design.

The validation and verification plan ([11] Annex E and F) defines how the functional and non-functional requirements stated in the definition phase documentation are demonstrated at all levels of modelling (pre-synthesis, post-synthesis and post–layout and bread-board if required). The document shall describe the test to be performed and how these tests ensure the fulfilment of the requirements.

5.2.3. Implementation

The design will be made using Matlab, specifically with the Simulink tool. The description is made using a subset of the matlab language, to allow its automatic translation to VHDL. The only exceptions shall be I/O interfaces, clock distribution, reset and asynchronous signals. These shall be implemented directly in VHDL and be the top entity of the design. The matlab code will be automatically translated to VHDL and instantiated in the VHDL top entity.

Test benches and test vectors shall be also automatically generated from matlab. The VHDL code shall be tested against this test bench to ensure full code coverage. The code coverage report shall be included in the FPGA Test Reports document.

5.2.4. Synthesis

The goal of this phase is to generate the netlist from the VHDL code. Constrain file with the pin assignment and clock frequencies and a script for automatic synthesis shall be generated. The FSM codification shall not be changed by the synthesis tool and only replication for high fanout logic shall be performed. The generated netlist shall be tested with the prior generated test benches.

The synthesis log file and the simulation result shall be included in the FPGA Test Report document.

5.2.5. Place and Route

The goal of this phase is to obtain a programming file useful to burn the target FPGA. A TCL script shall be developed to automate this process. The following tasks should be performed:

- Ensure that the intended operating (die voltage, temperature margin, default I/O standard) and environment (radiation) conditions are considered during the translation process
- Pin-out distribution
- Generate the programming file

- Back-annotate VHDL

Once the previous steps have been done, it is important to make sure that the proposed design meets all requirements and timing constraints. To ensure this, the back-annotated VHDL file shall be tested with the test benches.

Also, the place and route log, status report, timing datasheet report and pin report shall be included in the FPGA Test Report document.

5.2.6. Detailed design

In this stage, the FPGA Data Sheet shall be generated. It shall contain ([11] Data sheet):

- Detailed interface descriptions and register definitions.
- System overview of the device and a description of how to use it.
- Functionalities and operating modes.
- All signals shall be described.
- All electrical relevant data and their applicable conditions (e.g. temperature and capacitive load), including:
  - Absolute maximum ratings
  - Timing constraints and static timing analysis
  - Power consumption estimations
  - Sequential and combinational cell usage
  - Package description and pin assignment

5.2.7. FPGA Functional & Electrical Test with BB

The requirements that need to be tested in the laboratory, because they cannot or shall not be tested by simulation, shall be tested during the CTC board test. The CTC Test Report shall include a section describing these tests and their results.

5.2.8. FPGA Flight Model Programming

The FPGA Flight Model Programming will be performed by SENER. They shall define a FPGA Programming Procedure document with the steps done for programming the flight FPGA and once programed a FPGA Programming Report with the necessary data to check the correct programming of the FPGA.

5.2.9. DC Parameters test

Since this FPGA has a long heritage in space applications, PPBI is no longer required [NR04]. Still, a DC parameters test against the SMD shall be performed by SERMA and a report shall be generated of this activity.

5.2.10. Design Completed

Once the design is completed, an experience summary report shall be generated. The experience summary report shall include ([11] Annex I) at least:

- A summary of the main design objectives and constraints.
- An assessment of the actual development plan with respect the original one.
- An assessment of the development tools used and their performance.
- A presentation of non-conformances and problem areas.

- Synthesis results, modelling, test stimuli, documentation and application support and problems encountered.
- Recommendation and lessons learned.

5.3. FPGA Development Tools

SW development tools:

- Libero Project Manager, Version: 9.1.5.1, Release: v9.1 SP5 from Actel
- Synthesis: Synplify Premier with Design Planner G-2012.09-SP1 from Synopsis
- Actel Designer 9.1.5.1 software from Actel
- Matlab R2013a from Mathworks with Simulink 8.1 and HDL Coder 3.2
- Questa Sim 10.1d

Development HW tools:

- FPGA programming: Silicon Sculptor 3 from Actel for A54SX72A-1PQG208I device (commercial RTSX) with SMAX-208CQ-ACTEL adapter module for the flight model and SMAX-208PQ-ACTEL adapter module for the breadboard model.
- CT Camera breadboard
- Monitoring the external outputs using logic analyser/ analog oscilloscope (Agilent MS06104A 1GHz Mixed Signal Oscilloscope).
- Subsystem test benches for interfacing with the CT Camera.

5.4. Configuration Management

All configuration items generated during the FPGA development shall be put under documentation control including:

- All schematics and VHDL files generated during the development
- All stimulus files and test benches used for verification
- All output logs obtained during verification, synthesis and place and routing.
- All scripts used for automatic runs of the development tools and the input files needed to run the scripts.
- All tools and FPGA libraries actually used during the design shall be also documented and archived.

5.4.1. Control change

All the change procedures involving any VHDL file or documentation shall follow the project change control procedures ([12]).

5.4.2. Configuration Item Data List

A configuration item data list (CIDL) shall be produced, listing all documentation that represents the “as design” configuration.

Per each model assembled in the CT Camera FPGA, an “as-build configuration list” shall be produced (ABCL), which on top of the configuration documentation lists the NCR and RFW and the FPGAs programming reports.

5.4.3. Marking

Every fused FPGA should be labelled with a number. A list should be maintained with the following information:

- Firmware generation date: yyyy-mm-dd
- Subversion version number of the VHDL code, the synthesis file and the firmware file.
- Model (flight, engineering)
- CI number

5.5. Risk Assessment

The Actel RTSX are widely used in space application since their radiation robustness, low power consumptions and high temperature tolerance. In this sense, no problems are expected with the environmental working conditions.

First estimations of the gate usage for the firmware show that around a 50% of the RTSX72SU will be used. This gives a lot of margin for unexpected changes during the development. Also, it's expected to use around 50 signals and since the number of pins of the FPGA is 208 the design can grow without problem.

The highest expected clock frequency is 100 MHz. From the data sheet the maximum expected achievable frequency is 230 MHz. Therefore, plenty of margin is also available from the frequency point of view.

6. CTC FPGA Requirement Specification

The CTC FPGA main function is to provide the correlation images for the ISS. The following functions must be performed by the FPGA:

- Control the image sensor and image ADC for image readout.
- Provide a register bank to change image readout behaviour.
- SPI variant communication with the DPU to change the working parameters (Control Link).
- Send the image data to the DPU (Image Link).
- Obtain H/K data (power supplies and temperature).

6.1.1. Annotations

The following section explains the fields of the requirements tables.

Identification

Identification of the CTC FPGA requirement. Format: CTC-FPGA-R-number_id

Abbreviation of Requirement Types

The requirements table contains a column which includes an identifier that reflects the requirement type. In Table 6-1 the abbreviation of requirement types (RT) are listed.

CO	Configuration Requirement
DE	Design Requirement
EC	EMC Design Requirement
EL	Electrical Requirement
EV	Environmental Requirement
FU	Functional Requirement
HA	Handling Requirement
HF	Human Factor Requirement
IF	Interface Requirement
IL	Identification and Labelling Requirement
LA	Location and Alignment Requirement
LS	(Integrated) Logistic Support Requirement
MC	Mechanical Requirement
MI	Mission Requirement
OP	Optical Requirement
OR	Operational Requirement
PA	Product Assurance Induced Requirement
PY	Physical Requirement
SW	Software Requirement
TH	Thermal Requirement
VE	Verification Requirement

TABLE 6-1: ABBREVIATION OF REQUIREMENTS TYPES

Verification Method

The requirements table contains a column labelled *VM* and includes the *Verification Method*. This column could contain the letters *R, A, I, and T*, which are the abbreviations of the following verification methods listed in Table 6-2.

R	Review of Design
A	Analysis
I	Inspection
T	Test

TABLE 6-2: ABBREVIATION OF VERIFICATION METHODS

Parent

The parent is the origin of the FPGA requirement.

Remarks

Additional information concerning the requirement.

6.2. General requirements SO/PHI (CTC FPGA)

Identifier	RT	Requirement	VM	Parent	Remarks
CTC-FPGA-R-100	DE	CTC FPGA code shall be programmed into the following part numbers: - A54SX72A PQFP208 for Breadboard and for EFM board - RTSX72SU CQFP208 for QM, FM and FS boards	R	CTC-R-263	
CTC-FPGA-R-120	DE	The CTC FPGA design shall be with total code coverage over 90%. The correct codification of the uncovered lines shall be stated.	T		
CTC-FPGA-R-130	TH	The CTC FPGA design simulation shall consider a temperature range from -20ºC to +80ºC, a total dose of 25krads and a voltage ripple of 5%.	R	CTC-R-240, CTC-R-242, CTC-R-200 and CTC-R-201	
CTC-FPGA-R-140	DE	All the FPGA outputs shall be initialized to a known value during RESET state (table 3)	T		
CTC-FPGA-R-150	EL	CTC FPGA absolute maximum rates and operating conditions shall be as described on product specification.	R		
CTC-FPGA-R-160	EV	CTC FPGA environment constraints shall be as described on product specification.	R		
CTC-FPGA-R-180	DE	All FSM shall be encoded one-hot with parity check, allowing the maximum working frequency and SEU detection. If the parity check fails, the state machines shall go to a special error state, putting all signals to the safest possible state and shall trigger an error signal.	R		
CTC-FPGA-R-181	DE	All signals shall be synchronous except IL_CCLK.	R		
CTC-FPGA-R-190	DE	All input signals, except clock signals, shall be registered two times to decrease the probability of metastability.	R		

6.3. Input/output CTC FPGA signals

Identifier	RT	Requirement	VM	Parent	Remarks
CTC-FPGA-R-200	DE	The CTC FPGA shall have the input/output signals shown in Table 6-3.	R		
CTC-FPGA-R-210	DE	The I/O electrical specification as in [13].	R		

I/O signal	Pin number	IN/ OUT	Signal type	Output load (pF)	Slew	RESET value	Value during power up	Metastability handler needed	Remarks
IL_IDAT	4	OUT	LVTTL	10	HIGH	0	None	NO	
rst_n	7	IN	LVTTL	-	-	-	0	YES	Active low
IL_CCLK	9	OUT	LVTTL	10	HIGH	clk	None	NO	100 MHz clock
ADC_DR	21	IN	LVTTL	-	-	-	None	YES	
ADC_Data<0>	23	IN	LVTTL	-	-	-	None	YES	
ADC_Data<1>	25	IN	LVTTL	-	-	-	None	YES	
ADC_Data<2>	29	IN	LVTTL	-	-	-	None	YES	
ADC_Data<3>	31	IN	LVTTL	-	-	-	None	YES	
ADC_Data<4>	33	IN	LVTTL	-	-	-	None	YES	
ADC_Data<5>	35	IN	LVTTL	-	-	-	None	YES	
ADC_Data<6>	37	IN	LVTTL	-	-	-	None	YES	
ADC_Data<7>	39	IN	LVTTL	-	-	-	None	YES	
ADC_Data<8>	43	IN	LVTTL	-	-	-	None	YES	
ADC_Data<9>	45	IN	LVTTL	-	-	-	None	YES	
ADC_Data<10>	47	IN	LVTTL	-	-	-	None	YES	
ADC_Data<11>	49	IN	LVTTL	-	-	-	None	YES	
ADC_Out_of_Range	51	IN	LVTTL	-	-	-	None	YES	
ADC_CLK	53	OUT	LVTTL	15	HIGH	0	None	NO	
SignalExt	55	OUT	LVTTL	15	LOW	0	None	NO	
EnSignalExt	57	OUT	LVTTL	15	LOW	0	None	NO	
Star_CAL	59	OUT	LVTTL	15	LOW	0	None	NO	
Star_G0	61	OUT	LVTTL	15	LOW	0	None	NO	
Star_G1	63	OUT	LVTTL	15	LOW	0	None	NO	
Star_ASEL0	65	OUT	LVTTL	15	LOW	0	None	NO	
Star_R	69	OUT	LVTTL	15	LOW	0	None	NO	
Star_S	71	OUT	LVTTL	15	LOW	0	None	NO	
Star_Rst	73	OUT	LVTTL	15	LOW	0	None	NO	
Star_CLK_X	75	OUT	LVTTL	15	HIGH	1	1	NO	
CLK10	81	OUT	LVTTL	30	HIGH	1	1	NO	Generated 10 MHz clock
clk_1_10	82	IN	LVTTL	-	-	-	None	NO	HCLK input
Star_LD_X	85	OUT	LVTTL	15	HIGH	1	1	NO	
Star_LD_Y	87	OUT	LVTTL	15	LOW	1	1	NO	
Star_Addr<0>	89	OUT	LVTTL	15	LOW	0	None	NO	
Star_Addr<1>	91	OUT	LVTTL	15	LOW	0	None	NO	
Star_Addr<2>	93	OUT	LVTTL	15	LOW	0	None	NO	
Star_Addr<3>	95	OUT	LVTTL	15	LOW	0	None	NO	
Star_Addr<4>	97	OUT	LVTTL	15	LOW	0	None	NO	
Star_Addr<5>	100	OUT	LVTTL	15	LOW	0	None	NO	
Star_Addr<6>	102	OUT	LVTTL	15	LOW	0	None	NO	
Star_Addr<7>	104	OUT	LVTTL	15	LOW	0	None	NO	
Star_Addr<8>	106	OUT	LVTTL	15	LOW	0	None	NO	
Star_Addr<9>	108	OUT	LVTTL	15	LOW	0	None	NO	
ADC_HK_DIN	133	OUT	LVTTL	10	LOW	0	None	NO	
ADC_HK_DOUT	135	IN	LVTTL	-					
ADC_HK_SCLK	137	OUT	LVTTL	10	LOW	1	None	NO	
ADC_HK_CSn	139	OUT	LVTTL	10	LOW	1	None	NO	
clk	178	IN	LVTTL	-	-	-	None	NO	100 MHz, QCLKD
CL_SCLK	195	IN	LVTTL	-	-	-	None	YES	
CL_MOSI	197	IN	LVTTL	-	-	-	None	YES	
CL_MISO	204	OUT	LVTTL	10	LOW	0	None	NO	
CL_SINT	206	OUT	LVTTL	10	LOW	1	None	NO	

TABLE 6-3: CTC FPGA INPUT/OUTPUT SIGNALS

6.4. Clocks generation

Identifier	RT	Requirement	VM	Parent	Remarks
CTC-FPGA-R-300	DE	The CTC FPGA shall work with a 100 MHz ± 50 ppm over 60 minutes master clock	R		
CTC-FPGA-R-301	DE	The CTC FPGA shall generate a 10 MHz ± 50 ppm over 60 minutes clock from master clock	R		

6.5. Reset conditioning

Identifier	RT	Requirement	VM	Parent	Remarks
CTC-FPGA-R-400	DE	Rst_n input shall be asynchronous. If nRST input is set to "0", the CTC FPGA outputs shall be set to the values according table 3	T		
CTC-FPGA-R-410	DE	Rst_n shall be registered with the master clock two times to avoid metastabilities	R		
CTC-FPGA-R-420	DE	The Control Link shall be capable to perform a synchronous reset	T		

6.6. Configuration parameters

Identifier	RT	Requirement	VM	Parent	Remarks
CTC-FPGA-R-500	CO	The image size shall be changeable between 64 and 128 pixels.	T	[5] R-1290	Image Size, 8 bits
CTC-FPGA-R-501	CO	The rolling shutter offset value shall be tuneable between 0 (no rolling shutter) and image size – 1.	T	[5] R-1300	Rolling Shutter Offset, 7 bits
CTC-FPGA-R-502	FU	The frame rate shall be at least 300 fps.	T	[5] R-1310	
CTC-FPGA-R-503	CO	The frame rate shall be changeable by modifying a delay at the end of every row read from the sensor.	T	[5] R-1310	Row Delay, 10 bits
CTC-FPGA-R-504	CO	The image sensor read out area shall be changeable.	T	[5] R-1330	Image Offset X and Y, 10 bits each.
CTC-FPGA-R-505	CO	It shall be possible to choose the digital gain (x1, x2, x4)	T	[5] R-1340	Digital Gain, 2 bits
CTC-FPGA-R-506	CO	It shall be possible to choose the analog gain (x1, x2, x4, x8)	T	[5] R-1350	Analog Gain, 2 bits
CTC-FPGA-R-510	CO	It shall be possible to subtract a fixed value to the pixel value read prior sending to increase the dynamic range.	T		Offset subtraction, 10 bits
CTC-FPGA-R-520	CO	The sampling point of the image ADC shall be changeable.	T		Sampling point, 3 bits

6.7. Image acquisition control

Identifier	RT	Requirement	VM	Parent	Remarks
CTC-FPGA-R-600	FU	The FPGA shall have four working mode: - Idle mode: no images are taken and only in this mode the configuration parameters shall be changeable. - Continuous mode: sending continuously images to ISS Control. This mode is only left when ISS Control sends an Idle Mode command. - Single mode: only one image is send to ISS Control. Then the working mode is automatically changed to Idle Mode. - Test mode: same as continuous mode but the analog output of the image sensor is change to a fixed pattern. Used to test the analog chain without the sensor.	T	CTC-R-260	

CTC-FPGA-R-610	DE	The pixel readout frequency shall be 10 MHz.	T	CTC-R-261	
CTC-FPGA-R-620	FU	The timing diagram described at [14] shall be fulfilled for the image readout.	T	CTC-R-262	
CTC-FPGA-R-630	EL	The STAR 1000 CLK_X signal shall always be clocked, even when in Idle mode, except during the row selection.	T	CTC-R-262	[14]
CTC-FPGA-R-640	EL	The STAR 1000 LD_X and LD_Y signals shall be kept always asserted to '1' except when needed for the pixel read out.	T	[NR01] CTC-R-262	[14]
CTC-FPGA-R-650	FU	The output value of the sensor when the STAR 1000 CAL signal is on shall be stored and accessible through the Control Link.	T		This value should be the minimum output of the sensor.
CTC-FPGA-R-660	FU	The timing diagram described at [15] shall be fulfilled for the analog to digital conversion.	T		
CTC-FPGA-R-670	DE	The ADC CLK shall only be on when reading images to reduce power consumption.	T		
CTC-FPGA-R-680	FU	The column and row value when the ADC Out of Range signal is high shall be stored in a register accessible by the Control Link.	T		

6.8. HK acquisition

Identifier	RT	Requirement	VM	Parent	Remarks
CTC-FPGA-R-700	FU	The camera shall provide HK data: image sensor temperature, FPGA temperature, reference voltages, some voltage supplies and frame counter.	T	CTC-R-250	
CTC-FPGA-R-710	FU	The CTC FPGA shall manage a multiplexed 8-channels ADC for HK	R		
CTC-FPGA-R-720	DE	The FPGA shall provide the SPI I/O for controlling the serial ADC	T		
CTC-FPGA-R-730	DE	The SPI clock shall work at 5 MHz	T		
CTC-FPGA-R-740	DE	The FPGA shall store the value from the ADC to a register accessible by the Control Link.	T		Table 6-4 shows the ADC channels assignment
CTC-FPGA-R-750	FU	The H/K data stored at the FPGA shall be updated at least at 1 Hz frequency.	T		

ADC channel	HK signal
0	-5 Va
1	2.5 Va
2	STAR 1000 Temperature
3	FPGA Temperature
4	+5 Va
5	+5 Vd
6	1 V Voltage Reference
7	2.5 V Voltage Reference

TABLE 6-4: ADC CHANNELS ASSIGNMENT

6.9. Control Link interface

Identifier	RT	Requirement	VM	Parent	Remarks
CTC-FPGA-R-800	FU	The FPGA shall provide a counter with the number of images send to ISS. This counter shall only work when the camera is in continuous mode and shall be reset when it leaves this mode.	T	[5] R-1370	
CTC-FPGA-R-810	IF	The CTC FPGA shall include a control interface over LVDS for communicating with the DPU	R	CTC-R-110	
CTC-FPGA-R-820	IF	The DPU control interface input signals shall be CL_SCLK and CL_MOSI and the output signals shall be CL_MISO and CL_SINT.	R	CTC-R-102	
CTC-FPGA-R-830	DE	CL_SCLK frequency shall be 1 MHz	T	CTC-R-112	
CTC-FPGA-R-840	DE	The control link frame size shall be 24 bits and send in the following order: 1 bit for read/write operation, 5 bits for the command code, 10 bits for data and 8 bits for a CRC.	R		
CTC-FPGA-R-841	DE	A control link transmission shall consist of two frames. At the first one, the CTC shall send a status and the ISS Control the command. At the second transmission, the CTC shall send the reply to the command and the ISS Control a NOP command.	T		
CTC-FPGA-R-842	DE	The CTC shall reply to any unknown or wrong command (data out of bonds, CRC error …) with a STATUS frame.	T		
CTC-FPGA-R-843	DE	The CTC shall reply to any write command or NOP command sending back the same command.	T		
CTC-FPGA-R-844	DE	The CTC shall reply to any read command with the same header (read/write operation and command code) but changing the data field to the internal value.	T		
CTC-FPGA-R-845	DE	The value field shall be MSB first.	T		
CTC-FPGA-R-846	DE	The CRC used shall be a CRC-8 with polynomial 0xD5 ($x^8 + x^7 + x^6 + x^4 + x^2 + 1$).	R		
CTC-FPGA-R-847	DE	The error signal of the error state from the different FSMs shall be readable from ISS Control through the status frame.	R		
CTC-FPGA-R-848	DE	The command shall be the one shown at Table 6-5. An X at R/W means the command can be read or write. An X at value means this bit will contain data.	T		
CTC-FPGA-R-849	DE	The data content of a status frame shall be as shown at Table 6-6.	T	CTC-FPGA-R-847	
CTC-FPGA-R-850	DE	The working parameters shall be only changeable when in Idle Mode.	T		

R/W (First transmitted bit)	CODE (Transmitted bits 2 to 6)	COMMAND	VALUE (Transmitted bits 7 to 16, MSB first)
X	00011	Image Size	XXXXX XXX10
X	00101	Delay	XXXXX XXXXX
X	00110	Analog & Digital Pixel Gain	AA010 DD010
X	00111	Offset subtraction	XXXXX XXXXX
X	01001	Rolling Shutter Offset	XXXXX XX010
X	01010	Image Offset X	XXXXX XXXXX
X	01100	Image Offset Y	XXXXX XXXXX
X	01101	ADC Phase Shift	010XX 0101X
1	10001	Frame Counter	XXXXX XXXXX
1	10010	Column Out of Range	XXXXX XXXXX
1	10100	Row Out of Range	XXXXX XXXXX
1	10110	CAL Value	XXXXX XXXXX
1	11000	H/K Data 1	XXXXX XXXXX
1	11001	H/K Data 2	XXXXX XXXXX
1	11010	H/K Data 3	XXXXX XXXXX
1	11011	H/K Data 4	XXXXX XXXXX
1	11100	H/K Data 5	XXXXX XXXXX
1	11101	H/K Data 6	XXXXX XXXXX
1	11110	H/K Data 7	XXXXX XXXXX
1	11111	H/K Data 8	XXXXX XXXXX
0	00001	Mode Single Frame Read	01010 01010
0	00010	Mode Continuous Frame Read	01010 01010
0	00100	Mode Idle	01010 01010
0	01000	Mode Test	01010 01010
1	10000	Get current mode	XX010 01010
0	10101	RESET	01010 01010
0	01110	NOP	01010 01010
1	01110	STATUS	XXXXX XXXXX

TABLE 6-5: CONTROL LINK FRAMES

Transmitted Bit	Content
0	CRC error on the last frame
1	ADC input out of range
2 – 3	Working mode: 00, single mode; 01, continuous mode; 10, idle mode and 11 test mode.
4	Error at the Control Link block.
5	Fixed at zero.
6	Error at the Sensor Control block.
7	Error at the Image Link block.
8	Error at the H/K Sensor Read block.
9	Error at the clock generator block.

TABLE 6-6: STATUS FRAME

6.10. Image link interface

Identifier	RT	Requirement	VM	Parent	Remarks
CTC-FPGA-R-900	FU	The camera image link shall send 10 bits data words from every pixel.	T	CTC-R-264	
CTC-FPGA-R-910	IF	The Image Link consists of two output signals: IL_CLK and IL_DATA.	R	CTC-R-120	
CTC-FPGA-R-911	IF	The Image Link bit rate shall be 100 Mbps.	T	CTC-R-121	
CTC-FPGA-R-920	FU	The IL_CLK shall be an asynchronous 100 MHz clock. This signal shall be directly the clock coming from the external crystal, routed internally through the FPGA.	R		
CTC-FPGA-R-930	DE	The frame size shall be variable depending on the image size. The frame shall consist of a 10 bit preamble, 10 bits for the row sent, the pixel data (10 bits for every pixel) and 16 bits for a CRC.	R		
CTC-FPGA-R-940	DE	The preamble shall be 0x111 (LSB first).	T		
CTC-FPGA-R-950	DE	The pixel data shall be LSB.	T		
CTC-FPGA-R-960	DE	The CRC used shall be CRC-16-CCITT ($x^{16} + x^{15} + x^2 + 1$)	R		
CTC-FPGA-R-970	DE	The pixel data sent shall be pre-processed as follow: - If the ADC Out of Range signal is true and the MSB of the ADC is zero, the pixel data sent shall be zero. - If the ADC Out of Range signal is true and the MSB of the ADC is one, the pixel data sent shall be the maximum possible value (0x3FF). - If the ADC Out of Range signal is false and the offset subtraction parameter is bigger than the input data, the data sent shall be zero. - If the ADC Out of Range signal is false, the offset subtraction parameter is lower than the input data but the Digital Gain parameter causes the loss of information, the data sent shall be the maximum possible value. - Otherwise, the offset subtraction parameter shall be subtracted to the input data and this value is shifted right the number of times indicated by the Digital Gain parameter.	T		

7. FPGA Architecture Definition

The scope of this section is to explain the architecture of the firmware working on the CTC, following the directives given at [11]. In this sense, this document explains the different blocks in which the design should be divided, its functionalities and interfaces between them and external signals. It also shows the clock and reset schemes to implement. The pin assignment to be used is explained in CTC-R-FPGA-200.

7.1. Architecture design overview

The CTC firmware has been divided in the following blocks (Figure 7-1):

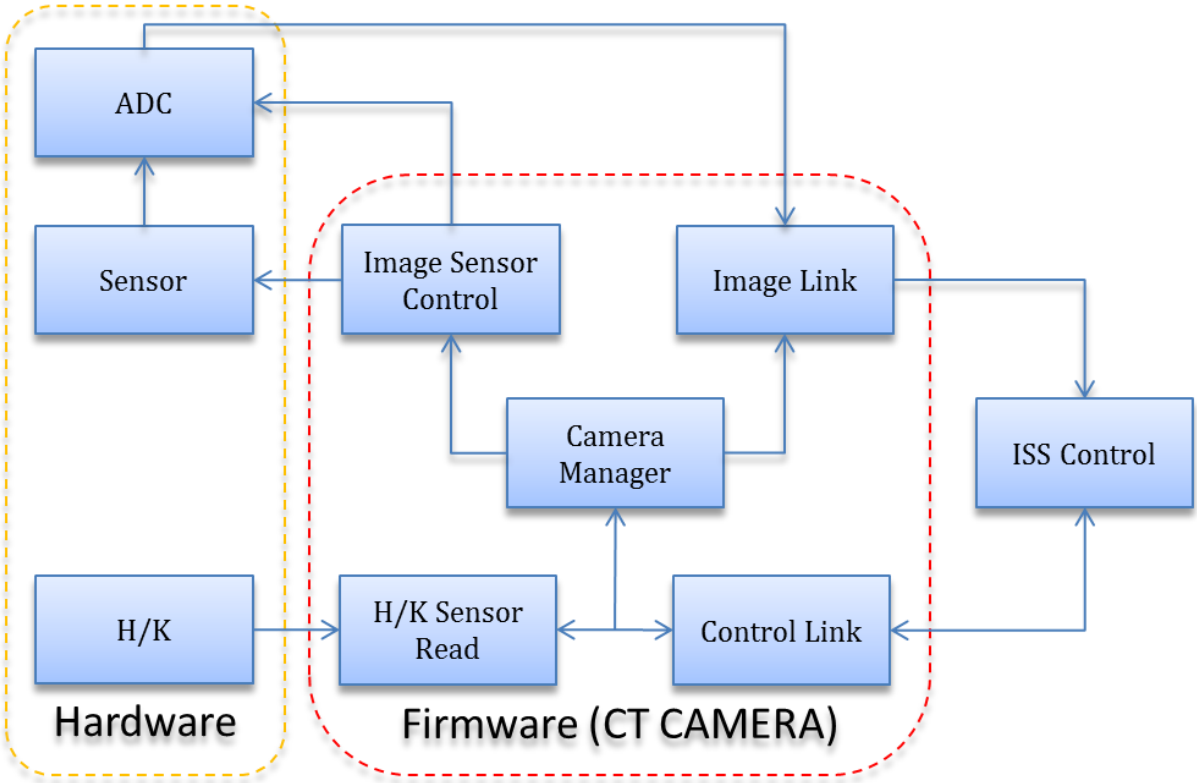

FIGURE 7-1 CTC FIRMWARE BLOCKS

- Image Sensor Control: block controlling the signals to the ADC and the STAR 1000 for the image readout process.
- Image Link: block reading the data from the ADC and sending it to the ISS.
- Camera Manager: block controlling the working mode of the CTC.
- H/K Sensor Read: block reading the housekeeping data.
- Control Link: block managing the communications between the CTC firmware and the ISS.

7.2. Working Modes

There are four different working modes (CTC-FPGA-R-600):

- Idle: in this mode Image Sensor Control and Image Link are halted. This is the only state where it's possible to change the firmware parameters. This is the start-up state.
- Single frame read: a single image is read and sent to the ISS. Once sent the working mode is changed to idle.

- Continuous frame read: continuously images are read and sent to the ISS. This mode is only left if the ISS send the idle command or the reset command.
- Test: a square 5 MHz signal with amplitude between the theoretical minimum to the maximum of the sensor is generated as input of the analog chain. The ADC output is sent to ISS normally. This mode only is useful to test that the analog circuitry and the sending of data to the ISS works as expected. The only way to leave this mode is when the ISS sends the idle command or the reset command.

7.3. Clock and reset scheme

The external crystal of 100 MHz (CTC-FPGA-R-300) is used as input for the quadrant clock QCLK. The reason for using the 100 MHz clock in the quadrant clock and not the dedicated clock network is the power consumption. Dedicated clock network has a low clock skew independently of the number of registers used as it has direct path without antifuses to every register. This ensures a very low propagation time and skew, but the problem with this is that it has a very high capacitive load, increasing power consumption.

From this 100 MHz clock, the 10 MHz clock is generated (CTC-FPGA-R-301) and externally routed to the dedicated clock network (HCLK).

The implemented reset will be an asynchronous asserted register two time for its deassertion (CTC-FPGA-R-400). For this, the external asynchronous active low reset is registered twice to decrease the probability of metastabilities (CTC-FPGA-R-410). Then, the registered reset is routed through the routed clock network CLKB, decreasing so the propagation time. Even if the signal is registered, the reset signal is treated asynchronous acting directly on the set/reset signals of the flip-flops.

7.4. Firmware blocks

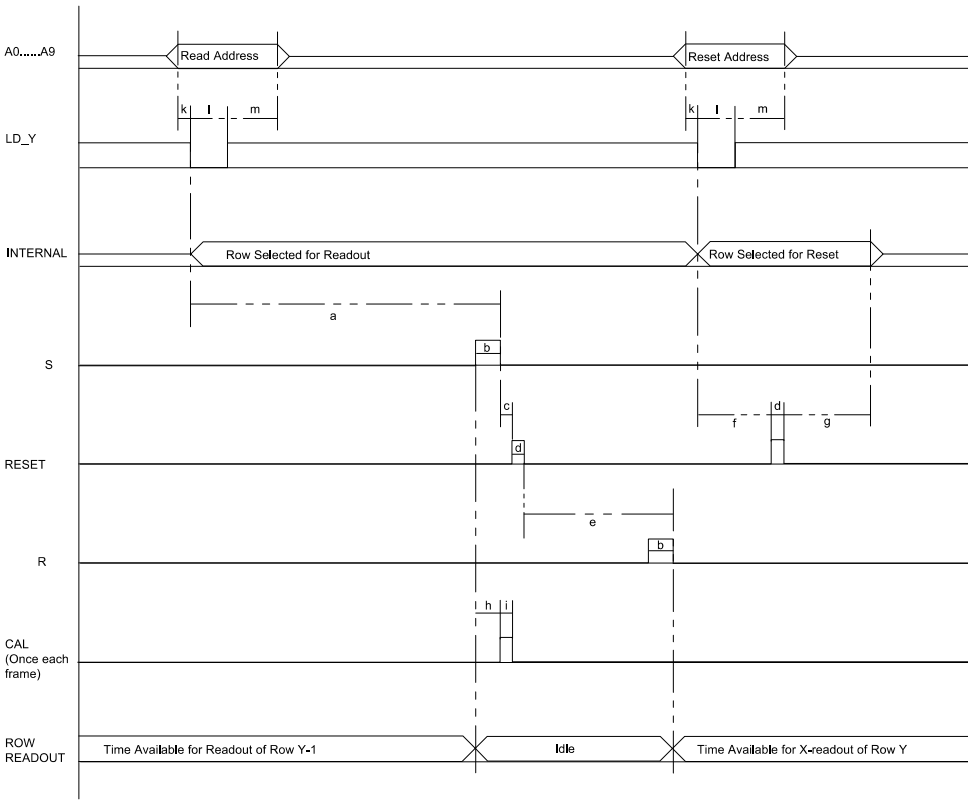

FIGURE 7-2 READ AND RESET OF A ROW

7.4.1. Image Sensor Control

The function of this block is controlling the STAR 1000 and the ADC during the image read out process. This block uses the 10 MHz clock.

7.4.1.1. Row read and reset timings

The Figure 7-2 shows a read of a row and a reset from another one (CTC-FPGA-R-620). The reset of another row is used to lower the integration time of a pixel. When the rolling shutter is zero this reset is not performed.

Taking into account that the block is working at 10 MHz, Table 7-1 shows the datasheet typical timing and the implemented one.

Therefore, the total needed time to read a row corresponds to k+a+c+d+e=5.6 us. And for the reset, the time is k+f+d+g=0.5 us.

The most relevant contribution to the row read process is the time needed by the internal row selection (timing a). Since the integration time must be configurable ([NR03] CTC-FPGA-R-503), a 10 bits parameter writeable by ISS Control allows adding extra delay to the default value of timing a.

Symbol	Datasheet typical time (ns)	Waiting cycles	Implemented waiting time (ns)
a	3600	36	3600
b	400	4	400
c	100	1	100
d	200	2	200
e	1600	16	1600
f	100	1	100
g	100	1	100
h	200	2	200
i	1000	10	1000
k	10	1	100
l	20	1	100
m	10	1	100

TABLE 7-1 ROW READ AND RESET TIMING

7.4.1.2. Column read timings

The column read is done as shown in Figure 7-1.

For this process two 10 MHz clocks (CTC-FPGA-R-610), LD_X and CLK_X, with a 180 degree phase shift are generated.

The selected column to read is acquired by the sensor on the rising edge of LD_X. The analog value of the pixel read is present at the output at the third falling edge of CLK_X. Therefore, the ADC conversion is done at the third rising edge of CLK_X, when the analog value should be stable at the ADC input.

If CLK_X is turned off, the values in the column register of the STAR 1000 leaks away after a while. This can cause multiple columns being selected at once, causing high current through the sensor and damaging it. Therefore, CLK_X is always turned on (CTC-FPGA-R-630). For the same reason, the LD_X and LD_Y signals are always asserted when no images are read (CTC-FPGA-R-640).

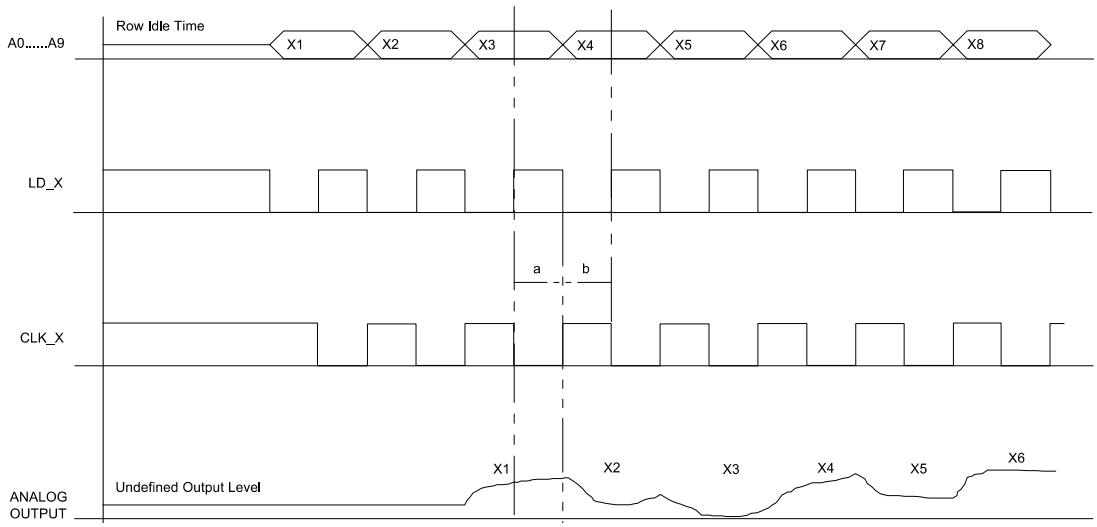

FIGURE 7-3 COLUMN READ

The needed time for reading all the columns are equal to the number of columns plus four times the clock cycle. From the four extra column cycles, three are due to the pipeline and one due to an extra column read cycle performed before the actual column to be readout to allow the electronics to stabilize. Hence, with the 10 MHz clock and the default value of 128 columns, the needed time is 13.2 us.

7.4.1.3. Image read frequency

Table 7-2 shows a summary of the timings involved in the reading of an image.

Actions	Time (us)
Row read	5.6
Row reset	0.5
Reading 128 columns	13.2

TABLE 7-2 IMAGE READ TIMING

Taking this in account, the time needed for reading a 128 by 128 image is shown in Table 7-3.

	Without reset	With reset
Readout period (ms)	2.406	2.470
Readout frequency (Hz)	416 Hz	405

TABLE 7-3 PERIOD AND FREQUENCY OF IMAGE READOUT

This value is greater than the required 300 fps (CTC-FPGA-R-502). But using the row delay parameter allows lowering the read out frequency down to 64 fps.

Since the Image Link works in real time this is also the frequency of the images sent to ISS. Only a delay form around 10 us is added between the analogic pixel value present at the sensor output and the data arriving at ISS.

7.4.1.4. State diagram

The state diagram is shown in Figure 7-4. The following states have been defined:

- Halt: start-up state of the Image Sensor Control. It remains in this state until the Camera Manager activates the start signal. Then, the FSM changes to the sendRow state. All signals are at a steady value during this state.
- sendRow: states in which the signals to select the next row are sent. If the delay parameter is not zero, the next state is the delay state. If yes, the next state is the readRow state.
- delay: configurable delay state to increase the exposure time of the sensor. Once the counter reaches the value of the delay parameter, the state is changed to the readRow state.
- readRow: state in which the needed signals to load the pixels in to the column amplifiers are sent. If the rolling shutter parameter is zero, the next state is the readCol state. Otherwise, the next state is the resetRow state.
- resetRow: state in which the reset of a row is applied. The next state is always the readCol state.
- readCol: state in which the column values are read. If the start signal from the Camera Manager is false (the CTC is in single frame mode) and an entire image has been sent, the next state is endADC state. If not (the CTC is in continuous frame mode), the next state is the sendRow state.
- endADC: state in which all the control signals are at a low level except the ones to the ADC, allowing so to finish the conversion of the remaining pixels.
- Error: state in which all output signals are in a safe state. The error state is only reached if the parity check of the one-hot encoded FSM fails. The FSM stays in this state until a reset of this block is done.

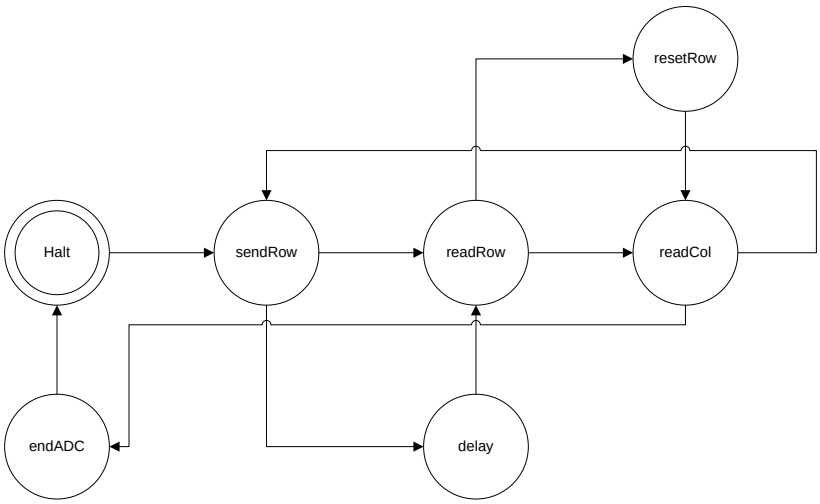

FIGURE 7-4 IMAGE SENSOR CONTROL STATE DIAGRAM

7.4.1.5. Signals

The input signals for this block are:

- start: signal coming from the Camera Manager. When this signal is active the Image Sensor Control starts image acquisition. In continuous working mode this signal is always on.
- Asynchronous registered system reset and synchronous reset coming from Camera Manager.
- The following parameters of the register bank: ImageSize, RSOffset, ImageOffsetX, ImageOffsetY and Delay.
-

The output signals to other blocks are:

- processFinished: signal to the Camera Manager informing that a frame read has been finished.
- newFrame: signal to Image Link which means that a new image acquisition has been started.
- eStarLD_X: signal turning on the LD_X signal generation. This signal goes to Camera Manager.
- Row: signal to Image Link with the actual row been read.
- startCAL: signal to Image Link to store the ADC output when the STAR 1000 CAL signal is enabled.
- ADCOEB_n: signal to Image Link that when zero means the output of the ADC has meaningful data.
- ILRst_n: reset signal to Image Link.
- Error_SC: error signal only true if the FSM reaches the error state.
- validData: signal to Camera Manager to activate the ADC clk (CTC-FPGA-R-670).

The output signals of the FPGA controlled by this block are: StarLD_Y, StarAddr (10 bits), StarRst, StarS, StarR, and StarCAL.

7.4.2. Image Link

The functions of this block are serializing the ADC output data, generating a packet from this value with a header and error detecting information and then sending it to the ISS. This block uses the 100 MHz clock (CTC-FPGA-R-911).

7.4.2.1. Image link frame

The Image Link data is sent with the less significant bit first (LSB, CTC-FPGA-R-950) with words of 10 bits (CTC-FPGA-R-900). The frame length depends upon the image size. In case of an image size of 128 by 128 the frame structure is shown in

Bit sent	1-10	11-20	21-1300	1301-1316
Content	Preamble (0x111)	Row sent	Pixel data	CRC-16-CCITT

Table 7-4 (CTC-FPGA-R-930). For a different size, the pixel data content will be equal to the image size multiplied by 10.

Bit sent	1-10	11-20	21-1300	1301-1316
Content	Preamble (0x111)	Row sent	Pixel data	CRC-16-CCITT

TABLE 7-4 IMAGE LINK FRAME

The first word sent is a preamble with value 0x111 (CTC-FPGA-R-940). The second word sent is the relative value of the actual row being sent. Then, the data is sent. Finally, a CRC-16-CCITT is added with a LFSR implementation as shown in Figure 7-5 (CTC-FPGA-R-960).

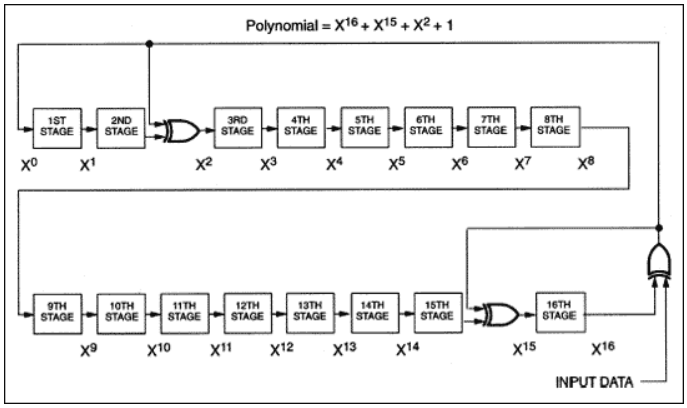

FIGURE 7-5 IMAGE LINK CRC-16-CCITT

The data from the sensor is read at the rising edge of the Data Ready signal from the ADC. From this value then the OffsetSubtraction parameter is subtracted (CTC-FPGA-R-510). Then, from the twelve bits only ten will be sent, selected by the Digital Gain value (CTC-FPGA-R-970). This value will only be sent if any of the next cases doesn't apply:

- If the OutOfRange signal (signal coming from the RHF1201, if true the analog input signal to the ADC is out of the full-scale range) is true and the MSB of the input data is one, the data sent is the maximum possible value (0x3FF).
- If the OutOfRange signal is true and the MSB of the input data is zero, the data sent is zero.
- If the OutOfRange signal is false and the OffsetSubtraction parameter (value to be subtracted to every pixel) is bigger than the input data, the data sent is zero.
- If the OutOfRange signal is false, the OffsetSubtraction parameter is not bigger than the input data but the Digital Gain parameter (parameter that allows the selection of which of the twelve bits will be sent) causes the loss of non-zero bits, the data sent is the maximum possible value (0x3FF)

7.4.2.2. State diagram

The state diagram is shown at Figure 7-6. The following states have been defined:

- Idle: start-up state of the Image Link FSM. It remains in this state until Image Sensor Control newFrame signal is true. Then, the states changes to the readData state.
- readData: this state is used to initialize the pipeline and to pre-process the input data as stated before. The next state is the preamble state (CTC-FPGA-R-660).
- Preamble: in this state the preamble of the frame is sent. The next state is the row state.
- Row: in this state the relative row number is sent, starting at zero. The next state is the data state.
- Data: in this state the pixel data is sent. This state is changed to the CRC state once the full row is sent.
- CRC: in this state the last sixteen bits of the frame, the once corresponding to the CRC, are sent. When done, the next state is the idle state.
- Error: state in which all output signals are in a safe state. The error state is only reached if the parity check of the one-hot encoded FSM fails. The FSM stays in this state until a reset of this block is done.

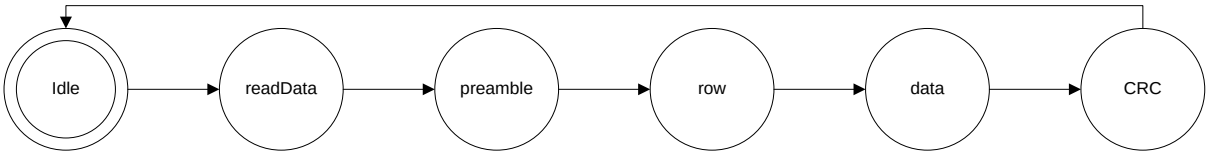

FIGURE 7-6 IMAGE LINK STATE DIAGRAM

7.4.2.3. Signals

The input signals are:

- newFrame: signal coming from the Image Sensor Control. This signal informs that a new image acquisition is starting.
- DataReady: signal coming from the RHF1201 (ADC). This signal is a copy of the clock sent to the ADC but with its rising edge shifted to the optimal point to read the ADC output data.
- OutOfRange: signal coming from the RHF1201 (ADC). If true the analog input signal to the ADC is out of the full-scale range.
- ADC_Data: 12 bits signal coming from the ADC, containing the digital value of the pixels.
- Row: 7 bits signal coming from the Image Sensor Link containing the relative row being read.
- startCAL: signal coming from the Image Sensor Control. When true, it tells to the Image Link that the ADC Data contains the digital value of the BLACKREF.
- ADC_OEB_n: signal coming from the Image Sensor Control. When zero, it tells to the Image Link that output of the ADC has meaningful data.
- Asynchronous registered system reset and synchronous reset coming from Image Sensor Control.
- The following parameters of the register bank: image size, offset subtraction and digital gain.

The output signals are:

- IDAT: signal sent to ISS containing the data of the Image Link communication (CTC-FPGA-R-910).
- CALvalue: signal sent to Control Link containing the value of the blackref analog output of the last row read (CTC-FPGA-R-650).
- outOfRange: signal indicating there was an ADC value out of range during the data acquisition.
- Error_IL: error signal only true if the FSM reaches the error state.
- error_OutOfRange_col and error_OutOfRange_row: signal containing the column and row of the last pixel which analogic value was out of the input range of the ADC (CTC-FPGA-R-680).

7.4.3. Camera Manager

The function of this block is managing the other blocks controlling the working mode of the CTC firmware. It also controls the image counter; 10 bits counter which in continuous working mode increments every time an entire image is read from the sensor ([NR03] CTC-FPGA-R-800). This block works at 10 MHz except the clock generator subblock, which works at 100 MHz. This block doesn't have any FSM.

The working mode can only be changed if the actual working mode is idle or if the new working mode will be idle. In case of changing to idle mode, a synchronous reset is being performed on Image Sensor Control and Image Link to ensure that these blocks will be in a known state before the next operation starts.

7.4.3.1. Signals

The input signals are:

- processFinished: signal coming from the Image Sensor Control informing when an entire image has been read.
- eLD_X: signal coming from the Image Sensor Control activating the LD_X clock generation.
- ADC_CLK_ena_n: signal coming from the Image Sensor Control to activate the ADC_CLK generation.
- CL_End: signal coming from the Control Link to tell the Camera Manager the transmission has finished and if there is a change of the working mode, it shall be done when this signal is true.
- changeWorkingMode: signal coming from Control Link to activate the change of working mode.
- newWorkingMode: two bit signal coming from Control Link with the code of the new working mode.
- Asynchronous registered system reset and synchronous reset coming from Control Link.
- The following parameters of the register bank: ADC phase shift and analog gain.

The output signals are:

- enable: signal sent to Image Sensor Control that starts the image read process.
- CMsRst_n: active low signal that resets Image Sensor Control.
- Clk10: 10 MHz clock used by the blocks working at this frequency.
- ADC_CLK: 10 MHz clock used for the ADC.
- CLK_X LD_X: clocks generated for the STAR 1000 with a phase shift between them of 180 degrees.
- G0: less significant bit of the analog gain from the STAR 1000.
- G1: more significant bit of the analog gain from the STAR 1000.
- frameCounter: 10 bit signal sent to Control Link counting the number of images read since entering in continuous working mode.
- workingMode: 2 bit signal sent to Control Link containing the actual working mode.
- erroCLK: error signal only true if the counter of the clock generator block has reached a value out of bounds.
- EnSignalExt and SignalExt: two signals used to generate an external 5 MHz square signal used in the test mode as analog input.
- A_SEL0: signal sent to the STAR 1000 used to select the analog output source. When in test mode this signal is used to change the input of the analog chain to the test signal generated via EnSignalExt and SignalExt.

7.4.4. Housekeeping Sensor Read

The functions of this block is reading the H/K values from the H/K ADC (CTC-FPGA-R-710) at a 1 Hz frequency (CTC-FPGA-R-750) and storing these values at a register bank accessible from the control link (CTC-FPGA-R-740). This block works at 10 MHz (CTC-FPGA-R-730).

7.4.5. Communication

The communication is similar to SPI (Figure 7-7). When the master (the FPGA) sets the chip select signal at a low level, the ADC starts reading the SCLK and DIN inputs. Keeping always the chip select signal at high level except during the communication with the H/K ADC ensures a synchronization point between them, independently of previous noise in this channel.

From the first to the third SCLK cycle the H/K ADC acquires the analog value to be converted during this transmission.

From the third to the fifth SCLK cycle the firmware sends, via DIN, the address to be selected by the input multiplexer of the ADC for the next conversion. This way we can choose between the eight different analog inputs.

From the fifth to the sixteenth SCLK cycle the H/K ADC sends, via DOUT, the digital value of the selected analog input at the previous transmission. The first bit sent is the most significant one.

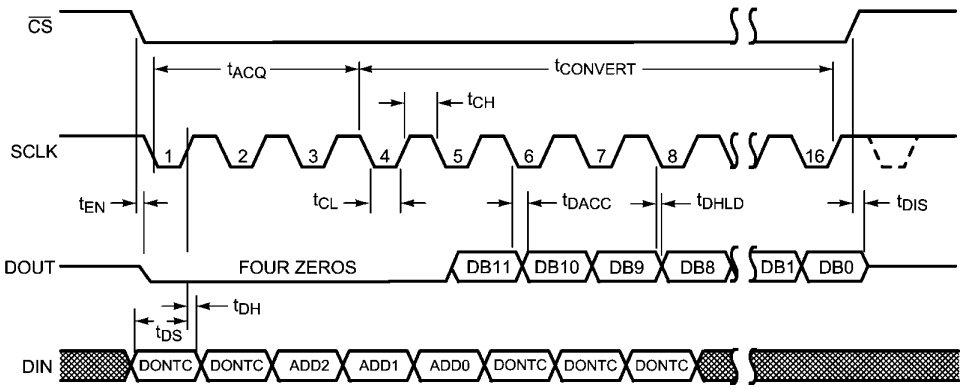

FIGURE 7-7 H/K ADC COMMUNICATION TIMING DIAGRAM

All digital values are updated at a 10 Hz frequency, and so this process is done at 80 Hz frequency (CTC-FPGA-R-70).

1.1.1. State diagram

The state diagram is shown at Figure 7-8. The following states have been defined:

- IDLE: start-up state of the FSM. Once the start signal comes from the counter to generate the 1/8 Hz signal, the state is changed to init.
- INIT: in this state the chip select signal goes to 0 while the other signal doesn't change. The next state is the run state.
- RUN: in this state the SCLK signal is a 5 MHz clock and the address of the next channel is sent. Once done, the next state is the wait state.
- WAIT: in this state the chip select signal goes to 1 while the other signal doesn't change. The next state is the finish state.
- FINISH: in this state, the serial value read from DOUT is stored in the corresponding 10 bit HKData register.
- ERROR: state in which all output signals are in a safe state. The error state is only reached if the parity check of the one-hot encoded FSM fails. The FSM stays in this state until a reset of this block is done.

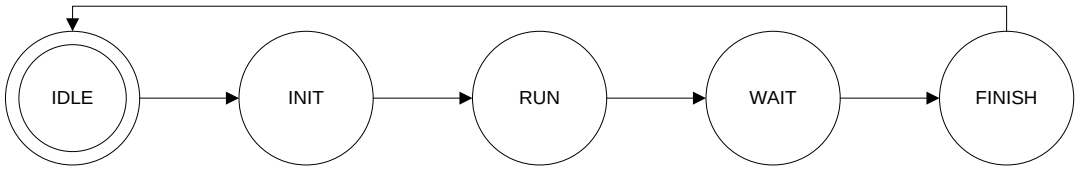

FIGURE 7-8 HOUSEKEEPING SENSOR READ STATE DIAGRAM

7.4.5.1. Signals

The input signals are:

- HK_DOUT: H/K ADC data output. The ADC changes its output data on the falling edge of HK_SCLK and the firmware reads the data on the rising edge of HK_SCLK.
- Asynchronous registered system reset and synchronous reset coming from Control Link.

The output signals are:

- HK_CS_n: active low H/K ADC chip select. When put at high level, H/K ADC outputs are at high impedance.
- HK_SCLK: 5 MHz clock signal for the H/K ADC communication.
- HK_DIN: input data to the H/K ADC. The firmware changes the data values at the falling edge of HK_SCLK and the H/K ADC reads the data at the rising edge.
- Error_HK: error signal only true if the FSM reaches the error state.
- HKData1 to HKData8: 10 bit signals with the stored H/K data of the 8 analog channels.

7.4.6. Control Link

The function of this block is to manage the control link, the SPI based communication with the ISS. This block works at 10 MHz. The control link is used to change the working mode and read or change the parameters of the firmware (CTC-FPGA-R-810). The CTC works as the slave and the ISS as the master.

7.4.6.1. Control link signals

- SCLK: 1 MHz clock generated by ISS (CTC-FPGA-R-830). On its rising edge the data of the channel is read and at the falling edge the data is changed. Transmissions of one word consist of 24 pulses with a longer high level at the end used, in conjunction with SINT, to synchronise the state between the master and the slave.
- MOSI (Master Output Slave Input): CTC reads the bit sent by ISS at the falling edge of SCLK and ISS writes the bit to be sent to CTC at the rising edge.
- MISO (Master Input Slave Output): ISS reads the bit sent by CTC at the falling edge of SCLK and CTC writes the bit to be sent to ISS at the rising edge.
- SINT (Slave controlled serial Interrupt): signal controlled by CTC with two different functions. When a communication starts, SINT goes in a low state and once the 24 bits are received, SINT goes again to a high state. Also, if no transmission is in progress and an error occurs at CTC, SINT goes low to inform ISS that an internal error has happened.

7.4.6.2. Frame

The frame of the control link has the next structure (Table 7-5) (CTC-FPGA-R-840):

Bit position	1	2-6	7-16	17-24
Code	Read/Write (R/W)	Command (COM)	Value (VAL)	CRC-8 (CRC)

TABLE 7-5 CONTENT OF A CONTROL LINK FRAME

The first bit of the transmission show if it is a read (1) or write (0) command. A write command is a command that changes the working mode or the value of a parameter at CTC.

The second to the sixth bit indicates which command we want to execute following the codes of Table 7-7 for parameters commands and Table 7-6 for working mode commands.

The seventh to the sixteenth bit content is the data value of the command. In case a command doesn't require any value to be sent, it will have a fixed pattern. The seventh bit transmitted is the most significant bit (MSB first, CTC-FPGA-R-845).

The bit seventeenth to twenty-fourth content is a CRC-8 with polynomial 0xD5 ($x^8 + x^7 + x^6 + x^4 + x^2 + 1$, CTC-FPGA-R-846).

In the Table 7-7 and Table 7-6, an X on the read/write field means that the command can be a read or a write command. For the value fields, an X means that this bit depends on the actual value to be transmitted (CTC-FPGA-R-848). Some commands don't require a frame of this length, but as we don't need a fast transmission rate, it's preferred to send frames of fixed length to increase reliability.

R/W	CODE	COMMAND	VALUE
0	00001	Mode Single Frame Read	01010 01010
0	00010	Mode Continuous Frame Read	01010 01010
0	00100	Mode Idle	01010 01010
0	01000	Mode Test	01010 01010
1	10000	Get current mode	XX010 01010
0	10101	RESET	01010 01010
0	01110	NOP	01010 01010
1	01110	STATUS	XXXXX XXXXX

TABLE 7-6 WORKING MODE COMMANDS

Any unknown or invalid command is replied with a STATUS command (CTC-FPGA-R-842). When CTC is in any other state than Idle the only valid commands are Mode Idle, Reset and NOP. Any other command will be treated like an invalid command and so will be replied with a STATUS.

R/W	CODE	COMMAND	VALUE
X	00011	Image Size	XXXXX XXX10
X	00101	Delay	XXXXX XXXXX
X	00110	Analog & Digital Pixel Gain	AA010 DD010
X	00111	Offset subtraction	XXXXX XXXXX
X	01001	Rolling Shutter Offset	XXXXX XX010
X	01010	Image Offset X	XXXXX XXXXX
X	01100	Image Offset Y	XXXXX XXXXX

X	01101	ADC Phase Shift	010XX 0101X
1	10001	Frame Counter	XXXXX XXXXX
1	10010	Column Out of Range	XXXXX XXXXX
1	10100	Row Out of Range	XXXXX XXXXX
1	10110	CAL Value	XXXXX XXXXX
1	11000	H/K Data 1	XXXXX XXXXX
1	11001	H/K Data 2	XXXXX XXXXX
1	11010	H/K Data 3	XXXXX XXXXX
1	11011	H/K Data 4	XXXXX XXXXX
1	11100	H/K Data 5	XXXXX XXXXX
1	11101	H/K Data 6	XXXXX XXXXX
1	11110	H/K Data 7	XXXXX XXXXX
1	11111	H/K Data 8	XXXXX XXXXX

TABLE 7-7 PARAMETER COMMANDS

The value meaning varies with the command. In most cases it will directly mean the value for the command. If this value is out of the range defined below the frame will be treated as invalid (without changing the CTC register value) and so replied with a STATUS.

- Image Size: It must be between 64 and 128. The default value is 128 (CTC-FPGA-R-500).
- Analog & Digital Pixel Gain: the two first bits of value (bits 7 and 8 of the frame) contain the analogic gain and the bits five and six of value (bits twelve and thirteen of the frame) contain the digital gain. The analogic gain sets the star 1000 output gain (x1, x2, x4 and x8, CTC-FPGA-R-506). The digital gain must be between zero and two (CTC-FPGA-R-505). With a digital gain of zero the CTC sends the ten lower bits of the ADC and with a gain of two it uses the ten most significant bits of the ADC.
- Rolling Shutter Offset: It must be between zero and the Image Size minus one. The default value is zero (CTC-FPGA-R-501).
- Image offset: It must be between zero and 1024 minus Image Size. The default value is 448 (CTC-FPGA-R-504).
- ADC Phase Shift: if the last bit is set to zero the base phase difference between the ADC sample clock and the Star 1000 output clock is of 180º, and if set to one there is no extra phase difference between the two clocks. The value set at the third and fourth bit adds a phase difference of about 36º multiplied by this value, added to the previous one (CTC-FPGA-R-520).
- Get current mode: the codification is the following: idle (00), single mode (01), continuous mode (10) and test mode (11).
- Status: it contains the internal status register with the following information (CTC-FPGA-R-849):
    - CRC Error (1 bit): if true there was a CRC error in the last transmission.
    - ADC Out of Range (1 bit): if true it means that the analog input to the ADC is out of the full-scale range. The two registers ColumnOutOfRange and RowOutOfRange shows the pixel where this happened. This flag is cleared when columnOutOfRange is read.
    - Working Mode (2 bits): shows the current working mode of CTC. Its value is the same as the content of get current mode.
    - Error in some CTC block (6 bits): The first bit means an error in the Control Link, the second is fixed to 0, the third in the Image Sensor Control, the fourth in Image Link, the fifth in the H/K Sensor Read and the last one in the block generating the Star 1000 clock (Table 7-8).

Bit transmitted	1	2	3- 4	5	6	7	8	9	10
Code	CRC Error	ADC Out Of Range	Working Mode	Error CL	'0'	Error SC	Error IL	Error HK	Error CLK

TABLE 7-8 STATUS CONTENT

- Other working mode commands: its value is irrelevant and so fixed to 0x014A.

1.1.2. Communication

This link is a bidirectional synchronous communication working at 1 Mbps. The word length of the control link is 24 bits. The clock starting value is zero (CPOL zero), with the data read on the falling edge (CPHA one) and with the most significant bit at the beginning.

The communication consists of two transmissions (CTC-FPGA-R-841). At the first transmission cycle, the master sends the command to be executed by CTC and the slave sends a STATUS frame. At the second transmission, the master sends a NOP frame and the slave the reply of the previous received command. In case of a parameter write command, change state command or a NOP frame, the reply will be exactly the same received frame (CTC-FPGA-R-843). And for a parameter read command, the value field will contain the data (CTC-FPGA-R-844). A timing diagram of a complete communication is shown in Figure 7-9.

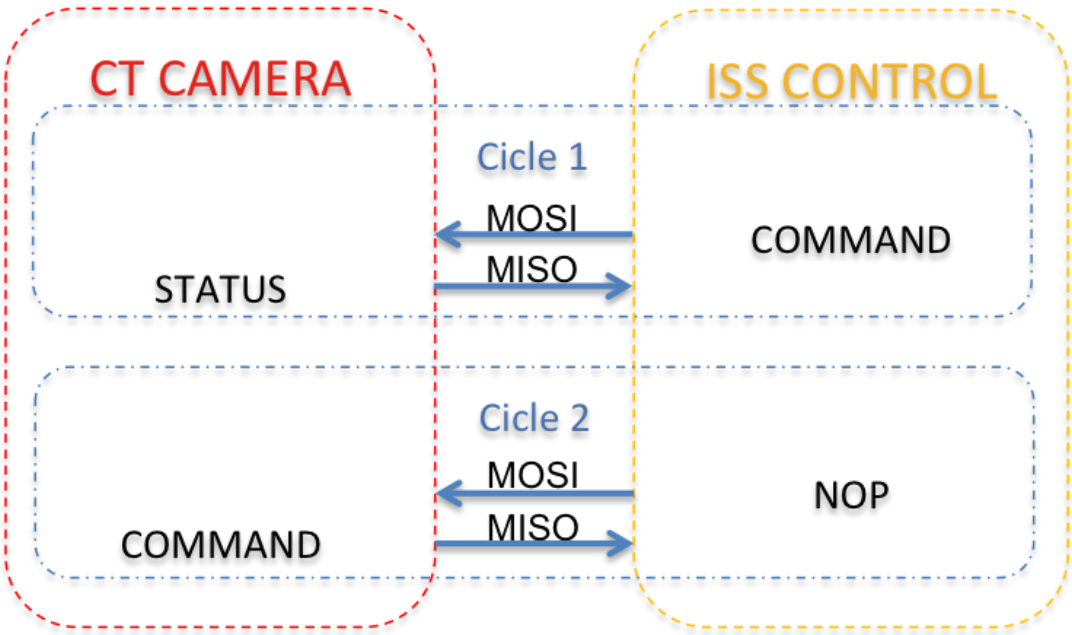

FIGURE 7-9 CONTROL LINK COMMUNICATION

A normal transmission initiated by the master (Figure 7-10) starts with the SCLK signal going to a high level. At the same time the master writes the first bit at MOSI. Once the slave is aware of the SCLK change, it writes the first bit of the status register to MISO. When the slave it's ready to start the transmission, it puts the SINT signal in a low level. Then, it also writes the first bit to be sent in MISO. In the case of the first cycle of the transmission the data to be sent is the status register. When the master detects the falling edge of SINT, SCLK starts working as the clock of the communication. The values of MOSI and MISO change at the rising edge and are read on the falling edge of SCLK. Once the slave has received 24 SCLK pulses it will put SINT in a high level again. If the

master has sent the 24 pulses and doesn't see the rising edge of SINT it will mean that some interference in the channel has masked some pulse. Therefore, it will continue sending pulses until SINT rises. This transmission will be lost but the synchronization between master and slave will be regained.

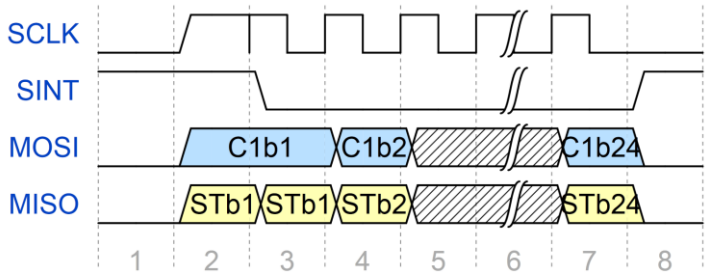

FIGURE 7-10 STARTING OF A TRANSMISSION INITIATED BY THE MASTER

If the slave detects an error in the CTC, it can ask the master to start a communication (Figure 7-11). In this case, while SCLK is at a low level, the slave lowers SINT and writes the first bit of the status register to MISO. When the master detects the change of SINT and wants to start the transmission, it activates SCLK and the communication goes on as usual.

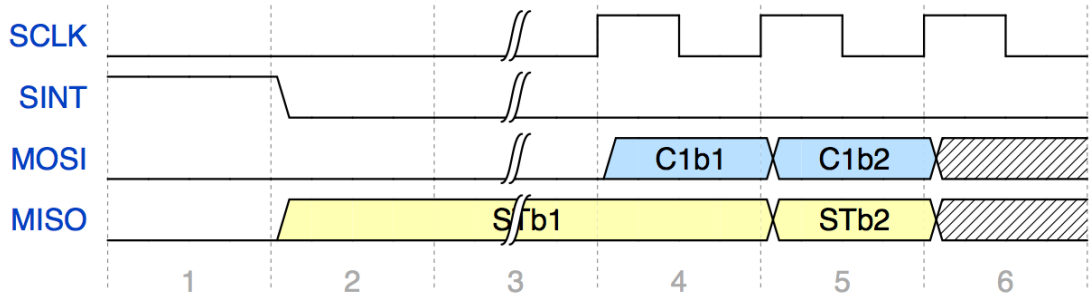

FIGURE 7-11 STARTING OF A TRANSMISSION INITIATED BY THE SLAVE

The first half of the communication ends when the slave has received 24 bits and put SINT in a high level (Figure 7-12). Once the master is prepared to continue with the communication, it changes the SCLK to a high level and writes the first bit of the NOP to MOSI. Then the slave writes the first bit of the status register to MISO.

If the slave doesn't lower SINT in a certain time (a timeout at ISS is reached), the master will suppose that CTC has stopped working properly. In this case, the master will activate SCLK and send the reset command to CTC. At the same time the slave will send the status register allowing ISS to know the reason of the error.

Otherwise, SINT will lower when the slave is ready to send the reply and it will write the first bit of it at MISO. When the master detects the falling edge of SINT it will activate the clock and send the NOP command and read the reply of CTC.

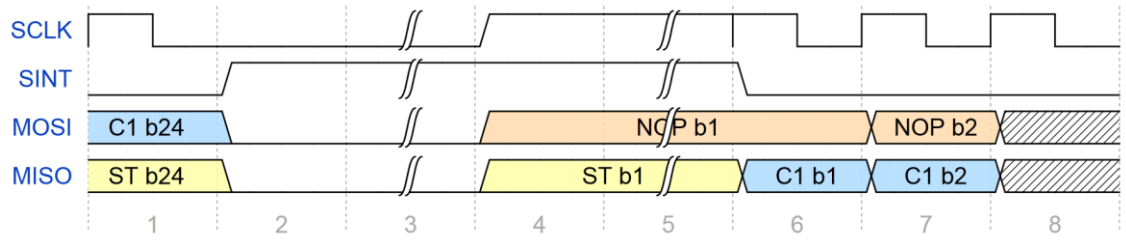

FIGURE 7-12 ENDING OF THE FIRST PART OF THE COMMUNICATION AND STARTING OF THE SECOND ONE

Once the 24 bits of the second part of the communication are transmitted, the master puts SCLK and MOSI in a low state and the slave puts SINT in a high level and MISO in a low level.

The input shift register content of MOSI is checked every cycle to ensure that the RESET command is always executed (CTC-FPGA-R-420). In case it is found, a synchronous reset is executed on all blocks of the CTC firmware. The reset frame is also the only exception to this schema. The reset command only consists of one communication, as the control link is immediately reset.

7.4.6.3. State diagram

The control link has to shift register for the input and the output. The input is checked every cycle to detect a reset command. The output is always loaded with the status register when a transmission finishes.

The state machine controlling the communication has the following states (Figure 7-13):

- Idle: control link is in this state until ISS starts a transmission. The only action performed in this state is, when an error occurred on CTC, changing SINT to inform ISS of a problem.
- sendStatus: in this state the 6 bits of the status code and the 10 bit of the status register are sent to ISS. Once finished the state is changed to sendCRCS.
- SendCRCS: in this state the 8 bits of the CRC-8-CCITT from the previous frame is sent. Then the state is changed to wait.
- Wait: in this state SINT is put on a high level. Once SCLK is at a high level also and the reply to the command is processed, the state is changed to sendReply.
- sendReply: in this state the reply to the received command is sent. In case the received command is invalid or there was a CRC error, the status frame is sent instead. Once the 16 bits were sent, the state is changed to sendCRCR.
- sendCRCR: in this state the 8 bits of the CRC-8-CCITT are sent. Then, the state goes back to idle.

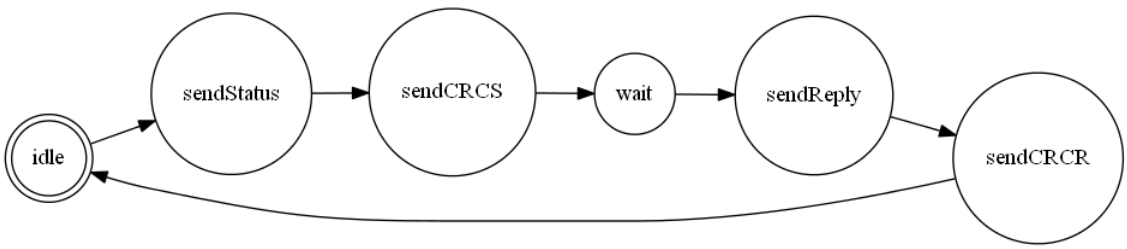

FIGURE 7-13 CONTROL LINK STATE DIAGRAM

An invalid command is one that falls within any of the following situations (CTC-FPGA-R-842):

- The command changes a parameter and the actual working mode is not Idle.
- The command changes a working mode but the actual working mode or the new working mode is not Idle.
- The command changes a parameter to one that is not allowed.
- The command has an unknown command code.
- The CRC check fails.

In any of these cases the reply will be the status register. In case of CRC error the reply will be also a status register, but a bit of the status register will show that the error comes from the CRC.

7.4.6.4. Signals

The input signals are:

- SCLK: clock signal from the Control Link coming from ISS.
- MOSI: data signal from the Control Link coming from ISS.
- frameCounter: 10 bit counter coming from Camera Manager with the actual number images sent since in continuous mode.
- workingMode: 2 bit signal coming from Camera Manager with the actual working mode.
- HKData1 to 8: the H/K values stored from the 8 analog channels.
- Error_HK, error_CLK, error_SC and error_IL: multiple error signals coming from all the blocks indicating an error have occurred on them.
- CALValue: 10 bit signal with the digital value of the STAR 1000 output during the CAL signal.
- outOfRange: signal to activate the out of range flag of the status register.
- Error_OoR_col and error_OoR_row: 10 bit signals with the column and row of the pixel which output was out of range of the ADC input.

The output signals are:

- MISO: data signal from Control Link to ISS.
- SINT: interrupt and control signal from Control Link to ISS.
- CL_End: signal that when the transmission has finished and if there is a change of the working mode, it shall be done when this signal is true.
- changeWorkingMode: signal to activate the change of working mode.
- newWorkingMode: two bit signal with the code of the new working mode.
- Register bank: register bank of the different parameters of the CTC.
- sysRst_n : active low synchronous reset that goes to all the other blocks of the CTC firmware.

7.5. Asynchronous Signals

Only one asynchronous signal is present in the design: IL_CCLK, the image link clock. This clock is the same than the 100 MHz clock coming from the external oscillator but routed through the FPGA (CTC-FPGA-R-920). To increase delay matching between IL_CCLK and IL_DATA (Image Link Data), a buffer cell, the Actel BUFD macro cell, is used. The place and routing tool, unlike other buffer cells, always keeps this cell. Doing so ensures a propagation delay difference between the two signals minor than 2.5 ns (a quarter of the period) in the different implementation tested.

8. FPGA Validation and Verification

The CTC FPGA firmware verification shall be performed at the end of the following phases: pre-synthesis, post-synthesis, post place and route, and post programming. The three first verifications shall be done by simulation with the simulation tool defined in section 5. The post programming validation shall be done with the breadboard and the commercial equivalent FPGA. Since there are electrical requirements, this shall be also tested with the breadboard.

8.1. Functional validation and verification

Different test procedures shall be coded to achieve at least 90% of code coverage (CTC-FPGA-R-120). The code coverage of every test bench shall be saved and they all will be merged in one. From this statement coverage database a report shall be automatically generated. The code coverage report will be included in the FPGA Test Reports document, as stated in the development plan.

8.1.1. Test procedures

8.1.1.1. Outputs during reset

The objective of this test is to validate that the outputs are as specified by requirement CTC-FPGA-R-140.

8.1.1.2. Control Link test

The objective of this test is to validate the Control Link, the register bank and the different working modes. This test shall cover the following requirements (section 6):

- Reset conditioning: CTC-FPGA-R-420
- Configuration parameters: CTC-FPGA-R-500, CTC-FPGA-R-501, CTC-FPGA-R-503, CTC-FPGA-R-504, CTC-FPGA-R-505, CTC-FPGA-R-506, CTC-FPGA-R-510 and CTC-FPGA-R-520.
- Image acquisition control: CTC-FPGA-R-600, CTC-FPGA-R-610, CTC-FPGA-R-620, CTC-FPGA-R-630, CTC-FPGA-R-650, CTC-FPGA-R-660, CTC-FPGA-R-670 and CTC-FPGA-R-680.
- HK Acquisition: CTC-FPGA-R-740
- Control Link Interface: CTC-FPGA-R-800, CTC-FPGA-R-830, CTC-FPGA-R-840, CTC-FPGA-R-841, CTC-FPGA-R-842, CTC-FPGA-R-843, CTC-FPGA-R-844, CTC-FPGA-R-845, CTC-FPGA-R-846, CTC-FPGA-R-847, CTC-FPGA-R-848, CTC-FPGA-R-849 and CTC-FPGA-R-850.
- Image Link Interface: CTC-FPGA-R-900, CTC-FPGA-R-911, CTC-FPGA-R-930, CTC-FPGA-R-940, CTC-FPGA-R-950 and CTC-FPGA-R-960.

8.1.1.3. Continuous Frame Mode Test

The objective of this test is to validate the sensor and image ADC control and the Image Link. This test shall cover the following requirements (section 6):

- Configuration parameters: CTC-FPGA-R-500, CTC-FPGA-R-501, CTC-FPGA-R-503 and CTC-FPGA-R-510.
- Image acquisition control: CTC-FPGA-R-600, CTC-FPGA-R-610, CTC-FPGA-R-620, CTC-FPGA-R-630, CTC-FPGA-R-660 and CTC-FPGA-R-670.

- Control Link Interface: CTC-FPGA-R-830, CTC-FPGA-R-840, CTC-FPGA-R-841, CTC-FPGA-R-843, CTC-FPGA-R-846 and CTC-FPGA-R-848.
- Image Link Interface: CTC-FPGA-R-900, CTC-FPGA-R-911, CTC-FPGA-R-930, CTC-FPGA-R-940, CTC-FPGA-R-950, CTC-FPGA-R-960 and CTC-FPGA-R-970.

8.1.1.4. House Keeping Test

The objective of this test is to validate the H/K ADC Control. No command must be sent from ISS Control. This test will cover the following requirements (section 6): CTC-FPGA-R-700, CTC-FPGA-R-710, CTC-FPGA-R-720, CTC-FPGA-R-730, CTC-FPGA-R-740 and CTC-FPGA-R-750.

8.2. Breadboard Verification

8.2.1. Electrical verification

The electrical test shall be carried out with the CTC and the DPU breadboards. A simplified version of the ISS Control firmware shall be used to send commands to the CTC through the Control Link and read images from the Image Link.

To ensure the electrical requirements are accomplished, an electrical verification shall be made. The electrical verification shall include:

- Inputs and outputs voltage levels of the device, in accordance with CTC-FPGA-R-210.
- Reset levels verification.

8.2.2. System level verification

Python scripts shall be developed to control the ISS Control through an UART from a computer. This allows sending commands and reading images from the CTC. To test the CTC firmware, python scripts shall be developed with the same commands sent to the CTC in the previous tests. The replies to these commands by the CTC shall be automatically tested to match the expected functionalities. In addition, images shall be taken to ensure the proper working of the image sensor, image ADC and image link. All these test and the procedure shall be explained in the CTC Test Plan document.

9. FPGA Test Procedures

All tests are done on the top module at the three development stages. First, at the HDL files prior synthesis to validate the functionalities and to ensure the full code coverage. Then, at post synthesis level to ensure the correct behaviour on this stage. Finally, at the post-layout level with minimum, typical and maximum timing delays to test the resulting firmware with a model as close as possible to the expected working conditions. Also this is why all the tests are performed on the top module, since the timing delays found will be much closer to the real ones than if the tests are performed on bloc basis.

9.1. Test procedures

9.1.1. Outputs during reset

The objective of this test is to validate that the outputs are as specified by requirement CTC-FPGA-R-140 and CTC-FPGA-R-400.

9.1.2. Control Link test

The objective of this test is to validate the Control Link and the different working modes. This test shall have a minimum simulation time of 3 ms. The following actions shall be done in this test in the following order:

ID	Action	Expected result	Requirement ([NR03])
1.	CL: Send a reset frame.	Star_CLK_X and CLK10 shall not change their behaviour. All other signal shall change to their reset values.	CTC-FPGA-R-420 CTC-FPGA-R-630
	MOSI <= '010101010100101011100011' Note that the reset frame only has one transmission.	MISO <= '101110000000000011110110' All other outputs shall be as specified by CTC-FPGA-R-140 requirement.	
2.	CL: Send a frame with invalid CRC.	The reply shall be a status frame as expected for an invalid frame and the CRC error bit shall be true.	CTC-FPGA-R-842
	First transmission: MOSI <= '111111111111111111111111' Second transmission: MOSI <= '001110010100101010011101'	First transmission: MISO <= '101110000000000011110110' Second transmission: MISO <=' 101110100000000011100000' (Note that the wrong CRC bit of the status frame is true)	
3.	CL: Change the working mode to Test Mode.	The reply shall be the same frame as send. The firmware shall enter test mode.	CTC-FPGA-R-600
	First transmission:	First transmission:	

	MOSI <= '00100001010001010011101 01' Second transmission: MOSI <= ' 00111001010001010100111 01'	MISO <= '10111010000000000111000 00' Second transmission: MISO <=' 00100001010001010011101 01'	
4.	The column data sent shall be the same for every row and its content shall be: 06FC 0700 0704 0708 070C 0710 0714 0718 071C 0720 0724 0728 072C 0730 0734 0738 073C 0740 0744 0748 074C 0750 0754 0758 075C 0760 0764 0768 076C 0770 0774 0778 077C 0780 0784 0788 078C 0790 0794 0798 079C 07A0 07A4 07A8 07AC 07B0 07B4 07B8 07BC 07C0 07C4 07C8 07CC 07D0 07D4 07D8 07DC 07E0 07E4 07E8 07EC 07F0 07F4 07F8 07FC 0800 0804 0808 080C 0810 0814 0818 081C 0820 0824 0828 082C 0830 0834 0838 083C 0840 0844 0848 084C 0850 0854 0858 085C 0860 0864 0868 086C 0870 0874 0878 087C 0880 0884 0888 088C 0890 0894 0898 089C 08A0 08A4 08A8 08AC 08B0 08B4 08B8 08BC 08C0 08C4 08C8 08CC 08D0 08D4 08D8 08DC 08E0 08E4 08E8 08EC 08F0 08F4 08F8 08FC 0900 0904 0908	The firmware shall enter the test mode. This means: - The EnSignalExt shall be '1' and SignalExt signals shall be a 5 MHz clock. - The ASEL0 signal shall change to '1' - The rows readout from the sensor shall start at the 448 and continue incrementing in one. - The CAL signal shall be on in accordance with [IR02] during the first row selection. - The ADC clock shall be a 10 MHz clock. - All control signal of the STAR 1000 and RHF1201 shall comply the timing diagrams in [IR02] and [IR03]. - The received data from the Image Link for every row shall be: 01C0 01C1 01C2 01C3 01C4 01C5 01C6 01C7 01C8 01C9 01CA 01CB 01CC 01CD 01CE 01CF 01D0 01D1 01D2 01D3 01D4 01D5 01D6 01D7 01D8 01D9 01DA 01DB 01DC 01DD 01DE 01DF 01E0 01E1 01E2 01E3 01E4 01E5 01E6 01E7 01E8 01E9 01EA 01EB 01EC 01ED 01EE 01EF 01F0 01F1 01F2 01F3 01F4 01F5 01F6 01F7 01F8 01F9 01FA 01FB 01FC 01FD 01FE 01FF 0200 0201 0202 0203 0204 0205 0206 0207 0208 0209 020A 020B 020C 020D 020E 020F 0210 0211 0212 0213 0214 0215 0216 0217	CTC-FPGA-R-610 CTC-FPGA-R-620 CTC-FPGA-R-630 CTC-FPGA-R-640 CTC-FPGA-R-660 CTC-FPGA-R-670

		0218 0219 021A 021B 021C 021D 021E 021F 0220 0221 0222 0223 0224 0225 0226 0227 0228 0229 022A 022B 022C 022D 022E 022F 0230 0231 0232 0233 0234 0235 0236 0237 0238 0239 023A 023B 023C 023D 023E 023F	
5.	CL: Send a frame to change the analog gain to 3 and digital gain to 3.	The reply shall be a status frame as expected for an invalid frame since changing parameters when not in Idle Mode is not allowed.	CTC-FPGA-R-850
	First transmission: MOSI <= '000110110101101001101100' Second transmission: MOSI <= ' 001110010100101010011101'	First transmission: MISO <= '101110001100000010000100' Second transmission: MISO <=' 101110001100000010000100'	
6.	CL: Change the working mode to Idle Mode. The reply shall be the same frame as send.	The firmware shall change to idle mode. All control signals of the STAR 1000 and RHF1201 and the signals EnSignalExt, SignalExt and ASEL0 shall change back to the reset values.	CTC-FPGA-R-600
	First transmission: MOSI <= '000100010100101001110000' Second transmission: MOSI <= '001110010100101010011101'	First transmission: MISO <= '101110001100000010000100' Second transmission: MISO <= '000100010100101001110000'	
7.	CL: Change the working mode to Continuous Frame Mode.	The firmware shall change to Continuous Frame Mode.	

	First transmission: MOSI <= '000010010100101010011000' Second transmission: MOSI <= '001110010100101010011101'	First transmission: MISO <= '101110000000000011110110' Second transmission: MISO <= '000010010100101010011000'	
8.	The column data sent shall be the same for every row and its content shall be: 06FC 0700 0704 0708 070C 0710 0714 0718 071C 0720 0724 0728 072C 0730 0734 0738 073C 0740 0744 0748 074C 0750 0754 0758 075C 0760 0764 0768 076C 0770 0774 0778 077C 0780 0784 0788 078C 0790 0794 0798 079C 07A0 07A4 07A8 07AC 07B0 07B4 07B8 07BC 07C0 07C4 07C8 07CC 07D0 07D4 07D8 07DC 07E0 07E4 07E8 07EC 07F0 07F4 07F8 07FC 0800 0804 0808 080C 0810 0814 0818 081C 0820 0824 0828 082C 0830 0834 0838 083C 0840 0844 0848 084C 0850 0854 0858 085C 0860 0864 0868 086C 0870 0874 0878 087C 0880 0884 0888 088C 0890 0894 0898 089C 08A0 08A4 08A8 08AC 08B0 08B4 08B8 08BC 08C0 08C4 08C8 08CC 08D0 08D4 08D8 08DC 08E0 08E4 08E8 08EC 08F0 08F4 08F8 08FC 0900 0904 0908	The firmware shall work in Continuous Frame Mode. This means: - The rows readout from the sensor shall start at the 448 and continue incrementing in one. - The CAL signal shall be on in accordance with [IR02] during the first row selection. - The ADC clock shall be a 10 MHz clock. - All control signal of the STAR 1000 and RHF1201 shall comply the timing diagrams in [IR02] and [IR03]. - The received data from the Image Link for every row shall be: 01C0 01C1 01C2 01C3 01C4 01C5 01C6 01C7 01C8 01C9 01CA 01CB 01CC 01CD 01CE 01CF 01D0 01D1 01D2 01D3 01D4 01D5 01D6 01D7 01D8 01D9 01DA 01DB 01DC 01DD 01DE 01DF 01E0 01E1 01E2 01E3 01E4 01E5 01E6 01E7 01E8 01E9 01EA 01EB 01EC 01ED 01EE 01EF 01F0 01F1 01F2 01F3 01F4 01F5 01F6 01F7 01F8 01F9 01FA 01FB 01FC 01FD 01FE 01FF 0200 0201 0202 0203 0204 0205 0206 0207 0208 0209 020A 020B 020C 020D 020E 020F 0210 0211 0212 0213 0214 0215 0216 0217 0218 0219 021A 021B 021C 021D 021E 021F 0220 0221 0222 0223 0224 0225 0226 0227 0228	CTC-FPGA-R-610 CTC-FPGA-R-620 CTC-FPGA-R-630 CTC-FPGA-R-640 CTC-FPGA-R-660 CTC-FPGA-R-670

		0229 022A 022B 022C 022D 022E 022F 0230 0231 0232 0233 0234 0235 0236 0237 0238 0239 023A 023B 023C 023D 023E 023F	
9.	CL: Read the working mode.	The reply frame shall show that the CTC is in Continuous Frame Mode.	CTC-FPGA-R-600
	First transmission: MOSI <= '110000010100101011010100' Second transmission: MOSI <= '001110010100101010011101'	First transmission: MISO <= '101110001000000000011001' Second transmission: MISO <= '110000100100101011001001'	
10.	CL: Change the working mode to Idle Mode.	All control signals of the STAR 1000 and RHF1201 shall have the reset values. The reply frame shall be the same as the received frame.	
	First transmission: MOSI <= '000100010100101001110000' Second transmission: MOSI <= '001110010100101010011101'	First transmission: MISO <= '101110001000000000011001' Second transmission: MISO <= '000100010100101001110000'	
11.	CL: Send a frame with a valid CRC but an undefined write command.	The reply shall be a status frame.	CTC-FPGA-R-842
	First transmission: MOSI <= '011111000000000011001110' Second transmission:	First transmission: MISO <= '101110000000000011110110' Second transmission:	

	MOSI <= ‘00111001010010101010011101’	MISO <= ‘10111000000000000011110110’	
12.	CL: Send a NOP frame.	The reply shall be a NOP frame.	CTC-FPGA-R-843
	First transmission: MOSI <= ‘00111001010010101010011101’ Second transmission: MOSI <= ‘00111001010010101010011101’	First transmission: MISO <= ‘10111000000000000011110110’ Second transmission: MISO <= ‘00111001010010101010011101’	
13.	CL: Change the image size to an invalid value (0).	The reply shall be a status frame.	CTC-FPGA-R-500
	First transmission: MOSI <= ‘00001100000000000001110100’ Second transmission: MOSI <= ‘00111001010010101010011101’	First transmission: MISO <= ‘00111001010010101010011101’ Second transmission: MISO <= ‘10111000000000000011110110’	
14.	CL: Read the image size.	The image size value shall be still the reset value (128).	
	First transmission: MOSI <= ‘10001101010010101000011111’ Second transmission: MOSI <= ‘00111001010010101010011101’	First transmission: MISO <= ‘10111000000000000011110110’ Second transmission: MISO <= ‘10001110000000101010110110’	
15.	CL: Change the image size to 64.	The reply shall be the same frame as send.	
	First transmission:	First transmission:	

	MOSI <= '000011010000000001111111' Second transmission: MOSI <= '001110010100101010011101'	MISO <= '101110000000000011110110' Second transmission: MISO <= '000011010000000001111111'	
16.	CL: Change the row delay to one	The reply shall be the same frame as send.	CTC-FPGA-R-503
	First transmission: MOSI <= '000101000000000101001001' Second transmission: MOSI <= '001110010100101010011101'	First transmission: MISO <= '101110000000000011110110' Second transmission: MISO <= '000101000000000101001001'	
17.	CL: Read the row delay.	The row delay value shall be zero.	
	First transmission: MOSI <= '100101010100101011110111' Second transmission: MOSI <= '001110010100101010011101'	First transmission: MISO <= '101110000000000011110110' Second transmission: MISO <= '100101000000000111100010'	
18.	CL: Change the digital and the analog gain to 3.	The reply shall be a status frame since a digital gain of 3 is invalid.	CTC-FPGA-R-505 CTC-FPGA-R-506
	First transmission: MOSI <= '000110110101101001101100' Second transmission: MOSI <= '001110010100101010011101'	First transmission: MISO <= '101110000000000011110110' Second transmission: MISO <= '101110000000000011110110'	

19.	CL: Read the analog and digital gain.	The digital gain value shall be still the reset value (0).	
	First transmission: MOSI <= '100110010100101010000011' Second transmission: MOSI <= '001110010100101010011101'	First transmission: MISO <= '101110000000000011110110' Second transmission: MISO <= '100110000100001010100001'	
20.	CL: Change the digital and analog gain to 0.	The reply shall be the same frame as send.	
	First transmission: MOSI <= '000110000100001000001010' Second transmission: MOSI <= '001110010100101010011101'	First transmission: MISO <= '101110000000000011110110' Second transmission: MISO <= '000110000100001000001010'	
21.	CL: Read the analog and digital gain.	The digital and analog gain shall be still zero.	
	First transmission: MOSI <= '100110010100101010000011' Second transmission: MOSI <= '001110010100101010011101'	First transmission: MISO <= '101110000000000011110110' Second transmission: MISO <= '100110000100001010100001'	
22.	CL: Change the offset subtraction parameter to 0.	The reply shall be the same frame as send.	CTC-FPGA-R-510
	First transmission: MOSI <= '000111000000000011000100'	First transmission: MISO <= '101110000000000011110110'	

	Second transmission: MOSI <= '00111001010001010010011101'	Second transmission: MISO <= '000111000000000011000100'	
23.	CL: Read the offset subtraction parameter.	The offset subtraction value shall be zero.	
	First transmission: MOSI <= '10011101010001010101111' Second transmission: MOSI <= '00111001010001010010011101'	First transmission: MISO <= '10111000000000011110110' Second transmission: MISO <= '10011100000000001101111'	
24.	CL: Change the rolling shutter parameter to 127.	The reply shall be a status frame, since the rolling shutter value send is bigger than the current image size.	CTC-FPGA-R-501
	First transmission: MOSI <= '00100111111111001001010110' Second transmission: MOSI <= '00111001010001010010011101'	First transmission: MISO <= '10111000000000011110110' Second transmission: MISO <= '10111000000000011110110'	
25.	CL: Read the rolling shutter parameter.	The rolling shutter value shall be still the reset value (0).	
	First transmission: MOSI <= '10100101010001011110010' Second transmission: MOSI <= '00111001010001010010011101'	First transmission: MISO <= '10111000000000011110110' Second transmission: MISO <= '10100100000000001001001101'	
26.	CL: Change the rolling shutter parameter to 0.	The reply shall be the same frame as send.	

	First transmission: MOSI <= '00100100000000101110011 0' Second transmission: MOSI <= '00111001010010101001110 1'	First transmission: MISO <= '10111000000000011110110' Second transmission: MISO <= '00100100000000101110011 0'	
27.	CL: Read the rolling shutter parameter.	The rolling shutter value shall be zero.	
	First transmission: MOSI <= '10100101010010101111001 0' Second transmission: MOSI <= '00111001010010101001110 1'	First transmission: MISO <= '10111000000000011110110' Second transmission: MISO <= '10100100000000101001101'	
28.	CL: Change the image offset X parameter to 1000.	The reply shall be a status frame, since the image offset X value send is bigger than the current 1024 minus the image size.	CTC-FPGA-R-504
	First transmission: MOSI <= '00101011111010000000111 1' Second transmission: MOSI <= '00111001010010101001110 1'	First transmission: MISO <= '10111000000000011110110' Second transmission: MISO <= '10111000000000011110110'	
29.	CL: Read the image offset X parameter.	The image offset X value shall be still the reset value (448).	
	First transmission: MOSI <= '10101001010010101000011 0'	First transmission: MISO <= '10111000000000011110110'	

	Second transmission: MOSI <= '00111001010010101010011101'	Second transmission: MISO <= '10101001110000000000111111'	
30.	CL: Change the image offset X parameter to 128.	The reply shall be the same frame as send.	
	First transmission: MOSI <= '00101000100000000000000010' Second transmission: MOSI <= '00111001010010101010011101'	First transmission: MISO <= '10111000000000011110110' Second transmission: MISO <= '00101000100000000000000010'	
31.	CL: Read the image offset X parameter.	The image offset X value read shall be 128.	
	First transmission: MOSI <= '10101001010010101010000110' Second transmission: MOSI <= '00111001010010101010011101'	First transmission: MISO <= '10111000000000011110110' Second transmission: MISO <= '10101000100000000010101001'	
32.	CL: Change the image offset Y parameter to 1000.	The reply shall be a status frame, since the image offset Y value send is bigger than the current 1024 minus the image size.	
	First transmission: MOSI <= '00110011111010001110011 1' Second transmission: MOSI <= '00111001010010101010011101'	First transmission: MISO <= '10111000000000011110110' Second transmission: MISO <= '10111000000000011110110'	

33.	CL: Read the image offset Y parameter.	The image offset Y value shall be still the reset value (448).	
	First transmission: MOSI <= '101100010100101001101110' Second transmission: MOSI <= '001110010100101010011101'	First transmission: MISO <= '101110000000000011110110' Second transmission: MISO <= '101100011100000011010111'	
34.	CL: Change the image offset Y parameter to 128.	The reply shall be the same frame as send.	
	First transmission: MOSI <= '001100001000000011101010' Second transmission: MOSI <= '001110010100101010011101'	First transmission: MISO <= '101110000000000011110110' Second transmission: MISO <= '001100001000000011101010'	
35.	CL: Read the image offset Y parameter.	The image offset Y value read shall be 128.	
	First transmission: MOSI <= '101100010100101001101110' Second transmission: MOSI <= '001110010100101010011101'	First transmission: MISO <= '101110000000000011110110' Second transmission: MISO <= '101100001000000001000001'	
36.	CL: Change the ADC sample point to (1, 1, 0).	The reply shall be the same frame as send.	CTC-FPGA-R-520
	First transmission: MOSI <= '001101000110000000010000'	First transmission: MISO <= '101110000000000011110110'	

	Second transmission: MOSI <= '00111001010001010010011101'	Second transmission: MISO <= '00110100011000000000010000'	
37.	CL: Read the ADC sample point.	The ADC sample point value shall be (1, 1, 0).	
	First transmission: MOSI <= '10110101010001010001000010' Second transmission: MOSI <= '00111001010001010010011101'	First transmission: MISO <= '10111000000000000011110110' Second transmission: MISO <= '10110101011010101011100110'	
38.	CL: Change the ADC sample point to (0, 1, 1).	The reply shall be the same frame as send.	
	First transmission: MOSI <= '00110100001000010101011000' Second transmission: MOSI <= '00111001010001010010011101'	First transmission: MISO <= '10111000000000000011110110' Second transmission: MISO <= '00110100001000010101011000'	
39.	CL: Read the ADC sample point.	The ADC sample point value shall be (0, 1, 1).	
	First transmission: MOSI <= '10110101010001010001000010' Second transmission: MOSI <= '00111001010001010010011101'	First transmission: MISO <= '10111000000000000011110110' Second transmission: MISO <= '10110101001010111010110'	
40.	CL: Send a frame with a valid CRC but an undefined read command.	The reply shall be a status frame.	CTC-FPGA-R-842

	First transmission: MOSI <= '100001010100101001000111' Second transmission: MOSI <= '001110010100101010011101'	First transmission: MISO <= '101110000000000011110110' Second transmission: MISO <= ''	
41.	CL: Change the working mode to Single Frame Mode.	The firmware shall change to Single Frame Mode.	CTC-FPGA-R-600
	First transmission: MOSI <= '000001010100101011101100' Second transmission: MOSI <= '001110010100101010011101'	First transmission: MISO <= '101110000000000011110110' Second transmission: MISO <= '000001010100101011101100'	
42.	The column data sent shall be the same for every row and its content shall be: 0200 0204 0208 020C 0210 0214 0218 021C 0220 0224 0228 022C 0230 0234 0238 023C 0240 0244 0248 024C 0250 0254 0258 025C 0260 0264 0268 026C 0270 0274 0278 027C 0280 0284 0288 028C 0290 0294 0298 029C 02A0 02A4 02A8 02AC 02B0 02B4 02B8 02BC 02C0 02C4 02C8 02CC 02D0 02D4 02D8 02DC 02E0 02E4 02E8 02EC 02F0 02F4 02F8 02FC 0300 0304 0308 0308	The firmware shall work in Continuous Frame Mode. This means: - The rows readout from the sensor shall start at the 128 and continue incrementing in one up to 191. Once reached, the firmware shall change back to Idle Mode. - The CAL signal shall be on in accordance with [IR02] during the first row selection. - The ADC clock shall be a 10 MHz clock. - All control signal of the STAR 1000 and RHF1201 shall comply the timing diagrams in [IR02] and [IR03]. - The Image Link shall receive 64 frames. - The received data from the Image Link for every row shall be:	CTC-FPGA-R-610 CTC-FPGA-R-620 CTC-FPGA-R-630 CTC-FPGA-R-640 CTC-FPGA-R-660 CTC-FPGA-R-670

		0081 0082 0083 0084 0085 0086 0087 0088 0089 008A 008B 008C 008D 008E 008F 0090 0091 0092 0093 0094 0095 0096 0097 0098 0099 009A 009B 009C 009D 009E 009F 00A0 00A1 00A2 00A3 00A4 00A5 00A6 00A7 00A8 00A9 00AA 00AB 00AC 00AD 00AE 00AF 00B0 00B1 00B2 00B3 00B4 00B5 00B6 00B7 00B8 00B9 00BA 00BB 00BC 00BD 00BE 00BF 00C0	
43.	CL: Read the frame counter register.	The value of the frame counter shall be 0.	CTC-FPGA-R-800
	First transmission: MOSI <= '110001010100101011111000' Second transmission: MOSI <= '001110010100101010011101'	First transmission: MISO <= '101110000100000001101011' Second transmission: MISO <= '110001000000000000111000'	
44.	CL: Read the CAL register.	The value of the CAL register shall be 308.	CTC-FPGA-R-650
	First transmission: MOSI <= '110110010100101000111100' Second transmission: MOSI <= '001110010100101010011101'	First transmission: MISO <= '101110000100000001101011' Second transmission: MISO <= '001110010100101010011101'	
45.	CL: Read the H/K Data register 1.	The value of the H/K Data register shall be 0.	CTC-FPGA-R-740

	First transmission: MOSI <= '111000010100101001100001' Second transmission: MOSI <= '001110010100101010011101'	First transmission: MISO <= '101110000100000001101011' Second transmission: MISO <= '111000000000000010100001'	
	CL: Read the H/K Data register 2.	The value of the H/K Data register shall be 0.	
	First transmission: MOSI <= '111001010100101001001101' Second transmission: MOSI <= '001110010100101010011101'	First transmission: MISO <= '101110000100000001101011' Second transmission: MISO <= '111001000000000010001101'	
	CL: Read the H/K Data register 3.	The value of the H/K Data register shall be 0.	
	First transmission: MOSI <= '111010010100101000111001' Second transmission: MOSI <= '001110010100101010011101'	First transmission: MISO <= '101110000100000001101011' Second transmission: MISO <= '111010000000000011111001'	
	CL: Read the H/K Data register 4.	The value of the H/K Data register shall be 0.	
	First transmission: MOSI <= '111011010100101000010101' Second transmission: MOSI <= '001110010100101010011101'	First transmission: MISO <= '101110000100000001101011' Second transmission: MISO <= '111011000000000011010101'	

	CL: Read the H/K Data register 5.	The value of the H/K Data register shall be 0.	
	First transmission: MOSI <= '111100010100101011010001' Second transmission: MOSI <= '001110010100101010011101'	First transmission: MISO <= '101110000100000001101011' Second transmission: MISO <= '111100000000000000010001'	
	CL: Read the H/K Data register 6.	The value of the H/K Data register shall be 0.	
	First transmission: MOSI <= '111101010100101011111101' Second transmission: MOSI <= '001110010100101010011101'	First transmission: MISO <= '101110000100000001101011' Second transmission: MISO <= '111101000000000000111101'	
	CL: Read the H/K Data register 7.	The value of the H/K Data register shall be 0.	
	First transmission: MOSI <= '111110010100101010001001' Second transmission: MOSI <= '001110010100101010011101'	First transmission: MISO <= '101110000100000001101011' Second transmission: MISO <= '111110000000000001001001'	
	CL: Read the H/K Data register 8.	The value of the H/K Data register shall be 0.	
	First transmission: MOSI <= '111111010100101010100101' Second transmission:	First transmission: MISO <= '101110000100000001101011' Second transmission:	

	MOSI <= '001110010100101010011101'	MISO <= '111111000000000001100101'	
46.	CL: Read the column out of range register.	The value of the column out of range register shall be 0.	CTC-FPGA-R-680
	First transmission: MOSI <= '110010010100101010001100' Second transmission: MOSI <= '001110010100101010011101'	First transmission: MISO <= '101110000100000001101011' Second transmission: MISO <= '110010000000000001001100'	
47.	CL: Read the row out of range register.	The value of the row out of range register shall be 0.	
	First transmission: MOSI <= '110100010100101001100100' Second transmission: MOSI <= '001110010100101010011101'	First transmission: MISO <= '101110000100000001101011' Second transmission: MISO <= '110100000000000010100100'	

TABLE 9-1 CONTROL LINK TEST STEPS

Additionally, the previous process will cover the following requirements:

- Control Link Interface: CTC-FPGA-R-830, CTC-FPGA-R-840, CTC-FPGA-R-841, CTC-FPGA-R-842, CTC-FPGA-R-843, CTC-FPGA-R-844, CTC-FPGA-R-845, CTC-FPGA-R-846, CTC-FPGA-R-847, CTC-FPGA-R-848 and CTC-FPGA-R-849.
- Image Link Interface: CTC-FPGA-R-900, CTC-FPGA-R-911, CTC-FPGA-R-930, CTC-FPGA-R-940, CTC-FPGA-R-950 and CTC-FPGA-R-960.

9.1.3. Continuous Frame Mode Test

The objective of this test is to validate the sensor and image ADC control and the Image Link. This test shall have a minimum simulation time of 3 ms. The following actions shall be done in this test in the following order:

ID	Action	Expected result	Requirement ([NR03])
1.	CL: Change the image size to 64.	The reply shall be the same frame as send.	CTC-FPGA-R-500
	First transmission: MOSI <= '000011010000000001111111' Second transmission: MOSI <= '001110010100101010011101'	First transmission: MISO <= '101110000000000011110110' Second transmission: MISO <= '000011010000000001111111'	
2.	CL: Change the row delay to 2.	The reply shall be the same frame as send.	CTC-FPGA-R-503
	First transmission: MOSI <= '001010000000001011100011' Second transmission: MOSI <= '001110010100101010011101'	First transmission: MISO <= '101110000000000011110110' Second transmission: MISO <= '000101000000001011100011'	
3.	CL: Change the offset subtraction parameter to 455.	The reply shall be the same frame as send.	CTC-FPGA-R-510
	First transmission: MOSI <= '000111011100011111101001' Second transmission: MOSI <= '001110010100101010011101'	First transmission: MISO <= '101110000000000001101011' Second transmission: MISO <= '001110111000111111101001'	
4.	CL: Change the rolling shutter offset to 1.	The reply shall be the same frame as send.	CTC-FPGA-R-501

	First transmission: MOSI <= '00100100000101011001111' Second transmission: MOSI <= '00111001010010101001110 1'	First transmission: MISO <= '10111000000000001101011' Second transmission: MISO <= '00100100000101011001111'	
5.	CL: Change the working mode to Continuous Frame Mode.	The reply shall be the same frame as send.	CTC-FPGA-R-600
	First transmission: MOSI <= '00001001010010101001100 0' Second transmission: MOSI <= '00111001010010101001110 1'	First transmission: MISO <= '10111000000000001101011' Second transmission: MISO <= '00001001010010101001100 0'	
6.	The column data sent shall be the same for every row and its content shall be: 06FC 0700 0704 0708 070C 0710 0714 0718 071C 0720 0724 0728 072C 0FFF 0734 0738 073C 0740 0744 0748 074C 0750 0754 0758 075C 0760 0764 0768 076C 0770 0774 0778 077C 0780 0784 0788 078C 0790 0794 0798 079C 07A0 07A4 07A8 07AC 07B0 07B4 07B8 07BC 07C0 07C4 07C8 07CC 07D0 07D4 07D8 07DC 07E0 07E4 07E8 07EC 07F0 07F4 07F8 07FC 0800 0804 0808 The out of range signal shall be true during the following output of the ADC:	The firmware shall work in Continuous Frame Mode. This means: - The rows readout from the sensor shall start at the 448 and continue incrementing in one up to 511. Once reached, the firmware shall start again at row 448. - The CAL signal shall be on in accordance with [IR02] during the first row selection. - The ADC clock shall be a 10 MHz clock. - All control signal of the STAR 1000 and RHF1201 shall comply the timing diagrams in [IR02] and [IR03]. - The Image Link shall receive 64 frames. - The received data from the Image Link for every row	CTC-FPGA-R-502 CTC-FPGA-R-970

	- The first CAL signal - The column 460 In any other case, it shall be zero.	shall be: 0000 0000 0000 0000 0000 0000 0000 0000 0001 0002 0003 0004 03FF 0006 0007 0008 0009 000A 000B 000C 000D 000E 000F 0010 0011 0012 0013 0014 0015 0016 0017 0018 0019 001A 001B 001C 001D 001E 001F 0020 0021 0022 0023 0024 0025 0026 0027 0028 0029 002A 002B 002C 002D 002E 002F 0030 0031 0032 0033 0034 0035 0036 0037 0038	

TABLE 9-2 IMAGE LINK TEST STEPS

Additionally, the previous process will cover the following requirements:

- Image acquisition control: CTC-FPGA-R-600, CTC-FPGA-R-610, CTC-FPGA-R-620, CTC-FPGA-R-630, CTC-FPGA-R-660 and CTC-FPGA-R-670.
- Control Link Interface: CTC-FPGA-R-830, CTC-FPGA-R-840, CTC-FPGA-R-841, CTC-FPGA-R-843, CTC-FPGA-R-846 and CTC-FPGA-R-848.
- Image Link Interface: CTC-FPGA-R-900, CTC-FPGA-R-911, CTC-FPGA-R-930, CTC-FPGA-R-940, CTC-FPGA-R-950 and CTC-FPGA-R-960.

9.1.4. House Keeping Test

The objective of this test is to validate the H/K ADC Control. No command must be send from ISS Control. This test shall have a simulation time of minimum 0.1 s since this is the time need to read all the eight housekeeping values. This test shall validate that the firmware complies with the timing diagram of [IR04].

This test will cover the following requirements: CTC-FPGA-R-700, CTC-FPGA-R-710, CTC-FPGA-R-720, CTC-FPGA-R-730, CTC-FPGA-R-740 and CTC-FPGA-R-750.

ID	Action	Expected result	Requirement ([NR03])
1.	Read previous selected channel and start conversion of channel 1 of the H/K ADC, complying with the timing diagram at [IR04]. Send a value of 0 for the previous channel conversion.	Save a value of 0 for H/K Data 1.	CTC-FPGA-R-700 CTC-FPGA-R-710 CTC-FPGA-R-720 CTC-FPGA-R-730 CTC-FPGA-R-740 CTC-FPGA-R-750
	DOUT <= '0000000000000000'	DIN <= '0000100000000000'	
2.	Read previous selected channel and start conversion of channel 2 of the H/K ADC, complying with the timing diagram at [IR04]. Send a value of 520 for the previous channel conversion.	Save a value of 130 for H/K Data 2.	
	DOUT <= '0000001000001000'	DIN <= '0001000000000000'	
3.	Read previous selected channel and start conversion of channel 3 of the H/K ADC, complying with the timing diagram at [IR04]. Send a value of 528 for the previous channel conversion.	Save a value of 132 for H/K Data 3.	
	DOUT <= '0000001000010000'	DIN <= '0001100000000000'	
4.	Read previous selected channel and start conversion of channel 4 of the H/K ADC, complying with the timing diagram at [IR04]. Send a value of 544 for the previous channel	Save a value of 136 for H/K Data 4.	

	conversion.		
	DOUT <= ‘0000001000100000’	DIN <= ‘1110000000000000’	
5.	Read previous selected channel and start conversion of channel 5 of the H/K ADC, complying with the timing diagram at [IR04]. Send a value of 576 for the previous channel conversion.	Save a value of 144 for H/K Data 5.	
	DOUT <= ‘0000001001000000’	DIN <= ‘1110100000000000’	
6.	Read previous selected channel and start conversion of channel 6 of the H/K ADC, complying with the timing diagram at [IR04]. Send a value of 640 for the previous channel conversion.	Save a value of 160 for H/K Data 6.	
	DOUT <= ‘0000001010000000’	DIN <= ‘1111000000000000’	
7.	Read previous selected channel and start conversion of channel 7 of the H/K ADC, complying with the timing diagram at [IR04]. Send a value of 768 for the previous channel conversion.	Save a value of 192 for H/K Data 7.	
	DOUT <= ‘0000001100000000’	DIN <= ‘1111100000000000’	
8.	Read previous selected channel and start conversion of channel 0 of the H/K ADC, complying with the timing diagram at [IR04].	Save a value of 1023 for H/K Data 8.	

	Send a value of 4095 for the previous channel conversion.		
	DOUT <= ‘0000111111111111’	DIN <= ‘0000000000000000’	

TABLE 9-3 H/K TEST STEPS

10. CTC FPGA CIDL

This section provides the Configuration Item Data List related to the CTC FPGA. The software needed for performing the design and tests of the source code is mentioned. Finally, the files composing the complete FPGA source code and the script employed for automatically performing the synthesis, place & route and the simulations are listed. In this case, a short description of its purpose and the current version is also included.

This document corresponds to the firmware version v12 for the complete CTC FPGA source code, which has been employed for passing CDR. The previous versions have been developed and tested in previous breadboards.

10.1. Software for designing and testing

Software	Purpose	Version
Actel Libero IDE	Project manager	v9.1 SP5
Synplify Premir with Design Planner	Synthesis of the source code	G-2012.09-SP1
Designer	Place and route of the source	v9.1 SP5
Questa Sim-64	Simulation of the source code	V10.1d

TABLE 10-1. SOFTWARE FOR DESIGNING AND TESTING

10.2. Source code

Item name	Description	File version
addCRC.vhd	Add the CRC to the Image Link	1391
CameraManager.vhd	Manage the CTC working mode	1391
ControlLink.vhd	Manage the communication with ISS Control	1391
CTCamera_top.vhd	Top level module of the CTC	1391
dataCount.vhd	Count the pixels send by the CTC	1391
FPGA.vhd	Connect the different modules of the CTC	1391
FPGA_pkg.vhd	Package with the different signal types for the CTC.	1391
FPGA_tc_d1_mod.vhd	Generate the synchronization signal between clock domains.	1391

genClk.vhd	Generate the 10 MHz clocks of the CTC	1391
HKSensorRead.vhd	Manage the communication with the H/K ADC.	1391
ImageLink.vhd	Read and send the image data	1391
ImageSensorControl.vhd	Control the image ADC and sensor.	1391
InOutBlock.vhd	Manage the low level communication with ISS Control.	1391

TABLE 10-2. FILES COMPOSING THE FIRMWARE VERSION V12 OF THE CTC FPGA SOURCE CODE

10.3. Script files structure

The following table contains the script files structure employed for executing the different tasks related to every module: synthesis, place & route and three simulations (pre-synthesis, post-synthesis and post-layout).

File name	Purpose	File version
CTC.sh	Main script which execute the different steps to produce and test the firmware	1454
script_synthesis.tcl	It performs the synthesis of the source code	1454
script_designer.tcl	It performs the place & route of the synthesized code	1350
run_pre_synthesis.do	It performs the pre-synthesis simulation of the source code	1391
run_post_synthesis.do	It performs the post-synthesis simulation of the VHDL files obtained after the synthesis	1391
run_post_layout.do	It performs the post-layout simulation of the back-annotate files obtained after the place & route	1550

TABLE 10-3. SCRIPT FILES STRUCTURE

11. FPGA Test Reports

The scope of this section is to provide a unique place with all the reports generated during the development phase of the CTC FPGA, as defined in the CTC FPGA Development Plan.

This document corresponds to CIDL of section 10.

11.1. Introduction

This document contains:

- Test bench results (chapter 11.2).
- Code coverage report (chapter 3).
- Synthesis log from Synopsis Synplify (synthesis directory, attached in the zip file).
- Placement and routing log from Actel Designer (designer directory, attached in the zip file).

11.2. Test bench report

The following section describes the output of the test benches defined in the CTC FPGA Test Procedure [NR02].

11.2.1. Pre Synthesis

The log file of the test bench run with the before synthesis is attached to the zip file (vsim/report/presynth.log).

No problems have been found. This run was also used to generate the code coverage report.

11.2.2. Post Synthesis

The log file of the test bench run with synthesis vhdl file is attached to the zip file (vsim/report/postsynth.log).

No problems have been found.

11.2.3. Post Layout

The log file of the test bench run with the post layout file is attached to the zip file (vsim/report/postlayout.log). All the test benches have been tested three times, with minimum, typical and maximum propagation delays.

11.2.3.1. Minimum delay

No errors have been found.

11.2.3.2. Typical delay

No errors have been found.

11.2.3.3. Maximum delay

No errors have been found.

11.3. Waveforms inspection

Specifications test-benches are based on comparing the output signals for every module with the expected ones. This implies that, if these signals are not identical at the comparing moment, warnings will appear in the final report.

This way of testing does not allow detecting glitches. Since the glitch detection can be performed easily by visual inspection, it has not been necessary to prepare another different test, but the output waveforms generated during the five simulations have been observed and analysed.

In the Table 11-1 the results from glitch detection are shown.

Test bench	Timing Delay	Waveform file	Glitches detected
Control Link Test	Maximum	CL_max.wlf	NO
	Typical	CL_typ.wlf	NO
	Minimum	CL_min.wlf	NO
Continuous Frame Mode Test	Maximum	IL_max.wlf	NO
	Typical	IL_typ.wlf	NO
	Minimum	IL_min.wlf	NO
House Keeping Test	Maximum	HK_max.wlf	NO
	Typical	HK_typ.wlf	NO
	Minimum	HK_min.wlf	NO

TABLE 11-1 GLITCH DETECTED

11.4. Code coverage report

11.4.1. Test Overview

The test benches have been designed to provide coverage of all reachable statements of the VHDL code. The uncovered statements will be justified in this section and shall be due to the error states of the FSM, existing for single events, or error signals related to these error states.

The full HTML code coverage statistic can be found attached in the zip file (CCReport\index.html).

11.4.2. Coverage statistics

A summary of the coverage statistics is shown at Table 11-2. The non-covered lines are explained in the following sections.

File	Active	Hits	Misses	Covered (%)
CTCamera_top.vhd	5	5	0	100.0
FPGA.vhd	69	69	0	100.0
FPGA_tc_d1_mod.vhd	2	2	0	100.0
HKSensorRead.vhd	176	170	6	96.6
CameraManager.vhd	123	123	0	100.0
ControlLink.vhd	277	277	0	100.0
ImageSensorControl.vhd	316	300	16	94.9
ImageLink.vhd	325	316	9	97.2
InOutBlock.vhd	285	270	15	94.7
addCRC.vhd	44	44	0	100.0
dataCount.vhd	48	47	1	97.9
genClk.vhd	63	61	2	96.9

TABLE 11-2 CODE COVERAGE STATISTICS

11.4.2.1. /u_DUT/u_CTCamera/u_HKSensorRead

Lines	Description
155	Error signal *errorCount* set to true. This statement can only be reach if a SEU changes the counter *bCounter* to a value out of bonds.
459-462	FSM error state. This state can only be reached if a SEU changes the state to an undefined state and the parity check fails.
474	FSM parity check fail, only reachable if a SEU changes the state to a state with even parity.

TABLE 11-3 HKSENSORREAD UNCOVERED STATEMENTS

11.4.2.2. /u_DUT/u_CTCamera/u_ImageSensorControl

Lines	Description
609-623	FSM error state. This state can only be reached if a SEU changes the state to an undefined state and the parity check fails.
650	FSM parity check fail, only reachable if a SEU changes the state to a state with even parity.

TABLE 11-4 IMAGESENSORCONTROL UNCOVERED STATEMENTS

11.4.2.3. /u_DUT/u_CTCamera/u_CameraManager/u_genClk

Lines	Description
175-176	Error signal *error* set to true and counter *clkCounter* reset to zero. This statement can only be reach if a SEU changes the counter *clkCounter* to a value out of bonds.

TABLE 11-5 GENCLK UNCOVERED STATEMENTS

11.4.2.4. /u_DUT/u_CTCamera/u_ImageLink

Lines	Description
698	Error signal *errorSer* set to true. This statement can only be reach if a SEU changes the counter *position* to a value out of bonds.
883-889	FSM error state. This state can only be reached if a SEU changes the state to an undefined state and the parity check fails.
909	FSM parity check fail, only reachable if a SEU changes the state to a state with even parity.

TABLE 11-6 IMAGELINK UNCOVERED STATEMENTS

11.4.2.5. /u_DUT/u_CTCamera/u_ImageLink/u_dataCount

Lines	Description
129	Error signal *errorCC1* set to true. This statement can only be reach if a SEU changes the counter *counter* to a value out of bonds.

TABLE 11-7 DATACOUNT UNCOVERED STATEMENTS

11.4.2.6. /u_DUT/u_CTCamera/u_ControlLink/u_InOutBlock

Lines	Description
656	Only reachable if the error signal due to SEU of the Control Link block is true. This statement changes the bit of the status frame corresponding to the Control Link error to true.
662	Only reachable if the error signal due to SEU of the Image Sensor Control block is true. This statement changes the bit of the status frame corresponding to the Control Link error to true.
667	Only reachable if the error signal due to SEU of the Image Link block is true. This statement changes the bit of the status frame corresponding to the Control Link error to true.
672	Only reachable if the error signal due to SEU of the H/K Sensor Read block is true. This statement changes the bit of the status frame corresponding to the Control Link error to true.
677	Only reachable if the error signal due to SEU of the genClk block is true. This statement changes the bit of the status frame corresponding to the CLK error to true.
682	Only reachable if some error signal due to SEU is true. Used to activate the SINT signal to inform ISS Control of a SEU at the CTC.
762, 779, 807, 822	Changes the FSM state to the error state when the counter gets out of bonds due a SEU.
836-837	Only reachable if some SEU changes the counter *counter_1* to an unexpected value. This statement allows sending again the status frame.
846	FSM parity check fail, only reachable if a SEU changes the state to a state with even parity.
849	Sets to true the error signal of the Control Link if the state of the FSM is the error state.
855	Changes the FSM state to the error state when the parity check fails.

TABLE 11-8 INOUTBLOCK UNCOVERED STATEMENTS

12. FPGA Data Sheet

12.1. Scope

The scope of this section is to gather all technical data of the design, as required by [11]. Most of this content has been already included in previous parts of the document, but to have a chapter meeting the requirements of the standard, the contents is duplicated.

12.2. Introduction

The CTC FPGA main function is to provide the correlation images for the ISS. The following functions must be performed by the FPGA:

- Control the image sensor (STAR 1000) and image ADC (RHF1201) for image readout.
- Provide a register bank to change image readout behaviour.
- SPI variant communication with the DPU to change the working parameters (Control Link).
- Send the image data to the DPU (Image Link).
- Obtain H/K data (power supplies and temperature) with a SPI ADC (ADC128S102).

Figure 12-1 shows a block diagram of the CTC.

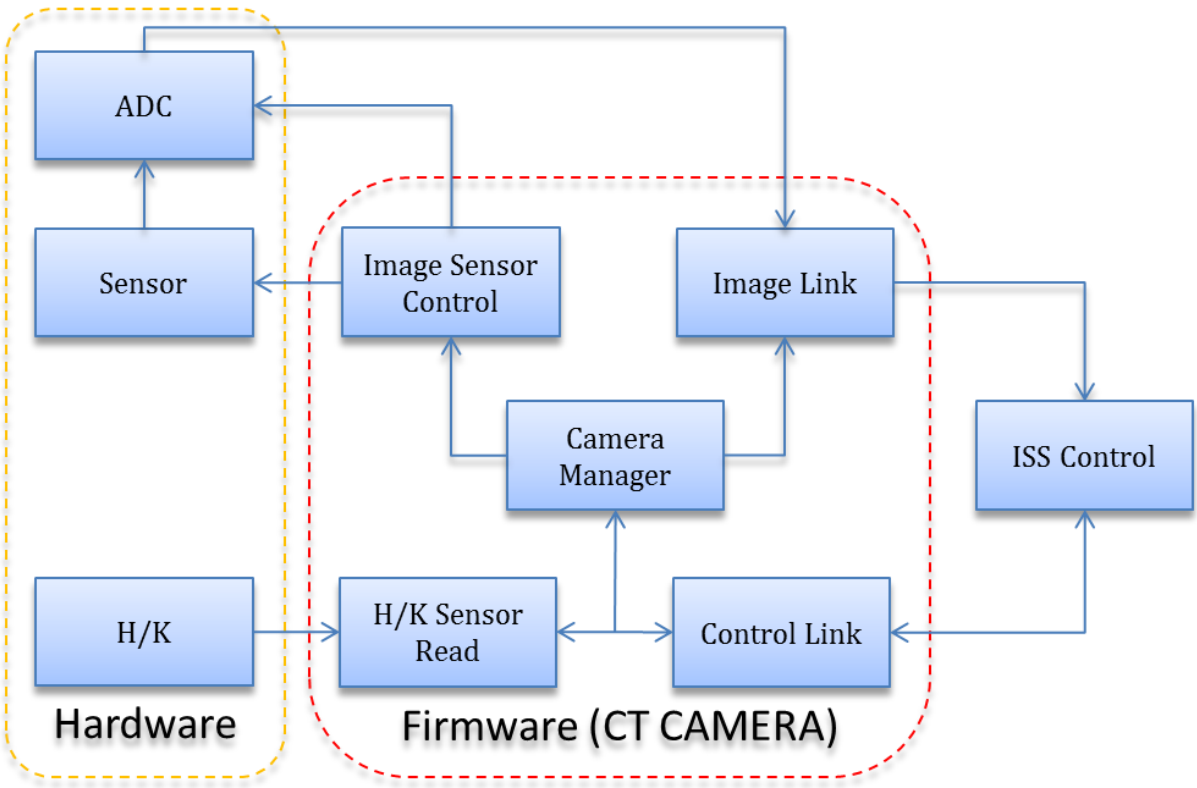

FIGURE 12-1 CTC FIRMWARE BLOCKS

The external oscillator frequency is 100 MHz. From this clock, a 10 MHz clock is generated. The 100 MHz clock is used for 10 MHz clock generation and at the Image Link block. The other blocks work at the 10 MHz frequency.

The FPGA device selected for managing the CT Camera functionalities is the Microsemi (Actel) RTSX72SU with speed grade -1 in CQFP208 package version. This device has been selected for the following reasons:

- Adequate number of I/O´s and low pinout dimension
- Robustness in radiation environment
- All register are TMR
- Low power consumption
- Extensive usage in space applications

12.3. Interfaces

12.3.1. Image Link

12.3.1.1. Signals

- IL_IDAT: serial data signal.
- IL_CCLK: asynchronous 100 MHz clock. This clock is the same than the 100 MHz clock coming from the external oscillator but routed through the FPGA.

12.3.1.2. Frame

The Image Link data is sent with the less significant bit first (LSB) with words of 10 bits. The frame length depends upon the image size. In case of an image size of 128 by 128 the frame structure is shown in Table 12-1. For a different size, the pixel data content will be equal to the image size multiplied by 10.

Bit sent	1-10	11-20	21-1300	1301-1316
Content	Preamble (0x111)	Row sent	Pixel data	CRC-16-CCITT

TABLE 12-1 IMAGE LINK FRAME

The first word sent is a preamble with value 0x111. The second word sent is the relative value of the actual row being sent. Then, the data is sent. Finally, a CRC-16-CCITT is added with a LFSR implementation as shown in Figure 12-2.

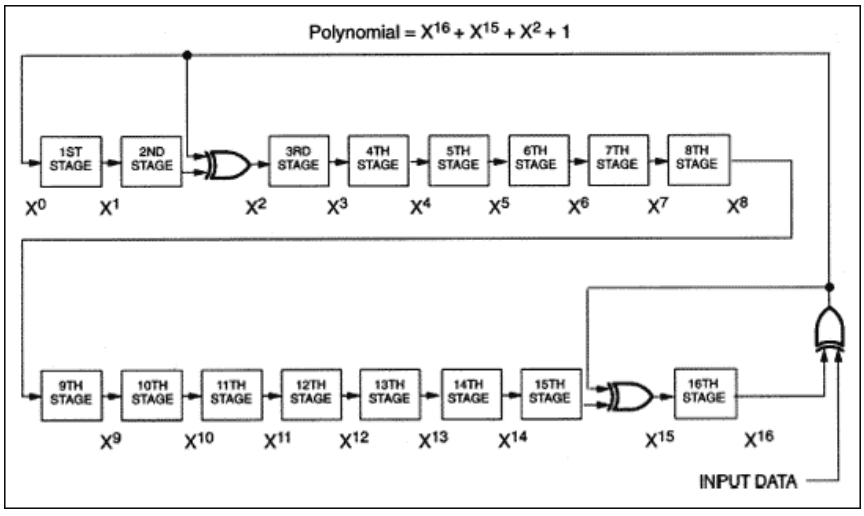

FIGURE 12-2 IMAGE LINK CRC-16-CCITT

12.3.2. Control Link

12.3.2.1. Control link signals

- SCLK: 1 MHz clock generated by ISS ([NR01] CTC-FPGA-R-830). On its rising edge the data of the channel is read and at the falling edge the data is changed. Transmissions of one word consist of 24 pulses with a longer high level at the end used, in conjunction with SINT, to synchronise the state between the master and the slave.
- MOSI (Master Output Slave Input): CTC reads the bit sent by ISS at the falling edge of SCLK and ISS writes the bit to be sent to CTC at the rising edge.
- MISO (Master Input Slave Output): ISS reads the bit sent by CTC at the falling edge of SCLK and CTC writes the bit to be sent to ISS at the rising edge.
- SINT (Slave controlled serial Interrupt): signal controlled by CTC with two different functions. When a communication starts, SINT goes in a low state and once the 24 bits are received, SINT goes again to a high state. Also, if no transmission is in progress and an error occurs at CTC, SINT goes low to inform ISS that an internal error has happened.

12.3.2.2. Frame

The frame of the control link has the next structure (Table 12-2):

Bit position	1	2-6	7-16	17-24
Code	Read/Write (R/W)	Command (COM)	Value (VAL)	CRC-8 (CRC)

TABLE 12-2 CONTENT OF A CONTROL LINK FRAME

The first bit of the transmission show if it is a read (1) or write (0) command. A write command is a command that changes the working mode or the value of a parameter at CTC. The second to the sixth bit indicates which command we want to execute following the codes of Table 12-3 for parameters commands and Table 12-4 for working mode commands. The seventh to the sixteenth bit content is the data value of the command. In case a command doesn't require any value to be sent, it will have a fixed pattern. The seventh bit transmitted is the most significant bit (MSB first).The bit seventeenth to twenty-fourth content is a CRC-8 with polynomial 0xD5 ($x^8 + x^7 + x^6 + x^4 + x^2 + 1$).

R/W	CODE	COMMAND	VALUE
0	00001	Mode Single Frame Read	01010 01010
0	00010	Mode Continuous Frame Read	01010 01010
0	00100	Mode Idle	01010 01010
0	01000	Mode Test	01010 01010
1	10000	Get current mode	XX010 01010
0	10101	RESET	01010 01010
0	01110	NOP	01010 01010
1	01110	STATUS	XXXXX XXXXX

TABLE 12-3 WORKING MODE COMMANDS

In the Table 12-3 and Table 12-4, an X on the read/write field means that the command can be a read or a write command. For the value fields, an X means that this bit depends on the actual value to be transmitted. Some commands don't require a frame of this

length, but as we don't need a fast transmission rate, it's preferred to send frames of fixed length to increase reliability.

R/W	CODE	COMMAND	VALUE
X	00011	Image Size	XXXXX XXX10
X	00101	Delay	XXXXX XXXXX
X	00110	Analog & Digital Pixel Gain	AA010 DD010
X	00111	Offset subtraction	XXXXX XXXXX
X	01001	Rolling Shutter Offset	XXXXX XX010
X	01010	Image Offset X	XXXXX XXXXX
X	01100	Image Offset Y	XXXXX XXXXX
X	01101	ADC Phase Shift	010XX 0101X
1	10001	Frame Counter	XXXXX XXXXX
1	10010	Column Out of Range	XXXXX XXXXX
1	10100	Row Out of Range	XXXXX XXXXX
1	10110	CAL Value	XXXXX XXXXX
1	11000	H/K Data 1	XXXXX XXXXX
1	11001	H/K Data 2	XXXXX XXXXX
1	11010	H/K Data 3	XXXXX XXXXX
1	11011	H/K Data 4	XXXXX XXXXX
1	11100	H/K Data 5	XXXXX XXXXX
1	11101	H/K Data 6	XXXXX XXXXX
1	11110	H/K Data 7	XXXXX XXXXX
1	11111	H/K Data 8	XXXXX XXXXX

TABLE 12-4 PARAMETER COMMANDS

Any unknown or invalid command is replied with a STATUS command. When CTC is in any other state than Idle the only valid commands are Mode Idle, Reset and NOP. Any other command will be treated like an invalid command and so will be replied with a STATUS.

The value meaning varies with the command. In most cases it will directly mean the value for the command. If this value is out of the range defined below the frame will be treated as invalid (without changing the CTC register value) and so replied with a STATUS.

- Image Size: It must be between 64 and 128. The default value is 128.
- Analog & Digital Pixel Gain: the two first bits of value (bits 7 and 8 of the frame) contain the analogic gain and the bits five and six of value (bits twelve and thirteen of the frame) contain the digital gain. The analogic gain sets the star 1000 output gain (x1, x2, x4 and x8). The digital gain must be between zero and two. With a digital gain of zero the CTC sends the ten lower bits of the ADC and with a gain of two it uses the ten most significant bits of the ADC.
- Rolling Shutter Offset: It must be between zero and the Image Size minus one. The default value is zero.
- Image offset: It must be between zero and 1024 minus Image Size. The default value is 448.
- ADC Phase Shift: if the last bit is set to zero the base phase difference between the ADC sample clock and the Star 1000 output clock is of 180º, and if set to one there is no extra phase difference between the two clocks. The value set at the third and fourth bit adds a phase difference of about 36º multiplied by this value, added to the previous one.
- Get current mode: the codification is the following: idle (00), single mode (01), continuous mode (10) and test mode (11).

- Status: it contains the internal status register with the following information:
  - CRC Error (1 bit): if true there was a CRC error in the last transmission.
  - ADC Out of Range (1 bit): if true it means that the analog input to the ADC is out of the full-scale range. The two registers ColumnOutOfRange and RowOutOfRange shows the pixel where this happened. This flag is cleared when columnOutOfRange is read.
  - Working Mode (2 bits): shows the current working mode of CTC. Its value is the same as the content of get current mode.
  - Error in some CTC block (6 bits): The first bit means an error in the Control Link, the second is fixed to 0, the third in the Image Sensor Control, the fourth in Image Link, the fifth in the H/K Sensor Read and the last one in the block generating the Star 1000 clock (Table 12-5).

Bit transmitted	1	2	3- 4	5	6	7	8	9	10
Code	CRC Error	ADC Out Of Range	Working Mode	Error CL	'0'	Error SC	Error IL	Error HK	Error CLK

TABLE 12-5 STATUS CONTENT

- Other working mode commands: its value is irrelevant and so fixed to 0x014A.

12.3.2.3. Communication

This link is a bidirectional synchronous communication working at 1 Mbps. The word length of the control link is 24 bits. The clock starting value is zero (CPOL zero), with the data read on the falling edge (CPHA one) and with the most significant bit at the beginning.

The communication consists of two transmissions. At the first transmission cycle, the master sends the command to be executed by CTC and the slave sends a STATUS frame. At the second transmission, the master sends a NOP frame and the slave the reply of the previous received command. In case of a parameter write command, change state command or a NOP frame, the reply will be exactly the same received frame. And for a parameter read command, the value field will contain the data. A timing diagram of a complete communication is shown in Figure 12-3.

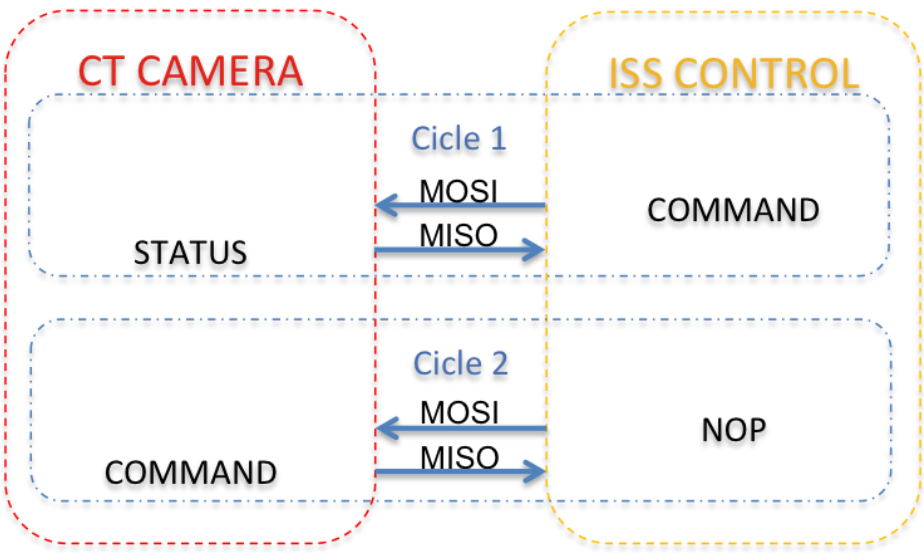

FIGURE 12-3 CONTROL LINK COMMUNICATION

A normal transmission initiated by the master (Figure 12-4) starts with the SCLK signal going to a high level. At the same time the master writes the first bit at MOSI. Once the slave is aware of the SCLK change, it writes the first bit of the status register to MISO. When the slave it's ready to start the transmission, it puts the SINT signal in a low level. Then, it also writes the first bit to be sent in MISO. In the case of the first cycle of the transmission the data to be sent is the status register. When the master detects the falling edge of SINT, SCLK starts working as the clock of the communication. The values of MOSI and MISO change at the rising edge and are read on the falling edge of SCLK. Once the slave has received 24 SCLK pulses it will put SINT in a high level again. If the master has sent the 24 pulses and doesn't see the rising edge of SINT it will mean that some interference in the channel has masked some pulse. Therefore, it will continue sending pulses until SINT rises. This transmission will be lost but the synchronization between master and slave will be regained.

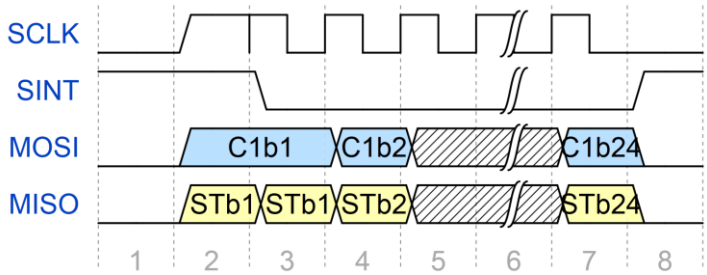

FIGURE 12-4 STARTING OF A TRANSMISSION INITIATED BY THE MASTER

If the slave detects an error in the CTC, it can ask the master to start a communication (Figure 12-5). In this case, while SCLK is at a low level, the slave lowers SINT and writes the first bit of the status register to MISO. When the master detects the change of SINT and wants to start the transmission, it activates SCLK and the communication goes on as usual.

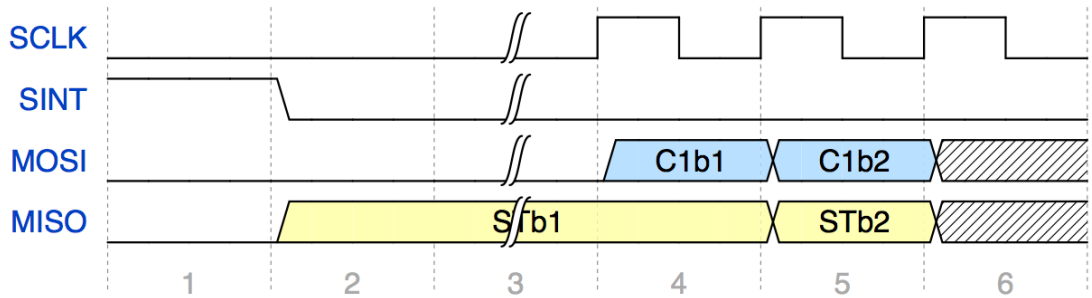

FIGURE 12-5 STARTING OF A TRANSMISSION INITIATED BY THE SLAVE

The first half of the communication ends when the slave has received 24 bits and put SINT in a high level (Figure 12-6). Once the master is prepared to continue with the communication, it changes the SCLK to a high level and writes the first bit of the NOP to MOSI. Then the slave writes the first bit of the status register to MISO.

If the slave doesn't lower SINT in a certain time (a timeout at ISS is reached), the master will suppose that CTC has stopped working properly. In this case, the master will activate SCLK and send the reset command to CTC. At the same time the slave will send the status register allowing ISS to know the reason of the error.

Otherwise, SINT will lower when the slave is ready to send the reply and it will write the first bit of it at MISO. When the master detects the falling edge of SINT it will activate the clock and send the NOP command and read the reply of CTC.

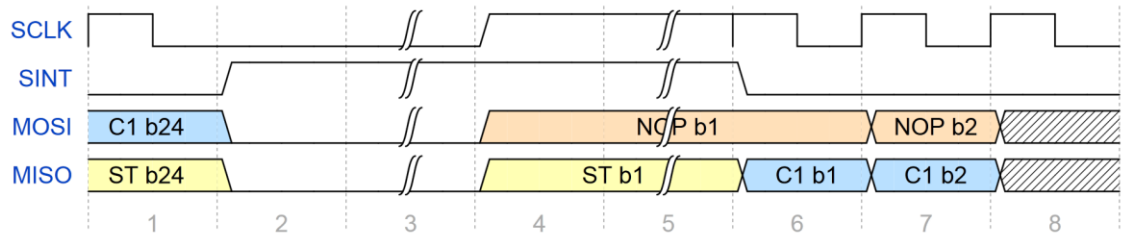

FIGURE 12-6 ENDING OF THE FIRST PART OF THE COMMUNICATION AND STARTING OF THE SECOND ONE

Once the 24 bits of the second part of the communication are transmitted, the master puts SCLK and MOSI in a low state and the slave puts SINT in a high level and MISO in a low level.

The input shift register content of MOSI is checked every cycle to ensure that the RESET command is always executed. In case it is found, a synchronous reset is executed on all blocks of the CTC firmware. The reset frame is also the only exception to this schema. The reset command only consists of one communication, as the control link is immediately reset.

12.4. Register definitions

Shows the different parameter registers of the FPGA.

Register name	# Bits (rw)	Reset value	Short description
Working Mode	2-rw	0	Defines the working mode of the CTC. Start in Idle Mode. The parameters are only writable when the CTC is in Idle Mode.
Image Size	7-rw	128	Defines the size of the frames to read from the camera.
Delay	10-rw	0	Defines the row delay during image readout.
Analog & Digital Pixel Gain	(2,2)-rw	(0, 0)	Set the analog gain (configurable gain of the STAR 1000) and the digital gain (bit shift right of the 12 bits from the ADC).
Offset subtraction	10-rw	0	Value subtracted to every pixel before sending.
Rolling Shutter Offset	6-rw	0	Defines the rolling shutter value applied to the STAR 1000.
Image Offset X	10-rw	448	X offset applied to the readout area of the STAR 1000.
Image Offset Y	10-rw	448	Y offset applied to the readout area of the STAR 1000.
Frame Counter	10-r	0	Counter with the number of frames send by the CTC since entering Continuous frame mode. It's reset when changing to Idle Mode.
Column Out of	10-r	0	Last column out of range of the ADC input.

Range			
Row Out of Range	10-r	0	Last row out of range of the ADC input.
CAL Value	10-r	0	Digital value of the STAR 1000 output during CAL signal.
H/K Data 1	10-r	0	Value of the channel 1 from the H/K ADC.
H/K Data 2	10-r	0	Value of the channel 2 from the H/K ADC.
H/K Data 3	10-r	0	Value of the channel 3 from the H/K ADC.
H/K Data 4	10-r	0	Value of the channel 4 from the H/K ADC.
H/K Data 5	10-r	0	Value of the channel 5 from the H/K ADC.
H/K Data 6	10-r	0	Value of the channel 6 from the H/K ADC.
H/K Data 7	10-r	0	Value of the channel 7 from the H/K ADC.
H/K Data 8	10-r	0	Value of the channel 8 from the H/K ADC.

TABLE 12-6 REGISTER DEFINITIONS

12.4.1. Working mode

This parameter defines the working mode of the CTC. The different working modes are explained in chapter 0. To change the working mode the frame defined in Table 12-4 must be sent.

12.4.2. Image Size

This parameter defines the size of the images read out of the STAR 1000. This value must be between 64 and 128. Also, the addition of the image size and Image Offset X or Y must be below 1024.

12.4.3. Delay

This parameter adds a delay before reading the columns of the STAR 1000. The delay is equal to the value multiplied by 100 ns plus 100 ns (minimum of two cycles of the 10 MHz clock). The delay lowers the number of frames per second and increases the integration time. Any value between 0 and 1023 is valid.

12.4.4. Analog and digital gain

This parameter is used to increase the pixel resolution. The analog gain acts directly on the STAR 1000 sensor applying an analog gain of x1, x2, x4 or x8 (digital values 0, 1, 2, 3 respectively). The digital gain shifts the output of the image ADC. Since only 10 bits are sent and the ADC has 12 bit resolution, only a digital gain of 0, 1 and 2 is allowed. With a digital gain of 0 the 10 most significant bits are sent and with a digital gain of 2 the 10 least significant bits.

12.4.5. Offset subtraction

The value of this parameter is subtracted to every pixel data sent. Any value between 0 and 1023 is valid. Using this value allows a first dark correction. In conjunction with the digital gain, this correction may allow having a better output range: i.e. if the maximum output value is 530 and the minimum dark value is 30, setting the offset subtraction to 30 and the digital gain to 1 will allow having a pixel data range from about 1000 DN to 0.

12.4.6. Rolling shutter offset

This value allows changing the rolling shutter of the image. Setting the value to zero, no rolling shutter is applied. A value of one means a reset of a row is performed one row before the actual readout. This means the integration time will be equal to the time of reading one row. This value can be from zero to the image size minus one.

12.4.7. Image offset X and Image offset Y

This parameter changes the read out area of the sensor. The value must be in the range of 0 to 1023 – Image Size.

12.4.8. Frame counter

10 bit read only value indicating the number of frames sent since entering continuous mode. This value resets to zero when in Idle Mode.

12.4.9. Column out of range and Row out of range

10 bits read only values containing the relative row and column when the out of range signal of the ADC was true for the first time.

12.4.10. H/K data 1 to 8

10 bits read only values with the digital value of the different channels of the H/K ADC.

12.4.11. Functionalities

The main functionality of the firmware is to control the sensor (STAR 1000) and the image ADC (RHF1201).

12.4.11.1. Image readout

12.4.11.1.1. Row read and reset timings

The Figure 12-7 shows a read of a row and a reset from another one. The reset of another row is used to lower the integration time of a pixel. When the rolling shutter is zero this reset is not performed.

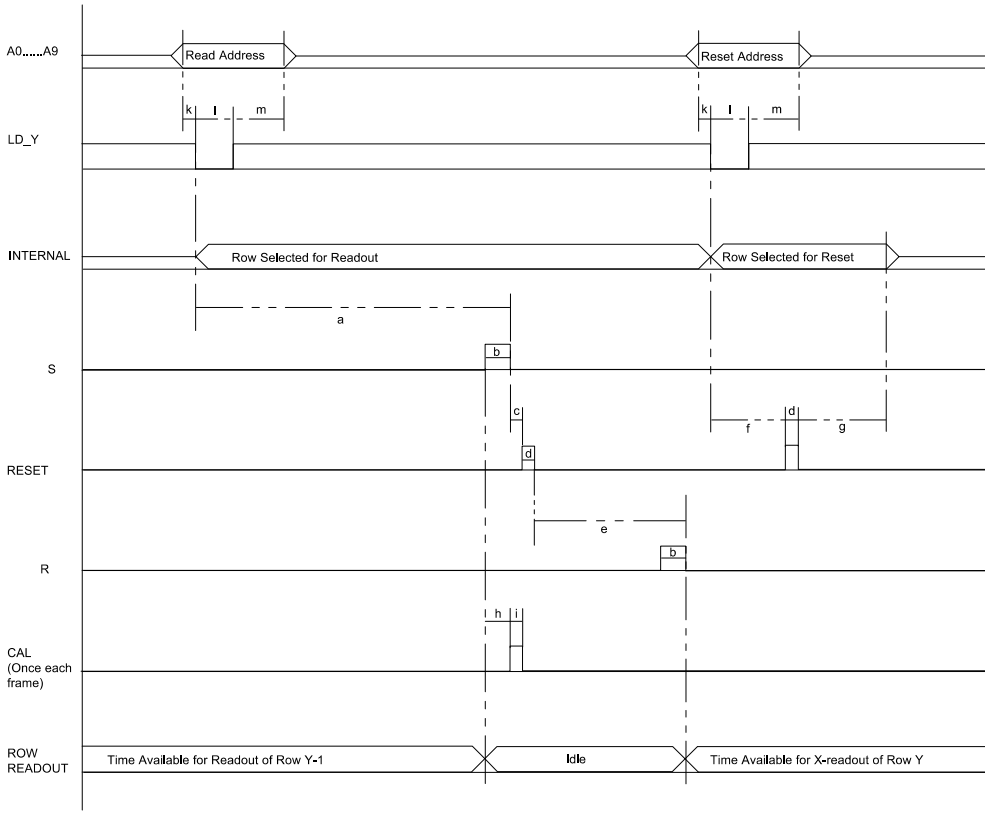

FIGURE 12-7 READ AND RESET OF A ROW

Taking in to account that the block is working at 10 MHz, Table 12-7 shows the datasheet typical timing ([IR01]) and the implemented one.

Therefore, the total needed time to read a row corresponds to k+a+c+d+e=5.6 us. And for the reset, the time is k+f+d+g=0.5 us. The most relevant contribution to the row read process is the time needed by the internal row selection (timing a). Since the integration time must be configurable, a 10 bits parameter writeable by ISS Control allows adding extra delay to the default value of timing a.

Symbol	Datasheet typical time (ns)	Waiting cycles	Implemented waiting time (ns)
a	3600	36	3600
b	400	4	400
c	100	1	100
d	200	2	200
e	1600	16	1600
f	100	1	100
g	100	1	100
h	200	2	200
i	1000	10	1000
k	10	1	100
l	20	1	100
m	10	1	100

TABLE 12-7 ROW READ AND RESET TIMING

12.4.11.2. Column read timings

The column read is done as shown in Figure 12-8.

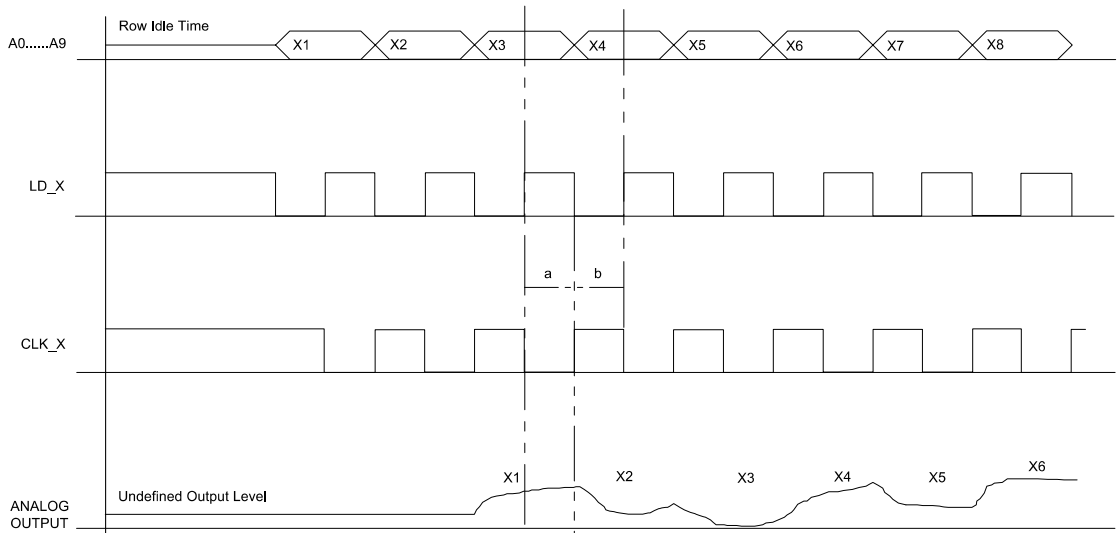

FIGURE 12-8 COLUMN READ

For this process two 10 MHz clocks, LD_X and CLK_X, with a 180 degree phase shift are generated.

The selected column to read is acquired by the sensor on the rising edge of LD_X. The analog value of the pixel read is present at the output at the third falling edge of CLK_X. Therefore, the ADC conversion is done at the third rising edge of CLK_X, when the analog value should be stable at the ADC input.

If CLK_X is turned off, the values in the column register of the STAR 1000 leaks away after a while. This can cause multiple columns being selected at once, causing high current through the sensor and damaging it. Therefore, CLK_X is always turned on. For the same reason, the LD_X and LD_Y signals are always asserted when no images are read.

The needed time for reading all the columns are equal to the number of columns plus four times the clock cycle. From the four extra column cycles, three are due to the pipeline and one due to an extra column read cycle performed before the actual column to be readout to allow the electronics to stabilize. Hence, with the 10 MHz clock and the default value of 128 columns, the needed time is 13.2 us.

12.4.11.3. Image read frequency

Table 12-8 shows a summary of the timings involved in the reading of an image.

Actions	Time (us)
Row read	5.6
Row reset	0.5
Reading 128 columns	13.2

TABLE 12-8 IMAGE READ TIMING

Therefore, the time needed for reading a 128 by 128 image is shown in Table 12-9.

	Without reset	With reset
Readout period (ms)	2.406	2.470
Readout frequency (Hz)	416 Hz	405

TABLE 12-9 PERIOD AND FREQUENCY OF IMAGE READOUT

This value is greater than the required 300 fps. But using the row delay parameter allows to lower the read out frequency down to 64 fps.

Since the Image Link works in real time this is also the frequency of the images sent to ISS. Only a delay form around 10 us is added between the analogic pixel value present at the sensor output and the data arriving at ISS.

12.4.12. Pixel data pre-processing

The data from the sensor is read at the rising edge of the Data Ready signal from the ADC ([IR02]). From this value then the OffsetSubtraction parameter is subtracted. Then, from the twelve bits only ten will be send, selected by the Digital Gain value. This value will only be send if any of the next cases doesn't apply:

- If the OutOfRange signal (signal coming from the RHF1201, if true the analog input signal to the ADC is out of the full-scale range) is true and the MSB of the input data is one, the data sent is the maximum possible value (0x3FF).
- If the OutOfRange signal is true and the MSB of the input data is zero, the data sent is zero.
- If the OutOfRange signal is false and the OffsetSubtraction parameter (value to be subtracted to every pixel) is bigger than the input data, the data sent is zero.
- If the OutOfRange signal is false, the OffsetSubtraction parameter is not bigger than the input data but the Digital Gain parameter (parameter that allows the selection of which of the twelve bits will be send) causes the loss of non-zero bits, the data sent is the maximum possible value (0x3FF)

12.4.13. H/K ADC control

The communication is similar to SPI (Figure 12-9, [IR03]). When the master (the FPGA) sets the chip select signal at a low level, the ADC starts reading the SCLK and DIN inputs. Keeping always the chip select signal at high level except during the communication with the H/K ADC ensures a synchronization point between them, independently of previous noise in this channel.

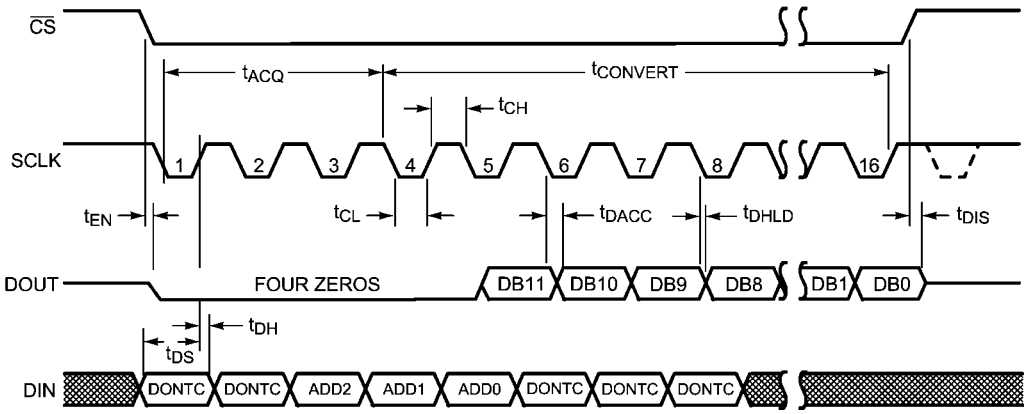

FIGURE 12-9 H/K ADC COMMUNICATION TIMING DIAGRAM

From the first to the third SCLK cycle the H/K ADC acquires the analog value to be converted during this transmission.

From the third to the fifth SCLK cycle the firmware sends, via DIN, the address to be selected by the input multiplexer of the ADC for the next conversion. This way we can choose between the eight different analog inputs.

From the fifth to the sixteenth SCLK cycle the H/K ADC sends, via DOUT, the digital value of the selected analog input at the previous transmission. The first bit sent is the most significant one.

All digital values are updated at a 10 Hz frequency, and so this process is done at 80 Hz frequency.

12.4.14. Integration time

The most relevant timings for calculating the integration time are shown at Table 12-10.

Parameter	Time (us)
Row read overhead	5.6
Row reset	0.5
Read one column	0.1

TABLE 12-10 TIMING PARAMETERS

If the rolling shutter value is zero, the integration time and frame period can be calculated with equation **9**:

$$IT\ w/o\ RS = ImageSize * \{5.6 + (Image\ Size + 4) * 0.1 + (Delay + 1) * 0.1\}\ [us] \quad (21)$$

However, if the rolling shutter value is not zero, equation 2 shows the integration time and equation 3 the frame period.

$$IT\ with\ RS = Rollign\ Shutter * \{5.6 + 0.5 + (Image\ size + 4) * 0.1 + (Delay + 1) * 0.1\}\ [us] \quad (22)$$

$$Frame\ Period = Image\ Size * \{5.6 + 0.5 + (Image\ Size + 4) * 0.1 + (Delay + 1) * 0.1\}\ [us] \quad (23)$$

12.5. Working Modes

They are four different working modes:

- Idle: in this mode Image Sensor Control and Image Link are halted. This is the only state where it's possible to change the firmware parameters. This is the start-up state.
- Single frame read: a single image is read and sent to the ISS. Once sent, the working mode is changed to idle.
- Continuous frame read: continuously images are read and send to the ISS. This mode is only left if the ISS send the idle command or the reset command.

- Test: a square 5 MHz signal with amplitude between the theoretical minimum to the maximum of the sensor is generated as input of the analog chain. The ADC output is send to ISS normally. This mode only is useful to test that the analog circuitry and the sending of data to the ISS works as expected. The only way to leave this mode is when the ISS send the idle command or the reset command.

12.6. Signals

12.6.1. Input signals

- Clk : 100 MHz clock.
- Rst_n : asynchronous registered reset signal.
- Clk_1_10 : 10 MHz clock.

12.6.1.1. From the image ADC

- ADC_Data[0:9] : data output of the ADC.
- ADC_DR : It is a copy of the ADC clock signal, but with its rising edge shifted to a point where the ADC data output is already stable. Used for the acquisition of the ADC_Data[0:9] signal.
- ADC_Out_of_Range: signal indicating that the analog input to the ADC is out of the operation range.

12.6.1.2. From the H/K ADC

- ADC_HK_DOUT: used in the SPI communication with the ADC.

12.6.1.3. From ISS Control

- CL_SCLK: 1 MHz nominal frequency clock of the Control Link.
- CL_MOSI: Control Link data.

12.6.2. Output Signals

- CLK10: generated 10 MHz clock connected to clk_1_10.
- EnSignalExt: enable of the test signal used to check the correct behaviour of the analog chain.
- SignalExt: 5 MHz clock signal used when in Test Mode to check the correct behaviour of the analog chain.

12.6.2.1. To the image ADC

- ADC_CLK: 10 MHz clock signal controlling the image ADC conversion.

12.6.2.2. To the STAR 1000

- STAR_LD_Y: control signal of the row latch.
- STAR_LD_X: control signal of the column latch.
- STAR_CLK_X: control signal of the column register. In conjunction with STAR_LD_X used to control the column selection.
- STAR_Addr[0:9]: row or column address, used in conjunction with STAR_LD_X and STAR_LD_Y.
- STAR_S: control signal of the column amplifier.
- STAR_Rst: row reset signal.
- STAR_R: control signal of the column amplifier.
- STAR_CAL: when high the output of the sensor is the reference offset voltage.

- STAR_G0: used to set the analog gain.
- STAR_G1: used to set the analog gain.
- STAR_ASEL0: signal used when in Test Mode to change the analog output of the STAR 1000 from the pixel matrix to the generated square test signal.

12.6.2.3. To ISS Control

- IL_IDAT: image link 100 Mbit/s data signal.
- IL_CCLK: image link 100 MHz clock signal. This signal is an internal routed copy of the 100 MHz oscillator clock.
- CL_SINT: Control Link SINT signal, used to control the transmission or alert ISS Control of a problem at the CTC.
- CL_MISO: Control Link data signal.

12.6.2.4. To the H/K ADC

- ADC_HK_CSn: chip select signal of the SPI communication with the H/K ADC.
- ADC_HK_SCLK: 5 MHz clock signal of the SPI communication with the H/K ADC.
- ADC_HK_DIN: data signal of the SPI communication with the H/K ADC.

12.7. Electrical Data

12.7.1. Working conditions

The working conditions for the CTC are:

- Nominal I/O voltage (V_{CCI}) of 3.30 V ± 0.17 V.
- Nominal core voltage (V_{CCA}) of 2.50 V ± 0.13 V.
- Junction temperature range from -20 ºC to 80 ºC.
- Tolerant to 25 KRad TID.

12.7.2. Absolute maximum ratings

The absolute maximum ratings are the following:

Parameter	Value
DC supply voltage range (VCCI)	-0.3 to +6.0 V dc
DC supply voltage range (VCCA)	-0.3 to +3.0 V dc
Input voltage range (VI)	-0.5 to +6.0 V dc
Output voltage range (VO)	-0.5 to (+VCCI +0.5) V dc
Storage temperature range (VSTG)	-65 ºC to +150 ºC
Lead temperature (soldering, 10 seconds)	300 ºC
Thermal resistance, junction-to-case (Θ_J)	0.5 ºC/W
Maximum junction temperature (TJ)	150 ºC

TABLE 12-11. ABSOLUTE MAXIMUM RATINGS

12.7.3. Resource usage

- Sequential cells: 886 of 2012 cells (44.04 %).
- Combinatorial cells: 1369 for 4024 cells (34.02 %).
- Logic cells: 2255 of 6036 cells (37.36 %).
- IO: 51 used of 170.
- One hardwired clock tree used for the 10 MHz clock.
- One routed clock tree for the asynchronous reset signal.
- One quadrant clock tree for the 100 MHz clock.

12.7.4. Pin Description

Name	Location	Type	I/O Technology
clk_1_10	82	Clock	LVTTL (1)
clk	178	Clock	LVTTL (1)
rst_n	7	Input	LVTTL (2)
ADC_Data[11]	49	Input	LVTTL (1)
ADC_Data[10]	47	Input	LVTTL (1)
ADC_Data[9]	45	Input	LVTTL (1)
ADC_Data[8]	43	Input	LVTTL (1)
ADC_Data[7]	39	Input	LVTTL (1)
ADC_Data[6]	37	Input	LVTTL (1)
ADC_Data[5]	35	Input	LVTTL (1)
ADC_Data[4]	33	Input	LVTTL (1)
ADC_Data[3]	31	Input	LVTTL (1)
ADC_Data[2]	29	Input	LVTTL (1)
ADC_Data[1]	25	Input	LVTTL (1)
ADC_Data[0]	23	Input	LVTTL (1)
ADC_DR	21	Input	LVTTL (1)
CL_SCLK	195	Input	LVTTL (1)
CL_MOSI	197	Input	LVTTL (1)
ADC_HK_DOUT	135	Input	LVTTL (1)
ADC_CLK	53	Output	LVTTL (3)
ADC_Out_of_Range	51	Input	LVTTL (1)
Star_CLK_X	75	Output	LVTTL (4)
CLK10	81	Output	LVTTL (5)
IL_IDAT	4	Output	LVTTL (6)
IL_CCLK	9	Output	LVTTL (6)
Star_Addr[9]	108	Output	LVTTL (7)
Star_Addr[8]	106	Output	LVTTL (7)
Star_Addr[7]	104	Output	LVTTL (7)
Star_Addr[6]	102	Output	LVTTL (7)
Star_Addr[5]	100	Output	LVTTL (7)
Star_Addr[4]	97	Output	LVTTL (7)
Star_Addr[3]	95	Output	LVTTL (7)
Star_Addr[2]	93	Output	LVTTL (7)
Star_Addr[1]	91	Output	LVTTL (7)
Star_Addr[0]	89	Output	LVTTL (7)
Star_LD_Y	87	Output	LVTTL (8)
Star_LD_X	85	Output	LVTTL (4)
Star_Rst	73	Output	LVTTL (7)
Star_S	71	Output	LVTTL (7)
Star_R	69	Output	LVTTL (7)
Star_CAL	59	Output	LVTTL (7)
Star_G0	61	Output	LVTTL (7)

Star_G1	63	Output	LVTTL (7)
CL_MISO	204	Output	LVTTL (9)
CL_SINT	206	Output	LVTTL (9)
ADC_HK_CSn	139	Output	LVTTL (9)
ADC_HK_SCLK	137	Output	LVTTL (9)
ADC_HK_DIN	133	Output	LVTTL (9)
EnSignalExt	57	Output	LVTTL (7)
SignalExt	55	Output	LVTTL (7)
Star_ASEL0	65	Output	LVTTL (7)

TABLE 12-12 PIN ASSIGMENT

12.7.5. DC Parameters

Name	Vcci (V)	Power Up State	Hot Swappable	Slew	Loading (pF)
LVTTL (1)	3.3	None	On		
LVTTL (2)	3.3	Low	On		
LVTTL (3)	3.3	None	On	High	15
LVTTL (4)	3.3	High	On	High	15
LVTTL (5)	3.3	None	On	High	20
LVTTL (6)	3.3	None	On	High	10
LVTTL (7)	3.3	None	On	Low	15
LVTTL (8)	3.3	High	On	Low	15
LVTTL (9)	3.3	None	On	Low	10

TABLE 12-13 DC PARAMETERS

12.7.6. AC Parameters

Description				Min	Max	Unit
Clock frequency	clk				114.929	MHz
Clock period	clk			8.701		ns
Clock frequency	clk_1_10				40.314	MHz
Clock period	clk_1_10			24.805		ns
Setup time	ADC_DR	before	clk (rise)	1.592		ns
Setup time	ADC_Data[0]	before	clk (rise)	2.554		ns
Setup time	ADC_Data[10]	before	clk (rise)	3.449		ns
Setup time	ADC_Data[11]	before	clk (rise)	3.891		ns
Setup time	ADC_Data[1]	before	clk (rise)	2.282		ns
Setup time	ADC_Data[2]	before	clk (rise)	2.329		ns
Setup time	ADC_Data[3]	before	clk (rise)	1.836		ns
Setup time	ADC_Data[4]		clk (rise)	1.540		ns

		before				
Setup time	ADC_Data[5]	before	clk (rise)	1.765		ns
Setup time	ADC_Data[6]	before	clk (rise)	2.436		ns
Setup time	ADC_Data[7]	before	clk (rise)	2.948		ns
Setup time	ADC_Data[8]	before	clk (rise)	3.323		ns
Setup time	ADC_Data[9]	before	clk (rise)	3.004		ns
Setup time	ADC_HK_DOUT	before	clk_1_10 (rise)	3.239		ns
Setup time	ADC_Out_of_Range	before	clk (rise)	4.088		ns
Setup time	CL_MOSI	before	clk_1_10 (rise)	2.405		ns
Setup time	CL_SCLK	before	clk_1_10 (rise)	3.141		ns
Hold time	ADC_DR	after	clk (rise)	-0.058		ns
Hold time	ADC_Data[0]	after	clk (rise)	-0.517		ns
Hold time	ADC_Data[10]	after	clk (rise)	-0.950		ns
Hold time	ADC_Data[11]	after	clk (rise)	-1.162		ns
Hold time	ADC_Data[1]	after	clk (rise)	-0.340		ns
Hold time	ADC_Data[2]	after	clk (rise)	-0.364		ns
Hold time	ADC_Data[3]	after	clk (rise)	-0.223		ns
Hold time	ADC_Data[4]	after	clk (rise)	0.012		ns
Hold time	ADC_Data[5]	after	clk (rise)	-0.141		ns
Hold time	ADC_Data[6]	after	clk (rise)	-0.470		ns
Hold time	ADC_Data[7]	after	clk (rise)	-0.751		ns
Hold time	ADC_Data[8]	after	clk (rise)	-0.845		ns
Hold time	ADC_Data[9]	after	clk (rise)	-0.693		ns
Hold time	ADC_HK_DOUT	after	clk_1_10 (rise)	-0.798		ns
Hold time	ADC_Out_of_Range	after	clk (rise)	-1.256		ns
Hold time	CL_MOSI	after	clk_1_10 (rise)	-0.402		ns
Hold time	CL_SCLK	after	clk_1_10 (rise)	-0.751		ns
Recovery time	rst_n	before	clk (rise)	1.691		ns
Removal time	rst_n	after	clk (rise)	-0.293		ns
Propagation delay	clk	to	IL_CCLK	3.328	7.525	ns
Propagation delay	clk (rise)	to	ADC_CLK	4.059	9.442	ns
Propagation delay	clk (rise)	to	CLK10	3.512	7.746	ns
Propagation delay	clk (rise)	to	IL_IDAT	3.561	7.868	ns

Propagation delay	clk (rise)	to	Star_CLK_X	3.438	7.635	ns
Propagation delay	clk (rise)	to	Star_LD_X	3.434	7.439	ns
Propagation delay	clk_1_10 (rise)	to	ADC_HK_CSn	2.758	13.162	ns
Propagation delay	clk_1_10 (rise)	to	ADC_HK_DIN	2.637	12.810	ns
Propagation delay	clk_1_10 (rise)	to	ADC_HK_SCLK	2.951	13.766	ns
Propagation delay	clk_1_10 (rise)	to	CL_MISO	3.867	15.999	ns
Propagation delay	clk_1_10 (rise)	to	CL_SINT	4.119	16.728	ns
Propagation delay	clk_1_10 (rise)	to	EnSignalExt	3.443	15.193	ns
Propagation delay	clk_1_10 (rise)	to	SignalExt	3.448	14.994	ns
Propagation delay	clk_1_10 (rise)	to	Star_ASEL0	4.053	15.887	ns
Propagation delay	clk_1_10 (rise)	to	Star_Addr[0]	3.023	13.913	ns
Propagation delay	clk_1_10 (rise)	to	Star_Addr[1]	3.061	13.994	ns
Propagation delay	clk_1_10 (rise)	to	Star_Addr[2]	3.137	14.237	ns
Propagation delay	clk_1_10 (rise)	to	Star_Addr[3]	3.296	14.589	ns
Propagation delay	clk_1_10 (rise)	to	Star_Addr[4]	3.495	14.994	ns
Propagation delay	clk_1_10 (rise)	to	Star_Addr[5]	3.448	14.994	ns
Propagation delay	clk_1_10 (rise)	to	Star_Addr[6]	3.534	15.273	ns
Propagation delay	clk_1_10 (rise)	to	Star_Addr[7]	3.768	15.768	ns
Propagation delay	clk_1_10 (rise)	to	Star_Addr[8]	3.234	14.444	ns
Propagation delay	clk_1_10 (rise)	to	Star_Addr[9]	3.093	14.048	ns
Propagation delay	clk_1_10 (rise)	to	Star_CAL	3.554	15.526	ns
Propagation delay	clk_1_10 (rise)	to	Star_G0	3.284	14.464	ns
Propagation delay	clk_1_10 (rise)	to	Star_G1	3.131	14.338	ns
Propagation delay	clk_1_10 (rise)	to	Star_LD_Y	2.947	13.751	ns
Propagation delay	clk_1_10 (rise)	to	Star_R	3.093	14.257	ns
Propagation delay	clk_1_10 (rise)	to	Star_Rst	3.566	15.553	ns

Propagation delay	clk_1_10 (rise)	to	Star_S	3.000	13.861	ns

TABLE 12-14 AC PARAMETERS

12.7.7. Power consumption

For the power consumption calculation the Actel Power Calculator has been used with the following conditions:

- 1369 combinatorial cells with an average switching of 0.1 MHz and 20% of them switching at this frequency.
- 886 register cells with an average switching of 0.1 MHz and 20% of them switching at this frequency.
- 222 register cells at the quadrant clock D with a 100 MHz clock.
- 665 register cells at the HCLK with a 10 MHz clock.
- 21 inputs with an average switching frequency of 1 MHz and an average number of inputs switching of 5.
- 34 outputs with an average switching frequency of 1 MHz and an average number of outputs switching of 8 with an average output load of 10 pF.
- Military range operating condition.

With these values, Table 12-15 shows the power consumption found.

Condition	P 2.5V (mW)	P 3.3V (mW)	P total (mW)
Best	350	22	372
Typical	421	25	446
Worst	519	56	575

TABLE 12-15 POWER CONSUMPTION

12.7.8. Package Characteristics

12.7.8.1. Mechanical characteristics

Notes:

- All exposed metalized areas and leads are gold plated 2.5 µm minimum thickness over 2.0 to 8.9 µm thickness of nickel.
- Seal ring area is connected to GND.
- Die attach pad is connected to GND.
- 18.5 gm approximated weight is measured after tie-bar removed.
- Tie-bar dimensions are for reference only.
- Case outline Y includes a large CuW heat spreader at the bottom of the package, which cannot be penetrated by X-ray.
- The CuW heat spreader is connected to GND.

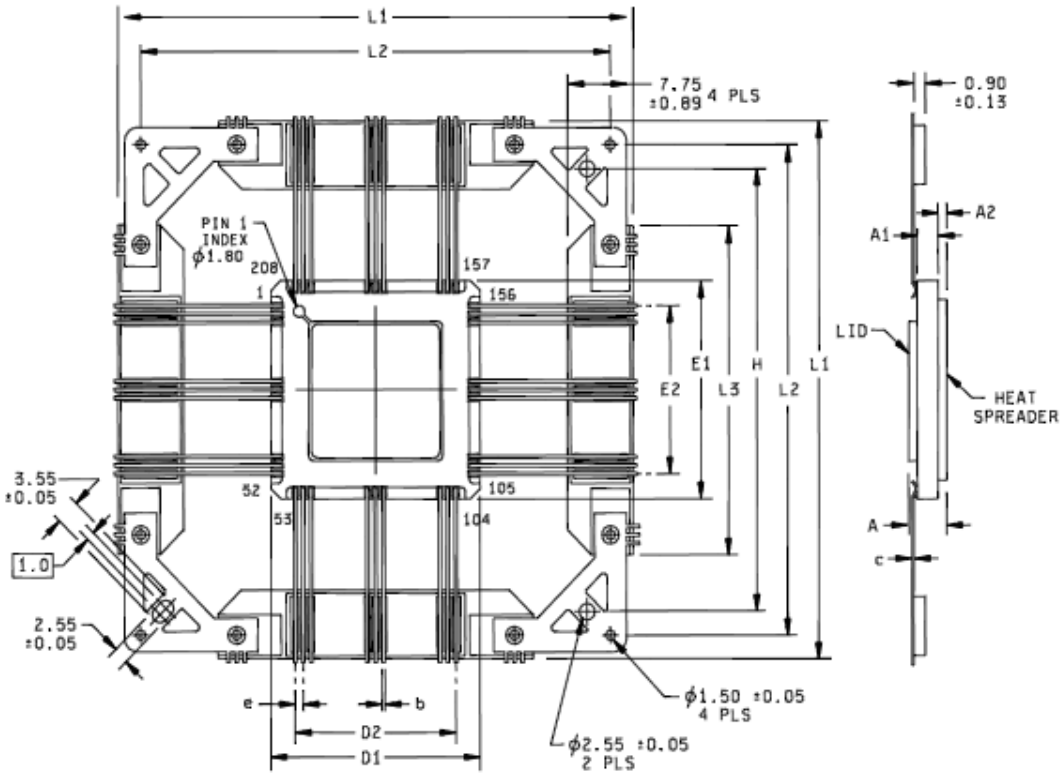

FIGURE 12-10 PACKAGE MECHANICAL DRAWING

Symbol	Minimum (mm)	Nominal (mm)	Maximum (mm)
A	2.82	3.36	3.90
A1	2.03	2.29	2.55
A2	0.37	0.50	0.63
b	0.18	0.20	0.23
c	0.10	0.15	0.20
D1/E1	28.96	29.21	29.46
D2/E2	25.50 BSC		
e	0.50 BSC		
L1	74.60	75.00	75.40
L2	70.00 BSC		
L3	56.30		
H	65.90 BSC		

TABLE 12-16 PACKAGE DIMENSIONS

12.7.8.2. Thermal characteristics

- Junction to the bottom of the package thermal resistance (Θ_{jc}): 2.0 ºC/W
- Junction to air thermal resistance of the package:
  - Still air: 20 ºC/W
  - Θ_{ja} 1.0 m/s: 16.5 ºC/W
  - Θ_{ja} 2.5 m/s: 15.0 ºC/W

13. CTC Test Report

This section shows the results of the execution of the CTC Test Plan. Since the Test Report consist of the filled out Test Plan, only the Test Report is included.

13.1. Equipment Under Test

The tests plan has been executed on the breadboard 3 (SOL-PHI-UB-HW2105-3.0) corresponding to the schematics of the annex. The firmware used corresponds to v12 (CIDL of section 10).

13.2. Test Setup

13.2.1. Test equipment

The Agilent MSO6104A 1 GHz 4GSa/s mixed signal oscilloscope will be used. The measures of the single-ended signals will be done with the 10073D 500 MHz passive probes.

Test equipment	Comments
Power supply / DC analyzer **N6705A**	To provide the different power supplies of the CPC and the LED matrix
Multimeter	To measure currents and voltages
MSO6104A	Oscilloscope to perform the measurements
CPC_EMU board	To provide the different power supplies of the CTC
DPU	To command the CTC
EGSE	PC controlling the power supplies and oscilloscope via LAN and DPU via RS-232 interface

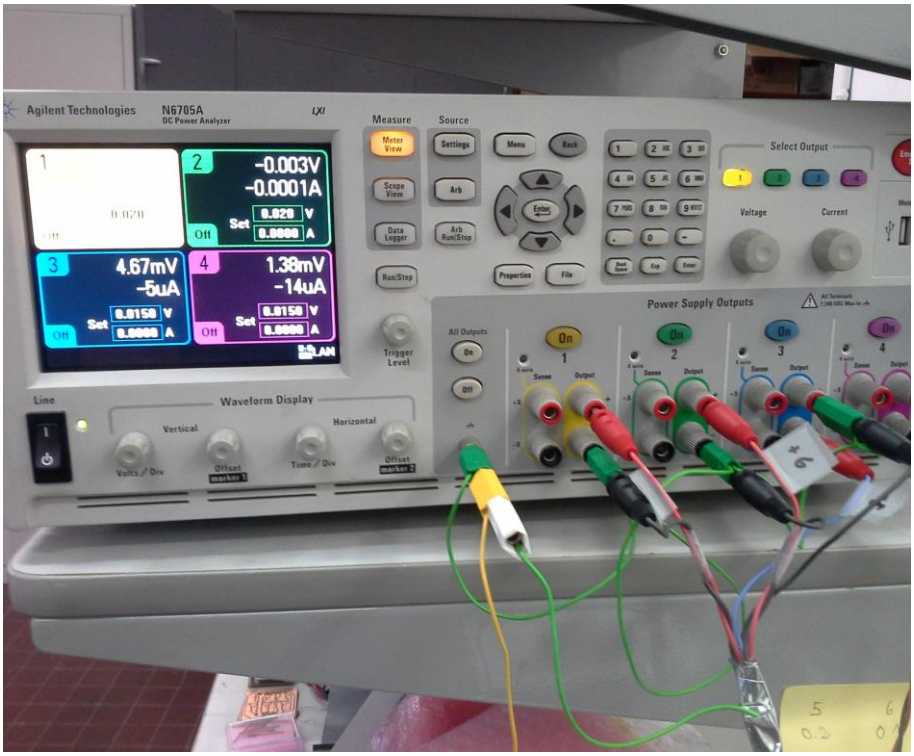

FIGURE 13-1. N6705 POWER SUPPLY

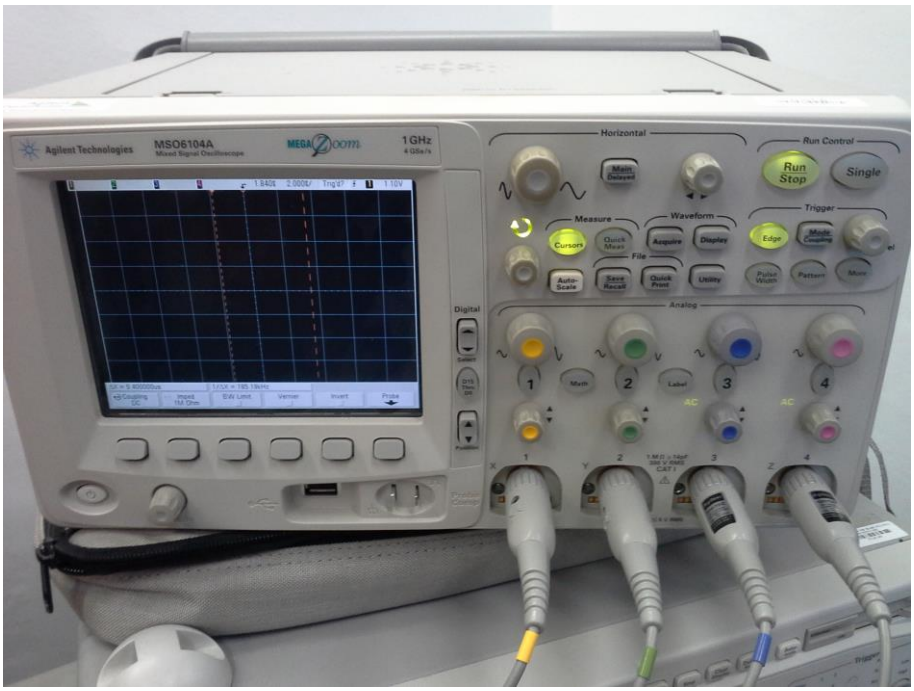

FIGURE 13-2. MSO6104A MIXED SIGNAL OSCILLOSCOPE

13.2.2. Installation and equipment connection

13.2.2.1. Power supply

The power supplies used will be the Agilent N6705A modular power analyzer. All grounds will be tied at the power supply to earth. Structural plane and thermal plane of the CTC will be also tied to ground.

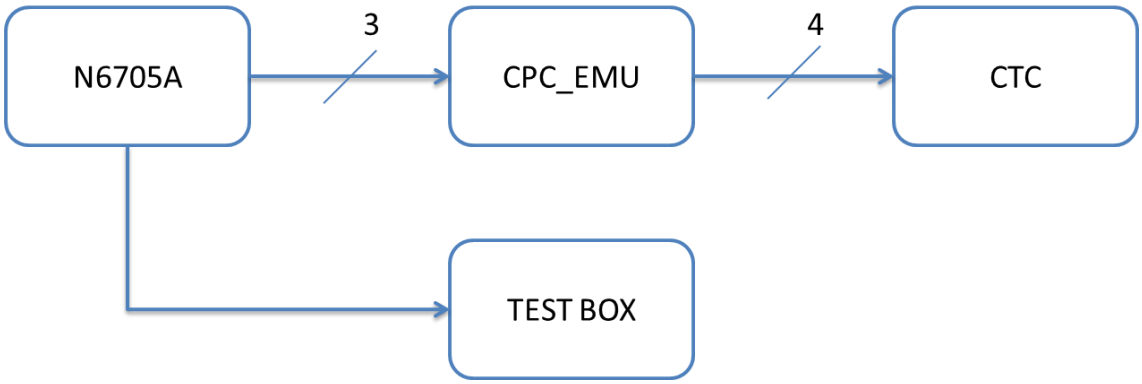

FIGURE 13-3 POWER SUPPLIES USED

The power supplies will be automatically configured from the script and should never be changed by hand. Table 13-1 shows the configuration used for the N6705A. Channels 1 to 3 are used for the CPC_EMU board and channel 4 for the LED matrix of the test box.

Channel	**1**	**2**	**3**	**4**
Voltage (V)	5	6	9	3.2
Current limit (mA)	200	100	100	100

TABLE 13-1. CURRENT LIMIT FOR THE DIFFERENT VOLTAGES

The CPC_EMU board will provide the outputs supplies according to the power supplies requirements of the CTC [7].

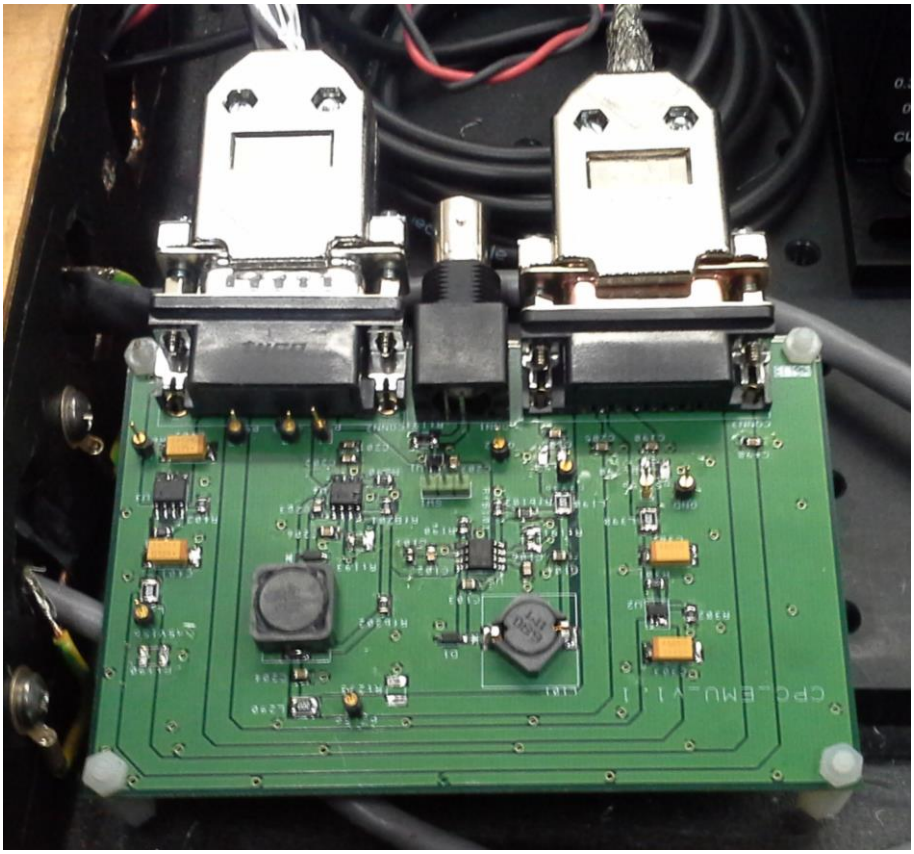

FIGURE 13-4. CPC_EMU_V1.1 BOARD

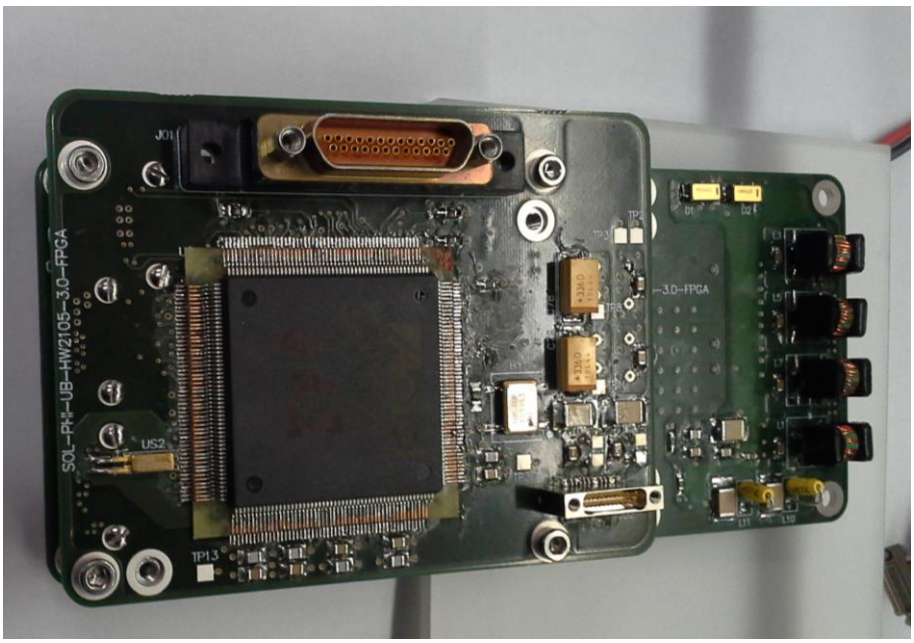

FIGURE 13-5. CTC BOARD UNDER TEST ABOVE THE LED MATRIX USED

13.2.2.2. EGSE

The data cable will be a shielded twisted pairs cable connected to the DPU CTC interface. The DPU will be connected via an USB Serial cable (TTL-232R-3V3) from FTDI to a PC and to earth. The software used for the test has been developed by the University of Barcelona and is written in python. The test requires minimal user intervention and a pop-up window with instructions for the operator will appear when an action not possible to accomplish be the scripts is required.

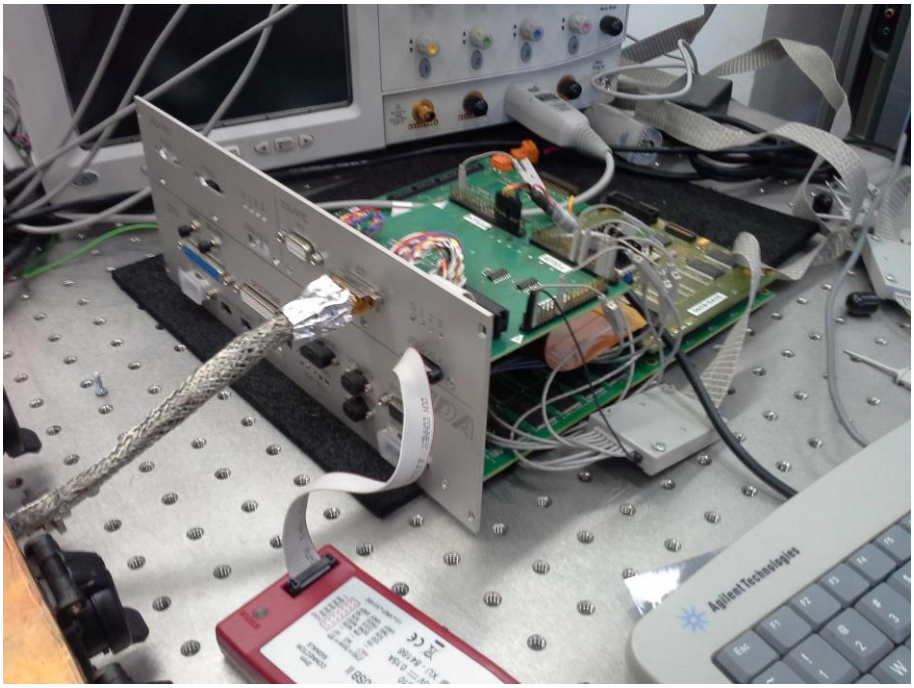

FIGURE 13-6. DPU USED AS PART OF THE EGSE WITH THE JTAG PROGRAMMER, THE RS-232 CABLE AND THE DATA CABLE TO THE CTC

13.3. Work-Sheets

13.3.1. Physical test

(Req: CTC-R-230, CTC-R-231, CTC-R-232 and CTC-R-233)

Step	Verification step	Expected result	Obtained result	Remarks
1.	Weight the two boards with the mounted electronics.	Less than 165 g.	101 g. PASS	
2.	Measure the CTC Detector Board.	125 by 55 mm	125 by 55 mm. PASS	
3.	Measure the CTC FPGA Board	80 by 60 mm	80 by 60 mm. PASS	
4.	Mounted the two boards together.			
5.	Measure the height of the two boards.	Less than 32.25 mm	32 mm. PASS	

TABLE 13-2. PHYSICAL TEST

13.3.2. Power supplies test

(Req: CTC-R-200, CTC-R-201, CTC-R-202, CTC-R203)

The power supplies shall be tested at the output of the power modules without the CTC connected and with the CPC_TEST_BOARD connected instead. The scope of this test is to check the correct power supply is provided to the electronics. The CTC_Power_Supplies script does this test.

Step	Verification step	Expected result	Obtained result	Remarks
1.	Execute the CTC_Power_Supplies script.			
2.	Connect the channel 1 of the oscilloscope to the -5 V test point.			
3.	Connect the channel 2 of the oscilloscope to the +2.5 V test point.			
4.	Connect the channel 3 of the oscilloscope to the +3.3 V test point.			
5.	Connect the channel 4 of the oscilloscope to the +5 V test point.			
6.	The script adjusts the time resolution to 10 ms of span.			
7.	The script adjusts the vertical			

	scale span to 6 V for channel 1.			
8.	The script adjusts the voltage offset of channel 1 to -5.15 V.			
9.	The script adjusts the vertical scale span to 3 V for channel 1.			
10.	The script adjusts the voltage offset of channel 2 to 2.5 V.			
11.	The script adjusts the vertical scale span to 4 V for channel 3.			
12.	The script adjusts the voltage offset of channel 3 to 3.3 V.			
13.	The script adjusts the vertical scale span to 6 V for channel 4.			
14.	The script adjusts the voltage offset of channel 4 to 5.15 V.			
15.	The script sets the trigger to 2.5 V of channel 4 and mode triggered.			
16.	The script turns on the power supplies.			
17.	The script measures the rise time of channel 1.	Less than 5 ms.	0.26 ms. PASS	

18.	The script measures the rise time of channel 2.	Less than 5 ms.	1 ms. PASS	
19.	The script measures the rise time of channel 3.	Less than 5 ms.	1.15 ms. PASS	
20.	The script measures the rise time of channel 4.	Less than 5 ms.	0.07 ms PASS	Figure 13-7 shows the start-up
21.	The script adjusts the time resolution to 10 ms of span and the vertical scale to 50 mV/square for all channels.			
22.	The script activates the averaging for 1024 counts.			
23.	The script sets the trigger to automatic.			
24.	The script measures the average value of channel 1.	-5.15V +/- 0.25V	-5.259 V. PASS	
25.	The script measures the average value of channel 2.	2.5V +/- 0.125V	2.512 V. PASS	
26.	The script measures the average value of channel 3.	3.3V +/- 0.165V	3.366 V. PASS	
27.	The script measures the average	5.15V +/- 0.25V	5.154 V. PASS	

	value of channel 4.			
28.	The script adjusts the time span to 1µs and the vertical scale to 20 mV/square for all channels. Set the inputs to AC coupling and the voltage offset to 0.			
29.	The script deactivates the averaging.			
30.	The script measures the AC Peak-to-Peak value for channel 1.	More than 20 mV	22.5 mV. PASS	
31.	The script measures the AC Peak-to-Peak value for channel 2.	More than 20 mV	23.7 mV. PASS	
32.	The script measures the AC Peak-to-Peak value for channel 3.	More than 20 mV	23.7 mV. PASS	
33.	The script measures the AC Peak-to-Peak value for channel 4.	More than 20 mV	22.5 mV. PASS	Figure 13-8 shows the AC noise from the CPC_EMU

TABLE 13-3. 2.5 V POWER SUPPLY

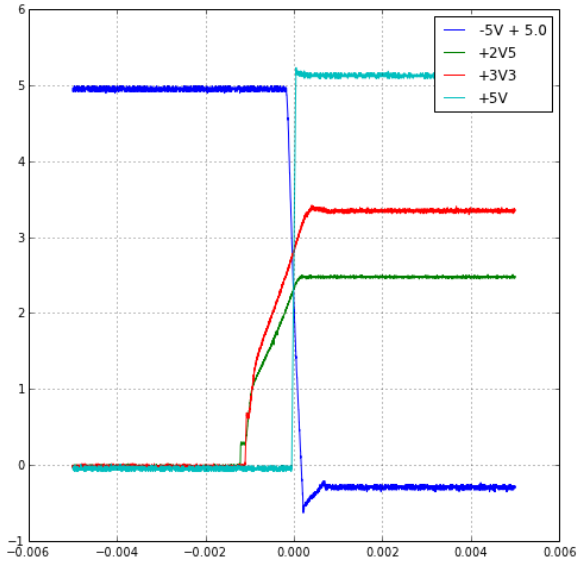

FIGURE 13-7. CPC_EMU POWER UP TRANSIENT

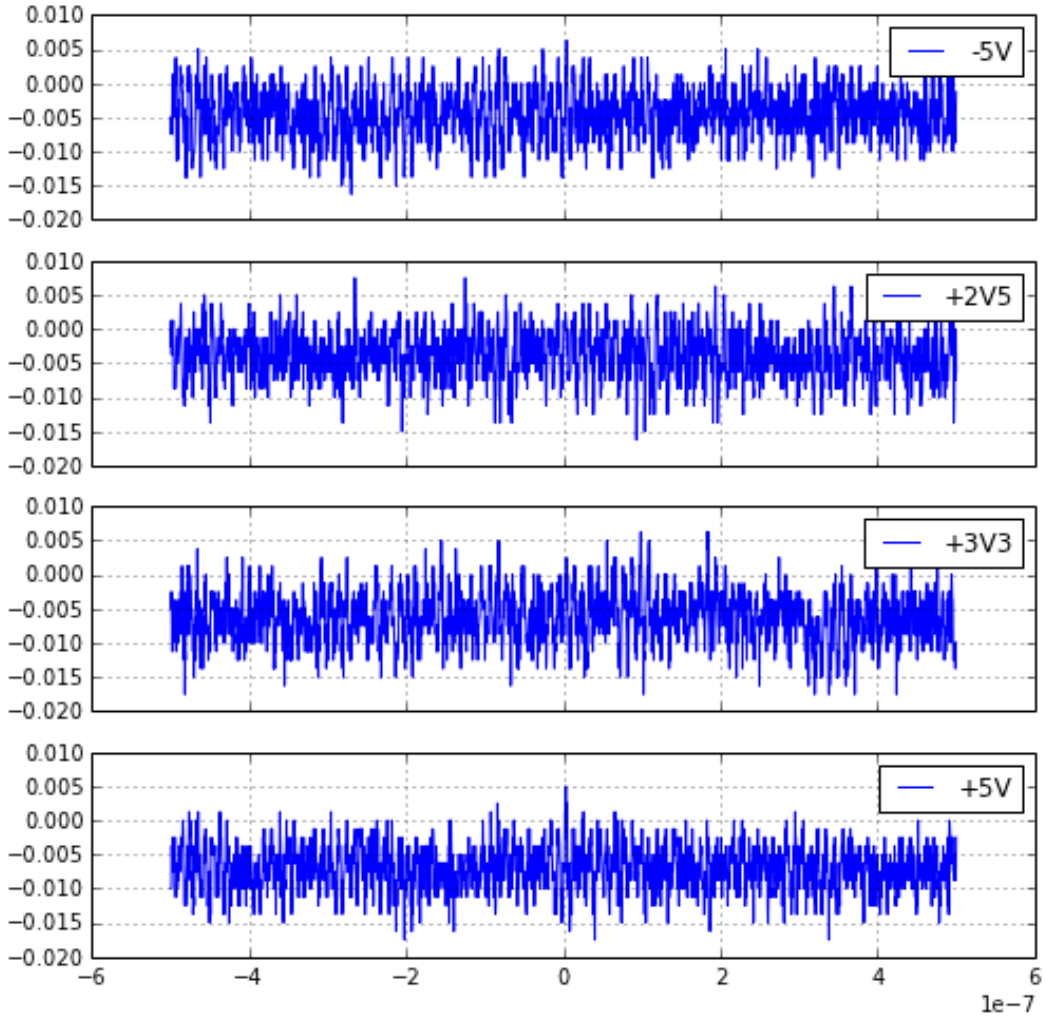

FIGURE 13-8. AC NOISE FROM THE CTC_EMU

13.3.3. Communication test

(Req: CTC-R-250)

This test will verify that the communication between the DPU and the CTC FPGA is working as expected. The CTC_Communication_Test script does this test.

Step	Verification step	Expected result	Obtained result	Remarks
1.	Execute the CTC_Communication_Test script.			
2.	Start the CTC power supplies.			
3.	The script sends a software reset	Status frame reply	Status frame. PASS	
4.	The script reads the Image Size	128	128. PASS	All these values are the firmware reset values.
5.	The script reads the row delay	0	0. PASS	
6.	The script reads the Analog & Digital Gain	Both 0	(0,0) PASS	
7.	The script reads the Offset subtraction	0	0. PASS	
8.	The script reads the rolling shutter offset	0	0. PASS	
9.	The script reads the Image Offset X	448	448. PASS	

10.	The script reads the Image Offset Y	448	448. PASS	
11.	The script reads the Frame Counter	0	0. PASS	
12.	The script reads the Column Out of Range	0	0. PASS	
13.	The script reads the Row Out of Range	0	0. PASS	
14.	The script reads the CAL value	0	0. PASS	
15.	The script sends the Get current mode	Idle Mode	Idle Mode. PASS	
16.	The script reads sends NOP	NOP frame	NOP frame. PASS	

TABLE 13-4. REGISTER READ TEST

13.3.4. H/K Test

(Req: CTC-R-250)

This test will ensure that the H/K ADC is working as expected and that all H/K signals are in the expected range. The CTC_HK_Test script does this test.

Step	Action	Expected result	Obtained result	Remarks
1.	Execute the CTC_HK_Test script.			
2.	Start the CTC power supplies.			
3.	Send a software reset.		STATUS frame	
4.	Read H/K Data 0		839	
5.	Read H/K Data 1		301	
6.	Read H/K Data 2		575	
7.	Read H/K Data 3		577	
8.	Read H/K Data 4		466	
9.	Read H/K Data 5		309	
10.	Read H/K Data 6		245	
11.	Read H/K Data 7		503	
12.	Using the H/K Data 6 calibrate the			

	ADC values and calculate the power supplies and temperatures			
13.	Measure with the multimeter the DC value of the -3.6 V supply.		-3.747 V	
14.	Write the previous value read from the multimeter. The value found from the H/K data shall be in a +/- 5 % margin.		-3.883 V. PASS	
15.	Measure with the multimeter the DC value of the 2.5 Va supply.		2.508 V	
16.	Write the previous value read from the multimeter. The value found from the H/K data shall be in a +/- 5 % margin.		2.493 V. PASS	
17.	Measure with the multimeter the DC value of the +3.3 Vd supply.		3.339 V	
18.	Write the previous value read from the multimeter. The value found from the H/K data shall be in a +/- 5 % margin.		3.314 V. PASS	
19.	Measure with the multimeter the DC value of the +5 Vd supply.		5.116 V	
20.	Write the previous value read from		5.099 V. PASS	

	the multimeter. The value found from the H/K data shall be in a +/- 5 % margin.			
21.	Measure the temperature of the STAR 1000 sensor.		25.9 ºC	
22.	Write the previous value read from the thermometer. The value found from the H/K data shall be in a +/- 5 % margin.		301.16 K. PASS	
23.	Measure the temperature of the FPGA sensor.		26.3 ºC	
24.	Write the previous value read from the thermometer. The value found from the H/K data shall be in a +/- 5 % margin.		299.82 K. PASS	

TABLE 13-5. H/K TEST

13.3.5. Image tests

(Req: CTC-R-264 and CTC-R-265)

This test will ensure that the dynamic range of the sensor is enough. The CTC_Image_Tests script does this test.

Step	Action	Expected result	Obtained result	Remarks
1.	Cover the sensor.			
2.	Execute the CTC_Image_Tests script.			
3.	Start the CTC power supplies.			
4.	The script sends a software reset.		STATUS frame.	
5.	The script sends to ISS the ISS_STAT_MEAN_STD command with parameters (5, 300, True, False)	Image with a pattern similar to a chess board with high values over 900 and low values below 300. The standard deviation of the pixels should be below 1.	Figure 13-9 shows the output. The maximum standard deviation of the image is 0.65625. PASS.	With this command, ISS calculates the mean value and standard deviation of 32 test images and returns to matrix with these data. The first 300 images are discarded.
6.	The script sets the rolling offset parameter to 1.	Read back the value to confirm that it is 1.	1. PASS	
7.	The script sends to ISS the ISS_STAT_MEAN_STD command with parameters (5, 300, False, False). This is done 64 times to read the entire sensor area from		Figure 13-10 shows the dark image.	With this command ISS read 32 images in continuous mode and return two matrixes: mean and standard deviation of each pixel. The first 300 images are

	row/column 2 to 1021. The first pixel column and row and the last two pixel columns and rows of the sensor area omitted.			discarded.
8.	Check for defective pixels. Any pixel having a mean value above 100 DN shall be excluded from further calculations.		(611, 44), (611,45)	
9.	The script turns on the LED matrix.	Power consumption higher than 50 mA is needed to reach saturation.	100 mA. PASS.	
10.	The script sets the rolling offset parameter to 0.	Read back the value to confirm that it is 0.	0. PASS	
11.	The script sends to ISS the ISS_STAT_MEAN_STD command with parameters (32, 300, False, False). This is done 64 times to read the entire sensor area from row/column 2 to 1021. The first pixel column and row and the last two pixel columns and rows of the sensor area omitted.		Figure 13-10 shows the saturation images.	This image will have enough illumination to have all pixels saturated.
12.	Check for defective pixels. Any pixel having a mean value below 500 DN shall be excluded from further calculations.		(611, 44)	

13.	The script calculates for each element of the matrix subtracts the mean value of the dark images from the mean value of the saturated image. This new matrix will be the dynamic range of each pixel.	The mean value of the matrix shall be above 512.	546 DN. PASS	
14.	The script divides the dynamic range matrix by the standard deviation matrix of the dark images.	The mean value of this matrix shall be greater than 8 bits.	10.2 bits. PASS	The ENOB shall be at least 8 bits.

TABLE 13-6. DYNAMIC RANGE TEST

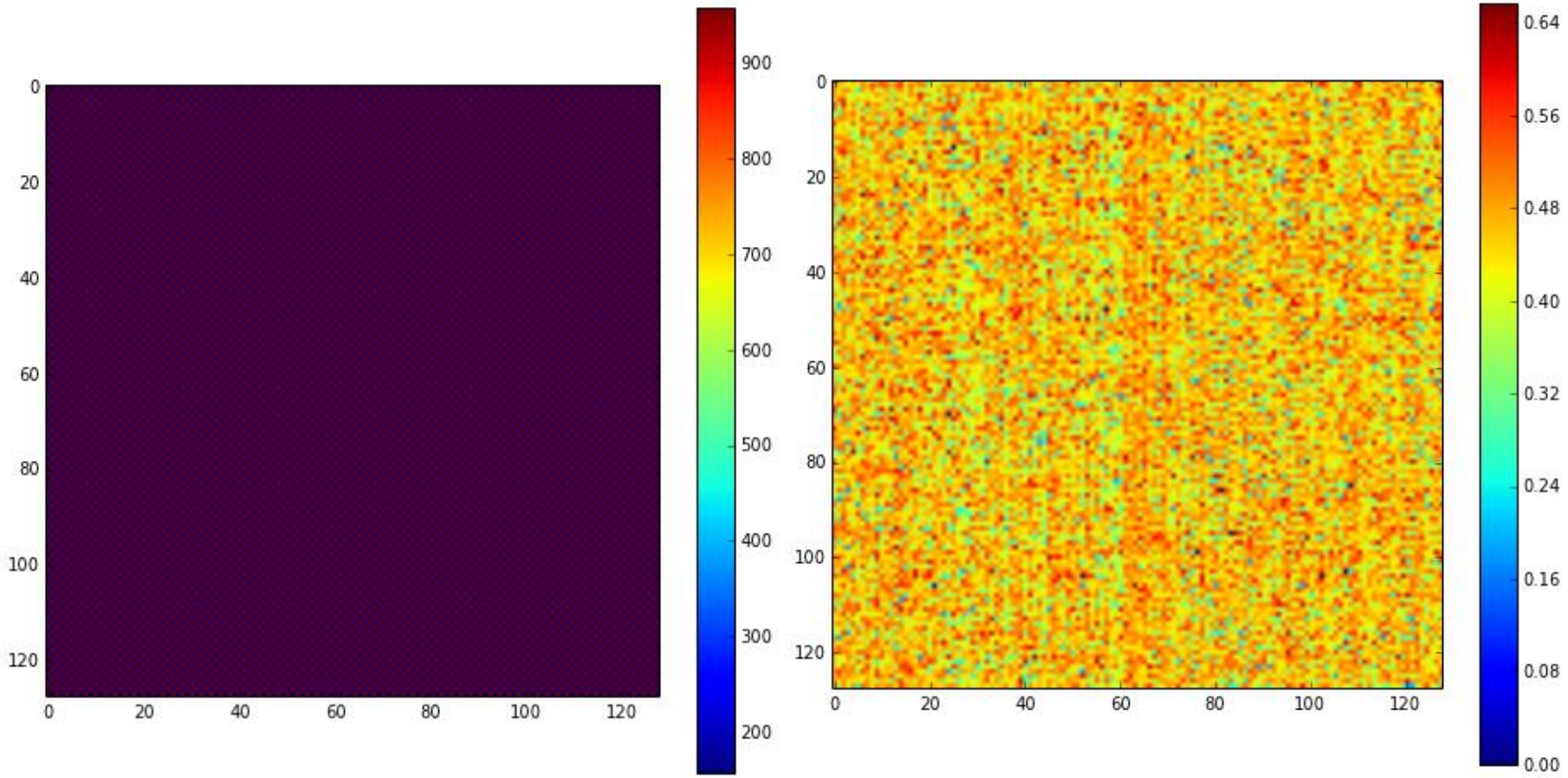

FIGURE 13-9. MEAN VALUE OF THE TEST IMAGE (LEFT) AND STANDARD DEVIATION OF THE TEST IMAGES (RIGHT)

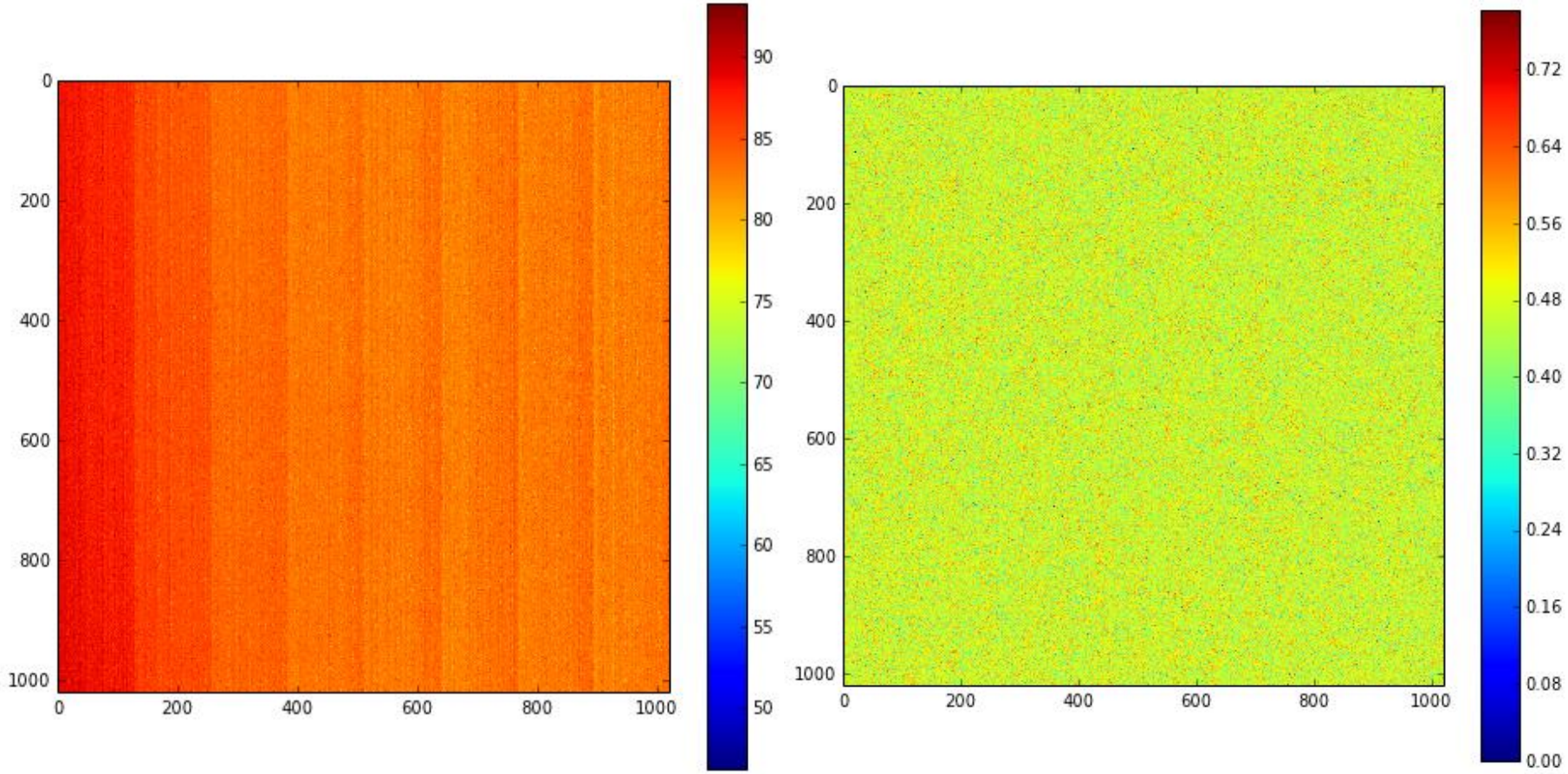

FIGURE 13-10. DARK MEAN VALUE (LEFT) AND STANDARD DEVIATION (RIGHT)

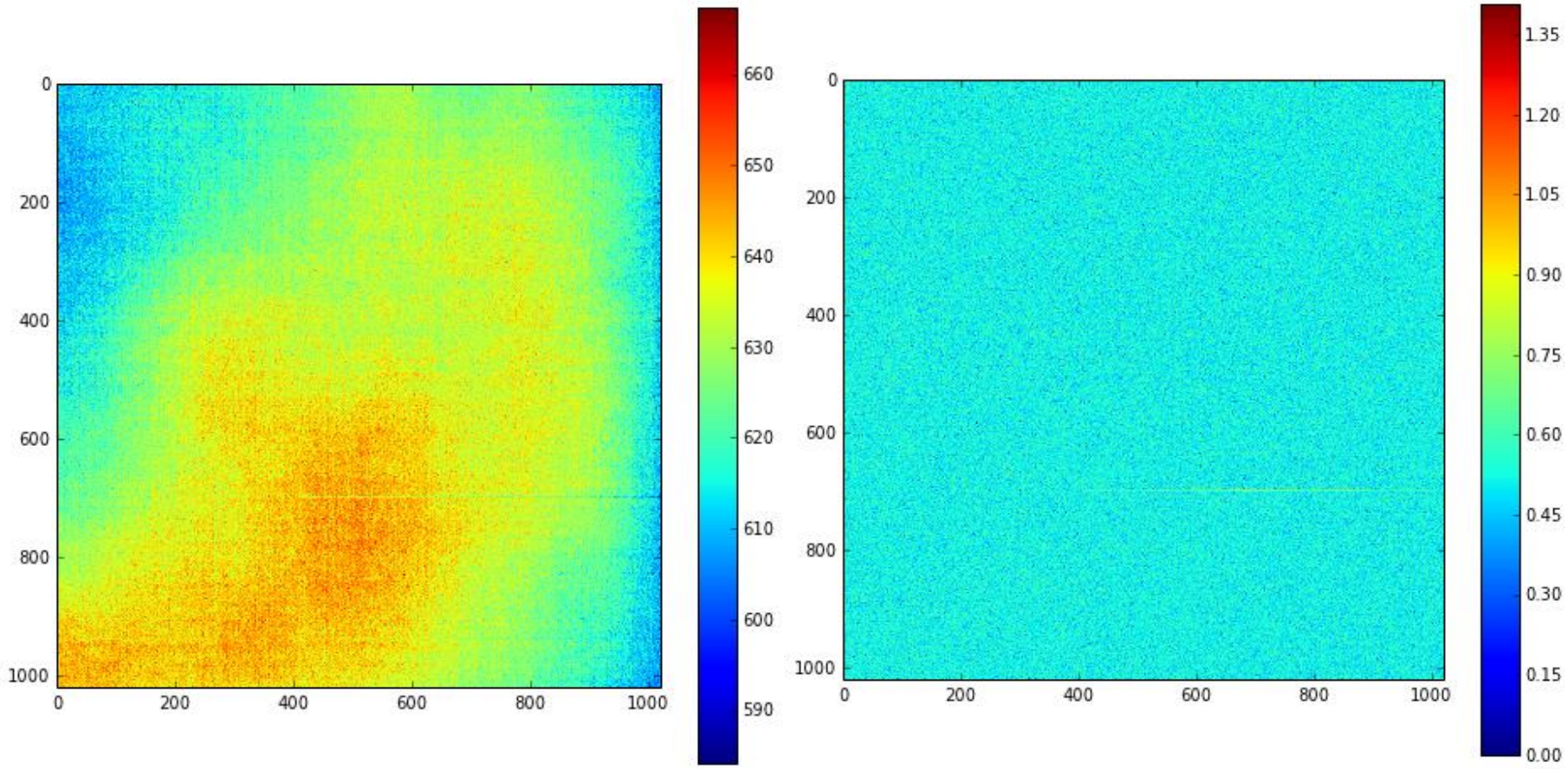

FIGURE 13-11. SATURATED IMAGES MEAN VALUE (LEFT) AND STANDARD DEVIATION (RIGHT)

13.4. Results

The following table shows the results of the different tests.

Test	Number of fails	Steps failed
13.3.1 Physical test	0	-
13.3.2 Power supplies test	0	-
13.3.3 Communication test	0	-
13.3.4 H/K Test	0	-
13.3.5 Image tests	0	-

FIGURE 13-12. TEST RESULTS

All tests passed without any failure. The defective pixel tests has shown also that a defective pixel affects the following one since the output driving capabilities of the sensor are not high enough to change the voltage if there is a big change from one pixel to the following one.

14. Conclusions

The results demonstrate that the developed CTC meets the requirements. The development had some special challenges, common in space applications, but not existing in other sectors:

- Space components: the components used in space applications needs a very high reliability hence they are much older than the typical commercial parts and with a much higher cost. Therefore, during the development phase, a trade-off between using commercial parts with similar performance and engineering space parts for the components without equivalent parts must be reach. Also, some common commercial components don't exist at all and common solutions used in other sectors are not available for space applications.
- Quality control: since the high costs involved in space missions, a lot of time and effort must be invested in quality control and documentation to ensure overall reliability. Therefore, some minor changes at some phases of the development mean a lot more time writing documents than actually implementing and testing the change.
- ECSS Standards: these standards are applicable to all ESA missions. For people not familiar with them, a lot of time needs to be invested to understand the structure of them and to find which are the relevant documents for the different tasks to be performed during the project. Also, finding examples of the documentation of other previous space missions is not straightforward.
- Flexibility: since performing changes to the developed application is not an option in a space mission (special for the CTC where the FPGA is not reprogrammable), the developed solution must be enough reconfigurable to adapt to future contingencies not expected during the mission design, always keeping power consumption and mass in the limits of the assigned budget.

All these special challenges must be taking into account for space applications and only experience in this sector and a good planning allows finding simple solutions and avoiding problems during the development.

Bibliography

[1] ESA, "Solar Orbiter. Exploring the Sun-heliosphere connection," July 2011.

[2] D. Müller, R. Marsden, O. St. Cyr y H. Gilbert, «Solar Orbiter Exploring the Sun-Heliosphere Connection,» *Solar Phys,* nº 285, pp. 25-70, 2013.

[3] Instituto de Astrofísica de Andalucía, "Harness Specification Document," 2013-07-17.

[4] Instituto de Astrofísica de Andalucía, "PHI Internal Electrical Interface Control Document," 2013-11-25.

[5] Kiepenheuer-Institut für Sonnenphysik, «ISS Specification,» 2013-06-17.

[6] ECSS, "Technical Requirements Specification," in *ECSS-E-ST-10-06C*, 2009-03-06.

[7] Max-Planck-Institut Für Sonnensystemforchung, «Camera Power Converter Interface Control Document EFM,» 2013-02-15.

[8] Kiepenheuer-Institut für Sonnenphysik, «MICD CTC Electronics,» 2013-11-25.

[9] Instituto Universitario de Microgravedad "Ignacio Da Riva", «PHI Optics unit reduced thermal model,» 2012-0-14.

[10] Instituto Nacional de Técnica Aeroespacial, «Radiation Analysis Report,» 2013-06-14.

[11] ECSS, «Space product assurance: ASIC and FPGA development,» de *ECSS-Q-ST-60-02C*, 2008-07-31.

[12] Max-Planck-Institut Für Sonnensystemforchung, «Configuration management plan,» 2012-09-27.

[13] Microsemi Corp., «RTSX-SU Radiation-Tolerant FPGAs,» March 2012.

[14] On Semi, «STAR1000 1M Pixel Radiation Hard CMOS Image Sensor,» October 2012.

[15] Standard Microcircuit Drawing, «Microcircuit, digital-linear, 12 bit 50 Msps analog to digital converter, monolithic silicon,» 2006-03-22.

[16] Max-Planck-Institut Für Sonnensystemforchung, «TN: Measurement of noise ripple spectrum un CPC EFM output VCCI (+5.15V),» 2013-05-17.

[17] Instituto de Astrofísica de Andalucía, «PBBI for PHI OTP FPGAs,» 2013-12-19.

[18] D. Fritsch y R. Spiller, «CCD versus CMOS - has CCD imaging come to an end?,» *Photogrammetric Week 01,* pp. 131-137, 2001.

[19] ESA, "Active Pixel Sensor," 2 Oct 2004. [Online]. Available: http://sci.esa.int/science-e/www/object/index.cfm?fobjectid=36027. [Accessed 2 Apr 2012].

Glossary

ABCL	As built configuration List
ADC	Analog to Digital Converter
APS	Active Pixel Sensor
BB	Breadboard
CCD	Charge Coupled Device
CDR	Critical Design Review
CI	Configuration items
CIDL	Configuration item data list
CMOS	Complementary Metal-oxide Semiconductor
CPC	Camera Power Converter
CQFP	Ceramic quad flat pack
CT	Correlator Tracker
CTC	Correlation Tracking Camera
DCR	DC Resistance
DN	Digital Number
DPU	Digital processing unit
ECSS	European Cooperation for Space Standardization
EFM	Electrical Functional Model
EID	Experiment Interface Document
EM	Engineering Model
ENB	Equivalent Noise Bandwidth
ENOB	Effective Number of Bits
EPD	Energetic Particle Detector
FPA	Focal Plane Assembly
EUI	Extreme Ultraviolet Imager
FAR	Flight Acceptance Review
FDT	Full Disk Telescope
FG	Fabry-Pérot Filtergraph system
FPGA	Field programmable gate array
FM	Flight Model
FS	Flight Spare Model
GAM	Gravity Assist Maneuvers
GBW	Gain Bandwith

HK	Housekeeping
HRT	High Resolution Telescope
HW	Hardware
I/O	Input output
IP	Intellectual property
IPDR	Instrument Preliminary Design Review
ISS	Image Stabilization System
LOS	Line-of-sight
LSB	Least Significant Bit
LVDS	Low Voltage Differential Signal
MAG	Magnetometer
METIS	Multi Element Telescope for Imaging and Spectroscopy
MSB	Most Significant Bit
N/A	Not applicable
NCR	Non conformity report
OPM	Off-pointing Mechanism
OTP	One Time Programmable
PDR	Preliminary Design Review
PHI	Polarimetric and Helioseismic Imager
PMP	Polarization Modulation Package
PSRR	Power Supply Rejection Ratio
RF	Radio Frequency
RFW	Request for waiver
RMS	Root Mean Square
RPW	Radio and Plasma Waves
RT	Requirement Type
RTL	Register transfer level
S/C	Spacecraft
SEL	Single Event Latch-up
SEU	Single Event Upset
SINAD	Signal to Noise and Harmonic Distortion Ratio
SO	Solar Orbiter
SO/PHI	Polarimetric and Helioseismic Imager for Solar Orbiter
SoloHI	Solar Orbiter Heliospheric Imager

SPI	Serial Protocol Interface
SPICE	Spectral Imaging of the Coronal Environment
SMD	Standard Microcircuit Drawing
SNR	Signal to Noise Ratio
SRF	Self Resonant Frequency
STM	Structural Thermal Model
SW	Software
SWA	Solar Wind Analyser
TBC	To be confirmed
TBD	To be defined
THD	Total Harmonic Distortion
TMR	Triple Modular Redundancy
TTC	Tip Tilt Controller
TTM	Tip Tilt Mirror
VHDL	VHSIC hardware description language