Analyzing stability Concerns in the presence of variations in Subthreshold SRAM

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ABSTRACT

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The Scaling of the CMOS technology has enabled the improvement in the speed and device density in the integrated circuits. The downside of this scaling is the increase in the subthreshold leakage of the transistor due to the constant reduction in the channel length, Subthreshold leakage is the primary contributor to the leakage energy of the integrated circuits. However this leakage current can be used to operate circuits that are highly energy constrained. Recent studies have shown that the voltage for minimum energy per operation lies below the threshold of the MOS transistor. This has raised considerable interest in the recent years towards the application of subthershold operation to achieve energy efficiency in processors and memory circuits.

The improvement in the energy efficiency in subthreshold processors, come at a cost of considerable increase in delay. The drive current in subthreshold decreases exponentially with the scaling of supply voltage. The low performance of the processor at such low voltages becomes a bottleneck for their use in performance driven application domains. Also the mismatch between the performance of the processor and memory aggravates at subthreshold voltages. The voltage for minimum energy per operation for memory is higher than that of the processor. There is also the issue of increased sensitivity of the circuit to variations. Random Dopant Fluctuations(RDF) are claimed to be the primary source of process variations in subthreshold. In memory structures, the conventional 6T SRAM is not able to provide decent stability for it to considered for subthreshold operation. There are proposals of 8T/10T subthreshold bit cells that offer higher stability than 6T, but they are limited by their slow access time.
Our aim is to design a bit cell that achieves greater stability than the 6T bit cell and also has smaller delay. We analyze the current subthreshold bit cells and show that the buffer-based bit cells lower the variations in the storage node voltage more than the other bit cells. We also show that the schmitt trigger based bit cell is able to achieve better tolerance to variations at the cost of lower noise margin than 6T. We find that the bit cells that break the feedback between the inverters during read or write, have high variations in their noise margins.
We propose a new bit cell that is able to discharge the bit lines in 41% less time than the 6T as it's discharge path is only of single transistor. The bit cell isolates the storage nodes from the read bit lines and thus achieve noise margins similar to the buffer based bit cells. However, because of single transistor discharge path, the bit cell suffers from low I_{on}/I_{off} ratio and we show that in 1Kbyte SRAM array, the delay in developing voltage drop among the bitlines is larger for our bit cell as compared to the 6T.

Keywords: Subthreshold, Weak Inversion, SRAM Bit-cell, Static Noise Margin, N-curve, Process Variations

Contents

Chapter 1

Introduction

1.1 Need for Energy Efficient Architecture

The prevalence of "anywhere-anytime" computing, made possible by the presence of battery operated mobile computing devices, has raised interest in energy efficient computing. The conventional way to reduce the energy consumption is to scale down the voltage supply, as energy decreases quadratically with respect to voltage. However, this also increases the delay and reduces the frequency.
The supply voltage has not scaled very well in recent years due to its secondary effect of decrease in frequency. The Dennard's MOSFET scaling rule, which is based on keeping the same electric field as we scale down to lower technologies, gives the same power density and lower delay as we move to lower technology nodes. However this scaling rule has not been followed by the industry and the supply voltage has started to stagnate. The voltage scaling trend predicted by ITRS is shown in figure 1.1.

More and more transistors are being put into the same die size to increase computation density. This is resulting in higher power density as we are moving to new technology nodes with smaller feature sizes. The problem of the presence of dark silicon has emerged that puts stern limits on the number of transistors in the silicon that can be turned on at a particular time, to meet the energy budget.

1.2 Why Aggressive Voltage Scaling?

The motivation for aggressive voltage scaling stems from the studies that show that maximum energy efficiency is achieved at voltage levels below threshold. Figure 1.2 shows how the total energy for a chain of 50 inverters reach a global minimum at voltage below the threshold voltage. The dynamic component of the energy decreases quadratically with supply voltage scaling and this decrease in dynamic energy contributes to most of the energy savings in the above threshold operation. Figure 1.2 also shows the exponential increase in delay as we scale down the supply voltage. Thus the transistors leak for longer period, consequently increasing the leakage energy of

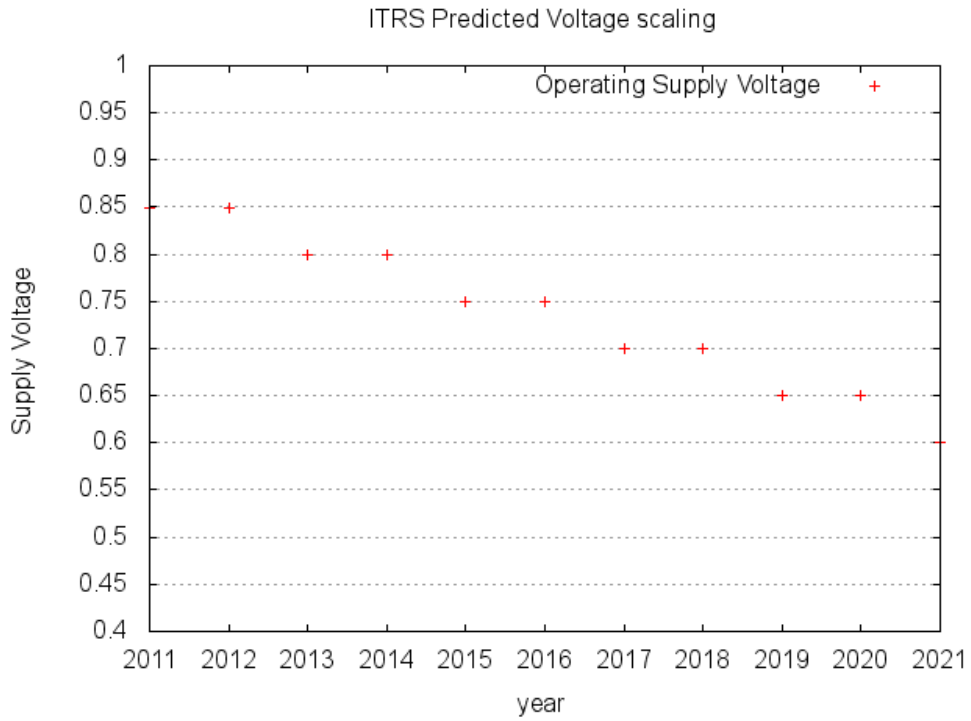

Figure 1.1 ITRS Predicted Voltage Scaling Trend for 2011 onwards

the system. The total energy of the system, given by Equation 1.1, is minimum at a voltage below the threshold voltage of the transistor.

$$E = E_{dyn} + E_{leak} = \frac{1}{2}.C.{V_{dd}}^2.\alpha + I_{leak}.V_{dd}.t_p \tag{1.1}$$

1.3 History

Circuits operating in Subthreshold region have been existing for a very long time, initially finding application in low performance analog devices like digital watches. The model for weak-inversion mode of transistor was proposed as early as in 1972 [15] which was further extended in 2000 [16]. The main contribution of the above work is the calculation of fundamental lower limit on supply voltage of CMOS circuits

$$vdd_{min} = \frac{2kT}{q} \ln(1+n) \tag{1.2}$$

where n is the slope factor. For ideal MOS tranistor, slope factor is $60mV/dec$, at $300K$. The minimum operating voltage Vdd_{min} for 180nm process MOSFET is shown to be 0.036V, at $300K$. This

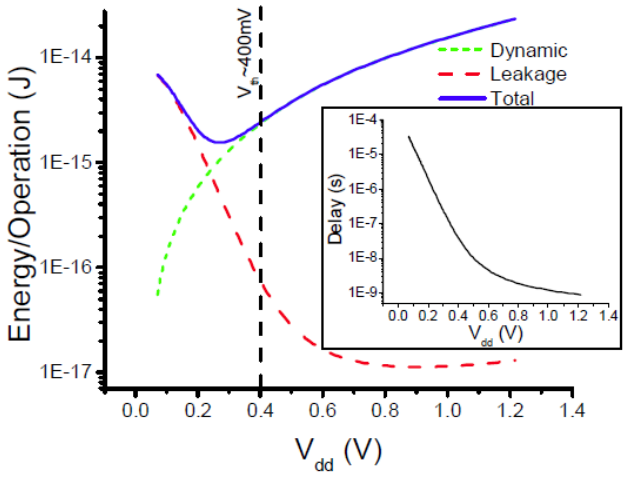

Figure 1.2 Delay and Energy consumption for a chain of 50 inverters with activity factor of 0.2 at echnology node 130nm. Source[12]

is significantly smaller voltage than what is being used today. The ITRS 2011 update shows that we can only go as low as $0.6V$ for the next 14 years if we keep on operating in super-threshold region of MOSFET. However since the leakage energy becomes the dominant source of energy consumption at such low voltages, the minimum energy consumption of the circuit happens at a slightly higher voltage. The minimum energy operation was shown to happen in subthreshold region in [14][18][19]. However the results also show an exponential increase in delay and increased sensitivity to process variations and, thus, subsequent reduction in performance. Stanford has developed an new CMOS technology, Stanford ULP CMOS, that allows adjusting the threshold voltage for different levels of circuit activity and also compensates for process variations. In recent years there have been some proposals of subthreshold processors that have shown high energy efficiency at the cost of reduced clock frequency.

1.4 Issues in Subthreshold Computing

The subthreshold operation is limited by its longer delay and smaller frequencies. So far, only wireless sensor networks and biomedical implants have been suggested to be potential application domains. It has been suggested to use a combination of above threshold and subthreshold voltages for burst-mode applications, but circuit optimizations done for subthreshold operation are not suitable for above threshold operation. For example, increasing the logic in each pipeline stage so as to decrease the impact of variations in subthreshold operation, limits the frequency in above threshold as larger depth increases the delay of the pipeline stage. Due to the exponential dependence of the subthreshold current on threshold voltage, the variance in the behavior of circuits at subthreshold voltages is much larger than at above threshold voltages and hence more chances of

circuit malfunctioning.

1.5 SRAM Bit-Cells in Subthreshold

SRAMs contribute a large fraction to the leakage and active power consumption. Thus to achieve the energy minimum operation, subthreshold SRAM design is equally important to the subthreshold processor design. The main challenges for Subthreshold SRAM design is the robustness, high access delay and large area overhead of the bit cells.

1. Noise Margin Stability of the bit cell decreases as we scale down to low voltages. The voltage noise margin for the SRAMs has the upper limit of $0.5 * Vdd$. As we scale down our supply voltages, the noise margin decreases to modest values. Due to this reduced noise margin, the probability of read/write failure in the presence of threshold voltage variations increases. At ultra-low supply voltage the effect of these variations become even more pronounced as the device strength at these voltages depends exponentially on the threshold voltage . The 6T bit cell loses its robustness at subthreshold supply voltages.

2. The reduced I_{on}/I_{off} ratio in the subthreshold, causes considerable delay in gaining sufficient differential voltage drop on the bit lines. This increases the access time of the SRAMs many fold. Also due to this reduced ratio, the probability for read error increases as the bit cells per column of the SRAM array are increased.

To understand the stability concerns of SRAM bit cells in ultra-low voltages, the noise margins of the recently proposed subthreshold bit cells are evaluated in the presence of variations to determine what modifications to the topology are most effective in increasing the stability.
The thesis is organized as follows. Chapter 2 provides basic background on subthreshold operation and shows that the digital circuits retain their functionality at subthreshold voltages via the example of inverter. Chapter 3 provides background on the read and write operation on the SRAM 6T bit cell. In Chapter 4, an overview of the recent subthreshold SRAM bit cells is given. We state our problem statement in Chapter 5 and propose a new subthreshold bit cell in Chapter 6. The metrics used for comparing the stability, performance and energy of the bit cells are described in Chapter 7. In Chapter 8, we discuss the stability, performance and energy results we obtained for different bitcells and compare our proposed bit cell with these bit cells. Finally in Chapter 9, we present our conclusion of this work and the future direction we will be taking.

Chapter 2

Subthreshold Operation

2.1 subthreshold operation

In a transistor operating at subthreshold voltages, the Gate-Source voltage,V_{gs}, is smaller than the threshold voltage, V_{th}, of the transistor. In the above threshold operation of the CMOS transistor, the drift current of the carriers dominate the current flow. However when the supply voltage is scaled down to subthreshold voltages, the electric field along the channel is not able to pull the electrons from the source to drain and as a result the diffusion current starts to dominate the current flow. This is shown in figure below. The subthreshold current is given by the following equation:

$$I_{sub} = I_o e^{(V_{gs}-V_{th})/nV_T}(1 - e^{-V_{-ds}/V_T}) \tag{2.1}$$

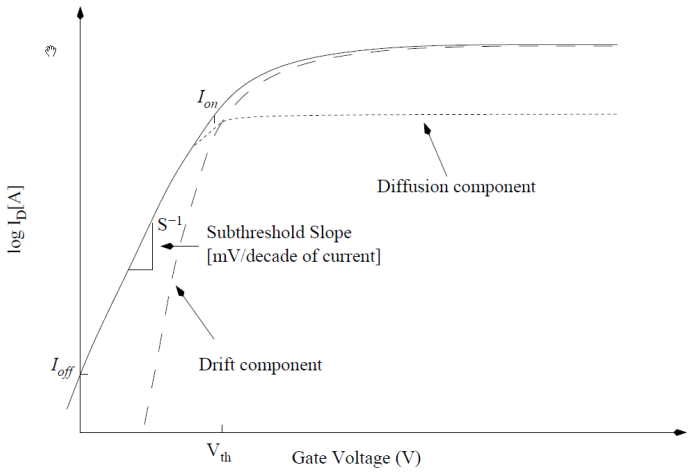

Figure 2.1 Change in the Drain Current of the transistor with gate voltage. In the above threshold, gate voltage diffusion current is the dominant component of the drain current. In below threshold, gate voltage drift current becomes dominant

where, $I_o = \mu_0 C_{ox} \frac{W}{L} V_T{}^2$, V_T is the thermal voltage and 'n' is the subthreshold swing coefficient given by $1 + \frac{C_{dep}}{C_{ox}}$. In subthreshold operation, where V_{dd} is less than V_{th},the I_{on} and I_{off} currents are defined as

$$I_{on} = I_{sub}[V_{gs} = V_{dd}] \tag{2.2}$$

$$I_{off} = I_{sub}[V_{gs} = V_{ss}] \tag{2.3}$$

The drain current in subthreshold region is exponentially dependent on the gate voltage, while in above threshold region it is quadratically dependent on the gate voltage. Due to this exponential dependence, the small changes in the gate voltage can result in large variations in the drain current. Also the exponential dependence of the subthreshold current on the threshold voltage makes it highly sensitive to V_{th} variations. The circuits operating in subthreshold regions thereby become highly prone to process variations. The Random Dopant Fluctuations,(RDF), which have been shown to be the dominant source of V_{th} variation in subthreshold, are increasing as we scale down to lower technology nodes.

2.2 Inverter operation in Subthreshold

The IV characteristic of the NMOS transistor is shown in figure 2.2. It is similar in shape to the IV characteristic at above threshold voltages. This shows that the transistor will have same functionality in subthreshold as that at above threshold voltages. The IV curve also shows that for at $V_{ds} \approx 100mV$, the dependence of the curve on V_{ds} starts to decrease. This is because, for $V_{ds} > 100mV$, the V_{ds} dependent term in the subthreshold equation, $(1 - e^{-V_{-ds}/V_T}) \ll 1$. Figure

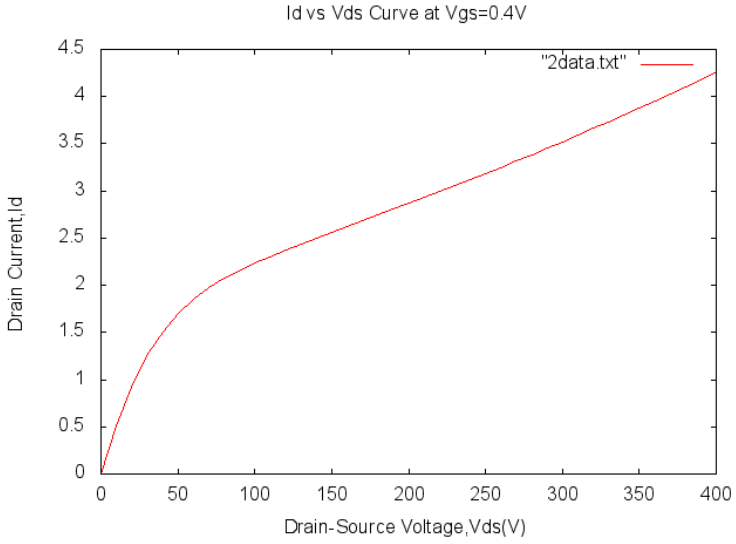

Figure 2.2 Id vs Vds Curve at Subthreshold Voltage. The curve is similar in shape to that at above threshold voltage, signifying similar behavior of the transistor in the subthreshold

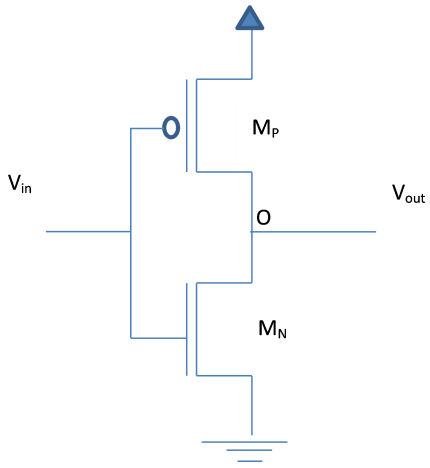

Figure 2.3 Schematic of the CMOS inverter

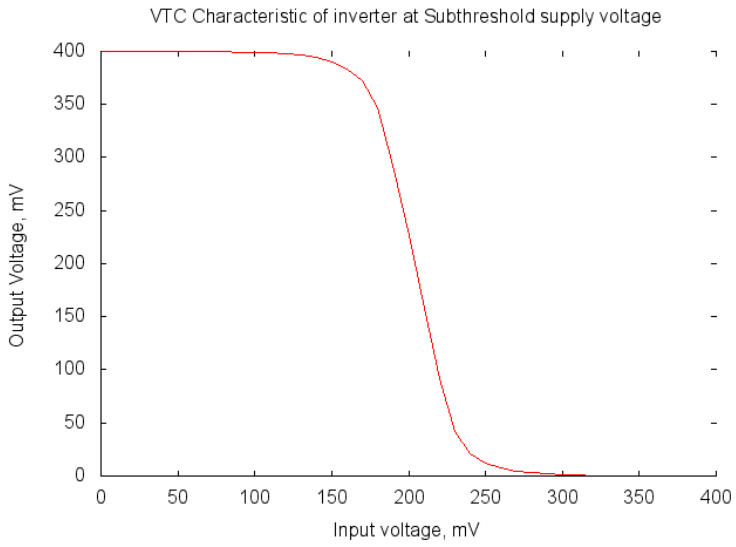

Figure 2.4 VTC of Inverter at Supply voltage of 400mV

2.3 shows the CMOS inverter schematic. The source of pull-down transistor M_N is connected to ground and the source of pull-up transistor M_P is connected to V_{DD}. The input voltage V_{in} is applied at the gate of the two transistors and output of the inverter V_{out} is voltage at node 'O'. The VTC characteristic of the transistor is shown in the figure 2.4. The shape of the VTC is similar to the shape at above threshold voltages. At input voltage close to V_{DD}, the pull-down transistor M_N has larger subthreshold current than pull-up transistor M_P, and voltage at node 'O' decreases. When the input voltage is close to ground, the pull-up transistor M_P has larger subthreshold current than the pull-down transistor M_N and the voltage at node 'O' increases.

Chapter 3

SRAM Operation

3.1 Schematic

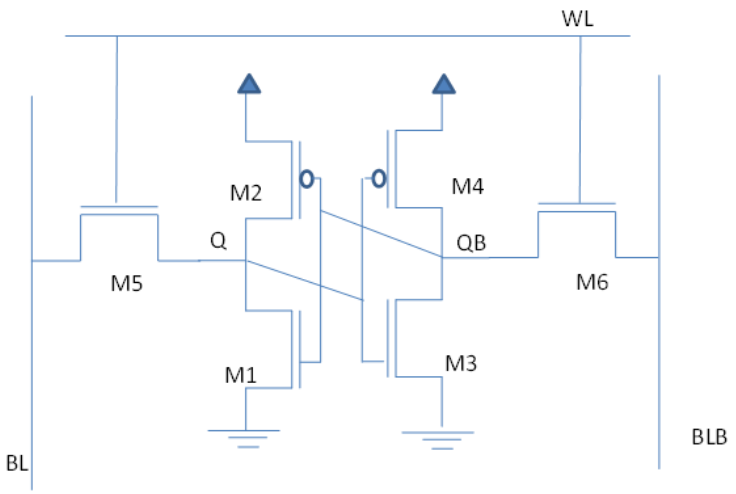

Figure 3.1 Id vs Vds Curve at Subthreshold Voltage. The curve is similar in shape to that at above threshold voltage, signifying similar behavior of the transistor in the subthreshold

The 6T bit cell is most commonly used bit cell structure in the SRAMs. It comprises of two inverter pairs[M_1 to M_4] with feedback loop and two pass transistors[M_5 and M_6] that connect the output of the inverters to the bit line. The schematic of the structure is shown in the figure 3.1. The storage nodes are denoted as 'Q' and 'QB'. 'WL' is the word line and Bit-lines are denoted as 'BL' and 'BLB' The area of the bit cell in 65nm technology is about 0.4-0.5μm^2.

3.2 SRAM Read Operation

SRAM read operation happens in following steps:

1. Precharge Phase: Both the bitlines are precharged to V_{DD}
2. Read Phase: The word line is set high and the pass transistors M_5 and M_6 are turned on . They connect the storage nodes Q and QB with the bit lines BL and BLB. The data stored in the storage nodes is transferred to the bit lines. This creates a small voltage difference between the voltages of the bitlines.
3. Sense Phase: This voltage difference in the bit lines is measured with sense-amplifier, and the output of the sense-amplifier is sent to the DataOut buffer.

The figure 3.2 show the read circuit of the 6T bit cell. It is assumed that the node 'Q' stores logic '1'

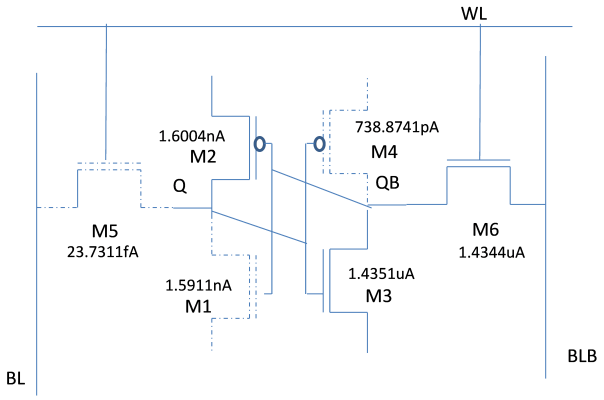

Figure 3.2 6T SRAM Bit cell read circuit at Vdd= 0.4V. (Q='1' and QB='0')

and node 'QB' stores logic '0'. The discharge path of the bit cell consists of the pass transistor M_6 and the pull-down transistor M_3. For successful read operation, the strength of the pass transistor should be less than the strength of the pull-down transistor, so that the voltage at node 'QB' does not rise. Otherwise if 'QB's votlage rises to the threshold voltage of transistor M_1, the data in the cell flips. The cell ratio,α (ratio of the widths of the pull-down transistor and pass-transistor) is usually 1.3 or higher. The read butterfly curve of the SRAM operating at subthreshold voltage is shown in figure 3.3. It shows that the feedback inverter structure retains its bistable state in the subthreshold votlages.

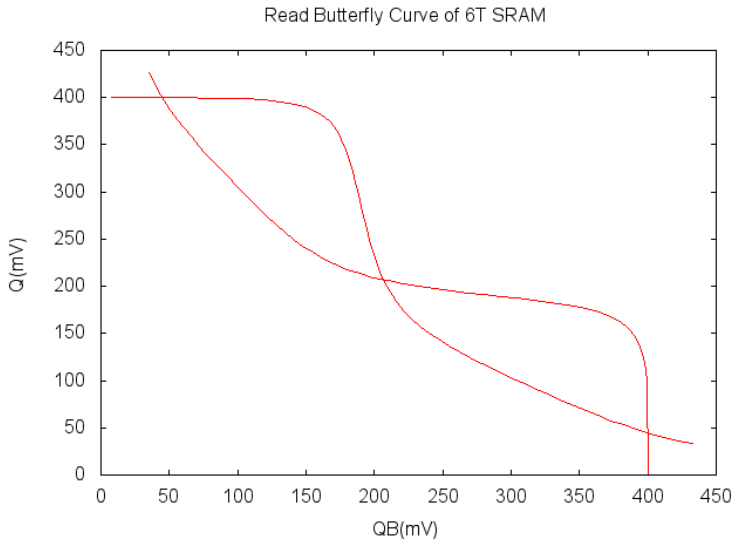

Figure 3.3 6T SRAM Read Butterfly curve at 0.4V supply voltage. (The bit cell retains its bi-stability at subthreshold votlages)

3.3 SRAM Write Operation

For SRAM write operation the data is read from the DataIn buffer and transferred to the bit lines. The word line is then set high and the pass transistors transfer the data from the bit lines into the storage node. The bitlines BL and BLB are charged to logic '0' voltage and logic '1' voltage respectively. For successful write operation the strength of the pass transistor should be higher than the strength of the pull-up transistors, so that logic '1' could be written successfully into the storage node. The pull-up ratio,β (ratio of the widths of the pull-up transistor and pass-transistor) is typically 1.8 or lower.

The write butterfly curve of 6T bit cell is shown in figure 3.4. It shows that the bit cell becomes monostable during write operation that allows for writing new value into its storage node.

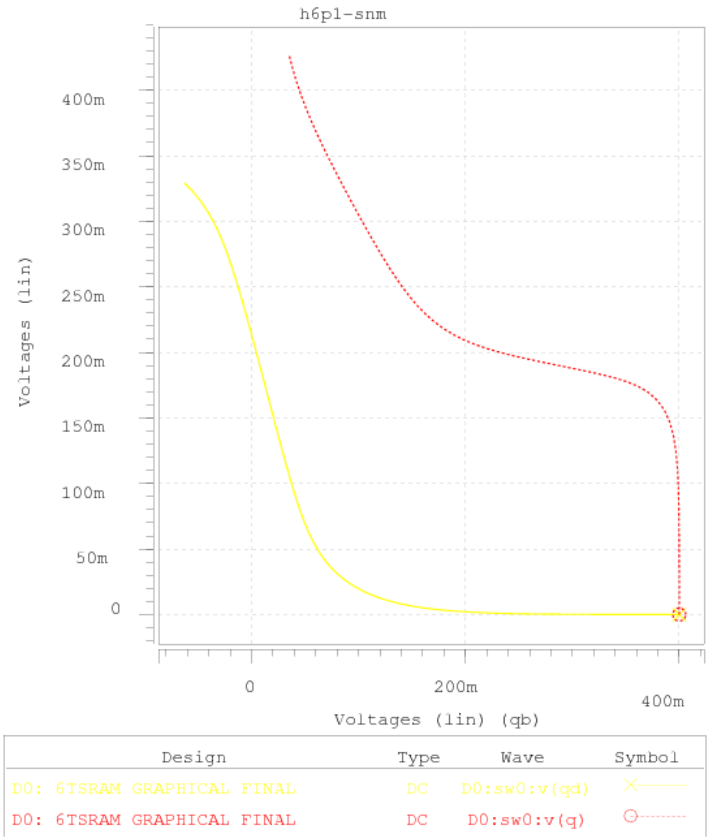

Figure 3.4 6T SRAM Write Butterfly curve at 0.4V supply voltage.(The bit cell becomes monostable during write operation)

Chapter 4

Related Work

4.1 Studies regarding impact of process variations in Subthreshold

To account for the high sensitivity of subthreshold operation, a study was done by Bo Zhai et.al.[12] at the 130 nm technology process. They claimed from their results that Random Dopant Fluctuations(RDF) will become the dominant source of variations in subthreshold. They showed that Drain induced barrier lowering(DIBL), which causes channel length variation and is the main source of threshold voltage variation in above threshold operation, decreases at low operating voltages. Thus the threshold voltage variation caused by channel length variation decreases when reducing supply voltage. Threshold voltage variation due to RDF, being solely dependent on the channel area and not dependent on the supply voltage, plays major role in subthreshold region operation. Figure 4.1

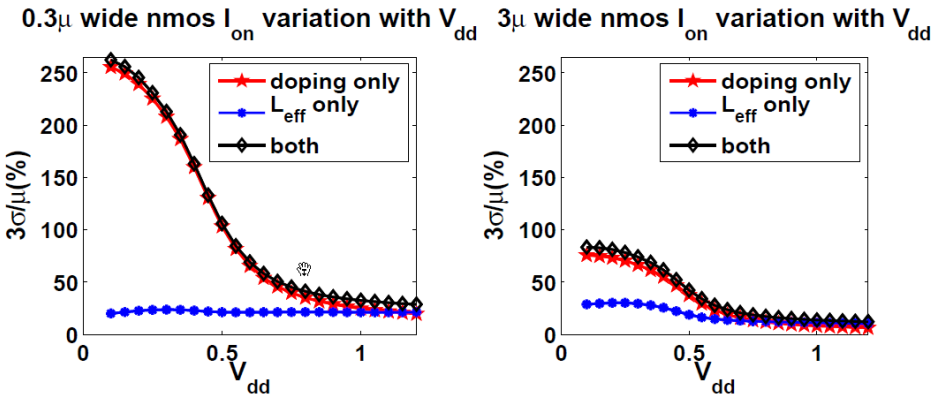

Figure 4.1 $3\sigma/\mu$ of I_{on} due to different variation sources over a wide range of V_{dd}, showing the dominance of RDF in subthreshold operation[source:Bo Zhai et.al. [12]]

shows that I_{on} variation due to RDF continues to increase even in subthreshold region.

In their study, they also proposed upscaling the device size and using larger logic depth pipeline as ways to mitigate effects of RDF variations. Larger Logic Depth Averages out timing variations if stage delays are effectively same for each pipeline stage. Another motivation for larger logic depth comes from the observation that change in the Energy Optimal supply voltage and subsequently change in energy decreases as logic depth increases. However, aggressive pipelining increases the activity factor,(α) which thereby improves the Energy efficiency per Operation as energy is being spent in useful work and not contributing to leakage energy. A trade-off exists between raising α through aggressive pipelining and reducing variation by increasing logic depth. In their results they also showed that Energy optimal Supply voltage increases in the presence of process variations. For nominal case(i.e. without presence of variations), the energy minimum for an inverter chain circuit occurs at depth of 10 inverters. The Energy minimum when considering variations shifted toward larger logic depth of 15 inverters.

Design Strategy	V_{min}	n	Energy/Op (w/o variation)	Energy/Op (w/ variation)
Nominal	130mV	10	15.0 fJ	31.8fJ
Variability-Aware	210mV	15	-	24.2fJ

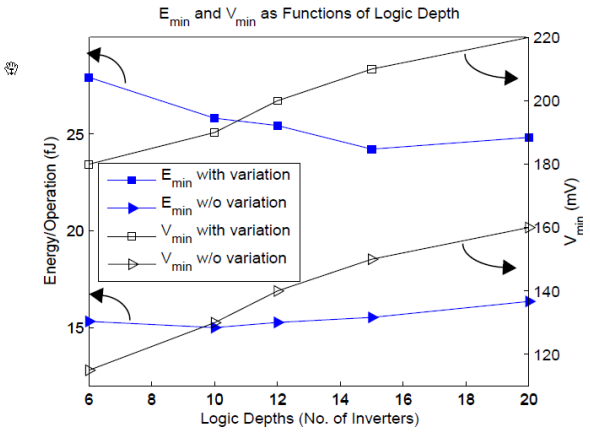

Figure 4.2 Minimum Energy per Operation versus Logic Depth with and without variations[source:Bo Zhai et.al. [12]]

A similar study at the device level was done by Vaddi et.al. [13] They based their studies on the 32nm technology node and analyzed alternate devices like DGSOI for subthreshold operation.

They claimed that these alternate devices ,DGSOI are better candidates in performance, robustness, and PVT insensitivity as compared to bulk static CMOS. They used Double-Gate FinFET(DGFinFET) as DGSOI device to compare with bulk static CMOS. They claim for the suitability of DGSOI device for subthreshold by showing that it gives better dc-response than bulk-CMOS as supply voltage is scaled down. Better VTC characteristics implies that DGSOI will have better noise margins than bulk CMOS. They claim to have observed 60-70% improvement in Power Delay Product as compared to CMOS bulk device. Their results show that FinFETs have 40% lower

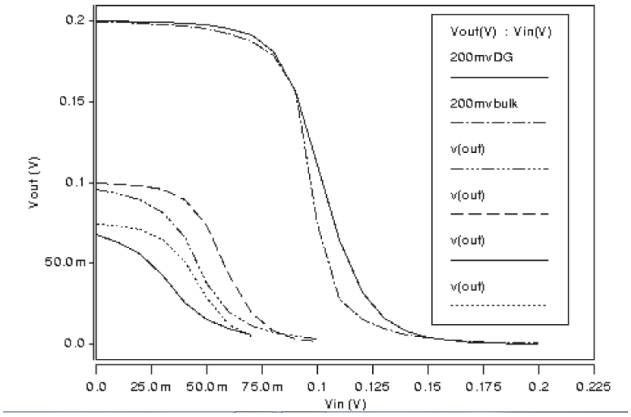

Figure 4.3 VTC comparison for 32nm DGSOI and bulk static CMOS inverters with scaling in supply voltage for Subthreshold[source:Vaddi et.al. [13]]

power variation, 34% lower delay variation and 47% lower PDP variation as compared to bulk CMOS circuit.

4.2 Subthreshold SRAMs

In the recent years, several SRAM bit cells have been proposed that have been claimed to work in the Subthreshold region successfully. These bitcells have higher stability than 6T bit cell at subthreshold voltages and employ one or more of the following modifiations over 6T.

1. Breaking the feedback between the inverters using Read/Write stages
   To increase the write ability of the bit cell, some proposals break the feedback. Thus the

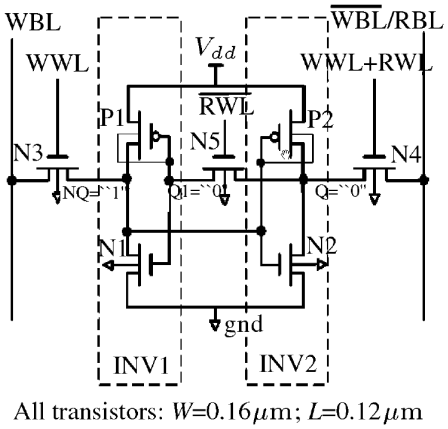

Figure 4.4 7t_1

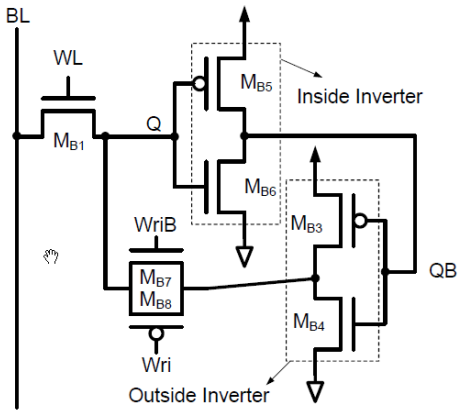

Figure 4.5 7t_2

write ability now only depends upon the strength of the pass transistors. Some proposals break the feedback during the read phase. If one storage node flips during read due to large voltage noise from bitlines, the other storage node retains it original value. However the stability of the bit cell in this approach, is dependent on the the transistor which controls the feedback. If this transistor is not able to effectively stop the feedback during write or read phase due to the presence of variations, the stability gains over standard 6T are marginal. Figure 4.4 and 4.5 show example of this category. The bit cell 7T-1[10] cuts off the feedback between the inverters when the cell is being read. The bit cell 7T-2 [1] cuts this feedback when the cell is being written.

2. Isolating the storage nodes from the bit lines
   The motivation here is to remove the voltage noise coming from the bitlines into the storage nodes. This is typically done in two ways

   (a) Inserting buffer between bitlines and storage node

   By inserting the buffer, the voltage noise from the bit lines only affects the voltage at the buffer and not at the storage nodes. Also as the discharge path for reading '0' is separated from the inverter of the bitcell, the voltage at storage node 'QB' in these bitcells is lower than that of conventional 6T bit cell. This allows to achieve the Read static noise margin, RSNM, close to the hold SNM of the bit cell. This method is limited by its greater read access delay. The 8T, 9T-1 [1], 10T-CC[4] and 10T-KL[3] bit cells shown in figures 4.6 - 4.9, are buffer based designs.

   (b) Connecting the bitlines to a psuedo-Storage node.
   This Pseudo-Storage node is created by adding one or more pair of pull-up or pull-down transistors to each of the inverters. The idea is same as above to reduce the current influx from the bitlines into the storage nodes. The 8T-2 [11] and 9T-2 [7] bit

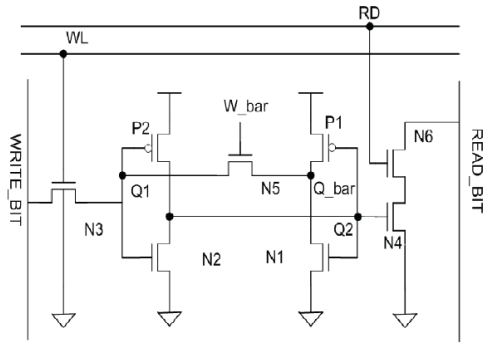

Figure 4.6 8T bit cell

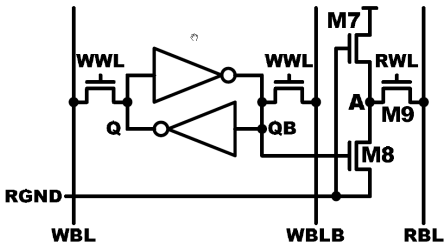

Figure 4.7 9T_1 Bit cell

cells shown in figures 4.10 and 4.11 are examples of this approach.

3. Using Virtual Ground or Virtual Vdd to facilitate the reading and writing operation

4. Improving the I_{on}/I_{off} ratio on the bitlines by making the current leakage data-independent The conditions of leakage current in the bit cell is shown in the figure. This ratio determines the maximum number of bit cells that can be put in a single column of SRAM array.

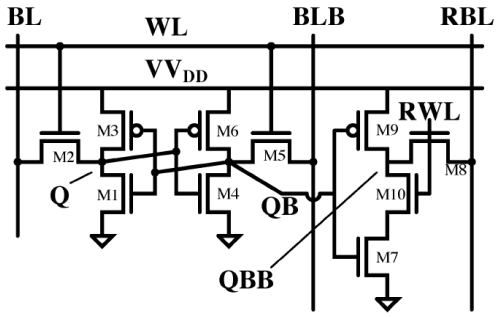

Figure 4.8 10T-CC bit cell

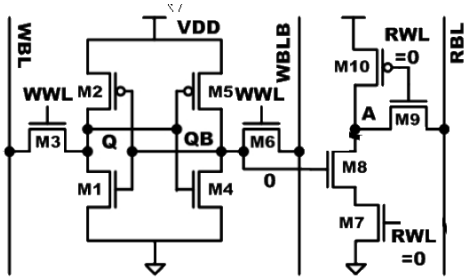

Figure 4.9 10T-KL bit cell

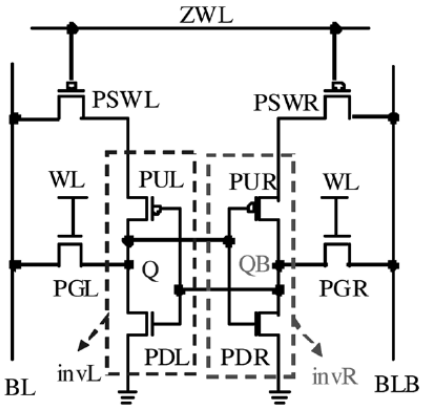

Figure 4.10 8T_2

5. Replacing Inverter pair with a different structure that is more stable to external noise
   The schmitt trigger [5] has been recently proposed to be a better alternative to the inverter in SRAM bit cell in handling variations. It achieves this by increasing the threshold voltage of the pair storing '1', so that fluctuations in the voltage of storage node '0' does not cause

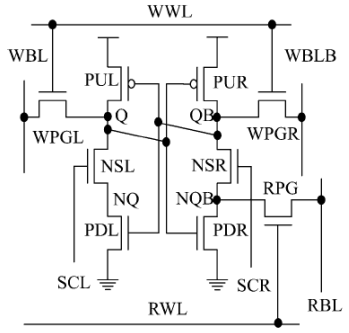

Figure 4.11 9T_2

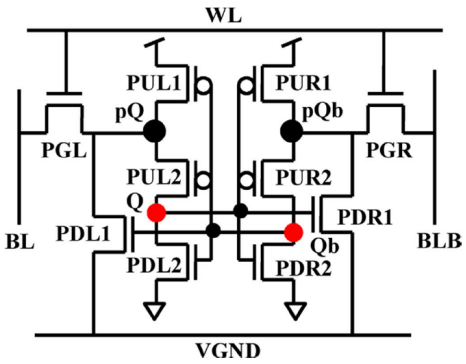

Figure 4.12 10T_PPN

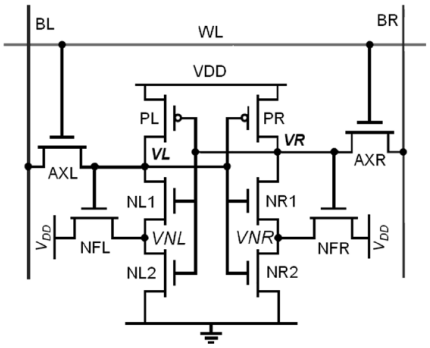

Figure 4.13 10t_schmitt

flipping of the bit cell. The 10T schmitt trigger bit cell is shown in figure 4.12 . Another example of this approach is the 10T-PPN [8] bit cell which is shown in figure 4.11.

Chapter 5

Problem Statement

5.1 Improving the stability and performance of Subthreshold SRAM by changes to topology

The stability of SRAM bit cell degrades at lower supply voltages. The noise margins of SRAM bit cell at subthreshold voltages are very small as compared to those at the above threshold voltages, making the bit cell very likely to flip contents during the read access. Figure 5.1 gives a comparison of the butterfly curves of the conventional 6T bit cell in above threshold voltage and subthreshold voltage.In the SRAMs operating at above threshold voltages, the stability of the bit cell is sensitive to the cell ratio for read operation and the pull-down ratio for the write operation. However, in subthreshold region, these changes to the strength of pass-transistor relative to the pull-up and pull-down transistors do not change the stability of the bit cell by any considerable factor(figure 5.2). Changes to the topology of the bit cell are required to make the bit cell stable at ultra-low voltages.

The stability of the bit cells at subthreshold voltages is further decreased due to its increased sensitivity to variations. The figure 5.3 shows that at supply voltage of 0.3V, the noise margin of 6T bit cell almost diminishes in the presence of 10% threshold voltage variations for 65nm technology node bit cell. Among the primary causal agents for reduction in the noise margins of the bit cell is the current influx into the bit cell storage nodes from the bit lines. As this current is exponentially dependent on the threshold voltage, storage node voltage becomes highly sensitive to threshold voltage variations, which reduces its noise margins even further. The leakage current share increases with supply voltage scaling which has the effect of decreasing the I_{on}/I_{off} ratio of the bit cell.(The I_{on} is the current flowing from the bit lines into the storage node '0' of the accessed bit cell. The I_{off} is the current flowing from the storage node '1' of the unaccessed bit cells on the same column into the bit lines).The consequence of this reduced ratio is the decreased bit line voltage drop which may result in a read failure.

Besides stability, operating in subthreshold region also worsens the performance in terms of access time. The delay increases exponentially in the subthreshold region, compared to linearly at above threshold supply voltages. The subthreshold SRAMs which have been proposed to have

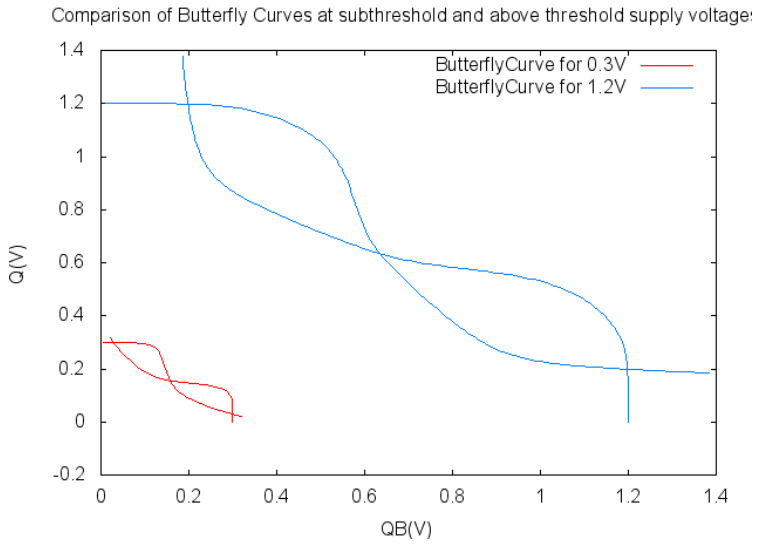

Figure 5.1 Comparison of Butterfly curves at subthreshold and above threshold voltages

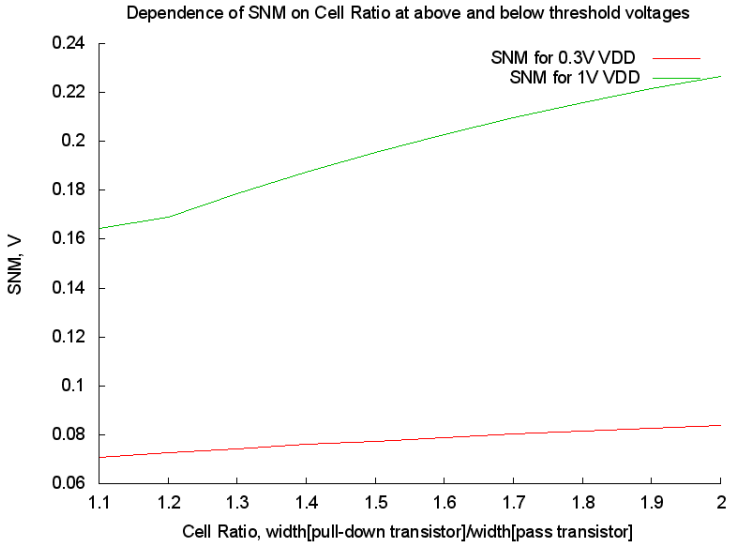

Figure 5.2 Comparison of SNM senstivity to Cell ratio at subthreshold and above threshold voltages

higher stability than the 6T bit cell also suffer from large read access time. A comparison of the read access delay of the 6T bit cell at above threshold and below threshold voltage is shown in the figure 5.5 and figure 5.6. Due to the reduced drive strength of the transistors in subthreshold, it takes longer time to achieve the desired drop on the bit lines. The variations again play their role to make the time to access the bit cell highly variable. The current flowing through the read

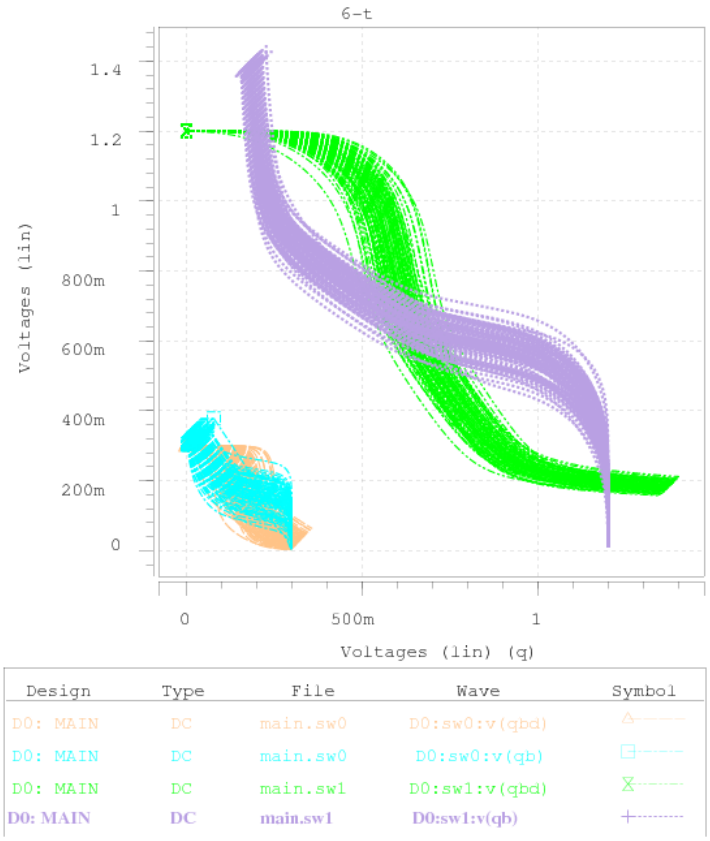

Figure 5.3 Comparison of Butterfly curves at subthreshold and above threshold voltages in the presence of 10% Vth variation for 1000 Monte Carlo simulations.

discharge path, is exponentially dependent on the threshold voltages of the transistors in this path. For the 6T bit cell, the discharge current becomes sensitive to the threshold voltage variations in the pull down transistor and the pass transistor. The increased variability in the access time makes it difficult for the SRAM to meet the frequency requirements

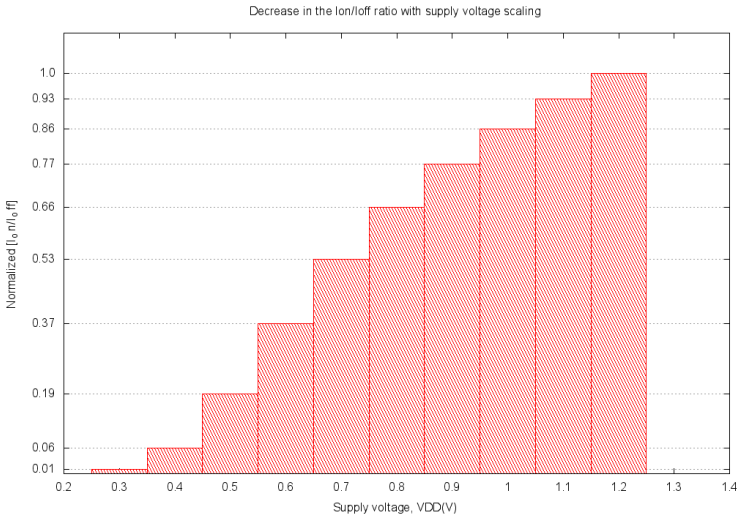

Figure 5.4 Change in I_{on}/I_{off} ratio with scaling of supply voltage normalized to the I_{on}/I_{off} ratio at vdd=1.2V

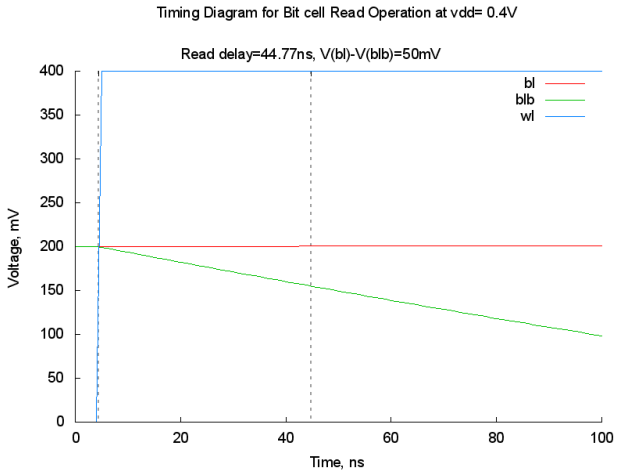

Figure 5.5 Timing Diagram for Read Operation at subthreshold voltage

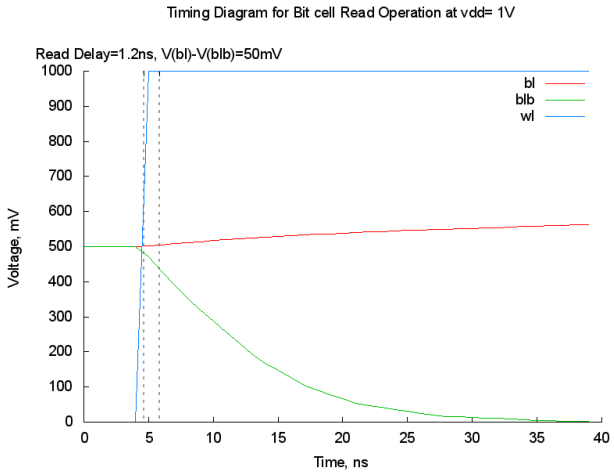

Figure 5.6 Timing Diagram for Read Operation at above threshold voltage

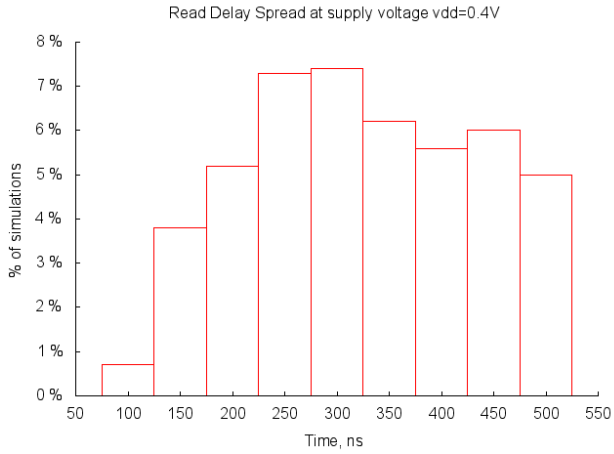

Figure 5.7 Read Delay Spread at subthreshold voltage. Read access failure for 52.8% simulations

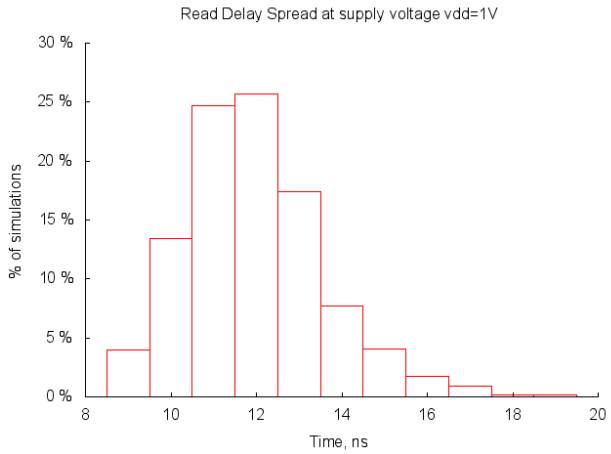

Figure 5.8 Read Delay Spread at above threshold voltage

Chapter 6

Proposal

We present our Subthreshold Bit cell proposal in this chapter. The bit cell is based on the premise that isolating the bit storage node from the bitlines improves the SNM. The access time is improved by using the storage node to control the discharge path consisting of only single transistor. In the buffer based bitcells that improve the SNM on the same premise, the storage node value is first stored in a buffer and through that buffer the value is read into the bit lines. This makes the discharge path longer, resulting in higher access time.

6.1 Bit Cell Architecture

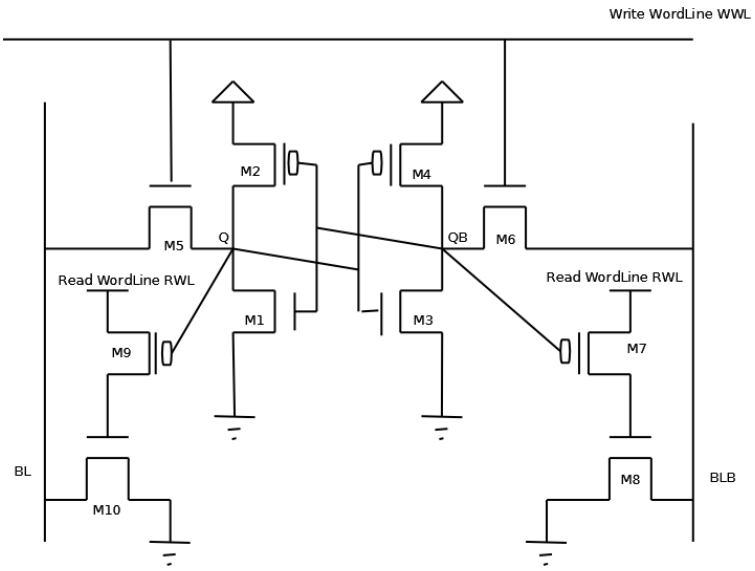

Figure 6.1 Proposed Bit cell Schematic

The figure 6.1 shows the proposed bit cell architecture. The inverter structure is the same as

that of 6T bit cell. The nodes Q and QB are used to control the Pull-Up transistors M7 and M9, those have their source connected to Word-Line(WL). The drain of these transistors is then used to control the Pull-Down transistors M8 and M10 that have their source connected to ground and drain connected the bit lines.

6.2 Read Operation

The read operation starts with the read word line, RWL set high and the bit lines BL and BLB precharged to VDD. Suppose the node Q stores logic '1' and node QB stores logic '0'. The node QB turnes the Pull-Up transistor, M7 on and the voltage at the gate of the Pull-Down transistor, M8 starts to rise. When the voltage at its gate rises above its threshold voltage, it starts discharging the bit line BLB. On the other side of the bit cell, since node Q is storing logic '1', the Pull-Up transistor, M9 is switched off and the gate voltage at the Pull-Down transistor, M10 is less than its threshold. As a result there is no discharge path for Bl.

6.3 Write Operation

The write operation starts with the write word line, WWL set high and voltages at bit lines BL and BLB applied same as the data to be written. This Write operation of the Bit cell is similar to that of the 6T bit cell. The pass transistors M5 and M6 are used to write into the bit cell.

Chapter 7

Evaluation Methodology

We have evaluated the stability and performance of the bit cells using simulation done with Hspice tool with 65nm Process technology PTM model. The node storing logic '0' is denoted by QB and node storing logic '1' is denoted by Q. The simulations were first done for single bit and then for 1kbyte sram array with 256 rows an 128 columns.

7.1 Simulation Tool: Hspice

Hspice is a tool for circuit simulation and analysis that works with MOS device models. It can precisely predict the timing, power consumption, functionality and yield of the design. We have simulated the SRAM circuits using the steady-state analysis of HSpice (also known as DC analysis) to obtain the noise margins, and using the transient analysis to obtain the access delay and energy consumption. To analyze the performance in the presence of variations, Monte Carlo analysis provided by HSpice was used.

7.2 Simulation Metrics

The bit cells were evaluated on the basis of following metrics.

7.2.1 Metric for Stability

The read stability of the bit cell is the amount of noise it can handle from the bit lines before flipping the data in the storage nodes. We have measured it according to the N-Curve method.

1. N- Curve N.Curve analysis was proposed by Evelyn Grossar et.al. to evaluate the stability of the bit cells. This analysis provides the noise and current margins for both read and write through the same N-shaped Curve.

   (a) N-Curve Circuit For extracting N-Curve, the bit-lines are both clamped at V_{dd} and the wordline is activated to put the cell in read operation mode. A voltage sweep V_{in} from

0V to V_{dd} is applied at the QB internal storage node V_r and the corresponding current I_{in} is measured. In three points A, B and C of the N-Curve, the current injected in V_r is zero. A and C correspond to the two stable points of the butterfly curve while B corresponds to the meta -stable point. When points A and B coincide, the cell is at the edge of stability and a destructive read can easily occur.

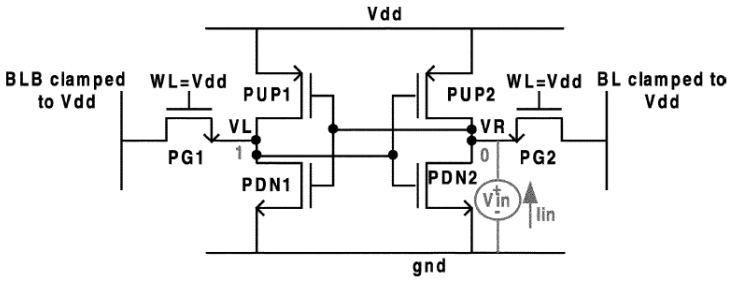

Figure 7.1 N Curve Circuit

(b) N-Curve metrics

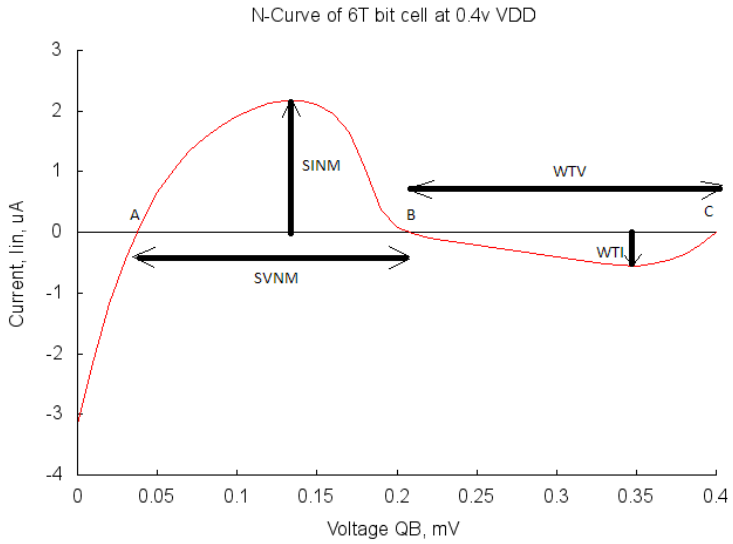

Figure 7.2 N Curve Metric

(c) Read Stability Criteria

i. Static Voltage Noise Margin, SVNM Measured as the distance between the points A and B, It is the amount of DC voltage noise from the bit lines that storage node QB can handle before flipping to value '1'.

ii. Static Current Noise Margin, SINM Measured as the maximum height of the curve between points A and B, it is the peak current noise from the bit lines that the storage node QB can handle before the voltage at that node rises to above the threshold of the inverter

(d) Write Stability Criteria

i. WTV Measured as the distance between the points B and C, It denotes the write trip point voltage. It is the minimum voltage drop on the bitlines that will cause the read failure.

ii. WTI Measured as the maximum negative height of the curve between B and C, it is the peak current noise from the bitlines that writes the cell when both bit-lines are kept at V_{dd}. This is the current margin of the cell for which its content changes. The ability to write the cell when both the bit-lines are clamped at V_{dd} results actually in a destructive read operation; therefore the absolute value of WTI should be large enough to cope with read stability requirements.

7.2.2 Metrics for Performance

(a) Read Access Time for a single bit cell is taken to be the time required to create a voltage difference of 50mV on the bit-lines which is used by the sense-amplifier to sense the data stored. The access time is calculated from the moment the Word line 'WL' pulse rises to 0.5 V_{dd}. For SRAM array, Read Access Time is taken to be time delay between the activation of OEN signal and correct value appearing at the output of the sense amplifier. This is an important metric because it determines the speed of memory circuit. Smaller access time of SRAM cell will make it faster to work with high speed computing systems. The variations due to aging effect, process variations, etc. change the behavior of cross coupled inverters in SRAM cell which results in access time failure

7.2.3 Metrics for Energy Efficiency

(a) Energy spent per Access. The total energy spent in reading bit value '0' and '1' is used as the metric for energy efficiency.

7.2.4 Modeling Variations

The local and global V_{th} variations have been added to the bit cells. The variations are added to the spice code using the variation block feature of the HSPICE. Both the local and global V_{th} variations are modeled as univariate independent random variable with normal distribution. V_{th} Mean = V_{th0} technology parameter V_{th} Variance = 10 %. The HSPICE defines the local and global variations as follows:

(a) Global Variations are defined as variations in device characteristics from lot to lot, wafer to wafer and chip to chip; they are caused by variations in starting material and differences between equipment and procedures. Global Variations affect all devices with the same model name in the same way.

(b) Local Variations are defined as variations between devices in proximity, or with common centroid layout on the same chip; they are caused by the microscopic variations in materials and geometry, and affect different devices differently

To measure the effect of these variation, Monte-Carlo simulations have been performed. The flow chart in figure, shows how the HSPICE perfoms monte-carlo simulation with variation blocks.

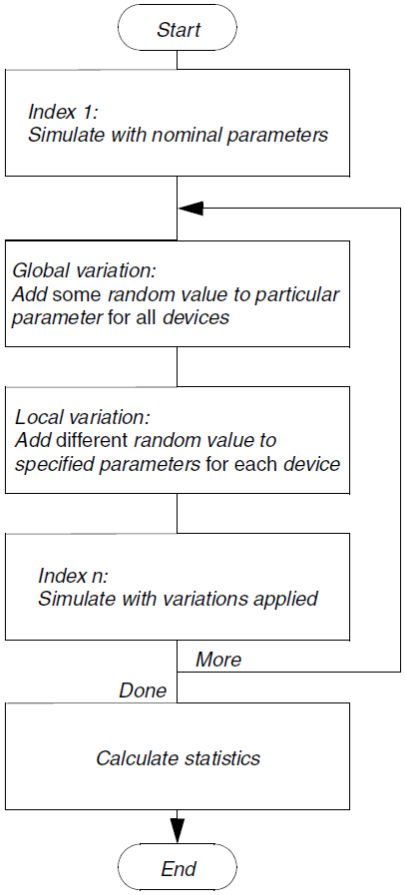

Figure 7.3 HSPICE Monte-Carlo Analysis with Variation Block

Chapter 8

Experiment Results and Discussion

8.1 Stability Comparison

We have analyzed the stability of the bitcells in terms of their noise margins, storage node QB voltage spread and the magnitude of the bitline current flowing into the storage node QB during the read access at the subthreshold supply voltage of 400mV. The ideal characteristics for a stable bit cell would be high voltage and high current noise margins with voltage at QB to be V_{SS} and voltage at node Q to be V_{DD}. However, in actual bit cells, the voltage at node QB is a small magnitude higher than V_{SS} and the voltage at node Q is slightly lower than V_{DD} . For 6T, the voltage at QB=399mV and voltage at Q=24.7mV (figure 8.1).
In order to achieve sufficient bitline voltage drop so as to perform successful read, the bitline current flowing through QB into the ground should be large enough. However this also results in the rise of the voltage at node QB. In the traditional above-threshold operation, this influx of current into QB from the bitlines does not cause any appreciable rise in the node voltage. However, when operating in subthreshold, the switching threshold voltage of the inverter,V_m is smaller as compared to above threshold, for example, assuming that it is $0.5 * VDD$, for 0.4V supply voltage, V_m is only 0.2V . The discharge current at subthreshold voltages, has the potential to rise the QB node voltage close to this switching threshold voltage of inverter, thereby reducing the read noise margin of the bit cell considerably. Bitcells such as, 8T and 10T, attempt to limit this current influx into QB by connecting the node QB to the bitlines through a buffer. The buffer provides a separate discharge path for the current to flow from the bitlines into the ground without flowing through QB and thus making the read margin same as hold margin.

As figure 8.2 shows these buffer-based bitcells are able to limit the QB node voltage to much lower voltages when compared to 6T bitcell. The voltage at QB node of the 8T bitcell is just 0.026mV while the voltage at the 6T's QB node is about 24.7mV. Similarly for the 10T-CC and 10T-KL bit cells, the QB node voltage is just 0.025mV and 0.089mV. The current flowing from the bitlines into the storage node QB for 8T, 10T-CC and 10T-KL are $4.5846 * 10^{-10}A, 4.5846 * 10^{-10}Aand 3.3245 * 10^{-10}A$ as compared to $1.4344 * 10^{-6}A$ for 6T bit cell. Our proposed bit cell

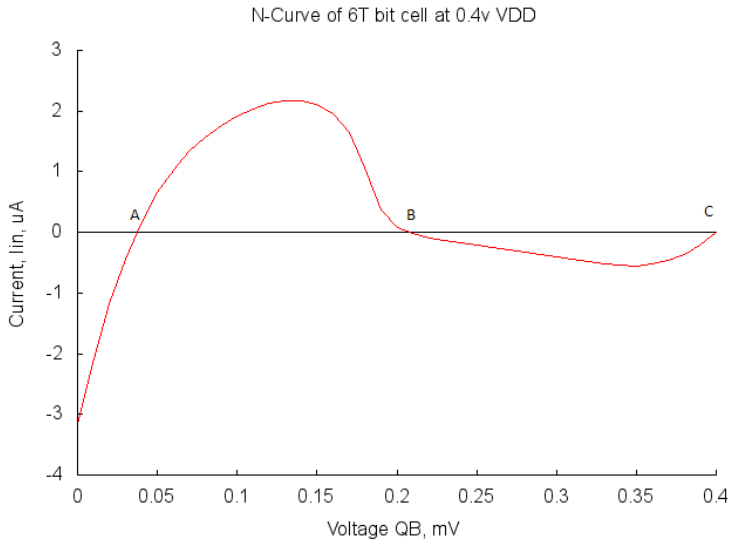

Figure 8.1 N-Curve of 6T-ST bit cell

has the QB node voltage of 0.05mV and $6.8458 * 10^{-10}A$ bitline current flowing into QB. These current and voltage values are very small compared to 6T as shown in the figure, where they seem to be nominal when normalized to 6T values.
The exceptions here are the 9T-2, 10T-1 and 10T-ST bit cells, that have higher storage node voltage despite small bitline leakage current. In the 9T-2 bit cell, the bit line is not directly connected to the storage node QB, but to pseudo-storage node that is connected to QB through a pull-down transistor. This pull-down transistor is switched off during the read.This explains the small current flowing into QB from bitlines. The rise in the voltage of QB can be explained from the observation that the node QB is cut-off from the ground during read operation and is only connected to the write pass transistors and the pull-up transistor. In 10T-1 bit cell also the read bit lines are connected to a pseudo storage node that is connected to the actual storage nodes through a pull-up transistor. This explains its lower bit line current. Since, its actual storage node is not directly connected to the ground, but rather through a pull-up transistor, the node voltage is higher at QB. In 10T-ST, the storage node QB has its pull-down transistor's source at higher voltage than gnd, and so its node voltage is also higher. Since the drain-source voltage for the pass-transistor connecting QB to bitline is now reduced, the bit line current flowing into QB also reduces.

This isolation of the storage nodes from the bitlines also reduces the coupling of variations in bitline voltage with the storage node voltage. For 6T bitcell, with 10% variation in Vth, the current flowing from the bitline into QB through pass-transistor showed variations of σ=1.2543μA with mean=1.5265μA. While for 8T bitcell, for the same V_{th} variation, the bitline current flowing into QB showed variation of only σ=1.23nA with mean=2.8nA. Figure 8.3 gives a comparison of the variation in bitline current flowing into QB of the bit cells. It shows that the bit cells that have large bitline current also have large variations in this current. The bitcells with buffer between

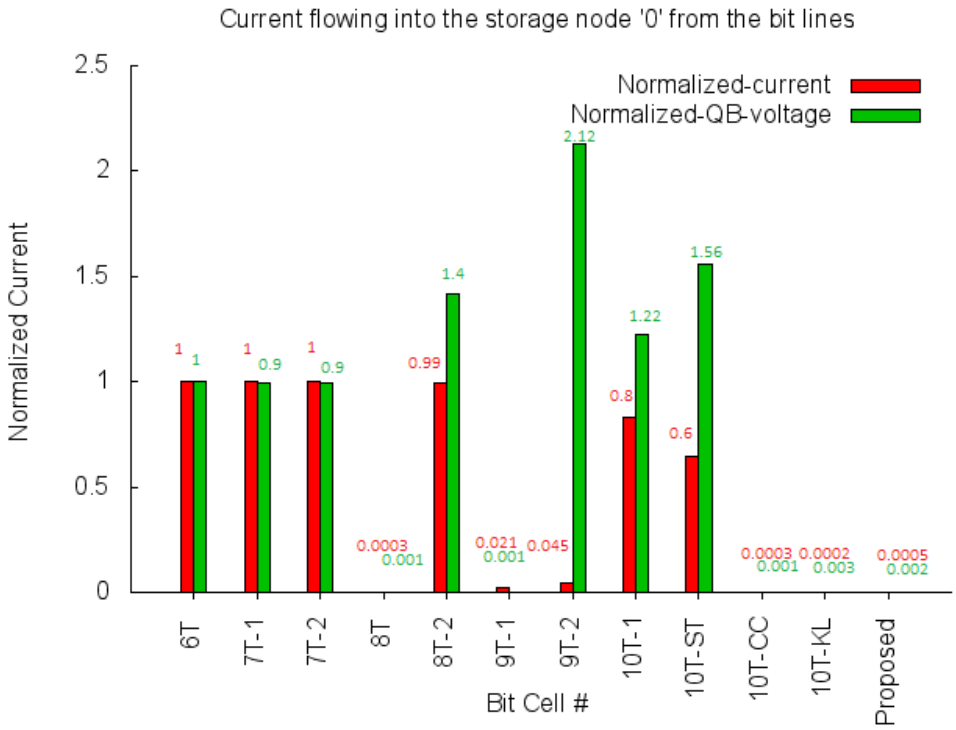

Figure 8.2 The normalised current flowing from bit lines into the storage node '0' and the normalized voltage at storage node '0'

storage node and bitline show minimum variation in this bitline current. The Schmitt trigger bit cell which has a smaller magnitude of bitline current flowing into QB than 6T also shows to have comparatively smaller variation(σ=0.78μA with mean=0.96μA) in the this current . Since the QB voltage is sensitive to bit line current flowing into QB, the nodes with higher bitline current show larger variations in their storage node voltages. The figure 8.4 shows that the bit cells that have larger node QB voltage value, also have larger variations in this voltge. The deviation in the node QB voltage for 6T is about 20.43mV. For 8T bit cells the deviation in QB node voltage is just about 0.31mV. For our proposed bit cell, the node QB σ=0.14mV.
The figures 8.11 to 8.14 give a comparison of the N-curve metrics for the bit cell in 1Kbyte SRAM array.

As discussed before, the discharge path during read in 8T and 10T bit cells is separated from the inverter structure of the bit cell. By integrating the buffer into the structure of the inverter we arrive at a structure that is similar to the schmitt trigger based bit cell. The benefit of integrating the buffer into the storage node inverter structure is that it provides control over the switching threshold voltage of the inverter based on the voltage at the storage node. The schmitt trigger based bit cells are able to increase the switching threshold voltage at the storage node Q. This increases the stability of the bit cell during read operation as it can now handle much larger voltage rise in the storage node QB. The comparison of the switching threshold voltages for the 6T inverter and

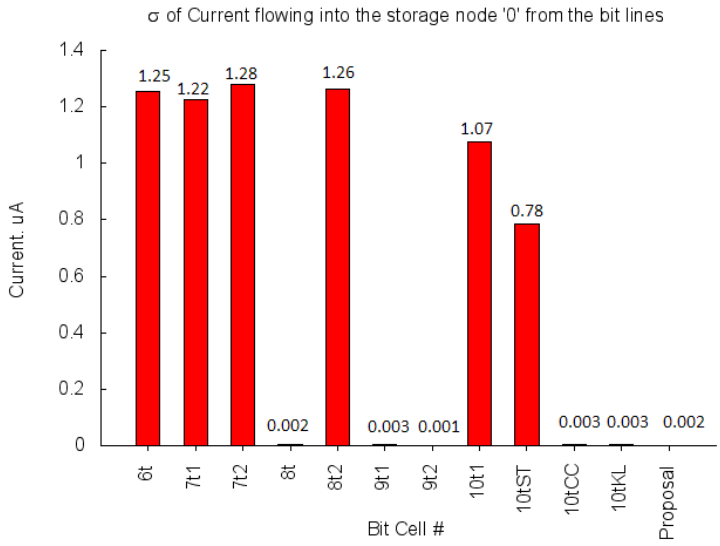

Figure 8.3 The σ of current flowing from bit lines into the storage node '0'

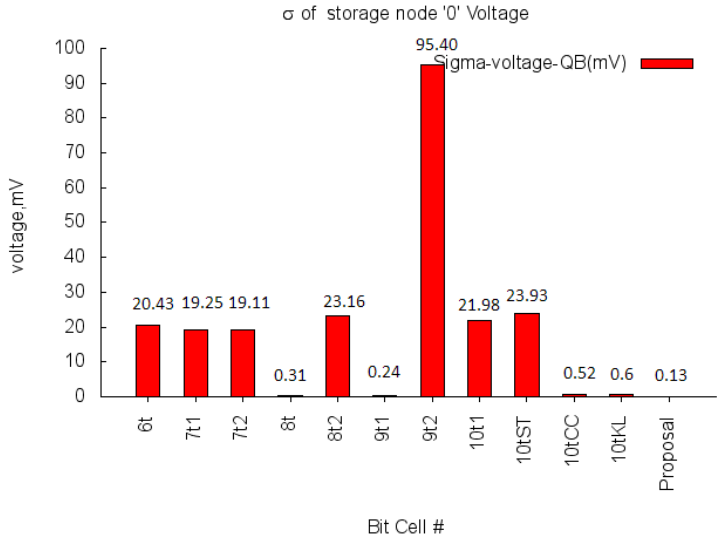

Figure 8.4 The σ of the storage node '0 voltage'

10T ST inverters is shown in the figure 8.5. The switching threshold voltage for the schmitt trigger node Q inverter is 20mV higher than inverter storing QB. Also it can be seen that the switching slope for ST is more closer to ideal switching slope than 6T bit cell. The increase in the stability of the ST structure is shown in figures 8.6 - 8.9 which show lower spread for 10T-ST VTC than 6T inverter structure. The comparison of noise margins of the bit cells in figure8.11 shows that 10T schmitt trigger bit cell is far more resilient to variations than other bit cells. In N-Curve for the ST

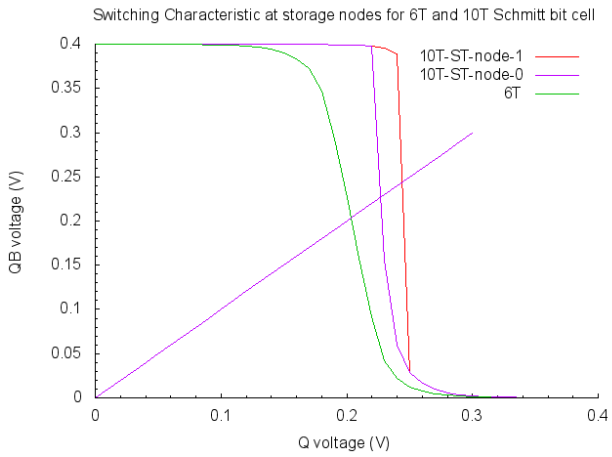

Figure 8.5 Comparison of the switching curve for storage node for 10T Schmitt and 6T

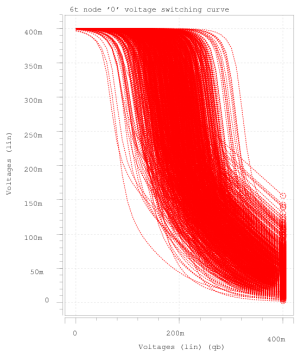

Figure 8.6 6T switching curve spread for node voltage '0'

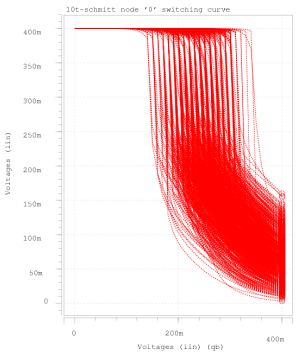

Figure 8.7 10T Schmitt switching curve spread for node voltage '0'

bit cell, shown in figure 8.10, the height of the curve from point A to point B remains relatively flat for large voltage range of QB. This again shows the stability of the ST based structure and can be attributed to the high threshold of node Q and the sharp switching slope of the this bit cell. However the comparison of the N-Curves of the 6T and 10T bit cell shows that the point A for ST is at higher voltage than that for 6T. This corresponds to having higher voltage at the node QB for ST and thus limits the voltage noise margin SVNM. This increase in the voltage at node QB is due to the current flowing into the node PQB from feedback transistor and the current flowing into QB from bit line. The figures 8.11-8.14 give the comparison of the stability of our proposed bit cells with other bit cells in 1Kbyte array configuration in terms of stability metric. The proposed bit cell isolates the bitlines from the storage node. Hence it have similar stability as the buffer based bitcells like 8T and 10T.

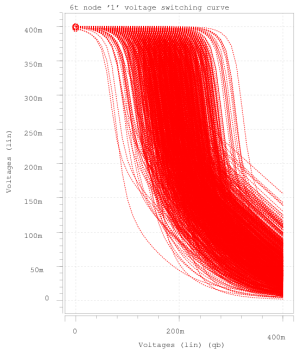

Figure 8.8 6T switching curve spread for node voltage '1'

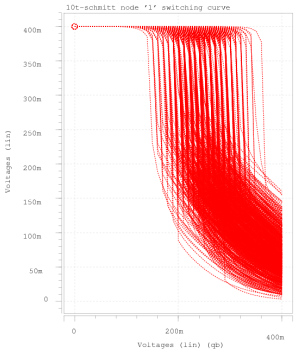

Figure 8.9 10T Schmitt switching curve spread for node voltage '1'

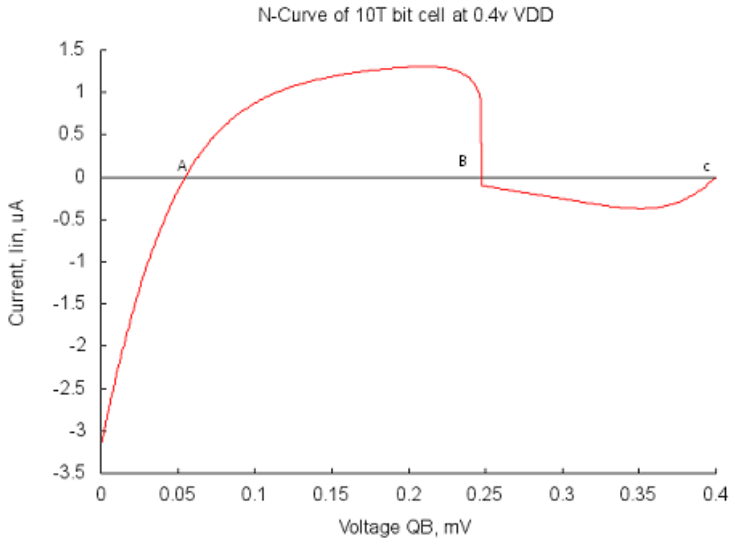

Figure 8.10 N-Curve of 10T-ST bit cell. The n-curve shows that 10T-ST bitcell can withstand high current noise, SINM, even when the voltage at node QB reaches very close to the metastable point B.

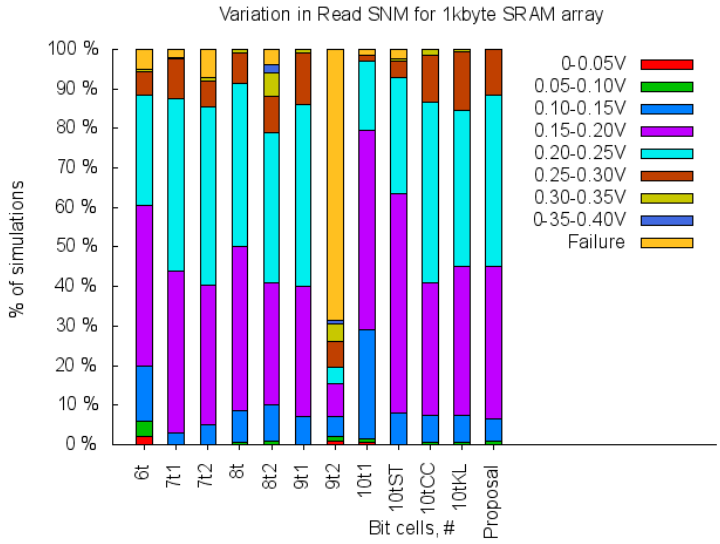

Figure 8.11 The voltage noise margin comparison of the bit cells in 1Kbyte SRAM array. The figure shows that the buffer based bitcells (8T, 9T1, 10T, 10TCC , 10TKL) have less failures in read SNM. Our proposol has SNM variation similar to these bitcells

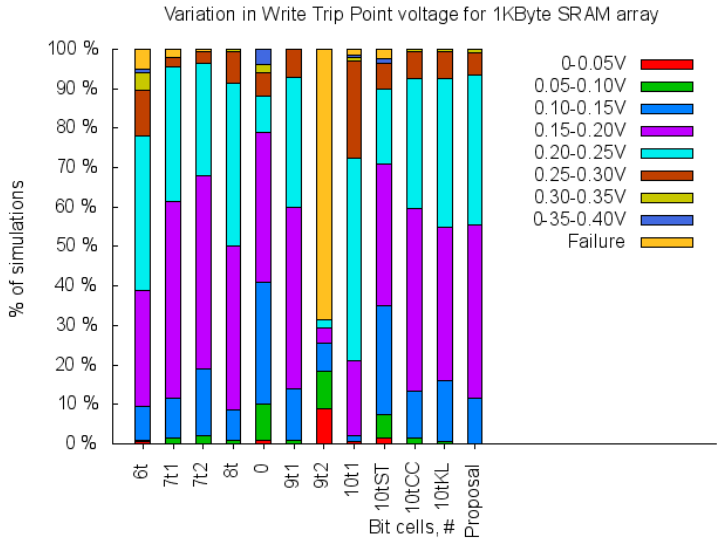

Figure 8.12 Comparison of variation in the write trip point of the bit cells in 1Kbyte SRAM array.

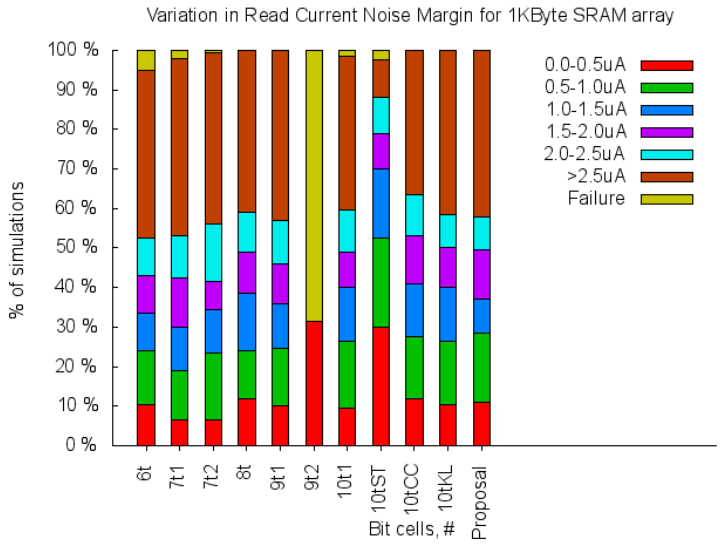

Figure 8.13 Comparison of the read noise current margins of bit cells in 1Kbyte SRAM array

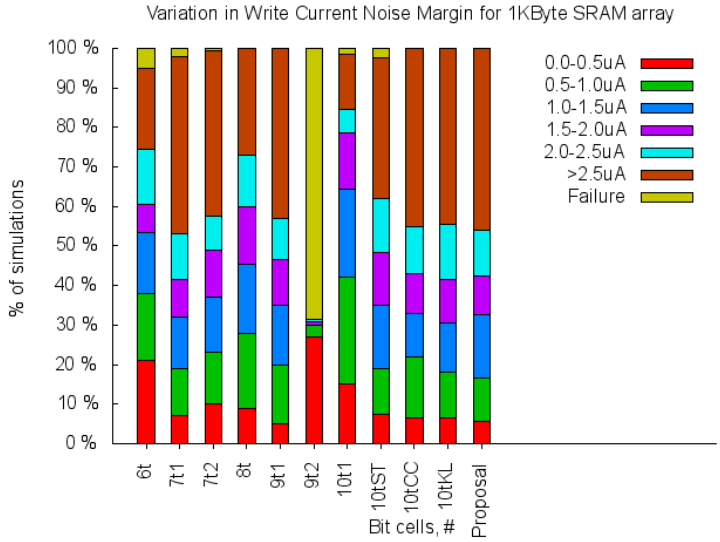

Figure 8.14 Comparison of the read noise current margins of bit cells in 1Kbyte SRAM array

8.2 Performance Comparison

The stability of the schmitt trigger based and buffer based bit cells come at a considerable cost of performance. The access time of these bitcells is more than that of 6T.

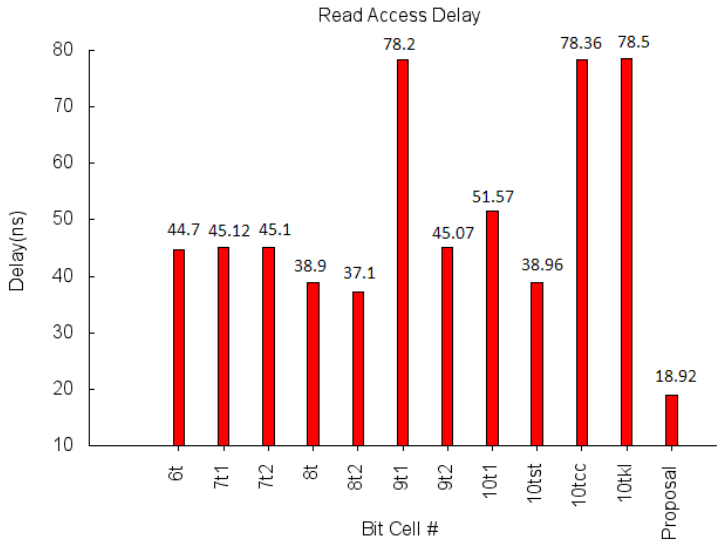

Figure 8.15 Read Access Delay of the bit cells

Considering the fact that 6T already incurs a huge penalty in the access time at subthreshold voltages, the large delay of these comparatively stable bit cells limits their usage to domains like wireless sensor networks, where energy and stability constrains are more important to meet than to achieve high frequency. However for performance driven domains, this increase in delay cannot be neglected.

Figures 8.16 and 8.17 show that our proposed bit cell allows for faster discharging of the bit lines than 6T bit cell. The timing diagrams in these figures are for a single bit cell. Comparison of the delay of the bit cells with our proposed bit cell is shown in figure 8.15.

The bitline BlB discharges because the node QB is storing '0' that turns on the pull-up transistor connecting the read wordline to the gate of the pull-down transistor in the discharge path. The bitline BL discharges because of the leakage current flowing through the pull-down transistor in the discharge path. The read portion of the timing diagram shows that the bitline BLB in our proposed bit cell discharges faster than the bit line BLB of 6T and of the other buffer-based bit cells. However, in 1Kbyte SRAM array, the BL bitline leakage increases in our proposed bitcell. This makes it difficult to get a differential voltage drop between the bitlines and the delay for our proposed bit cell in this array configuration is higher than the 6T. The timing diagrams of the 6T and the proposed bit cell in the array configuration are shown in figures 8.18 and 8.19. The variation in the read delay of the bit cells in array configuration is shown in figure 8.20.

Thus our proposal is limited by the number of bit cells that can be put in the single column, which is smaller than that of other buffer-based bit cells. Another limitation of our bit cell is the

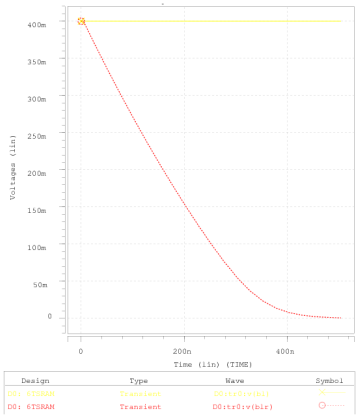

Figure 8.16 Bitline discharge delay for 6T bit cell.

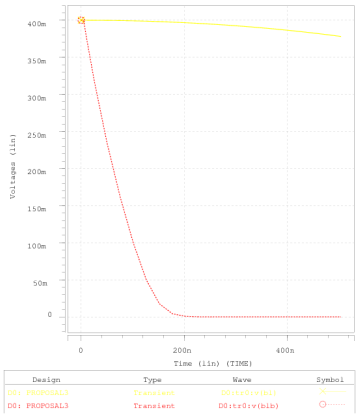

Figure 8.17 Bitline discharge delay for the proposed bit cell.

larger capacitive load on the read word line.

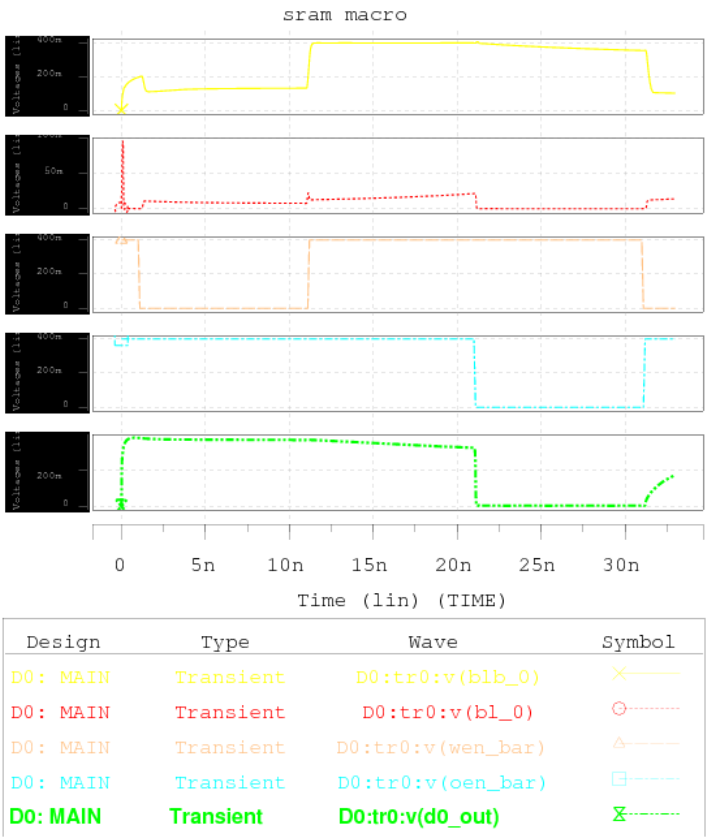

Figure 8.18 Timing diagram of 6T bit cell in 1Kbyte SRAM array. First '0' is written into the bit cell and then it is read.

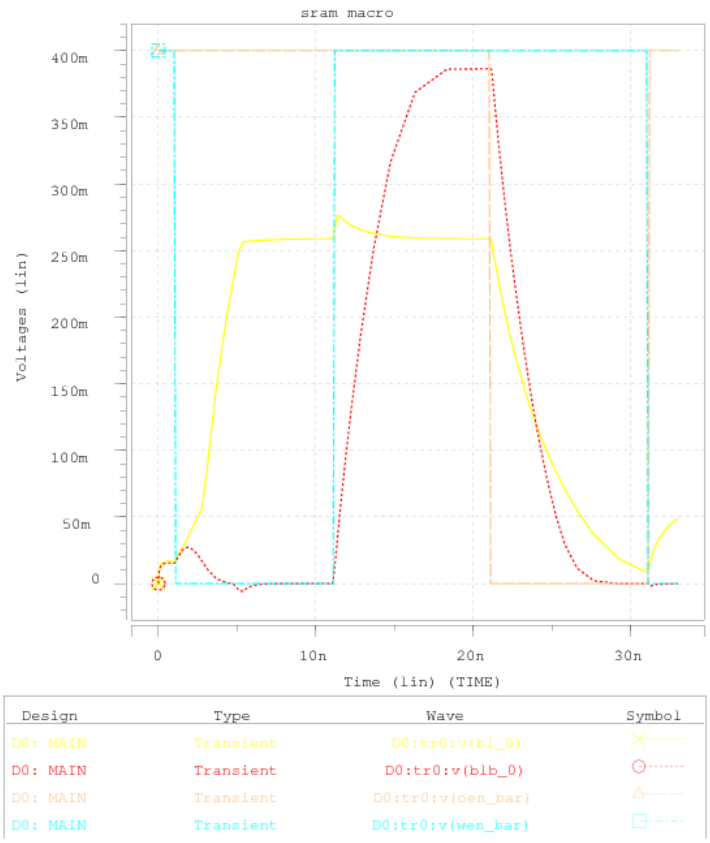

Figure 8.19 Timing diagram of the proposed bitcell in 1Kbyte SRAM array. First '0' is written into the bit cell and then it is read. Both the bitlines BL and BLB are discharging during read. This can result in read failure if the voltage difference between BL and BLB is very small during sense period.

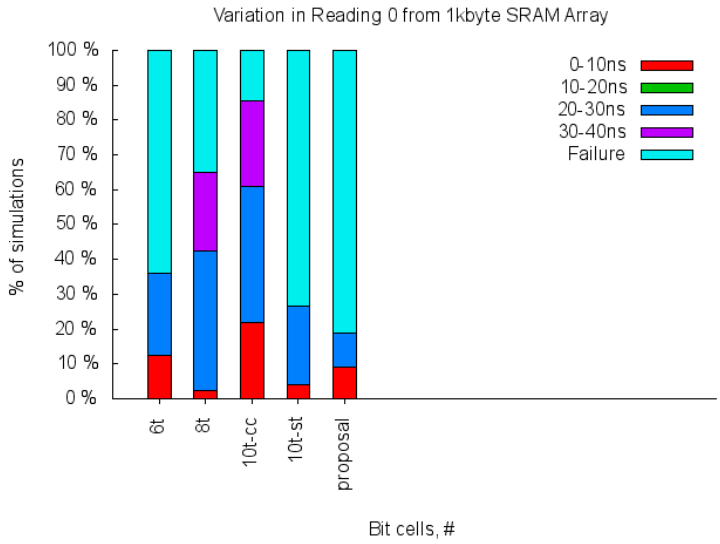

Figure 8.20 Comparison of the read delay for the bit cells in 1Kbyte SRAM array. The bit cell incurs more failures in read operation than other bitcells. This is caused by the discharging of bitline BL due to leakage. As a result, the voltage difference between BL and BLB is not enough for sense amplifier to read the correct value.

8.3 Energy Comparison

The comparison of the read and write access energy of our proposed bit cell with the 6T, schmitt and the buffer based bit cells is shown in the figure 8.21 and 8.22. This read energy is only the energy spent in reading from the storage nodes by switching the discharge path on and the energy spent in discharging the bitlines is not accounted in it metric. The energy per access for our bit cell is larger than the 6T bit cell due to the leakage through the BL bitline, which contributes to larger leakage energy. Since our write path is similar to the write path of the 6T bit cell, the write energy for the two are expected to be similar. However due to the due to larger leakage of the bitlines, the total write energy of our bit cells is larger than the 6T bitcell.

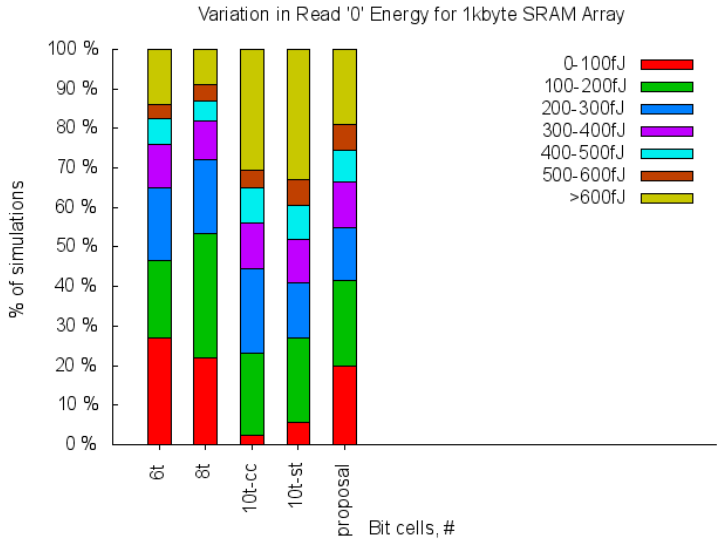

Figure 8.21 Read Energy variation for the bitcells in 1Kbyte array.

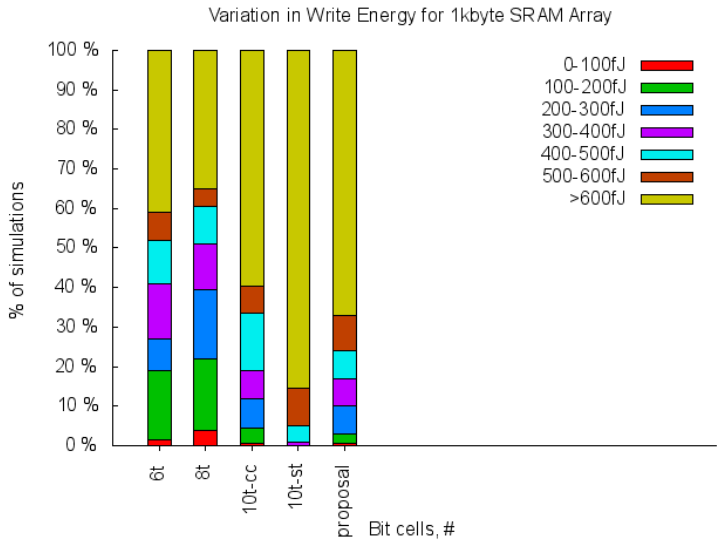

Figure 8.22 Write Energy variation for the bitcells in 1Kbyte array.

Chapter 9

Conclusions and Future work

We have proposed a new bit cell architecture in 65nm process technology for the subthreshold operation. This bit cell is able to discharge the bit lines faster than the other buffer based bit cells, thereby improving the read access time. Since it isolates the storage nodes from the bit lines, it achieves read SNM similar to the hold SNM of 6T. It's write operation is also similar to the write operation of the 6T. However the bit cell suffers from low I_{on}/I_{off} ratio and also high read wordline capacitance. In our future work, we will investigate current read/write assist technologies that reduce the bit line leakage and also reduce the impact of process variations. The conventional assist methods like Virtual Gnd and Body Biasing may not be the optimal methods as by reducing the leakage at one bit line, they will also reduce the discharge current in the read path at the other bit line, thereby increasing the read access time. Also the usefulness of Body Biasing decreases at ultra low voltages. A storage node value aware assist technology is required to reduce the bitline leakage .

Also the process technology used is now old and we would evaluate the bit cell in the newer 22nm technology process. In this and future process technologies, FinFETs may be better alternative to the bulk-CMOS devices for SRAM circuit, and so we will also investigate the stability and performance of the state-of-the-art subthreshold FinFET SRAM bitcells.

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