Escola Tècnica Superior d'Enginyeria Industrial de Barcelona

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Final Degree Project

Design, Fabrication and Verification of a Mixed-Signal XY Zone Monitoring Circuit and its Application to a Phase Lock Loop Circuit

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Resumen

El presente proyecto de final de carrera se centra en el diseño, análisis e implementación en silicio de una metodología de test/diagnosis basada en la comparación de firmas digitales generadas a partir de curvas de Lissajous. Se muestra su aplicación para testar la etapa de filtro de un circuito de bucle de enganche de fase (*phase lock loop*, PLL), así como los resultados experimentales de su implementación en tecnología CMOS de 65 nm.

La obtención de las firmas digitales se consigue mediante el uso de un circuito monitor, el cual, a partir de la composición de dos señales periódicas del circuito a analizar, genera, para cada punto de la curva de Lissajous, un valor digital. La utilización de varios monitores configurados de la manera adecuada permite una completa teselación del plano en diferentes zonas y por tanto, la generación de distintos códigos digitales (firma) a medida que la curva de Lissajous evoluciona en el tiempo.

El test del circuito y/o diagnosis del posible defecto se realiza mediante la comparación de la signatura *golden* o *sin defecto* y la signatura generada por el circuito testado. Para la comparación de firmas se emplea el concepto de distancia de Hamming entre códigos a modo de métrica de discrepancia. A partir de los valores precalculados de la métrica para cada posible valor del defecto se consigue realizar la diagnosis de este para el parámetro en estudio.

El trabajo se enmarca en el diseño de circuitos integrados de muy alta escala de integración usando una tecnología CMOS de actualidad (65 nm). Es por ello que se requieren técnicas de diseño analógico específicas, como lo son las estrategias centroidales para la elaboración de *layouts* o el correcto modelado de transistores nanométricos. Para esto último se hace uso del modelo Berkeley, el cual, debidamente ajustado a la tecnología empleada, proporciona aproximaciones muy aceptables y con relativa facilidad de uso.

Con el objetivo de verificar la metodología de test/diagnosis propuesta, se hace uso de una aplicación MATLAB que permite simular el comportamiento del circuito a testar en diferentes situaciones. Es posible excitar el circuito con distintas entradas, cambiar los parámetros de este, introducir defectos, o emplear distintos conjuntos de curvas para teselar el plano. La aplicación resulta fundamental para efectuar el proceso de diagnosis pues relaciona la cantidad de defecto con los valores de discrepancia obtenidos con la métrica definida.

Finalmente, se presentan los resultados experimentales obtenidos con el chip fabricado. Se constata el correcto comportamiento de este y la validez de la metodología de test/diagnosis propuesta.

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Foreword

Current final project is the result of almost two years of work on analog and mixed-signal test and design of VLSI circuits at *Departament d'Enginyeria Electrònica* (UPC). I started as an undergraduate grant student researching on the topic of analog comparators, actually, analizing a very simple sense amplifier structure which has become the digital stage of the proposed monitor circuit in this project. Gradually, with the aid of my advisor, I started to work in a deeper and more serious research together with professors.

From this work, three conference papers have been published and presented. Also, some of the performed research, shapes the pages of the current project. The research has not finished yet, since any step reveals a vast and amazing field to focus on and look into.

At the present, I am enrolled in the master program in Electronic Engineering (UPC) and continuing the research at *Departament d'Enginyeria Electrònica*. The outlines of current research concentrate on multi-parameter defects diagnosis and on-chip low power design techniques.

Álvaro Gómez Pau
June 2nd, 2010

Chapter 1

Introduction

1.1. Objectives and Scope

Current thesis is framed in the design and test of VLSI (very large scale of integration) circuits. The pursued objective is to develop a low cost and simple BIST (built-in self-test) technique that could be directly applied to analog and mixed-signals integrated circuits testing. The developed methodology is aimed to be used beyond test and apply it to defective circuit parameter diagnosis.

Project's starting point arises from a circuit studied by Ricard Sanahuja in his PhD thesis [1]. Sanahuja's circuit is a monitor circuit capable of composing two periodic signals and provide a differential output accordingly to a predefined monitor configuration. The presented testing method divides the plane into two zones using a straight line and checks whether the CUT remains in the specified zone or not. The differential output of the circuit should be transformed into a single ended digital signal.

The high end target of current project is, as said, to develop a reliable and low cost test/diagnosis methodology to be applied as a BIST technique. The objective is aimed to be achieved by analysing, designing and fabricating a CMOS version of the monitor circuit and use it to tesselate the XY plane into different zones. The composed signals generate a digital sequence (signature) which sould be compared to the free-defect one. This way, the study and definition of a suitable indicator of discrepancy between signatures is pursued too.

The nature of the project makes unavoidable the use of software tools (electrical or not) allowing the designer to check whether the proposed circuits/methodologies behave as expected or not. This drives to the importance of correct nanometric transistors models and accurate software simulation tools. A MATLAB application capable to emulate the tests/diagnosis methodology is also haunted.

The designed circuit is expected to be fabricated in a 65 nm CMOS technology and verified against a CUT with different levels of defects in order to show the final reliability of the proposed method on the fabricated chip.

1.2. Structure of the Project

The structure of project's memory has been organised accordingly to the chronological development of the project it describes. Several chapters recall specific and detailed information contained in the appendices. This way, the reader can go through the thesis in a straightforward way without delaying on demonstrations and detailed procedures.

Chapter 2 is devoted to transistor modeling. The classic quadratic Shichman-Hodges model is presented and discussed against current nanometric technologies for which it is not valid. The Unified MOSFET Model is introduced and fitted for ST-Microelectronics 65 nm transistors providing quite precise and manageable model for hand calculations.

In chapter 3, the monitor circuit that allows the composition of the Lissajous curves and generates the XY zonification is presented and analysed. Different analysis approaches are shown: overall operation, large signal, small signal,... Also, monitor's layout implementation is shown as well as the resulting switching curves from layout extraction simulations.

Chapter 4 presents the proposed metric definition in order to quantify signatures differences which allows the pass/fail test and parameter diagnosis (from the functional point of view). Also, its software implementation using a general purpose engineering oriented language like MATLAB is explained. The derived application capabilities are shown on a few examples of circuits with parameters out of tolerance ranges.

The test bench and circuit under test designs are detailed in chapter 5. Circuit design and layout of both PCBs are shown as well as a little theoretical approach to design of state

variable Biquad filters. Photographs of the obtained printed circuit boards are also displayed.

Chapter 6 is devoted to show the experimental results achieved once the monitor circuit has been fabricated and the developed methodology has been applied to a Biquad CUT (circuit under test). The results assert the reliability of the method and the correct monitor operaration as expected. The amount of defect of a CUT is succesfully diagnosed as the experimental results evidence.

Finally, in chapter 7 a recapitulation of the work is performed and some conclusions are drawn. Also, several future research paths are pointed out in order to improve the features of the presented circuits and methods.

In the appendices, different extra information can be found. This way, in appendices A and B the economic evaluation of the project and environmental impact assessment are described. In appendices C and D the theory behind the generalised leasts squares method is reviewed. Appendices E and F contain statistical related stuff. The former shows an evaluation of the number of simulations to be done when using Monte Carlo methods and the latter depicts the Anderson-Darling normality test method. In appendix G, the transfer function of the passive filter used by default on the PLL evaluation board is derived. Appendix H contains the code (mainly MATLAB) that has been used un the thesis. It also contains the datasheet of some used components.

Chapter 2

Transistor Modeling

Current integrated electronic technologies would not be as laboured as they are today without the aid of software tools. Advanced EDA (electronic design automation) computer programs aid electronic engineers to efficiently design, verify and fabricate high performace circuits, simulate them and make conclusions about what is the best technique or methodology to meet the project goals.

The use of EDA tools allow engineers to obtain accurate simulation results without the need of fabricating the circuit. They are even able to simulate process and temperature variations via technology statistical characterization and therefore give off results about system performance under several realistic scenarios.

Although all the benefits mentioned above, there are several things which can not be made by a computer. The hand of the electronic engineer must be present along the whole design process in order to assure quality. Many times, experience, intuition and the hability to successfully catch up simulation results are the best aptitudes to obtain a good design. This is why dealing with equations and performing hand made calculations is the proper way to cope with design specificacions.

In the field of integrated analog and mixed-signal electronics[1], the transistor is the most used device, so a model relating its electrical magnitudes is required to accomplish the design and analysis of any circuit. Of course, final calculations and design decisions will be

[1]The term *digital electronics* is just a level of abstraction, so do not exist itself, they are just well designed analog electronics.

made using simulated and experimental prototype results, but is extremely commendable to perform hand calculations in order to get the appropiate perspective of the overall bahaviour of the circuit.

2.1. The Shichman-Hodges Model

2.1.1. MOSFET Modeling Equations

In 1968 Shichman and Hodges proposed a large signal model for field effect transistors [2]. This model is considered as the classical MOSFET model. It delivers a great intuitive idea of what is happening inside the transistor and is extremely simple and usefull. Its derivation can be seen in [3, 4] as well as in the original article and almost in every textbook presenting analog electronic devices.

For an N-channel MOSFET transistor, the Shichman-Hodges model is,

$$\begin{aligned} I_{\mathrm{D}} &= 0, && V_{\mathrm{GS}} \leq V_{\mathrm{TH}} \\ I_{\mathrm{D}} &= k\frac{W}{L}\left((V_{\mathrm{GS}} - V_{\mathrm{TH}})V_{\mathrm{DS}} - \frac{V_{\mathrm{DS}}^2}{2}\right), && V_{\mathrm{GS}} > V_{\mathrm{TH}}, V_{\mathrm{DS}} < V_{\mathrm{GS}} - V_{\mathrm{TH}} \\ I_{\mathrm{D}} &= \frac{k}{2}\frac{W}{L}\left(V_{\mathrm{GS}} - V_{\mathrm{TH}}\right)^2, && V_{\mathrm{GS}} > V_{\mathrm{TH}}, V_{\mathrm{DS}} \geq V_{\mathrm{GS}} - V_{\mathrm{TH}} \end{aligned} \tag{2.1}$$

The three equations describe the behaviour of the device in the three possible working regions of the transistor: cut-off, ohmic (or linear) and saturation (or active). The magnitude I_{D} is the drain-source current, V_{TH} is the threshold voltage from which the transistor turns on and V_{GS} and V_{DS} are the voltages applied to gate and drain terminals. The quotient $\frac{W}{L}$ is the aspect ratio of the transistor (width/length) and the k parameter is the so called transistor process transconductance, $k = \mu C_{\mathrm{ox}}$. Many times, the product $k\frac{W}{L}$ is defined[2] as K, being simply called MOSFET transconductance. For a P-channel device the modeling equations are valid but inverting the side of the inequalities.

The classical MOSFET model is implemented in SPICE-like simulators under the name of SPICE Level 1 [5]. It means it is the most simple mathematical approach to the bahaviour

[2]Depending on the author, parameters k and K can be seen written as $\beta_{\square}$ and β respectively.

of MOSFET transistors. Of course, more accurate models are available involving dozens of parameters in order to precisely model the real behaviour. These models are usually provided by the technology manufacturer [6], including extensive documentation and PVT variations charaterization.

2.1.2. Schicman-Hodges Model for Hand Analysis

In order to show the usage of the Shicman-Hodges model, a simple NMOS inverter circuit will be analised (its transfer characteristic). Consider the active loaded inverter of Figure 2.1 with single supply of $V_{\mathrm{DD}} = 5\,\mathrm{V}$ and parameters of Table 2.1 for each device.

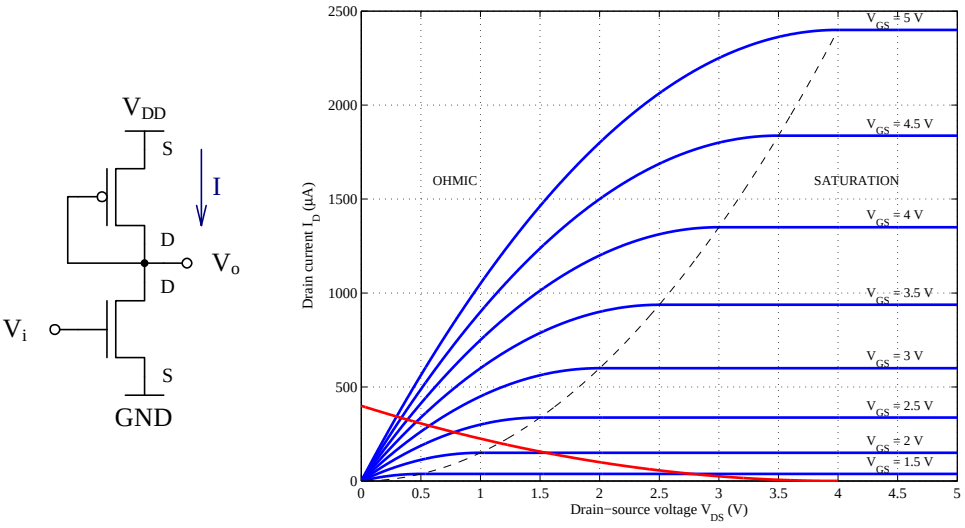


Figure 2.1: NMOS inverter schematic (left) and NMOS transistor DC characteristics with loading curve plotted (right).

The PMOS transistor has the drain and gate terminals shorted (diode configuration), so in inequality $V_{\mathrm{DS}} \leq V_{\mathrm{GS}} - V_{\mathrm{TH}}$ from equations (2.1) for a PMOS, the terms V_{DS} and V_{GS} cancell to yield $0 \leq -V_{\mathrm{TH}}$, that is $V_{\mathrm{TH}} \leq 0$, which allways states for a P-channel transistor. This way, the PMOS transistor works in saturation and acts as a current source. The delivered current is, therefore,

$$I = \frac{K_p}{2}(V_o - V_{\mathrm{DD}} - V_{\mathrm{TH}p})^2 \tag{2.2}$$

Depending on the working region of the NMOS transistor (which is function of its input

voltage V_i) and applying KCL at the output node, the input-output transfer curve can be computed and traced.

1. For $V_i \leq V_{\mathrm{TH}n}$, the driver transistor will be in cut-off, so $I = 0$, that is $\frac{K_p}{2}(V_o - V_{\mathrm{DD}} - V_{\mathrm{TH}p})^2 = 0$, from which $V_o = V_{\mathrm{DD}} + V_{\mathrm{TH}p}$ is obtained. Numerically, $V_o = 5 + (-1) = 4\,\mathrm{V}$.

2. For subsequent input voltages greater than $V_{\mathrm{TH}n}$, the NMOS transistor will work in saturation (we will check that later on seeing $V_o \geq V_i - V_{\mathrm{TH}n}$). The KCL equation is now, $\frac{K_p}{2}(V_o - (V_{\mathrm{DD}} + V_{\mathrm{TH}p}))^2 = I = \frac{K_n}{2}(V_i - V_{\mathrm{TH}n})^2$. Rooting this expression and solving for V_o yields,

$$V_o = V_{\mathrm{DD}} + V_{\mathrm{TH}p} - \sqrt{\frac{K_n}{K_p}}(V_i - V_{\mathrm{TH}n}) \tag{2.3}$$

   This equation is a straight line with a negative slope value of $\sqrt{\frac{K_n}{K_p}}$. In our case example, the equation is $V_o = 4 + \sqrt{6}(1 - V_i)$.

   The previous equation stands until the ohmic region is achieved. The boundary condition for this zone is $V_o = V_i - V_{\mathrm{TH}n}$, so $V_{\mathrm{DD}} + V_{\mathrm{TH}p} - \sqrt{\frac{K_n}{K_p}}(V_i - V_{\mathrm{TH}n}) = V_i - V_{\mathrm{TH}n}$, from which easily can be obtained the limit input voltage to keep the NMOS transistor working in saturation region,

$$V_{\mathrm{lim}} = V_{\mathrm{TH}n} + \frac{V_{\mathrm{DD}} + V_{\mathrm{TH}p}}{1 + \sqrt{\frac{K_n}{K_p}}} \tag{2.4}$$

   The limit input voltage for the example we are studying is $V_{\mathrm{lim}} = 2.15\,\mathrm{V}$. Check Figure 2.2 for details on the transfer characteristic.

3. For input voltages greater than V_{lim}, the driver transistor achieves ohmic region, so accordingly to Schicman-Hodges model the following equality states,

$$\frac{K_p}{2}(V_o - V_{\mathrm{DD}} - V_{\mathrm{TH}p})^2 = K_n\left((V_i - V_{\mathrm{TH}n})V_o - \frac{V_o^2}{2}\right) \tag{2.5}$$

   Which is a second order polynomial equation that can rearrenged as follows,

$$\left[1 + \frac{K_n}{K_p}\right]V_o^2 + \left[-2\left((V_{\mathrm{DD}} - V_{\mathrm{TH}p}) + \frac{K_n}{K_p}(V_i - V_{\mathrm{TH}n})\right)\right]V_o + \left[(V_{\mathrm{DD}} - V_{\mathrm{TH}p})^2\right] = 0 \tag{2.6}$$

Its solution is computed via the well known quadratic formula. The resulting expression is of the form $A + B\sqrt{CV_i}$, where A, B and C are constant values. Check Figure 2.2 to see the resulting rational function on the ohmic region of operation.

	$k\ \left(\frac{\mu A}{V^2}\right)$	$\frac{W}{L}$	$K\ \left(\frac{\mu A}{V^2}\right)$	V_{TH} (V)
PMOS	50	1	50	-1
NMOS	100	3	300	1

Table 2.1: MOSFET parameters for Figure 2.1 NMOS inverter.

In order to compare the Schicman-Hodges model and the performed analysis with real-life transistors, a simulation of the circuit in Figure 2.1 has been made. It has been achieved using HSPICE simulator with an ST-Microelectronics 65 nm technology.

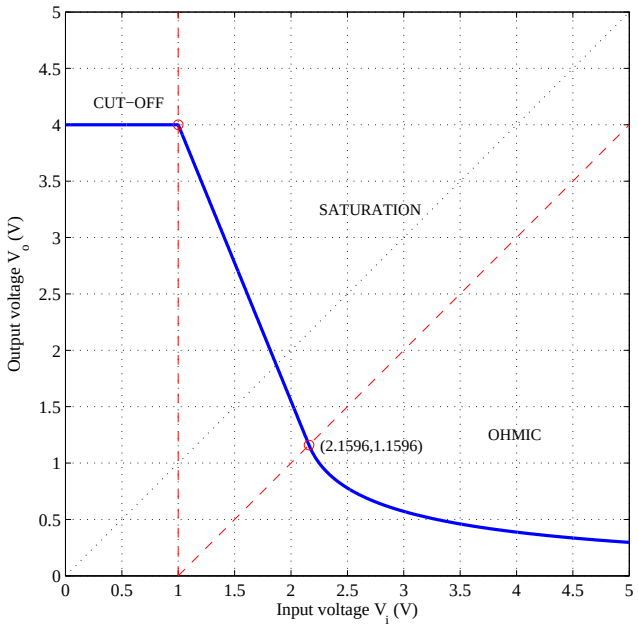


Figure 2.2: NMOS inverter transfer function determined via hand calculations and the Schicman-Hodges large signal MOSFET model.

As can be seen in Figure 2.2 and Figure 2.3, the two transfer characteristics highly differ. This fact strengths the need of obtaining a new model to be applied in hand calculations.

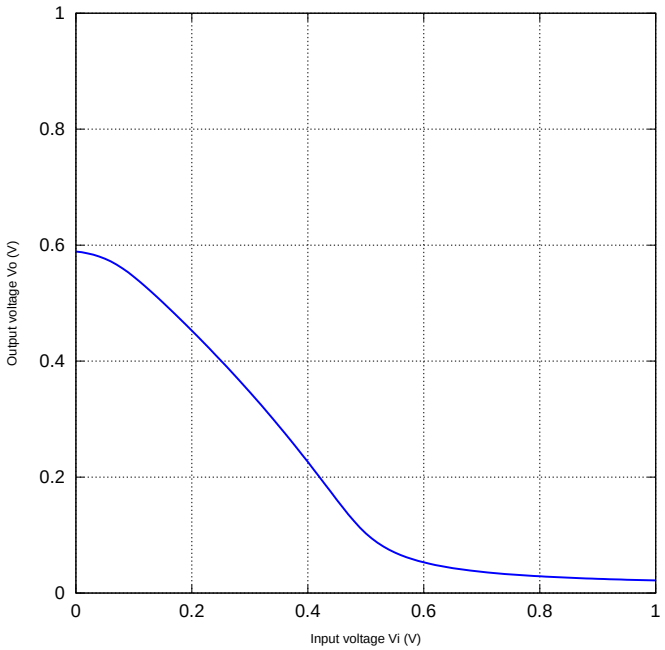


Figure 2.3: NMOS inverter simulated transfer function using ST 65 nm technology. For this technology, V_{DD} voltage is 1 V. The aspect ratio of the transistors have been kept identical to those considered in hand analysis.

2.2. The Unified MOSFET Model

Despite of its simplicity, the Shichman-Hodges Model does not match current transistors characteristic curves. This is due to second order effects, like velocity saturation or channel length modulation effects. For this reason, the following Berkeley model [7] is proposed and fitted using the generalised leasts squares method presented in appendix D.

Berkeley model equations are:

$$\begin{aligned} I_{\mathrm{D}} &= 0 && V_{\mathrm{GS}} \leq V_{\mathrm{TH}} \\ I_{\mathrm{D}} &= k\frac{W}{L}\left((V_{\mathrm{GS}} - V_{\mathrm{TH}})V_{\mathrm{min}} - \frac{{V_{\mathrm{min}}}^2}{2}\right)(1 + \lambda V_{\mathrm{DS}}) && V_{\mathrm{GS}} > V_{\mathrm{TH}} \end{aligned} \tag{2.7}$$

2.2.1. MOSFET Modeling Equations

As seen, Schichman-Hodges model is not suitable for modeling small transistors such as ST-65nm because it does not take in consideration second order effects like the channel length modulation or velocity saturation. Instead, the unified MOS model will be used. Accordingly to it, the drain current can be expressed as follows,

$$i_{\mathrm{d}} = k\frac{W}{L}\left(V_{\mathrm{gt}}V_{\mathrm{min}} - \frac{V_{\mathrm{min}}^2}{2}\right)(1+\lambda V_{\mathrm{ds}})$$

Where $V_{\mathrm{min}} = \min\{V_{\mathrm{gt}}, V_{\mathrm{ds}}, V_{\mathrm{dsat}}\}$ and $V_{\mathrm{gt}} = V_{\mathrm{gs}} - V_{\mathrm{TH}}$. The min function should be turned into a max function if a PMOS transitor is beeing modeled. The working region depends on the value of V_{min} as shown in the following table (for NMOS),

Region	V_{min}	Expanded model for i_{d}
Cut-off	$(V_{\mathrm{gs}} < V_{\mathrm{TH}})$	0
Linear	V_{ds}	$k\frac{W}{L}\left((V_{\mathrm{gs}} - V_{\mathrm{TH}})V_{\mathrm{ds}} - \frac{V_{\mathrm{ds}}^2}{2}\right)(1+\lambda V_{\mathrm{ds}})$
Vel. Sat.	V_{dsat}	$k\frac{W}{L}\left((V_{\mathrm{gs}} - V_{\mathrm{TH}})V_{\mathrm{dsat}} - \frac{V_{\mathrm{dsat}}^2}{2}\right)(1+\lambda V_{\mathrm{ds}})$
Sat.	V_{gt}	$\frac{k}{2}\frac{W}{L}(V_{\mathrm{gs}} - V_{\mathrm{TH}})^2(1+\lambda V_{\mathrm{ds}})$

2.2.2. Model Fitting to CMOS 65 nm

As can be seen, the unified MOS model depends on four parameters which have to be properly calibrated to approach the simulated curves (Spectre),

$$i_{\mathrm{d}} = f(V_{\mathrm{TH}}, k, V_{\mathrm{dsat}}, \lambda)$$

The direct analytical application of the leasts squares method is not suitable because of the nonderivability of the drain current function and the nonlinearity relations among the unknown parameters. It will be easier to find relations between the calibration parameters and then adjust de model empiricaly. These two criterion will be used:

CRITERION 1: The separation of curves $i_{\mathrm{d}} = f(|V_{\mathrm{ds}}| = V_{\mathrm{DD}})$ at velocity saturation region must be constant since they grow linearly.

CRITERION 2: The maximum current for $|V_{\mathrm{ds}}| = |V_{\mathrm{gs}}| = V_{\mathrm{DD}}$ will be fixed and equaled to the obtained simulation current.

Note that the criterions have been taken in the velocity saturation region because it is the most important and is usually assumed to be the working region for hand analysis.

The first criterion stands,

$$\begin{aligned} i_{\mathrm{d1}} &= k\frac{W}{L}\left((V_{\mathrm{gs}_1} - V_{\mathrm{TH}})V_{\mathrm{dsat}} - \frac{V_{\mathrm{dsat}}^2}{2}\right)(1 + \lambda V_{\mathrm{ds}}) \\ i_{\mathrm{d2}} &= k\frac{W}{L}\left((V_{\mathrm{gs}_2} - V_{\mathrm{TH}})V_{\mathrm{dsat}} - \frac{V_{\mathrm{dsat}}^2}{2}\right)(1 + \lambda V_{\mathrm{ds}}) \end{aligned}$$

Just for convenience let define $S = i_{\mathrm{d2}} - i_{\mathrm{d1}}$, so their difference stablishes,

$$S = k\frac{W}{L}V_{\mathrm{dsat}}(V_{\mathrm{gs}_2} - V_{\mathrm{gs}_1})(1 + \lambda V_{\mathrm{ds}})$$

From which V_{dsat} can be easily computed,

$$V_{\mathrm{dsat}} = \frac{S}{k\frac{W}{L}(V_{\mathrm{gs}_2} - V_{\mathrm{gs}_1})(1 + \lambda V_{\mathrm{ds}})}$$

The second criterion stands that,

$$i_{\mathrm{dMAX}} = k\frac{W}{L}\left((V_{\mathrm{gs}} - V_{\mathrm{TH}})V_{\mathrm{dsat}} - \frac{V_{\mathrm{dsat}}^2}{2}\right)(1 + \lambda V_{\mathrm{ds}})$$

where i_{dMAX} will be defined as M. This way, λ parameter is written as,

$$\lambda = \frac{1}{V_{\mathrm{ds}}} \left\{ \frac{M}{k\frac{W}{L}\left((V_{\mathrm{gs}} - V_{\mathrm{TH}})V_{\mathrm{dsat}} - \frac{V_{\mathrm{dsat}}^2}{2}\right)} - 1 \right\}$$

substituting V_{dsat} by the value finded previously and after a bit of algebra, the λ parameter yields,

$$\lambda = \frac{1}{V_{\mathrm{ds}}} \left\{ \frac{S^2}{2k\frac{W}{L}(V_{\mathrm{gs}_2} - V_{\mathrm{gs}_1})^2} \left(\frac{S(V_{\mathrm{gs}} - V_{\mathrm{TH}})}{V_{\mathrm{gs}_2} - V_{\mathrm{gs}_1}} - M \right)^{-1} - 1 \right\}$$

The calibration algorithm is listed below,

1. Compute from the simulated data the separation current at velocity saturation region and $|V_{\mathrm{ds}}| = V_{\mathrm{DD}}$, S and the maximum current given by the mosfet, M, when $|V_{\mathrm{gs}}| = |V_{\mathrm{ds}}| = V_{\mathrm{DD}}$ ($V_{\mathrm{DD}} = 1\,\mathrm{V}$ in this technology).

2. Plot $i_{\mathrm{d}} = f(V_{\mathrm{gs}})$ in order to estimate the threshold voltage V_{TH}. This can be done by polynomial adjustment as well.

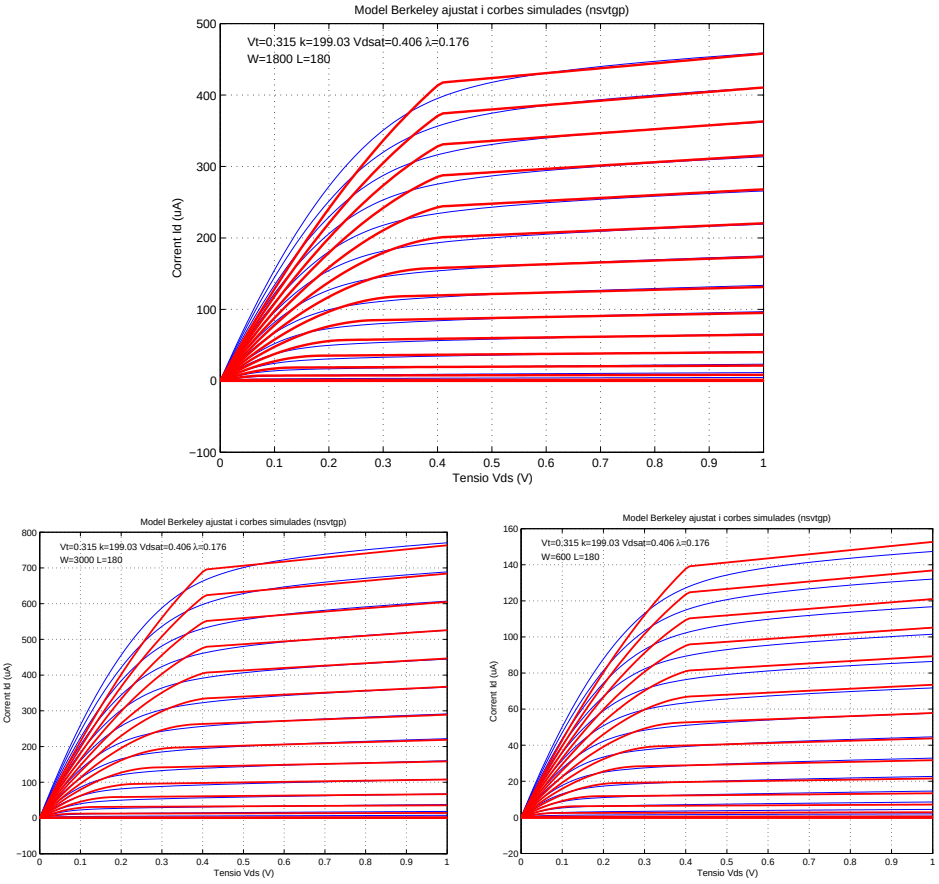
3. Define the value of the k parameter randomly so it will be adjusted empiricaly.

4. Compute the λ parameter using the derived expression.

5. Compute the V_{dsat} parameter using the derived expression.

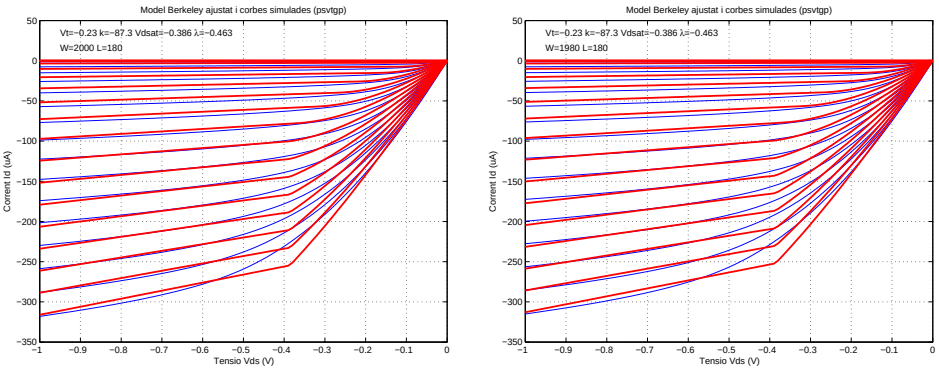
6. Adjust the k parameter to meet the minimum error between the model and the simulated data.

After the process of calibration depicted above, and the proper application of the generalisex leasts squares fitting method (with a good initial guess), the following adjusted curves are achieved for NMOS,



Where the first plot is the one that has been used to calibrate de model and the other two show the model adjusted to transistors with different aspect ratios.

The curves for PMOS transistors are,



As can be seen, in all the cases, a good current adjustment is achieved. The model is

suitable to be used in any hand analysis calculation, thus its simplicity and easy of use. Of course, the model does not present an outstanding precision[3], but delivers a quite reasonable and intuitive values.

[3]Simulation results have to be used for that.

Chapter 3

Proposed Monitor Circuit

In this chapter, the monitor circuit used for the XY zone monitoring method is presented and analysed. The results shown are obtained from hand calculation analysis and layout software simulations. The monitor circuit is formed of two circuits:

1. The circuit which composes the two signals intended to be used for testing. Here after will be called the first stage or input stage circuit.

2. The circuit of a high gain output stage analog comparator. Here after will be called as the second stage or output stage.

The firsts studies, designs and analysis of the input stage circuit were presented by Ricard Sanahuja in [1].

3.1. The XY Zoning Method

The XY zoning method is based on the composition of two relevant signals of the circuit, $x(t)$ and $y(t)$ in the same way an oscilloscope represents the trace configured in XY mode. For many simple circuits, the most suitable signals to compose are the input excitation and the output response of the CUT.

If the input signal $x(t)$ is formed by a finite spectrum of frequencies assuring rational reations among them and the signal is applied to a linear circuit, the input and response of the CUT, and therefore the composition, will be periodic. In such case, the resulting trace is called a Lissajous composition.

Of course, if the Lissajous compisition depends on the output of the CUT, a varied curve will be obtained if the circuit being tested is not operating inside the tolerance ranges. The discrepance of the golden and observed Lissajous curve is the fact that will allow to design a test and diagnosis method using such concepts.

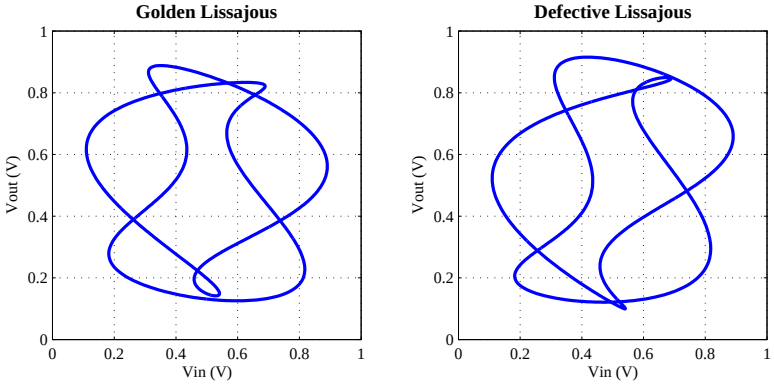


Figure 3.1: Golden and defective Lissajous.

In Figure 3.1 can be seen the response of a Biquad filter to a multitone input. On the left, the golden Lissajous is plotted. On the right, the characteristic filter frequency has been shifted 10% yielding therefore a slighly different Lissajous.

The main objective of the XY Zoning method is to test whether a circuit is ok or not by the comparison of a sequence of digital signatures generated by Lissajous composition analysis. In fact, the observed and defective Lissajous curves can be considered as the analog signature of the CUT, but these signature's comparison is hard to be accomplished in the analog world, so a digitalization of the information of each trace is required.

The dititalization of curve data is done by tesselating the XY plane in different regions and assigning a code to each zone. This way, the test procedure can be made just by checking whether the observed sequence of signatures are equal to those expected for a golden CUT or not. Figure 3.2 shows a possible tesselation of the XY plane using straight lines. Each line is a comparator that delivers a digital zero for one half of the plane and a digital one for the other half side.

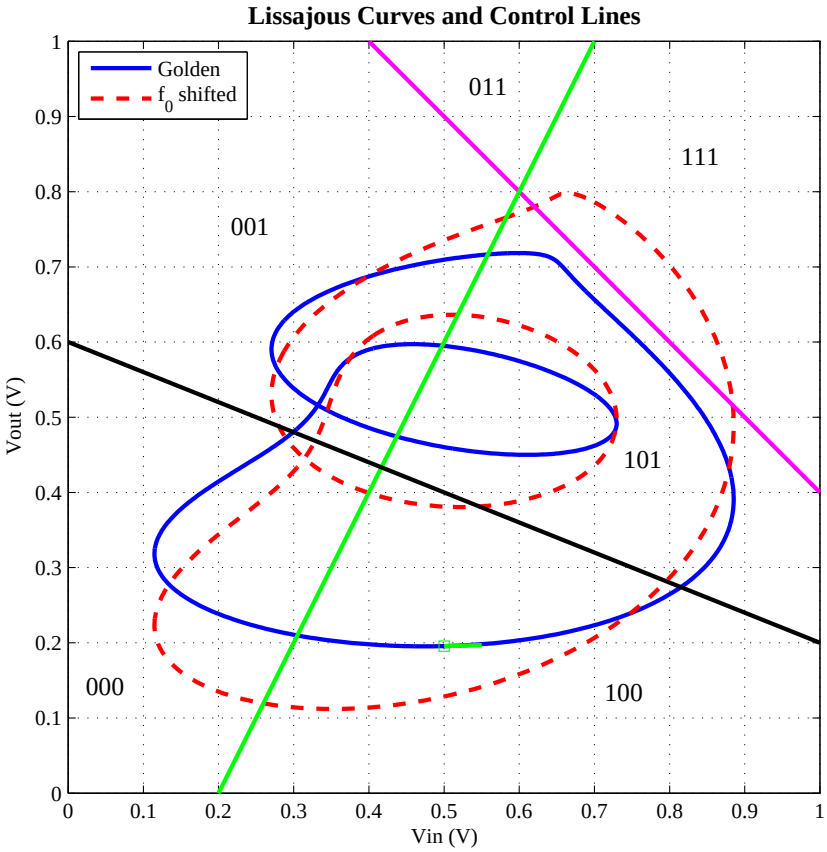


Figure 3.2: Lissajous curves and straight switching curves.

The chosen codification criteria has been the green control line for the MSB bit, then the magenta, and then the black line for the LSB bit. In this case, the golden sequence signature is,

$$G = \{100, 101, 001, 101, 001, 000\} \tag{3.1}$$

and for the observed Lissajous which comes from a defective Biquad filter is,

$$O = \{100, 101, 111, 101, 001, 000, 100, 101, 001, 000\} \tag{3.2}$$

As can be checked, the signatures are very different (even in length), so the method yields a simple and reliable way to discriminate circuits which are out of tolerances ranges.

A great amount of catastrophic defects can be detected just by checking the golden and defective sequences.

3.2. Circuit Analysis

In this section, the proposed monitor circuit is presented and analysed. Mainly, the objective is to show how does the circuit behaves in large signal conditions and explain an overview of its operation.

3.2.1. Input Stage

The previously explained XY zone monitoring method requires a simple and configurable nonlinear comparator to compose the pair of signals and provide a digital output. The first stage monitor circuit can be shown in Figure 3.3 [1, 8]. It follows the structure of a CMOS pseudo-differential comparator whose driver transistors have been split into two in order to obtain multiple inputs. The structure can be generalized as needed by adding more transistors in parallel. The active loading with positive feedback helps to improve the gain[1] of the comparator.

The operation of the first stage of the monitor circuit of Figure 3.3 is easy. Two of the four voltages are used as the inputs $x(t)$ and $y(t)$ of the Lissajous trace ($x(t)$ signal is, in general, a multitone function and $y(t)$ is the transient response of the CUT to the input excitation) and the other two voltages are set to a DC voltage level in order to change the shape and parameters of the switching curve. The usage of several monitors with different setup allows a suitable tesselation of the plane for the expected traces.

The active PMOS loading of the monitor input stage is absolutely symmetrical, so in order to simplify the analysis, pure resistive loading will be considered as shown in Figure 3.4. As the circuit being analysed is a comparator, the desired analysis will be performed arround the commutation point. As said, the active loading is symmetrical, son the commutation point (when the differential outputs crosses in the large signal analysis) takes place when

[1]The structure allows to add hysteresis to the comparator but in this application is not suitable thus has been disabled by adequately sizing the feedback transistors aspect ratio.

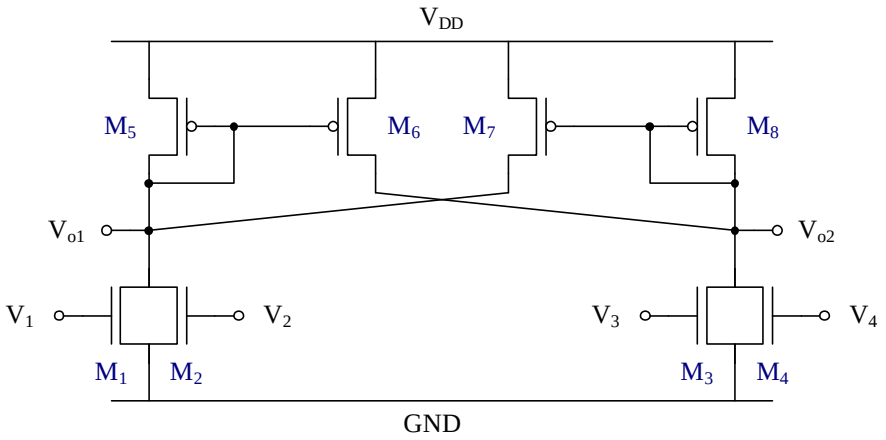


Figure 3.3: First stage model.

output nodes voltages are equal, or what is the same, when the left and right currents in both branches are the same value.

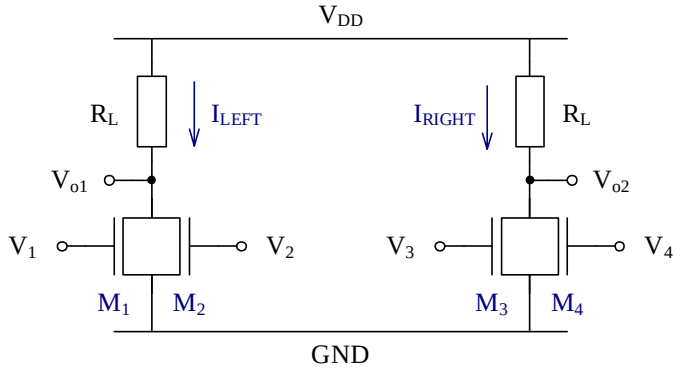


Figure 3.4: First stage resistive loading model.

Using the Unified MOSFET model in saturation (not velocity saturation) region and applying KCL at the output nodes, the following equation state,

$$k\frac{W_1}{L_1}(V_1 - V_{\mathrm{TH}})^2(1+\lambda V_{o1}) + k\frac{W_2}{L_2}(V_2 - V_{\mathrm{TH}})^2(1+\lambda V_{o1}) = k\frac{W_3}{L_3}(V_3 - V_{\mathrm{TH}})^2(1+\lambda V_{o2}) + k\frac{W_4}{L_4}(V_4 - V_{\mathrm{TH}})^2(1+\lambda V_{o2}) \quad (3.3)$$

And because of the fact the analysis is being done at the commutation point, $V_{o1} = V_{o2}$, so the term $1+\lambda V_{\mathrm{DS}}$ cancells out in both hand sides, as well as the process transconductance,

which can be constant for the same transistors. Just for convenience, the aspect ratio of the transistors will be indicated as $S_i = \frac{W_i}{L_i}$. Therefore, the resulting equation is,

$$S_1(V_1 - V_{\mathrm{TH}})^2 + S_2(V_2 - V_{\mathrm{TH}})^2 = S_3(V_3 - V_{\mathrm{TH}})^2 + S_4(V_4 - V_{\mathrm{TH}})^2 \tag{3.4}$$

As stated, both of the V_i, $k = 1, \ldots, 4$, voltages will be acting as the $x(y)$ and $y(t)$ variables, so is evident that the resulting curves will be quite different whether the signals x and y are applied to the same side of the monitor or not. Each case will be discussed in the following two subsections.

For both situations, note that the stated equation is not valid for $x, y < V_{\mathrm{TH}}$, because in subthreshold the transistor does not deliver current to the addition. The behaviour in such region is a straight line parallel to the axis whose variable makes the NMOS transistor operates in subthreshold.

Inputs at the Same Side

Suppose the input signals are applied at the same side of the monitor as $V_1 = x$ and $V_2 = y$, and voltages V_3 and V_4 are set to a DC voltage level, then,

$$S_1(x - V_{\mathrm{TH}})^2 + S_2(y - V_{\mathrm{TH}})^2 = \underbrace{S_3(V_3 - V_{\mathrm{TH}})^2 + S_4(V_4 - V_{\mathrm{TH}})^2}_{\alpha} \tag{3.5}$$

The right hand side term has been recalled as a constant α just for convenience. This way, dividing by α (which can not be zero as is the sum of positive and nonzero quantities) the whole equation yields,

$$\frac{(x - V_{\mathrm{TH}})^2}{\frac{\alpha}{S_1}} + \frac{(y - V_{\mathrm{TH}})^2}{\frac{\alpha}{S_2}} = 1 \tag{3.6}$$

just the equation of an ellipse centered at $(V_{\mathrm{TH}}, V_{\mathrm{TH}}) \in \mathbb{R}^2$ and with semi axis lengths $a = \sqrt{\frac{\alpha}{S_1}}$ and $b = \sqrt{\frac{\alpha}{S_2}}$. In Figure 3.5 can be shown different ellipses generated with different transistors aspect ratios and DC voltages.

Ellipse	S_1	S_2	S_3	S_4	V_3 (V)	V_4 (V)
Red	1	1	1	1	0.5	0.6
Blue	2	4	1	2	0.7	0.9
Green	1	5	1	1	0.6	0.9

Table 3.1: Ellipses parameters for curves in Figure 3.5. V_1 and V_2 are the $x(t)$ and $y(t)$ variables.

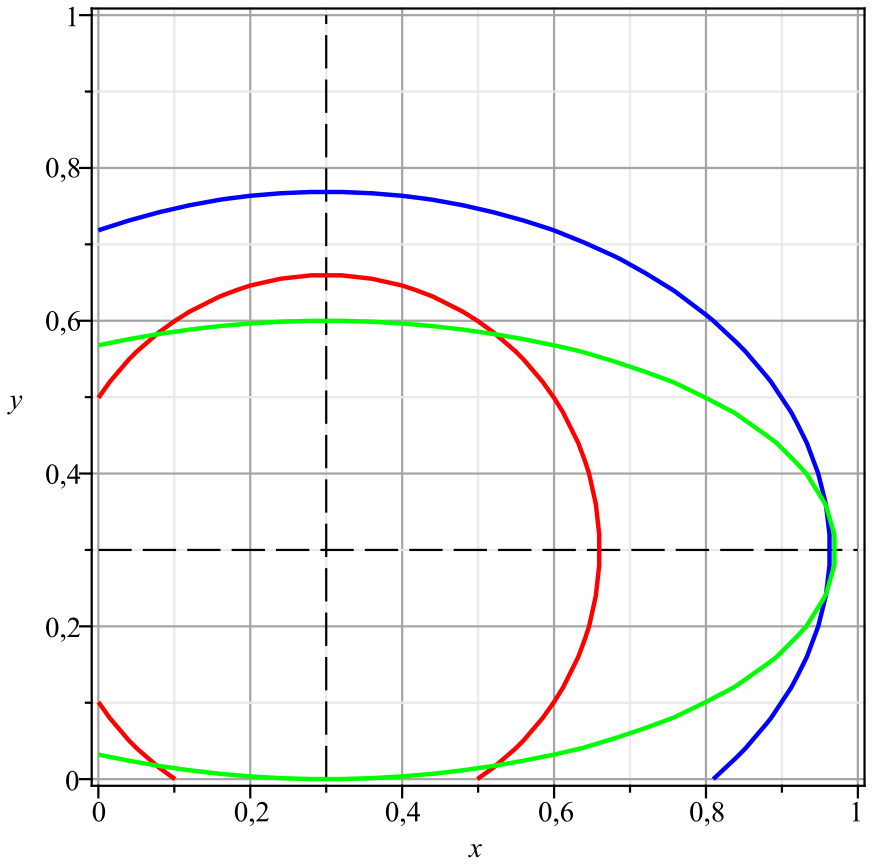


Figure 3.5: Different ellipses with parameters of Table 3.1.

Inputs at Different Sides

Suppose now the input signals are connected to $V_1 = x$ and $V_4 = y$ which lay at different sides of the monitor input stage circuit. This fact forces some minor changes to the KCL equation as follows,

$$S_1(x - V_{\mathrm{TH}})^2 - S_4(y - V_{\mathrm{TH}})^2 = \underbrace{S_3(V_3 - V_{\mathrm{TH}})^2 - S_2(V_2 - V_{\mathrm{TH}})^2}_{\alpha} \tag{3.7}$$

Again, the constant term of the right hand side has been recalled as α, but now α is written as a difference and therefore can be positive or negative. Under the assumption of being positive, the equation can be written as,

$$\frac{(x - V_{\mathrm{TH}})^2}{\frac{\alpha}{S_1}} - \frac{(y - V_{\mathrm{TH}})^2}{\frac{\alpha}{S_4}} = 1 \tag{3.8}$$

Which is the normalized equation of a hyperbola centered in $(V_{\mathrm{TH}}, V_{\mathrm{TH}}) \in \mathbb{R}^2$ with parameters $a = \sqrt{\frac{\alpha}{S_1}}$ and $b = \sqrt{\frac{\alpha}{S_4}}$. Note that due to the sign of α, the equation can yield different parametrizations ($t \geq 0$),

$$\left.\begin{aligned} x &= V_{\mathrm{TH}} + a\cosh t \\ y &= V_{\mathrm{TH}} + b\sinh t \end{aligned}\right\} \quad \text{or} \quad \left.\begin{aligned} x &= V_{\mathrm{TH}} + a\sinh t \\ y &= V_{\mathrm{TH}} + b\cosh t \end{aligned}\right\} \tag{3.9}$$

which are symmetrical having as symmetry axis the identity function $y = x$. Similarly as shown for same side inputs, several hyperbolas are plotted in Figure 3.6 with parameters in Table 3.2.

Hyperbola	S_1	S_2	S_3	S_4	V_2 (V)	V_3 (V)
Red	1	1	1	1	0.5	0.6
Blue	2	4	1	2	0.7	0.9
Green	1	5	1	3	0.6	0.9
Black	1	1	1	1	0.5	0.5

Table 3.2: Hyperbolas parameters for curves in Figure 3.6. V_1 and V_4 are the $x(t)$ and $y(t)$ variables.

Special attention requires the degenerated black hyperbola. Note that due to the absolutely equilibrated monitor (equal aspect ratios and voltages of the transistors connected to DC levels), the resulting equation yields to,

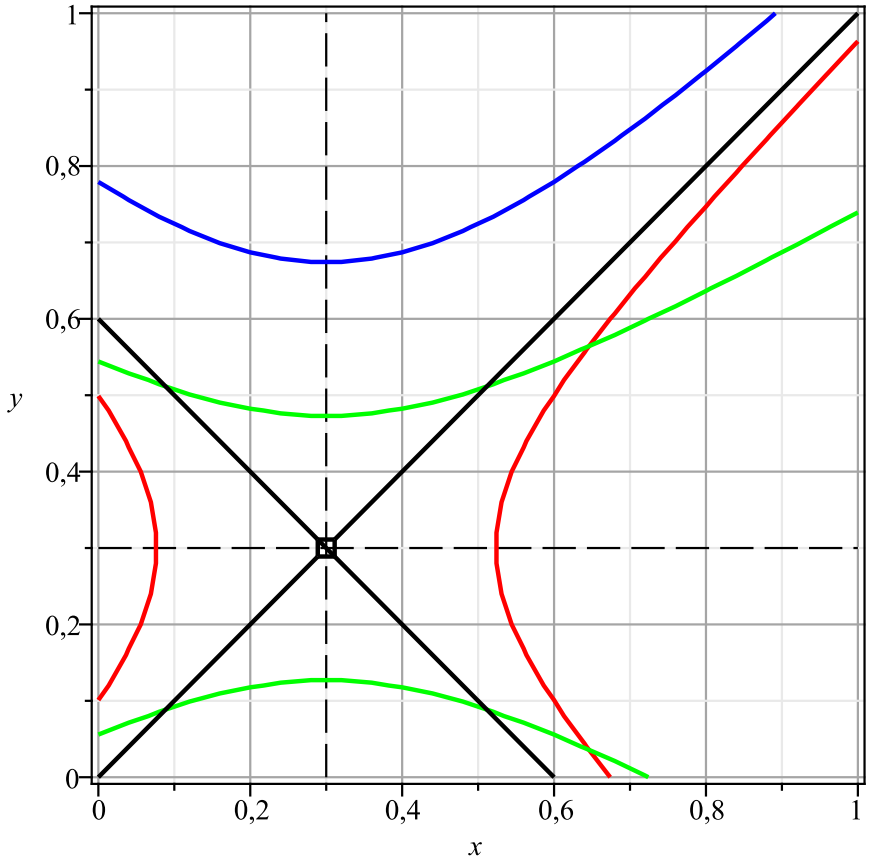


Figure 3.6: Different hyperbolas.

$$S_1(x - V_{\mathrm{TH}})^2 - S_4(y - V_{\mathrm{TH}})^2 = 0 \tag{3.10}$$

Rooting the equation, one finds the well known degenerated crossing straight lines centered at $(V_{\mathrm{TH}}, V_{\mathrm{TH}}) \in \mathbb{R}^2$,

$$y = V_{\mathrm{TH}} \pm \sqrt{\frac{S_1}{S_4}}(x - V_{\mathrm{TH}}) \tag{3.11}$$

3.2.2. Output Stage

The output stage of the monitor circuit is a plain comparator stage in order to dititalize the diferential output from the first stage [8,9]. Second stage comparator is formed by a three

CMOS comparator structure as can be checked in Figure 3.7. Each of these stages is described by the schematic in Figure 3.8.

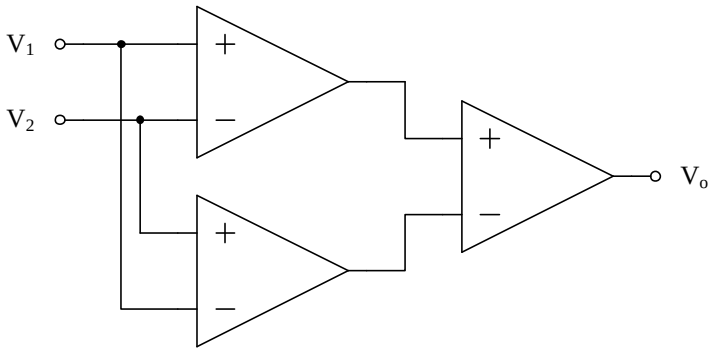


Figure 3.7: Second stage.

The aim of this structure is to increase the gain and therefore improve the digital output to be interpreted by the pad circuitry. The comparator is pretty simple to analyse due to the usage of a NMOS inverter in the left branch and the current mirror formed by M3 and M4 in order to equilibrate the branches.

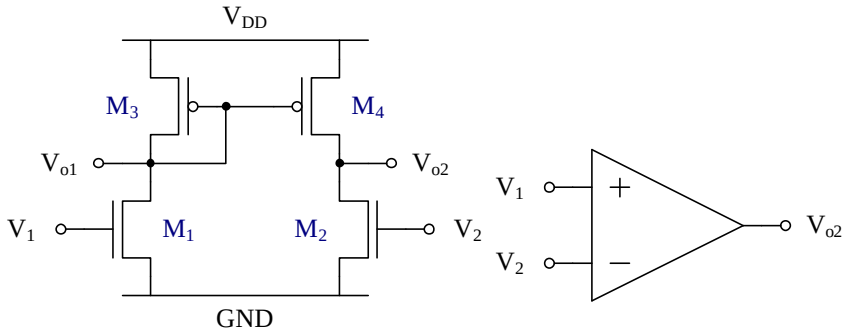


Figure 3.8: Second stage.

3.3. The small signal model general theory

If a transistor is supposed to work in the surroundings of a fixed point (the quiscent point or simply the Q-point, also the biasing point) a linear aproximation can be taken as a good approach to the current function. That is, the first order Taylor polynomial for $I_{\mathrm{d}} = f(V_{\mathrm{gs}}, V_{\mathrm{ds}})$ at $Q = (V_{\mathrm{GS}}, V_{\mathrm{DS}})$,

$$I_d = I_D + \left(\begin{array}{cc} \frac{\partial I_d}{\partial V_{\rm gs}} & \frac{\partial I_d}{\partial V_{\rm ds}} \end{array} \right)\Big|_Q \left(\begin{array}{c} v_{\rm gs} \\ \\ v_{\rm ds} \end{array} \right)$$

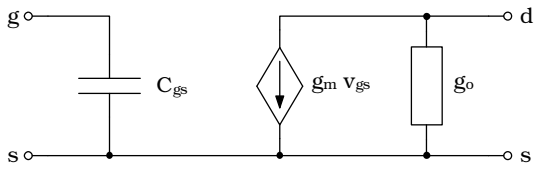
So the small signal amount of current is,

$$i_d = \frac{\partial I_d}{\partial V_{\rm gs}} \cdot v_{\rm gs} + \frac{\partial I_d}{\partial V_{\rm ds}} \cdot v_{\rm ds}$$

And defining, as usual, $g_m = \frac{\partial I_d}{\partial V_{\rm gs}}$ and $g_o = \frac{\partial I_d}{\partial V_{\rm ds}}$, the small signal current can be rewritten as,

$$i_d = g_m v_{\rm gs} + g_o v_{\rm ds}$$

Accordingly to the previous calculations the folowing circuit is achieved,



3.3.1. The small signal model applied to the first stage

In order to get a delay model of the circuit being studied, a small signal analysis will be performed. The model that will be used is the previously presented. Capacitance loading will be also considered to model the gate capacitance of the next stage.

Using the usual notation and refering to circuit components of presented first stage circuit, the nodal analysis yields the following system of equations,

$$\begin{bmatrix} g_{o1}+g_{o2}+g_{o5}+g_{o7}+s(C_{gs5}+C_{gs6}+C_{L1}) & 0 \\ 0 & g_{o3}+g_{o4}+g_{o8}+g_{o6}+s(C_{gs7}+C_{gs8}+C_{L2}) \end{bmatrix} \begin{bmatrix} V_{o1} \\ V_{o2} \end{bmatrix} = \begin{bmatrix} -g_{m1}V_1-g_{m2}V_2-g_{m5}V_{o1}-g_{m7}V_{o2} \\ -g_{m3}V_3-g_{m4}V_4-g_{m6}V_{o1}-g_{m8}V_{o2} \end{bmatrix} \quad (3.12)$$

Or what is the same,

$$\begin{bmatrix} g_{o1}+g_{o2}+g_{o5}+g_{o7}+g_{m5}+s(C_{gs5}+C_{gs6}+C_{L1}) & g_{m7} \\ g_{m6} & g_{o3}+g_{o4}+g_{o8}+g_{o6}+g_{m8}+s(C_{gs7}+C_{gs8}+C_{L2}) \end{bmatrix} \begin{bmatrix} V_{o1} \\ V_{o2} \end{bmatrix} = \begin{bmatrix} -g_{m1}V_1-g_{m2}V_2 \\ -g_{m3}V_3-g_{m4}V_4 \end{bmatrix} \quad (3.13)$$

Let us define,

$$\begin{aligned} G^{17} &= g_{o1}+g_{o2}+g_{o5}+g_{o7}+g_{m5} \\ G^{38} &= g_{o3}+g_{o4}+g_{o6}+g_{o8}+g_{m8} \\ C^{56} &= C_{gs5}+C_{gs6}+C_{L1} \\ C^{78} &= C_{gs7}+C_{gs8}+C_{L2} \end{aligned}$$

So, under the above definitions, the problem is,

$$\begin{bmatrix} G^{17}+sC^{56} & g_{m7} \\ g_{m6} & G^{38}+sC^{78} \end{bmatrix} \begin{bmatrix} V_{o1} \\ V_{o2} \end{bmatrix} = \begin{bmatrix} -g_{m1}V_1-g_{m2}V_2 \\ -g_{m3}V_3-g_{m4}V_4 \end{bmatrix}$$

Which is a linear system of equations of the form $Ax = b$ and its solution is given by

$x = A^{-1}b$.

Le us define, just for convenience, $\Delta = \det A$,

$$\Delta = (G^{17} + sC^{56})(G^{38} + sC^{78}) - g_{m6}g_{m7}$$

And A^{-1} and b are,

$$A^{-1} = \begin{bmatrix} G^{38} + sC^{78} & -g_{m7} \\ -g_{m6} & G^{17} + sC^{56} \end{bmatrix} \qquad b = \begin{bmatrix} -g_{m1}V_1 - g_{m2}V_2 \\ -g_{m3}V_3 - g_{m4}V_4 \end{bmatrix}$$

This way, the solution is,

$$\begin{bmatrix} V_{o1} \\ V_{o2} \end{bmatrix} = \frac{1}{\Delta} \begin{bmatrix} -g_{m1}(G^{38} + sC^{78})V_1 - g_{m2}(G^{38} + sC^{78})V_2 + g_{m3}g_{m7}V_3 + g_{m4}g_{m7}V_4 \\ g_{m1}g_{m6}V_1 + g_{m2}g_{m6}V_2 - g_{m3}(G^{17} + sC^{56})V_3 - g_{m4}(G^{17} + sC^{56})V_4 \end{bmatrix}$$

In order to simplify the analysis, let us suppose that all the g_{mi}, g_{oi} and C_{gsi} are equal. This assumption is valid because the analysis is taken place in the surroundings of the commutation point. This fact makes all the circuit balanced so currents are equal at the cross point of the outputs. The loading capacitances will be considered equal as well.

Under these conditions, the solution can be written as,

$$\begin{aligned} V_{o1} &= \frac{-g_m(G + sC)}{\Delta}(V_1 + V_2) + \frac{g_m^2}{\Delta}(V_3 + V_4) \\ V_{o2} &= \frac{g_m^2}{\Delta}(V_1 + V_2) + \frac{-g_m(G + sC)}{\Delta}(V_3 + V_4) \end{aligned}$$

Beeing $\Delta = (G + sC)^2 - g_m^2$ and $G = G_m + 4g_o$, $C = 2C_{gs} + C_L$.

We note that there are two transfer functions to consider,

$$H_1 = \frac{-g_m(G+sC)}{\Delta} \qquad H_2 = \frac{g_m^2}{\Delta}$$

The denominator Δ can be expanded and studied,

$$\Delta = \underbrace{G^2 - g_m^2}_{\Delta_0} + \underbrace{2GC}_{\Delta_1} s + \underbrace{C^2}_{\Delta_2} s^2$$

$$\begin{aligned} \Delta_0 &= (g_m + 4g_o)^2 - g_m^2 = 8g_o(g_m + 2g_o) \approx 8g_m g_o \\ \Delta_1 &= 2(g_m + 4g_o)(2C_{gs} + C_L) \approx 2g_m(2C_{gs} + C_L) \\ \Delta_2 &= C^2 \approx 0 \end{aligned}$$

So,

$$\Delta \approx \underbrace{8g_m g_o}_{a_0} + s(\underbrace{2g_m(2C_{gs} + C_L)}_{a_1})$$

The simplifications made above, can be perfectly justified if the orders of magnitude are known. Gate capacitances are in the order of tenths of fF (10^{-14}), the transconductance of the MOSFET is in the order of hundreds of μS (10^{-4}) and the output conductance is about two orders of magnitude less than g_m, that is, μS (10^{-6}).

The numerator of H_1 is a first order polynomial in s, but it will be approximated by a first order one neglecting the term C in its transfer function.

Then, the system is governed by the following transfer functions,

$$H_1 = \frac{-g_m G}{a_0 + a_1 s} \qquad H_2 = \frac{g_m^2}{a_0 + a_1 s}$$

And under the same assumptions considered for G ($G \approx g_m$), H_1 and H_2 become,

$$H_1 = \frac{-g_m^2}{a_0 + a_1 s} \qquad H_2 = \frac{g_m^2}{a_0 + a_1 s}$$

Which are identical unless its sign. These results match to the fact that the circuit beeing analyzed is a differential amplifier with splitted inputs,

$$\begin{aligned} V_{o1} &= \frac{g_m^2}{a_o + a_1 s}\left(-(V_1 + V_2) + (V_3 + V_4)\right) \\ V_{o2} &= \frac{g_m^2}{a_o + a_1 s}\left(+(V_1 + V_2) - (V_3 + V_4)\right) \end{aligned}$$

The transfer function of the system, can be written in its canonical form as,

$$H = \frac{\pm A_{\mathrm{DC}}}{1 + \frac{s}{\omega_0}}$$

With,

$$\begin{aligned} A_{\mathrm{DC}} &= \frac{g_m^2}{a_o} = \frac{g_m}{8 g_o} \\ \omega_0 &= \frac{a_0}{a_1} = \frac{4 g_o}{2 C_{gs} + C_L} \end{aligned}$$

In order to estimate the delay of the whole monitor, only one input will be considered as variable, then

$$\begin{aligned} V_{o1} &= -\frac{A_{\mathrm{DC}}}{1 + \frac{s}{\omega_0}} V_i \\ V_{o2} &= \frac{A_{\mathrm{DC}}}{1 + \frac{s}{\omega_0}} V_i \end{aligned}$$

Which its transient step response will be the typical of a first order system,

$$y(t) = A_{\mathrm{DC}}(1 - e^{-\omega_0 t})$$

The delay time will be defined as the time the switching (crossed outputs) takes place. Because of the two outputs are symmetrical, it will be at the time the half DC gain is achieved, so,

$$\frac{A_{\mathrm{DC}}}{2} = A_{\mathrm{DC}}(1 - e^{-\omega_0 t_\delta})$$

From where,

$$t_\delta = \frac{\ln 2}{\omega_0} = \frac{(2C_{gs} + C_L)\ln 2}{4g_o}$$

Note the independence of g_m from the delay expression.

3.3.2. The small signal model applied to the second stage

The comparison stage is implimented using three CMOS differential amplifiers. The analysis will be performed the same way and also loading capacitances will be considered. The nodal analysis yields the following set of linear equations,

$$\begin{bmatrix} g_{o1} + g_{o3} + s(C_{gs3} + C_{gs4} + C_{L1}) & 0 \\ 0 & g_{o2} + g_{o4} + sC_{L1} \end{bmatrix} \begin{bmatrix} V_{o1} \\ V_{o2} \end{bmatrix} = \begin{bmatrix} -g_{m1}V_1 - g_{m3}V_{o1} \\ -g_{m2}V_2 - g_{m4}V_{o1} \end{bmatrix}$$

That is,

$$\begin{bmatrix} g_{o1}+g_{o3}+g_{m3}+s(C_{gs3}+C_{gs4}+C_{L1}) & 0 \\ g_{m4} & g_{o2}+g_{o4}+sC_{L1} \end{bmatrix} \begin{bmatrix} V_{o1} \\ V_{o2} \end{bmatrix} = \begin{bmatrix} -g_{m1}V_1 \\ -g_{m2}V_2 \end{bmatrix}$$

Beeing the solution,

$$\begin{aligned} V_{o1} &= \underbrace{\frac{-g_{m1}}{g_{o1}+g_{o3}+g_{m3}+s(C_{gs3}+C_{gs4}+C_{L1})}}_{\tilde{H}} V_1 \\ V_{o2} &= \underbrace{\frac{-g_{m4}}{g_{o2}+g_{o4}+sC_{L2}}\tilde{H}}_{H_1} V_1 + \underbrace{\frac{-g_{m4}}{g_{o2}+g_{o4}+sC_{L2}}}_{H_2} V_2 \end{aligned}$$

Note that only the output V_{o2} is used to load the following stage, so we are interested in its transfer functions H_1 and H_2 only. The previous statement stablishes that the consideration $C_{L1}=0$ is fasible.

Under the assumptions that the commutation takes place when the circuit is perfectly balanced, it is legal to suppose, as we did in the monitor circuit analysis, that all the transconductances and output conductances are equal as well as the gate capacitances.

This yields the following transfer functions,

$$H_1 = \frac{-g_m}{2g_o+sC_{L2}} \frac{-g_m}{2g_o+g_m+2C_{gs}s} = \frac{g_m^2}{D(s)} \qquad H_2 = \frac{-g_m}{2g_o+sC_{L2}}$$

The denominator $D(s)$ of H_1 is aimed to be studied concisely,

$$D(s) = \underbrace{[2g_o(2g_o+g_m)]}_{a_0} + \underbrace{[4g_oC_{gs}+(2g_o+g_m)C_{L2}]}_{a_1} s + \underbrace{[2C_{gs}C_{L2}]}_{a_2} s^2$$

$$\begin{aligned} a_0 &= 2g_o(2g_o + g_m) \approx 2g_m g_o \\ a_1 &= 4g_o C_{gs} + (2g_o + g_m)C_{L2} \approx 4g_o C_{gs} + g_m C_{L2} \approx g_m C_{L2} \\ a_2 &= 2C_{gs}C_{L2} \approx 0 \end{aligned}$$

And then,

$$H_1 = \frac{g_m^2}{2g_m g_o + g_m C_{L2} s} \qquad H_2 = \frac{-g_m}{2g_o + sC_{L2}}$$

So, with the exception of sign, they are identical, fact that matches with the assumption that the circuit beeing analyzed was a differential amplifier. So the transfer function of the circuit is,

$$H = \frac{g_m}{2g_o + sC_{L2}}$$

And the output is,

$$V_{o2} = H(V_1 - V_2)$$

Let us write the transfer function as is usual for a first order system,

$$H = \frac{A_{\mathrm{DC}}}{1 + \frac{s}{\omega_0}}$$

With $A_{\mathrm{DC}} = \frac{g_m}{2g_o}$ and $\omega_0 = \frac{2g_o}{C_{L2}}$.

To estimate the delay time, the same methodology which has been applied to the first stage circuit will be considered here. The time to achieve the half of the DC gain is,

$$t_\delta = \frac{\ln 2}{\omega_0} = \frac{C_{L2}\ \ln 2}{2g_o}$$

Again, note the independence of g_m in the delay expression.

3.4. Layout Implementation

In analog electronics, and specially if using a small technolgy (65 nm), layout design is critical to meet circuit specifications. The studied monitor circuit layout has been carried out taking in consideration common centroid strategies [10] in order to minimize mismatch effects.

In Figure 3.9 can be appreciated the final layout design. It uses 5 metal layers, standard V_{TH} and general purpose ST-Microelectronics transistors.

In order to achieve the final centroidal structure, any transistor has been splitted into four assuring this way a well-balanced structure.

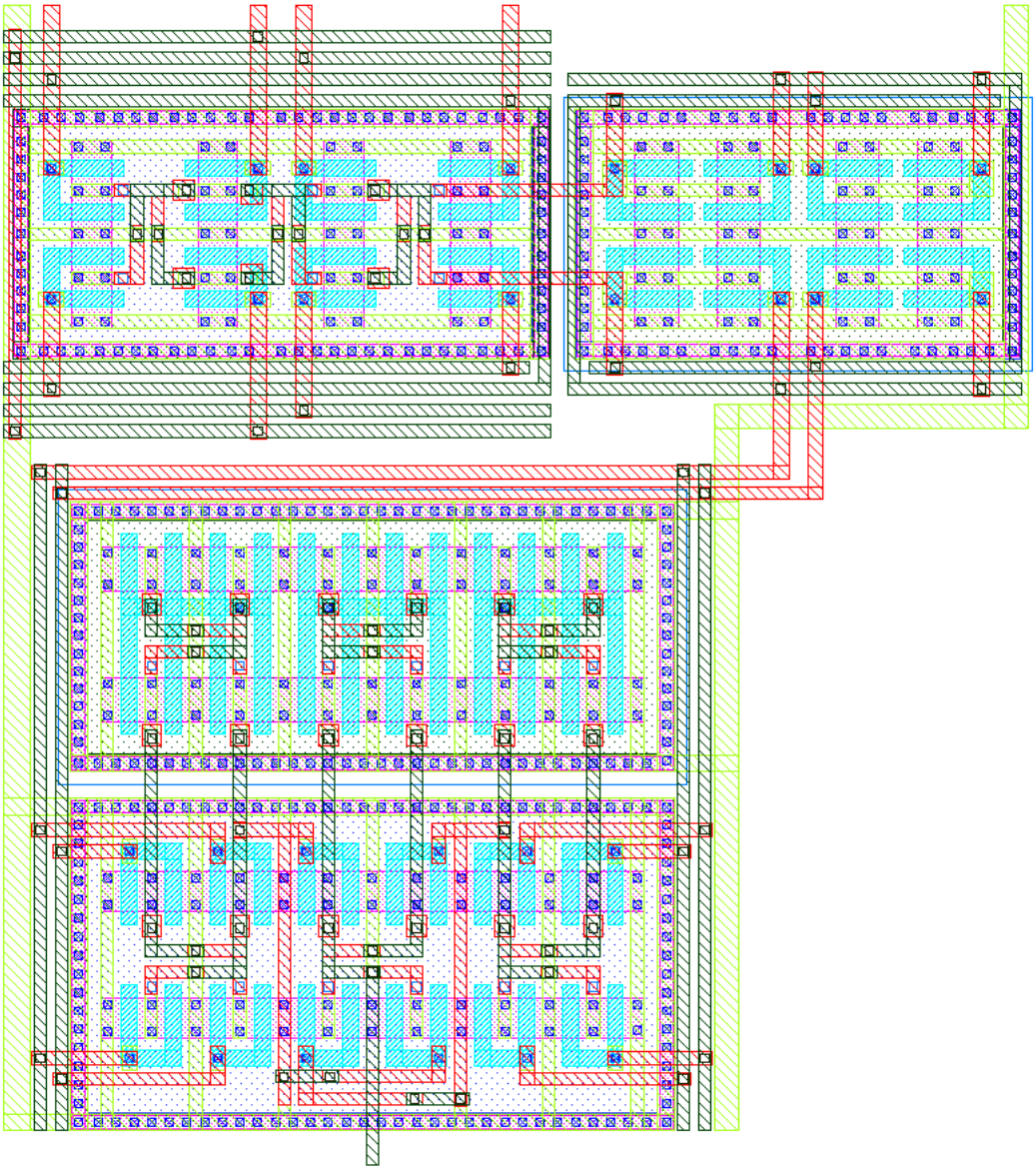


Figure 3.9: Layout implementation in CMOS ST-Microelectronics 65 nm technology. The total area used per monitor is 116.1 μm^2.

Chapter 4

Metric Definition

4.0.1. Definition

In order to be able to compare the digital signatures generated by the circuit, an indicator of difference is required. Taking in consideration the zone codification, a possible choice is the following definition of a Normalized Discrepancy Factor,

$$\mathrm{NDF} = \frac{1}{T}\int_0^T \mathrm{dist}(f,g)\,dt \tag{4.1}$$

where the functions $f(t)$ and $g(t)$ respectively represent the defective and golden signatures defined within the period T of the Lissajous curves. Operator dist() is the Hamming distance of the codes at each time instant. The NDF parameter indicates the discrepancy of the defective and golden instantaneous codes weighted by the duration of interval in which the Lissajous curve remains in the same zone.

The previous definition matches the average value of the Hamming distance chronogram over the interval $[0, T]$. For the example of Figure 4.2, a NDF of 0.102102 is obtained.

Because of the the zone codification criterion, neighbouring zones only vary in one bit. This is why Hamming distance is suitable, as can be observed in the lower chronogram of Figure 4.2, where the Hamming golden-defect distance is plotted during a period. Note the achievement of 2 (in the sense of Hamming distance) in the interval $[48, 50]\,\mu$s. This is

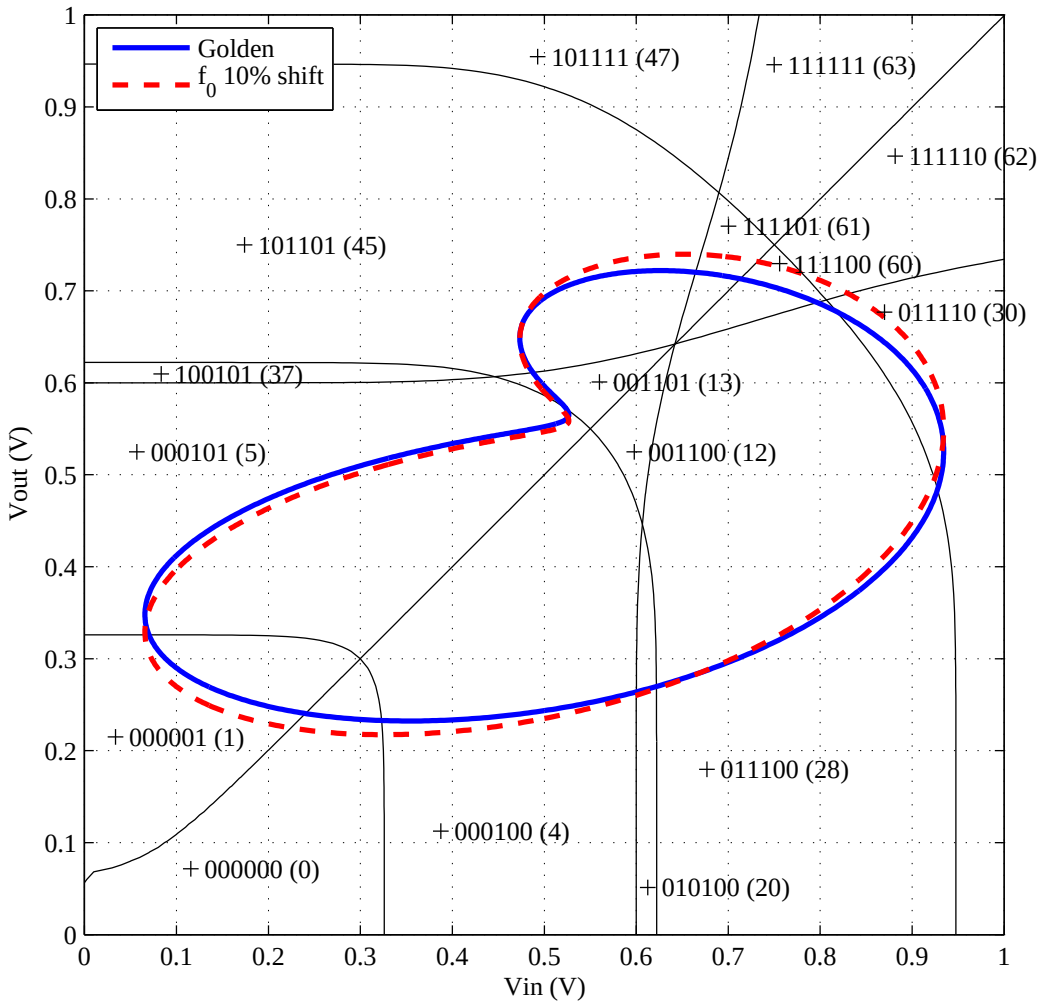


Figure 4.1: Control lines with zone codification and Lissajous compositions: golden and +10% shift in f_0.

because, in Figure 4.1, the faulty trace reaches zone 111110_2 (62_{10}) instead of the sequence 011110_2 (30_{10}), 011100_2 (28_{10}), 111100_2 (60_{10}), which will define a free-defect Lissajous.

4.0.2. Parameter Verification Process

The NDF is used to evaluate the amount of deviation of the parameters under verification. Circuits with parameters satisfying specifications are expected to present small NDF values. To evaluate the NDF effectiveness, extensive software simulations have been performed on a Biquad filter circuit with different degrees of deviation in the natural frequency

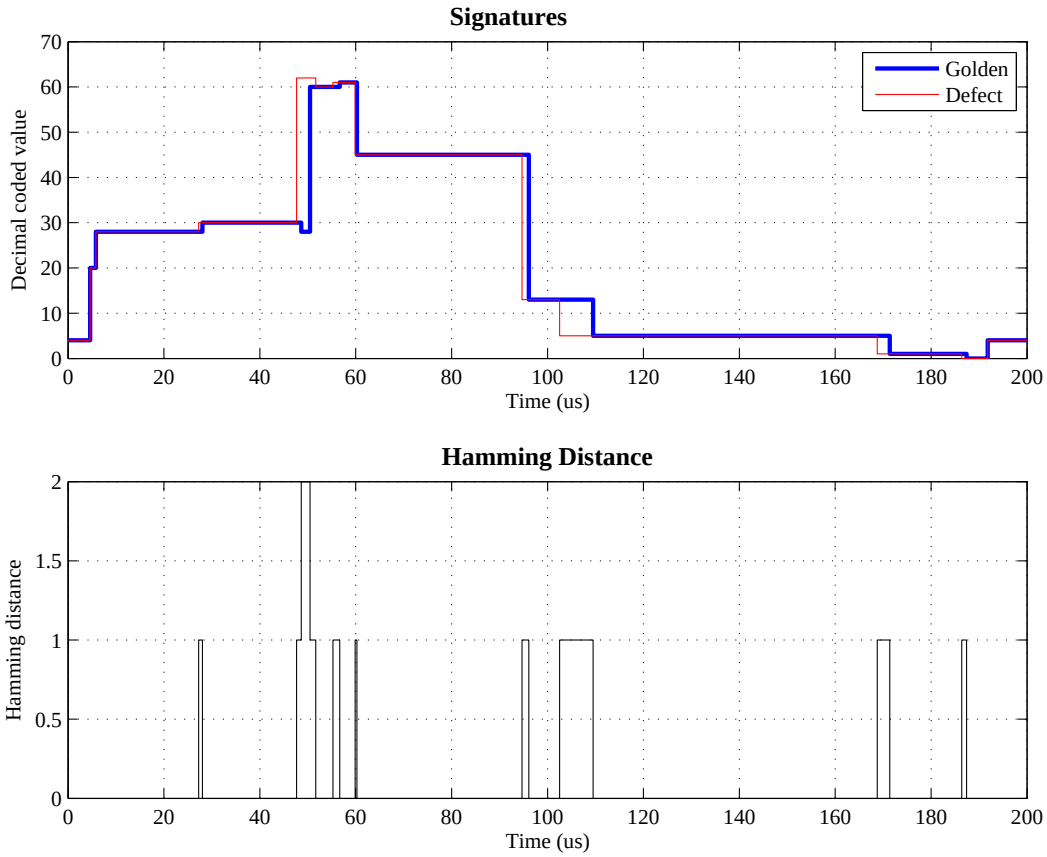


Figure 4.2: Chronogram of digital signatures and Hamming distances for +10% shift in f_0. NDF = 0.102102.

of the filter. The discrepancy factor increases almost linearly with the amount of deviation and quite symmetrically with positive and negative parameter deviations, as can be seen in Figure 4.4.

This metric detects discrepancies exceeding an absolute value over the nominal (golden) circuit parameter. In cases where the sign of the parameter deviation is required a data clustering procedure is used. To this purpose, distances between pairs of signatures are shown in Figure 4.5. This two-by-two comparison indicates that positive and negative defects lay separately in the N-dimensional space. Distances between same types of defects are also smaller than those mixing different types of defects.

A simple method to scatter the two groups of defects consists in computing a separation hyperplane. This data clustering method is performed by the calculation of the centre of gravity of every set and use it to define the hyperplane parameters. Let us respectively

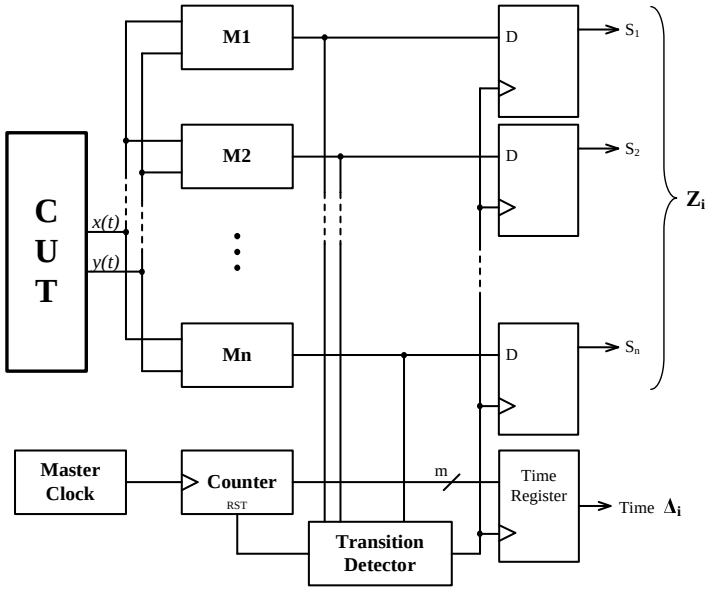


Figure 4.3: Asynchronous capturing module in order to generate the sigatures: the zone code and the time differences.

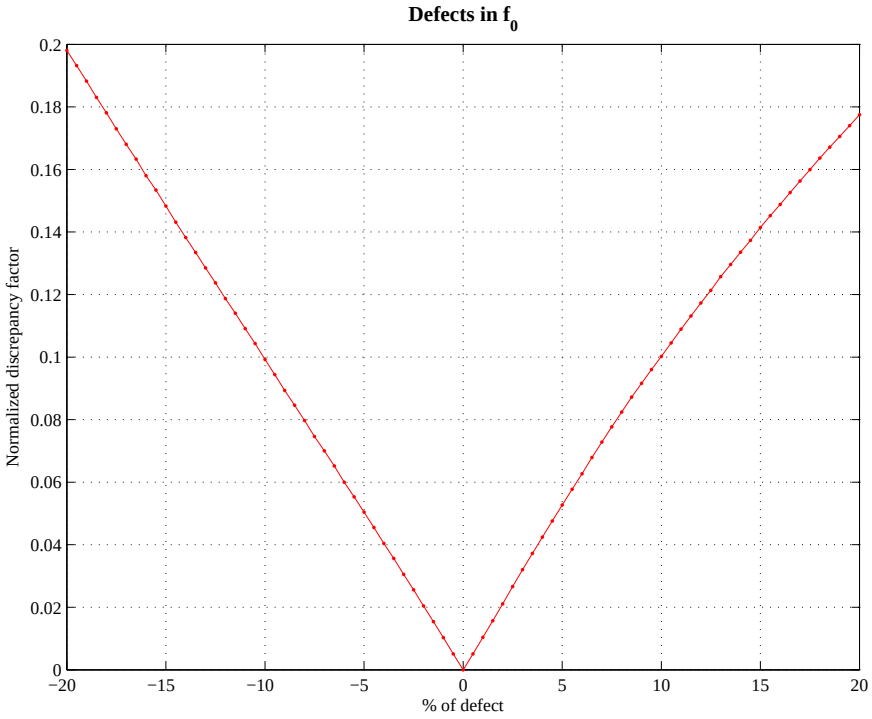


Figure 4.4: Normalized discrepancy factor for defects in f_0.

define z^+ and z^- as the centre of gravity of the positive and negative set of defects. In an N-dimensional vector space, a hyperplane takes the form,

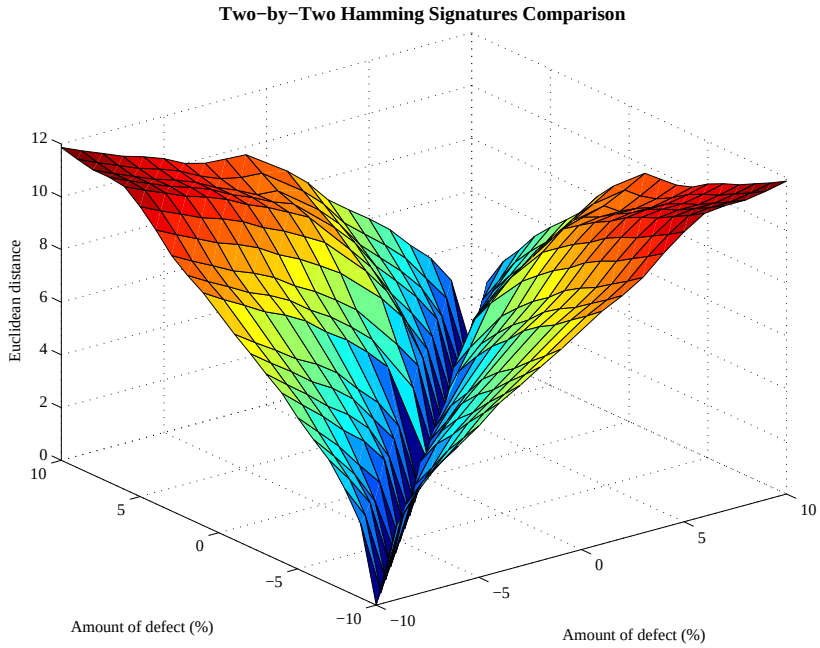


Figure 4.5: Distance between pairs of Hamming signatures.

$$\pi \equiv \sum_{i=1}^{N} n_i(z_i - p_i) = 0 \tag{4.2}$$

where $n = (n_1, \ldots, n_N)$ is a vector normal to π and $p = (p_1, \ldots, p_N)$ is any point within π. In this way, the following definitions become natural (see Figure 4.6),

$$n = z^+ - z^-, \quad p = \frac{z^+ + z^-}{2} \tag{4.3}$$

With the calculated π-hyperplane, parameter identification is easy because we only have to evaluate the resulting Hamming signature in the π equation. If the evaluation yields a positive number, the defect is positive whereas if it yields a negative value, the defect is negative. The amount of defect is determined with the graphical data of Figure 4.4.

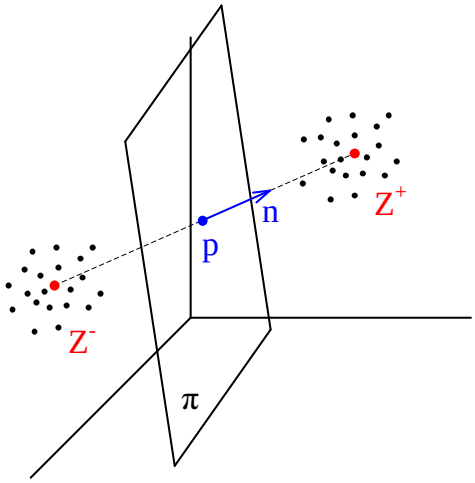


Figure 4.6: Sketch of the separation plane in a three-dimensional vector space.

Chapter 5

Test Bench and Circuit Under Test

In order to check the designed monitor circuit and the developed test/diagnosis methodology, a test bench and a CUT are required. Both have been designed in single sided copper PCB with the aim to provide easy access to signals and components. This chapter shows the results on the fabrication and points out the objectives being pursued.

Originally, the goal was to use a PLL board at 55 MHz to test the fabricated monitor, but due to the results on frequency response of the monitor circuit, the decision to test only the filter part has been taken. In order to see details of the purchased PLL board and the associated VCO chip see appendix I.

5.1. Test Bench Design

The fabricated monitor circuit has the following available signal connections:

1. Independent power supply for core and pads.
2. Four input voltages.
3. Two differential analog outputs from first stage (for each monitor).
4. One digital output from first stage (for each monitor).
5. One digital output from second stage (for each monitor).

Note that some of them are repeated for the balanced and unbalanced layouts that have been implemented.

The designed test bench has been designed in order to gain easy access to each signal and allow extra components connections as decoupling capacitors, wiring, probes, buffer outputs, filtering, CUT connections,... A rough design of the layout can be seen in Figure 5.1.

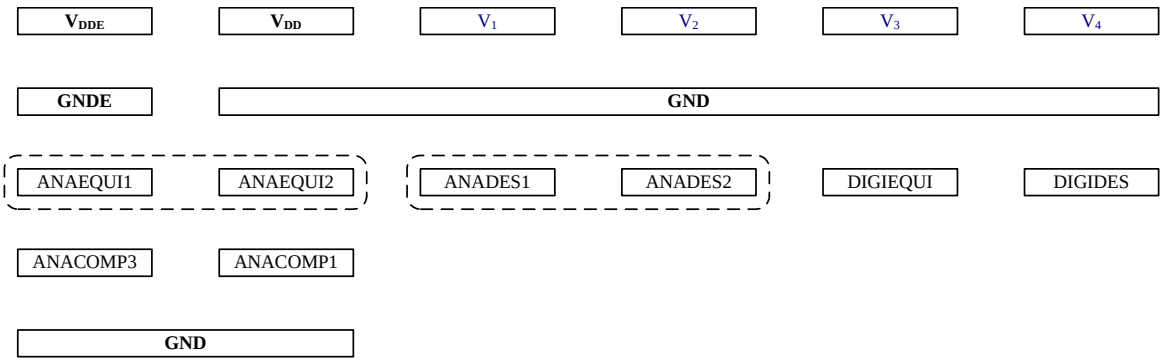


Figure 5.1: Test bench schematized layout.

The fabricated chip packaging requires IC51-0644-807 socket (see appendix I for socket details). This is not a common socket that can be found in OrCAD Layout footprint libraries, so it has been to be hand designed accordingly to socket datasheet dimensions. In order to create footprint pins, a small script has been coded in Visual Basic to automate the process.

Test bench has been designed with OrCAD Layout and has been fabricated by CNC routing to *Taller Mecànic ETSEIB*. The final PCB layout can be seen in Figure 5.2. The PCB has been provided with an array of prototyping pins in order to use them to connect different auxiliary circuits.

Tracks widths of the design have been set to 12 mils and have been hand routed in order to optimize the design and avoid extra line capacitances and induced antenna behaviour.

The designed test bench PCB has been sent for fabrication to *Taller Mecànic ETSEIB*. The final product can be seen in Figure 5.3. In the photograph also appears the chip socket, CUT circuit and connections.

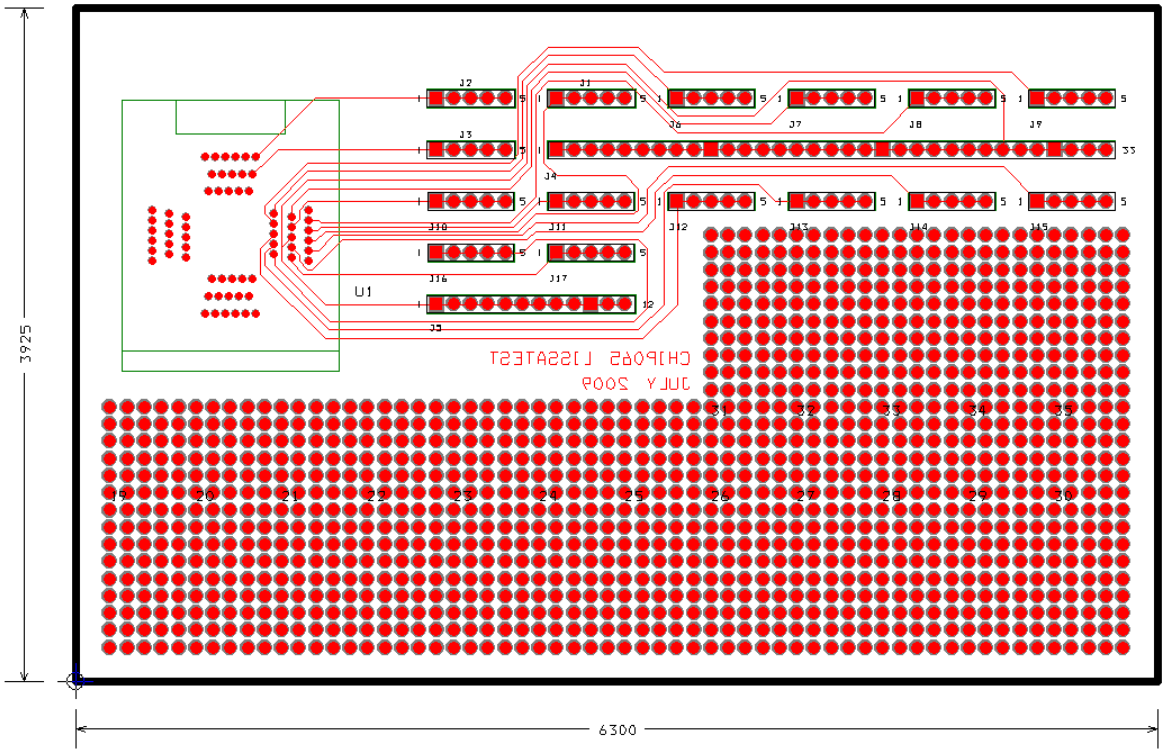


Figure 5.2: Test bench layout designed with OrCAD Layout. The design has been sent to CNC fabrication at *Taller Mecànic ETSEIB*.

5.2. Circuit Under Test Design

As the low-pass filter of the PLL implementation can be of any kind [11] (the PLL board provides input and output pins in case of future connections intentions) a second order biquad filter implementation has been selected to test the fabricated monitor. In the following lines, a brief introduction theory of biquad filters and the fabricated filter itself will be shown.

5.2.1. Low-Pass Biquad Filter Theroy

A second order low-pass Biquad filter [12] is a state variable filter which transfer function (relation between the input and the output signals) is described by the following expression (note that a cononical unity gain has been chosen for theoretical explanation),

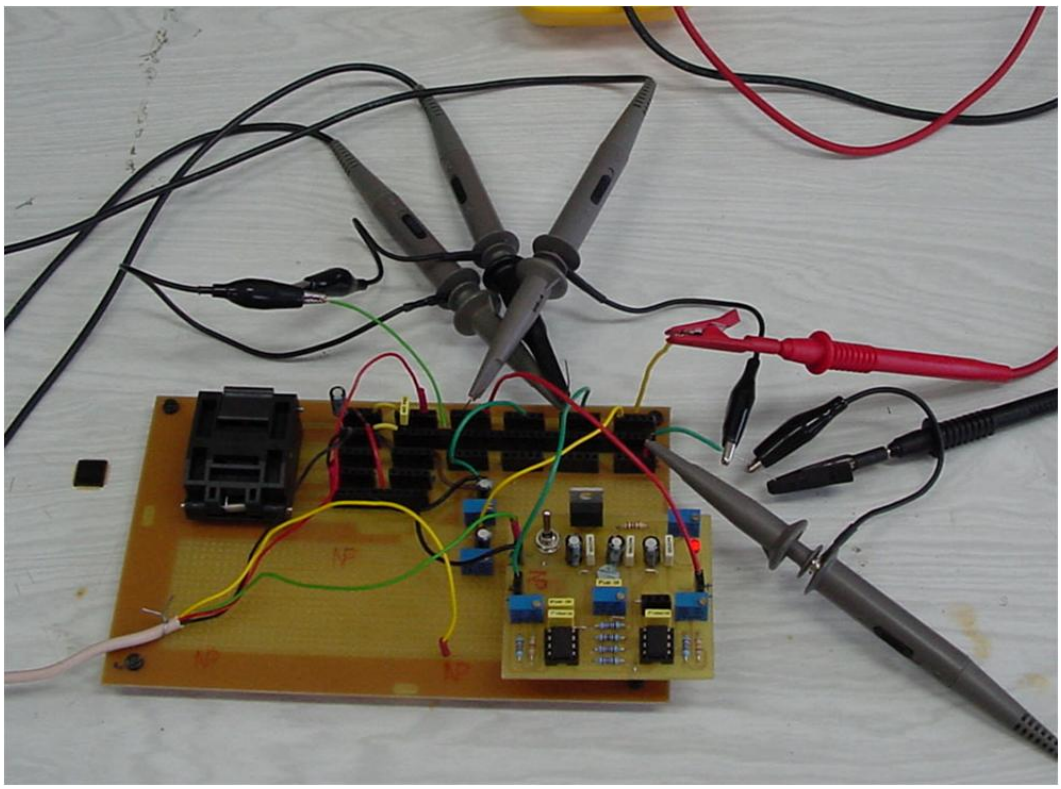


Figure 5.3: Photograph of the machined PCB to lodge the IC socket, CUT circuit and connections between the modules and the oscilloscope and function generator. Power supply wires and signal probes can be seen too.

$$\frac{V_o}{V_i} = \frac{1}{\frac{s^2}{\omega_0^2} + \frac{1}{Q}\frac{1}{\omega_0} + 1} \tag{5.1}$$

From the above expression, $\frac{s^2}{\omega_0^2}V_o + \frac{1}{Q}\frac{s}{\omega_0}V_o + V_o = V_i$ and multiplying by $\frac{\omega_0}{s}$ and solving for $\frac{s}{\omega_0}V_o$ yields,

$$\underbrace{\frac{s}{\omega_0}}_{\text{A}} = \frac{\omega_0}{s}V_i \underbrace{-\frac{1}{Q}V_o}_{\text{B}} \underbrace{-\frac{\omega_0}{s}V_0}_{\text{C}} \tag{5.2}$$

From the above equation, the block diagram of Figure 5.4 is obtained. Note that because the filter will be implemented using operationa amplifiers, it is easy to multiply by a negative constant.

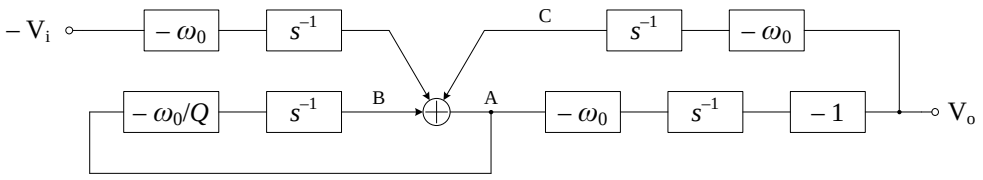


Figure 5.4: Block diagram.

It is immediate to draw the corresponding schematic from the block diagrams shown in Figure 5.4 using opertational amplifiers in inverting configuration. As can be checked in Figure 5.5, summing inverter/integrating amplifiers has been used.

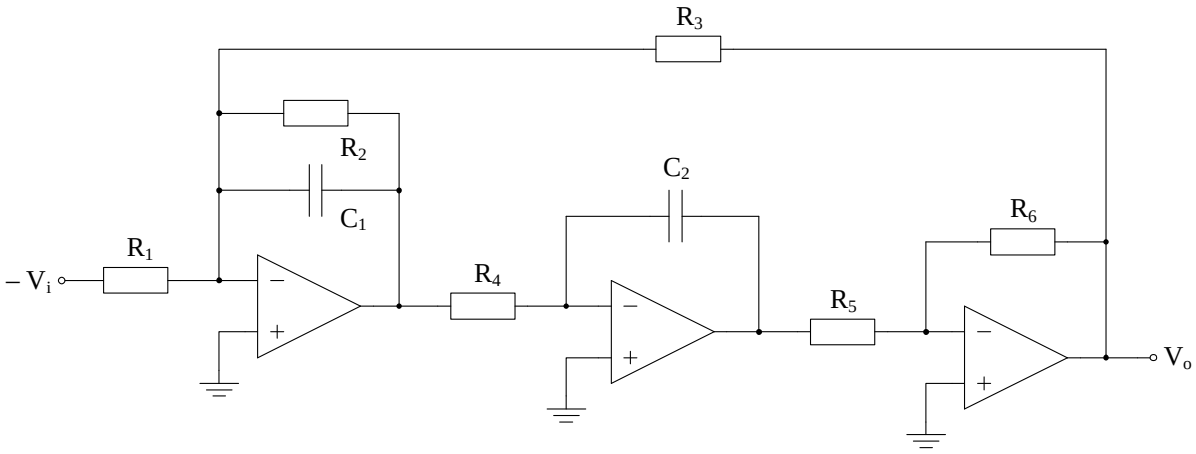


Figure 5.5: Biquad filter schematic.

Accordingly to the summing and integrating weights, the following equations state,

$$\omega_0 = \frac{1}{R_1 C_1}, \quad \frac{\omega_0}{Q} = \frac{1}{R_2 C_1}, \quad \omega_0 = \frac{1}{R_3 C_1}, \quad \omega_0 = \frac{1}{R_4 C_2}, \quad R_5 = R_6 \tag{5.3}$$

Any circuit with the same structure of Figure 5.5 and acoomplishing the previous set of equations will be Biquad filter.

5.2.2. Circuit Under Test Design

In order to generalize the results and understand the influence of each component on the different Biquad filter parameters, the structure of Figure 5.5 has been analysed without any restrictions on the components.

With a bit of algebra can be shown that the transfer function that steers the behaviour of Figure 5.5 circuit in the frequency domain is,

$$H(s) = \frac{-\frac{R_3}{R_1}}{1 + s(1 + sR_2C_1)R_4C_2\frac{R_3R_5}{R_2R_6}} \tag{5.4}$$

The denominator of the previous equation can be written in the form of as^2+bs+1 and identifying the polynomial coefficients, yield $a = \frac{R_3R_4R_5}{R_6}C_1C_2$ and $b = \frac{R_3R_4R_5}{R_2R_6}C_2$. For a filter with a denominator in the polynomial form presented earlier, its characteristic parameters are $\omega_0 = \frac{1}{\sqrt{a}}$ and $Q = \frac{\sqrt{a}}{b}$. In the case of the filter being studied, these parameters are,

$$A_{\mathrm{DC}} = -\frac{R_3}{R_1}, \quad \omega_0 = \sqrt{\frac{R_6}{R_3R_4R_5C_1C_2}}, \quad Q = R_2\sqrt{\frac{R_6C_1}{R_3R_4R_5C_2}} \tag{5.5}$$

With the aim of high performance and low distorsion and low noise in the signal levels, good quality operational amplifiers have been chosed. The Texas Instruments TLC2272 is a CMOS opamp with a typical offset voltage of 300 mV, input bias current as low as 1 pA, input impedance of about 10^{12} Ω, a high slew rate of 3.6 $\frac{\mathrm{V}}{\mu\mathrm{s}}$ and a CMRR and PSRR arround 75 and 90 dB respectively is the chosen solution.

In order to construct the filter, two dual TLC2272 have been used. Because of the dispose of four operational amplifiers, and extra one has been added at the end stage of the design as can be seen in the schematic in appendix I.

Accordingly to the previously presented equations, the components have been set to those presented in Table 5.1. All resistors (and potentiometers) values are in kΩ and capacitor values in nF.

R_1	R_2	P_2	R_3	R_4	R_5	R_6	P_6	R_7	R_8	P_8	C_1	C_2
22	4.7	5	22	22	22	22	50	22	20	5	1	1

Table 5.1: Components values. Resistors in kΩ and capacitors in nF.

The components have been calculated to allow the proper adejustment of the CUT parameters and to allow the inclusion of defects in the natural frequency of the filter. The potentiometers allow to achieve a ±20% of variation in the characteristic frequency of the filter from its nominal value of 10 kHz.

There is one experimental operation handicap in the use of such Biquad filter. Filter parameters values are function of different components, so by varying one potentiometer, not only the center frequancy os varied but also the quality factor, so it is mandatory for each defect to setup the filter properly.

The filter has been implemented in one sided copper PCB using OrCAD Layout software. The resulting layout can be checked in Figure 5.6. The routed process has been automatically in 12 mils tracks in width. The layout design includes a 5 V regulator as a power supply and connectors for input and output signals. Also, has been included a connector for allowing the user to use diodes at the output in order to provent over voltages to be applied directly to the chip.

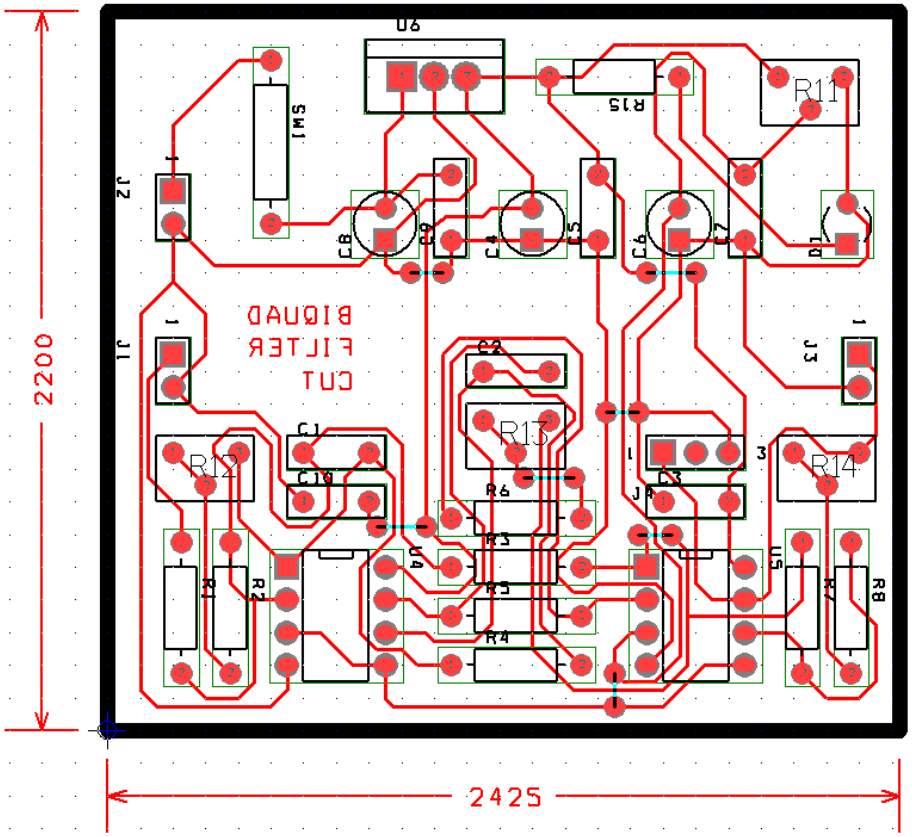


Figure 5.6: Biquad filter layout designed with OrCAD Layout.

In Figure 5.7 can be appreciated the resulting PCB. The fabrication technique has not been as laboured as test bench board since it has been homemade manufactured. The process consists on applying toner in order to define tracks and pads. Then an acid solution is applied

and after rinsing and removing the sticked toner, the PCB is finished. The method is only suitable for simple PCB (single sided and a few components).

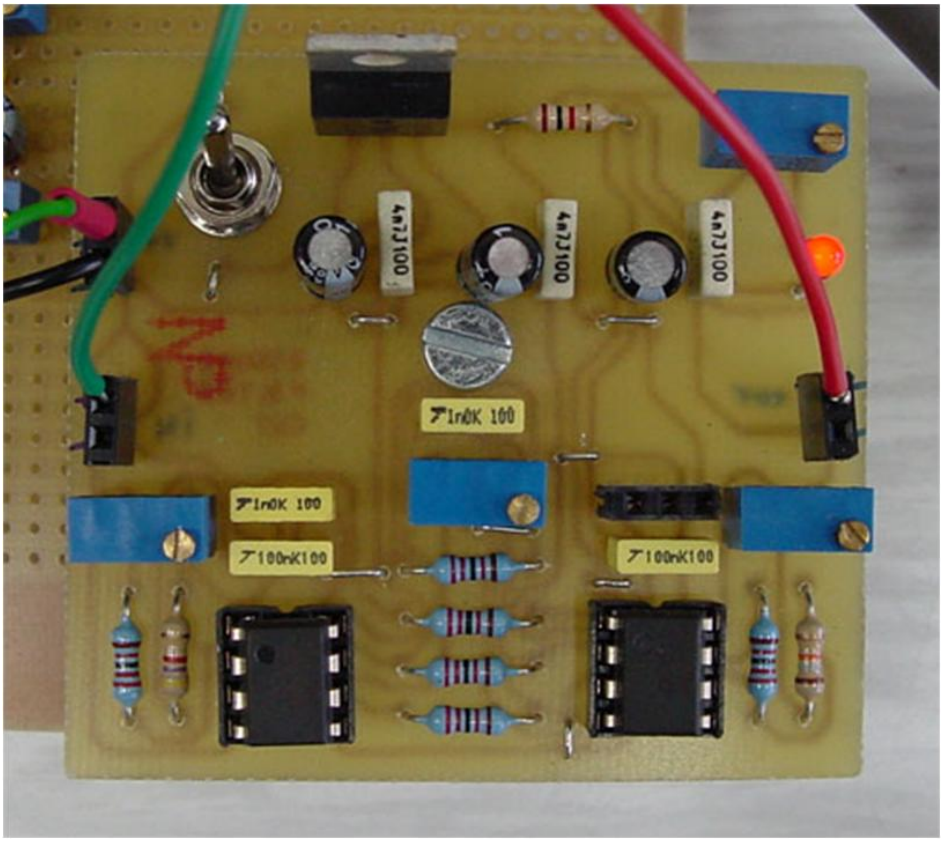


Figure 5.7: Photograph of the fabricated PCB for the circuit under test. It is a tunable low-pass Biquad filter. Input and output signal wires can be checked at the picture.

Chapter 6

Experimental Results

Once the chip has arrived from foundry (run S65C8_6), it has been tested in order to check its behaviour and performance. In Figure 6.1 can be seen an augmented photograph of the fabricated die using a bulk CMOS process. It has 1×1 mm^2 of area and lodges many research projects from the different Department interests areas.

The first test that has been applied to the circuit consists in checking if it is behaving like a nonlinear comparator. For this purpose, different input signals has been considered and different control DC voltages have been tuned. This allows a good coverage of the XY plane tesselation. In Figure 6.3 can be appreciated the transient response of the comparator to an input sinusoid and a constant reference.

Once the functional behaviour of the second stage circuit is tested, the switching curve generation in the XY plane is studied. In order to obtain such results, a quasi-static transient analysis has been applied considering a ramp input for one of the axis while maintaining the other to a constant DC level. The trip point of the digital output determines uniquely each point and shape of the switching curves. With the aid of a voltmeter and a function generator, the observed switching curves can be seen in Figure 6.4. The shape of the lines match the theoretically and simulated predicted, within the technology variability specifications. The configuration parameters for each considered curve are those appearing in Table 6.1

A complete check of the proposed method with the case example of the Biquad filter has been performed. The CUT circuit has been properly tuned for different f_0 shifts, which

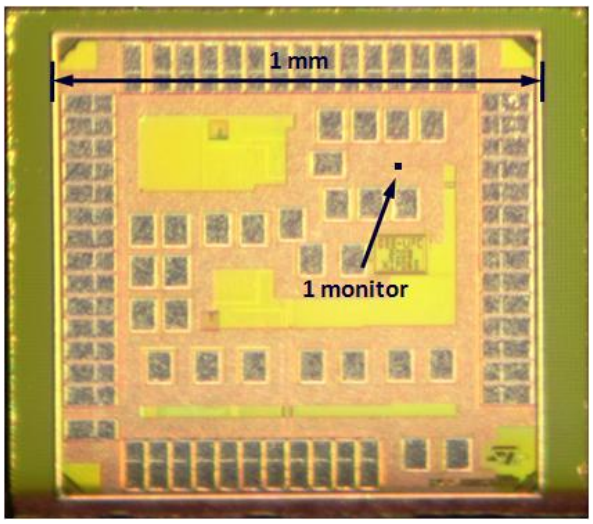


Figure 6.1: Photograph of the die of the fabricated chip. The photograph marks the area occupied by a single monitor.

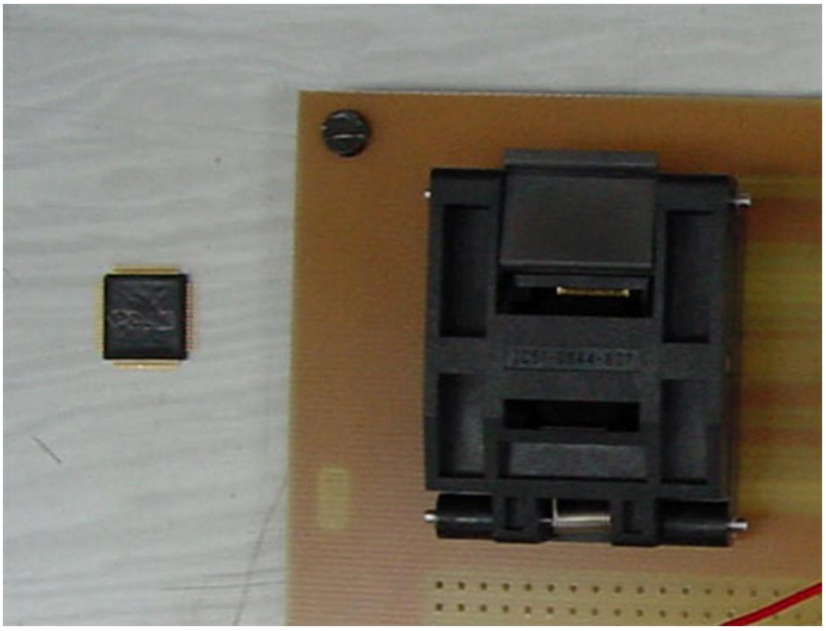


Figure 6.2: Detail of the IC socket (right) and the encapsulated chip (left).

response has been composed with the monitor circuit. This way, different signatures, for each switching curve, have been obtained. In Figure 6.5, the multitone input signal and its low-pass filter response can be seen, as well as the monitor circuit periodic digital code. In Figure 6.6, the resulting Lissajous composition of the input multitone excitation and the CUT response can be appreciated.

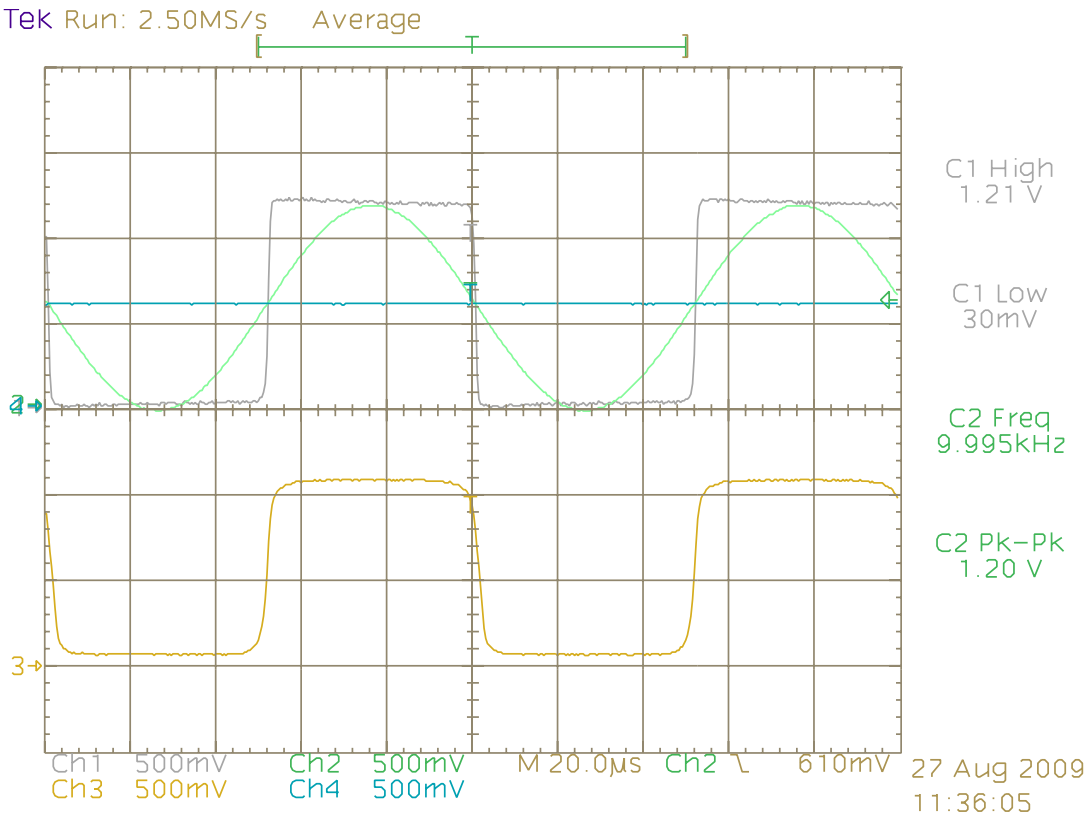


Figure 6.3: Experimental transient switching assuring the corrent performance of the comparator module. Can be appreciated the one stage output and the one corresponding to the trimodular architecture.

	Transistor widths (nm) ($L = 180\,\text{nm}$)				Applied input voltages (V)			
	M1	**M2**	**M3**	**M4**	V_1	V_2	V_3	V_4
1	3000	600	600	3000	Y axis	0.2	X axis	0.6
2	3000	600	600	3000	0.6	Y axis	0.2	X axis
3	1800	1800	1800	1800	Y axis	X axis	0.55	0.55
4	1800	1800	1800	1800	Y axis	X axis	0.3	0.3
5	1800	1800	1800	1800	Y axis	X axis	0.75	0.75
6	1800	1800	1800	1800	Y axis	0	X axis	0

Table 6.1: Input transistor dimensions and applied voltages for the curves depicted in Figure 6.4.

With the aid of the developed software tool, the difference with the golden signature has been computed for all the applied f_0 deviations. The obtained metric values are shown

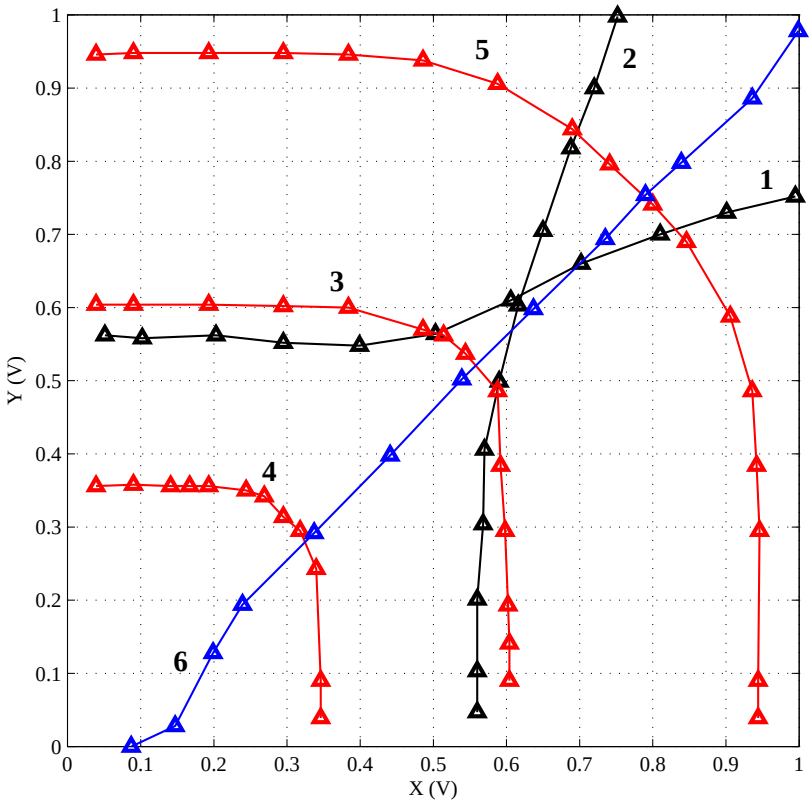


Figure 6.4: Experimental switching curves.

in Figure 6.7. With this mapping, any defective (only f_0 shifts) circuit can be diagnosed with the unique information of the resulting NDF factor.

As a case examples, three random f_o shifts (within the studied range of -20% to $+20\%$) have been applied to the CUT in order to compute their digital signature. With the aid of the metric and the mapping, the results of Table 6.2 are obtained. As can be seen, the predicted f_0 shifts are quite similar to the real ones, what validates the proposed method.

	CUT defect (%)	**NDF**	**Predicted defect (%)**
Example 1	-12	0.096	-11.9
Example 2	+1	0.010	0.89
Example 3	+18	0.88	+18.4

Table 6.2: CUT experimental results on the diagnosis procedure.

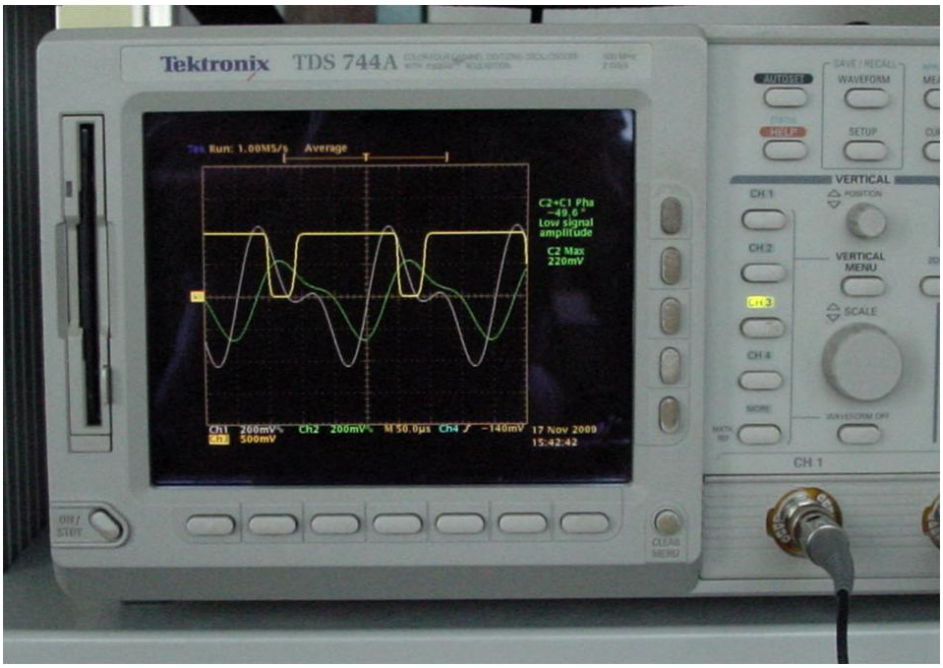


Figure 6.5: Transient response of the monitor circuit to a multitone input. Fundamental frequency is 10 kHz.

Figure 6.6: Shot of the oscilloscope screen composing the multitone input signal and the resulting from the Biquad low-pass filter. The resulting shape matches with the previously calculated one.

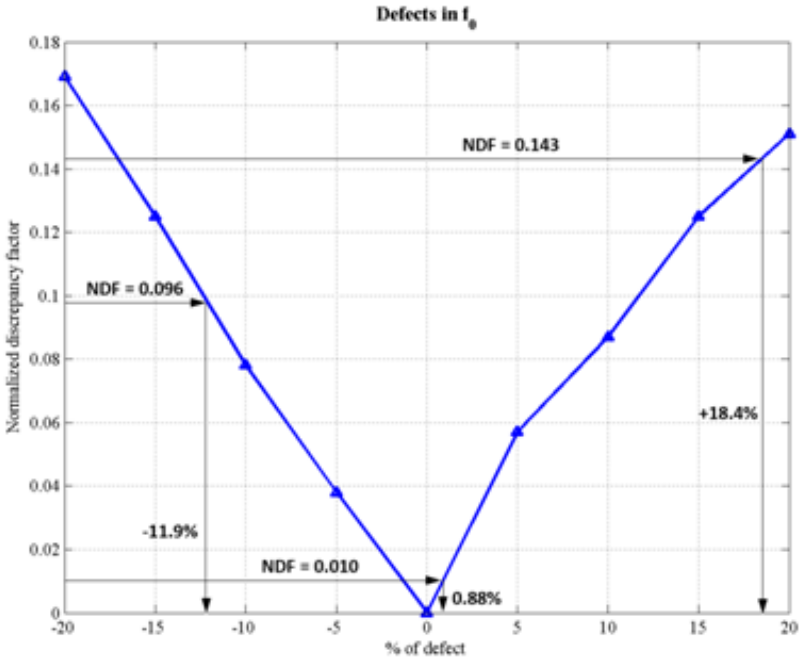


Figure 6.7: Mapping between the amount of defect in the Biquad filter characteristic frequency and the NDF factor resulting from golden-defective metric comparison.

Chapter 7

Conclusions and Future Work Outlines

A CMOS 65 nm monitor circuit has been presented and analysed. The monitor circuit is a two stage design. The former stage compares the signals and provides the switching curve tessellation. The latter is a high gain stage that digitises the differential output from the first stage in order to perform the codification for each XY plane zone. Both stages analysis include DC large signal and small signal study. For the last, a delay model has been developed and checked against simulation and experimental results.

The theoretical switching curves generated by the first stage have been achieved by the use of the fitted Unified MOSFET Model to ST-Microelectronics 65 nm technology. The fitting methodology is the well known linear least squares method generalized to nonlinear functions via first order Taylor approximation. DC and transient simulations results, PVT variations have been also studied using Monte Carlo simulations and the developed model considering Gaussian parameter distribution. Both studies (simulation and theoretical) yield similar results of an average of 60 mV of 6σ spread on switching curves.

The CMOS monitor circuit has been designed in ST-Microelectronics 65 nm technology by the use of common centroid analog design techniques in order to avoid (or at least minimize) mismatch effects. The layout has been included in a multiproject chip for fabrication.

A novel digital signature comparison and diagnosis method has been also presented.

The method takes advantage of the zone codification criteria which makes that neighbouring zones to be at Hamming-1. The discrepancy criterion is performed via the so defined Normalized Discrepancy Factor (NDF) as the average Hamming distance between the golden and the observed signatures over a period. Software simulations allow to determine the NDF factor as a function of the amount of defect allowing this way the diagnosis of a CUT. The mapping between NDF and the percentage of defect is a non one-to-one relation what makes necessary a statistical data clustering process using the fact that differences vectors lay in separately regions of the hyperspace.

In order to avoid the tedious statistical scattering process a new metric has been introduced. Its definition is similar to he former but uses two NDF, one for positive differences and one for negative differences. With the latter metric definition, the mapping of the amount of defect and the two NDF factors is performed in a straight forward way if the set of possible defects has been simulated.

The CUT diagnosis method shows high reliability and simple software implementation allowing to be directly applicable to any pair of signatures comparison in which Hamming distance makes sense of discrepancy. Experimental results have been presented showing that the developed method works as expected.

As a future work, a quantification of performance with noisy signal would be desirable. The method should consider switching bands and not thin curves. Under this assumption, the mapping between the NDF factor and the amount of defect will become into a statistical distribution function.

Also, a complete implementation of the method would be desirable, that is, not only the monitor circuit but also the CUT and the digital processing of signatures. This would require more silicon area but would be adequate in order to assess the reliability of the method under real circumstances.

More research in the method of generating the digital signatures would be a good starting point in order to go further in XY zoning methods. In the current project, two different methods have been presented: one for generating the digital signatures (XY plane tessellation) and one to perform the digital processing of the generated sequences. Both methods could be improved and tested experimentaly over many fabricated circuits.

Agradecimientos

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Bibliography

[1] R. Sanahuja, "On-Chip Monitor for Mixed-Signal testing based on X-Y Zoning," Ph.D. dissertation, Departament d'Enginyeria Electrònica, UPC, 2006.

[2] H. Shichman and D. A. Hodges, "Modeling and Simulation of Isolated-Gate Field-Effect Transistor Switching Circuits," *IEEE Journal of Solid-State Circuits*, vol. 3, pp. 285–289, September 1968.

[3] J. Rius, *Apunts d'Introducció a l'Electrònica.* Barcelona: CPDA-ETSEIB, 2005.

[4] H. Veendrick, *Deep-Submicron ICs*, 2nd ed. Deventer, The Netherlands: Ten Hagen en Stam, 2000.

[5] *HSPICE Command Reference*, Synopsis, September 2005.

[6] *Design Rules Manual for 65 nm Bulk CMOS Process*, STMicroelectronics, December 2005.

[7] J. M. Rabaey, A. Chandrakasan, and B. Nikolić, *Digital Integrated Circuits, a Design Perspective*, 2nd ed. Prentice Hall, 2003.

[8] P. E. Allen and D. R. Holberg, *CMOS Analog Circuit Design.* New York: Oxford University Press, 1987.

[9] J. P. Uyemura, *Introduction to VLSI Circuits and Systems.* John Wiley & Sons, 2002.

[10] T. Sakurai and A. R. Newton, "Alpha-Power Law MOSFET Model and its Applications to CMOS Inverter Delay and Other Formulas," *IEEE Journal of Solid-State Circuits*, pp. 584–594, April 1990.

[11] R. Pindado, "Phase Locked-Loop PLL: Fundamento y aplicaciones," *JCEE*, 2001.

[12] S. Franco, *Design with Operational Amplifiers and Analog Integrated Circuits*, 3rd ed. New York: McGraw-Hill, 2002.

[13] R. Sanahuja, A. Gómez, L. Balado, and J. Figueras, "Digital Signature Generator for Mixed-Signal Testing," in *Proceedings of the European Test Symposium*, Seville, 2009.

[14] A. Gómez, R. Sanahuja, L. Balado, and J. Figueras, "Verifying Analog Circuits Based on a Digital Signature," in *Proceedings of Design of Circuits and Integrated Systems Conference*, Zaragoza, 2009.

[15] A. Gómez, R. Sanahuja, L. Balado, and J. Figueras, "Analog Circuit Test Based on a Digital Signature," in *Proceedings of Design Automation and Test in Europe Conference*, Dresden, 2010.

[16] P. R. Gray, P. J. Hurst, S. H. Lewis, and R. G. Meyer, *Analysis and Design of Analog Integrated Circuits*, 4th ed. John Wiley & Sons, 2001.

[17] L. Balado, E. Lupon, J. Figueras, M. Roca, E. Isern, and R. Picos, "Verifying Functional Specifications by Regression Thechniques on Lissajous Test Signatures," *IEEE Transactions on Circuits and Systems*, April 2009.

[18] D. Long, X. Hong, and S. Dong, "Optimal Two-Dimension Common Centroid Layout Generation for MOS Transistors Unit-Circuit," in *Proceedings of IEEE International Symposium on Circuits and Systems*, May 2005, pp. 2999–3002.

[19] L. S. Milor, "A Tutorial Introduction to Research on Analog and Mixed-Signal Circuit Testing," *IEEE Transactions on Circuits and Systems*, pp. 1389–1407, October 1998.

[20] M. L. Bushnell and V. D. Agrawal, *Essentials of Electronic Testing.* Kluwer Academic Publishers, 2002.

[21] A. Ruíz, *Sel·lecció d'una targeta d'evaluació per PLL's*, April 2009.

[22] R. B. D'Augostino and M. A. Stephens, *Goodness of Fit Techniques.* New York: Marcel Dekker, 1986.

[23] R. Sanahuja, V. Barcons, L. Balado, and J. Figueras, "Testing Biquad Filters under Parametric Shifts Using X-Y Zoning," *Journal of Electronic Testing: Theory and Applications*, vol. 21, pp. 257–265, June 2005.

Appendix A

Costs Evaluation

Project costs evaluation is nearly as important as the correctness of the experimental results because the overall reliability of the proposed testing method will be judged by both outcomes. In this appendix, the costs attributed to the project development are depicted. They have been broken down into the following categories:

- Human resources costs
- Chip fabrication costs
- Materials costs
- Equipment and software costs
- Other costs

A.1. Human Resources Costs

Those costs concerning the people working on the project are attributed as human resources. In current thesis, three people have been considered and the involved costs are directly related to their professional categories and the time devoted to the project. The description of human resources costs can be seen in Table A.1.

Resource	**Function**	**Time (h)**	**Cost (€/h)**	**Total (€)**
Professor	Project manager	120	75	9000
Associate Professors	Consultants	120	70	8400
Junior Engineer	Project developer	2000	25	50000
			TOTAL (€)	**67400**

Table A.1: Human resources costs.

A.2. Chip Fabrication Costs

The fabrication of the chip has been carried out by CMP[1] on the firsts months of 2009. As explained, the multiproject chip has been fabricated using ST-Microelectronics 65 nm CMOS technology. The circuit die area is 1×1 mm^2 what makes the fabrication cost rise up to 9500 € accordingly to CMP fees.

A.3. Material Costs

In order to verify the correct operation of the fabricated circuit and the developed test/diagnosis methodology, different hardware is required besides the chip. In the following three subsections, the detailed costs for the test bench and CUT fabrication, as well as the PLL evaluation board, are listed.

A.3.1. Test Bench

The test bench consists in a single sided CNC machined PCB with routed traces from the chip socket to female header pins. The costs concerning the construction of the tests bench setup are displayed in Table A.2.

[1] Circuits Multi-Projets, `http://cmp.imag.fr`.

Item	**Unit cost (€/u)**	**Units**	**Cost (€)**
CNC machined single sided copper PCB	110.00	1	110.00
IC51-0644-807 socket	42.03	1	42.03
Female header	0.25	5	1.25
Decoupling capacitors	0.35	4	1.40
M4 screws	0.02	4	0.08
Tin soldering wire	2.30	1	2.30
		TOTAL (€)	**157.06**

Table A.2: Test bench costs.

A.3.2. Circuit Under Test

The circuit under test being used in the thesis is an active Biquad low-pass filter. In order to achieve a comfortable working setup, the CUT has been mounted on single sided copper PCB and then attached to the test bench board. The CUT components' costs are listed in Table A.3.

A.3.3. PLL Evaluation Board

As exposed in the thesis, the initial CUT circuit was intended to be a fully working PLL system, so an evaluation board for a phase lock loop circuit was purchased. It is composed by the PLL board itself, the synthesiser and the VCO circuits. The costs can be checked in Table A.4.

A.4. Equipment and Software Costs

Research and experimental work require instrumentation and laboratory equipment as well as engineering software tools to obtain the appropiate results. During the project, software tools have played an important role due to the nature of the research: circuit simulation, data fitting, data clustering, computer algebra calculations,... The same occurs with electronic instrumentation such as power supplies, oscilloscopes, function generators,

Item	**Unit cost (€/u)**	**Units**	**Cost (€)**
Single sided copper PCB	5.21	1	5.21
TLC2272 precision dual opamp	1.26	2	2.52
WR7808 5 V voltage regulator	0.47	1	0.47
3 mm red LED	0.18	1	0.18
Resistor 22k (1%)	0.05	6	0.30
Resistor 20k (5%)	0.01	1	0.01
Resistor 4k7 (5%)	0.01	1	0.01
Resistor 1k (5%)	0.01	1	0.01
Potentiometer 5k	0.37	2	0.74
Potentiometer 10k	0.35	1	0.35
Potentiometer 50k	0.35	1	0.35
Electrolytic capacitor 10u (16 V)	0.13	3	0.39
Plastic capacitor 100n (16 V)	0.05	5	0.25
Plastic capacitor 1n (16 V)	0.05	2	0.10
Female header	0.25	1	0.25
Lever switch	1.23	1	1.23
Tin soldering wire	2.30	1	2.30
0.8 mm drill bit	2.79	1	2.79
		TOTAL (€)	**12.00**

Table A.3: Circuit under test costs.

voltmeters,... All these equipment amortization costs can be checked in Table A.5.

For the calculations, a 10% increment over the price has been considered as a maintenance cost for equipment and as an aging cost for software tools.

The software appearing in Table A.5 is not the unique software that have been used. Many resources come from free software tools such as Linux, Spice, Perl, Maxima, Octave, Bash, LaTeX,...

Item	Unit cost (€/u)	Units	Cost (€)
PLL board EVAL-ADF411XEB1	130.55	1	130.55
Synthesiser ADF4112 for PLL board	5.24	1	5.24
Voltage controlled oscillator VCO1901960T	27.63	1	27.63
Shipping costs	66.24	–	66.24
Tin soldering wire	2.30	1	2.30
		TOTAL (€)	**231.96**

Table A.4: PLL evaluation board costs.

Item	Price (€)	Life (h)	Amort (€/h)	Time (h)	Cost (€)
TDS744A scope	4795	10000	0.53	80	42.20
AFG3102 funcgen	5110	10000	0.56	80	44.97
HP4284A supply	8982	10000	0.99	80	79.04
Multimeter	30	10000	0.00	80	0.26
Soldering iron	50	8000	0.01	5	0.03
PC	700	30000	0.03	3000	77.00
Laptop PC	900	20000	0.05	150	7.43
MS Windows XP	150	15000	0.01	3000	33.00
Cadence IC Design	2000	10000	0.22	1000	220.00
OrCAD	1495	15000	0.11	100	10.96
MATLAB	515	15000	0.04	2000	75.53
Maple	1895	15000	0.14	200	27.79
				TOTAL (€)	**618.22**

Table A.5: Equipment and software amortization costs.

A.5. Other Costs

During the development of the project, papers on the topic have published in different test and circuit design conferences such as European Tests Symposium (ETS) and Design of Circuits and Integrated Systems Conference (DCIS). In Table A.6 can be seen an overview

of the generated costs. They include the travel, the lodging and the conference fees.

Item	**Cost per person (€)**	**No. of people**	**Cost (€)**
ETS09 Symposium	589	2	1178
DCIS09 Conference	415	3	1245
		TOTAL (€)	**2423**

Table A.6: Other project related costs.

A.6. Overall Project Costs

In the previous sections, the breakdown of the costs related to the project have been exposed. The overall project economic evaluation yields from the summation of the partial costs found in each table. Table A.7 summarises the total costs of carrying out the presented project. The final cost rise up to 80342.24 €.

Item	**Cost (€)**
Human resources	67400.00
Chip fabrication	9500.00
Test bench	157.06
Circuit under test	12.00
PLL evaluation board	231.96
Equipment and software	618.22
Other	2423.00
TOTAL PROJECT COST (€)	**80342.24**

Table A.7: Overall project costs.

Appendix B

Environmental Impact Assessment

The proposed test and diagnosis methodology has been possible due the fabrication of a 65 nm multiproject chip using a bulk CMOS process. CMOS circuits fabrication demands many different chemical products utilisation in each process stage. The foundry cares about the recycling of the products and their correct usage in order to avoid extreme environmental damage.

The designed circuit is aimed to be used in buit-in testing techniques, what simplifies the test procedure in area, power and time consuming aspects. The overall advantage is seen in a considerably smaller price of the test. BIST techniques are considered DFT (design for testability) offering a great bunch of benefits as mentioned. DFT designs assure quality at a low price level due to the easier way the test is performed.

From the power consumption point of view, the fabricated monitor circuit draws only a few milliamps. For the first stage, which is basically analog, considering an average voltage of $V_{\mathrm{GS}} = 0.7$ V and $V_{\mathrm{DS}} = 0.5$ V for the input transistors, the total first stage current, I_{FIRST}, can be roughly computed by,

$$I_{\mathrm{FIRST}} = 4 \cdot 199.03 \cdot 10^{-6} \frac{1800}{180} (0.7 - 0.315)^2 (1 + 0.176 \cdot 0.5) \approx 1.3 \text{ mA} \qquad \text{(B.1)}$$

The core voltage supply is 1 V, what yields a total power consumption of about 1.3 mW. The second stage consumption can be attributed to the branches that operate in saturation

(trimodular second stage), so $I_{\mathrm{SECOND}} = \frac{3}{4} I_{\mathrm{FIRST}}$. Then, the resulting total power consumption is about $P_{\mathrm{TOT}} \approx 2.3$ mW, what is a quite small value compared to those consumed by an AATE (analog automatic test equipment).

On the hand of final physical assemble and verification, the developed test bench and CUT circuits have been made using discrete electronic components being compliant with the RoHS[1] (restriction of hazardous substances) policies. This fact guarantees that any component is totally free of hazardous stuff like lead, mercury, cadmium, chromium,...

[1] RoHS directives must be accomplished in Europe since july 2006.

Appendix C

Orthogonal Projection

C.1. Matrix of the Orthogonal Projection

In the following lines, the method for computing the matrix of the orthogonal projection of a given vector over a vectorial subspace will be demonstrated. The method makes extensive usage of linear algebra concepts and, although its apparent complexity, is the most suitable method for computer implementation and high amounts of data. The orthogonal projection computation is used in the leasts squares fitting method.

Let us consider F a vector subspace of a $\mathbb{R}$-vector space $E = \mathbb{R}^n$ ($\dim E = n$). Let $\{v_1, \ldots, v_r\}$ be a base of F ($\dim F = r$).

We note the orthogonal projection of a vector $\omega \in \mathbb{R}^n$ over the subspace F as $\Pi_F(\omega)$. Of course, $\Pi_F(\omega) \in F$ and therefore can be written as a linear combination of the vectors of any base of E this way,

$$\Pi_F(\omega) = \alpha_1 v_1 + \cdots + \alpha_r v_r \tag{C.1}$$

The vector $\Pi_F(\omega) - \omega$ is orthogonal to subspace F, that is $\Pi_F(\omega) - \omega \in F^{\perp}$ as can be seen in Figure C.1 and therefore, it will be for any vector within F. In particular, this will occur with the vectors of the base $v_1, \ldots, v_n$, so,

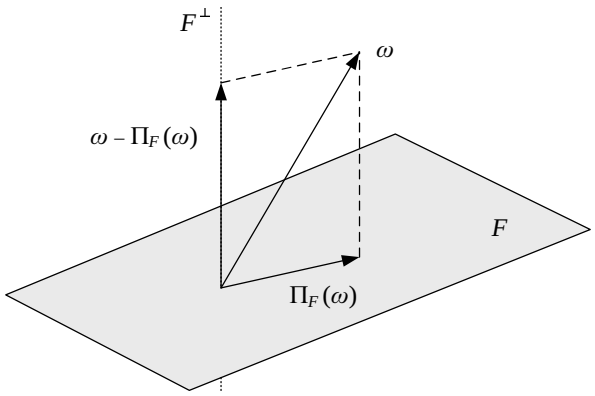


Figure C.1: Sketch of the decomposition of vector ω as the sum of the vector $\Pi_F(\omega) \in F$ and $\omega - \Pi_F(\omega) \in F^{\perp}$.

$$\left.\begin{array}{rcl} \Pi_F(\omega) - \omega & \perp & v_1 \\ \Pi_F(\omega) - \omega & \perp & v_2 \\ & \vdots & \\ \Pi_F(\omega) - \omega & \perp & v_r \end{array}\right\} \tag{C.2}$$

Because of the orthogonal relations written above, the dot product $\langle \cdot, \cdot \rangle$ will yield a zero value,

$$\begin{array}{rcl} \langle v_1, \alpha_1 v_1 + \cdots + \alpha_r v_r - \omega \rangle & = & 0 \\ \langle v_2, \alpha_1 v_1 + \cdots + \alpha_r v_r - \omega \rangle & = & 0 \\ & \vdots & \\ \langle v_r, \alpha_1 v_1 + \cdots + \alpha_r v_r - \omega \rangle & = & 0 \end{array} \tag{C.3}$$

Now, using the bilinearity of the dot product, we get,

$$\begin{aligned} \langle v_1, v_1\rangle\alpha_1 + \langle v_1, v_2\rangle\alpha_2 + \cdots + \langle v_1, v_r\rangle\alpha_r &= \langle v_1, \omega\rangle \\ \langle v_2, v_1\rangle\alpha_1 + \langle v_2, v_2\rangle\alpha_2 + \cdots + \langle v_2, v_r\rangle\alpha_r &= \langle v_2, \omega\rangle \\ &\vdots \\ \langle v_r, v_1\rangle\alpha_1 + \langle v_r, v_2\rangle\alpha_2 + \cdots + \langle v_r, v_r\rangle\alpha_r &= \langle v_r, \omega\rangle \end{aligned} \tag{C.4}$$

The above system can be written as $\Lambda\alpha = \langle v, \omega\rangle$ being Λ the matrix of the dot product. Defining A as the matrix formed by appending the vectors of the base of F in columns, the system is,

$$A^T A\alpha = A^T\omega \tag{C.5}$$

So now, we solve for unknowns α as $\alpha = [A^T A]^{-1}A\omega$ and because of the previous definition of $\Pi_F(\omega) = \alpha_1 v_1 + \cdots + \alpha_r v_r$, the solution to $\Pi_F(\omega)$ is,

$$\Pi_F(\omega) = A[A^T A]^{-1}A\omega \tag{C.6}$$

Where the matrix $A[A^T A]^{-1}A$ is the so called projection matrix over subspace F, $\Pi_F = A[A^T A]^{-1}A$. In fact it is the matrix of the linear application orthogonal projection.

Appendix D

Leasts Squares Fitting Method

The leasts squares method (LSM) is widely used for curve fitting. It takes special interest when trying to numerically compute parameters for a given fitting function commiting the smallest quadratic error. Mainly, the aim of the LSM is to give a solution to a overdetermined system of equations. In this thesis, has been used for transistor DC curves fitting accordingly to the Unified MOSFET model.

The subsequent lines show the derivation of the equations for the LSM in both cases:

- Classical linear leasts squares
- Generalised leasts squares

D.1. Linear Leasts Squares Method

Suppose we have an overdetermined linear system of equations, with no redundant equations, $A_{n\times r}x_r = b_r$, that is, the number of rows is greater than the number of columns ($n > r$). We will be also assuming that the columns of $A = (v_1 \mid \cdots \mid v_r)$, are linearly independent, so they are the base for a subvectorial space $F \in \mathbb{R}^n$ ($\dim F = r$). The original system can be rewritten as,

$$x_1 v_1 + \cdots + x_r v_r = b \tag{D.1}$$

So, if the previous equation has no solution, means that do not exist scalar values $\{x_1, \ldots, x_r\}$ such make the writting of vector b as a linear combination of vectors $\{v_1, \ldots, v_r\}$.

Now, we can substitute vector b by another b' which lays in the subspace generated by $v_1, \ldots, v_r$. The most reasonable vector to use is that which is the nearest from b. So b' should be the orthogonal projection of b over the generated subspace $v_1, \ldots, v_r$.

$$Ax = A(A^T A)^{-1} A^T b \tag{D.2}$$

Left multiplying by A^T and then by $(A^T A)^{-1}$ immediately yields the solution to the original system of equations by the linear leasts squares method,

$$x = (A^T A)^{-1} A^T b \tag{D.3}$$

D.2. Generalised Leasts Squares Method

The generalised LSM is a generalization of the linear leasts squares method to non-linear systems of equations. MOSFET drain current behaviour is governed by a quadratic law, what difficults the use of linear LSM. The generalised method using first order approximation suits perfectly to the needs of the fitting.

Suppose we have an overdetermined system of r non-redundant and non-linear equations of n variables ($r > n$),

$$\left.\begin{array}{rcl} F_1(x_1, \ldots, x_n) & = & 0 \\ & \vdots & \\ F_r(x_1, \ldots, x_n) & = & 0 \end{array}\right\} \tag{D.4}$$

Abbreviately, this system can be rewritten as a function of n variables mapping to an r dimension vector, $F : \mathbb{R}^n \longrightarrow \mathbb{R}^r$. This function can be approximated in the surroundings of a given point $X_0 \in \mathbb{R}^n$ with a first order multi-variate Taylor polynomial,

$$F(X_0) + J \underbrace{(X - X_0)}_{\Delta X} = 0 \tag{D.5}$$

Where J is the Jacobian matrix or first derivative matrix, defined as,

$$J = \begin{pmatrix} \frac{\partial F_1}{\partial x_1} & \cdots & \frac{\partial F_1}{\partial x_n} \\ \vdots & \ddots & \vdots \\ \frac{\partial F_r}{\partial x_1} & \cdots & \frac{\partial F_r}{\partial x_n} \end{pmatrix} \tag{D.6}$$

The approximation can be rewritten as $J\Delta X = -F(X_0)$, which has the form of the previously studied linear system and LSM can be applied as demonstrated before. The system to solve, having projected the term $-F(X_0)$ over the subvectorial space generated by the columns of J is $J\,\Delta X = J\left[J^T J\right]^{-1} J^T$, and therefore, the solution,

$$X = X_0 - \left[J^T J\right]^{-1} J^T F(X_0) \tag{D.7}$$

Applying the method iteratively, the following recursion relation gives the solution to the system using the leasts squares fitting method,

$$X_{k+1} = X_k - \left[J^T J\right]^{-1} J^T F(X_k) \tag{D.8}$$

So the solution for the fitting parameters can be obtained by just evaluating the functions and its first derivative matrix and performing some simple matrix algebra. The method has been implemented in MATLAB.

Appendix E

Estimation of Population Standard Deviation using Sample Data

Once an integrated circuit has been designed, it is usual to check its behaviour against PVT variations through the use of statistical technology characterization methods. The number of Monte Carlo simulations to perform is critical. It has to be sufficiently large to ensure a good coverage of the process variations and should not be that large to unnecessary delay the simulations.

Many of the parameter variations in integrated circuits behave as a normal distribution $N(\mu, \sigma)$. This fact implies that the distribution itself is totally defined by two parameters: the population mean (μ) and the population standard deviation (σ). Although this simple approach, it is not easy to obtain these values from the technology files provided by the manufacturer because of their inherit complexity. They involve large sets of parameters and even many times, the user has no documentation available on them.

In order to estimate the population mean and standard deviation, the user performs Monte Carlo simulations. The first of these parameters is relatively easy to extrapolate from the sample obtained by simulation since the sample mean ($\bar{x}$) is an unbiased estimator of population mean[1].

[1]Moreover, almost always, the population mean corresponds to the nominal value set by the user or the value given by a simulation run without enabling process variations.

The estimation of σ is not that easy, so we ask ourselves what is the ideal number of simulations in order to obtain a representative sample of our real circuit behaviour. In other words, accepting a given amount of discrepancy, what is the number of simulations to perform to assure the preestablished confidence levels.

Under the hypothesis of data normality[2], is shown that the statistic $\nu\frac{s^2}{\sigma^2}$ follows a χ^2_ν distribution. Being ν the number of degrees of freedom ($\nu = n-1$) and s^2 and σ^2 the sample and population variances respectively. That is,

$$\nu\frac{s^2}{\sigma^2} \sim \chi^2_\nu, \qquad \sigma^2 \sim \nu\frac{s^2}{\chi^2_\nu} \tag{E.1}$$

So just with that information on the parameter σ^2, confidence intervals can be computed considering a significance α (or confidence $1-\alpha$). Accordingly to Figure E.1 which shows an example χ^2 distribution, the X-coordinates of the left and right tail areas have to be computed.

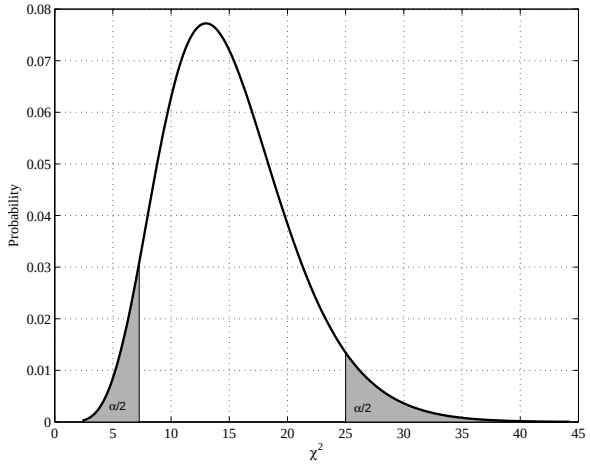


Figure E.1: Example χ^2 distribution with $\nu = 15$ and $\alpha = 0.05$.

The values $\chi^2_{\nu,\frac{\alpha}{2}}$ and $\chi^2_{\nu,1-\frac{\alpha}{2}}$ can be easily calculated with the aid of statistical tables or software[3] tools which provide the *inverse cumulative distribution function* (CDF) of the χ^2 distribution. In consequence, the $1-\alpha$ confidence interval for the population variance is,

[2]Normality tests should be applied, i.e., Anderson-Darling normality test.
[3]In MATLAB and OCTAVE is available the function `chi2inv`.

$$\mathrm{CI}_{1-\alpha}(\sigma^2) = \left[\frac{\nu s^2}{\chi^2_{\nu,1-\frac{\alpha}{2}}}, \frac{\nu s^2}{\chi^2_{\nu,\frac{\alpha}{2}}} \right] \tag{E.2}$$

Rooting the previous expression yields the confidence interval for the population standard deviation, which is more intuitive,

$$\mathrm{CI}_{1-\alpha}(\sigma) = \left[\frac{\sqrt{\nu} s}{\sqrt{\chi^2_{\nu,1-\frac{\alpha}{2}}}}, \frac{\sqrt{\nu} s}{\sqrt{\chi^2_{\nu,\frac{\alpha}{2}}}} \right] \tag{E.3}$$

As the limits of the confidence interval $\mathrm{CI}_{1-\alpha}(\sigma)$ are proportional to s, the following definition involving the lower and upper limits make sense,

$$\mathrm{LL} = \sqrt{\frac{\nu}{\chi^2_{\nu,1-\frac{\alpha}{2}}}}, \qquad \mathrm{UL} = \sqrt{\frac{\nu}{\chi^2_{\nu,\frac{\alpha}{2}}}} \tag{E.4}$$

And therefore, for any set of simulations with sample standard deviation s, the $1-\alpha$ confidence interval for the population standard deviation is,

$$\mathrm{CI}_{1-\alpha}(\sigma) = s\,[\mathrm{LL}, \mathrm{UL}] \tag{E.5}$$

In Figure E.2, several plots for the most common confidences has been plotted as a function of the number of Monte Carlo simulations. Using this graphical data or any other tabulated of software computed, confidence intervals can be generated.

As an example, let us suppose we have performed a set of 70 Monte Carlo Simulations over a circuit and we are interested in the voltage of certain node. Suppose a standard deviation of $s = 12.1$ mV calculated with the data from the 70 simulations and a confidence level of 99% in our decisions. Checking the LL and UL factors in the charts of Figure E.2 we read,

$$\mathrm{LL} = 0.8185, \qquad \mathrm{UL} = 1.2743 \tag{E.6}$$

What allows to determine a confidence interval for the population standard deviation. So we can assert with a confidence of 99% that $\sigma \in [9.9037, 15.4187]$. The designer will decide if this interval (mainly its upper bound) is conservative enough for the circuit being simulated and therefore fabricated.

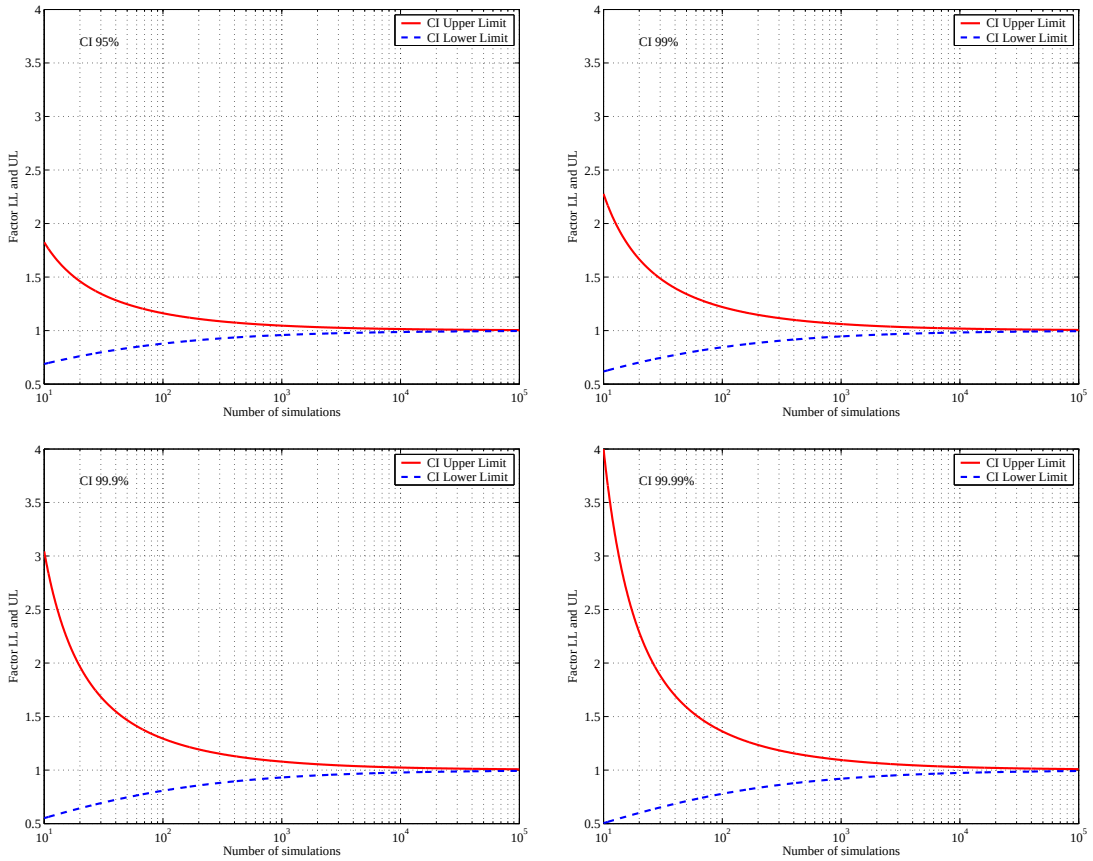


Figure E.2: Plots for LL and UL factors for different number of simulations and confidence intervals of 95%, 99%, 99.9% and 99.99%.

Appendix F

Anderson-Darling Normality Test

The check for normal data is a must in many situations involving statistical analysis. Integrated electronic circuits is a high demanding statistical techniques field and therefore a good exploratory data analysis should contain a normality test among others[1]. Here, the methodology for Anderson-Darling normality test will be exposed.

Let X be a sorted set of n data scalars,

$$X \equiv x_1 \leq x_2 \leq \cdots \leq x_n, \qquad n \geq 7 \tag{F.1}$$

Then, the Anderson-Darling statistic is computed in the following way,

$$\mathrm{AD}^2 = -n - \sum_{k=1}^{n} \frac{2k-1}{n} \ln\left[F(x_k)(1 - F(x_{N+1-k}))\right] \tag{F.2}$$

Where the function $F(t)$ is the normal cumulative distribution function (CDF), defined as,

$$F(t) = \int_{-\infty}^{t} \frac{1}{s\sqrt{2\pi}} e^{-\frac{1}{2}\left(\frac{\tau-\bar{x}}{s}\right)^2} d\tau \tag{F.3}$$

[1] In this work, a MATLAB version of the Anderson-Darling normality test has been implemented.

With $\bar{x}$ and s, the well known sample mean and sample standard deviation,

$$\bar{x} = \frac{1}{n}\sum_{k=1}^{n} x_k, \qquad s = \sqrt{\sum_{k=1}^{n} \frac{(x_k - \bar{x})^2}{n-1}} \tag{F.4}$$

The following step is to correct the Anderson-Darling statistic, mainly if the data set is small. The empirical formula is,

$$\mathrm{ADC}^2 = \mathrm{AD}^2 \left(1 + \frac{0.75}{n} + \frac{2.25}{n^2}\right) \tag{F.5}$$

Using the corrected ADC factor, the p-value can be checked at Table F.1. Given a level of significance α, the p-value reveals the acceptance/rejection of the normality assumption. It is defined as the probability of being wrong if the null hypothesis (H_0: The data is normal, for our significance test) is rejected. So if $p > \alpha$, we will assume the data is drawn from a Gaussian distribution.

ADC interval	p-value
$0 \leq \mathrm{ADC}^2 < 0.2$	$p = 1 - \exp\left[-223.73(\mathrm{ADC}^2)^2 + 101.14(\mathrm{ADC}^2) - 13.436\right]$
$0.2 \leq \mathrm{ADC}^2 < 0.34$	$p = 1 - \exp\left[-59.938(\mathrm{ADC}^2)^2 + 42.796(\mathrm{ADC}^2) - 8.318\right]$
$0.34 \leq \mathrm{ADC}^2 < 0.6$	$p = \exp\left[-1.38(\mathrm{ADC}^2)^2 - 4.279(\mathrm{ADC}^2) + 0.9177\right]$
$0.6 \leq \mathrm{ADC}^2 \leq 13$	$p = \exp\left[0.0186(\mathrm{ADC}^2)^2 - 5.709(\mathrm{ADC}^2) + 1.2937\right]$

Table F.1: p-value for Anderson-Darling statistic.

Appendix G

PLL Board Passive Filter

The purchased PLL evaluation board comes with no pre-soldered filter. This fact allows the user to design his own by varying the components on a given filter topology (see Figure G.1). The components (SMD package) can also be calculated with the aid of Analog Devices PLL simulation tool, ADIsimPLL.

In order to determine the type of the filter topology, its transfer function has been derived considering as input variables voltage and current. In both cases, the output variable is voltage.

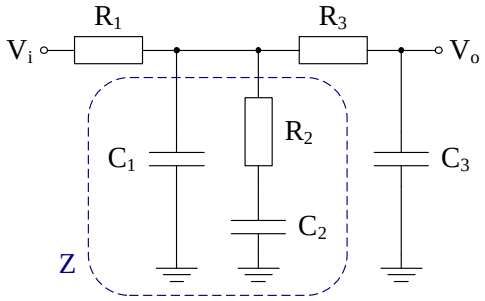


Figure G.1: Default passive filter implementation for PLL evaluation board. The components can be rapidly computed by ADIsimPLL software.

G.1. Voltage-Voltage Transfer Function

In Figure G.1, the C_1 and R_2, C_2 branches can be simplified to a single impedance $Z = \left(\frac{1}{sC_1}\right) \parallel \left(R_2 + \frac{1}{sC_2}\right)$. The resulting value, after rearranging terms, is,

$$Z = \frac{1 + sR_2C_2}{s(C_1 + C_2 + sR_2C_1C_2)} \tag{G.1}$$

Now, by substituting the two branches by their equivalent impedance, schematic of Figure G.2 is obtained. The analysis of this circuit is pretty simple if Thévenin's theorem is applied to simplify resistor R_1 and the newly computed Z as Figure G.3 shows.

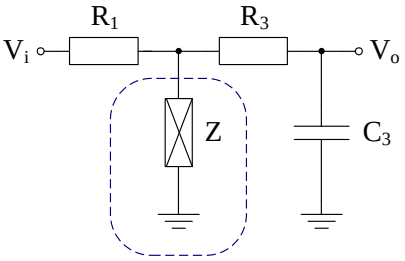


Figure G.2: Passive filter schematic with equivalent impedance Z.

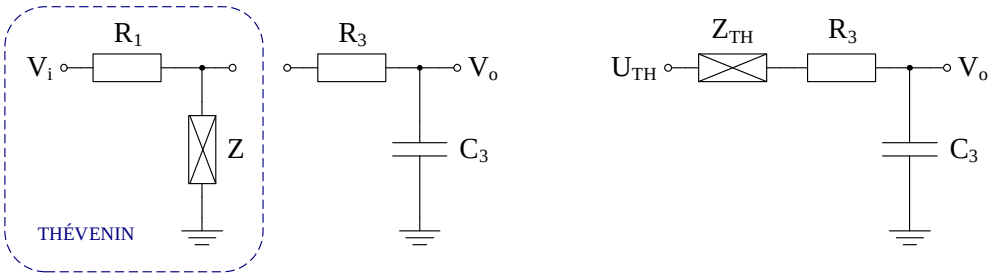


Figure G.3: Passive filter simplification using Thévenin's theorem.

Thévenin's voltage source matches the voltage between R_1 and Z, which form a voltage divider, $U_{\text{TH}} = \frac{Z}{R_1+Z} V_i$. Thévenin's equivalent impedance is the impedance seen once the input source has been shorted to ground, that is the parallel association of R_1 and Z, $Z_{\text{TH}} = \frac{R_1 Z}{R_1+Z}$.

Schematic on the right of Figure G.3 shows that the relation of V_o and V_i is again determined by a voltage divider, so recalling $H = \frac{V_o}{V_i}$ and taking into account the previous Thévenin parameters, one can write,

$$H(s) = \frac{\frac{1}{sC_3}}{R_3 + Z_{\text{TH}} + \frac{1}{sC_3}} \frac{Z}{R_1 + Z} \tag{G.2}$$

From where the transfer function characteristic of the filter can be derived in terms of the original components. Substituting Z with its value, as well as Z_{TH} and doing some easy but tedious math, yields,

$$H(s) = \frac{1 + sR_2C_2}{sR_1C_2(1 + sR_3C_3) + sR_1C_3(1 + sR_2C_2) + (1 + sR_1C_1)(1 + sR_2C_2)(1 + sR_3C_3)} \tag{G.3}$$

G.2. Current-Voltage Transfer Function

The PLL evaluation board operates with a current pump which injects it into the filter. Because of this, an alternate transfer function study is required considering current as the input variable.

Now, the situation is similar to the previously presented case. In Figure G.4 can be checked that branches containing capacitor C_1 and the series R_2 and C_2 can be simplified as done before. The resulting equivalent impedance is Z (see Equation (G.1)).

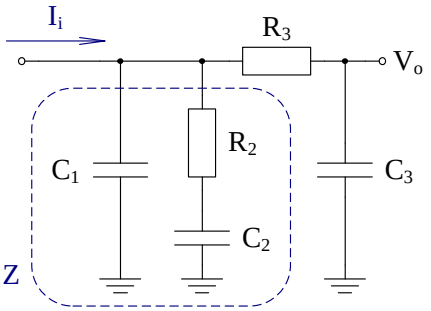


Figure G.4: Default passive filter implementation for PLL evaluation board considering input current as the input variable.

Substituting the three components by Z, the left schematic on Figure G.5 is achieved. The current source in parallel with impedance Z is in Norton's form, so can be redrawn in Thénenin's form as in the right hand side of the same figure.

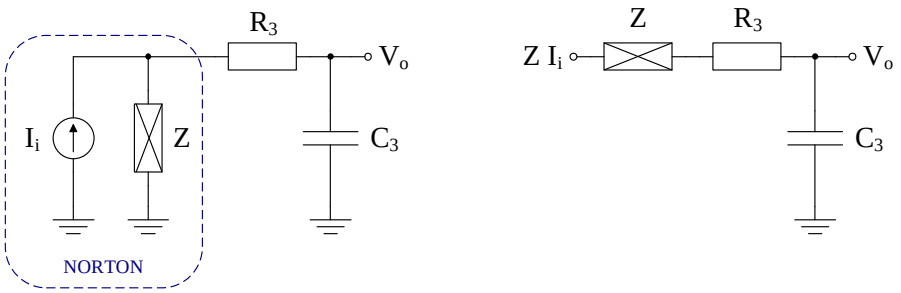


Figure G.5: Passive filter simplification using the equivalence of Thévenin and Norton's theorem parameters, $Z = Z_{\mathrm{TH}} = Z_{\mathrm{N}}$, $U_{\mathrm{TH}} = ZI_{\mathrm{N}}$.

Once again, the output voltage is just the result of a voltage divider with input ZI_i. Now, recalling $H = \frac{V_o}{I_i}$, the transfer function is,

$$H(s) = \frac{\frac{1}{sC_3}}{Z + R_3 + \frac{1}{sC_3}} \tag{G.4}$$

After the substitution of Z by its value and some arrangements on the denominator of $H(s)$, the following current-voltage transfer function is achieved,

$$H(s) = \frac{1 + sR_2C_2}{s\left(C_2(1 + sR_3C_3) + C_3(1 + sR_2C_2) + C_1(1 + sR_2C_2)(1 + sR_3C_3)\right)} \tag{G.5}$$

Appendix H

Matlab Codes

```
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%%%%% main matlab code in order to generate %%%%%%%%%%%%%%%
%%%%% the lissajous compositions and signatures %%%%%%%%%%%
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

clear;
clc;

path(path,'../scripts');
path(path,'../datos');

% entradas
Ai=[.3 .2];
fi=[5e3 10e3];

% para dcis 2010
Ai=[.2];
fi=[12753.19];

% fi=[15e3 10e3]; % enteros!!!
% Ai=[.22 .15]; % .2 primero
% fi=[5e3 10e3];

% una q varia mucho en longitud
% Ai=[.2 .1 .15 .1];
% fi=[20e3 10e3 15e3 5e3];
```

```
% dan una Lissajous bastante larga
% Ai=[.2 .3];
% fi=[25e3 10e3];

% interesante
% Ai=[.1 .25 .15];
% fi=[20e3 10e3 5e3];

% caracteristicas filtro
tipo_filtro='LP';
GAIN=1;
f0=10e3;
Q=.4;

Npuntos=1000;
Voffset=[.5 .5];

ruido=0.15/3;
ruido=0;

% curvas a utilizar
curvas=[10 20 31 41 51 61];
% curvas=[10 20 30 40 50 60 11 21 31 41 51 61];
% curvas=[10 20 31];
% curvas=[10 20];

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

defecto=1.1;
% nom='minus10';

[Ao1 phi1 T1 t1 xlis1 ylis1 signaturas1 instantes1 codificado1]= ...
    calcular_info(Ai,fi,tipo_filtro,f0,GAIN,Q,Npuntos,Voffset,curvas,ruido*0);
[Ao2 phi2 T2 t2 xlis2 ylis2 signaturas2 instantes2 codificado2]= ...
    calcular_info(Ai,fi,tipo_filtro,f0*defecto,GAIN,Q,Npuntos,Voffset,curvas,ruido);

yy1=[codificado1 codificado1(end)];
yy2=[codificado2 codificado2(end)];
[t resu1 resu2 hamm]= ...
    calcular_diferencias(instantes1,yy1,instantes2,yy2);

if length(hamm)==1
```

```
  hamm=hamm*ones(1,length(t)-1);
end

discrepancia=sum(diff(t).*hamm);
discrepanciaN=discrepancia/mean([T1 T2]);

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

figure(1); clf;
axis([0 1 0 1]);
axis square;
hold on;
grid on;
box on;

plot(10,10,'b-','LineWidth',2);
plot(10,10,'r--','LineWidth',2);
legend('Golden','f_0 10% shift','Location','NorthWest');

numeros=floor(curvas/10);
tipos=curvas-numeros*10;

for k=1:length(curvas)
  numero=numeros(k);

  if tipos(k)
    tipo='e';
  else
    tipo='d';
  end

  [x y]=leer_contorno(['c' num2str(numero) tipo '_0' '.dat']);
  plot(x,y,'k');
end

plot(xlis1,ylis1,'b-','LineWidth',2);
plot(xlis2,ylis2,'r--','LineWidth',2);

tam=.05;
px=[xlis1(1) xlis1(1)+(xlis1(2)-xlis1(1))/sqrt((xlis1(2)-xlis1(1))^2+(ylis1(2)-ylis1(1))^2)*tam];
py=[ylis1(1) ylis1(1)+(ylis1(2)-ylis1(1))/sqrt((xlis1(2)-xlis1(1))^2+(ylis1(2)-ylis1(1))^2)*tam];
line(px,py,'Color','g','LineWidth',2);
plot(xlis1(1),ylis1(1),'sg');
```

```
title('Lissajous Curves and Control Lines');
xlabel('Vin (V)');
ylabel('Vout (V)');

% codificar(curvas,0);

adecuar_texto;

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

figure(2); clf;

subplot(2,1,1);
hold on;
grid on;
box on;

stairs(instantes1*1e6,[codificado1 codificado1(end)],'b','LineWidth',2);
stairs(instantes2*1e6,[codificado2 codificado2(end)],'r');
legend('Golden','Defect');

title('Coded Signatures');
xlabel('Time (us)');
ylabel('Decimal coded value');
adecuar_texto;

subplot(2,1,2);
hold on;
grid on;
box on;

stairs(t*1e6,[hamm hamm(end)],'k');

% filtrando...
% nn=4;
% hammfil=filter(ones(1,nn)/nn,1,hamm);

hammfil=hamm;

for kk=3:length(hamm)
  if hamm(kk-2)==hamm(kk)
    hammfil(kk-1)=hamm(kk);
  else
    hammfil(kk-1)=hamm(kk-1);
```

```
  end
end

% la hamming filtrada
% stairs(t*1e6,[hammfil hammfil(end)],'m');
hamm=hammfil;

discrepancia=sum(diff(t).*hamm);
discrepanciaN=discrepancia/mean([T1 T2])
% end filtrando...

a=axis;

if a(4)==1
  a(4)=2;
  axis(a);
end

title('Hamming Distance');
xlabel('Time (us)');
ylabel('Hamming distance');
adecuar_texto;

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

disp(['Filter type: ' tipo_filtro ' (2nd order)']);
disp(['Filter characteristic frequency (kHz): ' num2str(f0*1e-3)]);
disp(['Filter gain: ' num2str(GAIN)]);
disp(['Filter quality factor: ' num2str(Q)]);

disp(['Input amplitudes (V): ' num2str(Ai)]);
disp(['Input frequencies (kHz): ' num2str(fi*1e-3)]);

disp(['Periods (us): ' num2str([T1 T2]*1e6)]);
disp(['Num. of control lines: ' num2str(length(curvas))]);
disp(['Signatures set length: ' num2str([size(signaturas1,1)-1 size(signaturas2,1)-1])]);

disp(['Discrepancy factor: ' num2str(discrepancia)]);
disp(['Discrepancy factor normalized with period: ' num2str(discrepanciaN)]);
disp(['Maximum Hamming distance: ' num2str(max(hamm))]);

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
```

```
% figure(1);
% print('-dpng',['liss_' nom '.png']);
% figure(2);
% print('-dpng',['chron_' nom '.png']);

figure(1);

grid on;

% for k=[1 2 3 4 5]
%   disp(k);
%   h=gtext(num2str(k));
%   set(h,'FontName','Times','FontSize',16,'FontWeight','Bold');
% end

length(signaturas1)
length(signaturas2)

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

fid=fopen('salida.dat','w');

fprintf(fid,'LA SIGNATURA GOLDEN (bin y dec), LONG=%d\n',size(signaturas1,1)-1);

for k=1:length(signaturas1)
  s=sprintf('%d',signaturas1(k,:));
  r=sprintf('%s (%d)',s,bin2dec(s));
  fprintf(fid,'%s\n',r);
end

fprintf(fid,'\n');
fprintf(fid,'LA SIGNATURA DEFECTO (bin y dec), LONG=%d\n',size(signaturas2,1)-1);

for k=1:length(signaturas2)
  s=sprintf('%d',signaturas2(k,:));
  r=sprintf('%s (%d)',s,bin2dec(s));
  fprintf(fid,'%s\n',r);
end

fclose(fid);

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%%%%% function to compute different info %%%%%%%%%%%%%%%%%%
```

```
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

function [Ao phi T tlis xlis ylis signaturas instantes codificado]=
   calcular_info(Ai,fi,tipo_filtro,f0,GAIN,Q,Npuntos,Voffset,curvas,ruido)

[Ao phi]=calcular_respuesta(tipo_filtro,GAIN,f0,Q,Ai,fi);

T=calcular_periodo(fi);
tlis=linspace(0,T,Npuntos);

[xlis ylis]=calcular_lissajous(Ai,fi,Ao,phi,tlis,Voffset);

% noise
ylis=ylis+ruido*randn(size(ylis));
ylis=ylis+ruido*sin(2*pi*1e6*tlis);

m=calcular_matriz(curvas,xlis,ylis);

[signaturas filtro]=reducir_matriz(m);
instantes=[tlis(filtro) T];

codificado=(signaturas*2.^(length(curvas)-1:-1:0)')';

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%%%%% function to compute the differences between %%%%%%%%%
%%%%% the signatures %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

function [t resu1 resu2 hamm]=calcular_diferencias(x1,y1,x2,y2)

t=unique([x1 x2]);

resu1=[];
resu2=[];

for k=1:length(t)-1
  tc=mean(t(k:k+1));

  z1=find(x1<tc);
  resu1=[resu1 y1(z1(end))];

  z2=find(x2<tc);
  resu2=[resu2 y2(z2(end))];
end
```

```
tt=bitxor(resu1,resu2);
hamm=sum((dec2bin(tt)=='1')');

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%%%% function to adequate the text of the plots %%%%%%%%%%
%%%% and get it ready for pretty printing %%%%%%%%%%%%%%%%
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

function adecuar_texto

tamanofuente=12;

% para los valores de los ejes
set(gca,'FontSize',tamanofuente);
set(gca,'FontName','Times');

% para las etiquetas de los ejes
for conta=1:3
  switch conta
   case 1
    eti='xlabel';
   case 2
    eti='ylabel';
   case 3
    eti='zlabel';
  end

  hand=get(gca,eti);
  set(hand,'FontSize',tamanofuente);
  set(hand,'FontName','Times');
end

% para el titulo
hand=get(gca,'title');
set(hand,'FontSize',tamanofuente+2);
set(hand,'FontName','Times');
set(hand,'FontWeight','Bold');

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%%%% function to obtain the frequency response %%%%%%%%%%
%%%% of the CUT (biquad filter) %%%%%%%%%%%%%%%%%%%%%%%%%
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
```

```
function [Ao phi]=calcular_respuesta(tipo,GAIN,f0,Q,Ai,fi)

denominador=(1-fi.^2/f0^2)+1/Q*fi/f0*j;

switch tipo
 case 'LP'
  numerador=GAIN;
 case 'BP'
  numerador=GAIN*1/Q*fi/f0*j;
 case 'SB'
  numerador=GAIN*(1-fi.^2/f0^2);
 case 'HP'
  numerador=-GAIN*fi.^2/f0^2;
end

H=numerador./denominador

Ao=abs(H);
phi=angle(H);

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%%%%% function to compute the period of the %%%%%%%%%%%%%%%
%%%%% multitone lissajous curve %%%%%%%%%%%%%%%%%%%%%%%%%%%
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

function resu=calcular_periodo(f)

f=floor(f);
D=mcm(f);
resu=mcm(D./f)/D;

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%%%%% function to compute the x and y components %%%%%%%%%%
%%%%% of the lissajous curve %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

function [x y]=calcular_lissajous(Ai,fi,Ao,phi,t,Voff)

x=zeros(1,length(t))+Voff(1);
y=zeros(1,length(t))+Voff(2);

for k=1:length(Ai)
  x=x+Ai(k)*sin(2*pi*fi(k)*t);
  y=y+Ai(k)*Ao(k)*sin(2*pi*fi(k)*t+phi(k));
```

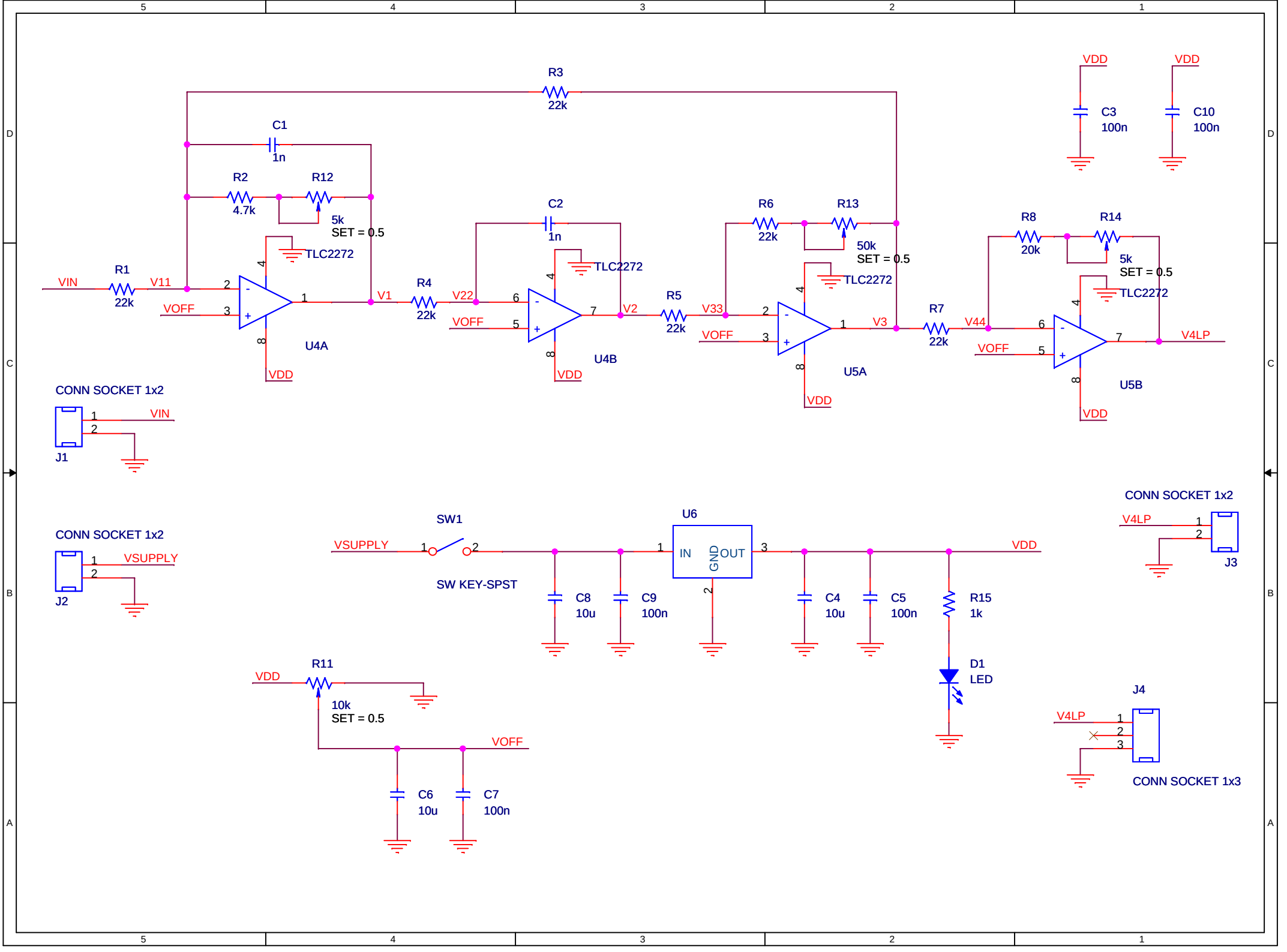
```
end

if max(x)>1 || max(y)>1 || min(x)<0 || min(y)<0
  disp('ATENCION: Datos fuera de rango 0-1');
end

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%%%%% function to compute the lcm of a given vector %%%%%%%
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

function resu=mcm(x)

N=length(x);

resu=1;

for k=1:N
  resu=lcm(resu,x(k));
end
```

Appendix I

Extra Stuff

I.1. Datasheets

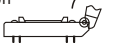
I.2. Published Papers


R3
22k
C1
1n
R2
4.7k
R12
5k
SET = 0.5
TLC2272
R1
22k
VIN
V11
VOFF
U4A
VDD
R4
22k
V1
V22
C2
1n
TLC2272
U4B
R5
22k
V2
V33
R6
22k
R13
50k
SET = 0.5
TLC2272
U5A
R7
22k
V3
V44
R8
20k
R14
5k
SET = 0.5
TLC2272
U5B
V4LP
C3
100n
C10
100n
CONN SOCKET 1x2
J1
VIN
CONN SOCKET 1x2
J2
VSUPPLY
SW1
SW KEY-SPST
U6
IN
GND
OUT
C8
10u
C9
100n
C4
10u
C5
100n
R15
1k
D1
LED
CONN SOCKET 1x2
J3
V4LP
R11
10k
SET = 0.5
C6
10u
C7
100n
J4
CONN SOCKET 1x3

IC51 Series (Clamshell)

Quad Flat Package (QFP, PQFP, TQFP)

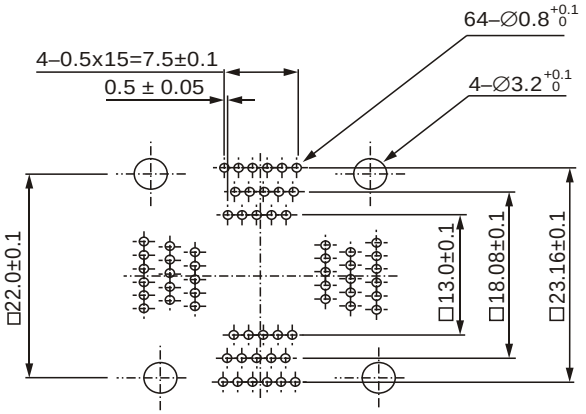
Socket & PCB Orientation



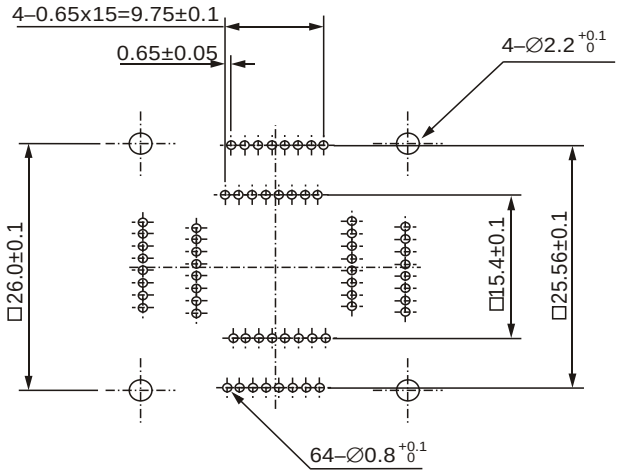
Top View from Socket

Recommended PCB Layouts (64 pins)

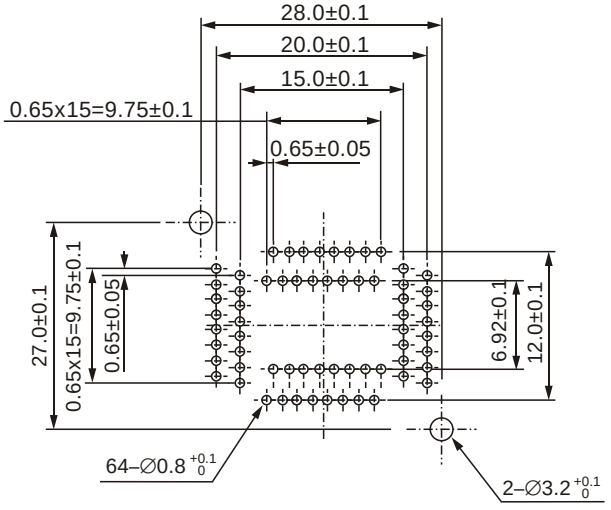
64 pins — IC51-0644-807



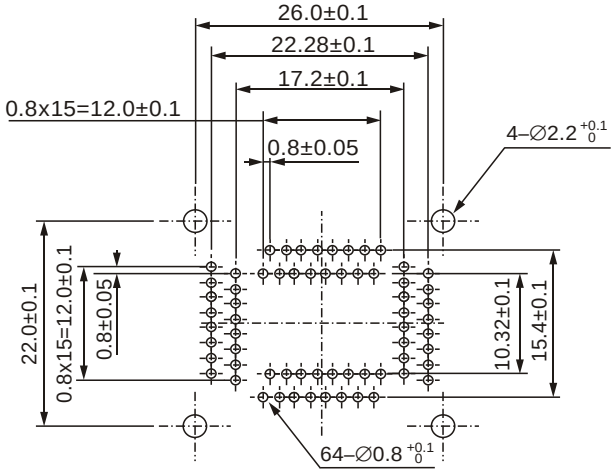
64 pins — IC51-0644-1586



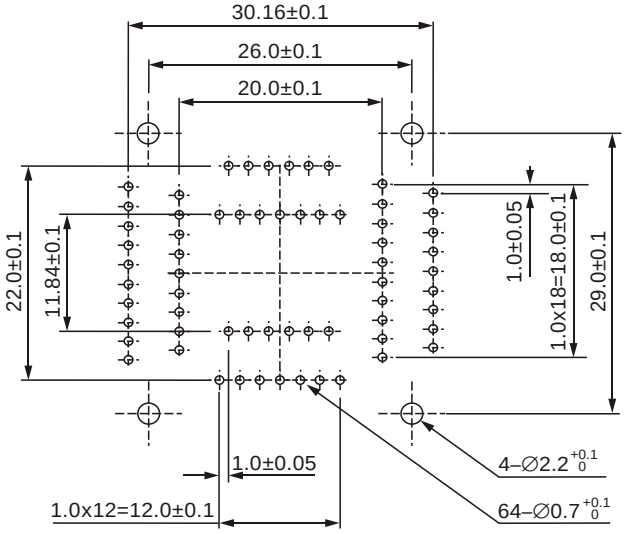
64 pins — IC51-0644-1602



64 pins — IC51-0644-824-1 / IC51-0644-824-2 / IC51-0644-824-3 / IC51-0644-692-*



64 pins — IC51-820-2.KS-9376 / IC51-0644-820-1 / IC51-0644-820-2 / IC51-0644-820-3 / IC51-0644-820-4 / IC51-0644-472



YAMAICHI ELECTRONICS - Munich 089 / 45109-0

RF PLL Frequency Synthesizers

ADF4110/ADF4111/ADF4112/ADF4113

FEATURES

ADF4110: 550 MHz; ADF4111: 1.2 GHz; ADF4112: 3.0 GHz; ADF4113: 4.0 GHz
2.7 V to 5.5 V power supply
Separate charge pump supply (V_P) allows extended tuning voltage in 3 V systems
Programmable dual-modulus prescaler 8/9, 16/17, 32/33, 64/65
Programmable charge pump currents
Programmable antibacklash pulse width
3-wire serial interface
Analog and digital lock detect
Hardware and software power-down mode

APPLICATIONS

Base stations for wireless radio (GSM, PCS, DCS, CDMA, WCDMA)
Wireless handsets (GSM, PCS, DCS, CDMA, WCDMA)
Wireless LANS
Communications test equipment
CATV equipment

GENERAL DESCRIPTION

The ADF4110 family of frequency synthesizers can be used to implement local oscillators in the upconversion and downconversion sections of wireless receivers and transmitters. They consist of a low noise digital PFD (phase frequency detector), a precision charge pump, a programmable reference divider, programmable A and B counters, and a dual-modulus prescaler (P/P + 1). The A (6-bit) and B (13-bit) counters, in conjunction with the dual-modulus prescaler (P/P + 1), implement an N divider (N = BP + A). In addition, the 14-bit reference counter (R counter) allows selectable REFIN frequencies at the PFD input. A complete phase-locked loop (PLL) can be implemented if the synthesizer is used with an external loop filter and voltage controlled oscillator (VCO).

Control of all the on-chip registers is via a simple 3-wire interface. The devices operate with a power supply ranging from 2.7 V to 5.5 V and can be powered down when not in use.

FUNCTIONAL BLOCK DIAGRAM

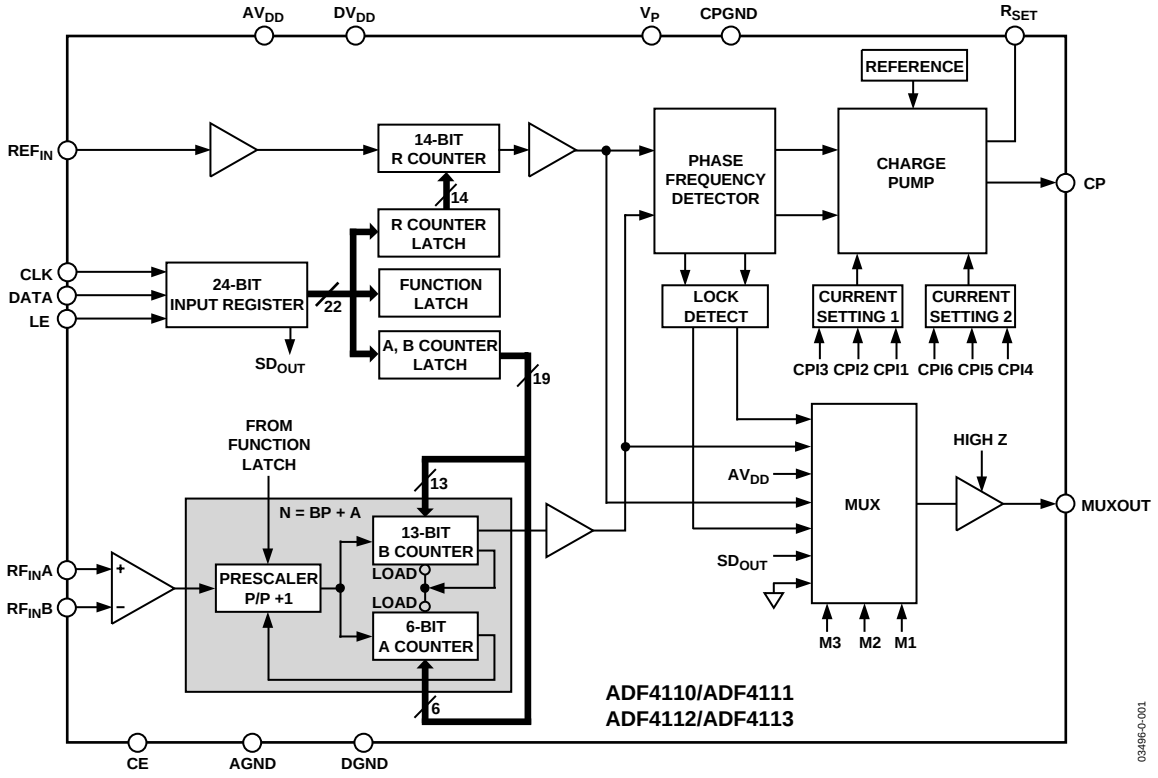


Figure 1. Functional Block Diagram

Rev. C

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REVISION HISTORY

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3/03—Data sheet changed from Rev. A to Rev. B.

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1/01—Data sheet changed from Rev. 0 to Rev. A.

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SPECIFICATIONS

AV_{DD} = DV_{DD} = 3 V ± 10%, 5 V ± 10%; $AV_{DD} \leq V_P \leq$ 6.0 V; AGND = DGND = CPGND = 0 V; R_{SET} = 4.7 kΩ; dBm referred to 50 Ω; T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Operating temperature range is as follows: B Version: −40°C to +85°C.

Table 1.

Parameter	B Version	B Chips[1]	Unit	Test Conditions/Comments
RF CHARACTERISTICS (3 V)				See Figure 29 for input circuit.
RF Input Sensitivity	−15/0	−15/0	dBm min/max	
RF Input Frequency				
ADF4110	80/550	80/550	MHz min/max	For lower frequencies, ensure slew rate (SR) > 30 V/µs.
ADF4110	50/550	50/550	MHz min/max	Input level = −10 dBm.
ADF4111	0.08/1.2	0.08/1.2	GHz min/max	For lower frequencies, ensure SR > 30 V/µs.
ADF4112	0.2/3.0	0.2/3.0	GHz min/max	For lower frequencies, ensure SR > 75 V/µs.
ADF4112	0.1/3.0	0.1/3.0	GHz min/max	Input level = −10 dBm.
ADF4113	0.2/3.7	0.2/3.7	GHz min/max	Input level = −10 dBm. For lower frequencies, ensure SR > 130 V/µs.
Maximum Allowable Prescaler Output Frequency[2]	165	165	MHz max	
RF CHARACTERISTICS (5 V)				
RF Input Sensitivity	−10/0	−10/0	dBm min/max	
RF Input Frequency				
ADF4110	80/550	80/550	MHz min/max	For lower frequencies, ensure SR > 50 V/µs.
ADF4111	0.08/1.4	0.08/1.4	GHz min/max	For lower frequencies, ensure SR > 50 V/µs.
ADF4112	0.1/3.0	0.1/3.0	GHz min/max	For lower frequencies, ensure SR > 75 V/µs.
ADF4113	0.2/3.7	0.2/3.7	GHz min/max	For lower frequencies, ensure SR > 130 V/µs.
ADF4113	0.2/4.0	0.2/4.0	GHz min/max	Input level = −5 dBm
Maximum Allowable Prescaler Output Frequency[2]	200	200	MHz max	
REFIN CHARACTERISTICS				
REFIN Input Frequency	5/104	5/104	MHz min/max	For f < 5 MHz, ensure SR > 100 V/µs.
Reference Input Sensitivity	0.4/AV_{DD}	0.4/AV_{DD}	V p-p min/max	AV_{DD} = 3.3 V, biased at AV_{DD}/2. See Note 3.
	3.0/AV_{DD}	3.0/AV_{DD}	V p-p min/max	AV_{DD} = 5 V, biased at AV_{DD}/2. See Note 3.
REFIN Input Capacitance	10	10	pF max	
REFIN Input Current	±100	±100	µA max	
PHASE DETECTOR FREQUENCY[4]	55	55	MHz max	
CHARGE PUMP				
I_{CP} Sink/Source				Programmable (see Table 9).
High Value	5	5	mA typ	With R_{SET} = 4.7 kΩ
Low Value	625	625	µA typ	
Absolute Accuracy	2.5	2.5	% typ	With R_{SET} = 4.7 kΩ
R_{SET} Range	2.7/10	2.7/10	kΩ typ	See Table 9.
I_{CP} 3-State Leakage Current	1	1	nA typ	
Sink and Source Current Matching	2	2	% typ	0.5 V ≤ V_{CP} ≤ V_P − 0.5 V.
I_{CP} vs. V_{CP}	1.5	1.5	% typ	0.5 V ≤ V_{CP} ≤ V_P − 0.5 V.
I_{CP} vs. Temperature	2	2	% typ	V_{CP} = V_P/2.
LOGIC INPUTS				
V_{INH}, Input High Voltage	0.8 × DV_{DD}	0.8 × DV_{DD}	V min	
V_{INL}, Input Low Voltage	0.2 × DV_{DD}	0.2 × DV_{DD}	V max	
I_{INH}/I_{INL}, Input Current	±1	±1	µA max	
C_{IN}, Input Capacitance	10	10	pF max	
LOGIC OUTPUTS				
V_{OH}, Output High Voltage	DV_{DD} − 0.4	DV_{DD} − 0.4	V min	I_{OH} = 500 µA.
V_{OL}, Output Low Voltage	0.4	0.4	V max	I_{OL} = 500 µA.

Parameter	B Version	B Chips[1]	Unit	Test Conditions/Comments
POWER SUPPLIES				
AV_{DD}	2.7/5.5	2.7/5.5	V min/V max	
DV_{DD}	AV_{DD}	AV_{DD}		
V_P	AV_{DD}/6.0	AV_{DD}/6.0	V min/V max	$AV_{DD} \le V_P \le 6.0$ V. See Figure 25 and Figure 26.
I_{DD}[5] ($AI_{DD} + DI_{DD}$)				
ADF4110	5.5	4.5	mA max	4.5 mA typical
ADF4111	5.5	4.5	mA max	4.5 mA typical
ADF4112	7.5	6.5	mA max	6.5 mA typical
ADF4113	11	8.5	mA max	8.5 mA typical
I_P	0.5	0.5	mA max	T_A = 25°C
Low Power Sleep Mode	1	1	µA typ	
NOISE CHARACTERISTICS				
ADF4113 Normalized Phase Noise Floor[6]	−215	−215	dBc/Hz typ	
Phase Noise Performance[7]				@ VCO output
ADF4110: 540 MHz Output[8]	−91	−91	dBc/Hz typ	@ 1 kHz offset and 200 kHz PFD frequency
ADF4111: 900 MHz Output[9]	−87	−87	dBc/Hz typ	@ 1 kHz offset and 200 kHz PFD frequency
ADF4112: 900 MHz Output[9]	−90	−90	dBc/Hz typ	@ 1 kHz offset and 200 kHz PFD frequency
ADF4113: 900 MHz Output[9]	−91	−91	dBc/Hz typ	@ 1 kHz offset and 200 kHz PFD frequency
ADF4111: 836 MHz Output[10]	−78	−78	dBc/Hz typ	@ 300 Hz offset and 30 kHz PFD frequency
ADF4112: 1750 MHz Output[11]	−86	−86	dBc/Hz typ	@ 1 kHz offset and 200 kHz PFD frequency
ADF4112: 1750 MHz Output[12]	−66	−66	dBc/Hz typ	@ 200 Hz offset and 10 kHz PFD frequency
ADF4112: 1960 MHz Output[13]	−84	−84	dBc/Hz typ	@ 1 kHz offset and 200 kHz PFD frequency
ADF4113: 1960 MHz Output[13]	−85	−85	dBc/Hz typ	@ 1 kHz offset and 200 kHz PFD frequency
ADF4113: 3100 MHz Output[14]	−86	−86	dBc/Hz typ	@ 1 kHz offset and 1 MHz PFD frequency
Spurious Signals				
ADF4110: 540 MHz Output[9]	−97/−106	−97/−106	dBc typ	@ 200 kHz/400 kHz and 200 kHz PFD frequency
ADF4111: 900 MHz Output[9]	−98/−110	−98/−110	dBc typ	@ 200 kHz/400 kHz and 200 kHz PFD frequency
ADF4112: 900 MHz Output[9]	−91/−100	−91/−100	dBc typ	@ 200 kHz/400 kHz and 200 kHz PFD frequency
ADF4113: 900 MHz Output[9]	−100/−110	−100/−110	dBc typ	@ 200 kHz/400 kHz and 200 kHz PFD frequency
ADF4111: 836 MHz Output[10]	−81/−84	−81/−84	dBc typ	@ 30 kHz/60 kHz and 30 kHz PFD frequency
ADF4112: 1750 MHz Output[11]	−88/−90	−88/−90	dBc typ	@ 200 kHz/400 kHz and 200 kHz PFD frequency
ADF4112: 1750 MHz Output[12]	−65/−73	−65/−73	dBc typ	@ 10 kHz/20 kHz and 10 kHz PFD frequency
ADF4112: 1960 MHz Output[13]	−80/−84	−80/−84	dBc typ	@ 200 kHz/400 kHz and 200 kHz PFD frequency
ADF4113: 1960 MHz Output[13]	−80/−84	−80/−84	dBc typ	@ 200 kHz/400 kHz and 200 kHz PFD frequency
ADF4113: 3100 MHz Output[14]	−80/−82	−82/−82	dBc typ	@ 1 MHz/2 MHz and 1 MHz PFD frequency

[1]The B chip specifications are given as typical values.
[2]This is the maximum operating frequency of the CMOS counters. The prescaler value should be chosen to ensure that the RF input is divided down to a frequency that is less than this value.
[3]AC coupling ensures AV_{DD}/2 bias. See Figure 33 for a typical circuit.
[4]Guaranteed by design.
[5] T_A = 25°C; $AV_{DD} = DV_{DD}$ = 3 V; P = 16; SYNC = 0; DLY = 0; RF_{IN} for ADF4110 = 540 MHz; RF_{IN} for ADF4111, ADF4112, ADF4113 = 900 MHz.
[6] The synthesizer phase noise floor is estimated by measuring the in-band phase noise at the output of the VCO, PN_{TOT}, and subtracting 20logN (where N is the N divider value) and $10\log F_{PFD}$: $PN_{SYNTH} = PN_{TOT} - 10\log F_{PFD} - 20\log N$.
[7] The phase noise is measured with the EVAL-ADF411xEB1 evaluation board and the HP8562E spectrum analyzer. The spectrum analyzer provides the REFIN for the synthesizer (f_{REFOUT} = 10 MHz @ 0 dBm). SYNC = 0; DLY = 0 (Table 7).
[8] f_{REFIN} = 10 MHz; f_{PFD} = 200 kHz; offset frequency = 1 kHz; f_{RF} = 540 MHz; N = 2700; loop B/W = 20 kHz.
[9] f_{REFIN} = 10 MHz; f_{PFD} = 200 kHz; offset frequency = 1 kHz; f_{RF} = 900 MHz; N = 4500; loop B/W = 20 kHz.
[10] f_{REFIN} = 10 MHz; f_{PFD} = 30 kHz; offset frequency = 300 Hz; f_{RF} = 836 MHz; N = 27867; loop B/W = 3 kHz.
[11] f_{REFIN} = 10 MHz; f_{PFD} = 200 kHz; offset frequency = 1 kHz; f_{RF} = 1750 MHz; N = 8750; loop B/W = 20 kHz
[12] f_{REFIN} = 10 MHz; f_{PFD} = 10 kHz; offset frequency = 200 Hz; f_{RF} = 1750 MHz; N = 175000; loop B/W = 1 kHz.
[13] f_{REFIN} = 10 MHz; f_{PFD} = 200 kHz; offset frequency = 1 kHz; f_{RF} = 1960 MHz; N = 9800; loop B/W = 20 kHz.
[14] f_{REFIN} = 10 MHz; f_{PFD} = 1 MHz; offset frequency = 1 kHz; f_{RF} = 3100 MHz; N = 3100; loop B/W = 20 kHz.

TIMING CHARACTERISTICS

Guaranteed by design but not production tested. $AV_{DD} = DV_{DD} = 3\ V \pm 10\%, 5\ V \pm 10\%$; $AV_{DD} \le V_P \le 6\ V$; AGND = DGND = CPGND = 0 V; $R_{SET} = 4.7\ k\Omega$; $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted.

Table 2.

Parameter	Limit at T_{MIN} to T_{MAX} (B Version)	Unit	Test Conditions/Comments
t_1	10	ns min	DATA to CLOCK setup time
t_2	10	ns min	DATA to CLOCK hold time
t_3	25	ns min	CLOCK high duration
t_4	25	ns min	CLOCK low duration
t_5	10	ns min	CLOCK to LE setup time
t_6	20	ns min	LE pulse width

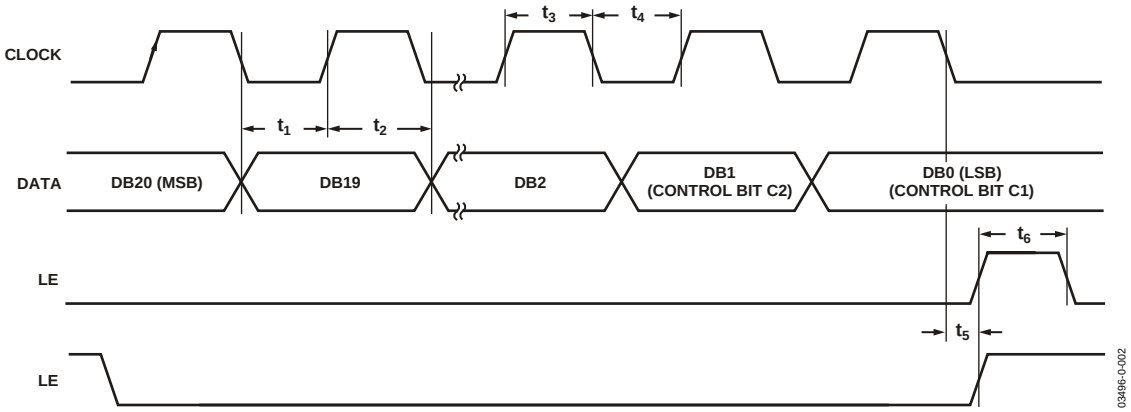

Figure 2. Timing Diagram

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted

Table 3.

Parameter	Rating
AV_{DD} to GND[1]	−0.3 V to +7 V
AV_{DD} to DV_{DD}	−0.3 V to +0.3 V
V_P to GND	−0.3 V to +7 V
V_P to AV_{DD}	−0.3 V to +5.5 V
Digital I/O Voltage to GND	−0.3 V to V_{DD} + 0.3 V
Analog I/O Voltage to GND	−0.3 V to V_P + 0.3 V
REF_{IN}, $RF_{IN}A$, $RF_{IN}B$ to GND	−0.3 V to V_{DD} + 0.3 V
$RF_{IN}A$ to $RF_{IN}B$	±320 mV
Operating Temperature Range	
Industrial (B Version)	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Maximum Junction Temperature	150°C
TSSOP θ_{JA} Thermal Impedance	150.4°C/W
LFCSP θ_{JA} Thermal Impedance (Paddle Soldered)	122°C/W
LFCSP θ_{JA} Thermal Impedance (Paddle Not Soldered)	216°C/W
Lead Temperature, Soldering	
Vapor Phase (60 sec)	215°C
Infrared (15 sec)	220°C

[1] GND = AGND = DGND = 0 V.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device is a high performance RF integrated circuit with an ESD rating of <2 kV, and it is ESD sensitive. Proper precautions should be taken for handling and assembly.

TRANSISTOR COUNT

6425 (CMOS) and 303 (Bipolar).

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

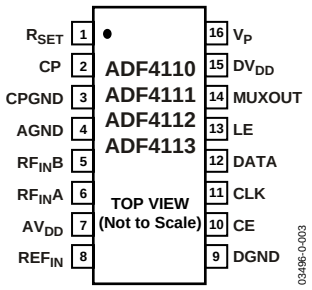

Figure 3. TSSOP Pin Configuration

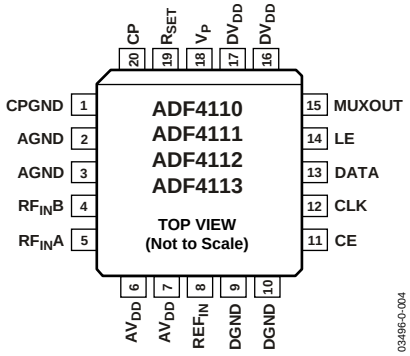

Figure 4. LFCSP Pin Configuration

Table 4. Pin Function Descriptions

TSSOP Pin No.	LFCSP Pin No.	Mnemonic	Function
1	19	R_{SET}	Connecting a resistor between this pin and CPGND sets the maximum charge pump output current. The nominal voltage potential at the R_{SET} pin is 0.56 V. The relationship between I_{CP} and R_{SET} is $I_{CPmax} = \frac{23.5}{R_{SET}}$ So, with R_{SET} = 4.7 kΩ, I_{CPmax} = 5 mA.
2	20	CP	Charge Pump Output. When enabled, this provides ±I_{CP} to the external loop filter, which in turn drives the external VCO.
3	1	CPGND	Charge Pump Ground. This is the ground return path for the charge pump.
4	2, 3	AGND	Analog Ground. This is the ground return path of the prescaler.
5	4	$RF_{IN}B$	Complementary Input to the RF Prescaler. This point should be decoupled to the ground plane with a small bypass capacitor, typically 100 pF. See Figure 29.
6	5	$RF_{IN}A$	Input to the RF Prescaler. This small-signal input is ac-coupled from the VCO.
7	6, 7	AV_{DD}	Analog Power Supply. This may range from 2.7 V to 5.5 V. Decoupling capacitors to the analog ground plane should be placed as close as possible to this pin. AV_{DD} must be the same value as DV_{DD}.
8	8	REF_{IN}	Reference Input. This is a CMOS input with a nominal threshold of V_{DD}/2, and an equivalent input resistance of 100 kΩ. See Figure 28. This input can be driven from a TTL or CMOS crystal oscillator, or can be ac-coupled.
9	9, 10	DGND	Digital Ground.
10	11	CE	Chip Enable. A logic low on this pin powers down the device and puts the charge pump output into three-state mode. Taking the pin high powers up the device depending on the status of the power-down Bit F2.
11	12	CLK	Serial Clock Input. This serial clock is used to clock in the serial data to the registers. The data is latched into the 24-bit shift register on the CLK rising edge. This input is a high impedance CMOS input.
12	13	DATA	Serial Data Input. The serial data is loaded MSB first with the two LSBs being the control bits. This input is a high impedance CMOS input.
13	14	LE	Load Enable, CMOS Input. When LE goes high, the data stored in the shift registers is loaded into one of the four latches; the latch is selected using the control bits.
14	15	MUXOUT	This multiplexer output allows either the lock detect, the scaled RF, or the scaled reference frequency to be accessed externally.
15	16, 17	DV_{DD}	Digital Power Supply. This may range from 2.7 V to 5.5 V. Decoupling capacitors to the digital ground plane should be placed as close as possible to this pin. DV_{DD} must be the same value as AV_{DD}.
16	18	V_P	Charge Pump Power Supply. This should be greater than or equal to V_{DD}. In systems where V_{DD} is 3 V, V_P can be set to 6 V and used to drive a VCO with a tuning range of up to 6 V.

TYPICAL PERFORMANCE CHARACTERISTICS

FREQ –UNIT	PARAM –TYPE	DATA –FORMAT	KEYWORD		IMPEDANCE –OHMS
GHz	S	MA	R		50
FREQ	MAGS11	ANGS11	FREQ	MAGS11	ANGS11
0.05	0.89207	–2.0571	1.05	0.9512	–40.134
0.10	0.8886	–4.4427	1.10	0.93458	–43.747
0.15	0.89022	–6.3212	1.15	0.94782	–44.393
0.20	0.96323	–2.1393	1.20	0.96875	–46.937
0.25	0.90566	–12.13	1.25	0.92216	–49.6
0.30	0.90307	–13.52	1.30	0.93755	–51.884
0.35	0.89318	–15.746	1.35	0.96178	–51.21
0.40	0.89806	–18.056	1.40	0.94354	–53.55
0.45	0.89565	–19.693	1.45	0.95189	–56.786
0.50	0.88538	–22.246	1.50	0.97647	–58.781
0.55	0.89699	–24.336	1.55	0.98619	–60.545
0.60	0.89927	–25.948	1.60	0.95459	–61.43
0.65	0.87797	–28.457	1.65	0.97945	–61.241
0.70	0.90765	–29.735	1.70	0.98864	–64.051
0.75	0.88526	–31.879	1.75	0.97399	–66.19
0.80	0.81267	–32.681	1.80	0.97216	–63.775
0.85	0.90357	–31.522			
0.90	0.92954	–34.222			
0.95	0.92087	–36.961			
1.00	0.93788	–39.343			

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Figure 5. S-Parameter Data for the ADF4113 RF Input (up to 1.8 GHz)

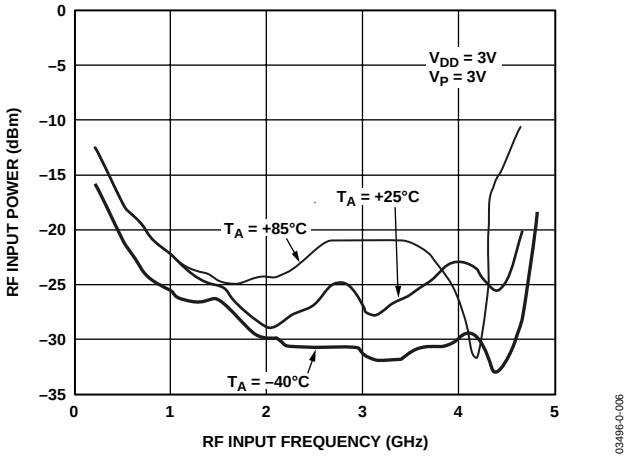

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Figure 6. Input Sensitivity (ADF4113)

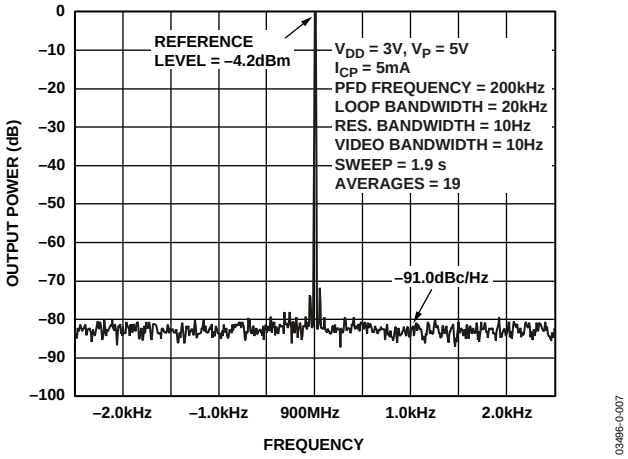

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Figure 7 ADF4113 Phase Noise (900 MHz, 200 kHz, 20 kHz)

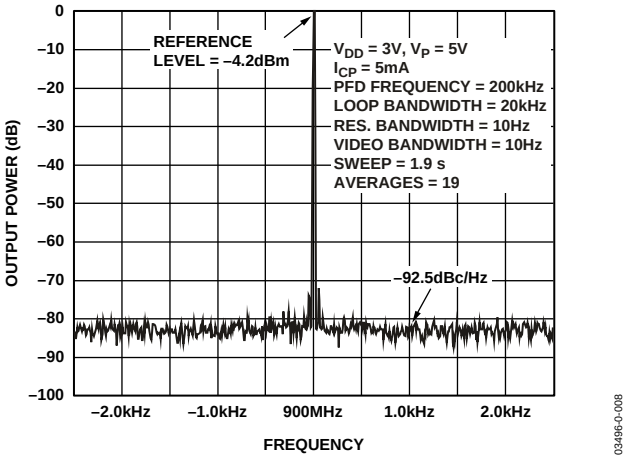

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Figure 8. ADF4113 Phase Noise (900 MHz, 200kHz, 20 kHz) with DLY and SYNC Enabled

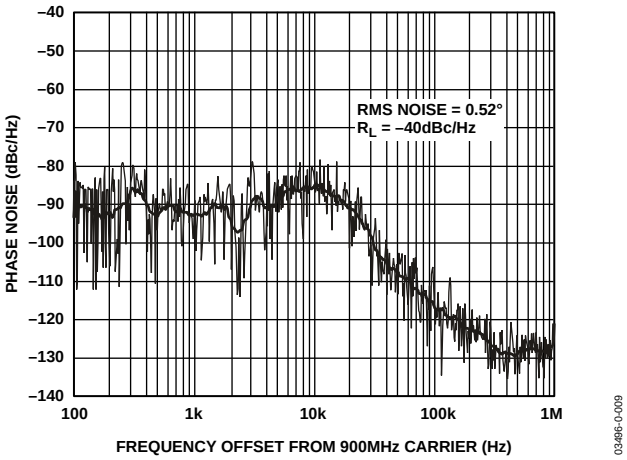

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Figure 9. ADF4113 Integrated Phase Noise (900 MHz, 200 kHz, 20 kHz, Typical Lock Time: 400 µs)

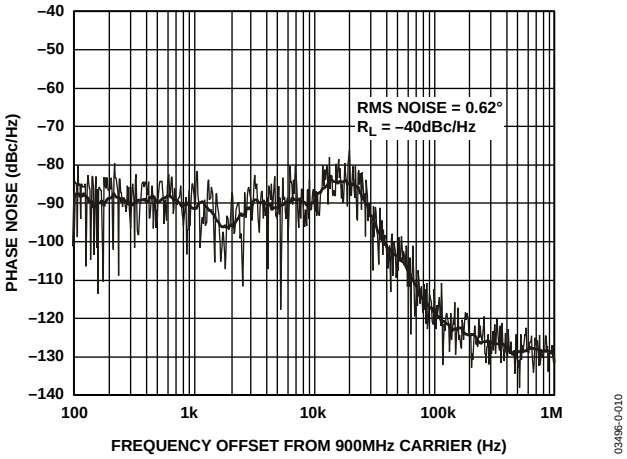

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Figure 10. ADF4113 Integrated Phase Noise (900 MHz, 200 kHz, 35 kHz, Typical Lock Time: 200 µs)

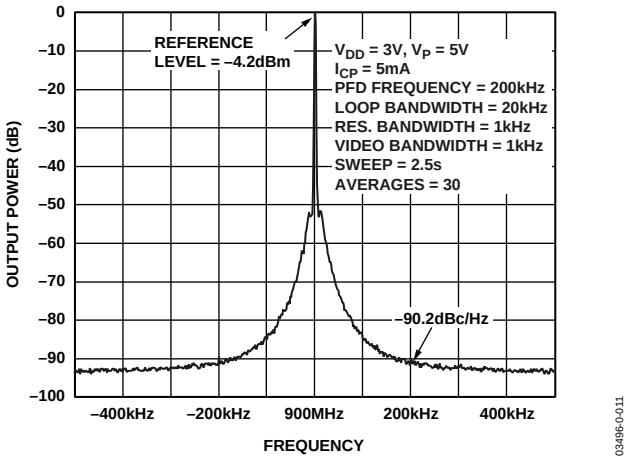

Figure 11. ADF4113 Reference Spurs (900 MHz, 200 kHz, 20 kHz)

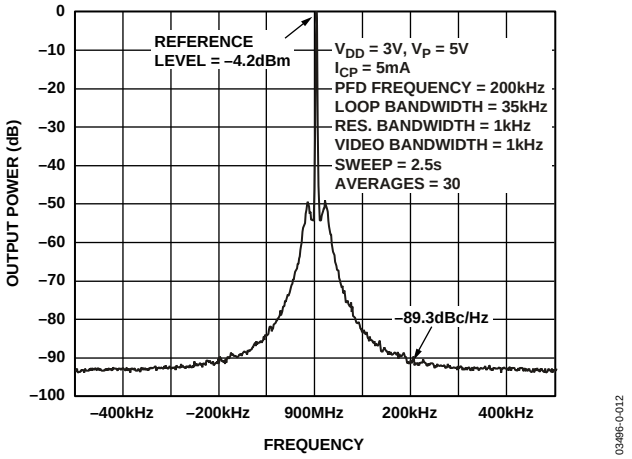

Figure 12. ADF4113 (900 MHz, 200 kHz, 35 kHz)

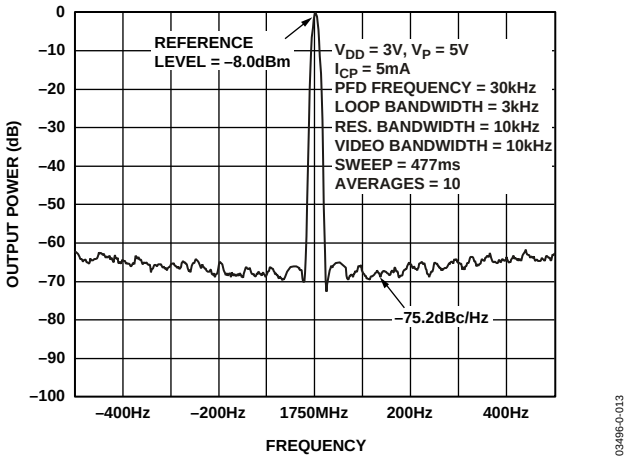

Figure 13. ADF4113 Phase Noise (1750 MHz, 30 kHz, 3 kHz)

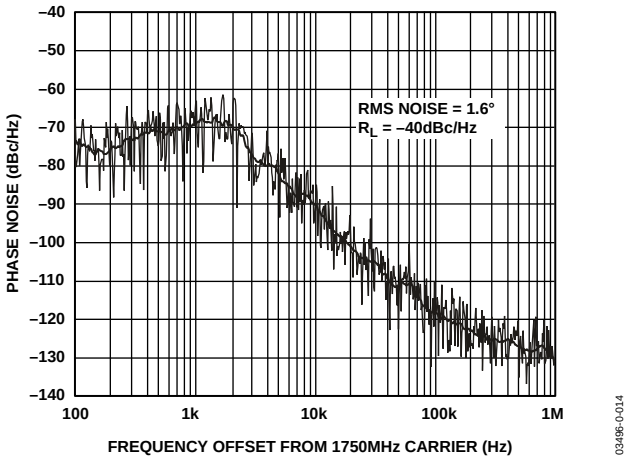

Figure 14. ADF4113 Integrated Phase Noise (1750 MHz, 30 kHz, 3 kHz)

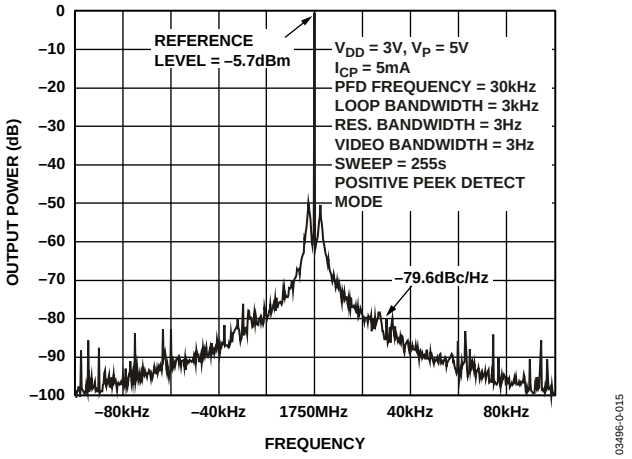

Figure 15. ADF4113 Reference Spurs (1750 MHz, 30 kHz, 3 kHz)

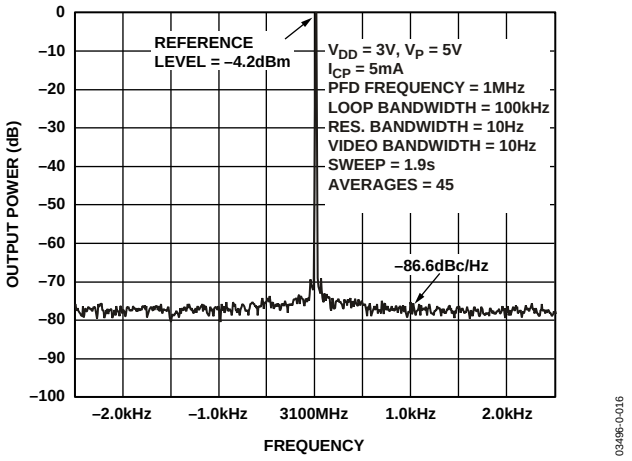

Figure 16. ADF4113 Phase Noise (3100 MHz, 1 MHz, 100 kHz)

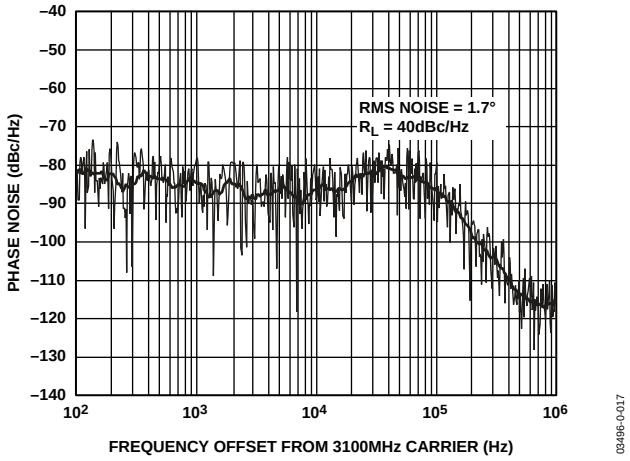

Figure 17. ADF4113 Integrated Phase Noise (3100 MHz, 1 MHz, 100 kHz)

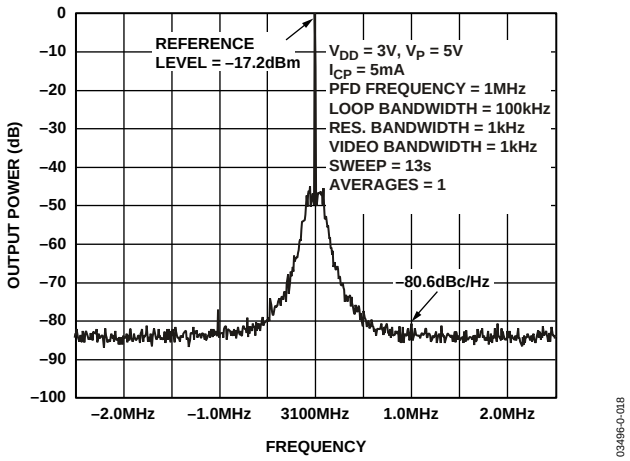

Figure 18. Reference Spurs (3100 MHz, 1 MHz, 100 kHz)

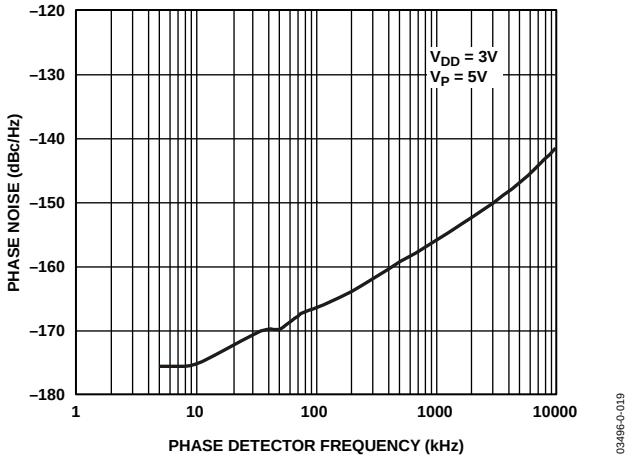

Figure 19. ADF4113 Phase Noise (Referred to CP Output) vs. Phase Detector Frequency

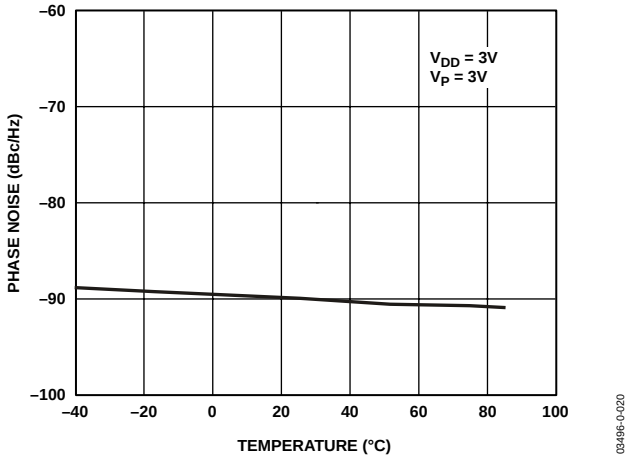

Figure 20. ADF4113 Phase Noise vs. Temperature (900 MHz, 200 kHz, 20 kHz)

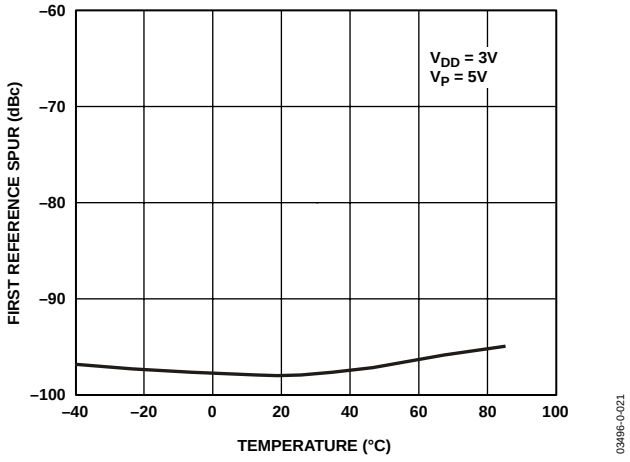

Figure 21. ADF4113 Reference Spurs vs. Temperature (900 MHz, 200 kHz, 20 kHz)

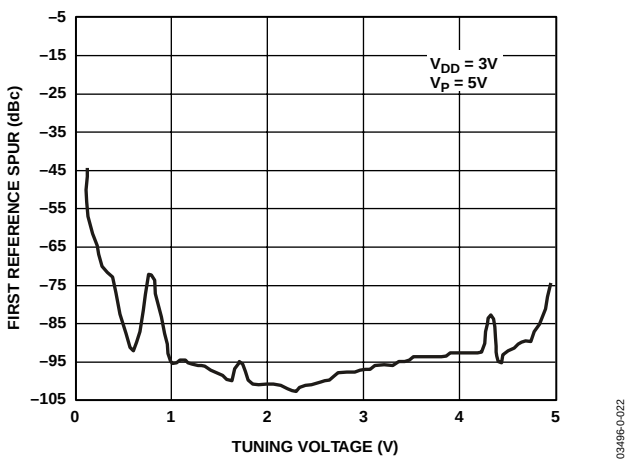

Figure 22. ADF4113 Reference Spurs (200 kHz) vs. V_{TUNE} (900 MHz, 200 kHz, 20 kHz)

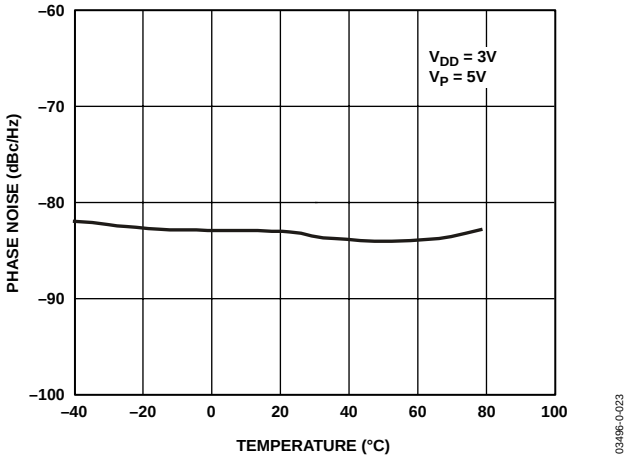

Figure 23. ADF4113 Phase Noise vs. Temperature (836 MHz, 30 kHz, 3 kHz)

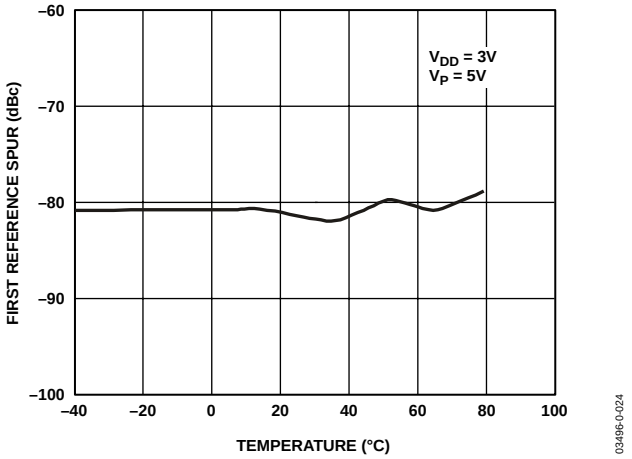

Figure 24. ADF4113 Reference Spurs vs. Temperature (836 MHz, 30 kHz, 3 kHz)

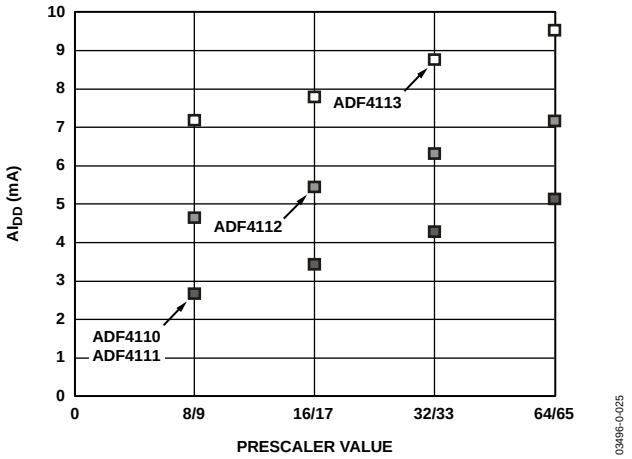

Figure 25. AI_{DD} vs. Prescaler Value

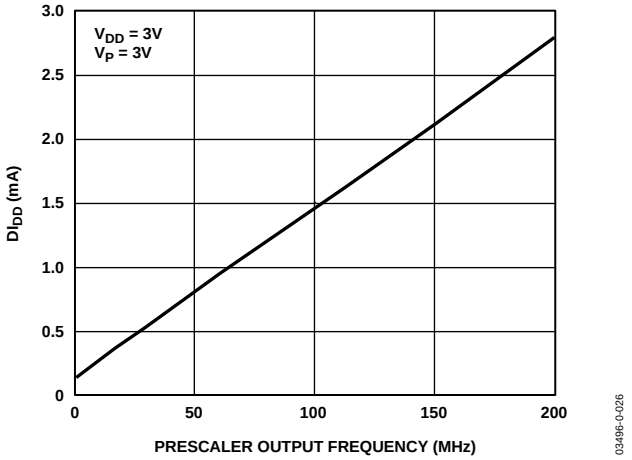

Figure 26. DI_{DD} vs. Prescaler Output Frequency (ADF4110, ADF4111, ADF4112, ADF4113)

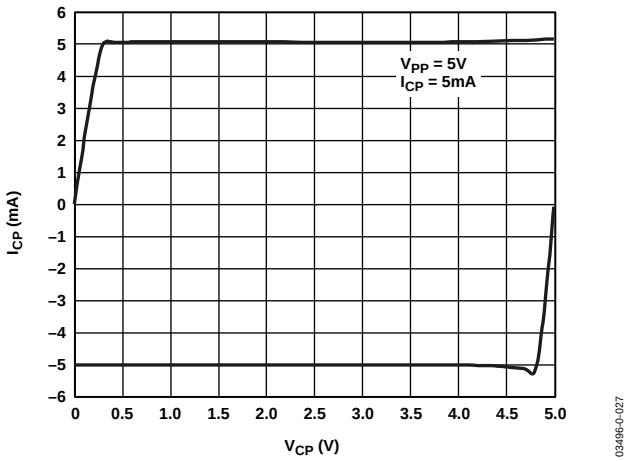

Figure 27. Charge Pump Output Characteristics for ADF4110 Family

CIRCUIT DESCRIPTION

REFERENCE INPUT SECTION

The reference input stage is shown in Figure 28. SW1 and SW2 are normally closed switches. SW3 is normally open. When power-down is initiated, SW3 is closed and SW1 and SW2 are opened. This ensures that there is no loading of the REF_{IN} pin on power-down.

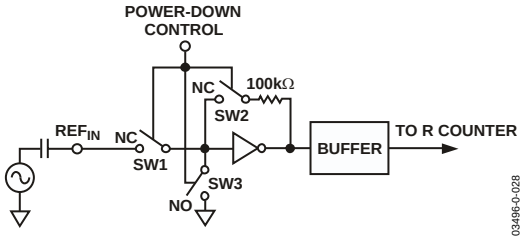

Figure 28. Reference Input Stage

RF INPUT STAGE

The RF input stage is shown in Figure 29. It is followed by a two-stage limiting amplifier to generate the current mode logic (CML) clock levels needed for the prescaler.

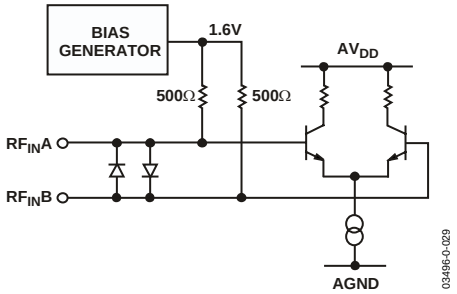

Figure 29. RF Input Stage

PRESCALER (P/P + 1)

Along with the A and B counters, the dual-modulus prescaler (P/P + 1) enables the large division ratio, N, to be realized (N = BP + A). The dual-modulus prescaler, operating at CML levels, takes the clock from the RF input stage and divides it down to a manageable frequency for the CMOS A and B counters. The prescaler is programmable; it can be set in software to 8/9, 16/17, 32/33, or 64/65. It is based on a synchronous 4/5 core.

A AND B COUNTERS

The A and B CMOS counters combine with the dual-modulus prescaler to allow a wide ranging division ratio in the PLL feedback counter. The counters are specified to work when the prescaler output is 200 MHz or less. Thus, with an RF input frequency of 2.5 GHz, a prescaler value of 16/17 is valid but a value of 8/9 is not.

Pulse Swallow Function

The A and B counters, in conjunction with the dual-modulus prescaler, make it possible to generate output frequencies that are spaced only by the reference frequency divided by *R*. The equation for the VCO frequency is

$$f_{VCO} = [(P \times B) + A]f_{REFIN}/R$$

where:

f_{VCO} = output frequency of external voltage controlled oscillator (VCO)
P = preset modulus of dual-modulus prescaler
B = preset divide ratio of binary 13-bit counter(3 to 8191)
A = preset divide ratio of binary 6-bit swallow counter (0 to 63)
f_{REFIN} = output frequency of the external reference frequency oscillator
R = preset divide ratio of binary 14-bit programmable reference counter (1 to 16383)

R COUNTER

The 14-bit R counter allows the input reference frequency to be divided down to produce the reference clock to the phase frequency detector (PFD). Division ratios from 1 to 16,383 are allowed.

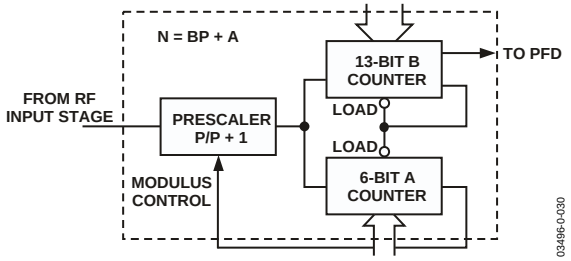

Figure 30. A and B Counters

PHASE FREQUENCY DETECTOR (PFD) AND CHARGE PUMP

The PFD takes inputs from the R counter and N counter (N = BP + A) and produces an output proportional to the phase and frequency difference between them. Figure 31 is a simplified schematic. The PFD includes a programmable delay element that controls the width of the antibacklash pulse. This pulse ensures that there is no dead zone in the PFD transfer function and minimizes phase noise and reference spurs. Two bits in the reference counter latch, ABP2 and ABP1, control the width of the pulse. See Table 7.

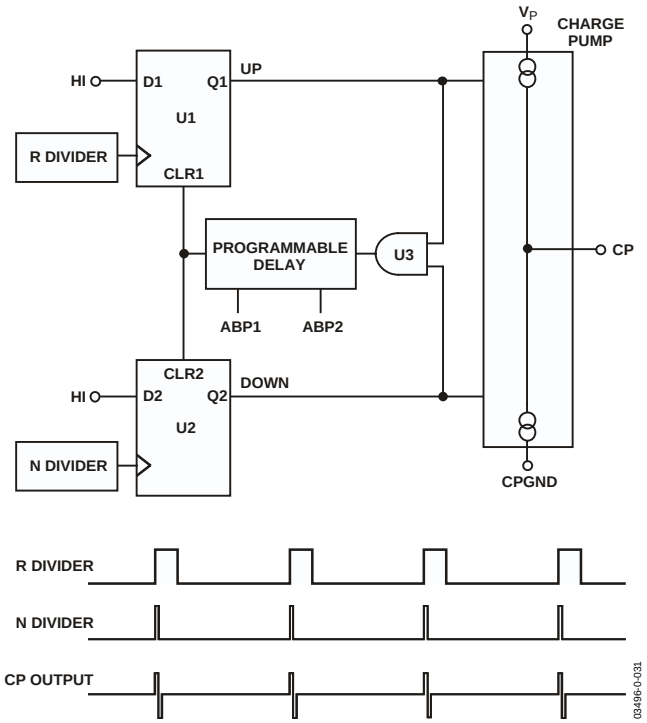

Figure 31. PFD Simplified Schematic and Timing (In Lock)

MUXOUT AND LOCK DETECT

The output multiplexer on the ADF4110 family allows the user to access various internal points on the chip. The state of MUXOUT is controlled by M3, M2, and M1 in the function latch. Table 9 shows the full truth table. Figure 32 shows the MUXOUT section in block diagram form.

Lock Detect

MUXOUT can be programmed for two types of lock detect: digital lock detect and analog lock detect.

Digital lock detect is active high. When LDP in the R counter latch is set to 0, digital lock detect is set high when the phase error on three consecutive phase detector (PD) cycles is less than 15 ns. With LDP set to 1, five consecutive cycles of less than 15 ns are required to set the lock detect. It stays high until a phase error greater than 25 ns is detected on any subsequent PD cycle.

The N-channel open-drain analog lock detect should be operated with a 10 kΩ nominal external pull-up resistor. When lock has been detected, this output is high with narrow low-going pulses.

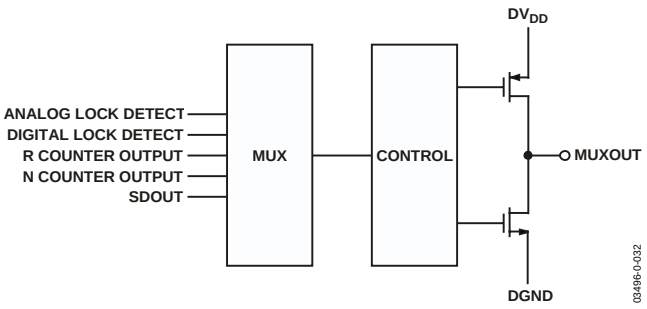

Figure 32. MUXOUT Circuit

INPUT SHIFT REGISTER

The ADF4110 family digital section includes a 24-bit input shift register, a 14-bit R counter, and a 19-bit N counter comprised of a 6-bit A counter and a 13-bit B counter. Data is clocked into the 24-bit shift register on each rising edge of CLK MSB first. Data is transferred from the shift register to one of four latches on the rising edge of LE. The destination latch is determined by the state of the two control bits (C2, C1) in the shift register. These are the two LSBs, DB1 and DB0, as shown in Figure 2. The truth table for these bits is shown in Table 5.

Table 6 shows a summary of how the latches are programmed.

Table 5. C2, C1 Truth Table

Control Bits		
C2	**C1**	**Data Latch**
0	0	R Counter
0	1	N Counter (A and B)
1	0	Function Latch (Including Prescaler)
1	1	Initialization Latch

Table 6. ADF4110 Family Latch Summary

REFERENCE COUNTER LATCH

RESERVED	DLY	SYNC	LOCK DETECT PRECISION	TEST MODE BITS		ANTI-BACKLASH WIDTH		14-BIT REFERENCE COUNTER, R													CONTROL BITS	
DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
X	DLY	SYNC	LDP	T2	T1	ABP2	ABP1	R14	R13	R12	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	C2 (0)	C1 (0)

X = DON'T CARE

N COUNTER LATCH

RESERVED		CP GAIN	13-BIT B COUNTER													6-BIT A COUNTER						CONTROL BITS	
DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
X	X	G1	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	A6	A5	A4	A3	A2	A1	C2 (0)	C1 (1)

X = DON'T CARE

FUNCTION LATCH

PRESCALER VALUE		POWER-DOWN 2	CURRENT SETTING 2			CURRENT SETTING 1			TIMER COUNTER CONTROL				FASTLOCK MODE	FASTLOCK ENABLE	CP THREE-STATE	PD POLARITY	MUXOUT CONTROL			POWER-DOWN 1	COUNTER RESET	CONTROL BITS	
DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
P2	P1	PD2	CPI6	CPI5	CPI4	CPI3	CPI2	CPI1	TC4	TC3	TC2	TC1	F5	F4	F3	F2	M3	M2	M1	PD1	F1	C2 (1)	C1 (0)

INITIALIZATION LATCH

PRESCALER VALUE		POWER-DOWN 2	CURRENT SETTING 2			CURRENT SETTING 1			TIMER COUNTER CONTROL				FASTLOCK MODE	FASTLOCK ENABLE	CP THREE-STATE	PD POLARITY	MUXOUT CONTROL			POWER-DOWN 1	COUNTER RESET	CONTROL BITS	
DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
P2	P1	PD2	CPI6	CPI5	CPI4	CPI3	CPI2	CPI1	TC4	TC3	TC2	TC1	F5	F4	F3	F2	M3	M2	M1	PD1	F1	C2 (1)	C1 (1)

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Table 7. Reference Counter Latch Map

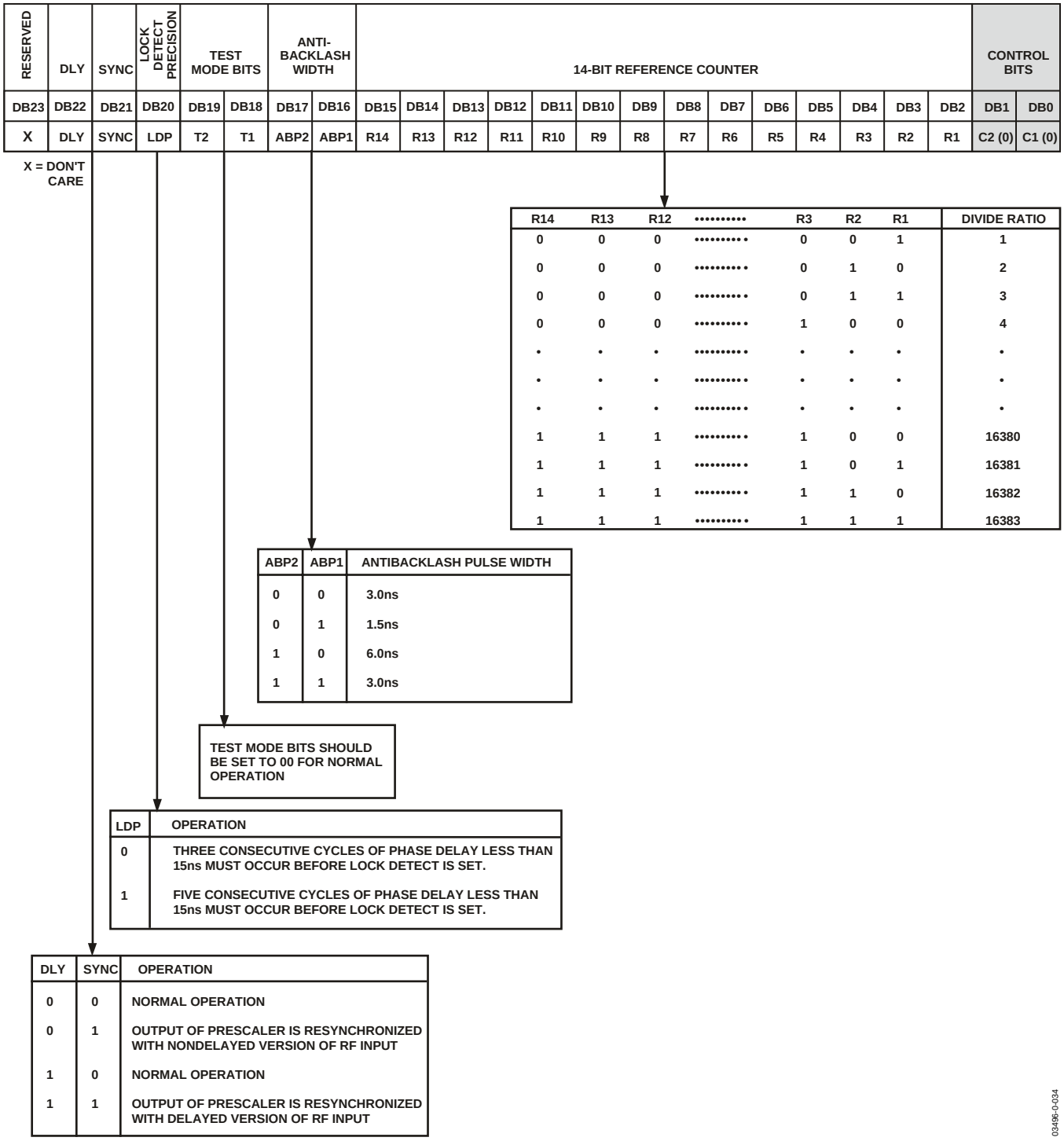

Table 8. AB Counter Latch Map

RESERVED		CP GAIN	13-BIT B COUNTER													6-BIT A COUNTER						CONTROL BITS	
DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
X	X	G1	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	A6	A5	A4	A3	A2	A1	C2 (0)	C1 (1)

X = DON'T CARE

A6	A5	•••••••••	A2	A1	A COUNTER DIVIDE RATIO
0	0	•••••••••	0	0	0
0	0	•••••••••	0	1	1
0	0	•••••••••	1	0	2
0	0	•••••••••	1	1	3
•	•	•••••••••	•	•	•
•	•	•••••••••	•	•	•
•	•	•••••••••	•	•	•
1	1	•••••••••	0	0	60
1	1	•••••••••	0	1	61
1	1	•••••••••	1	0	62
1	1	•••••••••	1	1	63

B13	B12	B11	•••••••••	B3	B2	B1	B COUNTER DIVIDE RATIO
0	0	0	•••••••••	0	0	0	NOT ALLOWED
0	0	0	•••••••••	0	0	1	NOT ALLOWED
0	0	0	•••••••••	0	1	0	NOT ALLOWED
0	0	0	•••••••••	0	1	1	3
0	0	0	•••••••••	1	0	0	4
•	•	•	•••••••••	•	•	•	•
•	•	•	•••••••••	•	•	•	•
•	•	•	•••••••••	•	•	•	•
1	1	1	•••••••••	1	0	0	8188
1	1	1	•••••••••	1	0	1	8189
1	1	1	•••••••••	1	1	0	8190
1	1	1	•••••••••	1	1	1	8191

F4 (FUNCTION LATCH) FASTLOCK ENABLE*	CP GAIN	OPERATION
0	0	CHARGE PUMP CURRENT SETTING 1 IS PERMANENTLY USED.
0	1	CHARGE PUMP CURRENT SETTING 2 IS PERMANENTLY USED.
1	0	CHARGE PUMP CURRENT SETTING 1 IS USED.
1	1	CHARGE PUMP CURRENT IS SWITCHED TO SETTING 2. THE TIME SPENT IN SETTING 2 IS DEPENDENT UPON WHICH FASTLOCK MODE IS USED. SEE FUNCTION LATCH DESCRIPTION.

*SEE TABLE 9

N = BP + A, P IS PRESCALER VALUE SET IN THE FUNCTION LATCH, B MUST BE GREATER THAN OR EQUAL TO A. FOR CONTINUOUSLY ADJACENT VALUES OF (N_X F_{REF}), AT THE OUTPUT, N_{MIN} IS (P^2–P).

THESE BITS ARE NOT USED BY THE DEVICE AND ARE DON'T CARE BITS

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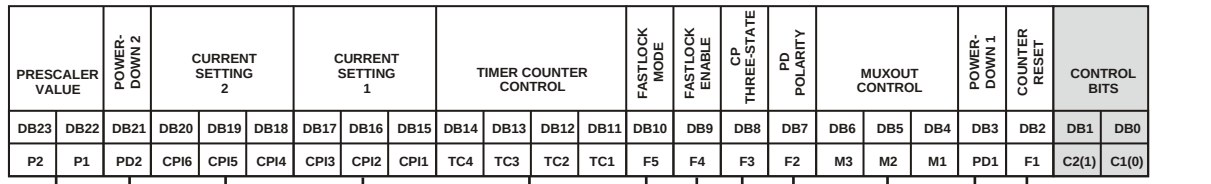
Table 9. Function Latch Map



F1	COUNTER OPERATION
0	NORMAL
1	R, A, B COUNTERS HELD IN RESET

F2	PHASE DETECTOR POLARITY
0	NEGATIVE
1	POSITIVE

F3	CHARGE PUMP OUTPUT
0	NORMAL
1	THREE-STATE

F4	F5	FASTLOCK MODE
0	X	FASTLOCK DISABLED
1	0	FASTLOCK MODE 1
1	1	FASTLOCK MODE 2

TC4	TC3	TC2	TC1	TIMEOUT (PFD CYCLES)
0	0	0	0	3
0	0	0	1	7
0	0	1	0	11
0	0	1	1	15
0	1	0	0	19
0	1	0	1	23
0	1	1	0	27
0	1	1	1	31
1	0	0	0	35
1	0	0	1	39
1	0	1	0	43
1	0	1	1	47
1	1	0	0	51
1	1	0	1	55
1	1	1	0	59
1	1	1	1	63

SEE FUNCTION LATCH, TIMER COUNTER CONTROL SECTION

M3	M2	M1	OUTPUT
0	0	0	THREE-STATE OUTPUT
0	0	1	DIGITAL LOCK DETECT (ACTIVE HIGH)
0	1	0	N DIVIDER OUTPUT
0	1	1	DV_{DD}
1	0	0	R DIVIDER OUTPUT
1	0	1	ANALOG LOCK DETECT (N-CHANNEL OPEN-DRAIN)
1	1	0	SERIAL DATA OUTPUT
1	1	1	DGND

CPI6	CPI5	CPI4	I_{CP} (mA)		
CPI3	CPI2	CPI1	2.7kΩ	4.7kΩ	10kΩ
0	0	0	1.09	0.63	0.29
0	0	1	2.18	1.25	0.59
0	1	0	3.26	1.88	0.88
0	1	1	4.35	2.50	1.76
1	0	0	5.44	3.13	1.47
1	0	1	6.53	3.75	1.76
1	1	0	7.62	4.38	2.06
1	1	1	8.70	5.00	2.35

CE PIN	PD2	PD1	MODE
0	X	X	ASYNCHRONOUS POWER-DOWN
1	X	0	NORMAL OPERATION
1	0	1	ASYNCHRONOUS POWER-DOWN
1	1	1	SYNCHRONOUS POWER-DOWN

P2	P1	PRESCALER VALUE
0	0	8/9
0	1	16/17
1	0	32/33
1	1	64/65

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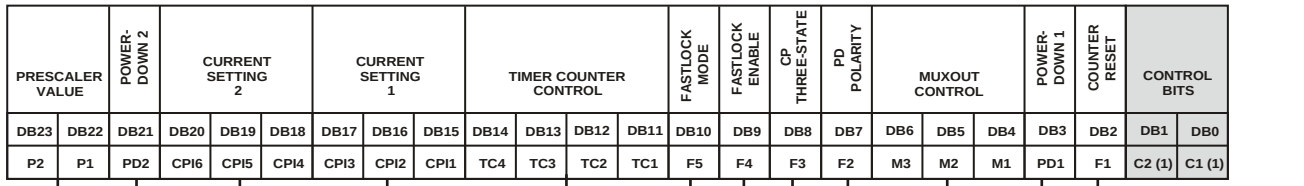
Table 10. Initialization Latch Map



PRESCALER VALUE		POWER-DOWN 2	CURRENT SETTING 2			CURRENT SETTING 1			TIMER COUNTER CONTROL				FASTLOCK MODE	FASTLOCK ENABLE	CP THREE-STATE	PD POLARITY	MUXOUT CONTROL			POWER-DOWN 1	COUNTER RESET	CONTROL BITS	
DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
P2	P1	PD2	CPI6	CPI5	CPI4	CPI3	CPI2	CPI1	TC4	TC3	TC2	TC1	F5	F4	F3	F2	M3	M2	M1	PD1	F1	C2 (1)	C1 (1)

F1	COUNTER OPERATION
0	NORMAL
1	R, A, B COUNTERS HELD IN RESET

F2	PHASE DETECTOR POLARITY
0	NEGATIVE
1	POSITIVE

F3	CHARGE PUMP
0	OUTPUT NORMAL
1	THREE-STATE

F4	F5	FASTLOCK MODE
0	X	FASTLOCK DISABLED
1	0	FASTLOCK MODE 1
1	1	FASTLOCK MODE 2

TC4	TC3	TC2	TC1	TIMEOUT (PFD CYCLES)
0	0	0	0	3
0	0	0	1	7
0	0	1	0	11
0	0	1	1	15
0	1	0	0	19
0	1	0	1	23
0	1	1	0	27
0	1	1	1	31
1	0	0	0	35
1	0	0	1	39
1	0	1	0	43
1	0	1	1	47
1	1	0	0	51
1	1	0	1	55
1	1	1	0	59
1	1	1	1	63

SEE FUNCTION LATCH, TIMER COUNTER CONTROL SECTION

M3	M2	M1	OUTPUT
0	0	0	THREE-STATE OUTPUT
0	0	1	DIGITAL LOCK DETECT (ACTIVE HIGH)
0	1	0	N DIVIDER OUTPUT
0	1	1	DV_{DD}
1	0	0	R DIVIDER OUTPUT
1	0	1	ANALOG LOCK DETECT (N-CHANNEL OPEN-DRAIN)
1	1	0	SERIAL DATA OUTPUT
1	1	1	DGND

CPI6	CPI5	CPI4	I_{CP} (mA)		
CPI3	CPI2	CPI1	2.7kΩ	4.7kΩ	10kΩ
0	0	0	1.09	0.63	0.29
0	0	1	2.18	1.25	0.59
0	1	0	3.27	1.88	0.88
0	1	1	4.35	2.50	1.76
1	0	0	5.44	3.13	1.47
1	0	1	6.53	3.75	1.76
1	1	0	7.62	4.38	2.06
1	1	1	8.70	5.00	2.35

CE PIN	PD2	PD1	MODE
0	X	X	ASYNCHRONOUS POWER-DOWN
1	X	0	NORMAL OPERATION
1	0	1	ASYNCHRONOUS POWER-DOWN
1	1	1	SYNCHRONOUS POWER-DOWN

P2	P1	PRESCALER VALUE
0	0	8/9
0	1	16/17
1	0	32/33
1	1	64/65

03496-0-037

FUNCTION LATCH

The on-chip function latch is programmed with C2, C1 set to 1. Table 9 shows the input data format for programming the function latch.

Counter Reset

DB2 (F1) is the counter reset bit. When DB2 is 1, the R counter and the AB counters are reset. For normal operation, this bit should be 0. Upon powering up, the F1 bit must be disabled, and the N counter resumes counting in "close" alignment with the R counter. (The maximum error is one prescaler cycle.)

Power-Down

DB3 (PD1) and DB21 (PD2) on the ADF411x provide programmable power-down modes. They are enabled by the CE pin.

When the CE pin is low, the device is immediately disabled regardless of the states of PD2, PD1.

In the programmed asynchronous power-down, the device powers down immediately after latching a 1 into Bit PD1, provided PD2 has been loaded with a 0.

In the programmed synchronous power-down, the device power-down is gated by the charge pump to prevent unwanted frequency jumps. Once power-down is enabled by writing a 1 into Bit PD1 (provided a 1 has also been loaded to PD2), the device goes into power-down on the next charge pump event.

When a power-down is activated (either synchronous or asynchronous mode including CE pin activated power-down), the following events occur:

- All active dc current paths are removed.
- The R, N, and timeout counters are forced to their load state conditions.
- The charge pump is forced into three-state mode.
- The digital clock detect circuitry is reset.
- The RFIN input is debiased.
- The reference input buffer circuitry is disabled.
- The input register remains active and capable of loading and latching data.

MUXOUT Control

The on-chip multiplexer is controlled by M3, M2, and M1 on the ADF4110 family. Table 9 shows the truth table.

Fastlock Enable Bit

DB9 of the function latch is the fastlock enable bit. Fastlock is enables only when this is 1.

Fastlock Mode Bit

DB10 of the function latch is the fastlock enable bit. When fastlock is enabled, this bit determines which fastlock mode is used. If the fastlock mode bit is 0, fastlock mode 1 is selected; if the fastlock mode bit is 1, fastlock mode 2 is selected.

Fastlock Mode 1

The charge pump current is switched to the contents of Current Setting 2.

The device enters fastlock by having a 1 written to the CP gain bit in the AB counter latch. The device exits fastlock by having a 0 written to the CP gain bit in the AB counter latch.

Fastlock Mode 2

The charge pump current is switched to the contents of Current Setting 2. The device enters fastlock by having a 1 written to the CP gain bit in the AB counter latch. The device exits fastlock under the control of the timer counter. After the timeout period determined by the value in TC4 through TC1, the CP gain bit in the AB counter latch is automatically reset to 0 and the device reverts to normal mode instead of fastlock. See Table 9 for the timeout periods.

Timer Counter Control

The user has the option of programming two charge pump currents. Current Setting 1 is meant to be used when the RF output is stable and the system is in a static state. Current Setting 2 is meant to be used when the system is dynamic and in a state of change (i.e., when a new output frequency is programmed).

The normal sequence of events is as follows:

The user initially decides what the preferred charge pump currents are going to be. For example, they may choose 2.5 mA as Current Setting 1 and 5 mA as Current Setting 2.

At the same time, they must also decide how long they want the secondary current to stay active before reverting to the primary current. This is controlled by the timer counter control bits, DB14 through DB11 (TC4 through TC1) in the function latch. The truth table is given in Table 10.

A user can program a new output frequency simply by programming the AB counter latch with new values for A and B. At the same time, the CP gain bit can be set to 1, which sets the charge pump with the value in CPI6–CPI4 for a period determined by TC4 through TC1. When this time is up, the charge pump current reverts to the value set by CPI3–CPI1. At the same time, the CP gain bit in the AB counter latch is reset to 0 and is ready for the next time the user wishes to change the frequency.

Note that there is an enable feature on the timer counter. It is enabled when Fastlock Mode 2 is chosen by setting the fastlock mode bit (DB10) in the function latch to 1.

Charge Pump Currents

CPI3, CPI2, and CPI1 program Current Setting 1 for the charge pump. CPI6, CPI5, and CPI4 program Current Setting 2 for the charge pump. The truth table is given in Table 10.

Prescaler Value

P2 and P1 in the function latch set the prescaler values. The prescaler value should be chosen so that the prescaler output frequency is always less than or equal to 200 MHz. Thus, with an RF frequency of 2 GHz, a prescaler value of 16/17 is valid but a value of 8/9 is not.

PD Polarity

This bit sets the phase detector polarity bit. See Table 10.

CP Three-State

This bit controls the CP output pin. With the bit set high, the CP output is put into three-state. With the bit set low, the CP output is enabled.

INITIALIZATION LATCH

When C2, C1 = 1, 1, the initialization latch is programmed. This is essentially the same as the function latch (programmed when C2, C1 = 1, 0).

However, when the initialization latch is programmed, an additional internal reset pulse is applied to the R and AB counters. This pulse ensures that the AB counter is at load point when the AB counter data is latched, and the device begins counting in close phase alignment.

If the latch is programmed for synchronous power-down (CE pin high; PD1 bit high; PD2 bit low), the internal pulse also triggers this power-down. The prescaler reference and the oscillator input buffer are unaffected by the internal reset pulse, so close phase alignment is maintained when counting resumes.

When the first AB counter data is latched after initialization, the internal reset pulse is again activated. However, successive AB counter loads after this will not trigger the internal reset pulse.

DEVICE PROGRAMMING AFTER INITIAL POWER-UP

After initial power-up of the device, there are three ways to program the device.

Initialization Latch Method

Apply V_{DD}. Program the initialization latch (11 in 2 LSBs of input word). Make sure the F1 bit is programmed to 0. Then, do an R load (00 in 2 LSBs). Then do an AB load (01 in 2 LSBs).

When the initialization latch is loaded, the following occurs:

1. The function latch contents are loaded.
2. An internal pulse resets the R, A, B, and timeout counters to load state conditions and three-states the charge pump. Note that the prescaler band gap reference and the oscillator input buffer are unaffected by the internal reset pulse, allowing close phase alignment when counting resumes.
3. Latching the first AB counter data after the initialization word activates the same internal reset pulse. Successive AB loads do not trigger the internal reset pulse unless there is another initialization.

CE Pin Method

1. Apply V_{DD}.
2. Bring CE low to put the device into power-down. This is an asynchronous power-down in that it happens immediately.
3. Program the function latch (10). Program the R counter latch (00). Program the AB counter latch (01).
4. Bring CE high to take the device out of power-down. The R and AB counters now resume counting in close alignment.

After CE goes high, a duration of 1 μs may be required for the prescaler band gap voltage and oscillator input buffer bias to reach steady state.

CE can be used to power the device up and down in order to check for channel activity. The input register does not need to be reprogrammed each time the device is disabled and enabled as long as it has been programmed at least once after V_{DD} was initially applied.

Counter Reset Method

1. Apply V_{DD}.
2. Do a function latch load (10 in 2 LSBs). As part of this, load 1 to the F1 bit. This enables the counter reset.
3. Do an R counter load (00 in 2 LSBs). Do an AB counter load (01 in 2 LSBs). Do a function latch load (10 in 2 LSBs). As part of this, load 0 to the F1 bit. This disables the counter reset.

This sequence provides the same close alignment as the initialization method. It offers direct control over the internal reset. Note that counter reset holds the counters at load point and three states the charge pump but does not trigger synchronous power-down. The counter reset method requires an extra function latch load compared to the initialization latch method.

RESYNCHRONIZING THE PRESCALER OUTPUT

Table 7 (the Reference Counter Latch Map) shows two bits, DB22 and DB21, which are labeled DLY and SYNC, respectively. These bits affect the operation of the prescaler.

With SYNC = 1, the prescaler output is resynchronized with the RF input. This has the effect of reducing jitter due to the prescaler and can lead to an overall improvement in synthesizer phase noise performance. Typically, a 1 dB to 2 dB improvement is seen in the ADF4113. The lower bandwidth devices can show an even greater improvement. For example, the ADF4110 phase noise is typically improved by 3 dB when SYNC is enabled.

With DLY = 1, the prescaler output is resynchronized with a delayed version of the RF input.

If the SYNC feature is used on the synthesizer, some care must be taken. At some point, (at certain temperatures and output frequencies), the delay through the prescaler coincides with the active edge on RF input; this causes the SYNC feature to break down. It is important to be aware of this when using the SYNC feature. Adding a delay to the RF signal, by programming DLY = 1, extends the operating frequency and temperature somewhat. Using the SYNC feature also increases the value of the AI_{DD} for the device. With a 900 MHz output, the ADF4113 AI_{DD} increases by about 1.3 mA when SYNC is enabled and by an additional 0.3 mA if DLY is enabled.

All the typical performance plots in this data sheet, except for Figure 8, apply for DLY and SYNC = 0, i.e., no resynchronization or delay enabled.

APPLICATIONS

LOCAL OSCILLATOR FOR GSM BASE STATION TRANSMITTER

Figure 33 shows the ADF4111/ADF4112/ADF4113 being used with a VCO to produce the LO for a GSM base station transmitter.

The reference input signal is applied to the circuit at $FREF_{IN}$ and, in this case, is terminated in 50 Ω. A typical GSM system would have a 13 MHz TCXO driving the reference input without any 50 Ω termination. In order to have channel spacing of 200 kHz (GSM standard), the reference input must be divided by 65, using the on-chip reference divider of the ADF4111/ADF4112/ADF4113.

The charge pump output of the ADF4111/ADF4112/ADF4113 (Pin 2) drives the loop filter. In calculating the loop filter component values, a number of items need to be considered. In this example, the loop filter was designed so that the overall phase margin for the system would be 45 degrees. Other PLL system specifications are

K_D = 5 mA
K_V = 12 MHz/V
Loop Bandwidth = 20 kHz
F_{REF} = 200 kHz
N = 4500
Extra Reference Spur Attenuation = 10 dB

All of these specifications are needed and used to come up with the loop filter component values shown in Figure 33.

The loop filter output drives the VCO, which in turn is fed back to the RF input of the PLL synthesizer. It also drives the RF output terminal. A T-circuit configuration provides 50 Ω matching between the VCO output, the RF output, and the RF_{IN} terminal of the synthesizer.

In a PLL system, it is important to know when the system is in lock. In Figure 33, this is accomplished by using the MUXOUT signal from the synthesizer. The MUXOUT pin can be programmed to monitor various internal signals in the synthesizer. One of these is the LD or lock-detect signal.

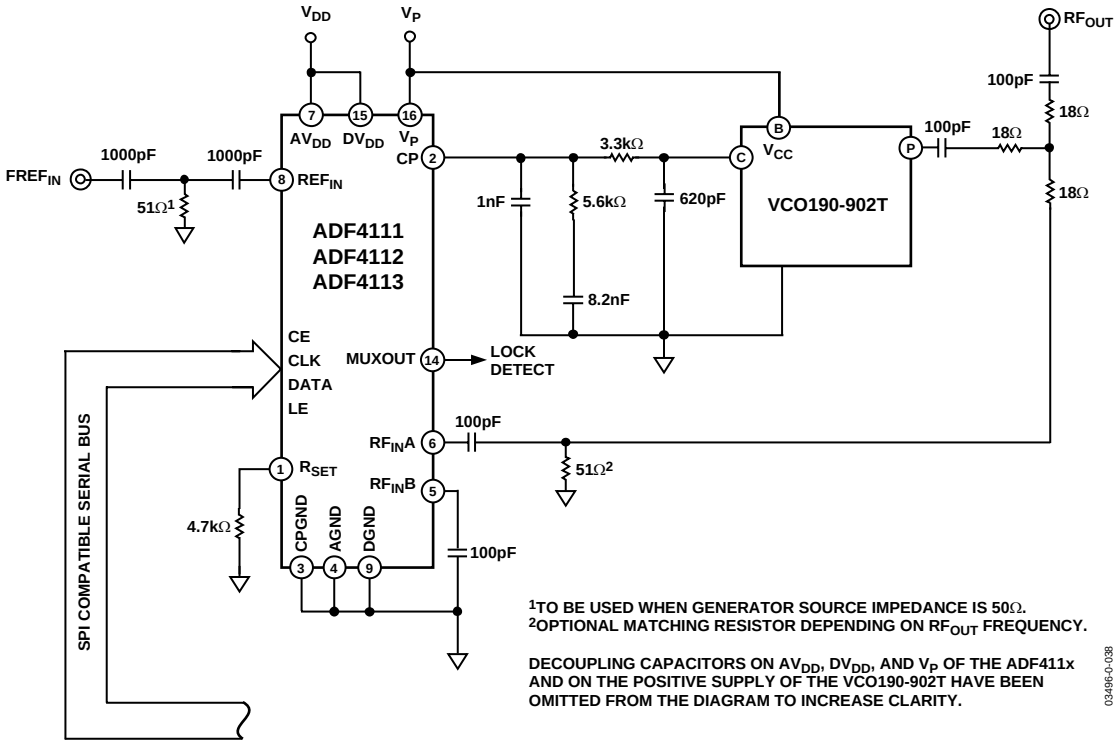


Figure 33. Local Oscillator for GSM Base Station

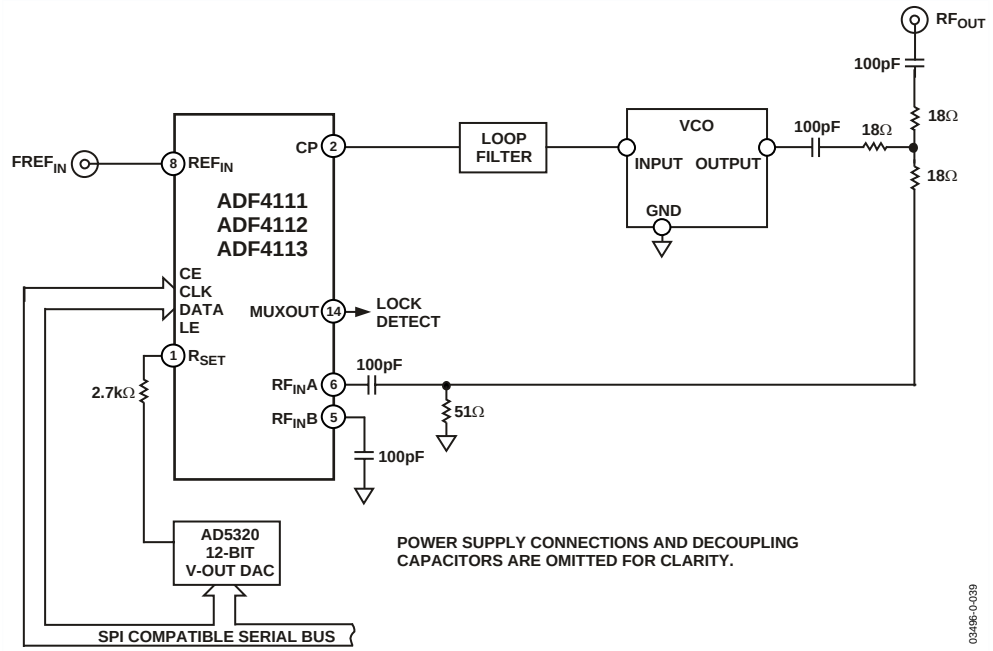


Figure 34. Driving the R_{SET} Pin with a D/A Converter

USING A D/A CONVERTER TO DRIVE THE R_{SET} PIN

A D/A converter can be used to drive the R_{SET} pin of the ADF4110 family, thus increasing the level of control over the charge pump current, I_{CP}. This can be advantageous in wide-band applications where the sensitivity of the VCO varies over the tuning range. To compensate for this, the I_{CP} may be varied to maintain good phase margin and ensure loop stability. See Figure 34.

SHUTDOWN CIRCUIT

The attached circuit in Figure 35 shows how to shut down both the ADF4110 family and the accompanying VCO. The ADG701 switch goes closed circuit when a Logic 1 is applied to the IN input. The low cost switch is available in both SOT-23 and MSOP packages.

WIDEBAND PLL

Many of the wireless applications for synthesizers and VCOs in PLLs are narrow band in nature. These applications include the various wireless standards like GSM, DSC1800, CDMA, and WCDMA. In each of these cases, the total tuning range for the local oscillator is less than 100 MHz. However, there are also wideband applications for which the local oscillator could have a tuning range as wide as an octave. For example, cable TV tuners have a total range of about 400 MHz. Figure 36 shows an application where the ADF4113 is used to control and program the Micronetics M3500-2235. The loop filter was designed for an RF output of 2900 MHz, a loop bandwidth of 40 kHz, a PFD frequency of 1 MHz, I_{CP} of 10 mA (2.5 mA synthesizer I_{CP} multiplied by the gain factor of 4), VCO K_D of 90 MHz/V (sensitivity of the M3500-2235 at an output of 2900 MHz), and a phase margin of 45°C.

In narrow-band applications, there is generally a small variation in output frequency (generally less than 10%) and a small variation in VCO sensitivity over the range (typically 10% to 15%). However, in wideband applications, both of these parameters have a much greater variation. In Figure 36, for example, there is a −25% and +17% variation in the RF output from the nominal 2.9 GHz. The sensitivity of the VCO can vary from 120 MHz/V at 2750 MHz to 75 MHz/V at 3400 MHz (+33%, −17%). Variations in these parameters change the loop bandwidth. This in turn can affect stability and lock time. By changing the programmable I_{CP}, it is possible to get compensation for these varying loop conditions and ensure that the loop is always operating close to optimal conditions.

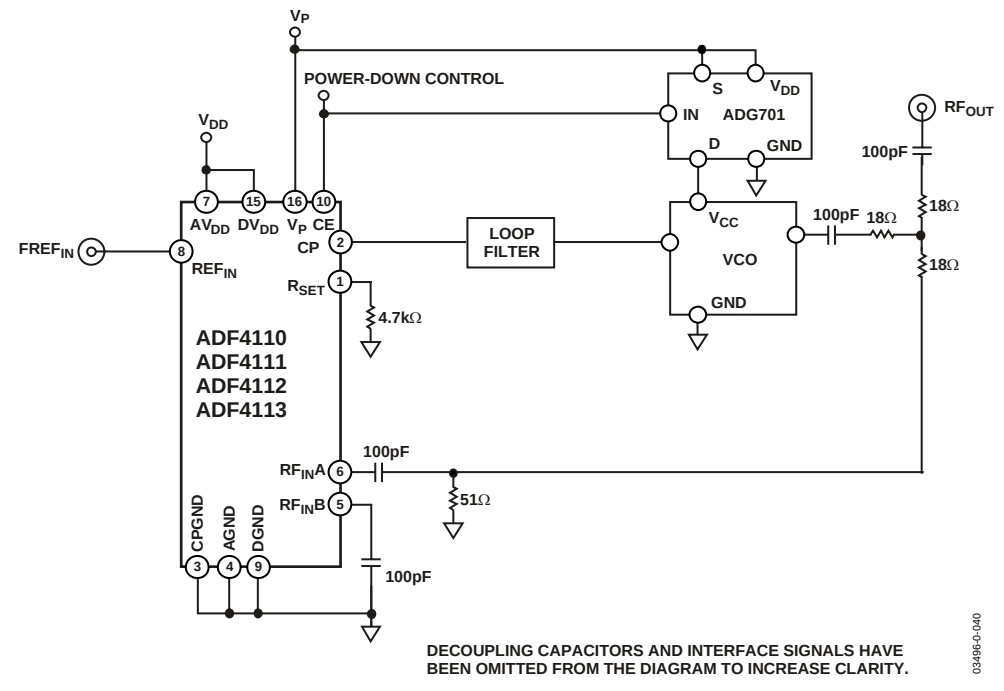


Figure 35. Local Oscillator Shutdown Circuit

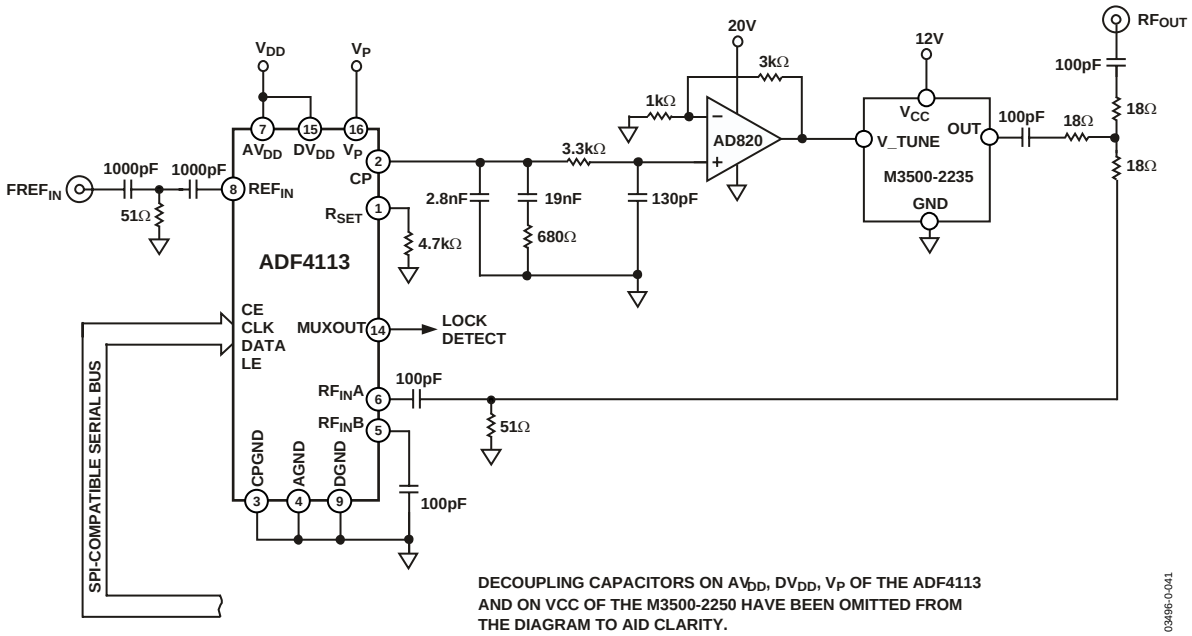


Figure 36. Wideband Phase-Locked Loop

DIRECT CONVERSION MODULATOR

In some applications, a direct conversion architecture can be used in base station transmitters. Figure 37 shows the combination available from ADI to implement this solution.

The circuit diagram shows the AD9761 being used with the AD8346. The use of dual integrated DACs such as the AD9761 with specified ±0.02 dB and ±0.004 dB gain and offset matching characteristics ensures minimum error contribution (over temperature) from this portion of the signal chain.

The local oscillator (LO) is implemented using the ADF4113. In this case, the OSC 3B1-13M0 provides the stable 13 MHz reference frequency. The system is designed for a 200 kHz channel spacing and an output center frequency of 1960 MHz. The target application is a WCDMA base station transmitter.

Typical phase noise performance from this LO is −85 dBc/Hz at a 1 kHz offset.

The LO port of the AD8346 is driven in single-ended fashion. LOIN is ac-coupled to ground with the 100 pF capacitor; LOIP is driven through the ac coupling capacitor from a 50 Ω source. An LO drive level of between −6 dBm and −12 dBm is required. The circuit of Figure 37 gives a typical level of −8 dBm.

The RF output is designed to drive a 50 Ω load but must be ac-coupled as shown in Figure 37. If the I and Q inputs are driven in quadrature by 2 V p-p signals, the resulting output power is around −10 dBm.

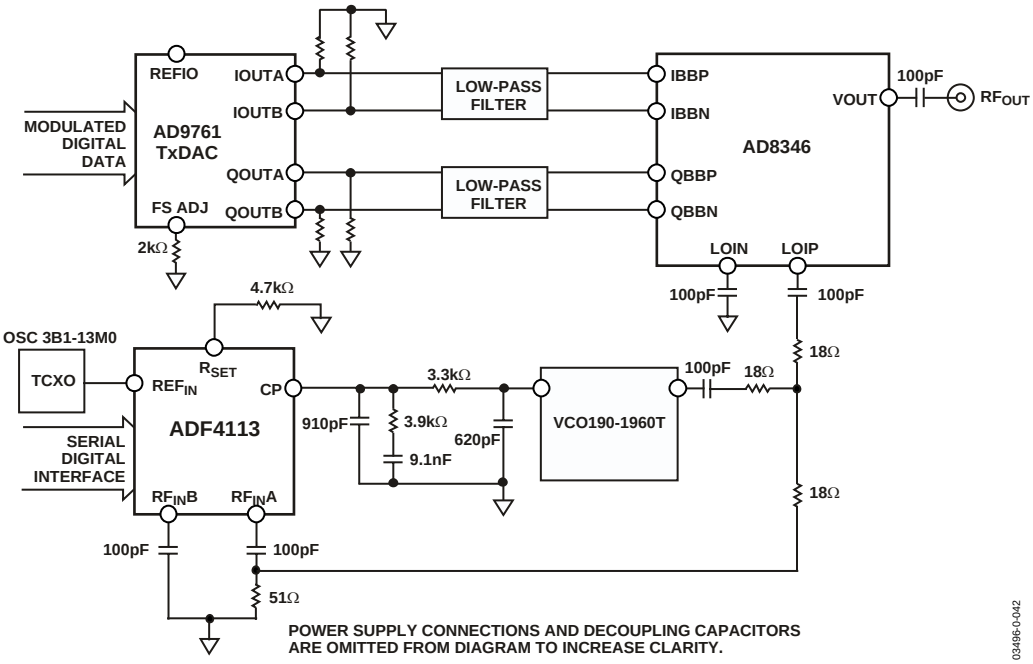


Figure 37. Direct Conversion Transmitter Solution

INTERFACING

The ADF4110 family has a simple SPI® compatible serial interface for writing to the device. SCLK, SDATA, and LE control the data transfer. When latch enable (LE) goes high, the 24 bits that have been clocked into the input register on each rising edge of SCLK get transferred to the appropriate latch. See Figure 2 for the timing diagram and Table 5 for the latch truth table.

The maximum allowable serial clock rate is 20 MHz. This means that the maximum update rate possible for the device is 833 kHz, or one update every 1.2 µs. This is certainly more than adequate for systems that have typical lock times in the hundreds of microseconds.

ADuC812 Interface

Figure 38 shows the interface between the ADF4110 family and the ADuC812 MicroConverter®. Since the ADuC812 is based on an 8051 core, this interface can be used with any 8051 based microcontroller. The MicroConverter is set up for SPI master mode with CPHA = 0. To initiate the operation, the I/O port driving LE is brought low. Each latch of the ADF4110 family needs a 24-bit word. This is accomplished by writing three 8-bit bytes from the MicroConverter to the device. When the third byte has been written, the LE input should be brought high to complete the transfer.

When power is first applied to the ADF4110 family, three writes are needed (one each to the R counter latch, N counter latch, and initialization latch) for the output to become active.

I/O port lines on the ADuC812 are also used to control power-down (CE input), and to detect lock (MUXOUT configured as lock detect and polled by the port input).

When the ADuC812 is operating in the mode described above, the maximum SCLOCK rate of the ADuC812 is 4 MHz. This means that the maximum rate at which the output frequency can be changed is 166 kHz.

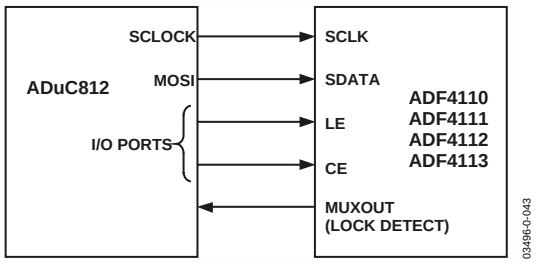


Figure 38. ADuC812 to ADF4110 Family Interface

ADSP-2181 Interface

Figure 39 shows the interface between the ADF4110 family and the ADSP-21xx digital signal processor. The ADF4110 family needs a 24-bit serial word for each latch write. The easiest way to accomplish this using the ADSP-21xx family is to use the auto buffered transmit mode of operation with alternate framing. This provides a means for transmitting an entire block of serial data before an interrupt is generated.

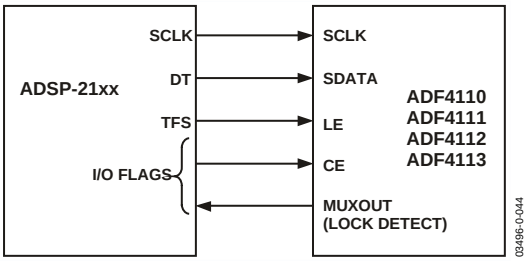


Figure 39. ADSP-21xx to ADF4110 Family Interface

Set up the word length for 8 bits and use three memory locations for each 24-bit word. To program each 24-bit latch, store the three 8-bit bytes, enable the auto buffered mode, and then write to the transmit register of the DSP. This last operation initiates the autobuffer transfer.

PCB DESIGN GUIDELINES FOR CHIP SCALE PACKAGE

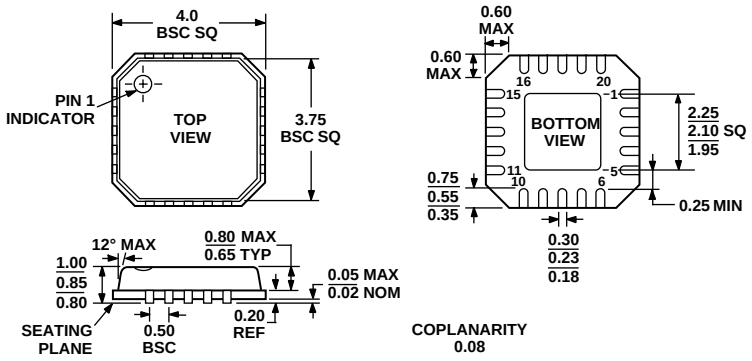
The lands on the chip scale package (CP-20) are rectangular. The printed circuit board pad for these should be 0.1 mm longer than the package land length and 0.05 mm wider than the package land width. The land should be centered on the pad. This ensures that the solder joint size is maximized.

The bottom of the chip scale package has a central thermal pad. The thermal pad on the printed circuit board should be at least as large as this exposed pad. On the printed circuit board, there should be a clearance of at least 0.25 mm between the thermal pad and the inner edges of the pad pattern. This ensures that shorting is avoided.

Thermal vias may be used on the printed circuit board thermal pad to improve thermal performance of the package. If vias are used, they should be incorporated in the thermal pad at 1.2 mm pitch grid. The via diameter should be between 0.3 mm and 0.33 mm, and the via barrel should be plated with 1 oz. copper to plug the via.

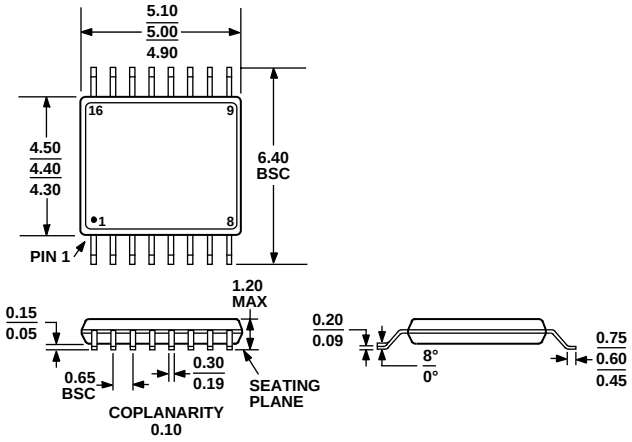
The user should connect the printed circuit board thermal pad to AGND.

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-220-VGGD-1

Figure 40. 20-Lead Lead Frame Chip Scale Package [LFCSP]
(CP-20-1)
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-153AB

Figure 41. 16-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-16)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
ADF4110BRU	–40°C to +85°C	Thin Shrink Small Outline Package	RU-16
ADF4110BRU-REEL	–40°C to +85°C	Thin Shrink Small Outline Package	RU-16
ADF4110BRU-REEL7	-40°C to +85°C	Thin Shrink Small Outline Package	RU-16
ADF4110BCP	–40°C to +85°C	Lead Frame Chip Scale Package	CP-20
ADF4110BCP -REEL	–40°C to +85°C	Lead Frame Chip Scale Package	CP-20
ADF4110BCP-REEL7	–40°C to +85°C	Lead Frame Chip Scale Package	CP-20
ADF4111BRU	–40°C to +85°C	Thin Shrink Small Outline Package	RU-16
ADF4111BRU-REEL	–40°C to +85°C	Thin Shrink Small Outline Package	RU-16
ADF4111BRU-REEL7	–40°C to +85°C	Thin Shrink Small Outline Package	RU-16
ADF4111BCP	–40°C to +85°C	Lead Frame Chip Scale Package	CP-20
ADF4111BCP-REEL	–40°C to +85°C	Lead Frame Chip Scale Package	CP-20
ADF4111BCP-REEL7	–40°C to +85°C	Lead Frame Chip Scale Package	CP-20
ADF4112BRU	–40°C to +85°C	Thin Shrink Small Outline Package	RU-16
ADF4112BRU-REEL	–40°C to +85°C	Thin Shrink Small Outline Package	RU-16
ADF4112BRU-REEL7	–40°C to +85°C	Thin Shrink Small Outline Package	RU-16
ADF4112BRUZ[1]	–40°C to +85°C	Thin Shrink Small Outline Package	RU-16
ADF4112BRUZ[1]-REEL	–40°C to +85°C	Thin Shrink Small Outline Package	RU-16
ADF4112BRUZ[1]-REEL7	–40°C to +85°C	Thin Shrink Small Outline Package	RU-16
ADF4112BCP	–40°C to +85°C	Lead Frame Chip Scale Package	CP-20
ADF4112BCP-REEL	–40°C to +85°C	Lead Frame Chip Scale Package	CP-20
ADF4112BCP-REEL7	–40°C to +85°C	Lead Frame Chip Scale Package	CP-20
ADF4113BRU	–40°C to +85°C	Thin Shrink Small Outline Package	RU-16
ADF4113BRU-REEL	–40°C to +85°C	Thin Shrink Small Outline Package	RU-16
ADF4113BRU-REEL7	–40°C to +85°C	Thin Shrink Small Outline Package	RU-16
ADF4113BRUZ[1]	–40°C to +85°C	Thin Shrink Small Outline Package	RU-16
ADF4113BRUZ[1]-REEL	–40°C to +85°C	Thin Shrink Small Outline Package	RU-16
ADF4113BRUZ[1]-REEL7	–40°C to +85°C	Thin Shrink Small Outline Package	RU-16
ADF4113BCP	–40°C to +85°C	Lead Frame Chip Scale Package	CP-20
ADF4113BCP-REEL	–40°C to +85°C	Lead Frame Chip Scale Package	CP-20
ADF4113BCP-REEL7	–40°C to +85°C	Lead Frame Chip Scale Package	CP-20
ADF4113BCHIPS	–40°C to +85°C	DIE	
EVAL-ADF4112EB1		Evaluation Board	
EVAL-ADF4113EB1		Evaluation Board	
EVAL-ADF4113EB2		Evaluation Board	
EVAL-ADF411XEB1		Evaluation Board	

[1] Z = Pb-free part.

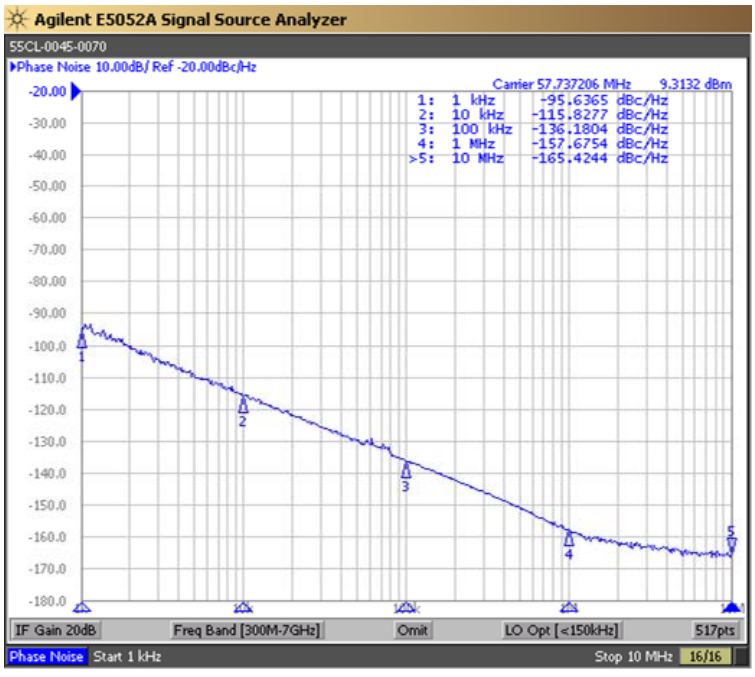
CRYSTEK MICROWAVE
A Division of Crystek Corporation

Voltage Controlled Oscillator-VCO
CVCO55CL-0045-0070

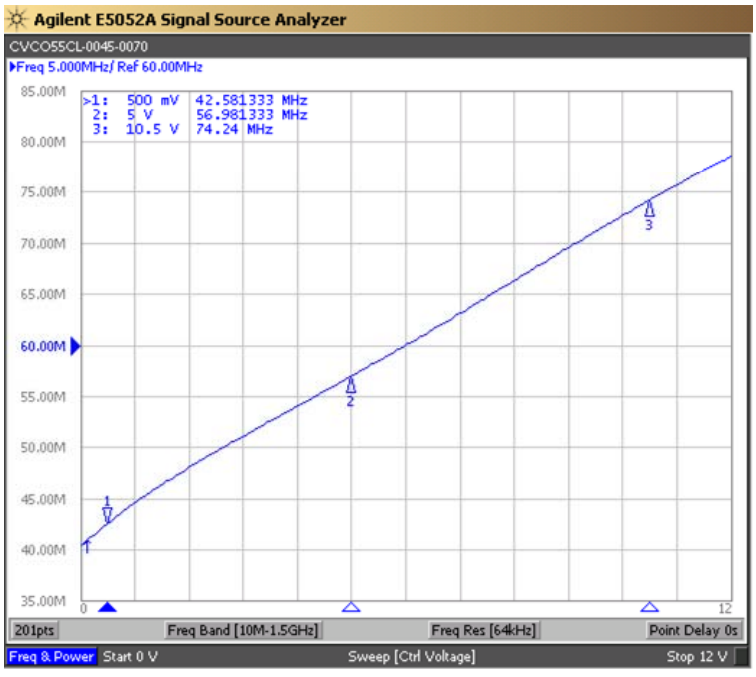
PERFORMANCE SPECIFICATION	MIN	TYP	MAX	UNITS
Lower Frequency:			45	MHz
Upper Frequency:	70			MHz
Tuning Voltage:	0.5		10.5	VDC
Supply Voltage:	4.75	5.0	5.25	VDC
Output Power:	+2.0	+5.0	+8.0	dBm
Supply Current:		15	22	mA
Harmonic Suppression (2nd Harmonic):		-10		dBc
Pushing:		0.5	1.0	MHz/V
Pulling, all Phases:		1.0	2.0	MHz pk-pk
Tuning Sensitivity:		4		MHz/V
Phase Noise @ 10kHz offset:		-115		dBc/Hz
Phase Noise @ 100kHz offset:		-134		dBc/Hz
Load Impedance:		50		Ω
Input Capacitance:			150	pF
Operating Temperature Range:	-40		+85	°C
Storage Temperature Range:	-45		+90	°C

RoHS Compliant

Phase Noise (1 Hz BW, Typical)



Tuning Curve (Typical)



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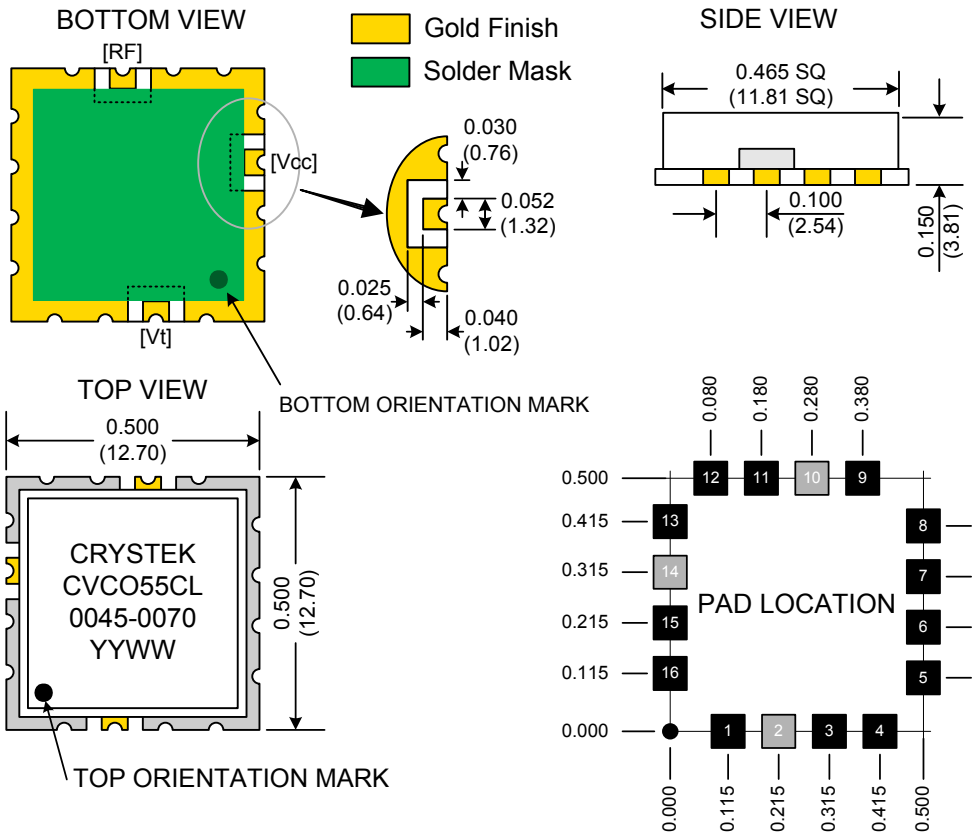
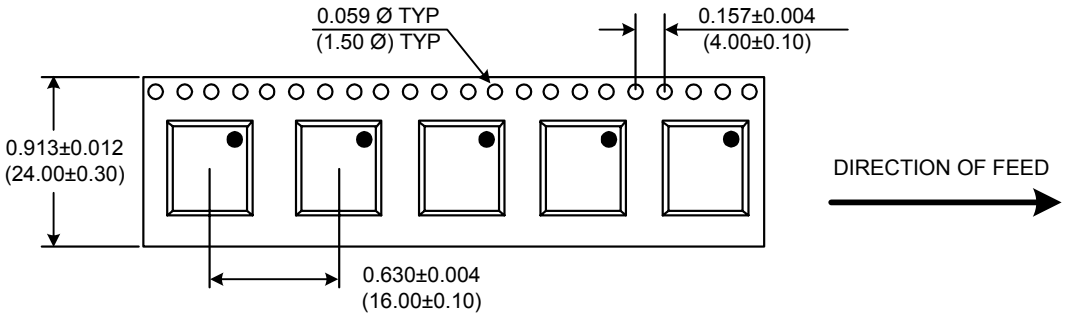
Voltage Controlled Oscillator-VCO
CVCO55CL-0045-0070



Pad	Connection
2	Vt
10	RF-OUTPUT
14	Vcc
Others	GROUND

- Unless otherwise specified, Dimensions are in: IN / (mm)
- Pad Location Dimensions are in: Inches

TAPE AND REEL



Drawing not to scale

Product Control:			
Crystek Part Number:	CVCO55CL-0045-0070	Release Date:	25-Feb-08
Revision Level:	D	Responsible:	C. Vales

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Digital Signature Generator for Mixed-Signal Testing

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Abstract—**A novel Digital Signature Generator to monitor two analog signals is proposed. The X-Y plane is divided by non linear boundaries into zones in order to generate the digital output for each analog (x,y) location. The circuit is based on a differential amplifier input stage modified by splitting the input MOSFETs. In this way two input signals are provided on each side of the differential stage. The output stage is based on a differential comparator with digital single ended output. The location and slope of the zone boundary depend on the relative sizes of the input transistors. The proposed signature generator is designed to be integrated in Built-In M-S testing and diagnosis circuits. Each monitor only requires 8 transistors for the input stage and 12 transistors for the digital output generator. The CUT intrusion on each monitored signal is reduced to the capacitive load of a single MOSFET. A STM 65 nm technology implementation is presented to demonstrate the viability of the proposal.**

Index Terms— **M-S Test, Digital signature generation, X-Y zoning, Multi-input comparator.**

I. INTRODUCTION

Monitoring internal signals of digital and mixed-signal circuits is becoming a widely used strategy in production testing and verification to increase the observability of the internal performance.

Built-in techniques for testing, signal integrity analysis and correlation of noisy signals are direct areas of application for such monitors. Internal monitors are widely used to increase the observability of signals embedded in large ICs, not easily accessed by primary I/Os.

Oscillation-test method [1], [2] current monitoring [3], [4] and Zoning [5], [6], have been used in the past for these purposes with good results in digital and mixed-signal applications. For testing purposes, X-Y Zoning, using straight lines to cut the plane into zones to monitor signal compositions (Lissajous curves), has been proposed [7], [8]. In the X-Y zone testing method, the monitoring of signals is based on the composition of two signals of the circuit, *x(t)* and *y(t)*, in a similar way that an oscilloscope in X-Y mode represents the evolution of two signals on the screen. If the composed signals are periodic with rational ratio of periods, the resultant curves are also periodic becoming the well-known Lissajous curves. The implementation of a straight line in the X-Y plane can be accomplished with the use of weighted adders and comparators. Several monitors have been proposed in the past for this purpose [10], [11], [12]. In these techniques, the Lissajous shape was used to select X-Y partitions delimited with straight lines. Recently, a generalization of the monitoring method for multiple variables using several hyperplanes has been proposed based on Lissajous compositions on a CUT with multitone excitation [9]. The method has been applied to verify parameter shifts in a physically programmable band-pass filter with selectable natural frequency. The experimental results showed a good prediction of the actual natural frequency with 0.34% error in the range of ±10% frequency shifts.

In this paper we investigate the possibilities of partitioning the X-Y plane using non-straight lines by taking advantage of the non-linear dependence of the nMOS transistor drain current I_D as a function of its gate-source voltage V_{GS}. The benefits of the proposal are the monitor small size and its low loading impact on monitored signals.

The paper is organized as follows. Section II is devoted to present the X-Y zoning method and the possible partition of the plane for testing purposes. A simplified mathematical model to analyze the possible lines, their shape and position are presented. Section III introduces the new structure of the signature generator, its on-chip implementation and performance evaluation using extensive electrical simulations. In section IV a summary of the work and conclusions about the results are presented.

II. CURRENT COMPARISON APPROACH.

Previous work on monitoring signals in the X-Y plane is based on dividing the X-Y plane by straight control lines that delimit the zones where the curve have points and the zones where the curve points are not expected. In this way, a large set of parametric and catastrophic defects can be detected by just checking whether the Lissajous curve remains in the specified zone or not. Figure 1 shows a Lissajous composition of a multitone input signal and the Low-Pass output of a Biquad filter. The the nominal shape is presented in Fig.1 a and the modified shape for 10% shift in the natural frequency of the filter is shown in Fig.1 b.. Monitoring is implemented using several control lines which divide the X-Y plane in multiple zones. The digital codes of the zones traversed by the Lissajous curve become the digital signature of the circuit. Digital signatures are efficiently accessed and

internally/externally processed. In this way the Mixed-Signal CUT test and parameter verification are facilitated.

Current comparison is a straightforward way to implement control lines composing two or more voltage signals. In contrast with voltage comparison, the easy way to add and subtract currents on nodes (Kirchorff's law) imply very simple structures. Furthermore, in CMOS applications, the quasi-quadratic current-voltage characteristic of MOS transistors, in saturation, enables the implementation of non linear curves to delimit zones in the X-Y plane. These characteristics facilitate the generation of efficient zone boundaries with low area overhead.

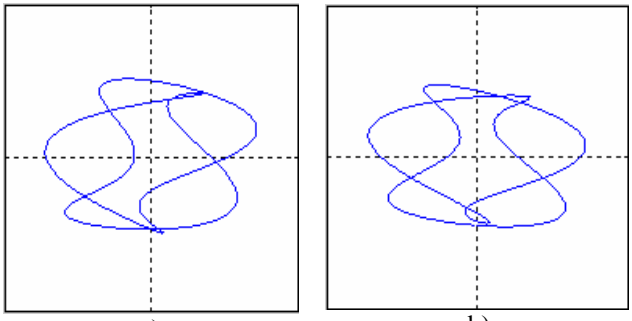

Figure 1. Lissajous composition of a multitone input signal and the Low-Pass output of a Biquad filter: a) Nominal shape, b) shape for 10% shift in the natural frequency of the filter.

In following paragraphs, we present a simplified model showing the principle of functionality of the proposed monitor.

A. Current Comparison Model

In order to illustrate the principle of operation of the monitor we will consider four voltage input signals V_1, V_2, V_3 and V_4, without loss of generality. As it will be discussed later, the number of monitored signals can be modified using the same principle of operation.

The basic architecture is similar to a source grounded differential pair or pseudo differential pair with two input transistors in each side [15], [16]. The input stage of the monitor is a differential-input differential-output stage with four input signals obtained splitting the input transistors in each side as indicated in Figure 2. The four-input monitor compares two currents generated by four voltages through the gate of nMOS transistors (transistors *M1*, *M2*, *M3* and *M4*) which deliver the current to be added at each branch of the differential input stage. Since the circuit is balanced, the output voltage will compare the currents of both branches of the monitor. Assuming equal transistor sizes, *M5* and *M8*, the switching point ($V_{out1} = V_{out2}$) will occur when:

$$I_5 = I_8 \tag{1}$$

where I_i denotes the current of transistor M_i, in Figure 2.

Using Kirchorff's law in the output nodes:

$$\begin{aligned} I_5 &= I_1 + I_2 - I_7 \\ I_8 &= I_3 + I_4 - I_6 \end{aligned} \tag{2}$$

due to the current mirroring of transistors (*M6, M5*) and (*M7, M8*) with a β ratio of their widths (0.9 in this design):

$$\begin{aligned} I_6 &= \beta I_5 \\ I_7 &= \beta I_8 \end{aligned} \tag{3}$$

Combining (1) with expressions (2) and (3):

$$(I_1 + I_2) - (I_3 + I_4) = (I_5 + \beta I_8) - (I_8 + \beta I_5) = 0 \tag{4}$$

From where we get,

$$I_1 + I_2 = I_3 + I_4 \tag{5}$$

In order to perform the current comparison analysis between both branches, the unified MOSFET model is used [13].

$$I_D = K\left(V_{GT}V_{MIN} - \frac{V_{MIN}^2}{2}\right)(1 + \lambda V_{DS}) \tag{6}$$

Where K is the product of the process transconductance and the MOS aspect ratio, V_{GT} stands for the difference, ($V_{GS} - V_{TH}$) being V_{TH} the threshold voltage. V_{MIN} is defined as:

$$V_{MIN} = \min\{V_{GT}, V_{DS}, V_{DSAT}\} \tag{7}$$

In the condition (5) and assuming all transistors working in saturation, the previous model takes the form,

$$I_D = \frac{K}{2}(V_{GS} - V_{TH})^2(1 + \lambda V_{DS}) \tag{8}$$

The gate-source voltage V_{GS}, is related with the input signal V_i in the way, $V_{GS} = V_i$, then

$$I_i = \frac{K_i}{2}(V_i - V_{THi})^2(1 + \lambda V_{DS}) \tag{9}$$

Combining (5) and (9) we obtain the commutation points that define the control line. Now, we consider four different transistor sizes, $K_1 \neq K_2 \neq K_3 \neq K_4$, identical threshold voltage $V_{TH1} = V_{TH2} = V_{TH3} = V_{TH4} = V_{THn}$, and constant parameter λ. As a result, we obtain a theoretical simplified expression for the current comparator as a function of the four input voltages:

$$K_1(V_1 - V_{THn})^2 + K_2(V_2 - V_{THn})^2 = K_3(V_3 - V_{THn})^2 + K_4(V_4 - V_{THn})^2 \tag{10}$$

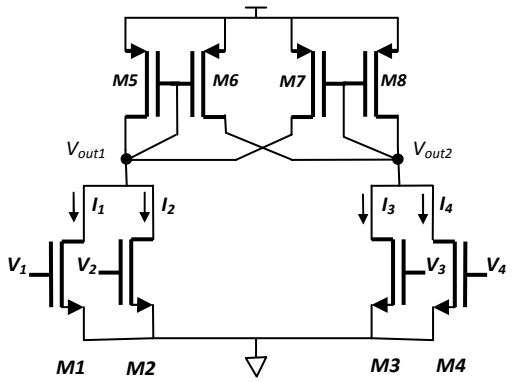

Figure 2. Four input current addition stage

The combination of transistor sizes with an adequate selection of input voltages allows controlling the position and shape of the control lines on the X-Y plane.

B. Curvature and position Control

To implement curves with different slopes and curvature in different positions of the X-Y plane two input voltages can act as the composed X-Y signals while the other two inputs act as positioning control signals. If the two composed signals are at the same side in (10) (V_1, V_2 or V_3, V_4), and the other two inputs are constant DC voltages, the curve has the general form:

$$a(x-h)^2 + b(y-h)^2 - c = 0 \qquad (11)$$

which is the equation of an ellipse centered in (*h, h);* in our case *(V_{THn}, V_{THn})*.

If the two composed signals are in opposite sides of the equality in (10) (V_1, V_3 / V_1, V_4 / V_2, V_3 or V_2, V_4 pairs), a hyperbola centered in (*h, h)* is obtained:

$$a(x-h)^2 - b(y-h)^2 - c = 0 \qquad (12)$$

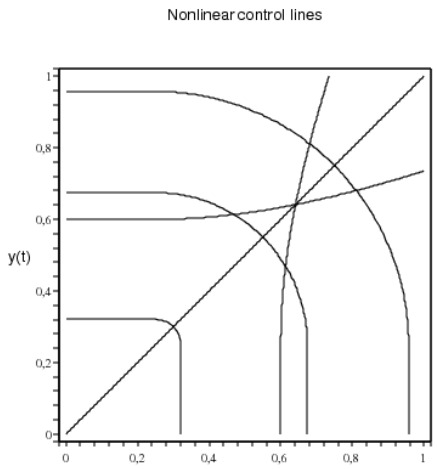

Figure 3. Mathematical model control lines for different parameters

In Figure 3 several theoretical ellipse and hyperbola segments are presented in the X-Y plane.

III. SIGNATURE GENERATOR IMPLEMENTATION

In order to implement the current comparison based monitor, with single ended digital output, we propose a circuit with the input stage shown in Figure 2 followed by the output stage circuit of Figure 4.

A. Monitor input stage

Based on the structure and analysis previously presented, this section is devoted to the generation of non linear control lines implemented in a 65nm CMOS technology. The position and shape of the control line is selected by choosing the input transistors and adequately sizing the input transistor dimensions (*W/L*). To maintain the balance of the active load, PMOS transistors, *M5* and *M8,* are equal sized transistors as well as *M6* and *M7*. In our design $W_{M6} = \beta W_{M5}$ and $W_{M7} = \beta W_{M8}$ with a width ratio of β =0.9. This feedback will improve the gain of the stage with no disturbance in the expected curves.

Table I summarizes the specific monitor configuration which defines de curves: transistor dimensions, applied (*x*, *y*) input signals and constant voltages at each comparator input. The sequence of digital outputs of the monitor generates the digital signature of the CUT.

B. Monitor Output stage

The output stage of the Monitor is a differential amplifier with single-ended output that digitalizes the differential output of the input stage. The main desired characteristics are simplicity, speed and wide common mode input range, thus, a simple sense amplifier structure has been chosen for the design. Three identical stages perform the final comparator function [14] as shown in Figure 4b.

The crossed inputs at the two first stages unbalance the voltage seen by the third stage which properly performs the comparison. The three modules are identical. Aspect ratio is 2000nm/180nm for the PMOS transistors and 1800nm/180nm for the NMOS ones.

The layout of the proposed signature generator implemented in STMicroelectronics 65nm-CMOS technology is depicted in Figure 5. In order to minimize mismatch effects, everyone transistor in Figure 2 has been split in four to balance the structure following two-dimension common-centroide design strategies [17]. According to the layout of Figure 5, distributions of NMOS and PMOS transistors are:

M1 M1 M4 M4	*M8 M8 M5 M5*
M3 M3 M2 M2	*M6 M6 M7 M7*
M2 M2 M3 M3	*M7 M7 M6 M6*
M4 M4 M1 M1	*M5 M5 M8 M8*

The area for the input stage is 53.54 μm^2 (11.64 µm × 4.6 µm) and for the output stage, 62.57 μm^2 (8.32 µm × 7.52 µm), summing a total of 116.1 μm^2 per monitor.

TABLE. 1. Input stage transistor dimensions W (nm) and applied voltages (V) for the curves depicted in Figure 6. All transistors with L=180 nm

	Transistor dimensions W/L (nm/180nm)				Applied input voltages (V)			
CURVE	M1	M2	M3	M4	V1	V2	V3	V4
1	3000	600	600	3000	Y axis	0.2	X axis	0.6
2	3000	600	600	3000	0.6	Y axis	0.2	X axis
3	1800	1800	1800	1800	Y axis	X axis	0.55	0.55
4	1800	1800	1800	1800	Y axis	X axis	0.3	0.3
5	1800	1800	1800	1800	Y axis	X axis	0.75	0.75
6	1800	1800	1800	1800	Y axis	0.5	X axis	0.5

.

C. *Simulation results*

As can be observed in Table I, changing the positions of the four input voltages, modifies curve shape and position. Figure 6 shows the layout simulation results of curves in Table I.

Comparing V_1 and V_3 voltages (one signal in each side of the differential pair) and setting V_2 and V_4 to a DC level, the resulting curves are segments of hyperboles (curves 1 and 2 of Figure 6). If both sides are symmetrical (transistor aspect ratio and constant voltages) we obtain a degenerated hyperbole that becomes a straight line cutting the plane at 45 degrees (curve 6 in Figure 6).

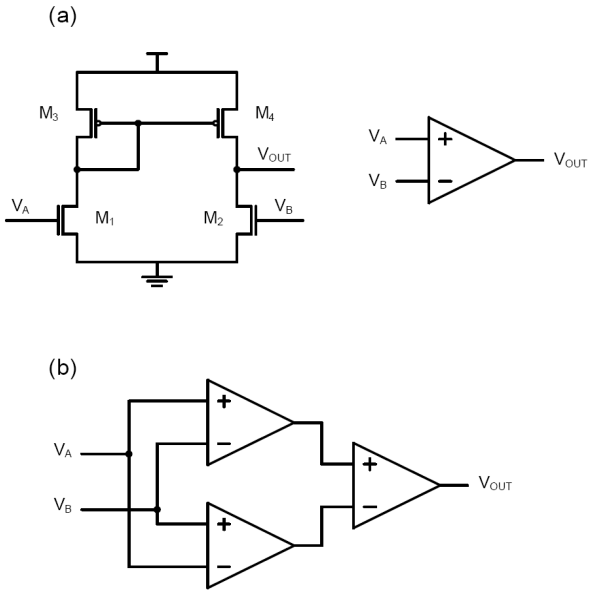

Figure.4 Output stage (a) One stage schematic and symbol (b) wiring of the three stages

On the other hand, we use both voltages in one branch of the differential pair (V_3, V_4), to control the line position, connecting two DC levels. With this configuration the quadratic addition of V_1 and V_2 happens and segments of ellipses are obtained as can be seen in curves 3 to 5, for different DC input voltages. Ellipses become a straight line for V_1 voltages below threshold voltage because M_1 transistor does not deliver current to the addition. Symmetrical straight line appears when V_2 voltage is below V_{TH}, then the ellipsis (curves 3 to 5) end with a straight line when reaching each axis.

Simulation results agree with the expected curves obtained through the mathematical model presented in Section II, considering the transistors working in saturation for the entire common mode range. Actual common mode input range is reduced by the V_{TH} of the input transistors. Below this voltage, *Mi* transistors enter the subthreshold region and, even

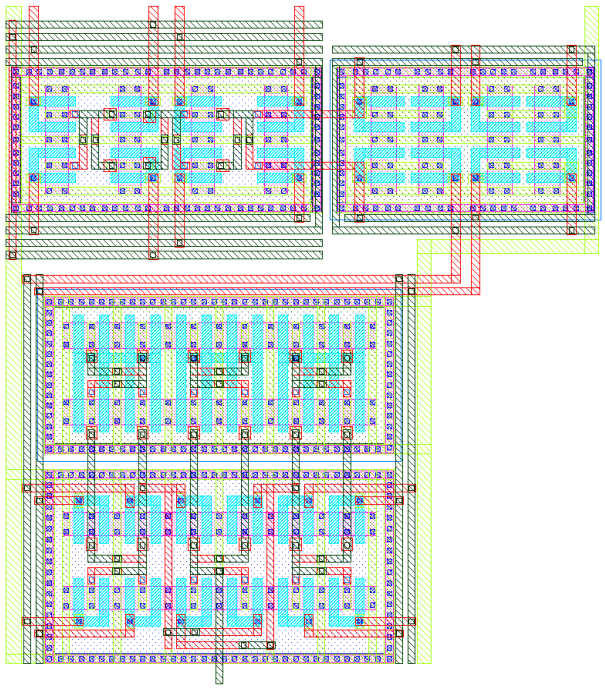

Figure 5. Digital Signature Generator Layout

though subthreshold currents are properly compared with the expected DC results, transient analysis reflects reduced timing parameters.

In the case study presented in Figure 6 with the monitor configurations in Table I we need six monitors one for each control line. Only two types of monitor circuit sizes are needed in order to cover the X-Y plane: One monitor with all four input transistor dimensions set to 1800nm/180nm (W/L); the second monitor with two transistors set to 600nm/180nm while the rest are 3000nm/180nm. Because the relation 600+3000 equals 1800+1800 the same load transistors (*M5, M6, M7 and M8*) are required.

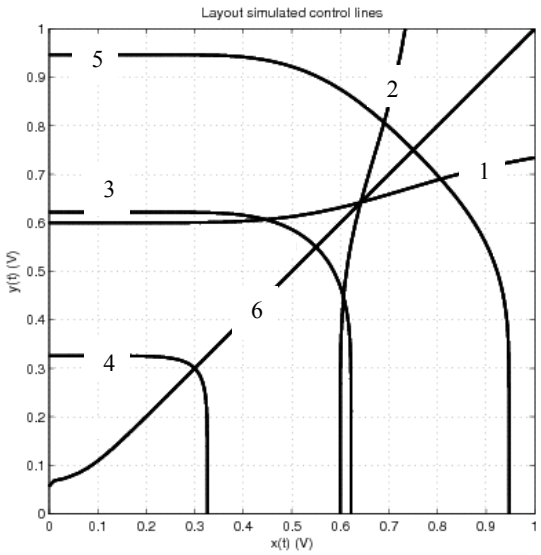

Figure 6. Layout simulated control lines of Table I.

D. Signature generation

The use of the proposed method for testing or parameter validation requires the use of several monitors, one for each curve cutting the X-Y plane. Depending on the Lissajous curve to be monitored the designer develops the adequate zones in the X-Y plane and then the specific monitors. The output of the monitors, sampled asynchronously during the evolution of the Lissajous cycle, represent the digital signature of the circuit. Using as example the control curves of Figure 6 combined with the nominal and the 10% parameter shift Lissajous curves of Figure 1 we obtain the composition represented graphically in Figure 7. The zones are codified in such a way that every monitor codifies a digital "1" when Lissajous curve is above the control line, or digital "0" when Lissajous curve is bellow the boundary. The outputs of the monitors processed by an asynchronous sampler, as indicated in Figure 8, deliver the periodic signatures shown in Table 2.

Due to the shape change of the Lissajous curve, and its position in the X-Y plane, in this example, there is a difference in the sequence length of the periodic output, as well as the zone codes reflecting different zone crossings.

The use of regression techniques as used in [9] will solve, in a general case, the mapping between measured signal (digital signature) and circuit parameter sets.

TABLE. 2. Digital Signatures of nominal and 10% natural frequency parametric variation in the case study of Figure 1 and Figure 6 for one period of the Lissajous curve.

Nominal
101010
101011
101111
101101
101111
101110
001110
001100
001000
001010
000010
100010
101010
101011
101111
101101
001101
001100
001000
001010

10% shift
101010
101011
101111
101101
001101
001100
001000
001010
101010
101011
101111
101101
101111
101110
001110
001100
001000
001010

IV. CONCLUSIONS

A low cost X-Y zoning Digital Signature generator has been proposed, based on a current comparator input stage followed by a differential voltage comparator output stage. The proposal converts the output differences of the input stage into binary signals used as digital signature of the monitor.

With a simple design, splitting the transistors of the input stage, only two different circuits are needed to cover adequately the X-Y plane. Zone boundaries are set by changing the input DC biasing voltages and/or the aspect ratio of the input transistors. Every monitor requires only 8 transistors for the input stage and 12 transistors for the digital output stage. The monitor area overhead is limited to 116,1 μm^2 which is an important reduction over voltage comparison alternatives. The loading on each monitored signals is limited to the capacitive load of the NMOS input transistors. With these monitors and fixed input biasing voltages the X-Y plane is partitioned into zones with non linear boundaries allowing effective monitoring of the Lissajous curves. The sequence of digital outputs of the monitor during one period of the Lissajous curve constitutes the digital signature of the CUT.

ACKNOWLEDGEMENTS

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REFERENCES

[1] Arabi K. , Kaminska B..”Oscillation-Test Strategy for Analog and Mixed-Signal Integrated Circuits”. *VLSI Test Symposium*, pp 476-482, 1996.

[2] Huertas G., Vazquez D., Rueda A., Huertas JL. “Oscillation-based test in bandpass oversampled A/D converters”. *Microelectronics Journal* Vol.34 pp 927–936. 2003.

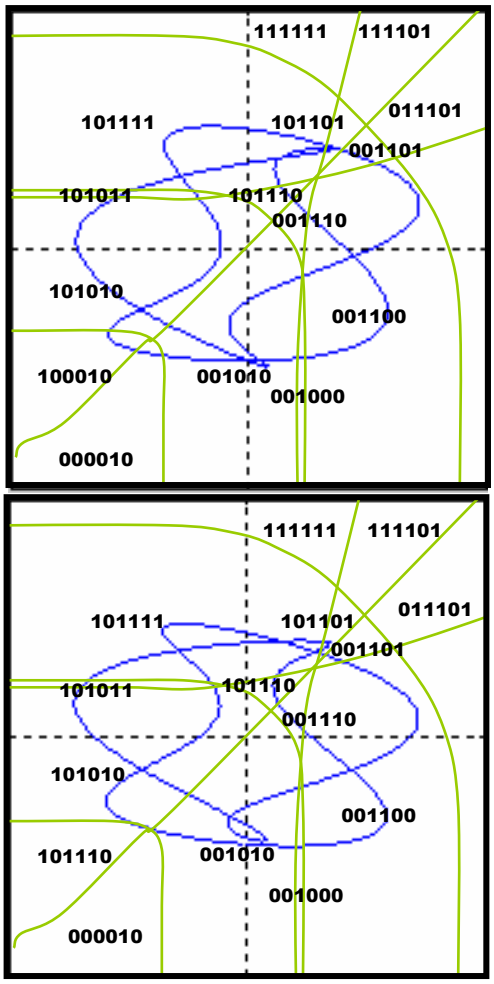

Figure 7 Lissajous curves evolving through control lines represented in Figure 6. Top curve represents the composition of multitone input voltage and nominal Low Pass output of a Biquad filter. Bottom curve is the same composition with a 10% parametric variation in the nominal frequency of the filter.

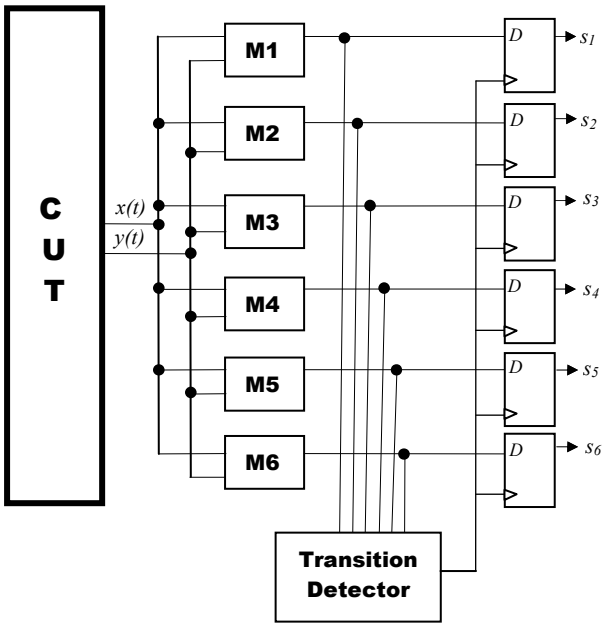

Figure 8. Asynchronous sampling of Digital signatures of the example in Figure 7

[3] De Venuto D., Kayak M.,Ohletz M.J. "Fault detection in CMOS/SOI mixed-signal circuits using the quiescent current test". *Microelectronics Journal* Vol.33 pp 387-397. 2002.

[4] Patel C., Singh A. Plusquellic J. "Defect detection under Realistic Leakage Models using Multiple IDDQ Measurements". *International Test Conference*. 2004, pp 319-328.

[5] Brosa A.; J. Figueras, "Digital Signature Proposal for Mixed-Signal Circuits". *International Test Conference*. pp 1041-1050, 2000

[6] Zenteno, A.; Champac, V.; Figueras, J, "Signal X-Y Zoning to Detect Inter-signal Delay Violations" *IEEE Letters* 2002, Vol. 38, Issue 14, pp. 686-688.

[7] A.M.Brosa, J.Figueras, "Digital Signature Proposal for Mixed-Signal Circuits" *Journal of Electronic Testing*, V 17, Nº 5, October 2001, pp 385-393

[8] Sanahuja, R; Barcons, V; Balado, L; Figueras, J. "Testing Biquad Filters under Parametric Shifts using X-Y Zoning". *International Mixed-Signal Testing Workshop* 2000, pp 283-288,.

[9] Balado, L.; Lupon, E.; Figueras, J.; Roca, M.; Isern, E.; Picos, R.;"Verifying Functional Specifications by Regression Techniques on Lissajous Test Signatures"*Circuits and Systems I: Regular Papers, IEEE Transactions on.* http://ieeexplore.ieee.org/stamp/stamp.jsp?arnumber=4663654&isnumber=4358591 Accepted for future publication.

[10] Sanahuja, R; Barcons, V; Balado, L; Figueras, J. "X-Y Zoning BIST: An FPAA Experiment". *IEEE International Mixed-Signal Testing Workshop* 2002, June 2002, pp 237-243,.

[11] Sanahuja R., Barcons V., Balado L., Figueras J. "Testing Biquad Filters under Parametric Shifts using X-Y Zoning" *International Mixed-Signal Testing Workshop* 2003, June 2003, pp 283-288.

[12] Sanahuja R., Barcons V., Balado L., Figueras J. "A Quasi Floating Gate Monitor for M-S BIST" *Latin American Testing Workshop 2005*, March 2005.

[13] J. M. Rabaey, A. P. Chandrakasan, B. Nikolic, "Digital Integrated Circuits: A Design Perspective", 2nd edition, Prentice Hall Electronics and VLSI Series, pp 58-71, 2003.

[14] J. P. Uyemura, "Introduction to VLSI Circuits and Systems", John Wiley & Sons, New York, pp 497-498, 2002.

[15] R. Jacob Baker "CMOS: Mixed-Signal Circuit Design" Wiley-IEEE, 2002, ISBN 0-471-22754-4.

[16] Yongwang Ding, Ramesh Harjani, "High-Linearity CMOS RF Front-End Circuits", *Springer US,* 2005, ISBN 978-0-387-23801-2.

[17] Di Long, Xianlong Hong, Sheqin Dong, "Optimal Two-Dimension Common Centroid Layout generation for MOS Transistors Unit-Circuit". IEEE International Symposium on Circuits and Systems, Vol. 3 pp 2999- 3002 , 2005.

Verifying Analog Circuits Based on a Digital Signature

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***Abstract*—Verification of analog circuit specifications is a challenging task requiring expensive test equipment and time consuming procedures. This paper presents a method for low cost parameter verification based on statistical analysis of a digital signature. A CMOS on-chip monitor and sampler circuit generates the digital signature of the CUT. The monitor composes two signals $(x(t), y(t))$ and divides the X-Y plane with nonlinear boundaries in order to generate a digital code for every analog (x, y) location. A metric to be used to discriminate the golden and defective signatures is also proposed. The metric is based on the definition of a discrepancy factor performing circuit parameter identification via statistical and pre-training procedures. The proposed method is applied to verify possible deviations on the natural frequency of a Biquad filter. Simulation results show the possibilities of the proposal.**

***Index Terms*—Mixed-Signal Test, Specification Verification, Monitoring, Nonlinear Zone Boundary.**

I. Introduction

As circuits increase in complexity, internal signals become deeper embedded into the structure what makes difficult their tracking from IC's primary inputs/outputs.

Analog and mixed-signal test, in parameter validation procedures, highlights the divorce between new technologies and available test methods. Manual test procedures and the high costs of analog automatic test equipments (AATEs) used for traditional specification based test require increasing resources. In order to assure quality, different methods have been proposed.

Oscillation based test (OBT) has been highly accepted and lately expanded by many authors [1]–[3]. The method consists on making some changes in the CUT which drive the system into a characteristic oscillation. Studying the resulting waveform many defects are detected. Yet, changes should be of minimum impact in the CUT's normal operation what may be a drawback of the method.

Otherwise, transient testing compares fault-free patterns with some characteristics of the CUT response to simple stimulus (step response or similar). Comparing responses, it is possible to discriminate between defective and non-defective circuits [4]–[6]. On the other hand, structural fault based tests look for the best stimuli to excite the fault. However, in many situations, fault-free does not mean specifications compliant [7], [8].

Alternate test methods [9], [10] try to overcome this analog test scenario using regression models as a technique to predict circuit specifications. Monitoring the power supply current has been used to detect faulty behavioural activity in the CUT [11]. Trying to improve the current resolution, some techniques use multiple chip supply paths [12] or study some interesting points of the circuit [13]. The impact of the monitor insertion into the supply lines and the increment of leakage currents in nanotechnologies limit the viability of these strategies.

In this paper we focus on built-in monitoring of analog signals combined with the on-chip digital signature generation in order to overcome AATE costs. Monitoring can be applied in production testing, diagnosis, parameter validation and signal integrity as well as in field and on-line test. Oscillation test method [2], [3], current monitoring [12], [13], and zoning [14], [15], have been used in the past for these purposes with promising results in digital and mixed-signal applications.

For test purposes, X-Y zoning uses straight lines to cut the plane into zones in order to monitor signal compositions (Lissajous curves) [16], [17]. Recently, a generalization of the monitoring method for multiple variables using several hyperplanes has been proposed. The study is based on Lissajous compositions in a CUT with multitone excitation [18].

In this context, we present: (a) A CMOS digital signature generator and (b) a metric to validate the circuit specifications. The latter is based on the definition of a discrepancy factor and its possibility to verify specifications via statistical and circuit pre-training methods.

The paper is organized as follows. Section II is devoted to present the X-Y zoning method, its possibilities and benefits in circuit testing. Section III introduces the new structure of the nonlinear boundary based signature generator. An on-chip implementation in a 65 nm technology is presented. Section IV is devoted to signature comparison through the defined discrepancy factor and its direct application to validate the natural frequency of a Biquad filter. In section V a summary of the work and conclusions are presented.

II. X-Y Zoning Method Description

In the X-Y zone testing method, signal monitoring is based on the composition of two signals of the circuit, $x(t)$ and $y(t)$, in a similar way an oscilloscope in X-Y mode represents the trace on the screen. If the ratio of the frequencies of the composed periodic signals is rational, the resultant curve is also periodic becoming the well-known Lissajous curves.

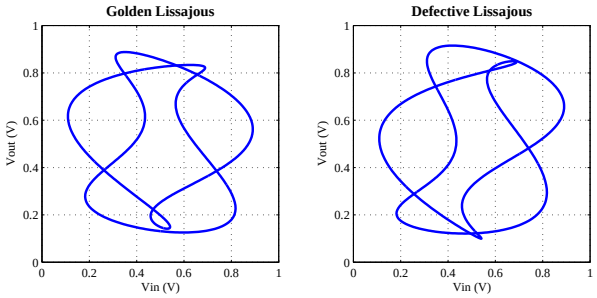

Fig. 1. Lissajous composition of a multitone input signal and the low pass output of a Biquad filter. Nominal shape (left) and 10% shift in the natural frequency of the filter (right).

Previous work on monitoring signals in the X-Y plane, is based on dividing the plane by straight lines that delimit the zones where the curve is allowed to have points and the zones where the points are not expected. As an example of application, the output of a low pass filter is represented as a function of its multitone input, generating the Lissajous curve of the CUT. The nominal fault-free curve is represented in the left side in Fig. 1. On the right, the figure shows the Lissajous curve with parameters of the filter out of specification tolerance. In this way, a large set of parametric and catastrophic defects can be detected by just checking whether or not the Lissajous curve remains in the specified zones. Using multiple partitions, the digital code of the zones traversed by the Lissajous curve becomes the digital signature of the circuit. Digital signatures are efficiently processed thereby reducing the overall mixed-signal test costs.

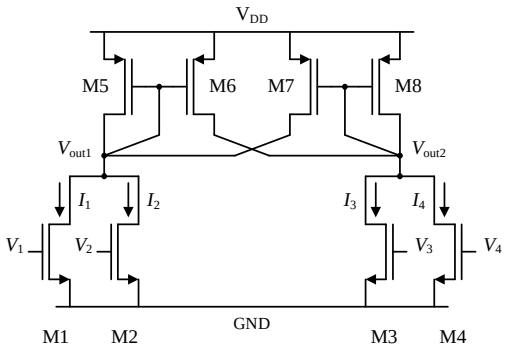

Fig. 2. Monitor schematic.

The implementation of a straight line in the X-Y plane has been accomplished with the use of weighted adders and comparators. Several monitors have been proposed in the past for this purpose [15], [17], [19]. In these approaches, the defective Lissajous was previously studied to select the best X-Y partitions delimited with straight lines. In [20] we proposed cutting the X-Y plane with non-straight boundaries. The method takes advantage of the nonlinear dependence of the NMOS transistor drain current I_{D} as a function of its gate-source voltage V_{GS}. The benefit is the simplification and the size reduction of the monitor.

In this work we go further presenting an efficient method for digital signature comparison and a metric for analog parameter validation.

III. Monitor for Digital Signature Generation

Current comparison is a straightforward way to implement control lines composing two or more voltage signals. In contrast with voltage comparison, the easy way to add and subtract currents (Kirchhorff's law) allows very simple structures to be used. Furthermore, in CMOS applications, the quasi-quadratic current-voltage characteristic of MOS transistors in saturation, enables the implementation of nonlinear curves to delimit zones in the X-Y plane. These characteristics make easier the generation of efficient zone boundaries and the reduction of area overhead.

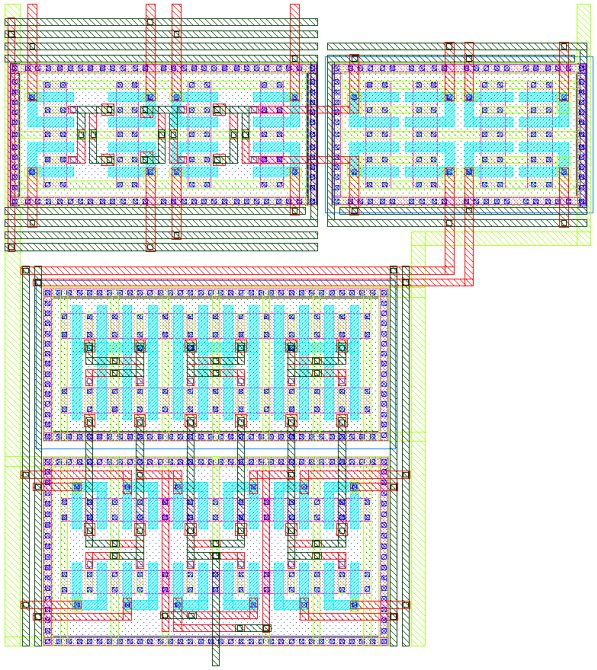

Fig. 3. Monitor layout.

A. Circuit Design

In order to implement the current comparison we propose the differential input stage of Fig. 2 [21], [22]. In the proposal, four input signals are used, even though the structure can be generalized by simply adding transistors in parallel.

This circuit with only two NMOS input transistors is the well-known "Source grounded differential pair" or "Pseudo

differential pair". For the PMOS, we use equal sized transistors M5 and M8 as active loads while equal sized transistors M6 and M7 perform the required feedback in order to improve the gain of the stage.

As shown in Fig. 2, input signals (V_1 to V_4) are directly connected to the gate of NMOS transistors (M1 to M4 respectively), which deliver the current to be added at each side of the differential input stage. Every transistor current is selected according to the needed curve parameters by adequately sizing the input transistor dimensions (W/L).

The layout of the proposed monitor, implemented in STMicroelectronics 65 nm CMOS technology, is depicted in Fig. 3. It also includes a high gain output stage. In the design, the transistors have been split in four to balance the structure in order to satisfy two-dimension common-centroid strategies [23] and thus minimize mismatch effects.

B. Commutation Curves

As can be observed in TABLE I, by interchanging positions of the four input voltages, curve shape and location are controlled. Fig. 4 shows the layout simulation results of the curves corresponding to circuits with the sizes and voltages specified in TABLE I.

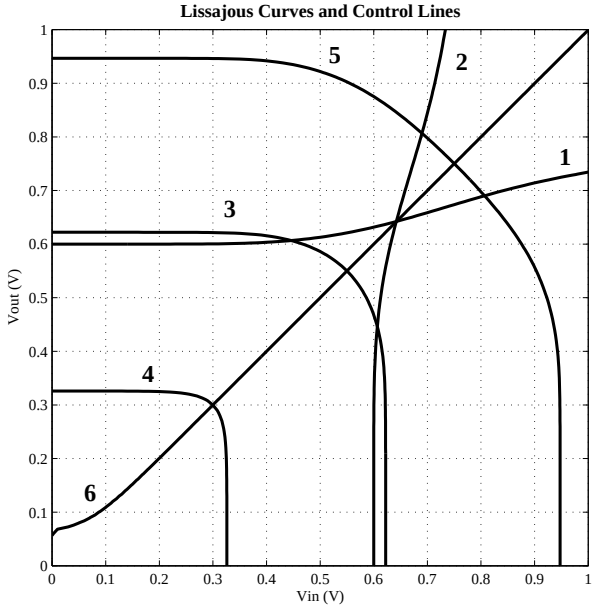

Fig. 4. Layout simulated control lines of TABLE I.

Comparing V_1 and V_3 voltages (one signal at each side of the differential pair) and setting V_2 and V_4 to a DC level, the resulting curves are segments of hyperbolae (curves 1 and 2 in Fig. 4). If both sides are symmetrical (transistor aspect ratio and constant voltages) we obtain a degenerated hyperbola that becomes a straight line cutting the plane at 45 degrees (curve 6 in Fig. 4).

On the other hand, we use both voltages in one branch of the differential pair (V_3, V_4), to control the line position, connecting two DC levels. With this configuration the quadratic addition of V_1 and V_2 happens and segments of ellipses are obtained as can be seen in curves 3 to 5. Ellipses become a straight line for input voltages below the threshold voltage because input transistors do not deliver current to the addition. Similar effect affects hyperbolae when reaching the axis.

TABLE I
INPUT TRANSISTOR DIMENSIONS AND APPLIED VOLTAGES FOR THE CURVES DEPICTED IN FIG. 4

	Transistor widths (nm) ($L = 180$ nm)				Applied input voltages (V)			
	M1	**M2**	**M3**	**M4**	V_1	V_2	V_3	V_4
1	300	600	600	300	Y axis	0.2	X axis	0.6
2	300	600	600	300	0.6	Y axis	0.2	X axis
3	1800	1800	1800	1800	Y axis	X axis	0.55	0.55
4	1800	1800	1800	1800	Y axis	X axis	0.3	0.3
5	1800	1800	1800	1800	Y axis	X axis	0.75	0.75
6	1800	1800	1800	1800	Y axis	0.5	X axis	0.5

IV. DIGITAL SIGNATURE PROCESSING

A. Basic Approach

In [20] a generalized test method using two observable signals was proposed. Test monitors the Lissajous trace across the nonlinearly divided X-Y plane comparing the resulting set of codes against the golden sequence. In the present work, in order to improve the resolution of the method for small parametric deviations, a new methodology and specification verifying process are proposed.

The zones in Fig. 4 are codified in such a way that every monitor delivers a digital "0" for the region that contains the origin, and a digital "1" for the complementary. Outputs from the monitors are processed by an asynchronous sampler which generates the periodic digital signature.

The signature of a CUT is defined as the sequence of pairs of zone code and time interval of permanence of the CUT's signals in a zone. This way, the signature registers the zone codes and the duration of the Lissajous curve in the same zone.

Formally, if the periodic Lissajous curve crosses k zones, $Z_1, Z_2, \ldots, Z_k$, and the time duration in each zone is denoted as Δ_i, $\forall i = 1, \ldots, k$, the CUT's signature is defined as,

$$\text{SIGNATURE} = \{(Z_1, \Delta_1), (Z_2, \Delta_2), \ldots, (Z_k, \Delta_k)\} \quad (1)$$

where Z_i represents the code of the i^{th} zone traversed and Δ_i represents the time duration in the i^{th} zone.

The implementation is schematized in Fig. 5, where an m-bit counter holds the time between code samples. Besides, in Fig. 6, the golden and +10% f_0 shift Lissajous curves can be observed when crossing the X-Y plane. The faulty trace

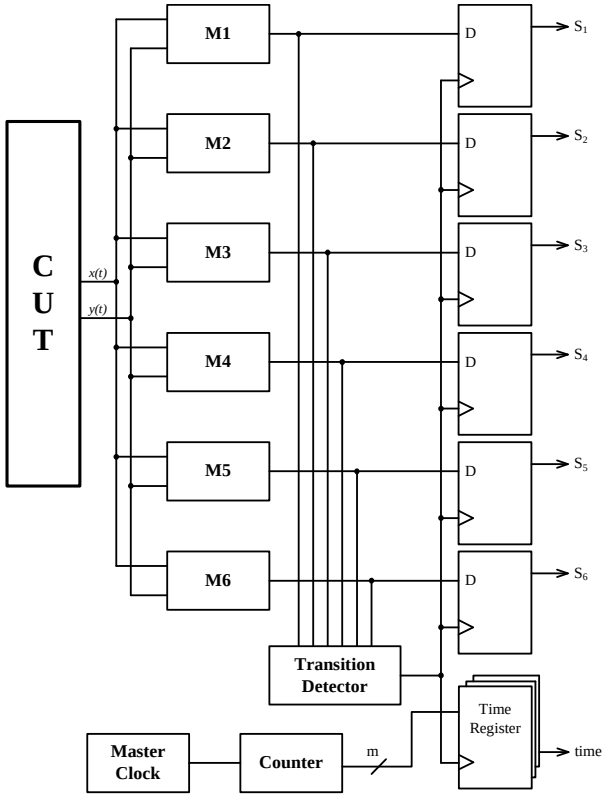

Fig. 5. Asynchronous sampling of digital signatures of the example depicted in Fig. 6 and Fig. 7.

draws on different zones at different instants which generates a different piecewise function.

The upper chronogram in Fig. 7 shows the zone code (in decimal) for any time t within the period of the Lissajous curves. This procedure in turn leads to a more precise and easier signature comparison when using an appropriate difference between function pairs. Due to the zone codification criterion, neighbour zones only vary in one bit. Furthermore, Hamming distance is suitable as can be observed in Fig. 7 lower chronogram, where the Hamming golden-defect distance is plotted during a period. Note the achievement of 2 (in Hamming distance sense) in the interval $[48, 50]\,\mu$s. This is because, in Fig. 6, the faulty trace reaches zone $111110_2\,(62_{10})$ instead of the sequence $011110_2\,(30_{10})$, $011100_2\,(28_{10})$, $111100_2\,(60_{10})$ what will define a free-defect Lissajous.

An indicator of signature difference is required. To achieve this goal we define the discrepancy factor as,

$$\mathrm{DF} = \int_0^T \mathrm{dist}(f, g)\, dt \tag{2}$$

where the functions $f(t)$ and $g(t)$ respectively represent the defective and golden zones defined within the period T of the Lissajous curves. Operator $\mathrm{dist}()$ is the Hamming distance of the codes at each time instant. It indicates the discrepancy of the defective and golden instantaneous codes weighted by the duration of interval in which the Lissajous curve remains in the same zone. This discrepancy factor is sensitive to the length of the curve. To avoid this handicap, a normalized version of the discrepancy factor will be used,

$$\mathrm{NDF} = \frac{1}{T} \int_0^T \mathrm{dist}(f, g)\, dt \tag{3}$$

The previous definition matches with the average value of the Hamming distance chronogram over the interval $[0, T]$. For the example of Fig. 7, a NDF of 0.102102 is obtained.

In order to investigate the reliability of the normalized discrepancy factor, extensive software simulation has been performed. It explores different degrees of deviation in the parameter under validation. Results are as expected: The discrepancy factor increases almost linearly with the amount of deviation and symmetrically with positive and negative defects, as can be seen in Fig. 8. Simulations on a Biquad filter with added white noise have been performed. In it, we use a 3σ spread of 1.5% of the supply voltage. Simulations show that deviations as low as 1% in the natural frequency of the filter are easily detected.

B. Parameter Verification Process

First, it is necessary to study if there is a difference between Hamming signatures of positive and negative defective circuits. To achieve this, a set of training defects have been considered: -10%, -9%,..., +9%, +10%. After computation, signatures are entirely equalized in time, as to obtain unique sized vectors. For instance, in our low pass filter, the resulting dimension of the previous set of defects is 136. Then, a set of 20 vectors of $\mathbb{R}^{136}$ have to be compared in order to identify significant difference between positive and negative defects. To this purpose, Euclidean distance has been used. Fig. 9 shows, in a 3D plot, the two-by-two comparison results. As can be seen, positive and negative defects respectively lay together in a $\mathbb{R}^{136}$ space. Distances between same types of defects are also smaller over those mixing different types of defects.

A simple method to scatter the two groups of defects is to compute a separation hyperplane. This data clustering method is performed by the calculation of the centre of gravity of every set and use it to define the hyperplane parameters. Let us respectively define z^+ and z^- as the centre of gravity of the positive and negative set of defects. In a N-dimensional vector space, a hyperplane takes the form,

$$\pi \equiv \sum_{i=1}^{N} n_i(z_i - p_i) = 0 \tag{4}$$

where $n = (n_1, \ldots, n_N)$ is a vector normal to π and $p = (p_1, \ldots, p_N)$ is any point within π. In this way, the following definitions become natural (see Fig. 10),

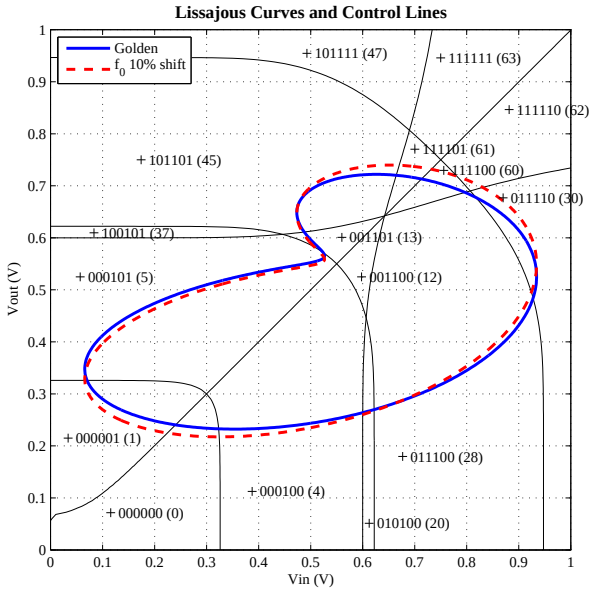

Fig. 6. Control lines with zone codification (in binary and decimal) and Lissajous compositions: golden and +10% shift in f_0.

$$n = z^+ - z^-, \quad p = \frac{z^+ + z^-}{2} \tag{5}$$

With the calculated π-hyperplane, parameter identification is easy because we only have to evaluate the resulting Hamming signature in the π equation. If the evaluation yields a positive number, the defect is positive and if it yields a negative value, the defect is negative. Defect quantity is determined by the use of the graphical data of Fig. 8.

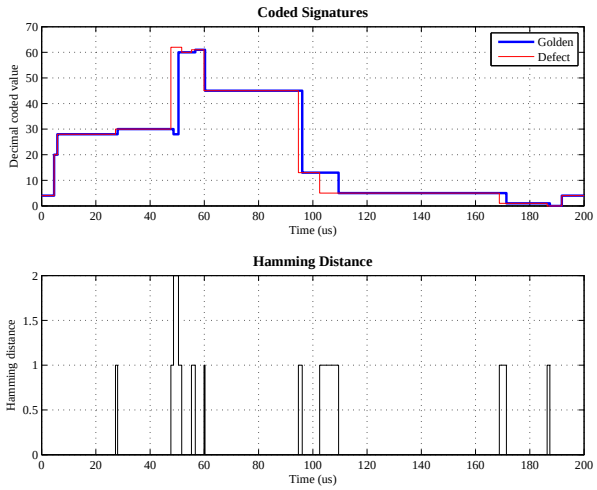

Fig. 7. Digital signatures and Hamming distances chronogram for +10% shift in f_0. NDF = 0.102102.

V. Conclusions

A low cost X-Y zoning monitor circuit has been proposed based on a four input current comparator and followed by a high gain stage. The monitor divides the X-Y plane with nonlinear boundaries into zones in order to generate a digital output for each analog (x, y) location. Zone boundaries can be adjusted by changing the biasing voltages and/or the aspect ratio of the input transistors.

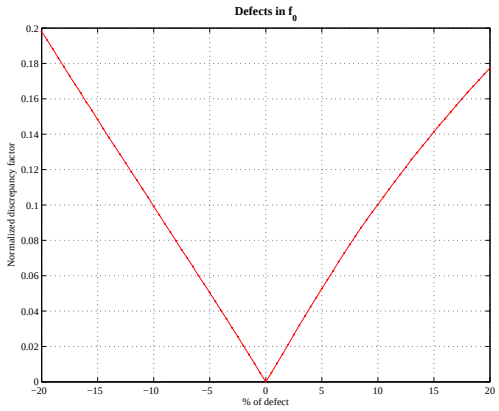

Fig. 8. Normalized discrepancy factor for defects in f_0.

In order to verify analog circuits with two observable signals, we define a metric to compare golden-defective digital signatures. Comparison is performed using the concept of Hamming distance and defines a discrepancy factor which extracts the amount of defect deviation. A normalized discrepancy factor (NDF) has been defined as the average value of the Hamming distance of the digital zone codes weighted by the time duration of each code.

Verification process is divided in two stages. The former is a data clustering method to compute a separation plane using a training set of defects which lay in opposite space regions. The latter verifies the circuit parameter deviation. This is performed using the mapping of the discrepancy factor and the quantity of deviation within the same sign group.

The method targets the verification of analog parameter specifications in analog and mixed-signal circuits.

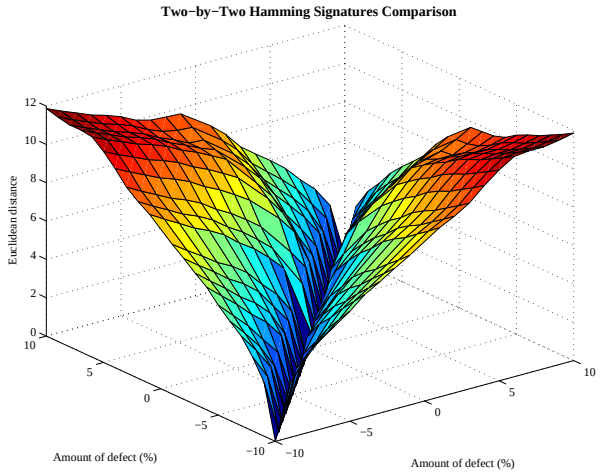

Fig. 9. Distance between pairs of Hamming signatures.

Results, based on the case example of a Biquad CUT, reflect the viability of the method. Accuracy is extremely dependant

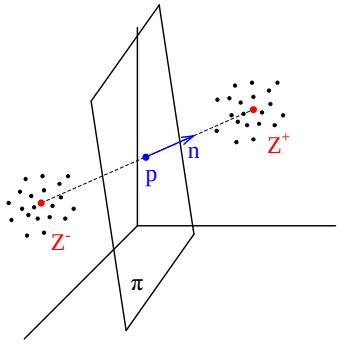

Fig. 10. Sketch of the separation plane in a three-dimensional vector space.

on the timing precision (counter size) and the signal quality. Simulations in a noisy environment, with a 3σ spread of 1.5% of the supply voltage, show encouraging results in detecting deviations as low as 1% in the natural frequency of the filter.

ACKNOWLEDGMENTS

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REFERENCES

[1] K. Arabi and B. Kaminska, "Oscillation-Test Strategy for Analog and Mixed-Signal Integrated Circuits," *VLSI Test Symposium*, pp. 476–482, 1996.

[2] A. Raghunathan, H. Shin, and J. A. Abraham, "Prediction of Analog Performance Parameters Using Oscillation Based Test," *Proceedings of the 22nd IEEE VLSI Test Symposium*, 2004.

[3] G. Huertas, D. Vázquez, A. Rueda, and J. L. Huertas, "Oscillation-based test in bandpass oversampled A/D converters," *Microelectronics Journal*, vol. 34, pp. 927–936, 2003.

[4] A. Walker, "A Step Response Based Mixed-Signal BIST Approach," *IEEE International Symposium on Defect and Fault Tolerance in VLSI Systems*, pp. 329–337, 2001.

[5] A. Walker and P. K. Lala, "A transition based BIST approach for passive analog circuits," *IEEE First International Symposium on Quality Electronic Design*, pp. 347–353, 2000.

[6] J. Font, J. Ginard, E. Isern, M. Roca, and E. Garcia, "A digital BIST for opamps embedded in mixed-signal circuits by analysing the transient response," *IEEE International Caracas Conference on Devices*, p. 1012, 2002.

[7] C. Hoffmann, "A new design flow and testability measure for the generation of a structural test and BIST for analogue and mixed-signal circuits," *Design, Automation and Test in Europe Conference and Exhibition*, pp. 197–204, 2002.

[8] K. Saab, N. Ben-Hamida, and B. Kaminska, "Parametric fault simulation and test vector generation," *Design, Automation and Test in Europe Conference and Exhibition*, pp. 650–656, 2000.

[9] P. N. Variyam and A. Chatterjee, "Specification-Driven Test Generation for Analog Circuits," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, pp. 1189–1201, 2000.

[10] R. Voorakaranam, S. S. Akbay, S. Bhattacharya, S. Cherubal, and A. Chatterjee, "Signature Testing of Analog and RF Circuits: Algorithms and Methodology," *IEEE Transactions on Circuits and Systems*, vol. 54, pp. 1018–1031, 2007.

[11] D. De Venuto, M. Kayak, and M. J. Ohletz, "Fault detection in CMOS/SOI mixed-signal circuits using the quiescent current test," *Microelectronics Journal*, vol. 33, pp. 387–397, 2002.

[12] G. O. D. Acevedo and J. Ramírez Angulo, "VDDQ: a built-in self-test scheme for analog on-chip diagnosis, compliant with the IEEE 1149.4 mixed-signal test bus standard," *International Caracas Conference on Devices*, p. 1026, 2002.

[13] C. Patel, A. Singh, and J. Plusquellic, "Defect Dtetection under Realistic Leakage Models using Multiple IDDQ Measurements," *International Test Conference*, 2004.

[14] A. Zenteno, V. Champac, and J. Figueras, "Signal X-Y Zoning to Detect Inter-Signal Delay Violations," *IEEE Letters*, vol. 38, pp. 686–688, 2002, issue 14.

[15] R. Sanahuja, V. Barcons, L. Balado, and J. Figueras, "X-Y Zoning BIST: An FPAA Experiment," *IEEE International Mixed-Signal Testing Workshop*, pp. 237–243, June 2002.

[16] A. M. Brosa and J. Figueras, "Digital Signature Proposal for Mixed-Signal Circuits," *Journal of Electronic Testing*, vol. 17, pp. 385–393, October 2001, number 5.

[17] R. Sanahuja, V. Barcons, L. Balado, and J. Figueras, "Testing Biquad Filters under Parametric Shifts using X-Y zoning," *Journal of Electronic Testing-Theory and Application*, vol. 20, pp. 257–265, 2005.

[18] L. Balado, E. Lupon, J. Figueras, M. Roca, E. Isern, and R. Picos, "Verifying Functional Specifications by Regression Techniques on Lissajous Test Signatures," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 56, pp. 754–762, April 2009, issue 4.

[19] R. Sanahuja, V. Barcons, L. Balado, and J. Figueras, "A Quasi Floating Gate Monitor for M-S BIST," *Latin American Testing Workshop*, March 2005.

[20] R. Sanahuja, A. Gómez, L. Balado, and J. Figueras, "Digital Signature Generator for Mixed-Signal Testing," *European Test Symposium*, 2009.

[21] C. Toumazou, F. G. Lidgey, and D. G. Haigh, *Analogue IC Design: The Current Mode Approach*. P. Peregrinus Ltd., 1990, london, UK.

[22] Y. Ding and R. Harjani, *High-Linearity CMOS RF Front-End Circuits*. Springer US, 2005, iSBN 978-0-387-23801-2.

[23] D. Long, X. Hong, and S. Dong, "Optimal Two-Dimension Common Centroid Layout generation for MOS Transistors Unit-Circuit," *IEEE International Symposium on Circuits and Systems*, vol. 3, pp. 2999–3002, 2005.

Analog Circuit Test Based on a Digital Signature

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***Abstract*—Production verification of analog circuit specifications is a challenging task requiring expensive test equipment and time consuming procedures. This paper presents a method for low cost on-chip parameter verification based on the analysis of a digital signature. A 65 nm CMOS on-chip monitor is proposed and validated in practice. The monitor composes two signals $(x(t), y(t))$ and divides the X-Y plane with nonlinear boundaries in order to generate a digital code for every analog (x, y) location. A digital signature is obtained using the digital code and its time duration. A metric defining a discrepancy factor is used to verify circuit parameters. The method is applied to detect possible deviations in the natural frequency of a Biquad filter. Simulated and experimental results show the possibilities of the proposal.**

***Index Terms*—Mixed-Signal Test, Specification Verification, Monitoring, Nonlinear Zone Boundary.**

I. Introduction

AS circuit complexity increases, internal signals become more embedded into the structure, making their tracking from IC's primary inputs/outputs difficult [1], [2].

Analog and mixed-signal parameter validation procedures highlight the divorce between current technologies and available test methods. The conditions attached to traditional specification based tests are manual, expensive and time consuming procedures which are applied to costly analog automatic test equipment (AATE). Built-in monitoring of analog signals, together with on-chip digital signature generation, aims to meet these challenges [3], [4].

A number of test techniques have been proposed. Oscillation based test (OBT) is widely accepted and has been lately expanded by several authors [5], [6]. Transient testing compares fault-free patterns with some characteristics of the CUT response to a simple stimulus [7], [8]. Some catastrophic structural fault based tests look for the best stimuli to excite the fault, typically shorts and opens. However, in many situations, fault-free does not mean specifications compliant, in particular with process variations in nanometric technologies [9]. Alternate test methods [10], [11] try to meet these analog test challenges by mapping easy-to-measure circuit parameters to circuit specifications by regression techniques. For test purposes, X-Y zoning uses straight lines to divide the plane into zones in order to monitor signal compositions (Lissajous curves) [12], [13]. Recently, a generalization of the monitoring method for multiple variables has been proposed. The study is based on Lissajous compositions in a CUT with multitone excitation [14].

Several approaches using oscillation test method [6], alternate test [11], and zoning [13], [14], have been used in combination with BIST techniques, yielding promising results in analog and mixed-signal applications.

The paper describes: (a) a CMOS digital signature generator based on X-Y zoning and (b) a test method based on the definition of a discrepancy factor which quantifies the difference between golden digital signatures and the monitor-generated signatures.

The paper is organized as follows. Section II presents the X-Y zoning method, its possibilities and benefits in circuit testing. Section III introduces the proposed signature generator structure and provides an on-chip nanometric implementation and some preliminary experimental results. Section IV is devoted to signature comparison through the discrepancy factor and its direct application to testing a Biquad filter. Section V summarizes the work and draws some conclusions.

II. X-Y Zoning Method Description

In the X-Y zone testing method, signal monitoring is based on the composition of two circuit signals, $x(t)$ and $y(t)$, in a similar way as an oscilloscope in X-Y mode represents the trace on the screen. If the frequency ratio of the periodic signals is rational, the resultant curve is also periodic, thus becoming the well-known Lissajous curve.

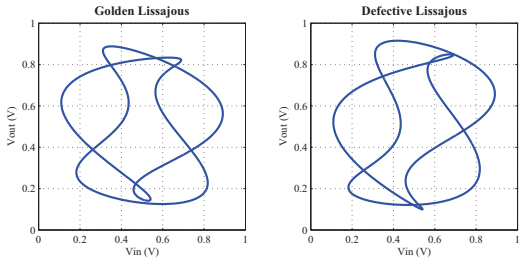

Fig. 1. Lissajous composition of a multitone input signal and the low pass output of a Biquad filter. Nominal shape (left) and 10% shift in the natural frequency of the filter (right).

In previous work on monitoring signals in the X-Y plane [12], [15], the plane is devided by straight lines that delimit the zones. As an example of application, the output of a low pass filter is plotted as a function of its multitone input, generating the Lissajous curve of the CUT. The nominal fault-free curve is represented on the left side of Fig. 1. On the right, the Lissajous curve with parameters of the filter out of specification tolerance is shown. In this way, a large set of parametric and catastrophic defects can be detected just by checking whether the Lissajous curve remains in the specified zones. Using multiple partitions, the digital code of the zones traversed by the Lissajous curve with the time interval spent by the Lissajous curve to traverse the zone becomes the digital signature of the circuit.

Straight lines are implemented in the X-Y plane using weighted adders and comparators. Several monitors have been proposed in the past for this purpose [13], [14]. In these approaches, Lissajous curves were previously studied to select the best X-Y partitions delimited by such lines. In order to simplify the monitors, non-straight boundaries have recently been proposed for the X-Y zones [15]. This method takes advantage of the nonlinear dependence of the nMOS transistor drain current I_{D} as a function of its gate-source voltage V_{GS}. The benefits are circuit simplification and significant reduction in monitor size.

In this work we present an efficient method for digital signature generation and a metric for analog parameter verification.

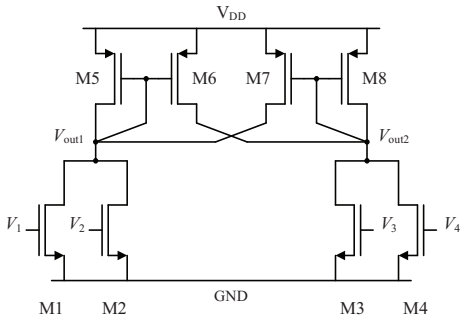

Fig. 2. Monitor circuit based on current comparison.

III. Monitor for Digital Signature Generation

Current comparison is a straightforward way to implement control curves by composing two or more voltage signals. In contrast with voltage comparison, addition and substraction of currents (Kirchhoff's law) allows the use of very simple structures. Furthermore, in CMOS applications, the quasi-quadratic current-voltage characteristic of MOS transistors in saturation enables the implementation of nonlinear curves to delimit zones in the X-Y plane.

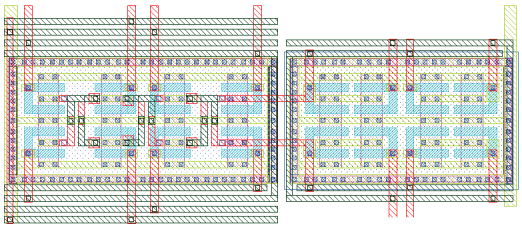

Fig. 3. Layout of the monitor in Fig. 2. It is implemented in STMicroelectronics 65 nm CMOS technology. The occupied area is $53.54\,\mu\mathrm{m}^2$.

A. Circuit Design

In order to compare currents, we propose the differential input stage of Fig. 2. In this implementation, four input signals are used, even though the structure can be generalized by simply adding transistors in parallel.

This circuit with only two nMOS input transistors is the well-known "Source grounded differential pair" or "Pseudo differential pair" [16]. For the pMOS, equal sized transistors M5 and M8 are used as active loads, while equal sized transistors M6 and M7 perform the required feedback to improve the gain of the stage.

As can be seen in Fig. 2, the input signals (V_1 to V_4) are directly connected to the gate of nMOS transistors (M1 to M4 respectively), which deliver the current to be added at each side of the differential input stage. Every transistor current is selected according to the required curve parameters by adequately sizing the input transistor dimensions (W/L).

The layout of the proposed monitor, implemented in STMicroelectronics 65 nm CMOS technology, is shown in Fig. 3. In this design, the transistors are split into four to balance the structure and thus satisfy two-dimension common-centroid strategies [17]. The area overhead is $53.54\,\mu\mathrm{m}^2$ ($11.64\,\mu\mathrm{m} \times 4.6\,\mu\mathrm{m}$). The design also includes a high gain output stage to digitalize the differential output of the monitor. The total area used per monitor is $116.1\,\mu\mathrm{m}^2$.

B. Control Curves

As can be observed in Table I, by interchanging positions of the four input voltages, curve shape and location are controlled. Fig. 4 shows the experimental curves for the configurations in Table I. Results lie in the predicted range for Monte Carlo simulations using the foundry technology statistical characterization.

Table I
Input configuration for the curves in Fig. 4

	Transistor widths (nm) ($L = 180$ nm)				Applied input voltages (V)			
	M1	**M2**	**M3**	**M4**	V_1	V_2	V_3	V_4
1	3000	600	600	3000	Y axis	0.2	X axis	0.6
2	3000	600	600	3000	0.6	Y axis	0.2	X axis
3	1800	1800	1800	1800	Y axis	X axis	0.55	0.55
4	1800	1800	1800	1800	Y axis	X axis	0.3	0.3
5	1800	1800	1800	1800	Y axis	X axis	0.75	0.75
6	1800	1800	1800	1800	Y axis	0	X axis	0

Comparing voltages V_1 and V_3 (one signal at each side of the differential pair) and setting V_2 and V_4 to a DC level, the resulting curves are segments of positive slope (curves 1 and 2 in Fig. 4). If both sides are symmetrical (transistor aspect ratio and constant voltages) we obtain a straight line cutting the plane at 45 degrees (curve 6). The distortion of curve 6 for small input voltages is caused by the subthreshold operation of the nMOS transistors.

When both voltages in one branch of the differential pair (V_3, V_4) are connected to DC levels, V_1 and V_2 are nonlinearly added, generating segments of negative slope as shown in curves 3 to 5. Boundary curves become a straight line for input voltages below the threshold voltage because the input transistors do not deliver current to the addition.

IV. Digital Signature

A. Signature Definition

The zones in the X-Y plane are codified so that every monitor delivers a digital "0" for the region containing the

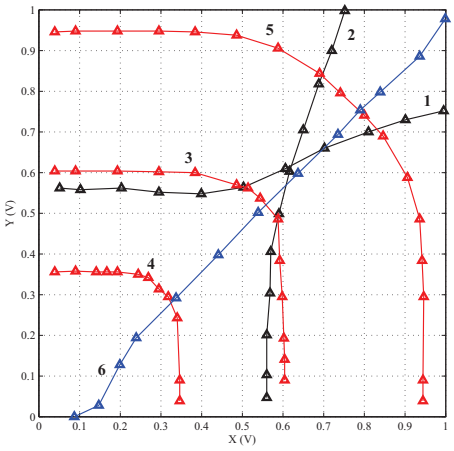

Fig. 4. Experimental control lines of TABLE I obtained for the monitor fabricated using STMicroelectronics 65 nm CMOS technology.

origin, and a digital "1" otherwise. The resulting zones and codes are shown in Fig. 4 and Fig. 6.

The signature of a CUT is defined as the sequence of pairs of zone code (Z_i) and time interval of permanence of the CUT's signals in the zone (Δ_i).

Formally, if the periodic Lissajous curve crosses k zones, $Z_1, Z_2, \ldots, Z_k$, and the time duration in each zone is denoted as Δ_i, $\forall i = 1, \ldots, k$, the CUT's signature is defined as,

$$\text{SIGNATURE} \equiv \{(Z_1, \Delta_1), (Z_2, \Delta_2), \ldots, (Z_k, \Delta_k)\}. \quad (1)$$

Monitor outputs are processed by an asynchronous capture which generates the digital signature. The implementation is illustrated in Fig. 5, where an m-bit counter holds the time between code captures.

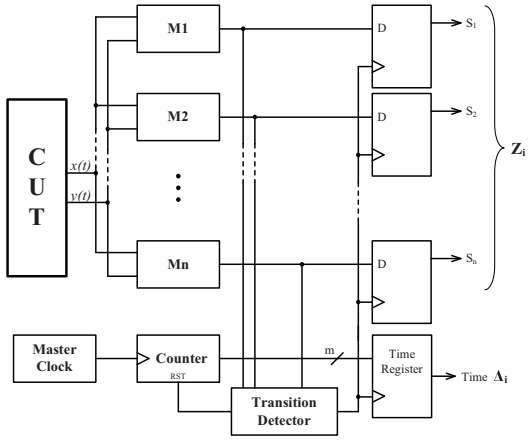

Fig. 5. Block diagram for asynchronous capture of digital signatures generating n-bit zone codes and m-bit time intervals.

In Fig. 6, the golden and +10% f_0 shift Lissajous curves evolve across the X-Y plane traversing different zones, delimited by nonlinear control curves, at different instants and thus generating different signatures.

Using the capture circuit of Fig. 5, the signatures of Fig. 7 are obtained for the defective and the defect-free curves. The chronogram in Fig. 7 shows the zone code for any time t within the period of the Lissajous curves.

B. Metric Definition

An indicator of signature discrepancies is required. We obtain it by defining the so-called normalized discrepancy factor as

$$\text{NDF} = \frac{1}{T}\int_0^T \mathrm{d_H}(S_O, S_G)\, dt, \quad (2)$$

where functions $S_O(t)$ and $S_G(t)$ respectively represent the observed defective and golden signatures defined within the period T of the Lissajous curves. Operator $\mathrm{d_H}()$ is the Hamming distance of the zone codes at each time instant. The NDF parameter indicates the discrepancy of the defective and golden instantaneous codes weighted by the duration of the time interval in which the Lissajous curve remains in the same zone.

The previous definition matches the average value of the Hamming distance chronogram over the interval $[0, T]$. For the example of Fig. 7, an NDF of 0.1021 is obtained.

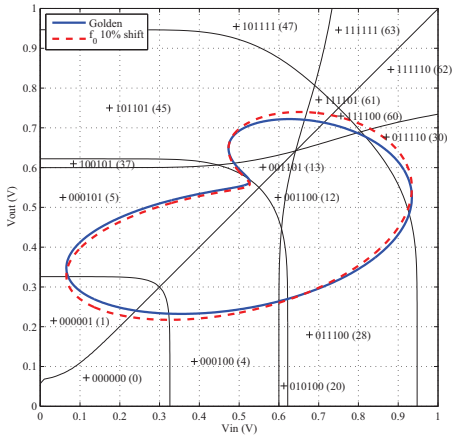

Fig. 6. Control curves with zone codification and Lissajous compositions: golden and +10% shift in f_0.

According to the zone codification criterion, neighbouring zones only differ in one bit. This is why the Hamming distance is suitable, as can be observed in the lower chronogram of Fig. 7, where the Hamming golden-defect distance is plotted over a period. Note a Hamming distance of 2 in the interval $[48, 50]$ μs (see Fig. 6) resulting from the faulty trace which reaches zone $111110_2\,(62_{10})$ instead of the sequence $011110_2\,(30_{10})$, $011100_2\,(28_{10})$, $111100_2\,(60_{10})$, which defines a defect-free Lissajous.

C. Parameter Verification Process

The NDF is used to evaluate the amount of deviation of the parameters under verification. Circuits with parameters meeting specifications are expected to have small NDF values. To evaluate the NDF effectiveness, extensive software simulations were performed on a Biquad filter circuit with

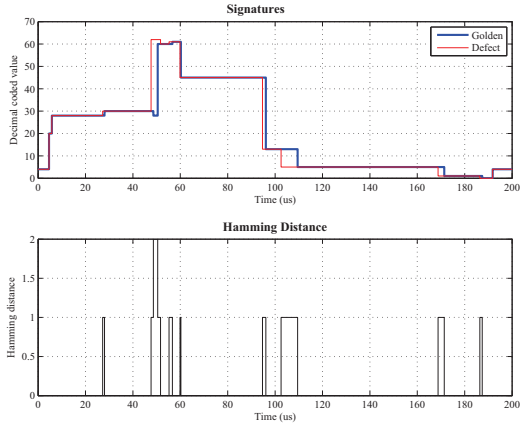

Fig. 7. Chronogram of digital signatures and Hamming distances for +10% shift in the f_0 parameter of a Biquad filter. NDF $= 0.1021$.

different degrees of deviation in the natural frequency of the filter. The discrepancy factor increases almost linearly with the amount of deviation and quite symmetrically with positive and negative f_0 parameter deviations, as can be seen in Fig. 8. The test decision is made by previously setting the desired level of tolerance and checking whether the NDF lies in the acceptance or rejection bands. Simulations conducted with high frequency white noise on the signals with null mean and a 3σ spread of $0.015\,\mathrm{V}$ show that deviations as low as 1% in the natural frequency of the filter are detected.

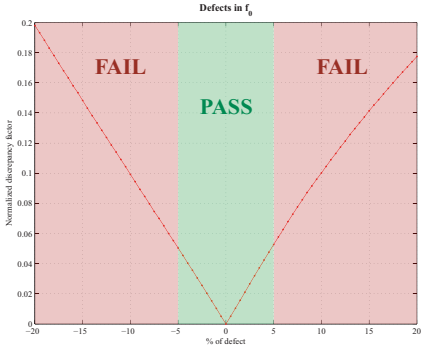

Fig. 8. Normalized discrepancy factor for defects in f_0.

V. Conclusions

In order to test analog circuits with two observable signals, we define a metric to compare digital signatures using the Hamming distance between the golden and CUT zone codes. A normalized discrepancy factor (NDF) characterizing the amount of parameter deviation is defined as the average value of the Hamming distance of the digital zone codes weighted by the time duration of each code. The test decision is made by mapping the discrepancy factor and the amount of deviation related to the acceptable band, as indicated in Fig. 8.

A low cost X-Y zoning monitor was designed and fabricated in STMicroelectronics 65 nm technology. The monitor is based on a four input current comparator followed by a high gain stage. The monitor divides the X-Y plane with nonlinear boundaries into zones to generate a digital output for each analog (x, y) location. Zone boundaries can be adjusted by changing the biasing voltages and/or the aspect ratio of the input transistors. Experimental measurements of the monitor zone boundaries were performed, yielding results in the range of the predicted Monte Carlo simulations values (process and mismatch) for STMicroelectronics 65 nm technology variability.

The method was applied on a Biquad Filter circuit to test the natural frequency parameter.

Acknowledgments

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References

[1] IEEE Standard for a Mixed-Signal Test Bus, IEEE std. 1149.4-1999.

[2] A. Sehgal, S. Ozev, and K. Chakrabarty, "Test infrastructure design for mixed-signal SOCs with wrapped analog cores," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 14, pp. 292–304, March 2006, issue 3.

[3] A. Valdés-Gracia, F. A. L. Hussien, J. Silva-Martínez, and E. Sánchez-Sinencio, "An Integrated Frequency Response Characterization System With a Digital Interface for Analog Testing," *IEEE Journal of Solid-State Circuits*, vol. 41, pp. 2301–2313, October 2006, issue 10.

[4] Chee-Kian Ong, Kwang-Ting Cheng, and L. C. Wang, "A new sigma-delta modulator architecture for testing using digital stimulus," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 51, pp. 206–213, January 2004, issue 1.

[5] K. Arabi and B. Kaminska, "Oscillation-Test Strategy for Analog and Mixed-Signal Integrated Circuits," *VLSI Test Symposium*, pp. 476–482, 1996.

[6] G. Huertas, D. Vázquez, A. Rueda, and J. L. Huertas, "Oscillation-based test in bandpass oversampled A/D converters," *Microelectronics Journal*, vol. 34, pp. 927–936, 2003.

[7] A. Walker, "A Step Response Based Mixed-Signal BIST Approach," *IEEE International Symposium on Defect and Fault Tolerance in VLSI Systems*, pp. 329–337, 2001.

[8] H. G. D. Stratigopoulos and Y. Makris, "Concurrent detection of erroneous responses in linear analog circuits," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 25, pp. 878–891, May 2006, issue 5.

[9] Fang Liu and S. Ozev, "Statistical Test Development for Analog Circuits Under High Process Variations," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 26, pp. 1465–1477, August 2007, issue 8.

[10] P. N. Variyam and A. Chatterjee, "Specification-Driven Test Generation for Analog Circuits," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, pp. 1189–1201, 2000.

[11] R. Voorakaranam, S. S. Akbay, S. Bhattacharya, S. Cherubal, and A. Chatterjee, "Signature Testing of Analog and RF Circuits: Algorithms and Methodology," *IEEE Transactions on Circuits and Systems*, vol. 54, pp. 1018–1031, 2007.

[12] A. M. Brosa and J. Figueras, "Digital Signature Proposal for Mixed-Signal Circuits," *Journal of Electronic Testing*, vol. 17, pp. 385–393, October 2001, number 5.

[13] R. Sanahuja, V. Barcons, L. Balado, and J. Figueras, "Testing Biquad Filters under Parametric Shifts using X-Y zoning," *Journal of Electronic Testing-Theory and Application*, vol. 20, pp. 257–265, 2005.

[14] L. Balado, E. Lupon, J. Figueras, M. Roca, E. Isern, and R. Picos, "Verifying Functional Specifications by Regression Techniques on Lissajous Test Signatures," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 56, pp. 754–762, April 2009, issue 4.

[15] R. Sanahuja, A. Gómez, L. Balado, and J. Figueras, "Digital Signature Generator for Mixed-Signal Testing," *European Test Symposium*, 2009.

[16] Yongwang Ding and Ramesh Harjani, *High-Linearity CMOS RF Front-End Circuits*. Springer US, 2005, ISBN 978-0-387-23801-2.

[17] Di Long, Xianlong Hong, and Sheqin Dong, "Optimal Two-Dimension Common Centroid Layout generation for MOS Transistors Unit-Circuit," *IEEE International Symposium on Circuits and Systems*, vol. 3, pp. 2999–3002, 2005.