Abstract

El principal objectiu d'aquest projecte final de carrera és implementar dues fonts d'alimentació de potència a $16^2/_3$ Hz per a la tracció elèctrica. La font d'alimentació treballarà com a *subestació*, proporcionant la potència necessària i el voltatge sinusoïdal a $16^2/_3$ Hz a una *catenària* d'on es connectarà una o més d'una *locomotora*. El sistema de tracció es composa de dues subestacions a cada extrem de la línia, la catenària i la locomotora. Les subestacions són modelades com VSI més un filtre LC, la catenària com una impedància variable i la locomotora com un VSI amb un filtre L en aquest cas. S'ha realitzat una revisió de la literatura per establir l'estat de l'art de les tècniques de control de la tensió i, seguidament, un estudi de la millor tècnica de control per inversors monofàsics. S'ha dissenyat, simulat, implementat en un DSPIC i validat experimentalment un control basat en controladors Proporcionals Resonants per regular la tensió de sortida de la subestació en diferents escenaris. En primer lloc, el control de tensió serà avaluat provocant canvis bruscos de corrent amb una càrrega resistiva, posteriorment amb una càrrega resistiva-inductiva i, finalment, amb un convertidor de corrent (locomotora).

Els objectius del projecte s'han superat satisfactòriament i el model de subestació d'alimentació per a la tracció elèctrica està en servei. El control de tensió implementat és capaç de seguir la referència amb error nul en estat estacionari i un temps de resposta de 10 ms.

Aquest projecte final de carrera s'ha dut a terme a "École Polytechnique Fédérale de Lausanne - Laboratoire d'Électronique Industriel (EPFL-LEI)" situada a Lausanne, Suissa. És una col·laboració entre el CITCEA-UPC i EPFL-LEI. Forma part d'una tesi doctoral que engloba aquest projecte final de carrera i un projecte de semestre. El principal objectiu de la tesi doctoral és validar experimentalment en una locomotora moderna FLIRT un mètode de control per compensar la caiguda de tensió que existeix en les catenàries injectant potència reactiva capacitiva. Per aconseguir tal fi, abans el control s'ha de probar en un model del sistema ferroviari a escala reduïda, amb la qual cosa es requeria un model de subestació (aquest projecte final de carrera) i un model de locomotora (projecte de semestre).

Table of Contents

List of Tables

List of Figures

List of Abbreviations

FAE Fictive Axis Emulation

IGCT Integrated Gate-Commutated Thyristor

PR Proportional Resonant

SOGI Second Order Generalized Integrator

VSI Voltage Source Inverter

1 Introduction

1.1 Statement of the Problem and Thesis Objectives

In 1888 the first electric working streetcar system was built. Since that, transports on rail have been increasing and, consequently, railway infrastructure have been growing up and extending all over the world. An important part of this infrastructure is the railway power supply system [2]. Many studies demonstrate the impacts of voltage drops in the catenary on the traffic flow. The weaker the power system and the heavier the traffic, the greater the voltage drops. And the greater the voltage drops, the more limited the maximal attainable tractive force on the locomotives.

In many Europe countries such as Switzerland, Germany, Austria, Sweden and Norway, single-phase low frequency AC railway power supply systems are connected to the ordinary 50 Hz power system through frequency converters to reduce the frequency level. In Austria they operate at 25 Hz, in Sweden and Norway at 16,7 Hz and the traction network analyzed in this thesis belongs to the swiss country where the frequency of the railway power supply system is $16^{2}/_{3}$ Hz.

Railway power supply systems are changing all the time. When a train moves, the impedance between it and the feeding points changes. The apparent power demands also change when the trains move. Both the active and reactive power demands of the locomotives may vary with the slopes of the railway, the train weights, the desired train velocity, catenary voltage levels, etc. The voltage drop along the catenary is caused by any locomotive absorbing real power from the catenary, and involves to a lower voltage in the front-end of the train. This effect is maximum at the end of a line which is supplied by one substation or in the middle of a line supplied by two substations. The main objective of the whole project (see abstract) is to compensate that voltage drop injecting capacitive reactive power. This is possible in modern locomotives thanks to the active front-end converters with IGBTs that make them able to independently absorb real and reactive power at any desired level if their power limits permit.

To achieve that objective, is needed a very clean sinusoidal voltage at the end of the substation, so the main objective of this thesis is to implement two scaled-down power substations to provide the desired voltage. So, the studied traction network is composed by two substations and a locomotive. The substations will be controlled with a 16 bit fixed-point DSP from Microchip and the locomotive with a 32 bit floating-point DSP from SHARC.

1.2 Thesis Outline

The main points of this thesis are:

- Design of the substation: Design of the scaled-down model, analysis of the Single-Phase VSI, design of the LC filter and the voltage control strategy. A description of the hardware and software of the prototype is done. Through simulations, an extensive study of the best approach for controlling the voltage is also done, both in the synchronous reference frame and the stationary reference frame. The Proportional Resonant controller is presented and fully analysed. The two substation prototypes are mounted and verified. Chapter 2.
- Description of the locomotive model is done in chapter 3. Calculation of the L filter, description of the current control method based on FAE and multivariable PI, the performance is tested through simulations and experimentally verified.
- The performance of the voltage control strategy is experimentally evaluated in Chapter 4. The experimental setup is built up with the contributions of all the participants in this project.
- Economic and environmental analysis is done in chapter 5.
- Finally the conclusions of this thesis are exposed.

2 Scaled-Down Power Substation

2.1 Traction Network Description

2.1.1 Railway Power Supply System

Swiss Federal Railways use 15 kV, 16⅔ Hz power supply provided by its own generation and distribution grid [3]. The main part of this grid is operated at 132 kV. The substations are connected to the three-phase 50 Hz high voltage grid with rotary or static converters to reduce the voltage level and frequency to the required values; power is also generated in hydroelectric plants. Figure 2.1 shows the power supply systems [4].

Power electronics application started in the 1970s with the slip control system in the rotating frequency converters. Rotating machines have long life expectancy, and converters are still being upgraded, however, the most advanced IGCT technology is now being used. Fully static converters were implemented for first time in 1994, in spite of the integration in the power supply system involved to several challenges:

- Static converters have practically null overload capacity, in consequence, they have to be designed for correctly switching also in high power demand peaks which do not occur that often.
- The critical parameter, in addition to the admissible output voltage distortion, is the distortion in the current of the trains fed by the converters. High distortion can affect other circuits, for exemple, low power signaling circuits.
- The difference in the fault current level produced by rotating machines and static converters, lower in the second ones, may lead in future to have to develop enhanced protection systems.

Nowadays several countries continue to exploit their railway network at 16⅔ Hz mostly for historical reasons and for the difficulty to change all their railway infrastructure, but there are no technical advantatges for not using the 50 Hz systems. Nevertheless, it has a major

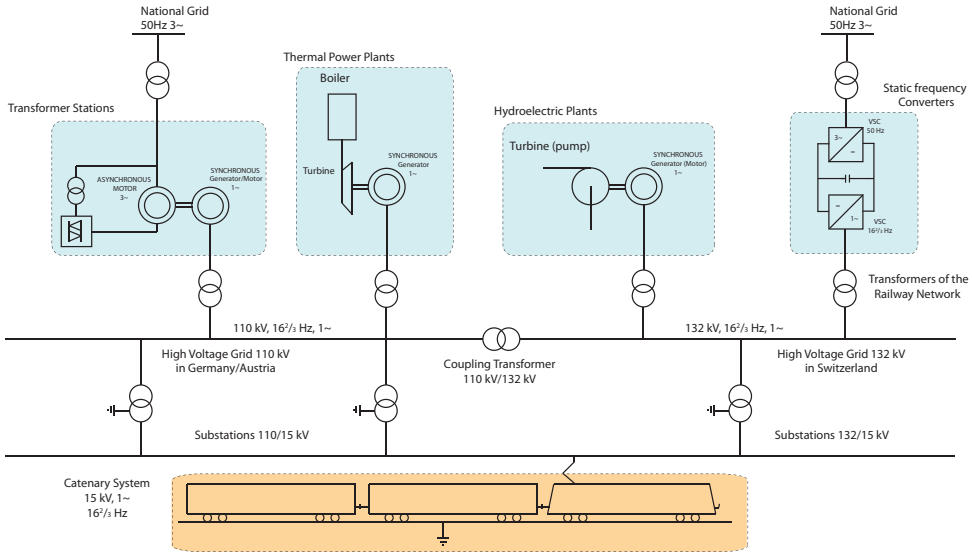

Figure 2.1: Power supply systems

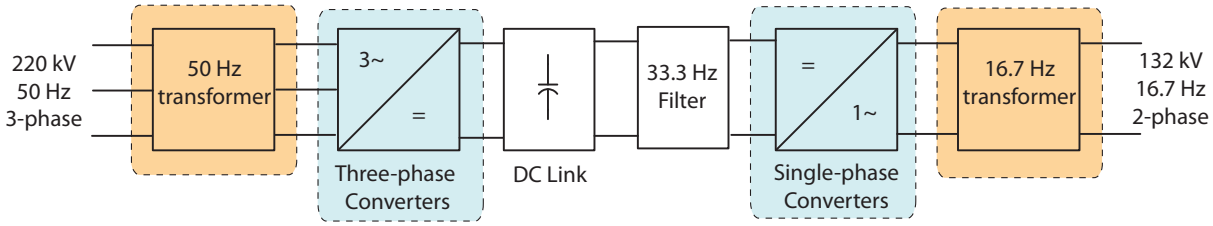

Figure 2.2: Schematic diagram of typical topology of frequency converters in railway power supply systems

disadvantage, the low frequency locomotives compared to the 50 Hz locomotives must have a heavier transformer. Low frequency transformers need to have heavier magnetic cores and larger windings for the same level of power conversion. That means, using a 50 Hz transformer in a $16^2/_3$ Hz system the transformer has to be de-rated to one third of their original power handling capability, and consequently the available tractive power.

A typical topology for frequency converters in railway power supply systems [5], is shown in the simplified schematic of Figure 2.2. As it can be observed, first the voltage is rectified with a three-phase voltage source rectifier (VSR) and fed into a DC link, then inverted with a single-phase voltage source inverter (VSI) to obtain the desired frequency level.

2.1.2 Railway System Studied

The real system studied is the section of the Swiss Federal railway network from Neuchâtel to Biel Route. The train consist on a FLIRT locomotive, equipped with active front-end converter that allows to independently absorb active and reactive power at different levels. An schematic diagram is shown in Figure 2.3, where the model of the substation and the train are detailed. The parameters of the real system are presented in Table 2.1.

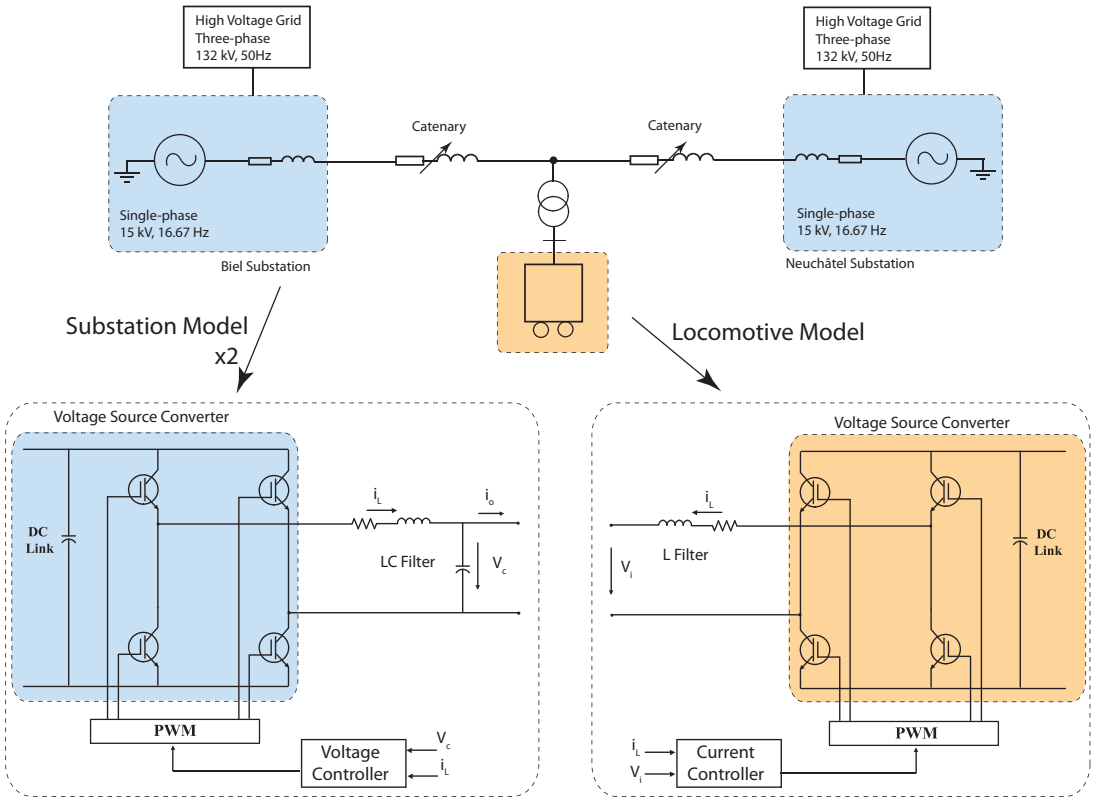

Figure 2.3: Schematic diagram of a section of the swiss railway network with two substations and one locomotive

Table 2.1: Parameters of the system of Figure 2.3

FLIRT locomotive			
Quantity	**Value**	**P.U.**	**Comment**
S_{base}	0,5 MVA	1 pu	Base Value of Locomotive Power
V_{pc}	385 V(rms)	1 pu	Locomotive Nominal Voltage
L_{trafo}	0,4 mH	0,14 pu	Leakage Inductance of Transformer
R_{trafo}	0,019 Ω	0,06 pu	Resistance of Transformer
$n_1 : n_2$	38961:1		Transformer Ratio
f_{sw}	2 kHz		PWM Carrier Frequency
Substations			
Quantity	**Value**	**P.U.**	**Comment**
Voltage Level	15000 V (rms)	1 pu	Substation Nominal Voltage
f	$16^2/_3$ Hz		System Nominal Frequency
$R_{catenary}$	0,08 Ω	0,00016 pu	Catenary Resistance per Km
$L_{catenary}$	1,24 mH	0,00026 pu	Catenary Inductance per Km
Distance	30 km		Distance Neuchâtel-Biel

2.2 Substation Structure

The substation is modeled as a VSI with an LC filter. The structure is presented in Figure 2.4.

The power is provided by a 200 V DC source, and the voltage is converted and controlled to obtain a clean 90 V amplitude sine-wave waveform. The modulation of the VSI and switching of the IGBTs consist in the 3-Level double frequency PWM modulation described in Section 2.3.2.

The control signal, u_{cs}, is provided by the voltage controller depending on the operation conditions: desired output voltage and provided power. The desired output voltage is the voltage reference of the controller and it is fixed at 90 V amplitude value, however, the power provided by the substation may vary depending on the distance between the train and the feeding point.

The filter consists in an inductance and a capacitor designed to eliminate the high frequency harmonics to obtain a clean voltage sine-wave in the ouput of the substation.

The control strategy is described in Section 2.6.2.

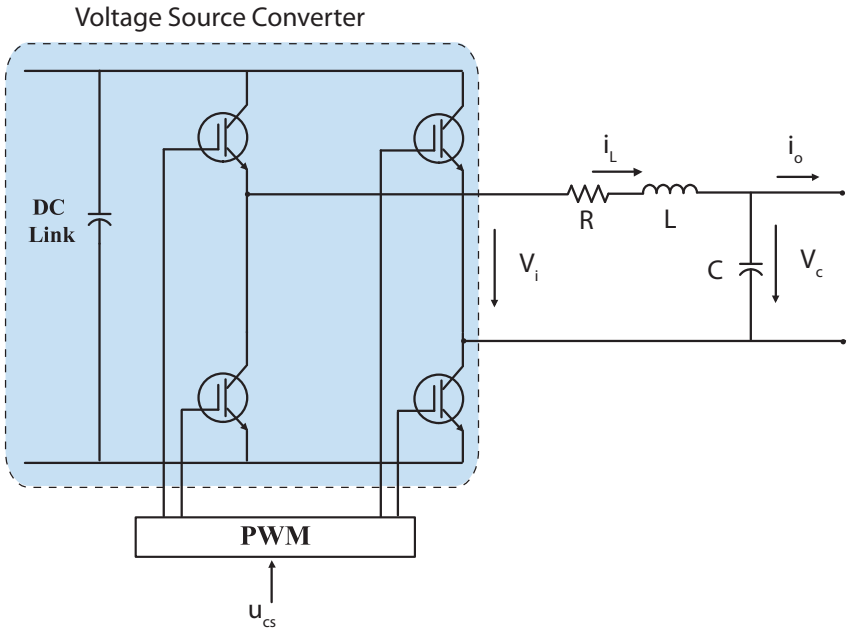

Figure 2.4: Substation power stage structure modeled as VSI with LC filter

2.2.1 Parameters of the Model

The parameters of the model are shown in Table 2.2.

Table 2.2: Parameters of the model

Quantity	Value	P.U.	Comment
Voltage Level	90 V (amplitude)	1 pu	Substation Nominal Voltage
Current Level	10 A (amplitude)	1 pu	Rated Current Level
V_{dc}	200 V	2,22 pu	DC Link Voltage
f	$16^2/_3$ Hz		System Nominal Frequency
f_{sw}	10 kHz		PWM Switching Frequency
f_s	10 kHz		Sampling Frequency
R	0,8 Ω	0,088 pu	Resistance of VSI Line Filter
L	8 mH	0,093 pu	Inductance of VSI Line Filter
C	50 μF	0,047 pu	Capacitor of VSI Line Filter

2.3 The Single-Phase Inverter

2.3.1 Basic Structure - The Full-bridge Inverter

In advantage from the half-bridge inverters the full-bridge single-phase inverter, usually called H bridge, lies in using the same dc input voltage the maximum output voltage of the full-bridge inverter is twice that of the half-bridge inverter. This implies that for the same power, the output current and the switch currents are one-half of those for a half-bridge inverter [6]. The H bridge structure is shown in Figure 2.5.

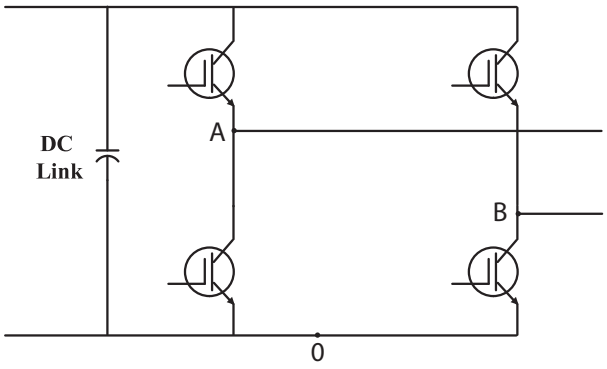

Figure 2.5: Single-phase full bridge inverter

This inverter consists of two one-leg inverters where both the amplitude and the frequency of the output voltage are controllable. The fundamental frequency of the output voltage is fixed by the frequency of the control signal. In order to produce a sinusoidal voltage, a sinusoidal control signal is compared with a triangular waveform, and the frequency of the second one establishes the inverter's switching frequency.

For this application, IGBTs are chosen as switches, since they have high speed and high input impedance characteristics as MOSFETs and high conductivity characteristics as BJTs. The IGBT is the natural choice for low and medium power applications.

2.3.2 Modulation of the Single-Phase Inverter

As said in Section 2.3.1, the control signal for Pulse-Width-Modulated inverters is sinusoidal. This signal is called the modulation signal and is generated by the controller and fed into the PWM module. For this application, 3-level double frequency modulation scheme is chosen, that

means that the switching output voltage has three possible values: $+V_{dc}$, 0 and $-V_{dc}$, and the frequency is double the switching frequency of the IGBTs. With this modulation of the inverter, for the same inductance filter the current ripple is half that of the two level modulation scheme, and similar effect happens with voltage ripple and the value of the capacitor filter. For the substation the switching frequency is 10 kHz, the voltage level is fixed at 90 V (amplitude), and a 200 V DC source is used, which implies that with no load connected to the inverter the control signal amplitude is 0,45. Figure 2.6 shows the 3-level double frequency PWM modulation for this application (for reasons of clarity, the frequency of the triangular waveform is set 150 Hz):

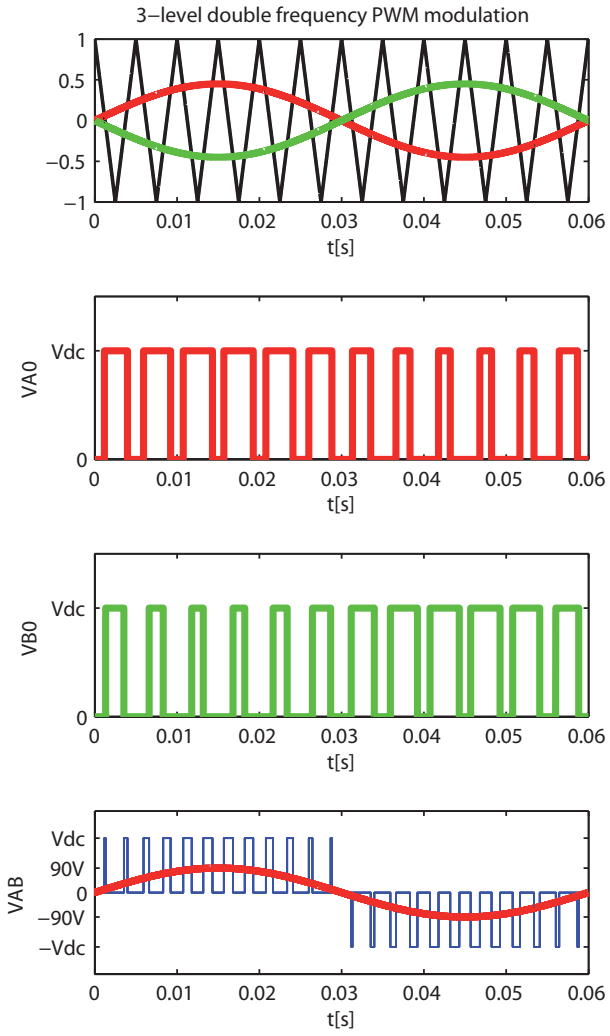

Figure 2.6: 3-level double frequency PWM modulation

As shown in Figure 2.6, the legs A and B of the full-bridge inverter are controlled separately by comparing v_{tri} with $v_{control}$ and $-v_{control}$ respectively. The logic signals to control the

switches in leg A are:

$$\begin{aligned} v_{control} > v_{tri}: \quad & A_{high}\ is\ on, \quad V_{A0} = V_{dc} \\ v_{control} < v_{tri}: \quad & A_{low}\ is\ on, \quad V_{A0} = 0 \end{aligned} \tag{2.1}$$

The logic signals to control the switches in leg B are:

$$\begin{aligned} -v_{control} > v_{tri}: \quad & B_{high}\ is\ on, \quad V_{B0} = V_{dc} \\ -v_{control} < v_{tri}: \quad & B_{low}\ is\ on, \quad V_{B0} = 0 \end{aligned} \tag{2.2}$$

The output of the inverter, V_{AB}, is then $V_{A0} - V_{B0}$ and in consequence the frequency of the signal is doubled.

2.3.3 Harmonic Analysis

First of all some terms need to be defined. The frequency modulation ratio m_f is defined as $m_f = f_{sw}/f_1$ [7], and $(V_{AB})h$ means the h harmonic of the signal V_{AB}. The advantage of doubling the switching frequency appears in the harmonic spectrum of the output voltage waveform, where the lowest harmonics are situated around twice the switching frequency, exactly at (2mf-1) and (2mf+1). The spectrum of the inverter output voltage for the substation is extracted from simulations and shown in Figure 2.7.

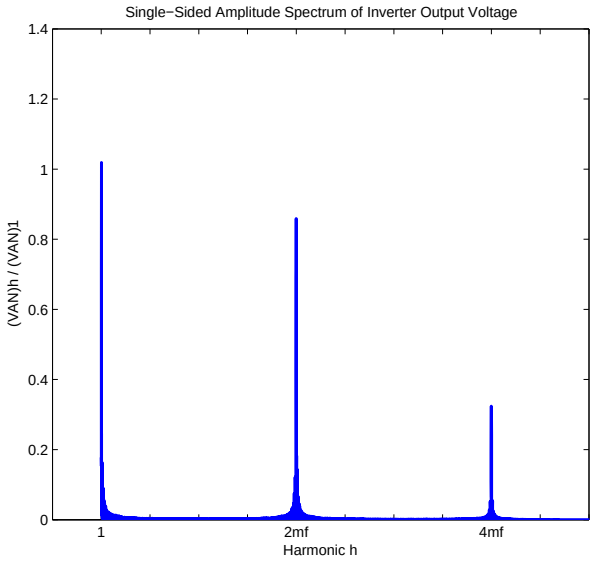

Figure 2.7: Single-sided amplitude spectrum of normalized inverter's harmonic voltages

As it can be observed, the next dominant harmonic is situated around 20kHz ($2m_f$), with an amplitud of approximately 85% of the fundamental frequency component, the other harmonics take place at multiples of $2m_f$. It is important to take into account that working with low control signals the amplitude of the harmonics is higher. That should not be a problem for the system performance because the cut-off frequency of the LC filter is design to be much less the harmonic $2m_f$, thus, all those high frequency harmonics are correctly filtered.

2.4 LC Filter Design

The objective of this part is to design an LC filter for the output of the converter in order to eliminate the high frequency voltage and current harmonics of the line to provide a clean sine-wave to the catenary of the model.

2.4.1 Inductor Calculation

In a full bridge inverter with 3 level double frequency PWM modulation the inductance of the output filter can be found with the following equation:

$$L = \frac{V_{dc}(1-\alpha)\alpha}{2\Delta I f_{sw}} \tag{2.3}$$

Where α is the maximum value of the control signal within a period and is calculated as the ratio between the amplitude of the output voltage and the DC voltage.

$$\alpha = \frac{\widehat{V}_{out}}{V_{dc}} \tag{2.4}$$

The admitted current ripple is fixed at 5% of nominal value and is maximum when the voltage is maximum. From equation 2.3 and 2.4 the inductance value results 5 mH. The inductance used in the setup is 8 mH.

2.4.2 Capacitor Calculation

Based on [8] the capacitance is calculated:

$$K = \left[\frac{\alpha^2 - \frac{15}{4}\alpha^4 + \frac{64}{5\pi}\alpha^5 - \frac{5}{4}\alpha^6}{1440}\right]^{1/2}$$
$$C = K\frac{V_{dc}}{Lf_{sw}^2\Delta V_{out}} \tag{2.5}$$

The admitted voltage ripple is fixed at 1% of voltage nominal value, so, the needed capacitor in terms of voltage ripple is 2,5 μF.

But the chosen capacitor is not that one calculated with Equation 2.5, it has to be much higher in order to help the controller to reduce the voltage peak caused by, for example, a load suddenly connected or disconnected from the substation. A 50 μF capacitor is finally used; a discussion of the advantatges and drawbacks of increasing the capacitor is done in Section 2.6.2.

With those paramenters of the filter, the cut-off frequency is located at 252 Hz, that means that the high frequency harmonic content of the voltage in the output of the inverter will be fully filtered.

2.5 Description of the Prototype

In this section a brief description of the hardware and software of the VSI prototype is done. The board contains mainly the four IGBT, isolated drivers, voltage and current sensors, communication ports with DSPIC, power supply inputs and some passive elements. The power stage schematic and the communications with the control stage are represented in Figure 2.8, where the main components of the board are shown.

Description of the hardware

- IGBT: IRGB4062DPbF from International Rectifier.
- Drivers: HCPL-314J 0.4 Amp Output Current IGBT Gate Drive Optocoupler from Avago Technologies.
- Voltage mesurement: Voltage Transducer LV 25-P.
- Current mesurement: Current Transducer LA 25-NP.
- Traco: TRACO TEN 3-1223 ±15V output.

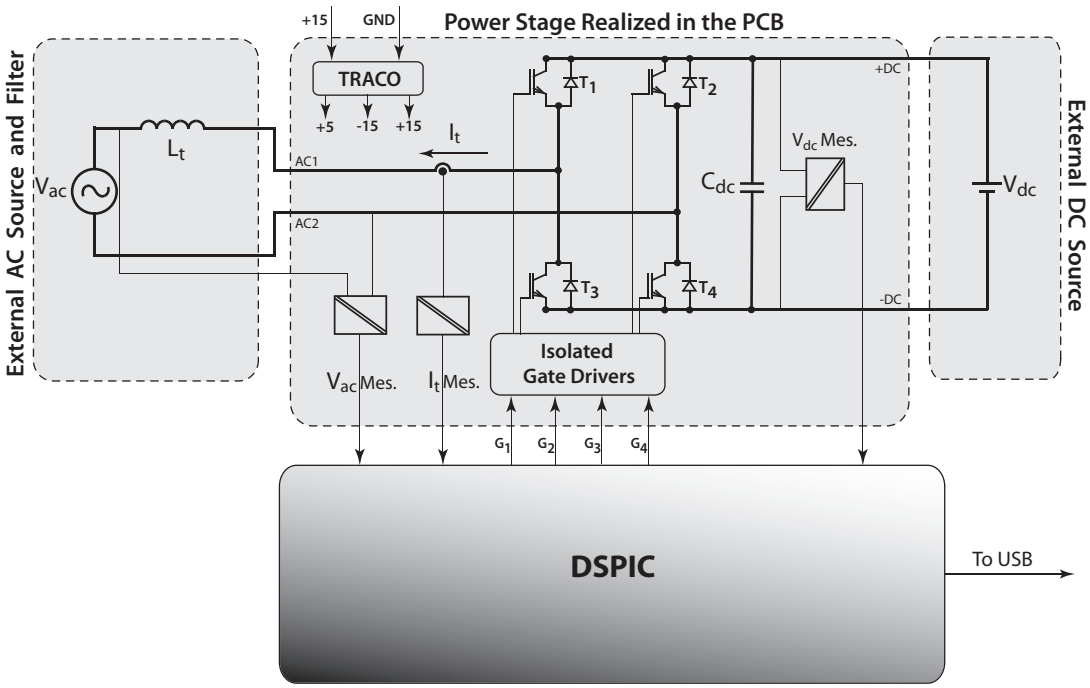

Figure 2.8: Schematic of the single-phase converter and control

- Voltage regulator: L7805CV Voltage regulator 5V.
- Connector 50 pins: Receives signals from DSPIC; gating signals for each IGBT.
- Connector 20 pins: Sends voltage/current mesurements to DSPiC.

For a detailed description of all the components see Appendix A.

Description of the software

The DSPIC board where the controller is implemented is based on the 16 bit DSPIC30F6010A of Microchip. It has been provided by the laboratory. The main features are:

Table 2.3: DSPIC features

CPU speed	30MIPs	Output compare	8
Flash memory	144 kbytes	PWM channels	8
RAM memory	8192 bytes	UART	2
EEPROM memory	4096 bytes	CAN controller	2
I/O ports	68	SPI	2
A/D converter	16(10bit)	I2C	2
Input Capture	8		

For more information about the communication with the VSI board see Appendix A.

2.6 Voltage Control of the Scaled-Down Power Substation

2.6.1 Literature Review. Voltage Control Strategies Available

The most important part of this master thesis is described in this section and the next one. The correct choice of the best voltage control strategy is essential. The voltage remains fixed, no voltage steps are applied, so the main task of the voltage controller is to keep the voltage of the substation as close as possible to the reference value whenever the load changes. As explained in Section 1.1, the impedance between the front-end of the locomotive and one substation changes according to the position of the first one. In other words, in this application the load changes all the time, being higher the power absorved by the train from the closest substation and lower in the farthest substation. Many approaches have been extracted from literature, all of them have been studied and simulated, to get knowledge about the voltage control and to consider the advantatges and drawbacks of each one to design an improved voltage control strategy for this application.

1. Single-loop feedforward+feedback using P+Resonant controller [1].
2. Double-loop voltage control using P+Resonant controller [1].
3. Single-loop dq voltage control using second order controller [9].

All those voltage control strategies have been tested by simulations considering different scenarios, in all of them the output voltage transient and frequency transient were compared. Those tests were:

- Substation connected to a resistive load: The performance of the controller has been evaluated with load steps, going from no-load to full-load.
- Substation connected to a resistive inductive load. Same performance evaluation.
- Substation connected to a current converter (locomotive): The performance of the controller has been evaluated making current steps with the current converter, as if a train started to consume power from the substation.

All three approches have been evaluated by those three tests. Firstly each control strategy have been studied and theorically analized, secondly a proper controller has been designed for each one, and finally the simulation results have been obtained. The main interest was in the voltage error ($V_{REF} - V_{out}$) but the frequency was also extracted by a PLL (Phase-locked Loop) and observed.

The best two voltage control strategies in terms of fastest response, best reference tracking and minimal frequency distortion were, in that order, the approaches based on PR controllers:

1. Double-loop voltage control using P+Resonant controller (Figure 2.9 (b))
2. Single-loop feedforward + feedback using P+Resonant controller (Figure 2.9 (a))

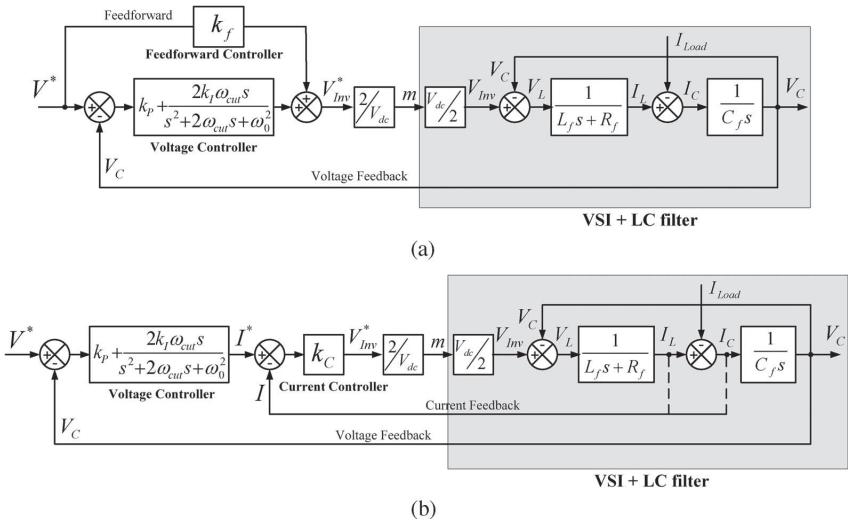

Figure 2.9: Control schemes for the VSI system in stationary frame using: (a) single-loop feedforward + feedback and (b) double-loop control. *Font [1]*

The simulation results applying current steps with a current converter for the control scheme of Figure 2.9 (b) are shown in Figure 2.10. In that picture, a high voltage peak appear when the load is suddenly connected. A current step causes a high current derivate in the inductance of the filter, which involves to a high peak of voltage that affect the output voltage and cannot be reduced to acceptable values with only the controller. A solution for reducing that voltage peak is to use a larger capacitor, but a larger capacitor consumes more current and the amplitude at the fundamental frequency will not be negligible. That means that even if there is not load connected to the substation, a permanent current is absorbed by the VSI. A compromise solution is found fixing the value of the capacitor at 50 μF, in consequence the current absorbed by the

capacitor is a 5% of the rated current of the substation.

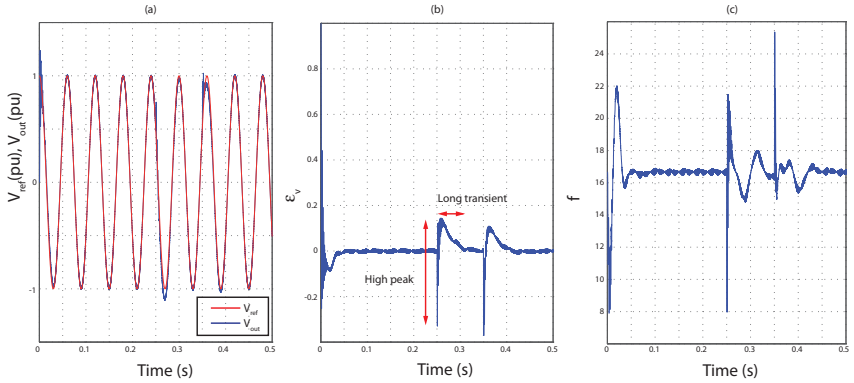

Figure 2.10: Simulation results applying current steps from no-load to full-load at time instants 0,25 ms and 0,35 ms: (a) Reference and output voltage waveforms (b) $\epsilon_v = V_{ref} - V_{out}$, (c) frequency transients of the output voltage

As it can be observed in the control scheme of Figure 2.9 (b), the best control strategy for this application of those five analysed is based on an inner current loop with a proportional controller and an outer loop consisting on a P+Resonant controller. Using a proportional controller the steady-state error of the current loop is not null which can cause problems in the performance of the controller and, furthermore, the design of the current protection for the circuit would have to consider that error. So the first improvement to be applied is to eliminate the steady-state error implementing a P+Resonant controller also for the current loop. The second point to focus on is the response time, a load current feedforward in the output of the voltage controller is added to help the controller to track the reference with a response time around 5ms, in other words, the controller anticipates the disturbance. How this current feedforward is done is explained in Section 2.6.2.

At this point, with some knowledge adquired from the literature available at the moment, a complete analysis of the improved voltage control strategies developped in this master thesis are realized in the next section.

2.6.2 Analysis of Double-loop Voltage Control Strategy

For this application, the load is constantly changing when the trains are moving, but the voltage level is kept constant, so the controller is designed to get the best dynamics when load steps are applied minimizing the effects of the system disturbance, the current absorbed by the trains. Hence, the objective of the control method is to implement a voltage controller with disturbance rejection capability. The idea for rejecting the disturbance is to implement a load current feedforward in the voltage loop, with or without a load current sensor. It is possible to improve the dynamics of the voltage controller with a feedforward of the inductance current, but filtered, as an approximation of the real load current.

The control strategy is evaluated using PI controllers in the synchronous reference frame and Proportional Resonant controllers in stationary frame to determine which has the best response, and a comparison between both controllers with or without the load current feedforward is done.

Test system:

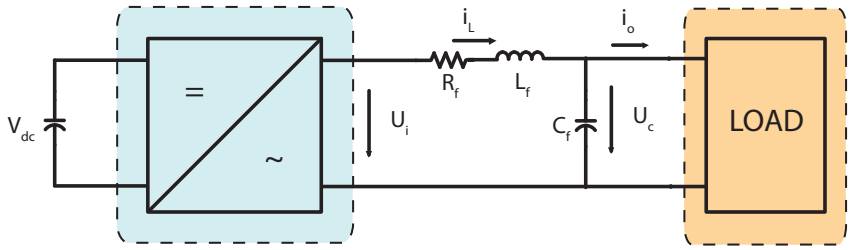

Figure 2.11: Single-phase test system

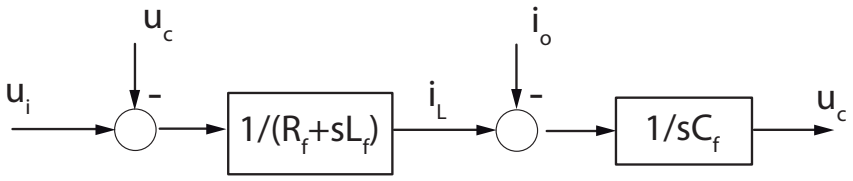

Figure 2.12: Structural diagram of the test system

To control the output voltage with zero steady-state error Proportional Resonant controllers and PI controllers are implemented in stationary reference frame and synchronous reference frame, respectively. The next three control strategies have been developped and simulated in Matlab/SIMULINK environment, and the Stationary Voltage Control Strategy has been

experimentally validated in a test bench.

Synchronous Voltage Control Strategy

See Appendix B.

Hybrid Synchronous/Stationary Voltage Control Strategy

See Appendix C.

Stationary Voltage Control Strategy

Analysing the system in time domain, applying KCL (Kirchhoff's current law) in the node of the test system of Figure 2.11 the next equation is found:

$$i_L(t) = i_c(t) + i_o(t) \tag{2.6}$$

$$i_L(t) = C_f \frac{du_c(t)}{dt} + i_o(t) \tag{2.7}$$

From Eq. 2.7, the inverter current has to be controlled as follows:

$$i_{L,ref}(t) = i_{c,ref}(t) + i_o(t) \tag{2.8}$$

where $i_{c,ref}$ represents the capacitor current reference and a feedforward of the load current is added, i_o. Figure 2.13 shows the voltage controller structure.

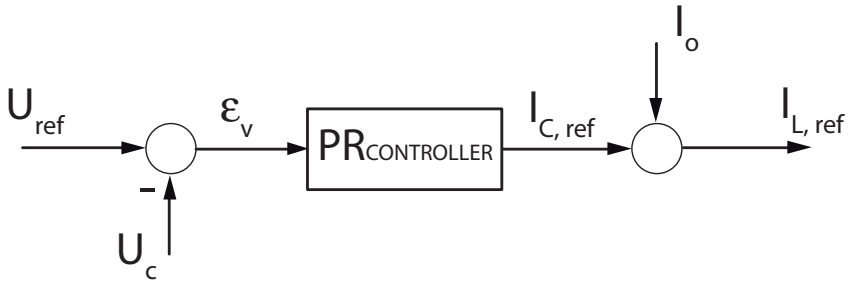

Figure 2.13: Structural diagram of the voltage controller

The reason on adding the load current feedforward is to compensate the effect of the disturbance on the output voltage. With this control strategy, the output of the controller is the reference for the capacitor current, not the inductor current.

The output voltage is affected by the inverter's voltage and the load current, the relation between them is shown in Eq. 2.9.

$$U_c(s) = \frac{1}{L_f C_f s^2 + R_f C_f s + 1} U_o(s) - \frac{R_f + L_f s}{L_f C_f s^2 + R_f C_f s + 1} I_o(s) \tag{2.9}$$

The magnitude of the impact of the load current to the output voltage, depends on the size of the inductor (represented by the inductance and the internal resistance). Two options are considered to reduce the effect of the load current, by hardware or by software. By hardware, the value of the inductor can be reduced, but that causes the current ripple to be higher. So, the chosen option for this application is implemented by software, including a feedforward of the disturbance in the voltage loop. The second can be done in two different manners:

1. Sensing the load current with a current sensor and feedfordward it
2. Estimating the load current
   (a) Calculating the load current: Normally the inductor current and the output voltage are known, so the load current can be easily calculated.
   (b) Filtering the inductor current: A low-pass filter can be used, and the result is added as a feedforward in the output of the voltage controller.

Measuring the load current the most accurate disturbance compensation is achieved, nevertheless an additional current sensor is needed. If the considered option is to calculate the load current, derivating the voltage usually causes stability problems, and finally filtering the inductor current the delay introduced by the filter limit the bandwidth of the voltage loop and, in consequence, the performance is slower than the first one. Moreover, if the fundamental frequency component of the capacitor current is high enough, which depends on the value of C_f, the approximation filtered-inductor-current to load-current ceases to be valid. Figure 2.14 shows the filtered line current and the load current when a load step is applied at 0,2 ms. Before the load step, the approximation is not correct, because of the fundamental component of the capacitor current, but when the load starts to consume current the filtered inductor current is almost the same as load current except for the delay between them. The design of the low-pass filter has to consider that this delay affects the dynamics of the voltage loop. The effect of using a heavier filter results in a better damping of the signal as shown in Figure 2.15, but also

involves in a slower response due to the higher delay introduced.

$$G_f(s) = \frac{K_f}{K_f + s} \tag{2.10}$$

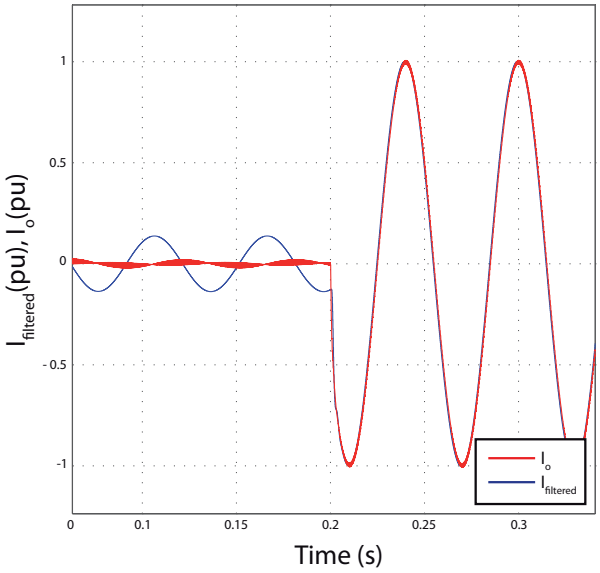

Figure 2.14: Comparison between filtered inductor current ($I_{filtered}$) and real sensed load current (I_o)

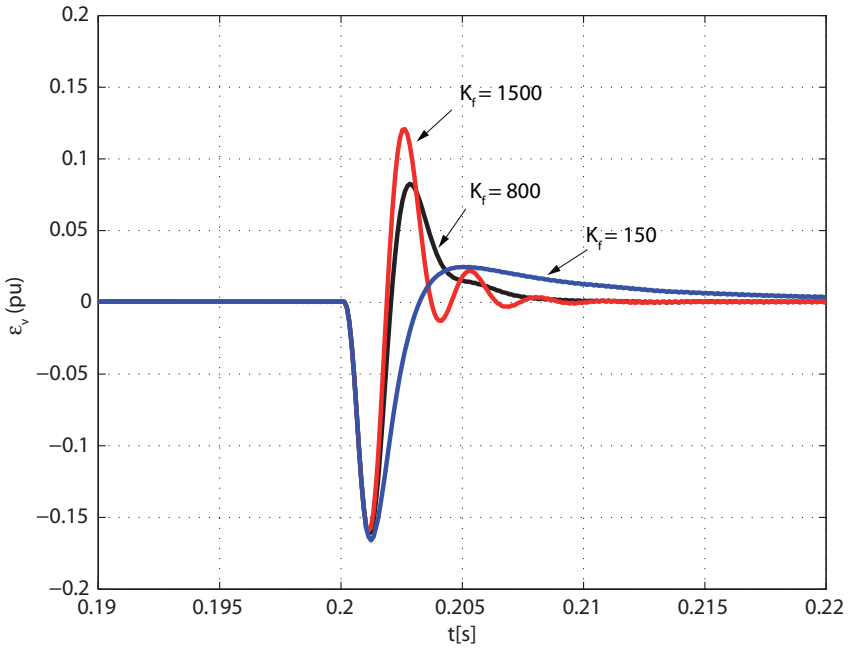

Figure 2.15: Effect of the low-pass filter applied to the inductor current to the voltage error

At this point, the power stage with control blocks is shown in Figure 2.16 and the complete structure of the adopted control strategy is presented in Figure 2.17, using the real load current as the feedforward, and in Figure 2.18 using the inductor's filtered current. The G_{pE} block represents a sum of delays from the treatment of the algorithm in the DSP, the measurements of signals, etc; approximated by a first order element.

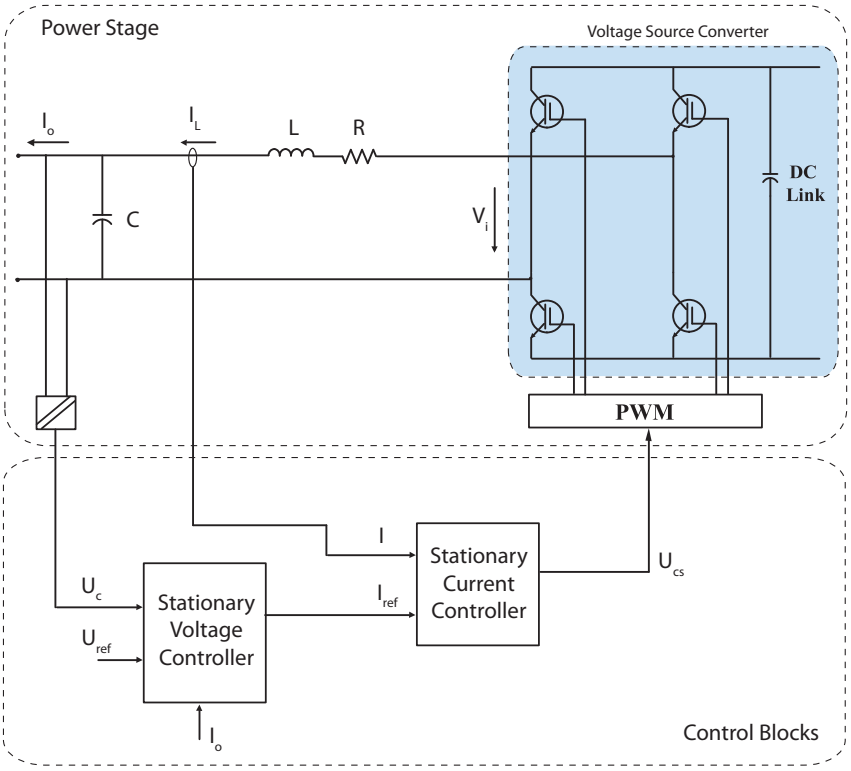

Figure 2.16: Test system with Stationary Voltage Control Strategy

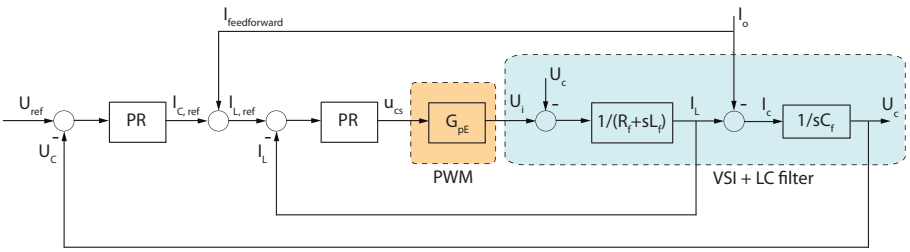

Figure 2.17: Control scheme for the VSI system in stationary frame using Proportional Resonant controllers, measuring the load current

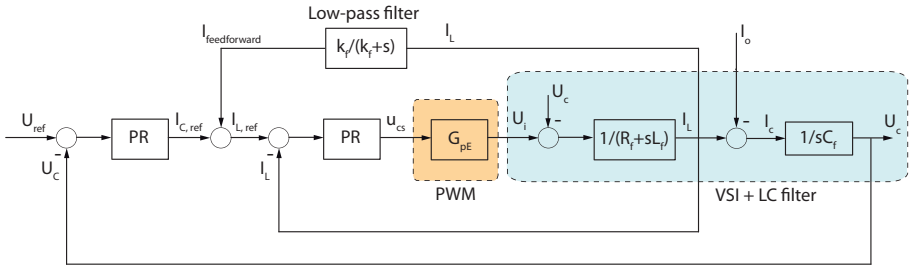

Figure 2.18: Control scheme for the VSI system in stationary frame using Proportional Resonant controllers, filtering the inductor current

Proportional Resonant Controller Implemented

It is known that the ideal Proportional Resonant controller is deduced from the transformation of the PI controller in the synchronous frame to a stationary frame [10], where an infinite gain is theorically obtained at the resonance frequency as the PI controllers with DC signals. But the P+Resonant controllers implemented in both voltage and current loops follow the practical structure shown in Figure 2.19; this structure is physically realisable. Bode diagrams of both controllers are presented in Figure 2.20.

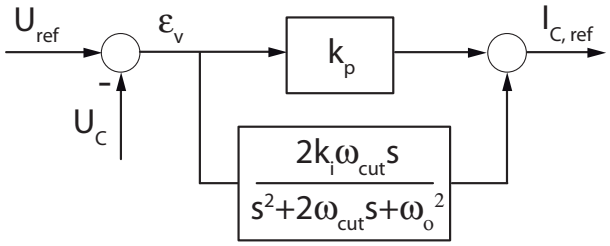

Figure 2.19: Structure of the Proportional Resonant controller

$$G_{PR}(s) = k_p + \frac{2k_i\omega_{cut}s}{s^2 + 2\omega_{cut}s + \omega_o^2} \tag{2.11}$$

where k_p is the proportional gain, k_i is the integral term at the fundamental frequency (ω_o) and the term ω_{cut} affect the controller's performance under frequency variations from the target frequency. ($G_{PR}(j\omega_o) = k_p + k_i$, at ω_o the terms ω_{cut} are cancelled). Increasing k_i the gain is increased and the bandwidth is not affected, increasing ω_{cut} both the gain and bandwidth are increased (except at the resonance frequency).

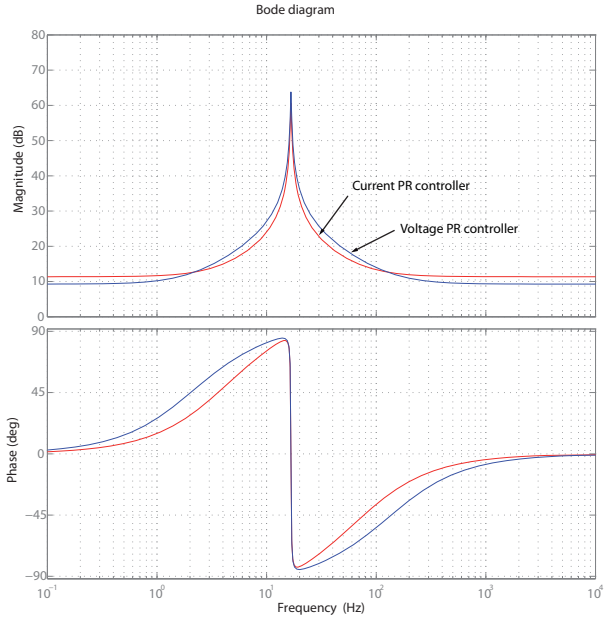

Figure 2.20: Bode diagrams of current and voltage P+Resonant controllers

The design of the controllers have been done imposing the gain and phase margin conditions at the crossover frequency:

$$\begin{aligned} |G_o(j\omega_{co})| &= 1 \\ \angle G_o(j\omega_{co}) &= -180^\circ + phm \end{aligned} \tag{2.12}$$

where G_o is the open-loop transfer function, ω_{co} is the crossover frequency and phm is the desired phase margin.

Design of Current Controller

Plant transfer function:

$$G_c = \frac{I_L}{U_i} = \frac{sC_f}{s^2 L_f C_f + sRC_f + 1} \tag{2.13}$$

Open-loop transfer function:

$$G_{oc} = \frac{I_L}{\epsilon_c} = (k_c + \frac{2k_{ci}\omega_{cut}s}{s^2 + 2\omega_{cut}s + \omega_o})G_c \tag{2.14}$$

Closed-loop transfer function:

$$G_{cc} = \frac{I_L}{I_{L,ref}} = \frac{G_{oc}}{1 + G_{oc}} \tag{2.15}$$

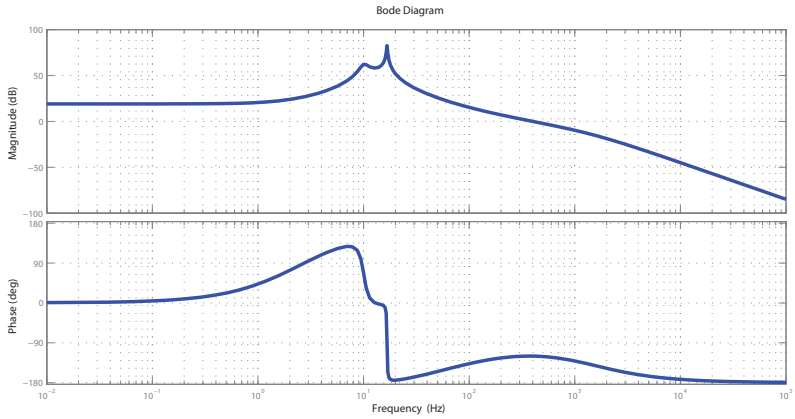

Figure 2.21: Bode diagram of final voltage open-loop system

With a selected ω_{cut} (0,8 rad/s), the porportional gain k_c and the integral gain k_{ci} can be determined imposing Eq. 2.12 to G_{oc}.

Design of Voltage Controller

Plant transfer function:

$$G_v = \frac{U_C}{I_{C,ref}} = G_{cc}\frac{1}{sC_f} \tag{2.16}$$

Open-loop transfer function:

$$G_{ov} = \frac{U_C}{\epsilon_v} = (k_p + \frac{2k_i\omega_{cut}s}{s^2 + 2\omega_{cut}s + \omega_o})G_v \tag{2.17}$$

The same ω_{cut} was chosen for the voltage controller, and k_p and k_i are found imposing Eq. 2.12 to G_{ov}.

Note that G_{oc} is fourth order transfer function, so G_{ov} is a sixth order transfer function.

Those equations give the start values of the controller parameters from which the final PR controllers are found. First the current controller has been tuned with a fixed AC voltage at the output and a PLL, to correctly track a sine-wave current reference with zero steady-state error and a response time around 2-3ms, then through an interactive multiloop controller tuning process the gains of the outer voltage loop controller have been adjusted to obtain the best performance.

Figure 2.21 shows the open-loop voltage bode diagram. The final open-loop crossover

frequency is situated at 400 Hz, almost 21 times the fundamental frequency of the railway system, and the phase margin at 60°.

2.6.3 Simulation Results

The response of the voltage controller is evaluated by applying current steps with the current converter of the train, as if the train started to consume power from the substations at different levels. The control strategy is tested on simulations and experimentally.

A comparison between the strategies using a sensed load current feedforward or a filtered inductor current feedforward is done.

The control strategy has been tested in the traction network described in Section 2.1.2, Figure 2.22 shows the test system developed in Simulink/MATLAB software environment. A detailed view of the substation and locomotive models are shown in the figures below.

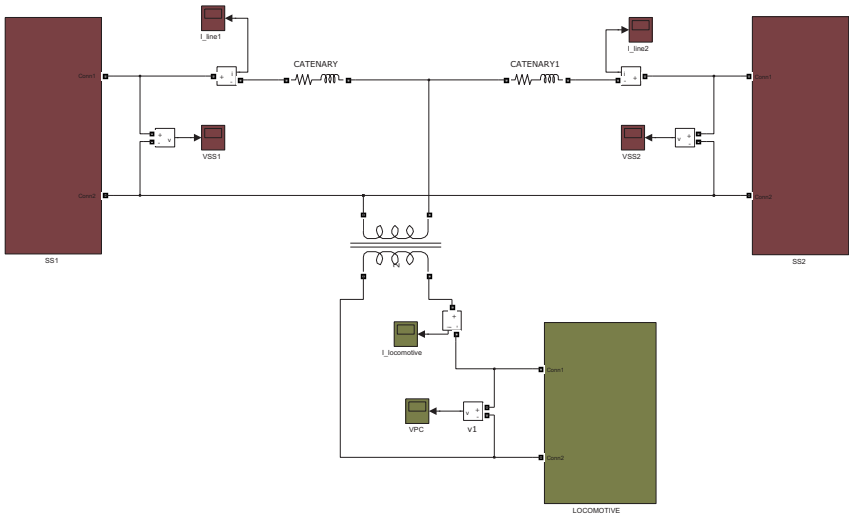

Figure 2.22: MATLAB/Simulink schematic of the traction network studied

First the control and the signal-processing algorithms have been discretized by using the bilinear method and implemented with the S-function tool of Simulink/MATLAB (digital controller blocks in Figure 2.23 and Figure 2.24).

To evaluate the voltage controller performance the worst case for the substation is considered, which means that the distance between the train and substation is minimum so the whole power consumed by the train is provided by the closest substation.

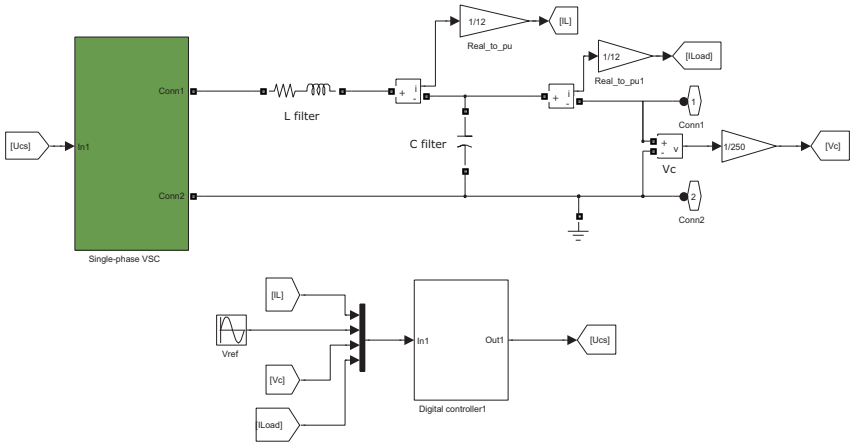

Figure 2.23: MATLAB/Simulink schematic of the substation model

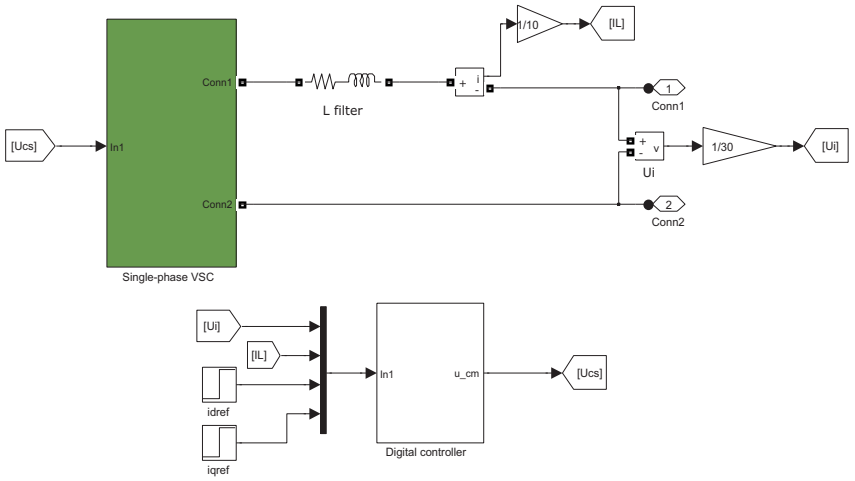

Figure 2.24: MATLAB/Simulink schematic of the locomotive model

A. Current feedforward sensing the load current with a current sensor

The results are shown in Figure 2.25. At time instant $t = 0,2\ s$, reference values for train current are set to $i_d = 0,8\ pu$ and $i_q = 0,6\ pu$, at time instant $t = 0,28\ s$ i_d is set to zero and i_q to 1 pu. The voltage error (ϵ_v) and current error (ϵ_c) are evaluated. The voltage controller is capable to track the voltage reference with a transient response of 5 ms and zero steady-state error. The error peak in terms of voltage is at 6,4% of nominal voltage. The parameters of this test system are those from Table 2.2 for the substations, and those from Table 3.1 for the locomotive, in resume, 90 V is the amplitude of the reference voltage (1 pu), 10 A is the reference for train currents (1 pu).

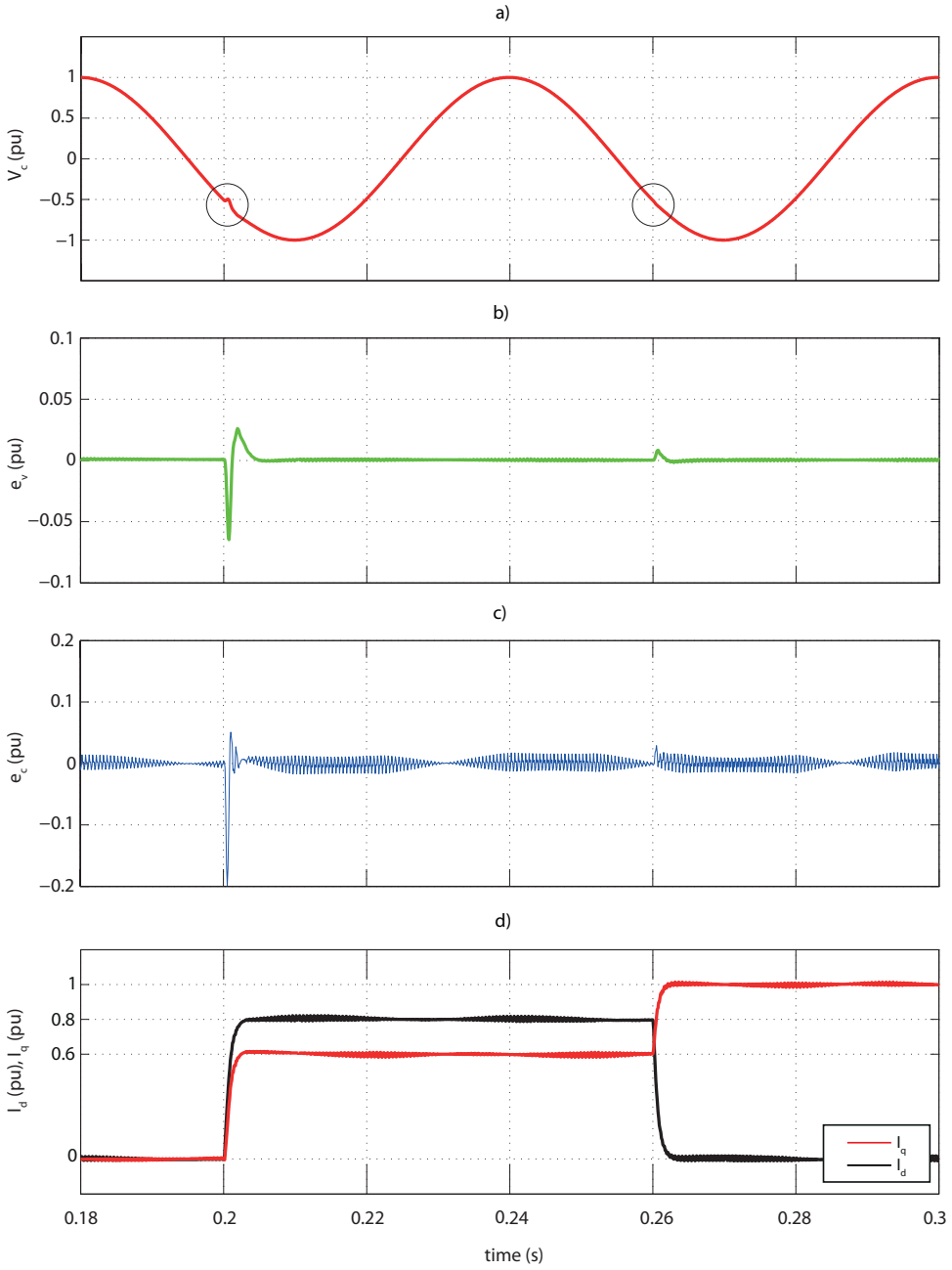

Figure 2.25: Simulation results using the sensed load current feedforward approach: (a) Output voltage (b) Voltage error (c) Current error (d) d and q-axis of train current steps applied to the system

B. Current feedforward filtering the inductor current

The strategy evaluated corresponds to the structure shown in Figure 2.18. Same current steps are applied, and the results are a response time of 7 ms, and an error in voltage of maximum 15,9%. Worse results were expected, as the load current in this case is estimated, but in some

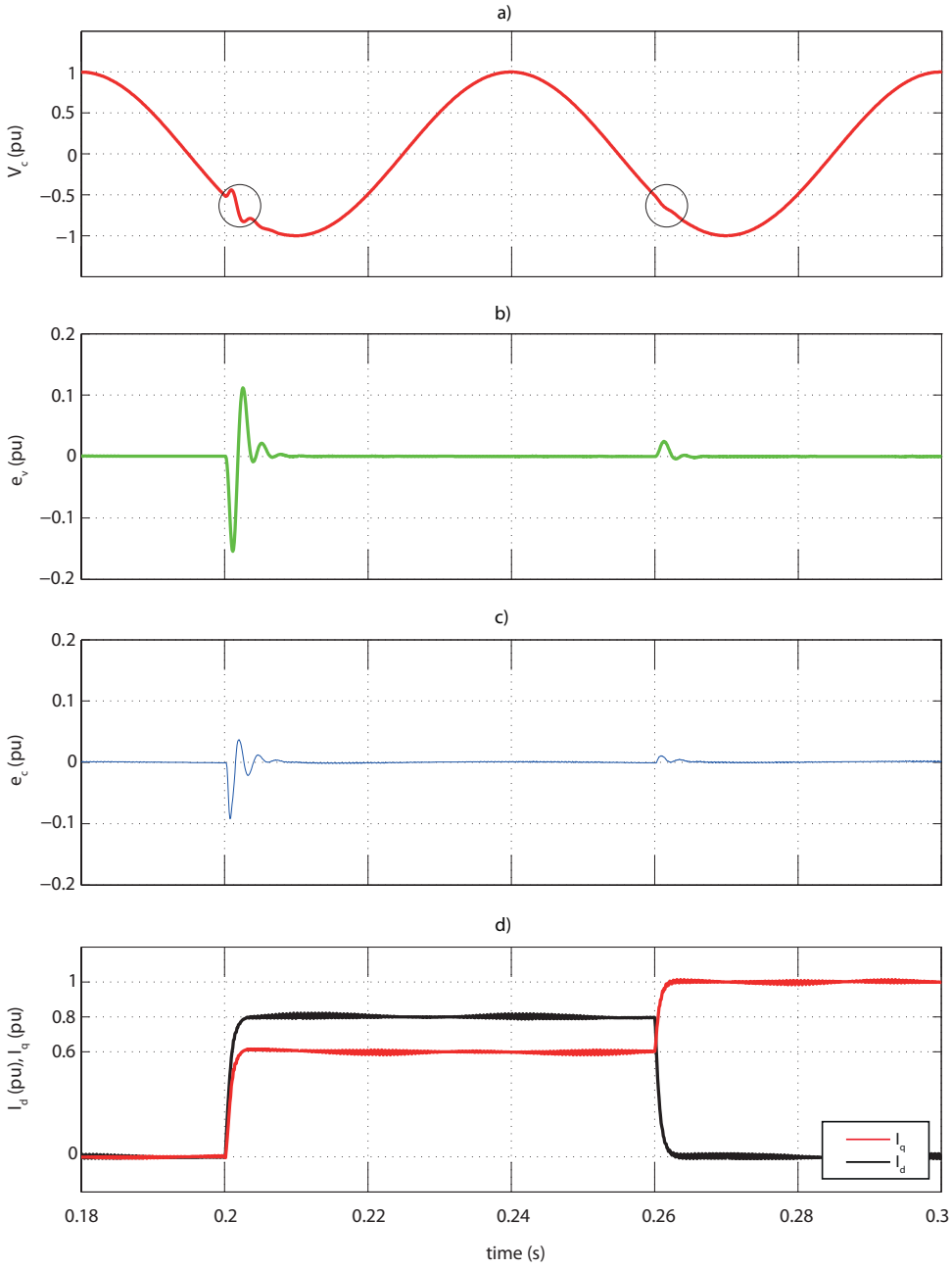

Figure 2.26: Simulation results using the filtered inductor current feedforward approach: (a) Output voltage (b) Voltage error (c) Current error (d) d and q-axis of train current steps applied to the system

applications, usually low-cost, this method provides a good enough voltage response to load steps without any additional current sensor. The delay introduced by the low-pass filter, which is 0,8 ms, affects the dynamics of the controller making it slower as the delay increases.

3 Scaled-Down Power Locomotive

3.1 Locomotive Structure

In this section the model of the locomotive is described, as well as the current control strategy based on FAE and Multivariable PI controller in the synchronous reference frame [11] and [12].

Modern locomotives are equipped with active front-end converters connected to the tractive AC motors betweeen a DC link and three-phase converters. Figure 3.1 shows the active front-end converter and the control strategy implemented to regulate the DC Link voltage and the PC (Coupling Point) voltage.

The locomotive model is based on single-phase VSI, but connected to the catenary through an L filter and a coupling transformer (Figure 3.1). When the tractive motors of the train start consuming power, the current of the train is controlled in order to regulate the power exchanged between the VSI and the substation. Part of the active power is used to maintain the voltage of the DC link capacitor (V_{dc}) at the desired level, this is done by the DC Voltage Controller. Furthermore the PC Voltage Controller regulates V_{pc} to keep it at its nominal value injecting an amount of capacitive reactive power depending on the position of the train.

For the current control, first a SOGI+PLL [13] is needed to create the ortogonal component of the voltage of the "grid" and track its frequency. Secondly a FAE technique is used to create the ortogonal component for the current of the inductor. A single-phase stationary-to-synchronous transformation is applied to obtain the dq-axis components of the signals involved in the current controller and a synchronous-to-stationary transformation to turn back to stationary frame the outputs of the controller. The DQ Current controller, based on Multivariable-PI technique, tracks the dq-axis reference currents with zero steady-state error and generates the control signal. Finally the PWM module provide the gate signals for each IGBT. The current control strategy is implemented in a 32 bit floating-point DSP from SHARC.

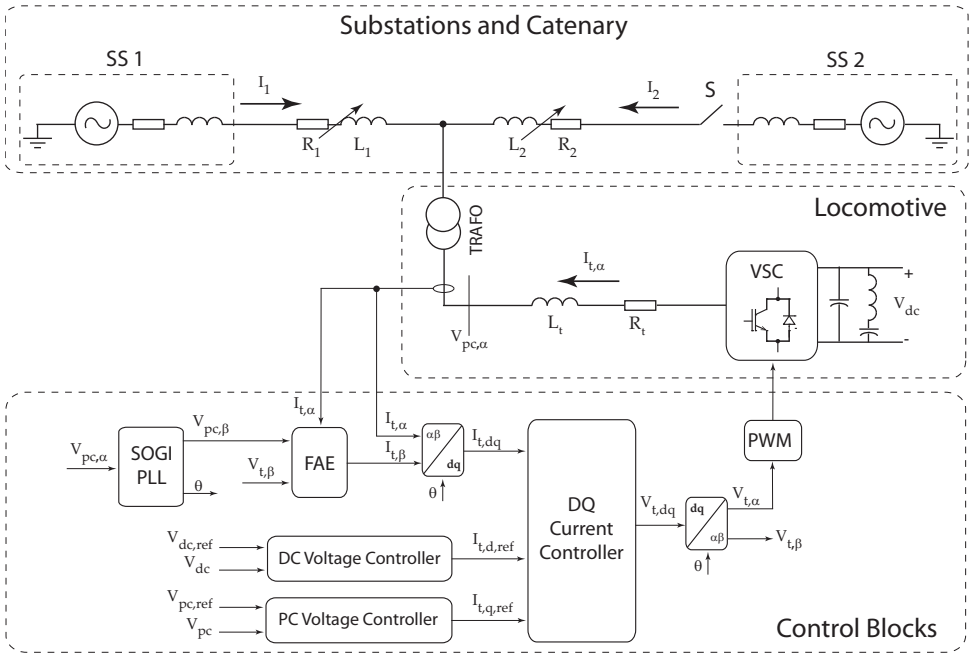

Figure 3.1: Traction network power stage and structure of the control strategy for the locomotive

3.1.1 Parameters of the Model

The parameters of the model are shown in Table 3.1.

Table 3.1: Parameters of the model

Quantity	**Value**	**P.U.**	**Comment**
S_{base}	150 W	1 pu	Base Value of Locomotive Power
U_i	30 V(amplitude)	1 pu	Locomotive Nominal Voltage
V_{dc}	200 V		DC Link Voltage
$n_1 : n_2$	3:1		Transformer Ratio
f	$16^2/_3$ Hz		System Nominal Frequency
f_{sw}	2 kHz		PWM Switching Frequency
f_s	10 kHz		Sampling Frequency
R	1 Ω	0,33 pu	Resistance of VSI Line Filter
L	25 mH	0,873 pu	Inductance of VSI Line Filter

L Filter Design

The procedure to design the correct filter is the same as shown in Section 2.4.1. First, using Eq. 2.3, a value of 2,55 mH is found to obtain a maximum current ripple of 5%. But this is not the inductor used, and the reason is now explained. When the train is in the middle of the line, the catenary impedance between the coupling point of the train and the closest substation is maximum. In this case, between the output voltage of the VSI (which is a very distorted voltage) and the very clean sinusoidal voltage of the closest substation there are few impedances as represented in Figure 3.2. The distortion in U_i depends on how electrically far is this point from the distorted voltage of the VSI. So the ratio L_{cat}/L_f is now considered (neglecting the trafo impedance and considering pure inductances), the distortion can be reduced either reducing the catenary inductance, or increasing the filter inductance. When the train is in the middle of the line, the distortion seen was too high, so the value of the L filter was increased until 25 mH.

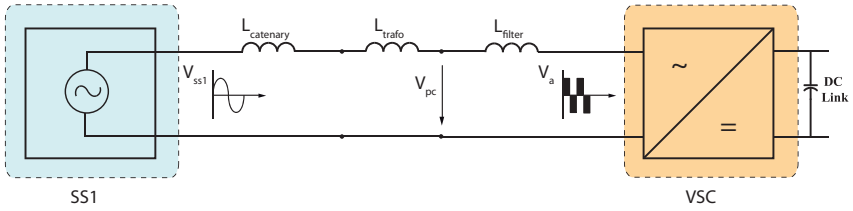

Figure 3.2: Detail of the impedances between the locomotive and the closest substation

3.2 Simulation Results

To evaluate the current controller, several current steps were applied to the system in both d and q axis. The performance of the controller is shown in Figure 3.3. At time instant $t = 0,2\ ms$ $I_{d,ref}$ is set to 1 pu and at time instant $t = 0,4\ ms$ d and q-axis reference currents are set to 0,6 pu and 0,8 pu, respectively.

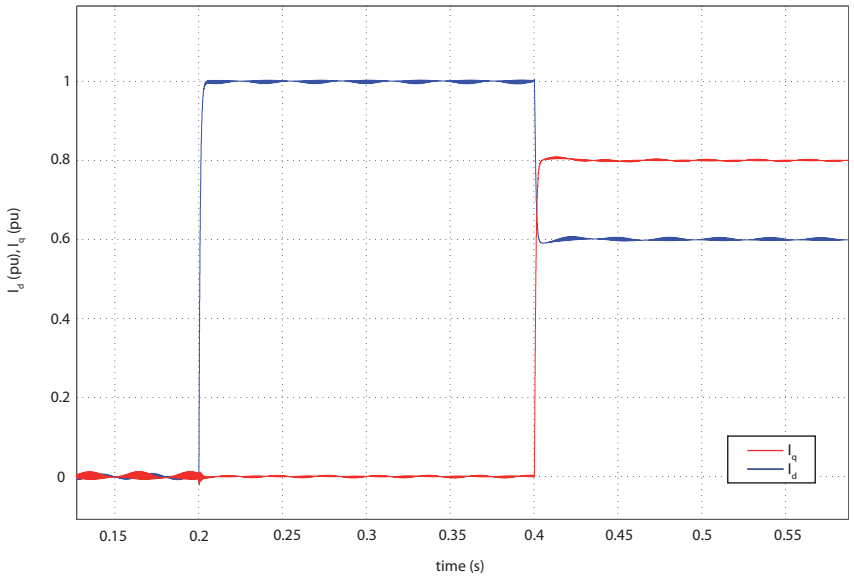

Figure 3.3: Transient response to step changes in d and q-axis reference currents

4 Experimental Results

4.1 Description of the Setup

The implementation of the control strategy for the substation has been done in a 16-bit DSP developed by Microchip, DSPIC30F6010A, which provides a C programming environment. A DSPIC board provided by the "Laboratoire d'Électronique Industriel" has been used.

A picture of the setup is shown in Figure 4.1 and Figure 4.2.

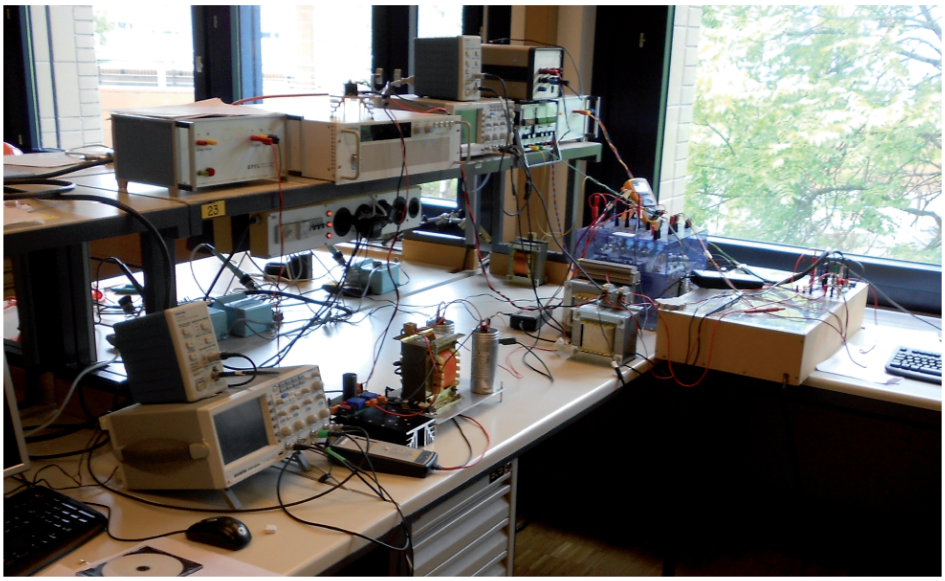

Figure 4.1: Experimental setup

The DSP has been configured with the PWM modulation especified in Section 2.3.2, the ADC (Analog to Digital Converter) for correclty sample all the measurements at 10 kHz, also dead times have been included to avoid shortcircuits in the DC link capacitor and all the needed registers have been configured to obtain data, to communicate with a PC for changing different variables of the controller online, etc.

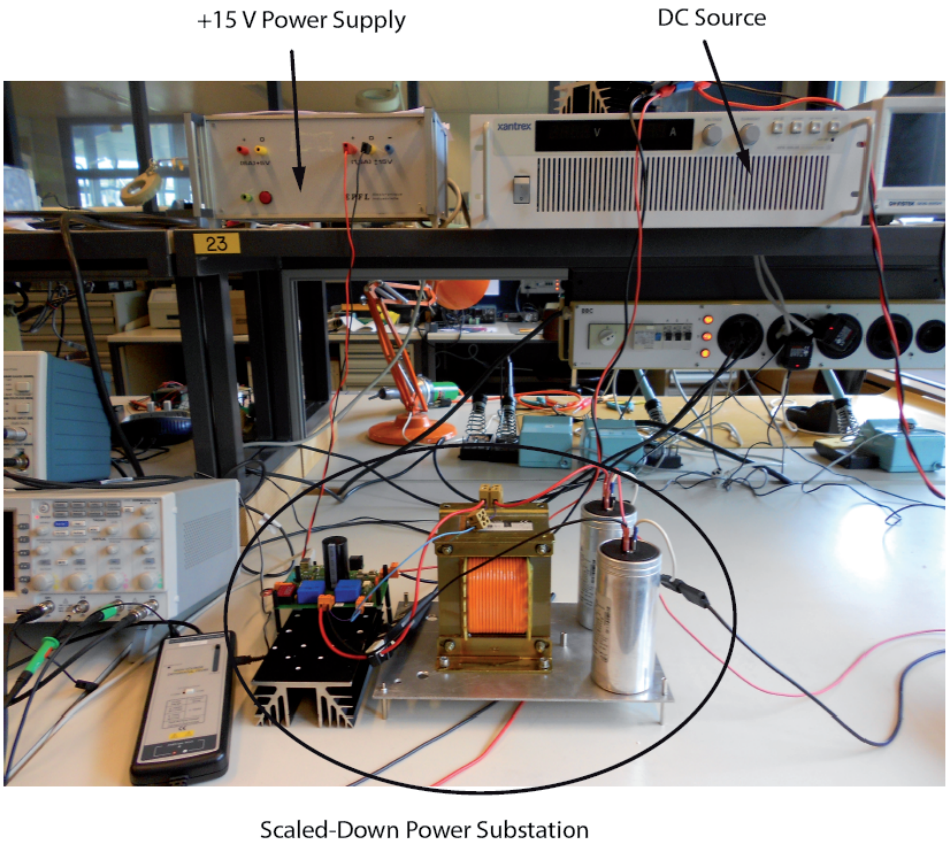

Figure 4.2: Scaled-Down Power Substation

4.2 Performance Evaluation: Resistive Load

A variable resistance has been used to apply different load steps. Figure 4.3 shows an schematic of the test.

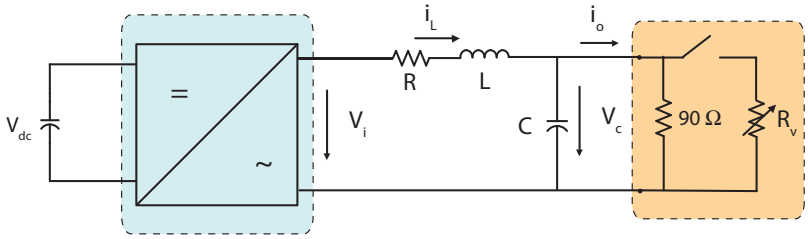

Figure 4.3: Test system consisting on a resistive load

A. Current feedforward sensing the load current with a current sensor

This configuration belongs to the scheme of Figure 2.17. A current sensor (LEM) has been connected in series with the load and a voltage divider circuit and some passive elements have been placed to scale the measurement and send it to an analog input of the DSPIC board. A discrete filter has been implemented in the codes because the current measure contained some noise and that caused the output of the controller to oscillate and, in consequence, the output voltage of the substation was not completely clean.

Figure 4.4 and Figure 4.5 show the response of the controller to different current steps.

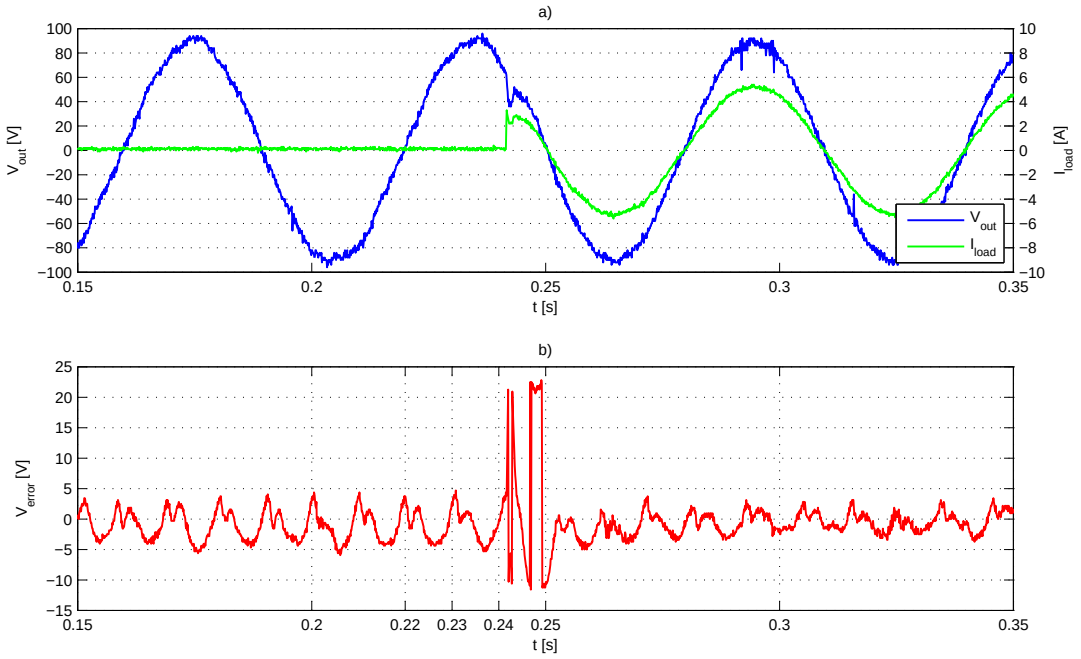

Figure 4.4: Resistive load step from no load to 5,5 A. (a) Output voltage and load current transients (b) Reference voltage - Output voltage

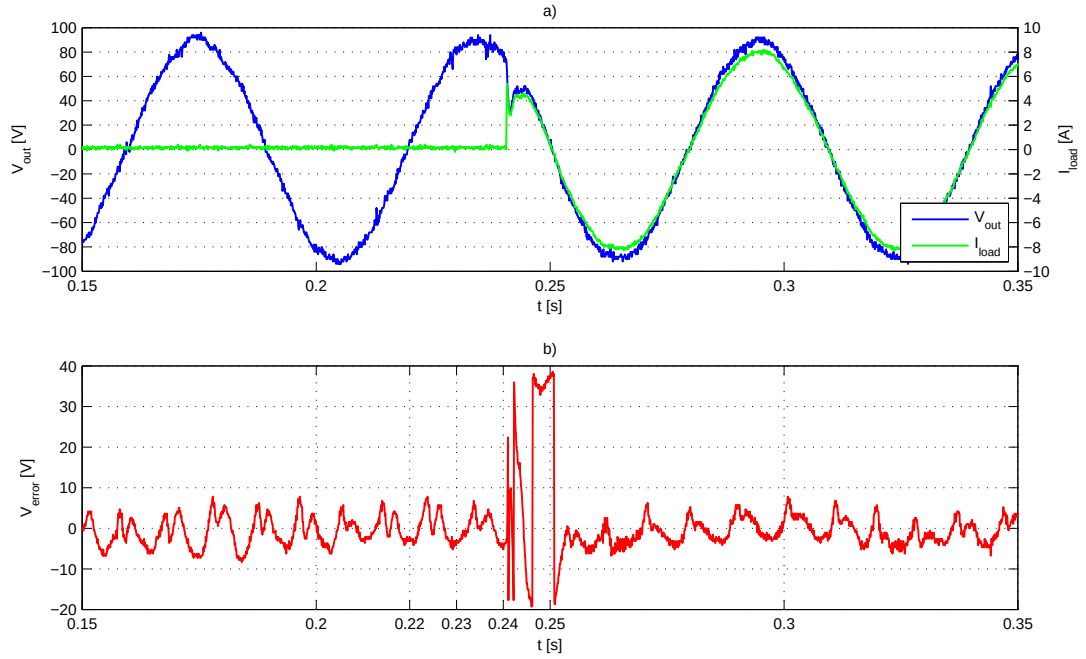

Figure 4.5: Resistive load step from no load to 8 A. (a) Output voltage and load current transients (b) Reference voltage - Output voltage

B. Current feedforward filtering the inductor current

A controller following the structure shown in Figure 2.18 has been implemented in the DSP. The low-pass filter for filtering the inductor current has been tunned at 48 Hz to cut all the high frequency harmonics of this signal. Several tests have been done to validate the performance of the controller.

Figure 4.6 and Figure 4.7 show the response of the controller to different current steps.

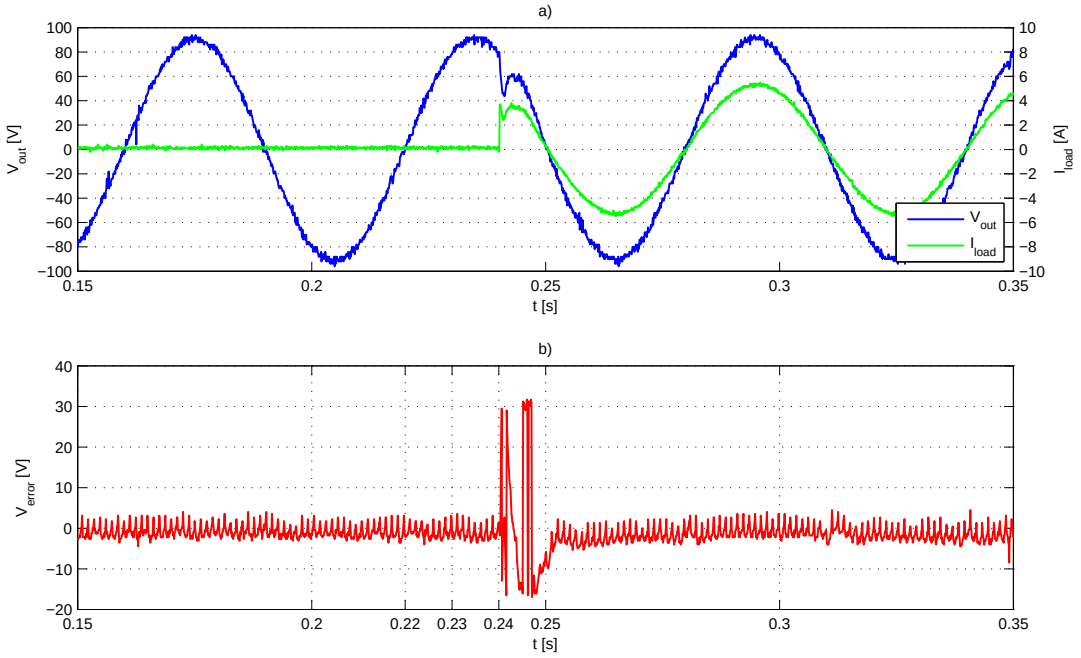

Figure 4.6: Resistive load step from no load to 5,5 A. (a) Output voltage and load current transients (b) Reference voltage - Output voltage

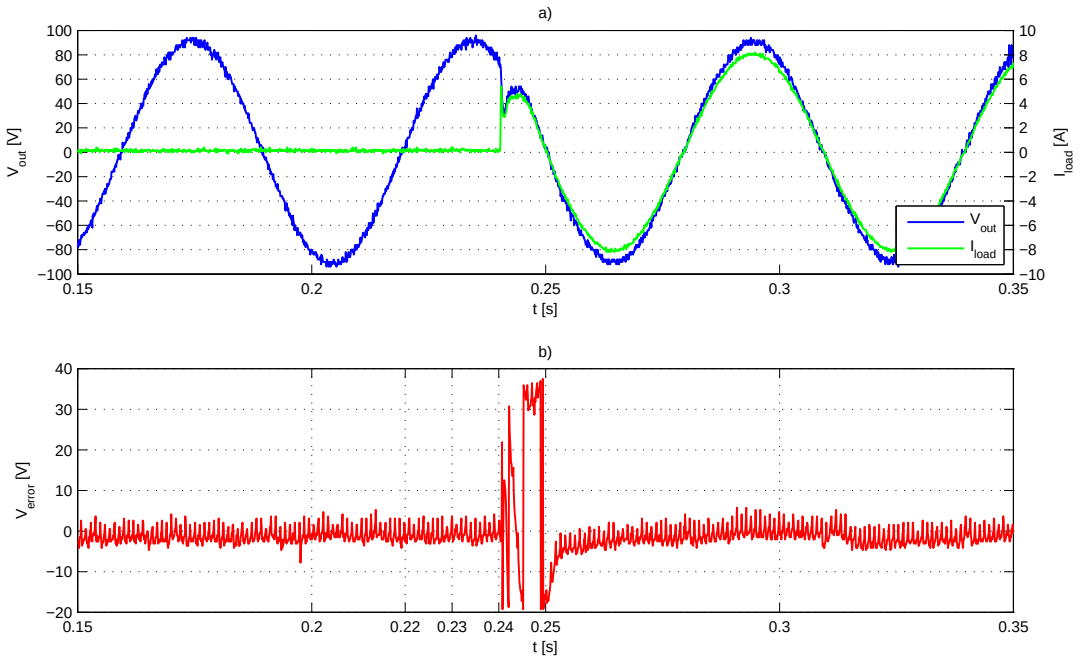

Figure 4.7: Resistive load step from no load to 8 A. (a) Output voltage and load current transients (b) Reference voltage - Output voltage

With a resistive load the current and the voltage are in phase as it can be observed in those figures. To correctly evaluate the performance of the controller it is better to compare both estrategies, A and B, applying load steps at the same current level. This was difficult with a manual switch but the captures were good enought to make conclusions. The voltage and the current were measured with differential probes and the voltage error was extracted with a Digital to Analog Converter from the DSPIC.

Comparing Fig 4.5 and Fig 4.7, there are no big differences in terms of error peak and response time between doing the current feedforward measuring directly the load current or filtering the inductor current as an estimation of the load current. This could happen because a heavy filter of 25 Hz was needed in the load current measure so an additional delay was introduced and, in consequence, the load current disturbance was not as good compensated as it could be. The noise source could be the external board built for the current measurement with "through hole" components, wiring and an improvised connection to the analog input of the DSPIC.

A response time of 10 ms has been obtained and is considered fast enought for this railway application. The maximum voltage error is around 40 % when a current step of 8 A is applied by a manual switch, it is good enought because the current steps that will be applied to the system with the locomotive (current converter) will not be a step with almost infinite slope so the error will be much less.

As it can be observed in the error pictures the voltage error with approach B contains high frequency ripple of 770 Hz, and with approach A the ripple frequency is 90 Hz. This error is the difference between the mesured voltage and the reference voltage, this means that the output voltage contains lower frequency harmonics in case A. A possible reason to explain this low frequency ripple is that the output of the controller, the control signal, is not perfectly sinusoidal and contains some ripple that affect directly to the voltage of the H-bridge inverter and consequently to the output voltage of the substation.

4.3 Performance Evaluation: Resistive-Inductive Load

The performance is now evaluated adding an inductor in series with a resistor as a load for the substation. The test system is shown in Figure 4.8.

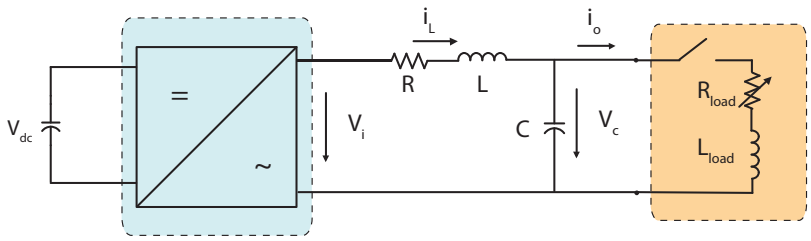

Figure 4.8: Test system consisting on a RL load

In this test the load consists on a resistance and an inductor in series with a phase shift between the load current and voltage of 30° in the first test (5 A) and 54° for the 8 A test. So when the current step is applied at the same position of the voltage curve, the amount of current involved is lower than with the resistive load because of that phase shift, this explains the lower peak of voltage error. Observing now the ripple in this voltage error, the current measure in approach A introduces some distortion that increases the ripple until a bit more than 5 V in steady-state whereas with approach B the ripple is located around half of that value, 2,5 V.

A. Current feedforward sensing the load current with a current sensor

Figure 4.9 and Figure 4.10 show the response of the controller to different current steps.

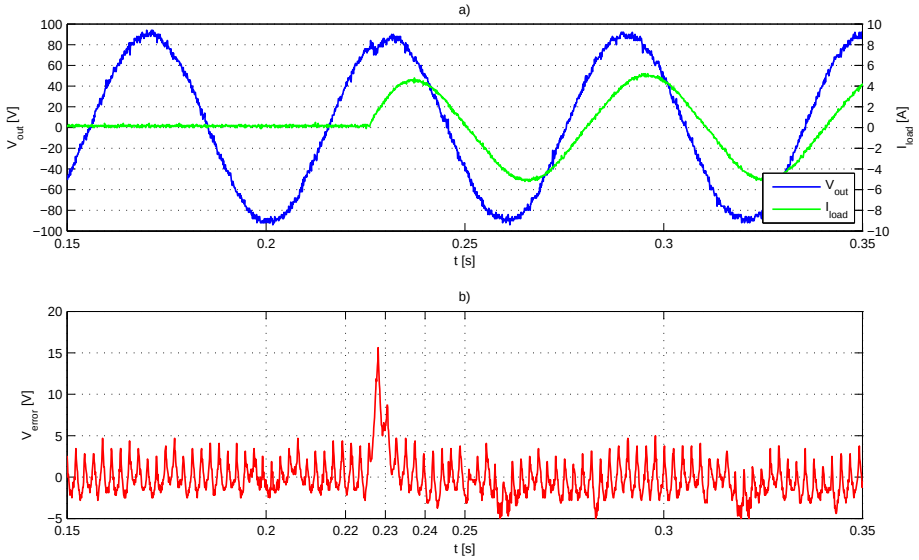

Figure 4.9: RL load step from no load to 5 A. (a) Output voltage and load current transients (b) Reference voltage - Output voltage

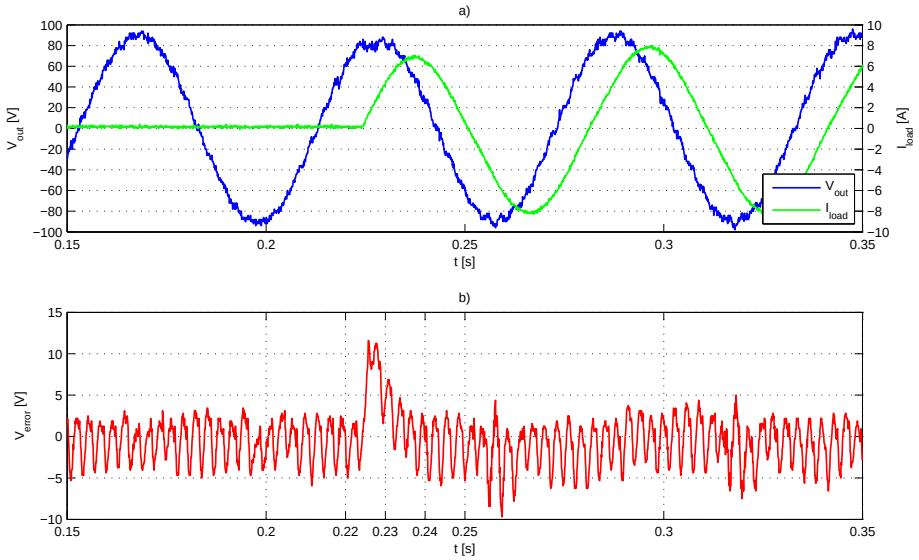

Figure 4.10: RL load step from no load to 8 A. (a) Output voltage and load current transients (b) Reference voltage - Output voltage

B. Current feedforward filtering the inductor current

Figure 4.11 and Figure 4.12 show the response of the controller to different current steps.

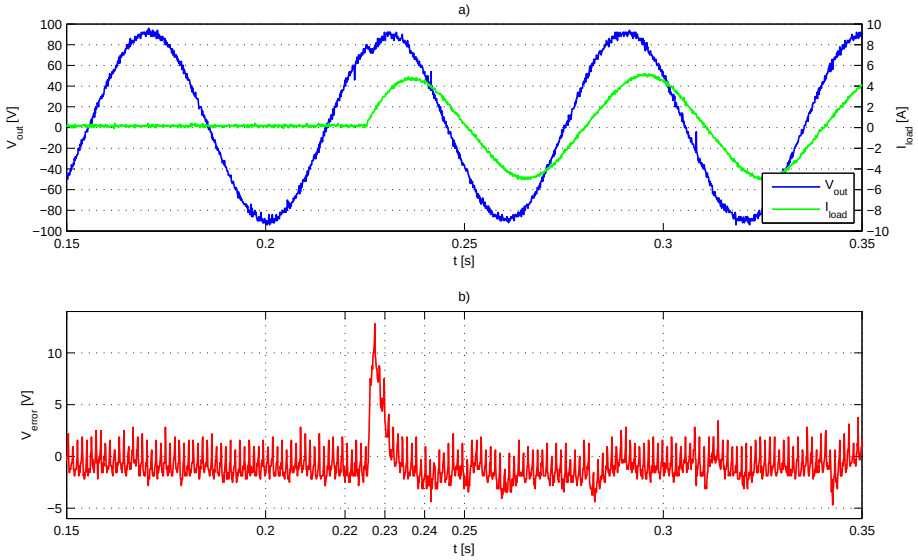

Figure 4.11: RL load step from no load to 5 A. (a) Output voltage and load current transients (b) Reference voltage - Output voltage

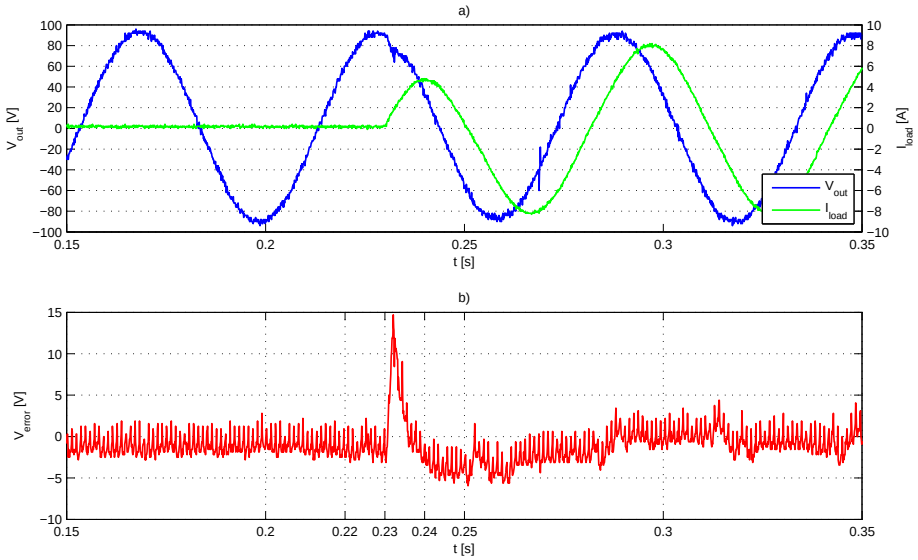

Figure 4.12: RL load step from no load to 8 A. (a) Output voltage and load current transients (b) Reference voltage - Output voltage

4.4 Effect of the Current Feedforward in the Voltage Controller

This section demonstrates that adding a feedforward of an approximation of the load current by filtering the inductor's current helps the controller to achieve the steady-state with a shorter transient.

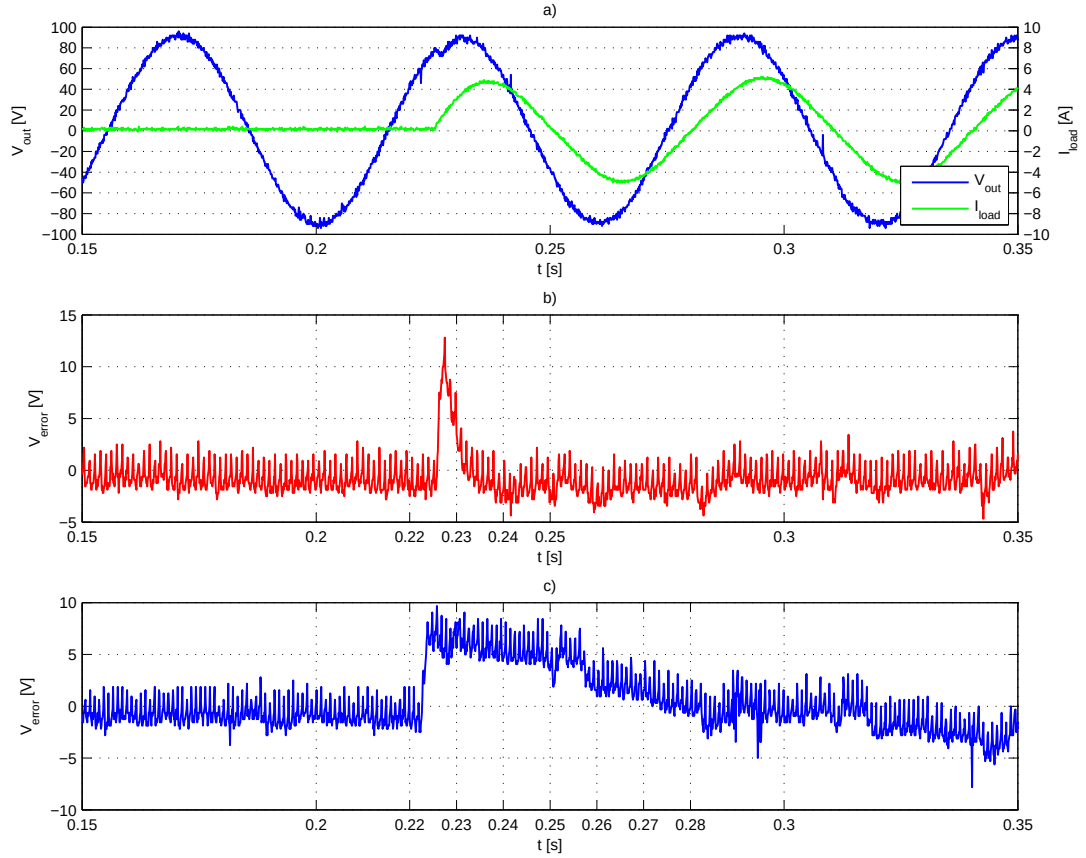

Figure 4.13: RL load step from no load to 5 A. (a) Output voltage and load current transients (b) Voltage error with feedforward filtering inductor's current (c) Voltage error without feedforward

As it can be observed in Figure 4.13, where the voltage error with or without feedforward is shown, including the load current feedforward helps the controller to achieve with a faster transient the steady-state mantaining the voltage peak at a reasonable value. The time to reach steady-state is five times less, enought to experimentally validate the disturbance rejection cabalitity of the voltage control strategy.

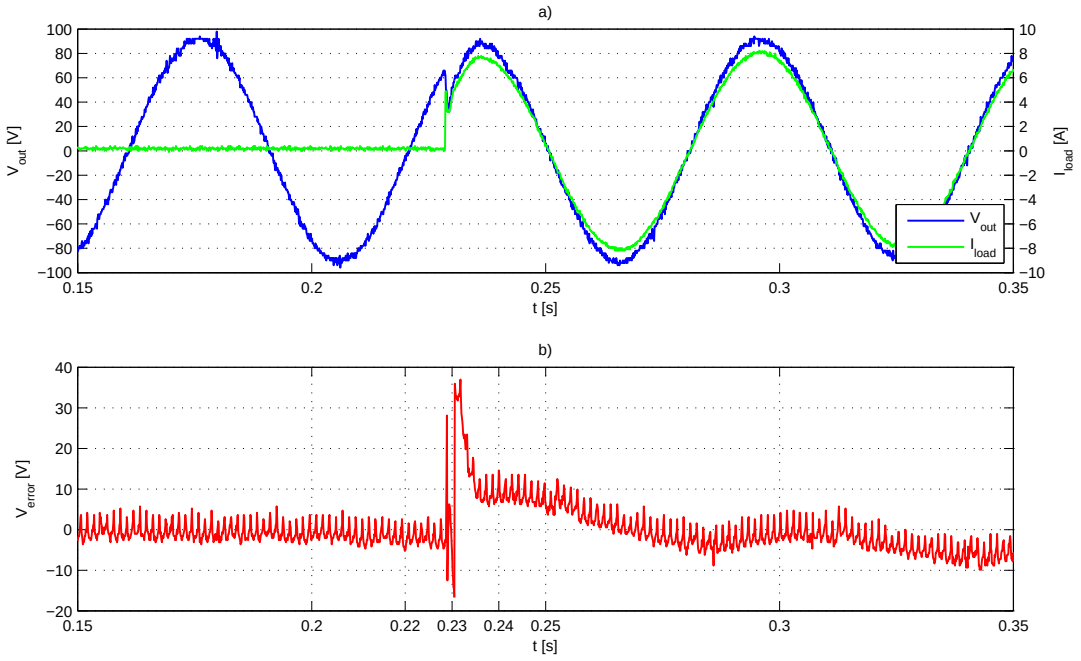

Figure 4.14: Resistive load step from no load to 8 A. (a) Output voltage and load current transients (b) Reference voltage - Output voltage

4.5 Effect of the Filter of the Current Feedforward in the Voltage Controller

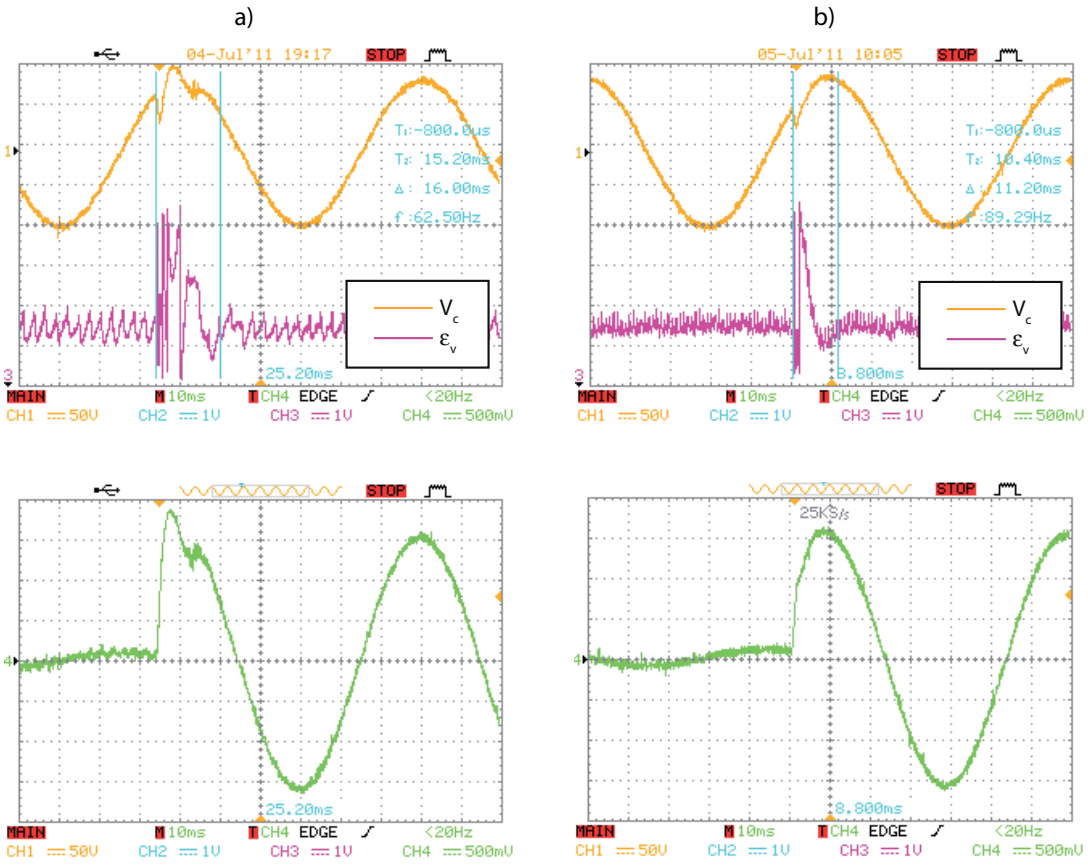

Figure 4.15: Load step from no load to 8 A. (a) Voltage and voltage error (amplified) during the transient and inductor current filtering at 200 Hz cut-off frequency (b) Voltage and voltage error (amplified) during the transient and inductor current filtering at 24 Hz cut-off frequency

The effect of changing the cut-off frequency of the filter of the feedforward or, in other words, the parameter K_f of Figure 2.18, is shown in Figure 4.15. The test consisted on a load step from no load to 8 A. As demonstrated before in simulation, applying a heavier filter increases the damping effect into the voltage error. With those parameters the delay introduced by the heavier filter does not slow down so much the performance of the controller.

4.6 Performance Evaluation: One Substation One Locomotive

The most interesting test belows to this section. Now the substation is connected to a current converter which represents a locomotive. The current converter consists in a single-phase inverter with the current control strategy based on FAE and Multivariable-PI described in Section 3.1. The test system is represented in the schematic of Figure 4.16 and the setup in Figure 4.17 and Figure 4.18.

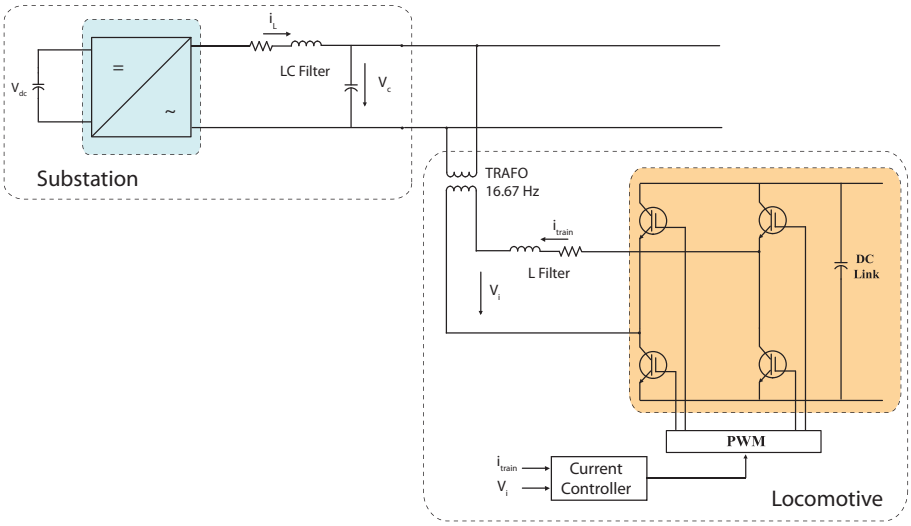

Figure 4.16: Test system with a current converter as a load

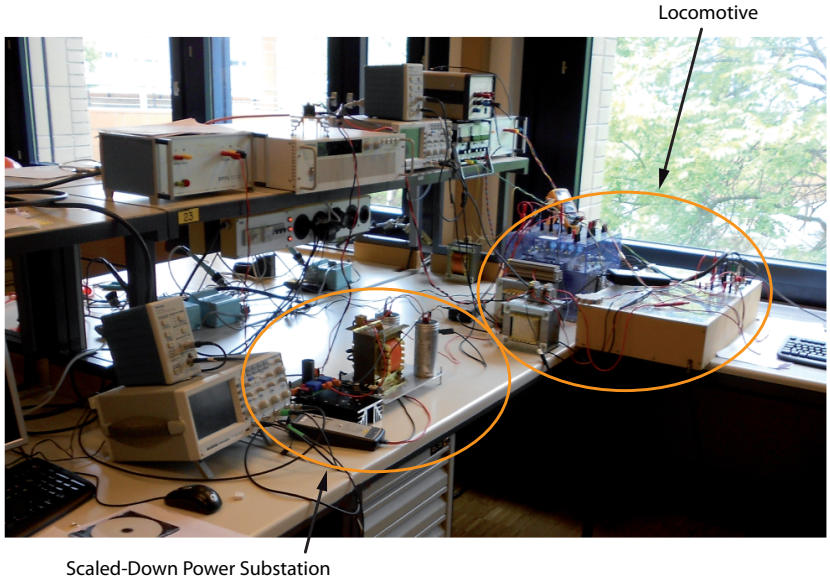

Figure 4.17: One Substation - One Locomotive

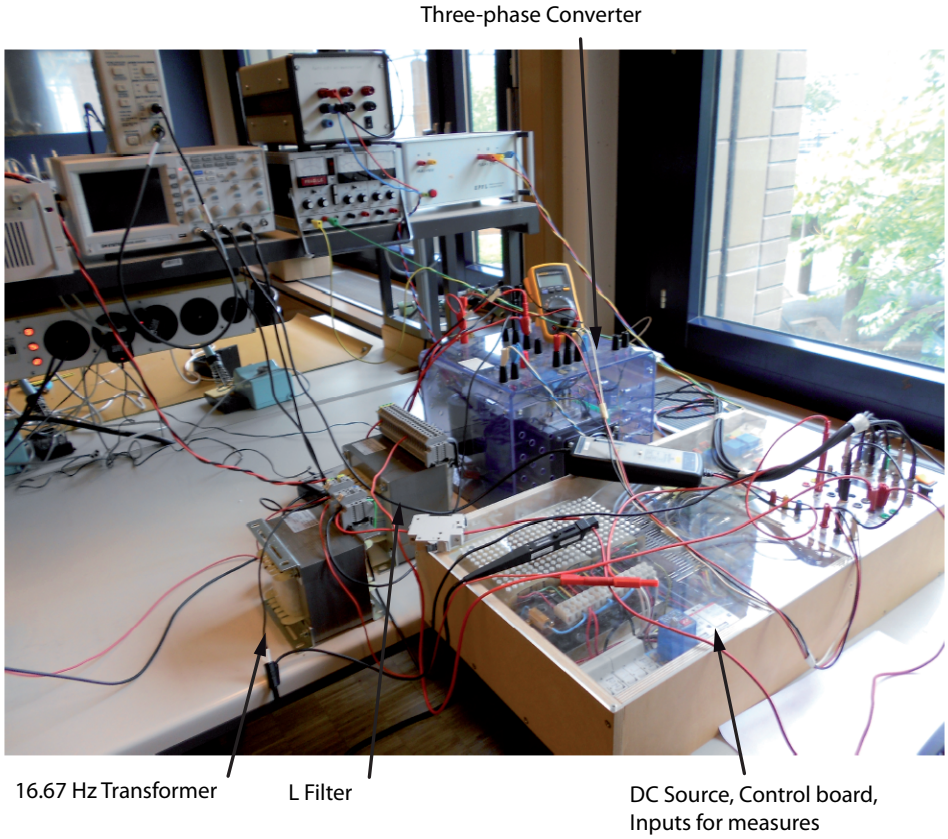

Figure 4.18: Model of the locomotive

For the locomotive, two legs of a three-phase converter made of IGBT were used, as well as a single-phase $16^2/_3$ Hz transformer with a turn ratio 3:1 and an inductor of 25 mH as a filter. The output voltage of the substation was 90 V amplitude value, so the voltage at the secondary of the transformer was 30 V amplitude value. The switching frequency of the inverter was 2 kHz, the sampling frequency 10 kHz and the rest of paramenters were the same as described in Table 3.1. The box shown in Figure 4.18 has a DC Voltage output of 270 V, contains the control board with a SHARC microprocessor, a measurements board made of LEMs for current and voltage measures with the required wiring to send the signals to the microprocessor and other elements not needed for this application.

For this test, the SHARC was programmed with a current control strategy mentioned in Section 3.1 based on FAE and a Multivariable-PI controller, [11] and [12]. A relevant observation after the implementation of this control method is the importance of the correct balancing between the fictive axis and the real axis. An accurate identification of the exact parameters of

the resistance and inductance of the system is essential for the correct operation of the FAE. If the fictive plant differs from the real plant the fictive current and the real current could not have the same amplitude, or even worst, they could not be ortogonal any more. If that happens, the dq components generated by the stationary to synchronous transformation are not constant, and the PI controller will not provide a good response. After several tests in open and closed loop with a 50 Hz grid, finally the correct parameters for the FAE and the Multivariable-PI where found so the current converter was ready to be connected to the $16^2/_3$ Hz substation.

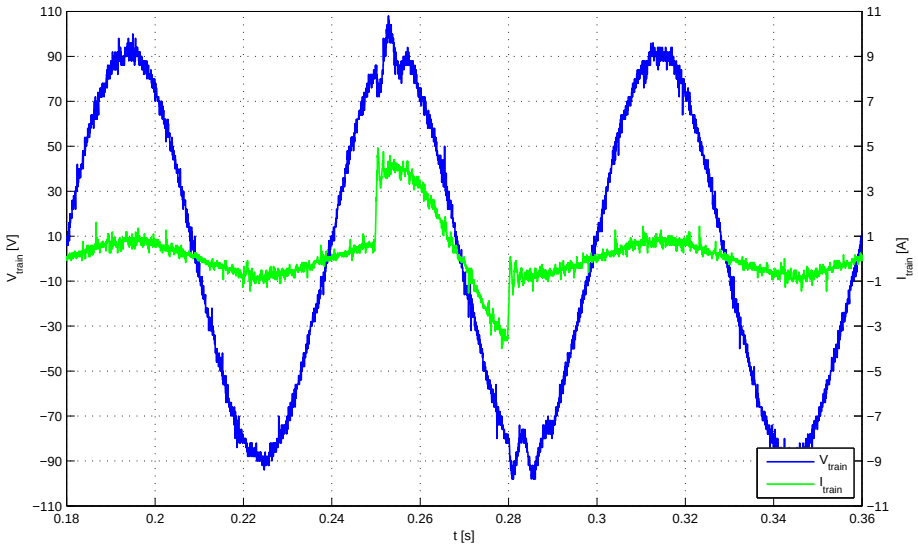

Figure 4.19: 4 A Current step with current converter as a load

A current step of 4 A and 30 ms was applied to the substation and the results were quite good as it can be observed in Figure 4.19. The voltage controller was capable to track the reference with a response time around 10 ms with an acceptable error. This error peak is not a problem because in real railway systems the current step created by a train can take sometimes one or two seconds, not few milliseconds as in this test, so the voltage would be much less affected.

5 Economic and Environmental Analysis

5.1 Economic Analysis

An economic analysis is done in this chapter. First the cost of the prototype is exposed and afterwards the cost in terms of research and development is presented.

5.1.1 Cost of the Prototype

The cost of all the components of the prototype is broken down in Table 5.1. The labor cost is considered 25 € per hour.

Table 5.1: Cost of the prototype

Description	**Quantity**	**Reference**	**Cost [€]**
Power IGBT	4	IRGB4062DPbF	27,28
Optocoupler	2	HCPL314J	5,70
Current Mesure	1	LA25NP	22,29
Voltage Mesure	1	LV25-P	73,57
DC Voltage Mesure	1	AD629	8,35
Quad Low-Power 10MHz Rail-to-Rail I/O Operational Amplifier	1	LM6134BIM	4,08
TRACO	1	TRACO TEL3	14,70
Voltage Regulator	1	TL780-05KCS	0,74
1 Amp General Purpose Rectifier	2	1N4005	0,2
Capacitor DC link	1	-	18,02
Capacitors	11	-	1,87
Resistors	22	-	4,50
Connectors	6	-	4,35
Fuse 10 A	1	-	0,21
Heat Sink	1	-	1,60
PCB	1	-	45
Inductor (output LC filter)	1	-	35
Capacitor (output LC filter)	1	-	25
Labor	16h	-	400
DSPIC board	1	-	150
Total			**842,46**

5.1.2 Research and Development

The cost of the prototype in terms of R&D includes the research, design, implementation in the DSPIC of the voltage control strategy and the experimental validation of the scaled-down power substation. The cost of the tools used in this project like the computer and simulation software are calculated based on a 3 year amortization and a project lenght of 5 months. The software for programming the DSPIC, MPLAB, is free software provided by Microchip so is not included in the list.

Table 5.2: Cost related to computer tools

Description	**Price [€]**	**Amortizised price [€]**
Computer	1000	139
Matlab/SIMULINK	1800	250
Total		**389**

Table 5.3 show the cost of research, design, implementation in the DSPIC and experimental validation considering a prize per hour of 40 €.

Table 5.3: Cost related to research, design and implementation in the DSPIC

Description	**Hours**	**Total cost [€]**
Research	240	9600
Design	360	14400
Implementation in the DSPIC	360	14400
Experimental validation	240	9600
Total		**48000**

The total cost in terms of R&D is **48389 €**.

5.1.3 Total Cost of the Project

The resume of all the components of the total cost of this project is presented in Table 5.4.

Finally the total cost of the project obtained is **59835,92 €**.

Table 5.4: Total cost

Description	**Total cost [€]**
Prototype	842,46
Research and Development	48389
Subtotal	**49231,46**
Unforeseen expenses (3%)	1476,94
Total	**50708,40**
IVA (18 %)	9127,51
Total (including IVA)	**59835,92**

5.2 Environmental Analysis

In project management it is always important to consider the interaction with the environment. In this master thesis, a prototype of a regulated $16^2/_3$ Hz power supply has been manufactured, so the effects against the environment that this product could cause during its development and operation are analysed. This environmental analysis take into account the materials used to built up the prototype, the energy consumption and the correct recycling of all the components.

5.2.1 Materials Used in the Prototype

The prototype manufactured in this master thesis fulfil the requirements of the RoHS Directive 2002/95/EC (Directive on the restriction of the use of certain hazardous substances in electrical and electronic equipment).

5.2.2 Energy Consumption

The energy consumption of all the electric devices which take part in the prototype development is not so high compared with the energy consumption during the operation of the power supply along its expected life. The effects against the environment come from the generation of this electric energy and it has to be considered the emissions of sustances harmful to the environment.

Regarding the Electromagnetic compatibility (EMC), this prototype is connected to the grid between a DC power supply, so first of all the high frequency current harmonics in the DC

side of the converter absorved by the DC power supply have to be considered. Depending on the harmonic content in the current consumption, the power absorved by the prototype and the harmonic rejection capability of the DC power supply some current harmonics could be injected to the grid. The harmonic content is high but the power consumed is limited to 450 W, furthermore if a good DC source is chosen the whole setup will meet the requirements of the EMC.

5.2.3 Components recycling

The european directive who regulates the recycling of all electrical goods is 2002/96/EC WEEE (Waste Electrical and Electronic Equipment), which imposes the responsability for the disposal of waste electrical and electronic equipment on the manufacturers of such equipment. Following this directive, there is a commitment on the side of this master thesis to collect and recycle every component of this prototype.

Conclusions

In this project a 16⅔ Hz regulated power supply for traction systems has been developped and experimentally validated.

The results of the conducted study are:

- The substation is capable to provide a regulated 16⅔ Hz voltage of 90 V with a maximum current of 10 A.
- When a resistive load consuming 8 A (amplitude) is suddently connected the controller is capable track the reference voltage with zero steady-state error and a response time of 10 ms.
- Experimentally validated the performance under non linear loads (converter) up to 4 A with zero steady-state error and a response time of 10 ms.
- Voltage control strategy with a current feedforward filtering the inductor's current is experimentally validated.
- Voltage control strategy with disturbance rejection capability is experimentally validated.
- A Full DQ and Hybrid versions of voltage control are developped and validated by simulations.

The obtained results have been considered successful. The scaled-down power substation is in service, ready for future works on it.

Future works:

- Improve the transient response of the voltage control strategy.
- Implement a Full DQ Synchronous Voltage Control Strategy.
- Implement a Hybrid Stationary/Synchronous Voltage Control Strategy.

Acknowledgements

It is a pleasure to thank all who made this thesis possible, especially Prof. D. Montesinos, for his excellent guidance, support and patience. Without him, I could not perform this thesis in "École Polytechnique Fédérale de Lausanne". I would also like to acknowledge the support of CITCEA-UPC.

I owe my deepest gratitude to my supervisor in EPFL Prof. A. Rufer, who gave me the opportunity to develop my thesis in the "Laboratoire d'Électronique Industriel".

I would also like to express my sincere appreciation to Mr. Bahrani Behrooz, for his invaluable attention and guidance throughout my stay in the EPFL-LEI. Without his advices, guidance and support this work would not have been successful.

I am grateful to my entire family and my friends, for providing a lovely environment for me.

Lastly, and most importantly, I wish to thank my parents Carles and Aurora, and Patricia, for their understanding, endless patience and encouragement when it was most required.

References

[1] Yun Wei Li. Control and Resonance Damping of Voltage-Source and Current-Source Converters LC Filters. 56(5):1511–1521, 2009.

[2] L. Abrahamsson and L. Soder. Railway Power Supply Investment Decisions Considering the Voltage Drops - Assuming the Future Traffic to Be Known. In *Proc. 15th Int. Conf. Intelligent System Applications to Power Systems ISAP '09*, pages 1–6, 2009.

[3] M. Aeberhard, C. Courtois, and P. Ladoux. Railway traction power supply from the state of the art to future trends. In *Proc. Int Power Electronics Electrical Drives Automation and Motion (SPEEDAM) Symp*, pages 1350–1355, 2010.

[4] René Schäfer. Vom Hydrogenerator über rotierende Umformer zum vollstatischen Umrichter. *Bulletin SEV/VSE*, 11/93.

[5] J. Ranneberg. Transformerless topologies for future stationary AC-railway power supply. In *Proc. European Conf. Power Electronics and Applications*, pages 1–11, 2007.

[6] T. Undeland N. Mohan and P. Robbins. *Power Electronics: Converters, Applications and Design.* Second edition, 1995. Page 212.

[7] T. Undeland N. Mohan and P. Robbins. *Power Electronics: Converters, Applications and Design.* Second edition, 1995. Pages 203-210.

[8] P. A. Dahono, A. Purwadi, and Qamaruzzaman. An lc filter design method for single-phase pwm inverters. In *Proc. Int Power Electronics and Drive Systems Conf*, pages 571–576, 1995.

[9] H. Karimi, H. Nikkhajoei, and R. Iravani. Control of an Electronically-Coupled Distributed Resource Unit Subsequent to an Islanding Event. 23(1):493–501, 2008.

[10] D. N. Zmood and D. G. Holmes. Stationary frame current regulation of pwm inverters with zero steady-state error. 18(3):814–822, 2003.

[11] B. Bahrani, A. Rufer, S. Kenzelmann, and L. A. C. Lopes. Vector Control of Single-Phase Voltage-Source Converters Based on Fictive-Axis Emulation. 47(2):831–840, 2011.

[12] B. Bahrani, S. Kenzelmann, and A. Rufer. Multivariable-PI-based DQ Current Control of Voltage Source Converters with Superior Axes Decoupling Capability. (99), 2010. Early Access.

[13] M. Ciobotaru, R. Teodorescu, and F. Blaabjerg. A new single-phase pll structure based on second order generalized integrator. In *Proc. 37th IEEE Power Electronics Specialists Conf. PESC '06*, pages 1–6, 2006.

[14] S. Kenzelmann, P. Barrade, Y. Louvrier, and A. Rufer. The monophasor theory: Analytical development and practical demonstration on a single phase voltage source inverter: In remembrance of Hansruedi Bühler. In *Proc. 13th European Conf. Power Electronics and Applications EPE '09*, pages 1–10, 2009.

[15] Simone Buso and Paolo Mattavelli. Digital Control in Power Electronics. *Synthesis Lectures on Power Electronics*, 1(1):105–108, 2006.

Appendices

Appendix A

Detailed description of the prototype

In addition to the brief description of the VSI board done in Section 2.5, the BOM and the schematic of the board are detailed in Table A.1 and Figure A.1, respectively.

Table A.1: Bill of Materials

Comment	**Pattern**	**Quantity**	**Components**	**Description**
IRGB4062DPbF	TO-220AB	4	Q1, Q2, Q3, Q4	Power IGBT
HCPL314J	SO-G16/D10.4	2	OPTO1, OPTO2	Optocoupler
LA25NP	LA25NP	1	LEM1	Current Mesure
LV25-P	LV25-P	1	LV25-P	Voltage Mesure
AD629	SO-G8	1	U2	DC Voltage Mesure
LM6134BIM	SO-G14/E2	1	U1	Quad Low-Power 10 MHz Rail-to-Rail I/O Operational Amplifier
TRACO TEL3	TRACO TEL3	1	TRACO1	+15V,-15V, power supply
Volt Reg	TO-220AB	1	VR1	Voltage Regulator
Diode 1N4005	DIO10.46-5.3x2.8	2	D1, D2	1 Amp General Purpose Rectifier
Cap	CC1310-0504	3	C2, C3, C4	Capacitor
Cap	Cout470uF	1	C8	Capacitor
Cap	RAD-0.3	8	C1, C5, C6, C7, C9, C10, C11, C12	Capacitor
Res1	AXIAL-0.3	17	R5, R6, R7, R8, R9, R10, R11, R12, R13, R14, R15, R16, R17, R18, R20, R21, R22	Resistor
Res2	RES-MIO	4	R1, R2, R3, R4	Resistor
Res2	RSMF3B-3W	1	R19	Resistor
Jumper	RAD-0.2	3	W1, W2, W3	Jumper Wire
Header 10X2	HDR2X10	1	JP5	Header, 10-Pin, Dual row
Header 2	Connector	2	JP1, JP3	Header, 2-Pin
Header 2	Small connector	2	JP2, JP4	Header, 2-Pin
Header 25X2	HDR2X25	1	JP6	Header, 25-Pin, Dual row
Fuse 1	Fuse 24mm	1	F1	Fuse

Also the communications with the DSPIC board are detailed; the most important pin connections are listed below.

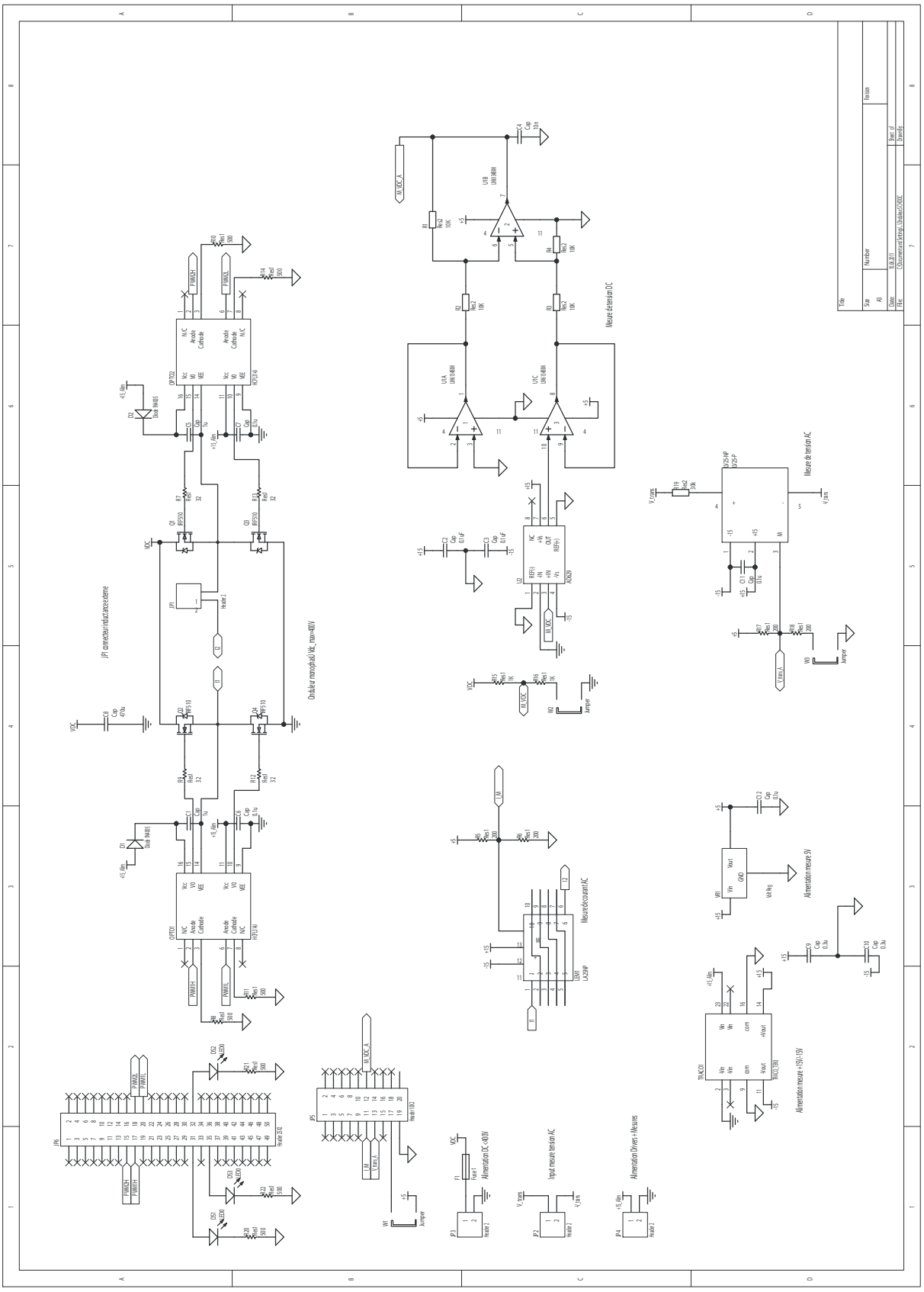

Figure A.1: Schematic of the VSI board

Table A.2: Pin connections

50 pins connector (JP6)		20 pins connector (JP5)	
Pin	**Description**	**Pin**	**Description**
15	PWM2H	11	Current mesure (I_M)
17	PWM1H	12	V_{dc} mesure (M_VDC_A)
18	PWM2L	13	Voltage mesure (V_trans_A)
20	PWM1L		

A picture of the VSI board with DSPIC board is shown in next figure with the schematic below:

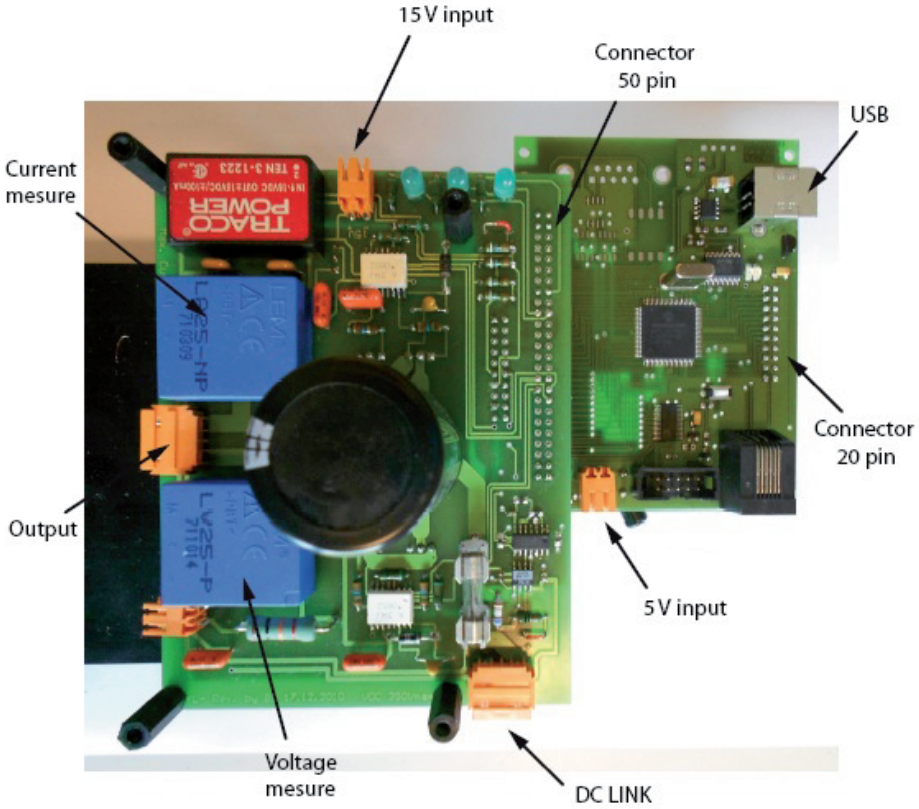

Figure A.2: Picture of the VSI+DSPIC setup

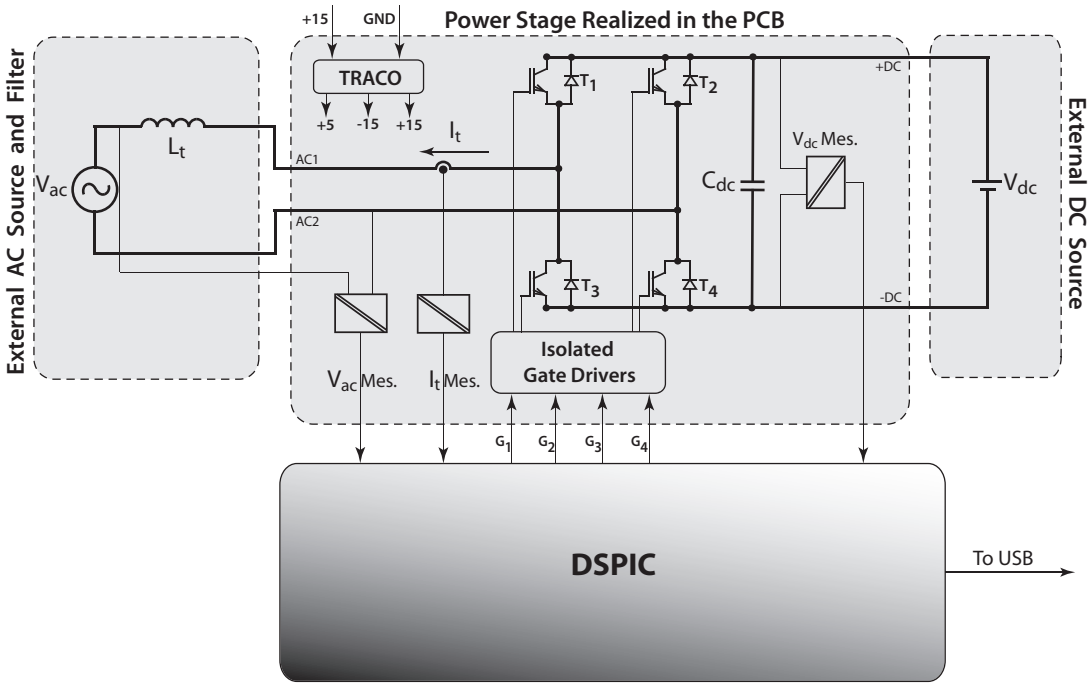

Figure A.3: Schematic of the single-phase converter and control

Appendix B

Synchronous Voltage Control Strategy

B.1 Synchronous Reference Frame System Analysis

Applying KCL (Kirchhoff's current law) in the node of the test system shown in Figure 3.8 in Section 3.4.2 the next equation is found:

$$i_L(t) = i_c(t) + i_0(t) \tag{B.1}$$

$$i_L(t) = C_f \frac{du_c(t)}{dt} + i_0(t) \tag{B.2}$$

Transforming Eq. B.2 from time domain to stationary $\alpha\beta$ frame using monophasor theory [14], the following is obtained:

$$\underline{i}_L^s = C_f \frac{d\underline{u}_c^s(t)}{dt} + \underline{i}_0(t) \tag{B.3}$$

Eq. B.3 transformed into Laplace domain is represented in Figure B.1.

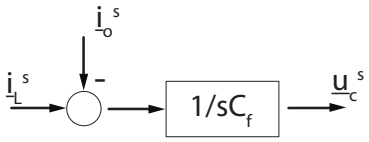

Figure B.1: Representation of Equation B.3 in Laplace domain

In this system the load can change at any time so for the controller the current of the load acts as a disturbance. It is an unknown input in the system as it is not possible to establish a relation as $I_c = U_c/Z_{load}$ because Z_{load} is unknown. Furthermore, the load would be non-linear if a current converter is connected as a load.

Applying a stationary-to-synchronous transformation to Eq. B.3 according to $x_{dq} = x_{\alpha\beta}e^{-j\omega t}$, the following equation in the rotating reference frame is derived:

$$\begin{bmatrix} i_d \\ i_q \end{bmatrix} = C_f \begin{bmatrix} du_{c,d}/dt \\ du_{c,q}/dt \end{bmatrix} + \begin{bmatrix} 0 & -\omega C_f \\ \omega C_f & 0 \end{bmatrix} \begin{bmatrix} u_{c,d}/dt \\ u_{c,q}/dt \end{bmatrix} + \begin{bmatrix} i_{o,d} \\ i_{o,q} \end{bmatrix} \tag{B.4}$$

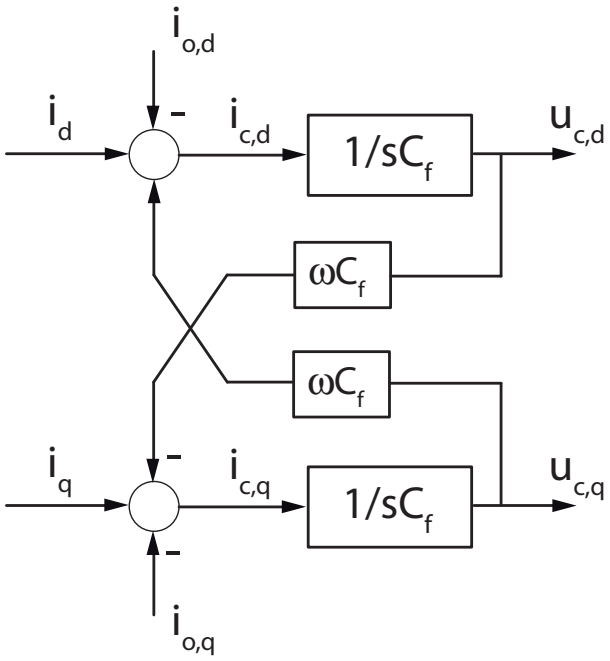

Figure B.2: Representation of Equation B.4 in Laplace domain

Eq. B.4 transformed into Laplace domain is represented in Figure B.2, where the coupling terms of the system are shown.

In order to achieve decoupled control of $u_{c,d}$ and $u_{c,q}$, the current reference that has to provide the voltage controller and feed into the current controller should be as follows:

$$\begin{aligned} i_d &= i_{c,d} - \omega C_f u_{c,q} + i_{o,d} \\ i_q &= i_{c,q} + \omega C_f u_{c,d} + i_{o,q} \end{aligned} \tag{B.5}$$

where $i_{c,d}$ and $i_{c,q}$ are the capacitor reference currents in "d" and "q" axis respectively, and a feedforward of the load current is considered.

By substituting i_d and i_q from Eq B.5 to Eq. B.4, the next system of equations is obtained:

$$\begin{bmatrix} i_{c,d} \\ i_{c,q} \end{bmatrix} = C_f \begin{bmatrix} du_{c,d}/dt \\ du_{c,q}/dt \end{bmatrix} \tag{B.6}$$

As it can be seen in Eq. B.6, the relation between the output of the voltage controller and the voltage we need to regulate is the equation of the capacitor.

The voltage controller has to follow the structure shown in Figure B.3.

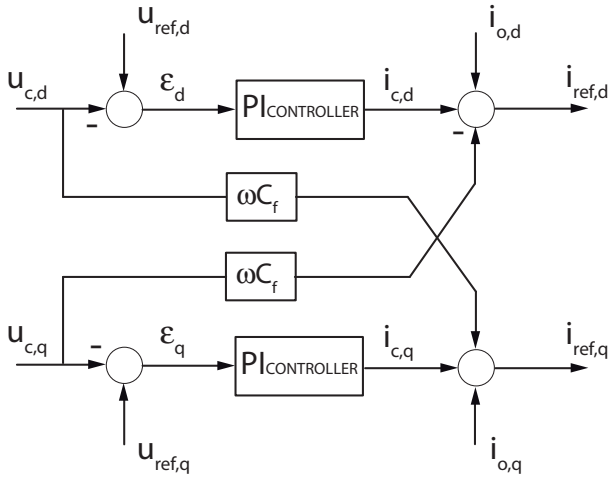

Figure B.3: Structural diagram of the dq voltage controller

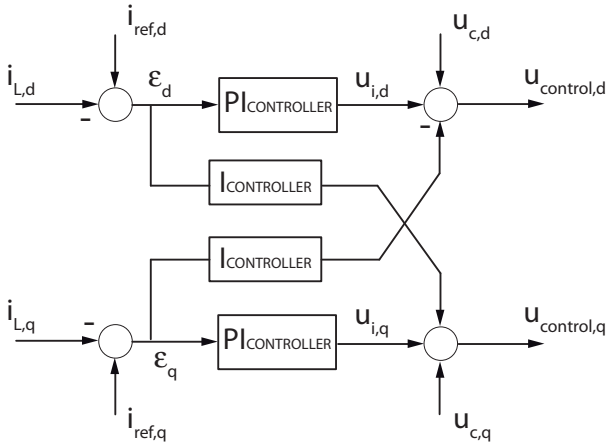

Figure B.4: Structural diagram of the dq current controller

The dq current controller could be just a proportional controller or a PI-controller to achieve zero steady state error. In this system where the main objective is to control the voltage it is not indispensable to have a zero steady state error in the current loop as long as the voltage loop has zero steady state error, but is true that to ensure the dynamics under possible adverse conditions the best option is to have null error in both loops.

Considering now the current loop, FAE in combination with a Multivariable-PI controller, detailed in [11] and [12], is used to create the control signal for the inverter. Figure B.4 shows the structure of the current controller.

At this point, the synchronous double-loop control strategy is represented in Figure B.5.

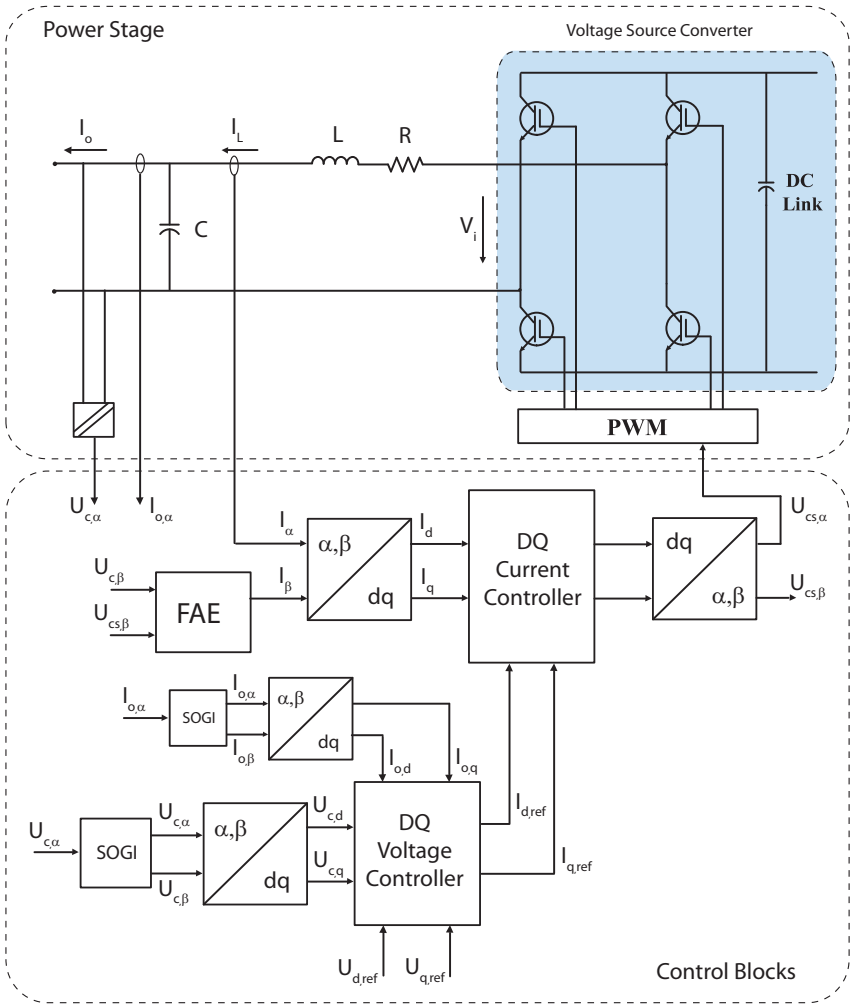

Figure B.5: Test system with the Synchronous Voltage Control Strategy

Design of Current Controller

Plant transfer function:

$$G_c = \frac{I_L}{U_i} = \frac{1}{R_f} \frac{1}{1 + s\frac{L_f}{R_f}} \tag{B.7}$$

Open-loop transfer function:

$$G_{oc} = \frac{I_L}{\epsilon_c} = \frac{sT_n + 1}{sT_i} G_c = \frac{sT_n + 1}{sT_i} \frac{1}{R_f} \frac{1}{1 + s\frac{L_f}{R_f}} \tag{B.8}$$

The parameters T_n and T_i are equal to $\frac{L_f}{R_f}$ and $\frac{1}{R_f}\frac{1}{k}$, the gain k is tuned to achieve the desired response time. So the open-loop transfer function for the current control (neglecting the time constant of the PWM module) is:

$$G_{oc} = \frac{k}{s} \tag{B.9}$$

The coupled terms for the multivariable-PI, both integral controllers, are equal to $\omega\frac{T_n}{T_i}$.

Closed-loop transfer function:

$$G_{cc} = \frac{I_L}{I_{L,ref}} = \frac{G_{oc}}{1+G_{oc}} = \frac{1}{s\frac{1}{k}+1} \tag{B.10}$$

Design of Voltage Controller

Plant transfer function:

$$G_v = \frac{U_C}{I_{C,ref}} = G_{cc}\frac{1}{sC_f} = \frac{1}{s\frac{1}{k}+1}\frac{1}{sC_f} \tag{B.11}$$

Open-loop transfer function:

$$G_{ov} = \frac{U_C}{\epsilon_v} = \frac{T_{nv}s+1}{sT_{iv}}G_v = \frac{T_{nv}s+1}{sT_{iv}}\frac{1}{s\frac{1}{k}+1}\frac{1}{sC_f} \tag{B.12}$$

Again, T_{nv} and T_{iv} are designed to be $\frac{1}{k}$ and $\frac{1}{C_f}\frac{1}{k_v}$, and the gain k_v is tuned to obtain the desired dynamics in voltage loop. The final open-loop transfer function is obtained:

$$G_{ov} = \frac{k_v}{s^2} \tag{B.13}$$

Finally the complete structure of the developped controller is shown in Figure B.6

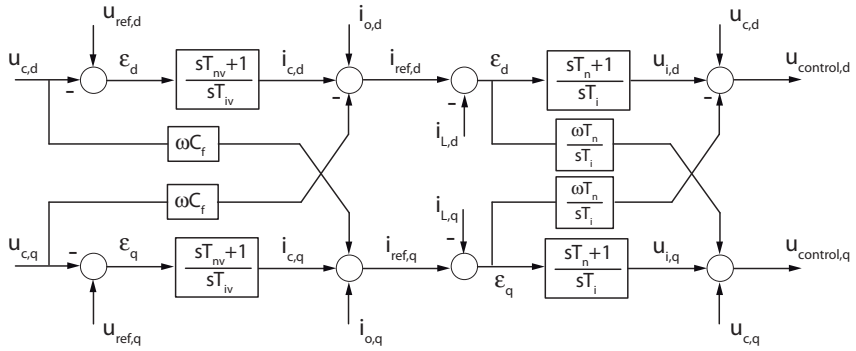

Figure B.6: Structure of the synchronous reference frame controller developped

B.2 Performance Evaluation

With the same test system developped in Matlab/SIMULINK environment described in Section 4.2 and with the same operation conditions the performance of the Synchronous Voltage Control Strategy is evaluated. Figure B.7 shows the simulation results. The voltage controller is capable

to track the voltage reference with a transient response of 4 ms and zero steady-state error. The voltage error peak is at 6,7% of nominal voltage. As it can be observed, both d and q-axis components of the voltage are affected which means that the amplitude and the phase of the voltage are distorted during the transient.

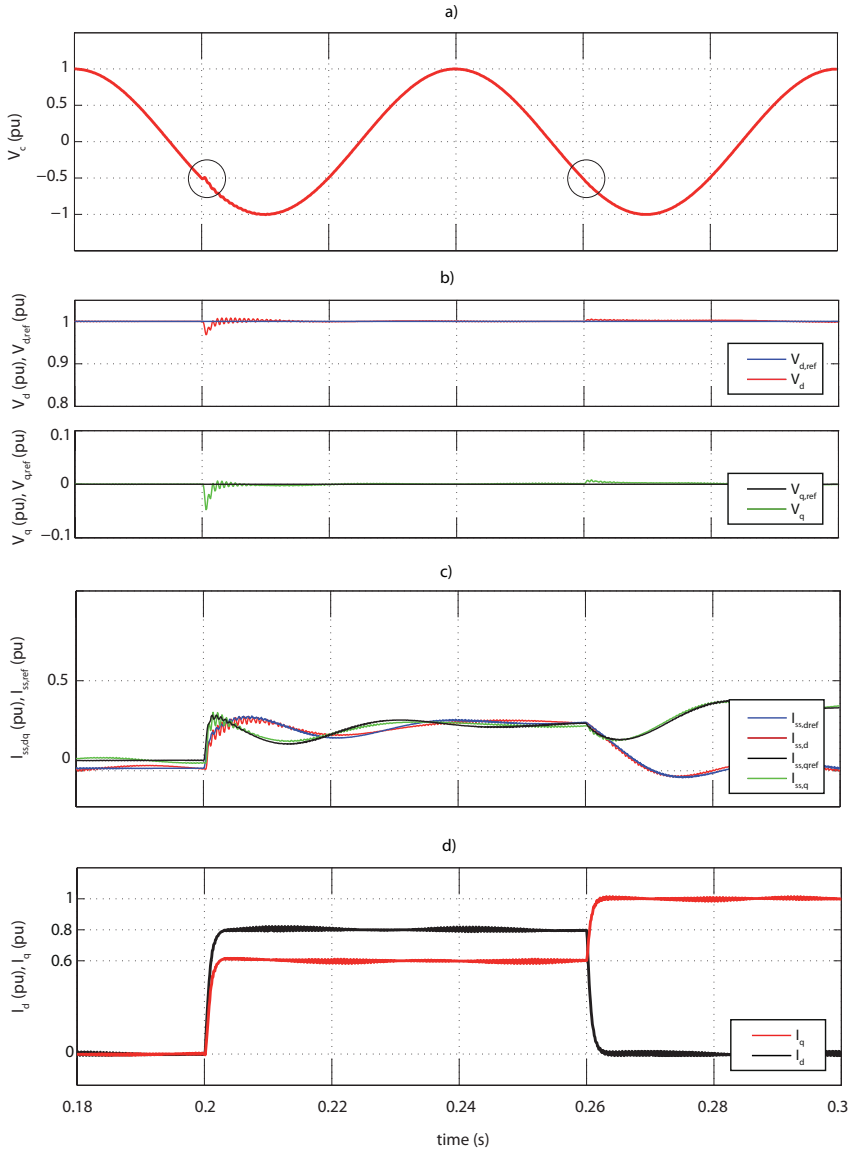

Figure B.7: Simulation results using the sensed load current feedforward approach: (a) Output voltage (b) Output voltage and reference voltage in d and q-axis (c) Substation d and q-axis currents (d) d and q-axis of train current steps applied to the system

Appendix C
Hybrid Synchronous/Stationary Voltage Control Strategy

C.1 Hybrid System Description

After analysing the stationary frame strategy and synchronous frame strategy separately a hybrid version is now considered. The idea is to demonstrate if using a Multivarible-PI controller in DQ frame for current control combined with P+Resonant controller in stationary frame for voltage control better dynamics are obtained. For this purpose, a SOGI and a stationary-to-synchronous transformation is used to obtain the dq components of the reference currents that feed the DQ current controller.

Controller Design: In this hybrid system, the method for calculating the controller with the especified dynamics consists on transforming the DQ Current Controller into the equivalent P+Resonant in stationary frame. Then, the open loop and closed loop transfer functions are developped with both controllers in the same reference frame. The equivalent P+Resonant controller is found [15]:

$$G_{PReq}(s) = k_p + \frac{k_i}{s} \Longrightarrow G_{PReq}(s) = k_p + \frac{2k_i s}{s^2 + \omega_o^2} \tag{C.1}$$

Now, both controllers follow a P+Resonant structure, so the procedure to calculate the parameters of the controller is similar to that described in Section 3.4.2 considering this time an equivalent PR ideal controller for current loop.

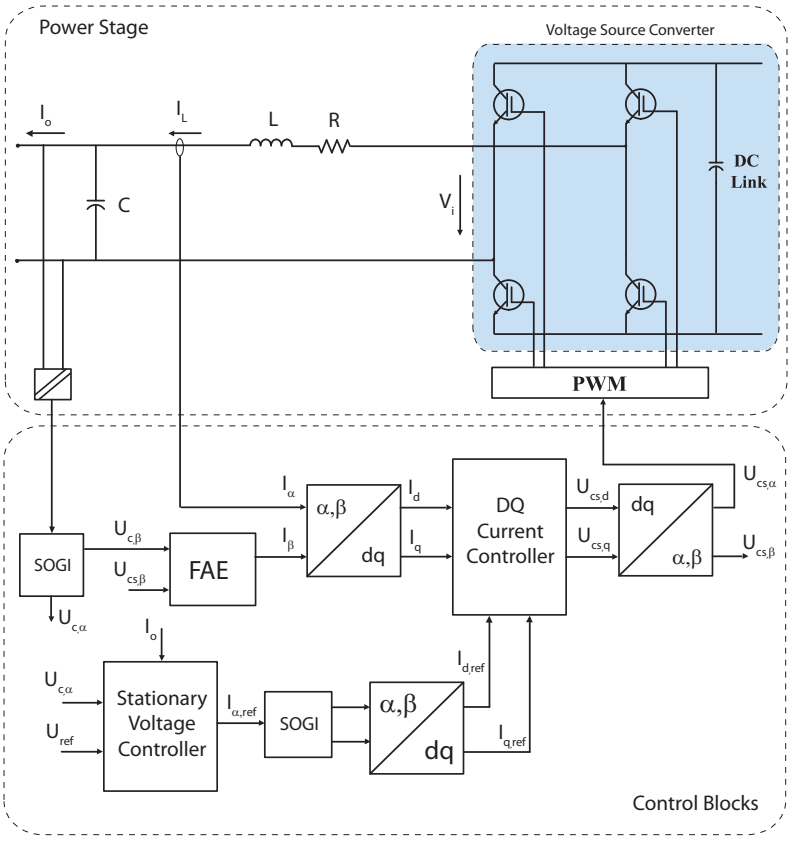

Figure C.1: Test system with the Hybrid Synchronous/Stationary Voltage Control Strategy

C.2 Performance Evaluation

The simulation results for this hybrid configuration are shown in Figure C.2. The voltage controller is capable to track the voltage reference with a transient response of 4 ms and zero steady-state error. The error peak in terms of voltage is at 6,7% of nominal voltage.

The results are quite similar to the ones obtained with the stationary frame control strategy and the same happens with the full DQ version. This could be expected because the performance of the P+R controllers in stationary reference frame is the dual of the performance of PI controllers working in synchronous reference frame.

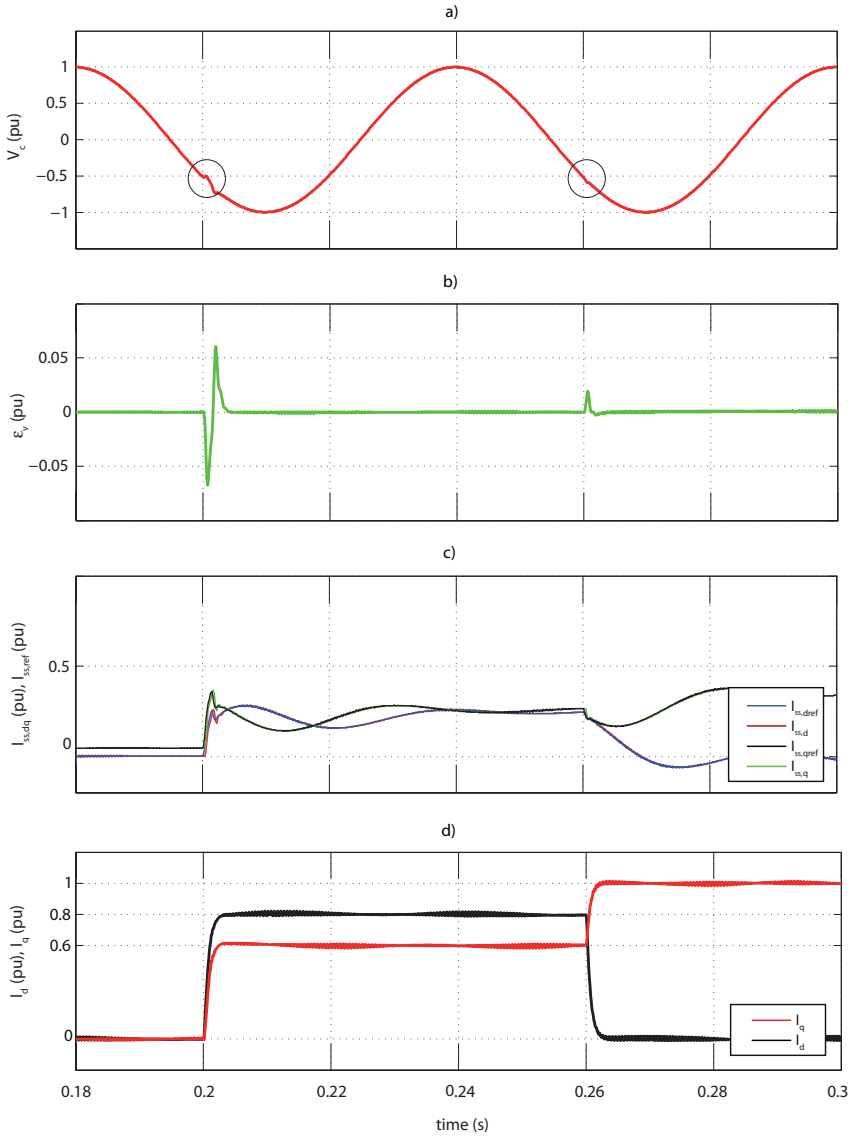

Figure C.2: Simulation results using the sensed load current feedforward approach: (a) Output voltage (b) Voltage error (c) Substation d and q-axis currents (d) d and q-axis of train current steps applied to the system