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Design and Implementation of an Envelope Tracking Power Amplifier Using Switched Amplifiers and Slow Envelopes

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To my beloved family and my adored girl

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Abstract

This master thesis presents the design and implementation of an Envelope Tracking (ET) transmitter including an envelope amplifier based on switched power amplifiers and algorithms for slew-rate and bandwidth reduction. The ET transmitter here presented constitutes a research environment that will allow investigate possible solutions to solve the linearity-efficiency trade-off of the power amplifiers. The design and implementation of the envelope amplifier includes commercial switching devices driven by pulsed signals generated by a Field Programmable Gate Array (FPGA). The pulsed signals are modulated using Pulse Width Modulation (PWM) and Delta-Sigma Modulation ($\Delta-\Sigma$ M) aimed to achieve a high efficient amplification. The signals, amplitudes, modulation frequencies and bandwidths used during the design and implementation are compatible with current communications standards.

This master thesis also presents a new algorithm for reduction of the envelope bandwidth as well as improvements over the existing slew-rate reduction algorithm presented in [1]. These improvements were implemented in the FPGA and validated in the implemented transmitter.

Results show that switching amplification is limited by the availability of current technologies in this field and the algorithms for reducing slew rate and bandwidth of the envelope are suitable to overcome this limitation while new technologies allow higher switching frequencies.

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Abbrevations and notations

Δ-Σ M	Delta-Sigma Modulation
ADC	Analog to Digital Converter
DAC	Digital to Analog Converter
DPD	Digital Pre-Distortion
DSP	Digital Signal Processor
DVB-H	Digital Video Broadcasting Handheld
DVB-T	Digital Video Broadcasting – Terrestrial
EA	Envelope Amplifier
EDGE	Enhanced Data Rates for GSM Evolution
EER	Envelope Elimination and Restoration
ET	Envelope Tracking
FPGA	Field Programmable Gate Array
GSM	Global System for Mobile Communications
HSDPA	High Speed Downlink Packet Access

IF Inter-medium Frequency

IF Intermediate Frequency

LED Light-Emitting Diode

LO Local Oscillator

LO local oscillator

LTE Long Term Evolution

OFDM Orthogonal Frequency Division Multiplexing

PAPR Peak to Average Power Ratio

PWM Pulse Width Modulation

RF Radio Frequency

RF Radio Frequency

RFPA Power Amplifier

SPA Switched Power Amplifier

SPA Switched Power Amplifier

WCDMA FDD Wideband Code Division Multiple Access - Frequency Division Duplex

WIMAX Worldwide Interoperability for Microwave Access

Chapter 1

Introduction

The necessity for high speed data rates and high spectral efficiency in communications technologies is pushing new communications standards to use linear modulations schemes like band-limited BPSK, QPSK, and multilevel QAM in combination with techniques as Orthogonal Frequency Division Multiplexing (OFDM). On the one hand, OFDM offers high data transmission rate (several Mega bauds) and is robust on multipath scenarios. However, as a counterpart for its transmission, the modulated radio signal exhibits rapid envelope variations.

	Standard	Launch year	Typical carrier BW (MHz)	Typical spectral efficiency (bit/sec/Hz)	Approximated PAPR (dB)
2G cellular	GSM	1991	0.2	0.17	0.0
Digital TV	DVB-H	2007	8.0	0.28	8.0
2.75G cellular	EDGE	2003	0.2	0.33	3.5
3G cellular	WCDMA FDD	2001	5.0	0.51	7.0
Digital TV	DVB-T	1997	8.0	0.55	8.0
Wi-Fi	IEEE 802.11 a/g	2003	20	0.90	9.0
WIMAX	IEEE 802.16d	2004	20	1.20	8.5
Wi-Fi	IEEE 802.11n	2007	20	2.40	9.0
3.5G cellular	HSDPA	2007	5.0	2.88	8.0
3.9G cellular	LTE	2009	20	8.00	10.0

Table 1.1: Comparison of the modulation characteristics and bandwidths of typical mobile wireless transmitters and communications standards [2]

These envelope variations produce an average value lower than its peak value. Having in mind that this signal goes through the power amplifier (PA), this implies an average output power lower than its maximum peak output power. The ratio between this two is known as the Peak to Average Power Ratio (PAPR), and as Table 1.1 shows,

for newer communications standards their PAPR values are becoming higher, in fact, the better the spectral efficiency is the higher the PAPR is.

1.1 Linearity-efficiency problem for PA in current communication standards

When a linear PA -class A, AB, B- is used to amplify the radio signal, high PAPRs values force to operate the PA at high back-off levels to avoid distortions on the linear modulations. Such approach implies a poor efficient amplification, since the PA amplifies a signal below the maximum possible and therefore, spends more time operating below its maximum efficiency. The non-used energy on the amplification is dissipated as heat reducing the life time of the battery, in the case of mobile devices, and increasing the costs due to the additional cooling system that is required, in the case of base stations.

On the other hand, a high efficient amplification could be achieved using switched PA (SPA) (Class C, D, E, F). In this case, it is possible to reach (theoretically) 100% efficiency. However, switched amplification is highly non-linear and therefore, matter of concern because the newer generation standards use linear modulations schemes that should be linearly amplified. In this way arises a trade-off between efficiency and linear amplification. It could be achieved either a highly linear amplification with poor efficiency or a high efficient amplification with non-linear distortions.

The linearity-efficiency problem has been widely studied on the literature. Given the fact that SPAs are highly efficient, but non-linear, some structures try to take advantage of this, creating configurations to achieve a linear amplification. This is the case of architectures like *Linear Amplification Using Non-Linear Components* (LINC) [3], *Combined Analog Locked Loop Universal Modulator* (CALLUM) [4], and *Envelope Elimination and Restoration* (EER) [5]. On the other hand, other architectures use linear power amplifiers under specific configurations in order to achieve a high efficient amplification, this is the case of architectures like *Envelope Tracking* (ET) [6] and all those architectures based on dynamic supply. However, it is important to mention that the power amplifier architectures are not limited to use purely linear, or non-linear amplifiers, instead, there exist others that use both types of amplifiers to achieve a high efficient and linear amplification. These architectures include the *Doherty Power Amplifier* (DPA) which is widely deployed in current radio-base stations working in L-S-C bands with time varying envelope signals as WiMax, WLAN, etc. Using the DPA drain efficiencies up to 70% have been reported for output powers between 5 W

and 10 W [7, 8, 9, 10], whereas the efficiency achieves values around 50% for 250 W [11].

From the above mentioned architectures EER and ET are two promising amplifiers for the newer generation radio signals [12, 13]. Omitting the fact that these architectures use different PA classes, both architectures use dynamic power supply to achieve a high efficient amplification. However, both amplifiers share a common drawback as well: They require an envelope amplifier (EA), capable to provide high efficiency and linearity in a wide bandwidth in order to be able to follow accurately the rapid envelope changes. Such task becomes even more complex when dealing with high PAPR signals, where the envelope bandwidth extends, theoretically, throughout the spectrum (in practice between 5 and 7 times the bandwidth of the base-band complex modulated signal) [14, 15]. However, recently an approach based on the slew-rate limitation [1] and bandwidth reduction [16] of the envelope have been proposed to overcome this problem, moreover, this technique has shown promising results [17, 18, 19].

1.2 Contributions of this master thesis

Despite of the results presented in the literature using bandwidth and slew-rate reduction algorithms [17, 18, 19], there is not yet a transmitter implementing these techniques in combination with switched amplification. Furthermore, the method for bandwidth reduction proposed in [16] has the main drawback to be an iterative algorithm and therefore, it is not a real time implementable technique. On the other hand, the method of slew-rate limitation proposed in [1] is a real-time algorithm, but the resulting signal does not have a clear spectral limitation, which may cause problems when highly-efficient switched techniques are used.

This master thesis presents the design and implementation of an ET transmitter including an envelope amplifier based on switched amplification and algorithms for slew-rate and bandwidth reduction of the amplified envelope. The transmitter presented in this master thesis constitutes a research environment that will allow investigate possible solutions to solve the linearity-efficiency trade-off of the power amplifiers. The design and implementation of the EA includes commercial switching devices driven by pulsed signals generated by a Field Programmable Gate Array (FPGA) and modulated using Pulse Width Modulation (PWM) and Delta-Sigma Modulation ($\Delta - \Sigma$ M) to achieve an efficient amplification. The signals, amplitudes, modulation frequencies and bandwidths are compatible with current communications standards.

This master thesis also presents a new algorithm for reduction of the envelope bandwidth as well as improvements over the slew-rate reduction algorithm presented in [1]. These improvements were implemented in a FPGA and validated in the implemented transmitter.

1.3 Organization of this master thesis

In addition to this chapter, this master thesis includes the following content:

Chapter 2 includes the state-of-the-art of power amplification architectures for wireless communications. Here, a detailed explanation of the treated power amplifier architecture as well as its problems and limitations is presented. This chapter provides the required theoretical background necessary to understand the development of this project.

Chapter 3 gives a full description of the design and implementation of all the parts that comprises the envelope tracking transmitter. This chapter starts giving a list of the requirements to fulfill, and continues with the description of the existing problems at each stage of the design. Simulations, partial results and proposed solutions to overcome the difficulties are fully described for independent parts of the ET transmitter.

Chapter 4 presents the final design of the transmitter. Further tests and limitations are presented before to integrate all the parts that comprises the ET. This chapter concludes presenting the final implementation and some results that show the reliability of the design.

Chapter 5 includes the findings and the conclusions extracted from the development of this project, as well as possible improvements and further work.

Appendices include a description of tools used during the development of this project and some simulations results.

Chapter 2

State of the Art of Power Amplification Strategies for Wireless Communications

2.1 Power amplifiers

In general, a power amplifier (PA) is defined as a device that increases the power of an arbitrary input signal. The added power is exhibited at the output signal and is taken from a DC-input power. PA are classified depending on the architecture used to perform the amplification. Moreover, each of these configurations led to different outputs waveforms and efficiencies.

The classification of the existing PA architectures is referred in the literature as *classes*, existing class A,B,C,D,E and F [20]. All these classes, except the class A, employ various nonlinear, switching, and wave-shaping techniques in order to provide a linear and efficient amplification. However, not all these classes provide a linear amplification, allowing their classification in two main groups namely, the linear amplifiers and the non-liner amplifiers. Besides, the PA are also classified depending on the conduction angle, making reference to the angle when the amplifier starts to work if a sinusoid is considered at its input.

2.1.1 Linear amplifiers

The linear amplifiers include the classes A and B, although some authors also include the class AB as an intermedium class between classes A and B [21]. These configurations are considered linear because the phase and the amplitude of the output signal

is linearly related with the amplitude and phase of the input signal. In the following, a brief description of these topologies is addressed.

Class A

The general class A amplifier is shown in Figure 2.1. In the class A topology the amplifier remains biased in the active region during all normal operating conditions. This condition implies that the device is always ready to amplify the input signal but also that the nominal bias current is nonzero, therefore, there is always some power dissipation in the device.

The configuration showed in Figure 2.1 reaches a maximum theoretical efficiency of 25 % for an ideal PA, however in RF configuration the resistor R_L is replaced by an inductor, rising its theoretical efficiency up to 50 %. The low efficiency of the class A amplifier is mainly due to its never-zero I-V product during its operation, in fact, the lowest efficiency is reached when there is no signal in the input port, in which case all the power is dissipated in the device.

Despite its low efficiency, the class A power amplifier behaves as an ideal power amplifier regarding its input/output relation. Since the transistor is all the time in the active region, the amplification of the signal is performed over an specific load line which design is relative linear to minimize distortion between the input and the output.

Due to the high linearity of this class of amplifier and its low efficiency this amplifiers is widely used in applications requiring low power, high linearity and where the efficiency is not critical.

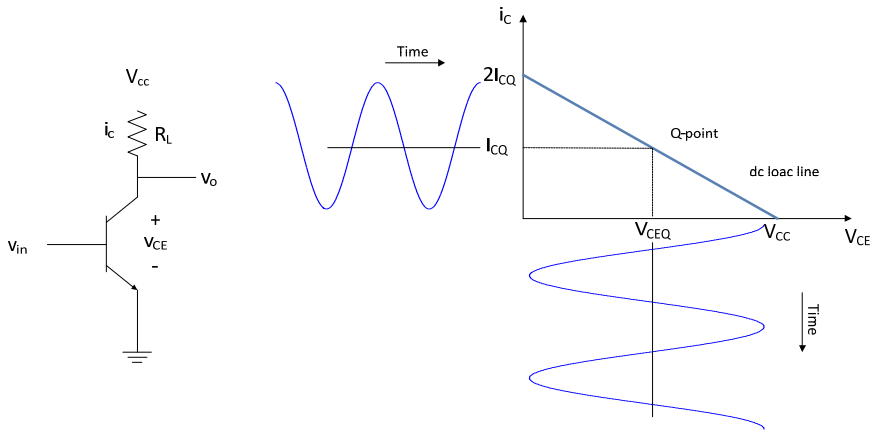


Figure 2.1: Class A amplifier

Class B

In the class B architecture the power amplifier is not in the active region when the input signal is zero. This sets its quiescent current to zero and there is no power dissipation in absence of input. The amplifier enters in the active region when the input signal crosses the conduction threshold. As result, the amplification is linear just after crossing the threshold.

The classical class B amplifier is an emitter-follower (actually this is the most used configuration on RF applications), however, it is also used in a push-pull configuration as Figure 2.2 shows. By using this configuration when the input signal has both positive and negative values, it is possible the amplification of both semi-cycles.

The instantaneous efficiency changes with the output voltage and reaches a maximum theoretical value of 78.5 % for an ideal PA. This efficiency is considerably greater than the exhibited by the class A amplifier, however the main drawback of this architecture is the crossover distortion caused by the non-conduction region as Figure 2.2 shows.

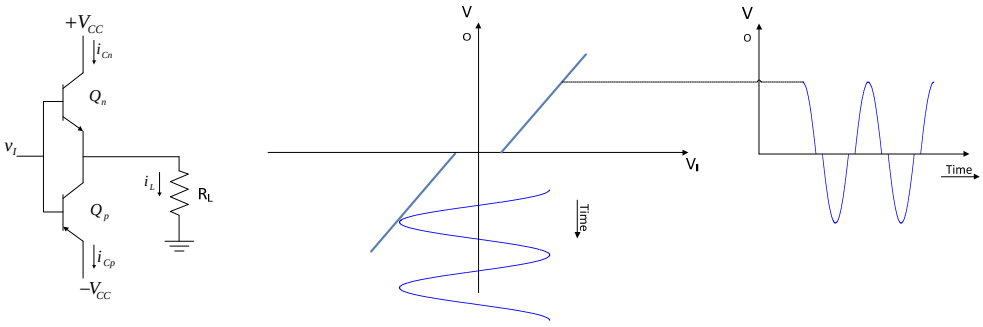


Figure 2.2: Class B amplifier

Class AB

The class AB attempts to solve the distortion of the crossover region that the class B amplifier exhibits. The crossover distortion is virtually suppressed establishing the biasing of the PA right at the threshold of its operation. As in the case of the class B, this architecture is used either as a emitter-follower or in a push-pull configuration (see Figure 2.3) ,to allow amplification of signals with positive and negative values. Nevertheless, it has to be pointed out that distortion can still occur produced by disparities between the amplifiers.

The class AB reaches efficiency values between 50 % and 78 % and is used in audio as well as applications of low, medium, high and very high frequencies [22] when variations are introduced over its classical configuration.

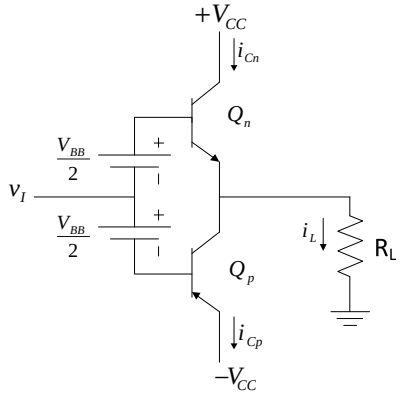


Figure 2.3: Class AB amplifier

2.1.2 Non-linear amplifiers

In those applications where the linearity is not critical and the efficiency is the main concern, the non-linear amplifiers are widely used. In contrast to the linear amplifiers, the non-linear amplifiers don not exhibit a linear relation between the phase and amplitude of the input and output. The non-linear amplifiers includes the class C, D, E and F; in the following, a brief description of this amplifiers is addressed.

Class C

In class C the amplifier is biased and controlled by a conduction angle which is set such that the amplifier is active for less than half of the waveform described by a sinusoid. However, the load of the amplifier should be tuned to provide a full cycle of output signal for the fundamental, or resonant frequency. The use of this amplifiers is, therefore, limited for a fixed frequency and produces the lost of the linearity in the amplification process. Nevertheless, its theoretical efficiency tends to 100 % when the conduction angle tends to zero. Unfortunately, 100 % efficiency is physically unreachable by the amplifier and a typical compromise lead to efficies around 85 %

Class D

This class of amplifier employs at least two active elements whose operate as switches to create a square signal at the output. The generated signal is then low pass filtered passing the first harmonic to the load. As the current is driven just by the switched-on active element, then the theoretical efficiency is 100 % for an ideal PA. Nevertheless, due to losses associated to saturation, switching speed and junction capacitances, the practical efficiency is less than 100 % and is inversely proportional to the switching frequency.

The class D amplifier is widely used in audio applications where efficiencies of more than 90% have been reported for output powers around 10 W [23]. However due to the degradation of its efficiency when the swhitching frequency increases this topology is not used in high frequency applications.

Class E

In the class E amplifier the active device is used as a switch. Its configuration includes an RF-choke inductor used as a pull up device and operates as a current source. The goal in this class of amplifiers is to design the load network to reduce the I-V product over the active device allowing the efficiency of an ideal amplifier approach to 100 %.

Class F

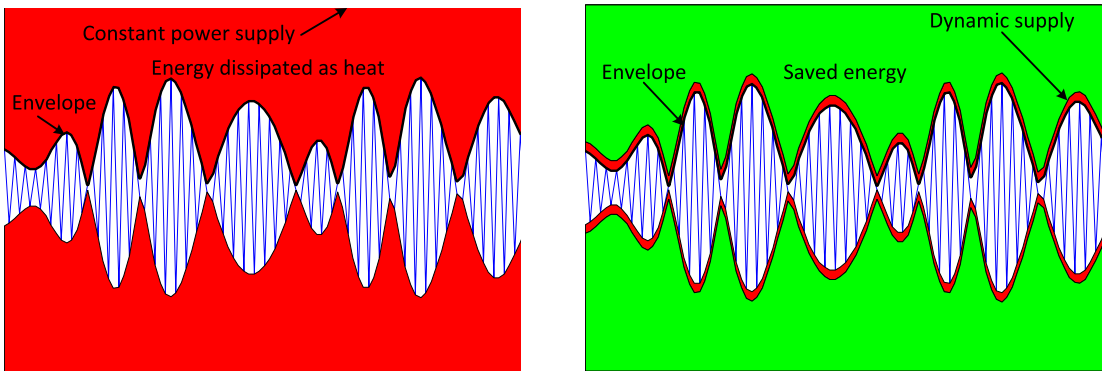
Class F amplifiers are also based on the tuning of its load to reduce the I-V product over the active device. In this class of amplifier a resonator is used to block some, or all, the odd harmonics of the output current. By doing this, a square wave voltage out-of-phase with the current is created at the output. The voltage output exhibits a square waveform as well as the current. Therefore, (ideally) the device switch its state yielding a zero I-V product and so reaching 100% ideal efficiency.

2.2 Dynamic supply for high efficient RF amplification

In wireless communications a high efficient amplification directly implies an efficient use of batteries, in the case of mobile devices, and less energy consumption, in the cases of

fixed radio bases. On the other hand, the transmitted signals of newer communications standards are exhibiting higher PAPR as Table 1.1 shows. Moreover, the new standards are using linear modulations in the transmitted signals, making these signals very susceptible to non-linear distortions.

With linearity and efficiency being crucial aspects in newer communications standards, using the classical high efficient amplifiers presented in the previous section is not a viable solution becasue the linearity is completely lost. Regarding the linear amplifiers, they fulfill the linearity requirement but its efficiency is poor. Moreover, in the presented linear amplifiers the efficiency is reduced even more when the amplified signal exhibits high PAPR. As Figure 2.4a shows, when linear amplifiers are used to amplify signals below its maximum output voltage, the energy that was not used on amplification is wasted as heat. A suitable solution to overcome this problem is to use an amplifier whose voltage supply is dynamically adjusted depending on the required output voltage. This approach is illustrated in Figure 2.4b and is know in the literature as "dynamical supply". By implementing this approach, it is saved most of the energy previously wasted as heat, increasing the total efficiency of the radio transmitter in about 20 %-30 % [24].



(a) Static power supply (b) Dynamic power supply

Figure 2.4: Static and dynamic power supply

Two of the more promising amplifier architectures for the newer generation radio signals implementing the dynamic supply are the Envelope Tracking (ET) and the Envelope Elimination and Restoration (EER) architectures [12, 13]. These two architectures try to achieve a linear and efficient amplification by using different PA classes, nevertheless, these architecture face problems in their implementation that are worth of mention.

2.2.1 Envelope Elimination and Restoration (EER)

The EER technique was one of the first architectures implementing the separation of the amplitude and phase information. This technique is also known as Khan technique, making reference to L. R. Khan who introduced this concept for the first time in 1952 [5]. Originally this architecture was developed to solve the problem of high cost and low efficiency in single-sideband transmitters where typically a series of cascaded linear PA were required.

Figure 2.5 shows the block diagram of the EER architecture. It is basically composed by two paths, namely the amplitude and the Radio Frequency (RF) paths. In the first one, a limiter is used to obtain the zero-crossing of the RF signal. By doing this, the envelope of the signal is removed while the phase information is preserved. This turns the PA input into a constant envelope signal, allowing a high-efficient amplification using a Switched Power Amplifier (SPA) (Class C,D,E,F). On the other hand, in the amplitude path the envelope of the RF signal is extracted using an envelope detector. This envelope is then amplified proportionally to the RF output using an Envelope Amplifier (EA). As final step, the amplitude information dynamically supplies the RFPA voltage, "restoring" the amplitude information. Examples of classic EER systems can be found in [25, 26, 27].

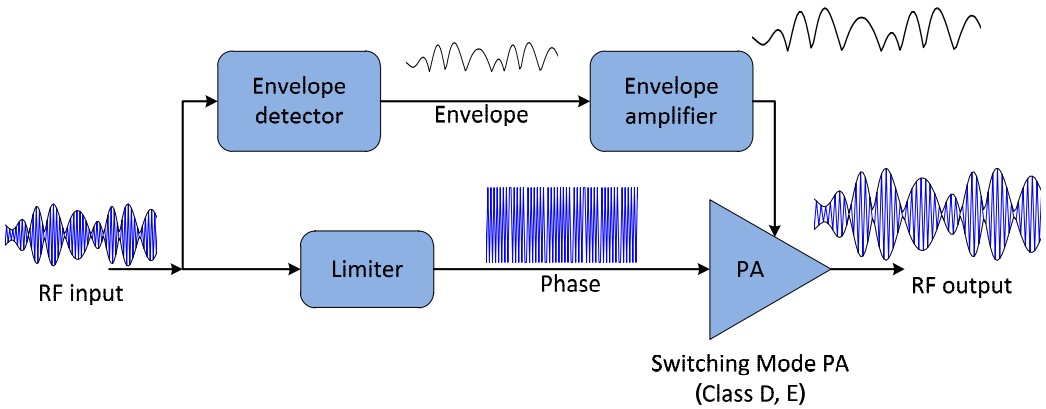


Figure 2.5: Envelope Elimination and Restoration (EER) transmitter architecture

In modern EER, usually a Digital Signal Processor (DSP) is used to generate the envelope and the I-Q components [28, 13, 19] as Figure 2.6 shows. The phase information is obtained modulating to RF the scaled I-Q components. Such configuration avoids the use of an envelope detector and makes easier the adjustment of possible misalignment between the two paths. Nevertheless, in this case the EER becomes a misnomer because there is not elimination of the envelope. However, the name is still in use [2, 29], although some authors call this configuration polar transmitter [30, 31, 32].

Anyhow, despite the misnomer, in general the term EER is referred to any system where the phase-modulated RF signal is amplified through a nonlinear amplifier and the envelope signal is used to modulate and amplify the phase-modulated RF signal whereas polar transmitter refers to all those architectures where amplitude and phase information are used in the amplification process.

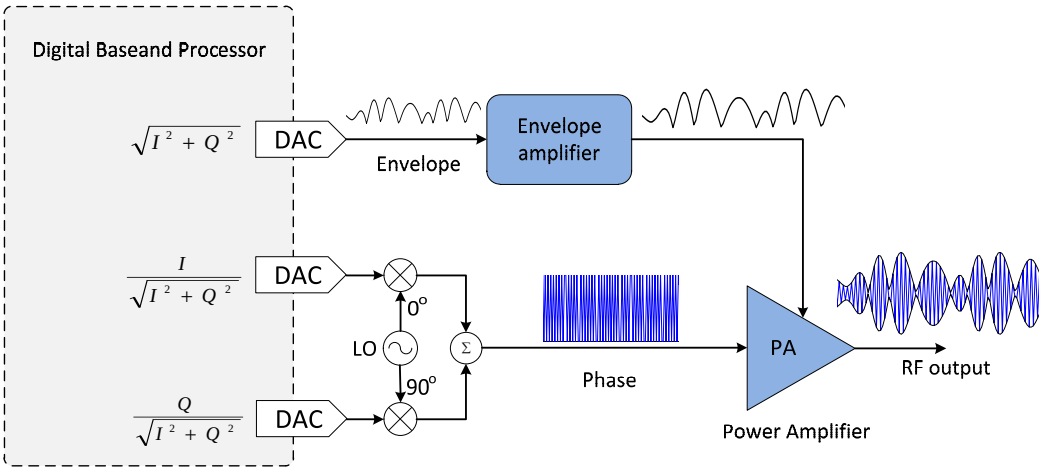


Figure 2.6: Polar transmitter architecture

2.2.1.1 Issues and drawbacks

Delay mismatch

Of crucial importance in this architecture is the synchronization between the input RF signal and the supply voltage of the RFPA. As shown in Figure 2.5 and Figure 2.6 this architecture performs the product of the envelope and phase inside the PA, therefore, these signals should be properly aligned, otherwise it will imply a miss correspondence between amplitude and phase for each transmitted symbol, which will be exhibited as non-linear distortion at the output that cannot be corrected even using Digital Pre-Distortion (DPD).

Simulations presented in [14] indicate that synchronization accuracy around ±20 ns is required for every 1 MHz of RF bandwidth to meet linearity requirements. However, despite of the importance of the alignment, nowadays delay mismatch is not a mayor issue due to the wide use of FPGAs and DSP on the transmitter architectures [28, 13, 19]. These processors facilitate the correction of temporal misalignment in the generated data.

Bandwidth expansion and linear amplification

The definition of constellation as well as the transmission of the signals is usually done in terms of Cartesian coordinates. However, any signal could be represented using either Cartesian or polar coordinates. The Cartesian representation is shown in equation 2.1, where $I(t)$ represents the In-phase component, $Q(t)$ represents the In-quadrature component and ω_c represents the carrier frequency. On the other hand, the polar representation is shown in equation 2.2, where $A(t)$ represents the amplitude, or envelope, of the signal, $\phi(t)$ represents the phase and ω_c the carrier frequency.

$$s(t) = I(t)sin(\omega_c t) - Q(t)cos(\omega_c t) \tag{2.1}$$

$$s(t) = A(t)cos(\omega_c t + \phi(t)) \tag{2.2}$$

The relation between equations 2.1 and 2.2 is ruled by:

$$A(t) = \sqrt{I(t)^2 + Q(t)^2} \tag{2.3}$$

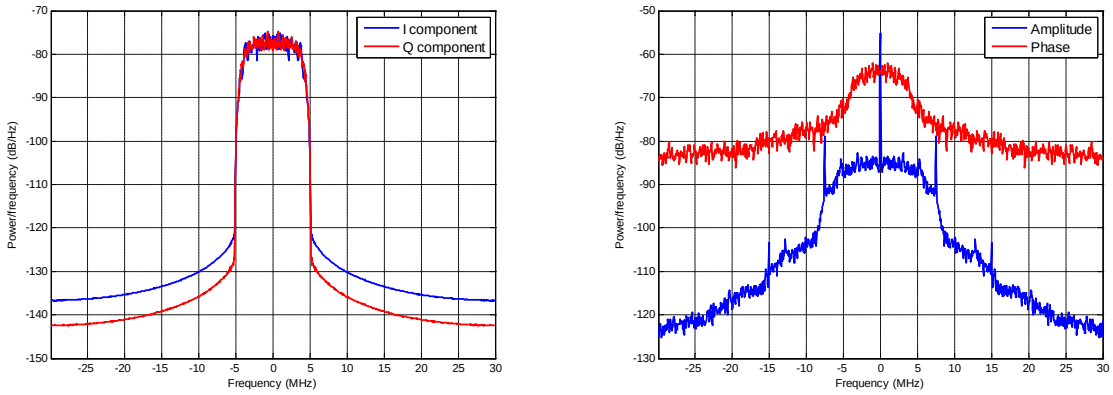
$$\phi(t) = tan^{-1}\left(\frac{Q(t)}{I(t)}\right) \tag{2.4}$$

As can be appreciated from equations (2.1) and (2.2), the relation between the polar and Cartesian representations is not linear. In fact, when a transformation from Cartesian to Polar is performed, the non-linear relationship between them causes the polar vectors to lose the band-limited property held on the Cartesian representation. That is, after a Cartesian to polar conversion, the bandwidths of the envelope and phase signals are different, actually wider, than the corresponding bandwidths of I and Q signals.

This phenomena is termed "bandwidth expansion" and turns out to be theoretically infinite, i.e. the bandwidth expansion is extended theoretically throughout the spectrum. For example, consider a two tone signal with carrier frequency ω_c and modulation frequency ω_m. The RF signal has a defined and finite bandwidth around ω_m, but its envelope contains frequency components at dc, $2\omega_m$, $4\omega_m$, $6\omega_m$, $8\omega_m$, ... etc. However, in practical implementations the bandwidth is considered at least 5 to 6

times larger than the Cartesian bandwidth signal [14, 15] in order to avoid significant distortion at the output. In general, it could be stated that such bandwidth truncation is restricted by the maximum allowed distortion at the final output.

To illustrate the bandwidth expansion phenomenon in a practical case, consider the 16-QAM signal in Cartesian representation exhibiting a 5 MHz bandwidth. Such signal is represented on the left side in Figure 2.7a, notice that such Cartesian representation have a clear and well defined bandwidth spectrum. On the right side, in Figure 2.7b is shown the equivalent polar representation. Notice that the resulting amplitude (in blue) and phase (in red) signals do not have a well defined bandwidth spectrum any longer. Moreover, the spectrum is wider and, as mentioned before, a good approximation could be considering a bandwidth expansion about 5-6 times the original bandwidth, i.e. around 25 MHz.



(a) I-Q components

(b) Phase and amplitude components

Figure 2.7: Bandwidth expansion phenomenon for a 16-QAM signal

The distortion caused over the output signal occurs because the information originally contained on the I-Q signals is now split into two other signals, namely the envelope and the phase. These signals should be completely preserved in order to avoid any loss of information, because such losses imply distortion at the output.

In those cases where the envelope and phase signals are directly synthesized by digital processors (Figure 2.6), the bandwidth expansion could represent an issue due to the necessity to sample the signal at least twice its bandwidth (in order to hold the Nyquist criteria). However the developments achieved in DACs and digital processing allow to overcome this difficulty.

On the other hand, the main problem caused by the bandwidth expansion is in the implementation of dynamic power supply because the information of the amplitude is used in this process. Therefore, the envelope amplifier should provide a fast enough

dynamic response. Such requirement is not easy to fulfill, and the task becomes even harder when the efficiency is considered.

DC-DC converters satisfying the bandwidth, output power, linearity and efficiency requirements are still matter of study. Current solutions achieve just hundreds of KHz with output power in the order of mW or several tens of watts in the best cases [26]

2.2.2 Envelope Tracking (ET)

A block diagram of the ET architecture is shown in Figure 2.8. This architecture is usually included in the group of polar architectures. However, strictly speaking, the ET does not belong to this group because the RFPA input signals are not the phase and amplitude. Instead, its inputs are the RF signal and the envelope of the signal used to dynamically supply the voltage to the RFPA.

As Figure 2.8 shows, the RFPA input signal is non-constant. This forces to use a linear PA (Class A, B, AB) in order to avoid distortion on the linear modulated signal. Given the fact that linear PA are not highly efficient, this architecture attempts to achieve a high efficient amplifications relying on the dynamic power supply. The maximum power saving occurs when the supply is adjusted to the minimum level where the power amplifier is still linear. In some cases, the PA could even operates at weak compression.

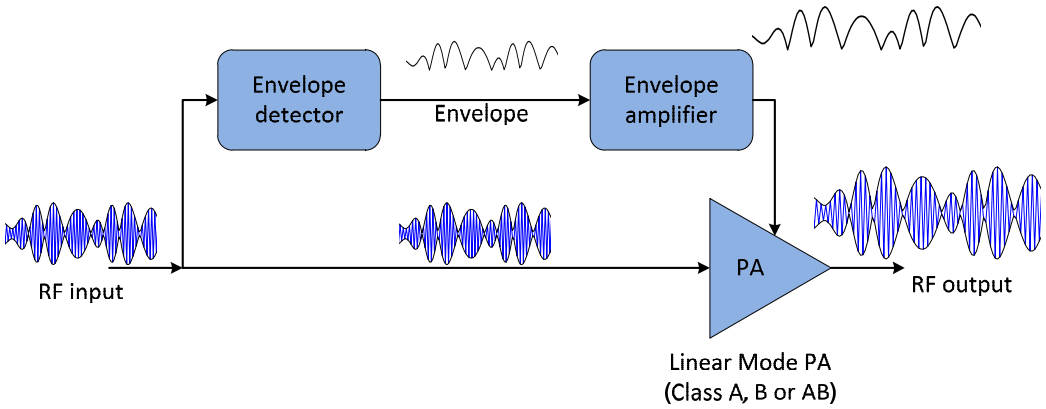


Figure 2.8: Envelope Tracking transmitter architecture

2.2.2.1 Issues and drawbacks

Since ET and EER use a similar signal processing, these architectures face common problems. However, tt is important to remark that the ET technique has been proposed to improve the efficiency of the linear PAs (Class A, B, AB, C) by adapting its power supply voltage. On the other hand, the EER technique is aimed to improve the efficiency by using a high-efficient non-linear PA that processes a constant envelope phase modulated signal. In any case, both techniques behave ideally like a highly-efficient linear PA.

Delay mismatch

Similar to the EER architecture, in the ET architecture the synchronization between the envelope and the RF input signal of the PA is important even when the product of the envelope and the phase is not performed inside the PA. The reason is because the PA should be kept away from the compression point. If there exist a misalignment such that the compression point is crossed, then it will occur linear distortion in all those points where the compression point is exceeded. However, if the RFPA never goes beyond the compression point there is no non-linear distortion, which makes the ET architecture more robust to delay mistmatch, compared with the EER architecture.

As also occurs in the EER architecture, nowadays delay mismatch is not a mayor issue due to the wide use of FPGAs and DSP on the transmitter architectures [28, 13, 19] which facilitate the correction of temporal misalignment in the generated data.

Dynamic supply voltage distortion

In the dynamic supply, the maximum power saving occurs when the supply voltage is adjusted to the minimum level where the PA is still linear, that is, as close as possible to the compression point. However, a constant adjustment of the power supply implies a repeatedly change on the PA bias conditions, or equivalently, a repeatedly change on its input/output relation because the load line is changed. Those changes on the PA's input/output relation, induces non-linear distortion in the output signal.

Fortunately, the distortion induced by the dynamic supply is not a major issue. The inclusion of feedback control loops combined with Digital Pre-Distortion (DPD) techniques allow to compensate the changes in order to achieve a linear amplification

[33, 34, 35, 36, 37].

Bandwidth expansion and linear amplification

This architecture shares the problem of DC-DC converters with the EER architecture: The bandwidth expansion resulting from the Cartesian to Polar conversion makes difficult to perform the amplification of the envelope efficiently and provide good linearity and high voltage outputs simultaneously. DC-DC converters satisfying these characteristics are still matter of study.

2.3 High efficient envelope amplification

The straightforward approach to amplify the envelope of in architectures like EER and ET is to use a linear regulator to adjust the supply voltage of the RFPA [38]. The use of linear regulator topology achieves wide bandwidth and good noise performance, nevertheless, as a counterpart, this solution brings down the efficiency achieved using dynamic supply.

Two of the main attempts to improve efficiency are the multilevel converter [39] (Class G modulator) and the buck converter (Class S modulator) [40].

2.3.1 Class G architecture

The approach of the class G is to use a linear amplifier provided with more than one power level supply. In order to reduce the power consumption, the class G is provided with two or more voltage supply power levels and switch between them as the output signal approaches to each one. That is, if the input signal remains at low levels, the power supply is adjusted to a level that allows linear amplification, reducing this way the power consumption. This approach is similar to use dynamic supply but it is adapted just to few discrete levels.

The main concern with this amplifier is the introduction of linear distortion during the conmmutation from one level to another. However, nowadays the class G amplifiers is firmly established in powered subwoofers, and current applications use this class in ADSL telephone-line drivers [41].

2.3.2 Class S amplifier

The class S architecture attempts to achieve high efficiency using switched amplifiers. The input signal is encoded using a modulation to turn the input signal into a pulsed signal. The pulsed signal is efficiently amplified using a switched amplifier and is later recovered using a passive filter at the output of the amplifier. Classical S architecture employs PWM or $\Delta - \Sigma$M to modulate the signal.

The theoretical efficiency of this architecture is 100 %, because the I-V product tends to zero in the device. However, there exist switching losses when the commutation between *on* and *off* states is performed, which means that its efficiency is reduced as the switching frequency increases.

The main drawback of the class S amplifier is the switching frequency necessary to amplify the input signal because this frequency should be several times the bandwidth of the signal to be amplified [42]. However, in practice the switching frequency goes up to five times the bandwidth of the input signal [24]. Such task becomes complex when this class of amplifier is used to amplify the envelope of the signal because this is, in general, a wide bandwidth signal, for example for a 4 MHz bandwidth signal in the Cartesian format, its envelope bandwidth has around 20 MHz, requiring at least a switching frequency of around 100 MHz.

Another matter of concern is the filter used at the output. This filter should be selective depending on the modulation used as well as provide a high attenuation in the rejecrted band in order to eliminate the switching noise. On the other hand, the introduction of a filter in the architecture induces a delay that should be taken into account for the alignment of the RFPA input signals.

DC-DC converters satisfying the bandwidth, output power and efficiency requirements are still matter of study. Current solutions achieve just hundreds of KHz with output power in the order of mW or several tens of watts in the best cases [26]. In the mean time, partial solutions like bandwidth and slew-rate envelope reduction [19, 17] have been proposed in the literature as an alternative to fulfill the mentioned requirements in bandwidth and output voltage.

2.4 Modulations for switched amplification

The procedure to perform switched amplification consists in first converting, or modulating, the signal to be processed into pulses. If a class S amplifier is considered, the pulses are amplified using a PA on switched mode and as final step the amplified output is filtered using a passive filter. The output of the filter is (ideally) an amplified version of the input signal.

Regarding the initial modulation necessary to amplify the signal, two of the more used modulation techniques are the Pulse Width Modulation (PWM) and the Delta Sigma modulation ($\Delta - \Sigma$M). Having in mind the final application, an envelope amplifier, these techniques presents advantages and drawbacks that will be shortly addressed.

2.4.1 Pulse Width Modulation (PWM)

Pulse width modulation is a well-known technique that has found applications on time division multiplexers [43, 44], radio frequency transmitters [20], optical data storage [45], control of AC–DC power converters, and the like. Moreover, there exists many variations regarding the output format and carrier used to modulate the input signal. However, the following explanation does not address all these possibilities, instead it is focused on the suitability of the PWM to develop an envelope amplifier. Further explanations and a deep analysis can be found in [46]

A block diagram of the PWM technique is shown in Figure (2.9). A carrier is generated and used as reference by a comparator to produce either a "high" or "low" output. As the graphic above the block diagram shows, the comparator yields a "high" output (in red) if the input signal (in blue) is above the carrier (in black), otherwise a "low" level is exhibited at the output. If an efficient switched amplification of the signal wants to be performed, it has to be done between the PWM output and the low pass filter. This sequence represents the basic modulation process behind the PWM, nevertheless as possible variations the carrier, here showed as a sawtooth signal, could be a triangular as well or any other variation of these two. Regarding the comparator output, there exist variations including three or more levels. Anyhow, each of these approaches yields a different spectrum output.

The PWM is a nonlinear process, in fact, once the demodulation is performed, the overall process results in distortion of the modulating (input) signal. That is, the

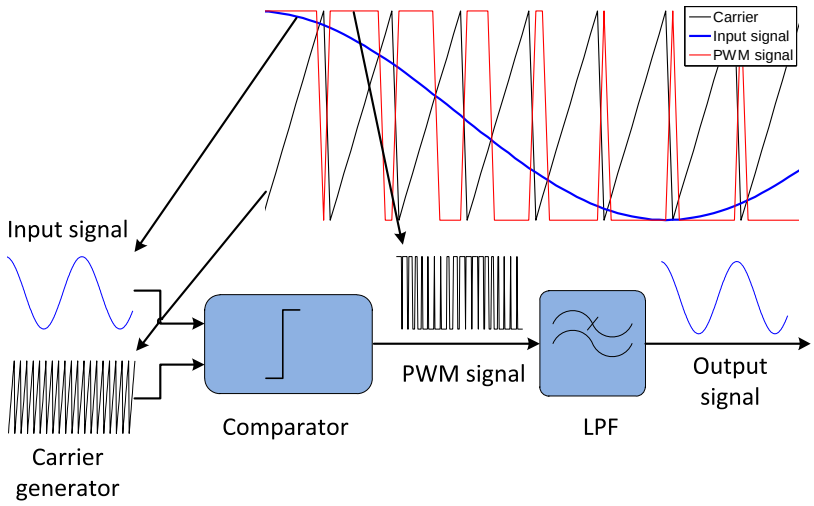


Figure 2.9: Pulse width modulator block diagram

output signal is never going to be the same like the input signal. A particular problem on the PWM is its inherent noise in the modulated signal, which spectrum resembles white noise.

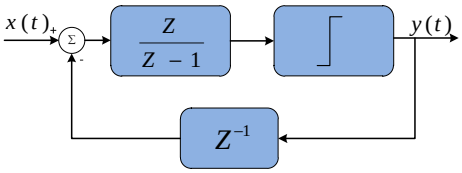
Regarding the spectrum of the modulated signal, it is important to point out that the higher the frequency of the carrier is the further is the first spectrum replica of the base band, and so a less selective filter is needed to recover the signal. Moreover, higher carrier frequencies yields better resolution in the modulated signal. This facts imposes the main limitation on applications where it is required to implement this architectures on a digital signal processor, because the sampling frequency is limited by the maximum clock speed of the processor. This limitation results in a trade-off between the resolution and the frequency of the carrier because increasing the number of points that conforms the carrier implies a reduction of its frequency. Not to mention the resolution losses associated to the number of bits to represent the signal.

The design of the filter require special attention because its response should be flat and the rejected band should has enough attenuation to remove the undesired noise introduced by the carrier replicas and the switching noise

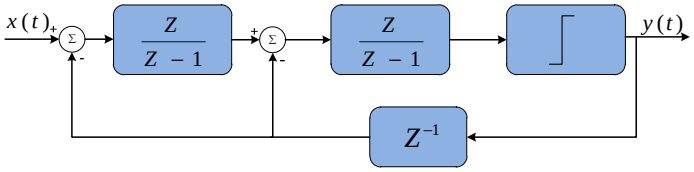
2.4.2 Delta Sigma Modulation ($\Delta - \Sigma$)

This modulation technique is very popular in audio applications and Digital to Analog Converters (DAC) and Analog to Digital Converters (ADC). Different to PWM where the switching noise spectrum resembles white noise, the delta sigma modulator distributes the quantization error, or noise, such that it is very low in the band of inter-

est. This characteristic is partially introduced by the oversampling principle which is the act of sampling the input signal at a frequency higher than the Nyquist frequency (twice the input signal bandwidth).



(a) First-order delta-sigma modulator block diagram



(b) Second-order delta-sigma modulator block diagram

Figure 2.10: First and second order delta-sigma modulators block diagram

Figure 2.10 shows the block diagram of a first order Delta-Sigma modulator. The input signal enters in the system via a summing junction. Then the signal goes through an integrator which feeds a comparator that performs the one-bit quantization. The output of the comparator is then fed back to the input summing junction, and is also the resulting output. Including more integrators in the structure changes the noise shaping of the modulator. Figure 2.10b shows a second order Delta-Sigma modulator. Higher order are also possible but not always stable as the first and second order showed in the above figures.

An analysis of the frequency response of the modulator lead to the noise shape showed in Figure 2.11. As can be observed in this figure, the quantization noise is high pass filtered, pushing it towards the sampling frequency. Increasing the order of modulator increases the order of this filtering effect.

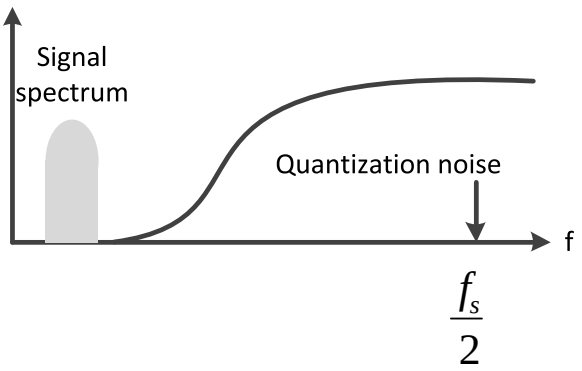


Figure 2.11: Noise shaping on a delta-sigma modulator

The characteristic noise shaping exhibited by the Delta-Sigma modulator allows to relax the order of the filter used in the demodulation comparing with the required in the PWM. Moreover, other Delta-Sigma configurations allow to modulate signals, not just in base-band but also at other frequencies.

2.5 Digital Pre-Distortion (DPD)

The basic idea of Pre-distortion is to build a correction module that compensates the non-linearity of the power amplifier, in this sense, a pre-distorter tries to invert the nonlinear function of the PA such that, the cascade responses of both PA and pre-distorter results in a linear response as Figure 2.12 illustrates.

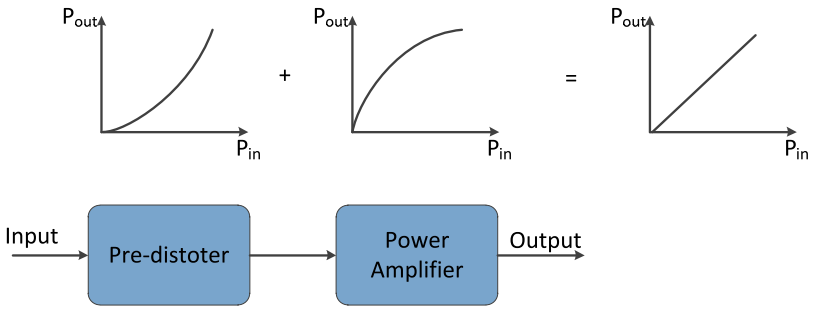


Figure 2.12: Pre-distortion concept block-diagram

The procedure to include a pre-distorter comprise modeling the power amplifier by taking samples of the inputs and the output of the power amplifier. Based on these samples a mathematical model is developed and then inverted to produce the opposite distortion of the exhibited by the power amplifier. This model is then placed at the input of the amplifier resulting in a linear amplification.

The modeling step is a complex task and several mathematical approaches can be found in the literature. These approaches include Nonlinear Auto-Regressive Moving Average (NARMA)[47], Volterra series (or pruned Volterra) [48], memory polynomials, Wienner-Hammerstein models [49] and neural networks among others.

Chapter 3

Envelope Tracking design and implementation

During the design and implementation process of the envelope amplifier, more than one possible solution was tried in order to achieve the best performance in the final testbed. This chapter addresses a detailed description of the procedure followed to achieve the final design and the limitations found during the process.

This chapter starts giving a full description of the desired structure of the Envelope Tracing as well as the technical details that have to be accomplished in the design. Given the fact that during the development limitations related with the available resources appeared, the subsequent section gives a brief description of the available resources to develop this project. The following sections include a full description of the design and implementation as well as simulations results of the partial stages.

3.1 Required structure and technical details

The design of the envelope tracking testbed had to include a reliable and robust configuration because the structure will be used to develop research activities. Due to its end use, the testbed should allow to work with real and recent communications standards. As initial requirement the following technical details were considered:

- The envelope amplifier should include a switched amplifier aimed to achieve a high efficient amplification
- Modulation at RF using a 2GHz carrier exhibiting a bandwidth of around 5 MHz in order to simulate real communications standards.

- The envelope amplifier should provide peak voltage levels around 30V with currents up to 2A to the RFPA drain in order to accomplish real radio-base stations transmission power.

- The structure has to incorporate digital pre-distortion to the RFPA using an FPGA. So the RFPA inputs and output should be able to be monitored. Moreover, as an innovative research work, the design will include the slew-rate reduction algorithm described in Section 3.3.

Having in mind the above described restrictions, a general block diagram of how the testbed should looks like is shown in Figure 3.1

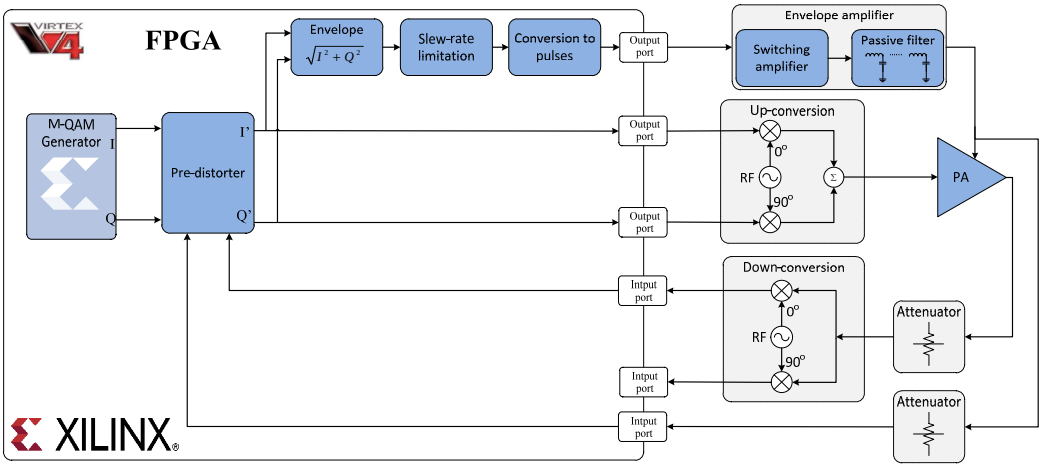


Figure 3.1: General scheme of the initial design for the ET transmitter

3.2 Environment description

During the design and implementation processes, some limitations related with the available resources where faced at different stages. For this reason, it is worth mentioning the main available resources as well as their advantages and disadvantages in the completeness of the final test bench. The following section gives such description focusing on the specifications related with the development of this project.

Field Programmable Gate Array (FPGA)

The available FPGA is a Virtex 4 developed by Xilinx Inc, which programming environment is the Xilinx ISE. This FPGA includes two Digital to Analog Converters and two Analog to Digital Converters. The DAC should be driven by a 14-bit fixed-point

signal with the binary point at the position 13 while the input ADCs is restricted in the range ±1V. The four converters are restricted to work with a clock speed lower than 64 MHz. On the other hand, the internal clock is able to work at predefined frequencies, these frequencies include 20 MHz; 25 MHz; 30 MHz; 33.33 MHz; 40 MHz; 45 MHz; 50 MHz; 60 MHz; 66.66 MHz; 70 MHz; 75 MHz; 80 MHz; 90 MHz; 100 MHz and 120 MHz. However, since converters are needed then this list is limited to the first eight frequencies.

The number of DACs and ADCs imposed a primary limitation over the implementation: Since it was desired to implement an envelope tracking amplifier with possibilities to use pre-distortion, it was necessary to monitor the inputs and the output of the power amplifier. The inputs comprise the dynamic voltage supply, i.e. the amplified envelope, and the RF signal, which is composed by the I and Q components. On the other hand, the output is the RF amplified signal, composed by the amplified versions of the I and Q components. Such monitoring would require three outputs and three inputs from the FPGA point of view, which was not straightforward.

The two DACs would be used to generate the I and Q components, but one more would be missing to generate the envelope signal. To get around this difficulty, it was created an output from a Light-Emitting Diode (LED) whose status could be controlled from the programming environment. This LED was removed from the FPGA board so its output could be used to generate a two levels signal. The measured voltage at this output was 0V on the *off* state and 3.3 V on the *on* state. This new output would allow to generate the pulsed envelope signal.

A similar approach to the above described could not be used for the ADCs. To solve the problem of monitoring three signals, one ADC was used to sample the envelope while the other had to be used to monitor the I and Q components simultaneously. The last was possible by sampling the signal at Frequency (IF) instead of doing it at baseband. The theoretical explanation and practical implementation of the IF sampling is fully described in 3.9.

A better understanding about the usage of the FPGA inputs/outputs can be achieved by means of figure (3.2) which shows a scheme of the inputs/outputs and the signal handled by each port.

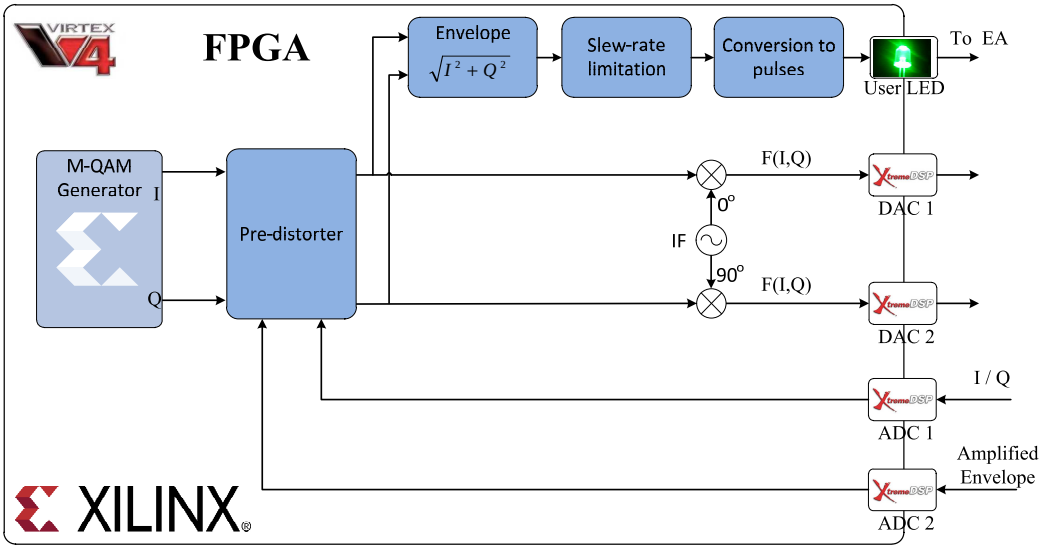


Figure 3.2: Use of the input/output ports of the FPGA

Up-conversion to RF

The up-conversion to RF was performed using a direct up-conversion device from Texas Instrument model TRF372017EVM. A general block diagram of this up-converter is shown in Figure (3.3). As the block diagram shows, the up-converter includes its own local oscillator (LO), moreover this LO could be used on the demodulation to achieve a coherent demodulation. Further details about this device can be found in [50, 51]

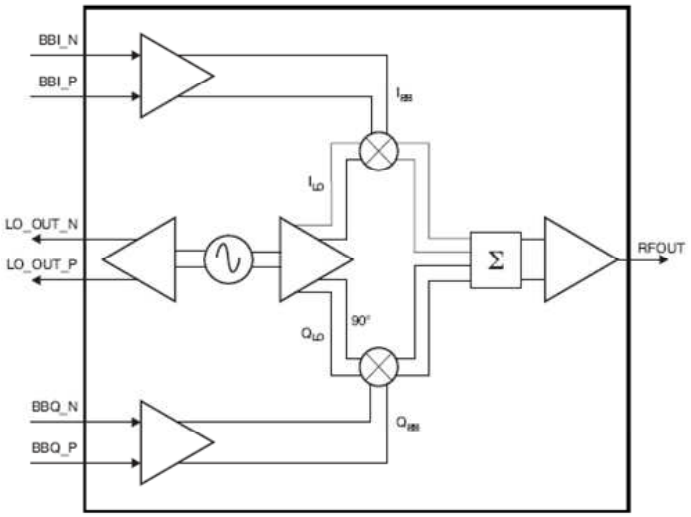


Figure 3.3: Up-converter block diagram (TRF372017EVM)

RF power amplifier

The amplified envelope supplied dynamically the voltage to a RFPA included on a Cree Inc. Eval. Board CGH40010-TB (GaN HEMT transistor, 10 W CW). Specific details about this amplifier could be found in [52]

Down-conversion

The down-conversion using a receiver direct down-converter quadrature demodulator from Texas Instrument. This down-converter is present on the evaluation module TRF371125 and includes programmable base-band filters, adjustable dc offset correction, and buffer amplifiers to directly drive ADCs. The basic block diagram of this down-converter is shown in Figure (3.4). Further details regarding this device can be found in [53, 54]

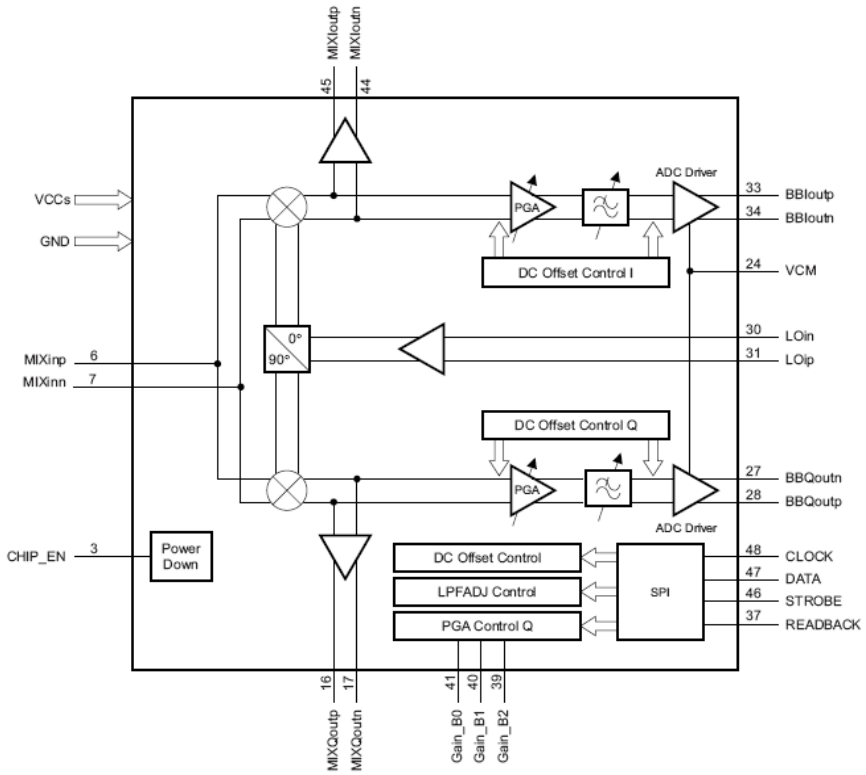


Figure 3.4: Down-converter block diagram (TRF371125EVM)

Measurement equipment

The measurement equipment consisted on an *Agilent Infinium* oscilloscope model DSO90404A for sampling the input and output signals at 2GHz. An Agilent N2783A

probe for measuring the transistor drain current. An *Agilent* spectrum analyzer to visualize the spectrum of the signals. Additionally other general oscilloscopes, voltage sources and laboratory material were employed.

3.3 Slew-rate reduction algorithm

The slew-rate parameter defines the maximum possible slope that the PA is able to follow. Low values in this parameter limits EAs to follow the rapid changes on the envelope of the signal; if the envelope has a very wide spectrum bandwidth, it means that the signal contains high frequency components, whose changes the EA is not able to follow. It does not exist a formal correspondence between the slew-rate and the bandwidth of any signal, however as will be shown a limitations on the slew-rate implies a limitation on the bandwidth and vice-verse.

The slew-rate envelope reduction algorithm is fully described in [1]. In short the algorithm could be described as follows: The envelope signal is processed in real time to obtain a reduced bandwidth version of it. This processing is based on present and future values of the original envelope occasioning an small delay that could be compensated like any other misalignment in the signal paths of either EER or ET architectures. The algorithm defines four parameters: The maximum slew rate ($\pm\Delta_M$), the minimum number of steps for going from 0 to 1 on a one-normalized excursion ($N = \Delta_M^{-1}$), the original envelope signal ($E(n)$) and the reduced bandwidth envelope ($E_s(n)$). Moreover the following conditions must be hold:

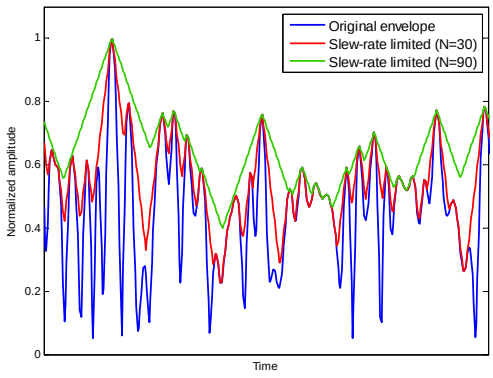
- At time n, the generated envelope $E_s(n)$ must be at least $E(n+k)-k\Delta_M$in order to hold $E_s(n+k) > E(n+k)$ at any subsequent time $n+k$
- $E_s(n-1) - \Delta_M < E_s(n) < E_s(n-1) + \Delta_M$ in order to limit the slew rate variations

By using a intermediate variable $y(n)$ representing an upper bound of $E(n)$ and a lower bound of $E_s(n)$, the algorithm (in its causal version) could be written as:

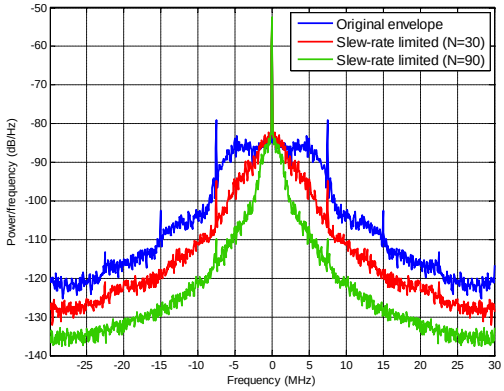
$$y(n-N) = max_{i=0,1,2...N}\{E(n-N+i) - i\Delta_M\} \tag{3.1}$$

$$E_s(n-1) - \Delta_M < E_s(n) < E_s(n-1) + \Delta_M \tag{3.2}$$

Figure (3.5) shows the time and spectral representations of the envelope and its reduced. As could be observed in this figure, the smaller is the maximum slewrate allowed the narrower the bandwidth of the resulting signal is, therefore it exists a direct relationship between these two parameters.



(a) Time representation for the original envelope (blue), and two different slew-rate limitations.



(b) Frequency representation for the original envelope (blue), and two different slew-rate limitations.

Figure 3.5: Time and frequency representation for a 16-QAM signal and its slew-rate limitation.

3.4 Pulse Width Modulator

3.4.1 Implementation on the FPGA

The main limitation of the pulse width modulator concerning its implementation on the FPGA was the clock speed of the processor. As explained in Section 2.4.1, in order to achieve a good result, the clock speed is desired to be as high as possible. In this way, it would be possible for a fixed bandwidth signal, to achieve a good resolution in the modulated signal and its first replica would be away from base-band in the frequency spectrum. Nevertheless, the necessity to use both the DAC and ADC, imposes a maximum clock speed of 60 MHz (see Section 3.2). On the other hand, even if higher frequencies were allowed on the FPGA clock speed, it wouldn't be possible to work using those frequencies because the hardware of the envelope amplifier also imposes limitations. Current technology allow to amplify just few MHz signals when tens of volts are desired at the output.

In order to simulate quickly and accurately the results that could yield the FPGA, initially a MATLAB script was developed. This script is shown in Figure A.1

on Appendix A and considers the signal processing involved in the modulation as well as the FPGA clock limitation.

By using a 60 MHz clock and different input signals, it was determined that the maximum possible useful bandwidth could be around 2 MHz when a 6 MHz sawtooth carrier is used. This fact led to use the algorithm presented in Section 3.3, in order to reduce the envelope slew-rate up to the point when approximately a 2 MHz bandwidth envelope was achieved. Such reduction was obtained using N = 88 in the algorithm.

A block diagram of the implemented pulse with modulator is shown in Figure (3.6). For a correct functioning, the input should be limited in the interval [0 1) and should be represented using a 14-bit fixed-point signal with the binary point at the position 13 (Q1.13). As Figure 3.6 shows, the carrier is generated using an incremental one step counter. This counter is limited in the interval [0 9] yielding a frequency of $f_{carrier}$ = 60 MHz/10 = 6 MHz. Its output is multiplied by a constant to limit it in the interval [0 9) and allow its representation using a Q1.13 signal. As final step, a logical comparator is used to determine whether the signal is above or below the carrier, yielding "high" or "low" respectively and so producing the modulated signal.

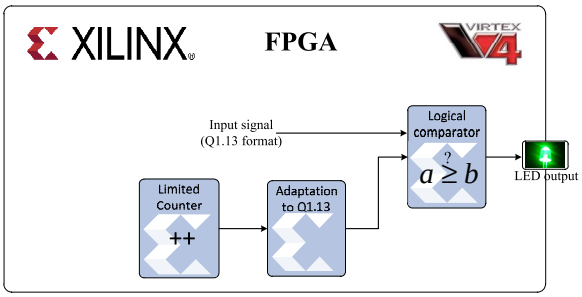
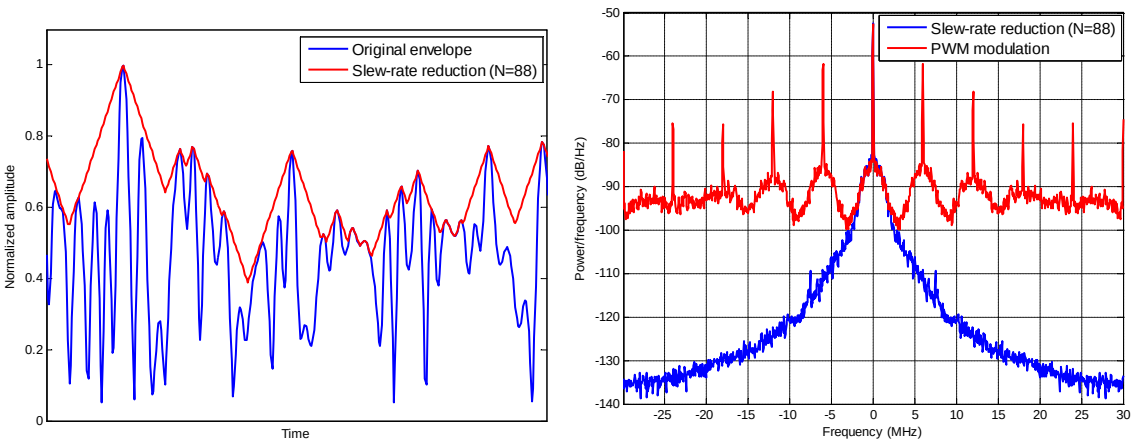


Figure 3.6: Block diagram of the implemented PWM

3.4.2 Simulation results

Figure 3.7 shows the graphics obtained using the pulse width modulator implemented on the FPGA. Figure 3.7a shows the envelope of a 16-QAM signal (in blue) and its reduced slew-rate version (in red) in time domain, whereas Figure 3.7b shows the spectrum of the reduced slew-rate envelope (in blue) and its modulation using PWM (in red). As can be observed, it is possible to recover only an spectrum bandwidth of around 2 MHz. Other conbination of shapes and frequencies of the carrier and input signal bandwidthl lead to worse results.

Despite the limitation of the input signal bandwidth above explained, it is important to remark that variations on the PWM technique offers the possibility to



(a) Time representation of the original envelope (blue) and its slew-rate limited version (red)

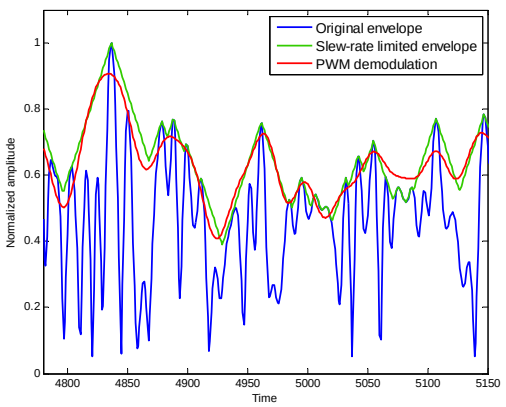
(b) Frequency representation of the slew-rate limited envelope (blue) and its PWM modulation (red)

Figure 3.7: Modulation using PWM and a slew-rate limited envelope

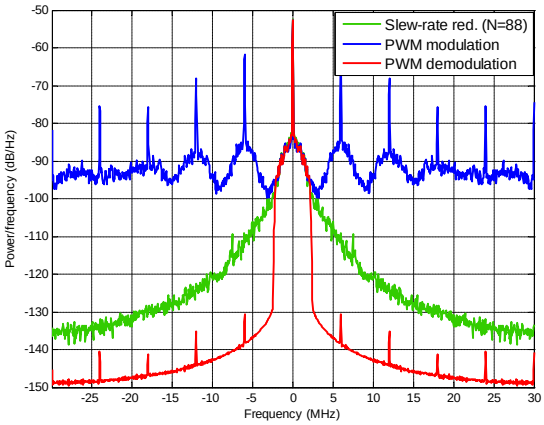
generate pulses exhibiting more than two levels at the output, which led to better results. However since a LED was used as output to the signal, the only possibility was to implement the two level approach.

Regarding the demodulation of the signal, a simple low pass filter is enough to recover the original signal, or a similar version, since it is impossible to exactly recover the original one. A digital low pass filter was synthesized to have an idea about the appearance of the signal once amplified and demodulated. At this point it is worth mentioning that even if the precise demodulator filter was found in this step, it is not possible to reproduce in the analog domain the same filter. There exist many methods to go from analog to digital domain and vice-verse(e.g. bi-linear transform, etc.), nevertheless none of them offers exactly the same response, there are always changes on the phase and magnitude margins in addition to the errors associated with the circuit components values. However, filtering on the digital domain could give a good idea about the final output in the analog domain. Figure 3.8 shows in time and frequency representation of the pulse width modulation and demodulation process. Figure 3.8a shows the original envelope (in blue), the slew-rate limited envelope (in green) and the resulting signal once the demodulation have been performed (in red). Notice that the recovered signal is not very similar to the original one in the time domain. This difference would not be so crucial if the recovered signal was always above the original envelope, but if this is not the case, then the PA would be beyond the compression point. In other words, if the recovered signal was below the envelope it would mean that the requested output signal is greater than the supply voltage and therefore the PA becomes unable to amplify its input appearing non-linear distortion at the output.

Concerning the spectral representation showed in Figure 3.8b, it should be emphasized that in the demodulation process a very selective digital filter with a high attenuation on the rejected band have been used. However, despite the use of this filter, the carrier frequency and its replicas appear in the spectrum of the demodulated signal. Moreover, in this result no amplification of the signal was performed; this suggest that the analog filter to be implemented should be very selective and should have a high attenuation in the rejected band.



(a) Time representation of the original envelope (blue), its slew-rate limitation (green) and its demodulation (red) when PWM is used



(b) Frequency representation of the slew-rate reduced envelope (in green), its modulated (in blue) and demodulated (in red) versions when the PWM technique is used

Figure 3.8: Demodulation using PWM and a slew-rate limited envelope

The above results suggest that the PWM is not suitable to amplify the signal resulting from the slow-rate reduction algorithm. Moreover, since this signal is not clearly limited in bandwidth and the pulse width modulator allows to recover at most 2 MHz bandwidth, a possible solution seems to be to limit the spectrum of the modulating signal. Such approach would be studied in the subsequent sections.

3.5 Delta-Sigma Modulator

3.5.1 Implementation on the FPGA

The primary limitation was imposed by the maximum allowed clock speed. As mentioned in Section 2.4.2 the higher the clock speed is the further the switching noise could be pushed away from base-band, that is, far away from the spectrum portion to be recovered. However, the necessity to use both the DAC and ADC, imposes a maximum clock speed of 60 MHz (see Section 3.2). On the other hand, even if higher

frequencies were allowed on the FPGA clock speed, it would not be possible to work using those frequencies because the hardware of the envelope amplifier also imposes limitations. Current technology allow to amplify just few MHz signals when decades of voltage are desired at the output.

Again, in order to simulate quickly and accurately the results that could provide the FPGA, a MATLAB script was developed. This script is shown in Figure B.1 on Appendix B and considers the signal processing involved for a first and second order $\Delta - \Sigma$ modulation as well as the FPGA clock limitation. Higher orders are not implemented because those systems could become unstable (see 2.4.2). Nevertheless, the suitability of higher orders was evaluated using the MATLAB *Delta Sigma Toolbox* available in [55].

By using the Delta Sigma Toolbox several orders, gains and oversampling ratios as well as different bandwidth input signals were evaluated. This evaluation lead to the conclusion that the best possible result is obtained using a second order delta sigma modulator, including an oversampling ratio of 5 and an infinite gain of when the input signal has around 2 MHz bandwidth. This fact led to use the algorithm presented in Section 3.3, in order to reduce the envelope slew-rate up to the point when approximately a 2 MHz bandwidth envelope was achieved. Such reduction was obtained using N = 88 in the algorithm.

The block diagram of the implementation of the delta sigma modulator is shown in Figure 3.9 . For a correct functioning, the input should be limited in the interval [0 1) and should be represented using a 14-bit fixed-point signal with the binary point at the position 13 (Q1.13). Notice that the structure of this filter is the same structure shown in Figure 2.10b, but here the filters have been expressed in the time domain instead of the Z-domain. It is important to remark that the subtractions don not introduce additional delays, otherwise the system could become unstable. After going through two filters the error signal arrives to a logical comparator that is used to determine whether the signal is above or below the constant, in this way the "high" and "low" outputs are induced and so producing the modulated signal.

3.5.2 Simulation results

Figure 3.10 shows the graphics obtained using the second-order $\Delta - \Sigma$ modulator implemented on the FPGA. Figure 3.10a shows the envelope of a 16-QAM signal (in blue) and its reduced slew-rate version (in red) in time domain, whereas Figure 3.10 shows the spectrum of the reduced slew-rate envelope (in blue) and its modulation

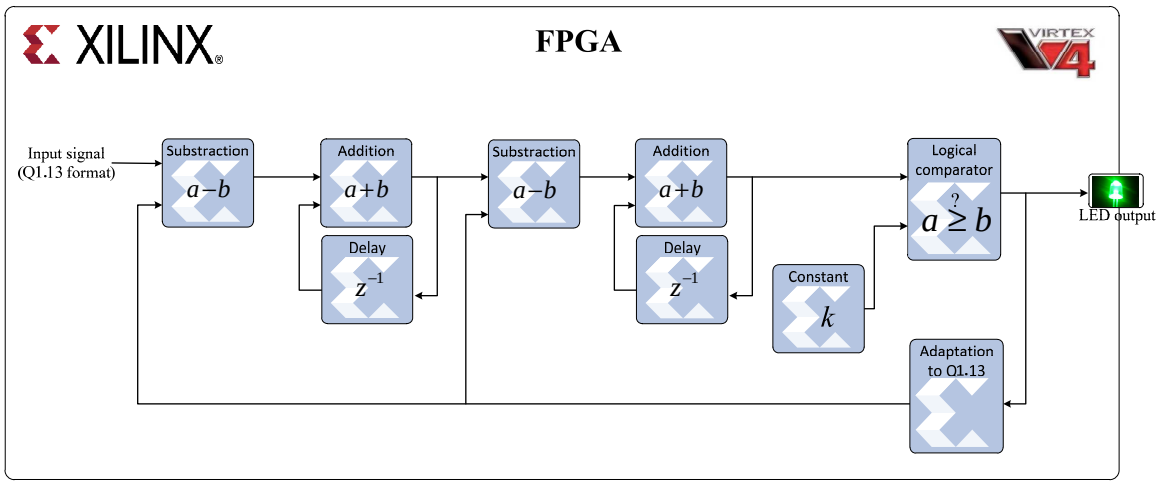
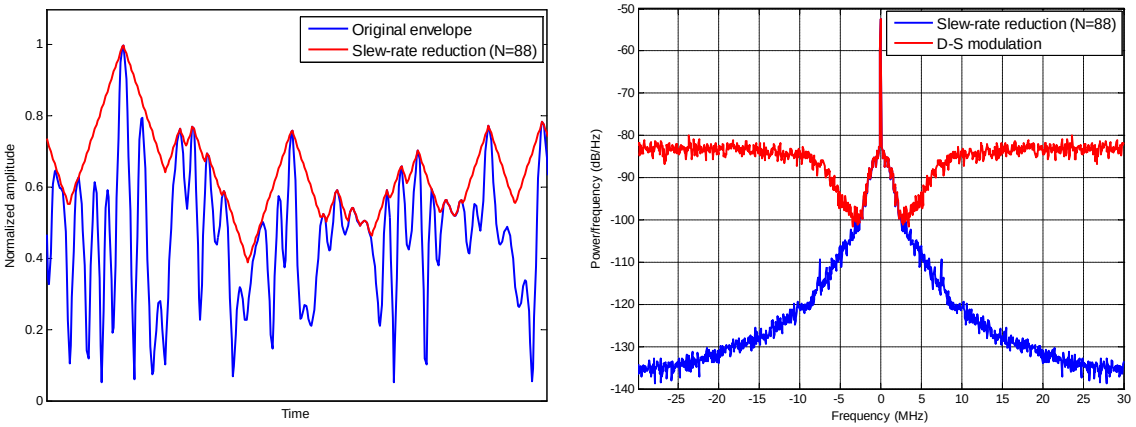


Figure 3.9: Block diagram of the second-order Delta Sigma modulator implemented on the FPGA

using $\Delta - \Sigma$ (in red), notice that using this modulation technique a maximum of 2 MHz bandwidth can be recovered at the output.



(a) Time domain of the envelope and its reduced slew-rate version

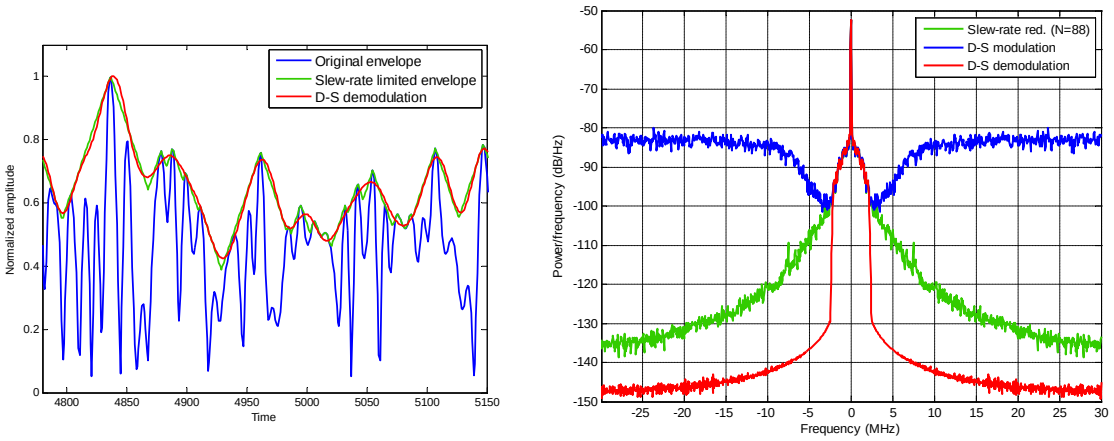
(b) Frequency representation of the reduced slew-rate envelope and its modulation \Delta-\Sigma

Figure 3.10: Modulation using $\Delta - \Sigma$M and a slew-rate limited envelope

Regarding the demodulation of the signal, similar to the PWM case, a simple low pass filter is enough to recover the original signal. In order to make a fair comparison it was employed the same filter used in PWM case. Figure 3.11a shows the original envelope (in blue), the slew-rate limited envelope (in green) and the resulting signal once the demodulation is performed (in red). Notice that compared with the PWM, the recovered signal seems to be closer to the original signal. Moreover, it is closer to be above the original envelope, which is a crucial point regarding the modulation-demodulation processes.

On the other hand, Figure 3.11 shows the spectrum of the slew-rate limited

envelope (in green), its modulation using Delta Sigma (in blue) and the demodulated signal (in red). Note that, like in the PWM case, despite of the similarity between the modulating and demodulated signal in the time domain, the spectral representation shows that a big part of the spectrum signal have been lost due to the filtering effect (demodulation). However, the demodulated spectrum does not exhibits the undesired carrier of the PWM and its replicas.



(a) Time representation of the original envelope (blue), its slew-rate limitation (green) and its demodulation (red) when $\Delta - \Sigma$M is used

(b) Frequency representation of the slew-rate reduced envelope (in green), its modulated (in blue) and demodulated (in red) versions when the $\Delta - \Sigma$M technique is used.

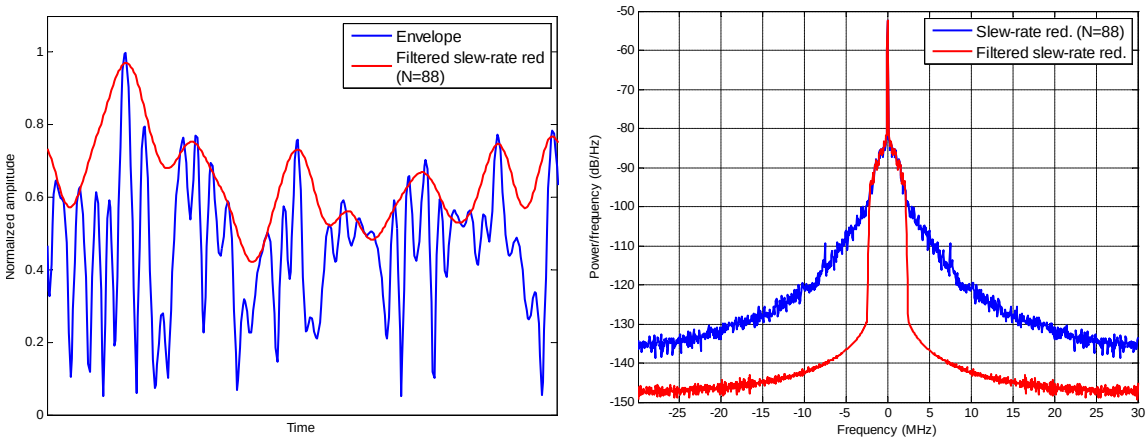
Figure 3.11: Demodulation using $\Delta - \Sigma$M and a slew-rate limited envelope

Once more, similar to the PWM these results suggest that the $\Delta - \Sigma$M does not allow to recover completely the signal due to its unclear spectrum limitation. Therefore, as suggested before, possible solution seems to be to limit the spectrum of the input signal (slow envelope). Anyhow, comparing the simulation results obtained in the PWM case and here, it is clear that the $\Delta - \Sigma$M yields better results.

3.6 A new algorithm for bandwidth reduction

The simulation results of the PWM and $\Delta - \Sigma$M showed in Sections 3.4.2 and Section 3.5.2 respectively, suggest that the input signal is not adequate to perform these modulations and recover a good enough result. A simple and short test puts on evidence this hypothesis: Let us consider the modulating signal, that is, the slew-rate limited envelope obtained for N=88 using the algorithm presented in Section 3.3. Instead of modulating this signal, either using PWM or $\Delta - \Sigma$, it is low pass filtered to check its time domain representation. Figure 3.12 shows the frequency and time domain representations of the slew-rate limited envelope (in blue) and its low pass filtered version

(in red). As Figure 3.12a shows, the recovered signal is still below the original envelope at some points. Such phenomenon occurs because the slew-rate limiter algorithm introduce peaks in the time domain when the slew-rate reduction is performed. However, to represent those peaks in the frequency domain high frequency components are required. Those components are removing when low pass filtering the signal, and the peaks cannot be represented any more, occasioning that the signal appears below the original envelope.



(a) Time representation of the original envelope (blue) and the resulting signal after limiting the slew-rate and filtering (red).

(b) Frequency representation of the original envelope (blue) and the resulting signal after limiting the slew-rate and filtering (red).

Figure 3.12: Time and frequency representation for a 16-QAM signal and its slew-rate limitation filtered.

A possible solution to this problem seems to be limiting clearly the spectrum of the input signal. Unfortunately a direct low pass filtering of the original envelope cannot be done directly. This will not ensure that the resulting signal is going to be above the original envelope in all the points. An indirect way to low pass filter a signal is averaging the samples. However, a couple of details are worth of mention: First, the average have to be done using future and pass samples, and second, even when the average is performed using both past and future samples, the resulting signal still can be below the original envelope. These statements will be shortly explained

This problem led to the development of a bandwidth reduction algorithm in order to have a clear limitation of the bandwidth when the reduction is performed. Such limitation in bandwidth implies also a limitation on the slew-rate which means that both switching and linear envelope amplifiers would be able to follow the changes of the signal. Moreover, this bandwidth limitation would allow a better modulation using either PWM or $\Delta - \Sigma$M.

3.6.1 Mathematical formulation

This developement of the algorithm for the bandwidth envelope reduction was inspired in an image processing technique used to detect the contours of objects in images. The image processing algorithm is called *Snakes* and for the sake of simplicity a similar notation will be used here to describe the bandwidth reduction algorithm. Further details about the Snake algorithm can be found in [56].

The goal of this new bandwidth reduction algorithm is to create a new envelope with clear and adjustable spectral limitation such that this new envelope is always above the original envelope. To do so, this algorithm uses as starting point a constant whose value is the maximum possible value achieved by the original envelope. For a fixed time interval, this constant value is iteratively adjusted to the shape of the original envelope having in mind the spectral limitation, that is, a clear bandwidth limitation. Such restrictions are fulfilled using two main strategies: The first one, assigning internal and external forces in the deformation of the new envelope and the second one, repeating strategic sample values in combination with averaging.

The external force represents the force that moves the new envelope towards the original envelope, this force is governed by a gradient which turns out to be the square of the difference between the value of the new envelope and the value of the original envelope at a given iteration and point. It could be thought as the force exerted by a spring that joints these two curves. For example, let $E(n)$ be the original envelope and $E_s(n)$ the new envelope, where the sub-index "s" stands for *"slow"* making reference to its slowness in time compared with $E(n)$. The external force, at the sample n and iteration k, that moves the $E_s(n)$ towards $E(n)$ is given then by:

$$F_{ext}(n,k) = C_1 \left(E_s(n,k) - E(n)\right)^2 \tag{3.3}$$

On the other hand, the internal forces are those forces that keep the new envelope smooth, avoiding in this way the apparition of high frequency components on the new envelope. Tho achieve this smoothness, the internal forces are based on derivatives. If the first and second order derivatives are considered, then the internal force, at the sample n and iteration k, is given by:

$$F_{int}(n,k) = \frac{\partial E(n,k-1)}{\partial n} + \frac{\partial^2 E(n,k-1)}{\partial n^2} \tag{3.4}$$

However, continuous derivatives are not defined on the digital domain, instead Taylor approximations could be used to reproduce their equivalent in the digital domain. For the first four order derivatives, their Taylor approximations are given by:

Central first derivative, fourth order:

$$\left|\frac{\partial u}{\partial x}\right|_i = \frac{-u_{i+2} + 8u_{i+1} - 8u_{i-1} + u_{i-2}}{12\Delta x} \tag{3.5}$$

Central second derivative, fourth order:

$$\left|\frac{\partial^2 u}{\partial x^2}\right|_i = \frac{-u_{i+2} + 16u_{i+1} - 30u_i + 16u_{i-1} - u_{i-2}}{12\Delta x^2} \tag{3.6}$$

Central third derivative, fourth order:

$$\left|\frac{\partial^3 u}{\partial x^3}\right|_i = \frac{-u_{i+3} + 8u_{i+2} - 13u_{i+1} + 13u_{i-1} - 8u_{i-2} + u_{i-3}}{8\Delta x^3} \tag{3.7}$$

Central fourth derivative, second order:

$$\left|\frac{\partial^4 u}{\partial x^4}\right|_i = \frac{u_{i+2} - 4u_{i+1} + 6u_i - 4u_{i-1} + u_{i-2}}{\Delta x^4} \tag{3.8}$$

Higher orders and detailed explanations to obtain the approximations could be found in [57, 58, 59]. However, for the sake of simplicity in the following explanation just the firsts two order derivatives are considered. Nevertheless, it should be pointed out that the higher derivatives orders are considered the better the reduction of higher frequencies is. In a MATLAB script developed to simulate the behave of this algorithm derivatives up to fourth order were considered. The script is shown in Figure D.1 on the Appendix D.

Considering the above listed approximations, and using just the first and second order derivatives, the equation 3.4 could be rewritten as:

$$\begin{aligned} F_{int}(n,k) = {} & |C_2\left(-E(n+2) + 8E(n+1) - 8E(n-1) + E(n-2)\right)|_{k-1} + \\ & |C_3\left(-E(n+2) + 16E(n+1) - 30E(n) + 16E(n-1) - E(n-2)\right)|_{k-1} \end{aligned} \tag{3.9}$$

Where C_2 and C_3 are constants to allow a better adjustment of the influence of each term in addition to substitute the denominators of equations 3.5 and 3.6. The total force is the result of the combination of the external force (equation 3.3) and the internal forces (equation 3.9). In terms of equation, it could be written as:

$$F_{total} = F_{ext} - F_{int} \tag{3.10}$$

Then a partial result of the new envelope at the iteration k is given by:

$$E'(n,k) = E_s(n,k-1) - F_{ext} + F_{int} \tag{3.11}$$

The internal and external forces contribute in the deformation of the new envelope, but even when derivatives up to fourth order are considered, it is not enough to keep the smoothness and bandwidth limitation. In particular, in the equation 3.11 the resulting signal ($E'(n,k)$) may not be band-limited and smooth signal if it is not ensured $E_s(n,k-1)$ to hold the same property. Moreover, F_{ext} results from $E(n)$ (see equation 3.3), which has wide bandwidth. This is the reason why the averaging is introduced in the algorithm.

On the other hand, depending on the constants used to adjust the internal and external forces, $E'(n,k)$ (in equation 3.11) could be below the the original envelope ($E(n)$). To ensure that the resulting signal is going to be always above, the external force is set to zero in all those points where $E'(n,k)$ is below ($E(n)$). However, since this breaks the smoothness of the signal, an average has to be performed, usually more than once, to limit the bandwidth of the signal make it smooth. Once it has been ensured that the external force is band-limited and smooth, the mathematical operation of the equation 3.11 is performed and the slow envelope for the next iteration is given by:

$$E_s(n,k+1) = E'(n,k) \tag{3.12}$$

Regarding the averaging process it has to be emphasized that the averaging performed in this algorithm is based on future and pass samples, otherwise the resulting signal will be asymmetrically deformed. For example, consider an averaging of 31 samples, for the signal showed in blue color in the Figure 3.13 (the reason to use 31 samples will be shortly clarified). If the average of this signal is computed using only pass samples, that is the average value of the sample n is based on the average of the

samples n, n-1, n-2.... n-20, then the resulting signal is the one showed in red color. On the other hand, if the averaging is computed using a central pivot, that is the average of the sample n is based on the average of the samples n-10, n-9, n-8.... n-1,n,n+1,...n+8,n+9,n+10, then the resulting signal is the one showed in green color. As can be deduced then, pass and future samples are required in order to keep symmetry on the averaged signal, moreover, it is necessary to use an odd number of samples otherwise the symmetry is also broken. The counterpart of this averaging method is the introduction of delays, that has to be compensated before the transmission of the signal.

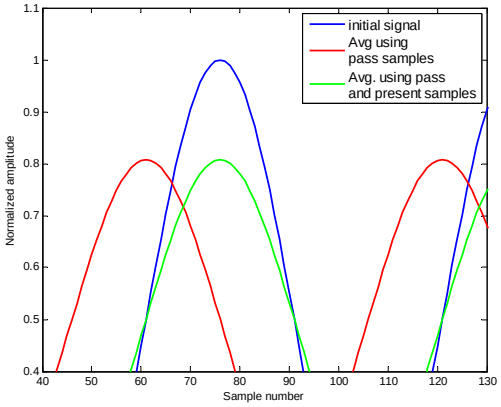
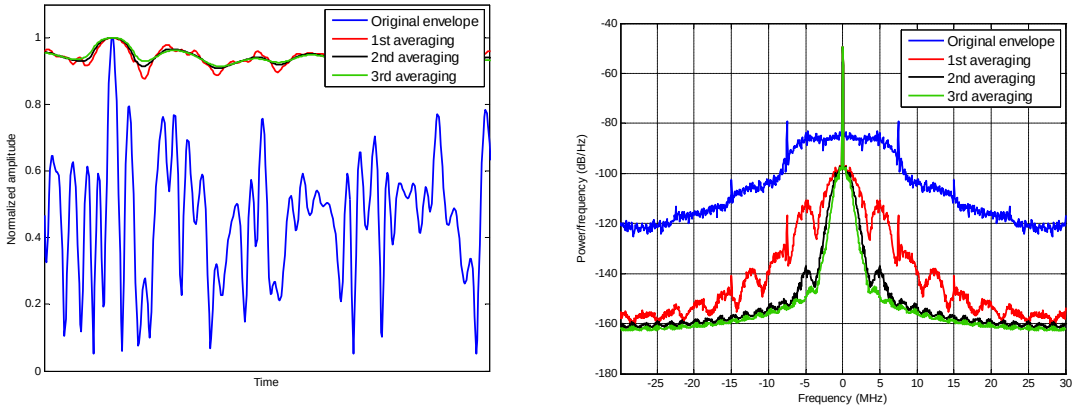


Figure 3.13: Averaging process

The number of samples to be averaged is closely related to the bandwidth of the signal desired to achieve. For instance, if it is desired to limit the bandwidth to BW, and the clock speed of the FPGA is F_s then the number of points to average would be $N = F_s/BW$. Therefore, for a bandwidth restriction of 2 MHz, the number of samples to average is $N = 60\,MHz/2\,MHz = 30$, but since the number of samples should be odd, the closest odd number is $N = 31$

The averaging process using a central pivot produces a uniform deformation. Nevertheless, the resulting signal still can go below the original one performing this average. However, this is not the case in this algorithm, since the averaging process is performed on the external forces which is later subtracted from the slow envelope of the previous iteration. In this case, the performance of the average repeatedly in the same iteration will led to have a better bandwidth limitation but if the process is performed in excess the variations of the slow envelope are reduced. This is not desirable because it implies a reduction of the expected efficiency in the envelope tracking architecture; remember that the ideal case is to supply the RFPA voltage with a signal as similar as possible to the envelope of the RF signal to be transmitted. Figure 3.14 shows the effect of performing up to three averages in the first iteration. As can be seen in this

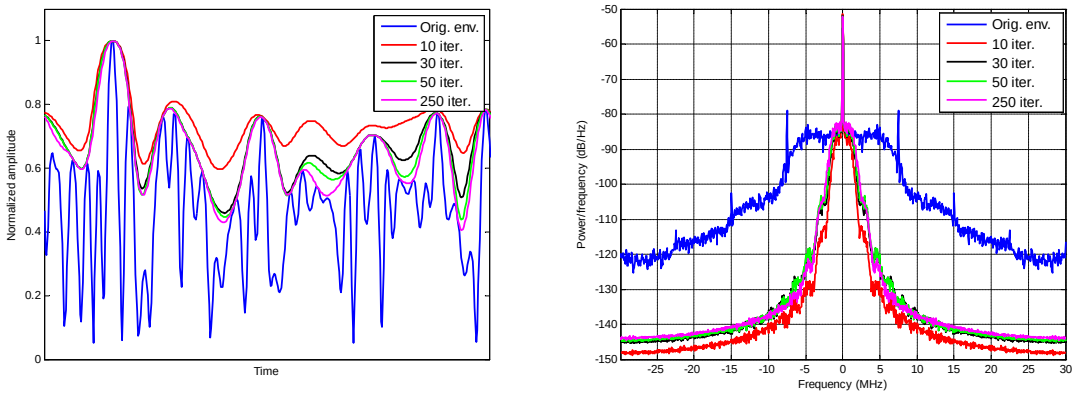
figure, the more times the averaged is performed the smoother is the signal and the better is the bandwidth limitation, but the envelope tends to be a constant



(a) Effect in the time domain (b) Effect in the frequency domain

Figure 3.14: Effect of the number of averages in one iteration

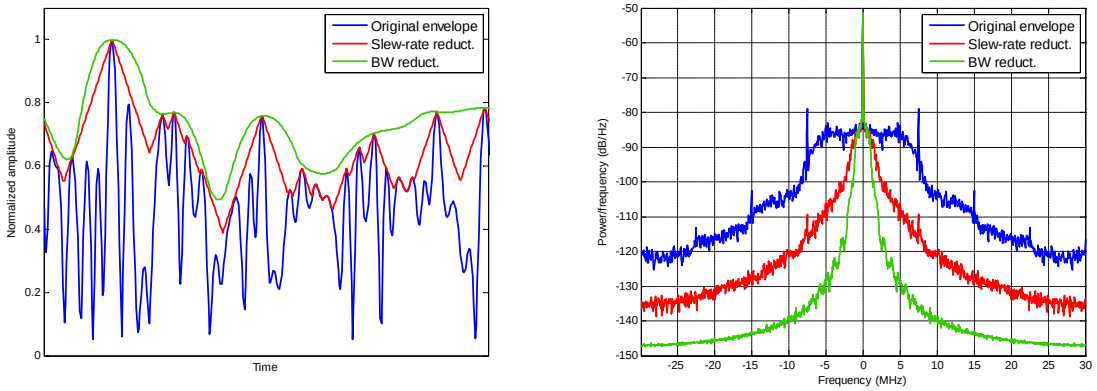
Figure 3.15 shows bandwidth reduction algorithm results in both, time and frequency domain. This results were obtained using five averages at each iteration. The bandwidth limitation was set to 3.5 MHz. Notice that most of the information in frequency is contained inside this bandwidth and the slow envelope is always above the original envelope no matters the number of iterations. The main difference regarding the number of iterations is that the higher is the number of iterations the better adjusted is the slow to its original version and still preserving the bandwidth limitation. This implies a better efficiency in the envelope architecture.



(a) Effect in the time domain (b) Effect in the frequency domain

Figure 3.15: Effect of the number of iterations using five averages

On the other hand, Figure 3.16 compares the results obtained in time and frequency domain for the slew-rate reduction algorithm, when N = 87 is used, and the



(a) Time representation of the original envelope (blue), its slew-rate limitation (red) and its bandwidth reduction (green)

(b) Frequency representation of the original envelope (blue), its slew-rate limitation (red) and its bandwidth reduction (green)

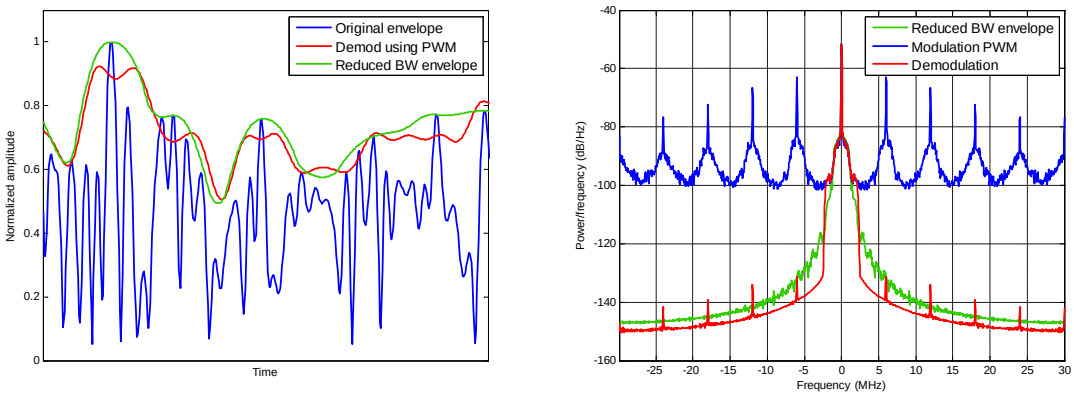
Figure 3.16: Comparison between the slew-rate reduction algorithm and the bandwidth reduction algorithm

results obtained for the bandwidth reduction algorithm, using five averaging at each iteration for a 2 MHz bandwidth limitation.

The above presented graphics show that the bandwidth reduction algorithm performs a clearer limitation in frequency compared to the slew-rate reduction algorithm. Moreover, slew-rate limitation is achieved as well since high variation are avoided in the slow envelope. However, it has to be pointed out that the implementation of this algorithm on a FPGA is not straightforward. The necessity to perform loops, replication of samples and modification of present, pass and "future" samples of the signal during several iterations, make difficult its implementation in real time, not to mention the associated computational load. However it is part of further work to find a suitable way to implement this algorithm on a FPGA. In the mean time, in order to validate the performance of this algorithm, once that the slow envelope was computed in MATLAB, a *shared memory* (memory included in XILINX ISE to transfer values from MATLAB to the FPGA) was used to transfer this signal to the FPGA and simulate its modulation using PWM and Delta-Sigma. Results are showed in the following section.

3.6.2 Simulation results using Pulse Width Modulation

The simulation of the PWM was done using the structure explained in section 3.4.1. The results of the simulation in time and frequency domain are shown in Figure 3.17. Note that in Figure 3.17a the demodulated signal is not always above the original



(a) Time representation of the original envelope (blue), its bandwidth reduction (green) and its demodulation (red) when PWM is used

(b) Frequency representation of the original envelope (blue), its bandwidth reduction (green) and its demodulation (red) when PWM is used

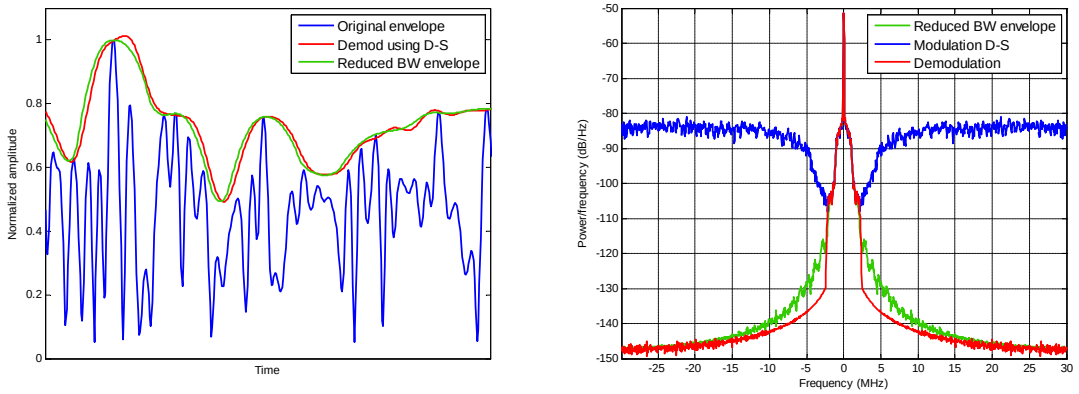
Figure 3.17: Modulation using PWM and the bandwidth reduction algorithm

envelope. However, this signal is closer to the be above the original envelope compared with the signal demodulated when the slew-rate reduction algorithm is used (see Figure 3.8a). The reason to this fact is that most of the information is contained inside the recuperated bandwidth. However, the reason that the signal goes below could be either because the complete signal is not recovered o because the carrier replicas of the pulse width modulator that remains in the spectrum introduce some distortion.

3.6.3 Simulation results using Delta-Sigma Modulation

The simulation of the pulse $\Delta - \Sigma$M was done using the structure explained in section 3.5.1. The results of the simulation in time and frequency domain are shown in Figure 3.18. Note that in Figure 3.18a the recovered signal is always above the original envelope, although it is not accurately followed. Comparing this result with the one obtained using the slew-rate algorithm (see Figure 3.11a), here the resulting signal follows better the original one. The reason is because most of the information of the signal is contained inside the recovered bandwidth. Moreover in comparison with the result obtained using PWM, the signal does not suffer the distortion introduced by the carrier replicas.

The simulations results obtained using PWM and $\Delta\Sigma$M suggest that this algorithm would allows a better performance of the envelope tracking performance regarding the distortion at the output. However, as mentioned before, its implementation on a FPGA is not straightforward and so a different approach had to be found to get around this problem. This situation led to modify the slew-rate reduction algorithm,



(a) Time representation of the original envelope (blue), its bandwidth reduction (green) and its demodulation (red) when $\Delta\Sigma$M is used

(b) Frequency representation of the original envelope (blue), its bandwidth reduction (green) and its demodulation (red) when $\Delta\Sigma$M is used

Figure 3.18: Modulation using $\Delta\Sigma$M and the bandwidth reduction algorithm

such that the resulting signal exhibits a clearer limitation in bandwidth. This band-limitation characteristic was included based on some principles used in the bandwidth reduction algorithm, as explained in the following section.

3.7 Modifications over the slew-rate reduction algorithm

3.7.1 Mathematical formulation

The difficulty to implement the bandwidth reduction algorithm on the FPGA lead to find an alternative solution to improve the results obtained using PWM and $\Delta - \Sigma$M. This solution, as the results presented in the previous sections suggest, should be the incorporation of a clearer bandwidth limitation of the input signal.

On the one hand, when the slew-rate reduction algorithm is used in combination either with PWM or with $\Delta - \Sigma$M, it was observed that cannot be completely recovered the input signal, partially because of its wide spectral characteristic which is truncated during the demodulation. However, the algorithm is simple and real time implementable. On the other hand, when the bandwidth reduction algorithm is used, the recovered signal is closer to be the equal to the original one, nevertheless the algorithm to reduce the bandwidth is complex and its implementation on FPGA is not straightforward. Based on these results, a reasonable solution seems to be to find an alternative that incorporates somehow both characteristics: being implementable in real time implementable and performs bandwidth limitation. Such characteristics

were found on a system that first performs the slew rate limitation and subsequently a subsystem that limits the bandwidth of the resulting signal.

The subsystems that limits the bandwidth of the slew-rate reduced signal is based on the mathematical principles used in the bandwidth reduction algorithm, that is, it is based on the principles of sample replication and averaging (see Section 3.6.1). However, there exists basically three differences between the procedure followed in that algorithm and the one followed here; first, in the bandwidth reduction algorithm the replication of samples and averaging processes are performed over a partial result (the external force) which is later used to compute the slow envelope. On the other hand, here those two processes are performed directly over the slow envelope. To do so, the replication of the samples takes place around local maxima of the signal, that is, over the peaks introduced by the slew-rate reduction algorithm.

Second, as consequence of the direct application of replication and averaging over the slow envelope, it is necessary to take into account an important fact: what happens if two, or more, consecutive peaks appear during the sample replication. If the samples are not replicated properly and in enough quantity, it could be the case that after the averaging, the resulting signals is below the original envelope. A possible solution to this particularity could be to replicate the maximum sample value during the consecutive local maxima. Nevertheless, such approach would imply a reduction in the efficiency of the envelope tracking architecture. The most viable solution is then to replicate only the necessary samples as many times as it is required, that is, the number of samples to be averaged in order to preserve the local maximum. To do so, if a local maximum comes after a higher local maximum the replication of the lower local maximum should take place just on those locations where smaller samples are present. This process is illustrated in the Figure 3.19: The signal showed in blue has three local maxima. The replicated samples are those shown in black while the others, the red samples, are those samples that should be omitted. The highest value is replicated as many times as necessary (13 times in this case) while the replication of the samples of the other two local maxima just takes place in those locations where there is no sample exhibiting a higher value.

In third place, in order to avoid the iterative process, a low pass filter was included once it was ensured that the signal was going to be maintained above the original envelope. Even when the replication and averaging is performed, high frequency components can still remain, occasioned by the discontinuities introduced in the replication of samples. Those components are partially removed by the averaging, but a digital low pass filter can be used to remove them completely and avoid the

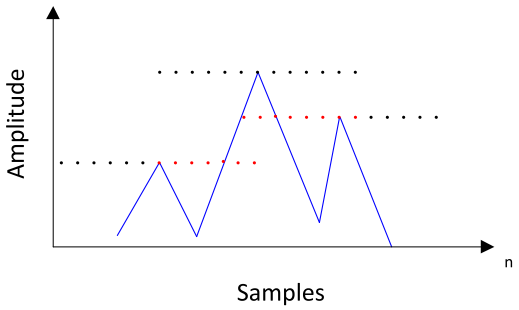


Figure 3.19: Sampling replication process

iterations. However, special attention should be paid to the cut-off frequency of the designed filter, since this frequency should be higher than the equivalent low pass filter performed by the averaging process. If this condition is not hold, it cannot be ensured that the resulting signal is going to be always above the original envelope. In addition, the filter has to has a flat response on the passband, otherwise it will induce signal distortions.

3.7.2 Implementation on the FPGA

Figure 3.20 shows the block diagram of the subsystem that performs the sample replication and averaging process. Despite it is now shown in the diagram, the slew-rate reduction algorithm is previously performed. The output of that system is the input of the subsystem shown below, notice that the input states it. The replication of samples and averaging is performed twice in order to ensure that the resulting signal is going to be always above the original envelope.

The subsystem that performs the replication process uses a principle based on the first derivative to detect the local maxima: By using three consecutive samples, if the subtraction of the first two and the last two have different sign, the there is a maximum, or minimum depending on the reference. Once a local maximum is detected its value is stored in a register and a limited counter is used to count the number of samples replicated. When the replication is finished the output of the register yields zero. The drawback for this structure arises if another local maximum with a lower value comes, in this case the counter is restarted and a lower sample value is going to be replicated. This problem is solved by replicating the structure. Each counter is then independent and consecutive local maxima do not introduce difficulties. As a final step, the maximum of the replicated structured and the input signal is computed. It is important to remark that the delays in the process are adjusted such that the replication of samples seem to be implemented over past and "future" samples. However

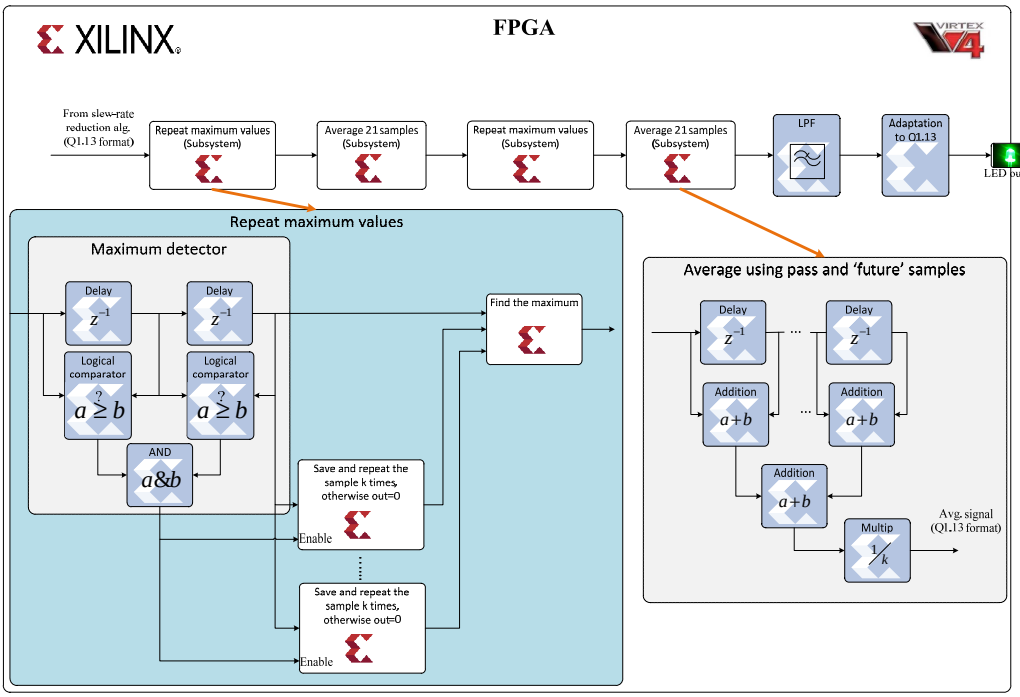


Figure 3.20: Block diagram of the implemented slew-rate/band-limitation process

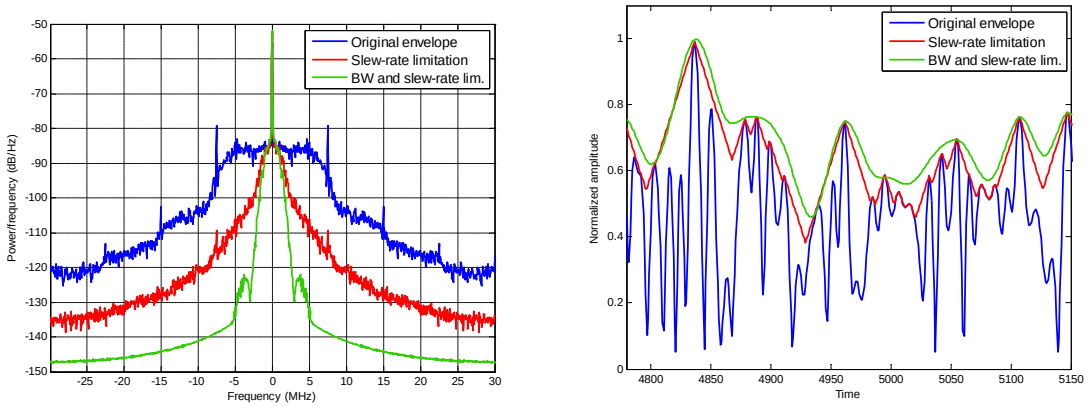
the process is completely causal.

The output of the subsystem that replicates the samples is the averaging subsystem. The averaging is performed adding the values of a given set of samples and then dividing by the number of samples included in the set.

The last block corresponds to a low pas filter, which is used to remove the remaining high frequency components. As mentioned previously, special attention should be paid to the cut-off frequency and the the flatness of the band pass. The performance of the complete process is shown in Figure 3.21. This figure shows the time and frequency representations of the original envelope (in blue), the envelope when the slew-rate limitation is performed (in red) and the envelope when the signal is slew-rate/band-limited.

3.7.3 Simulation results using Pulse Width Modulation and Delta Sigma Modulation

Figure 3.23 shows the modulation and demodulation process when the PWM technique is used to modulate the slew-rate/bandlimited envelope. Notice that the result is very similar to the one obtained when the bandwidth reduction algorithm is used. The recovered signal is not always above the original signal but tries to follow its changes

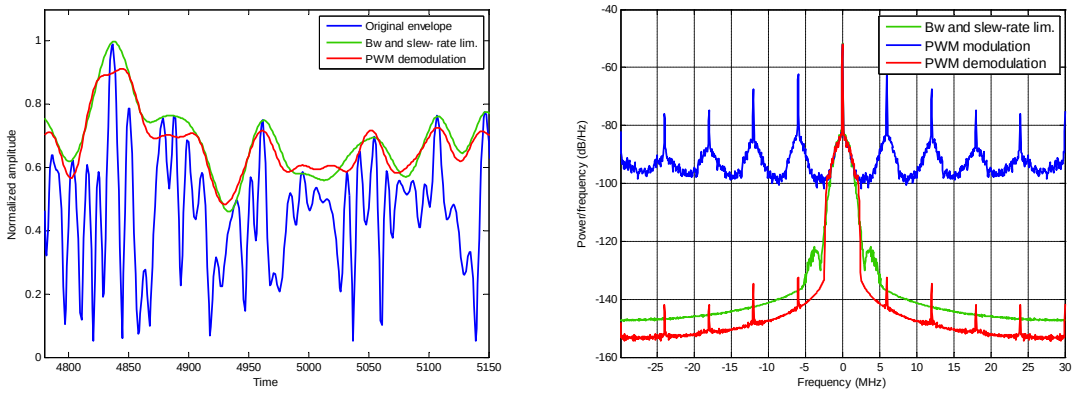


(a) Frequency representation of the original envelope (blue), its slew-rate limitation (red) and its slew-rate/band-limited version (green)

(b) Time representation of the original envelope (blue), its slew-rate limitation (red) and its slew-rate/band-limited version (green)

Figure 3.21: Comparison between the slew-rate reduction algorithm and the slew-rate/band-limited envelope.

in the time domain. Regarding the frequency domain it can be seen that most of the spectral information is recovered, however there is still presence of the PWM carrier replicas.

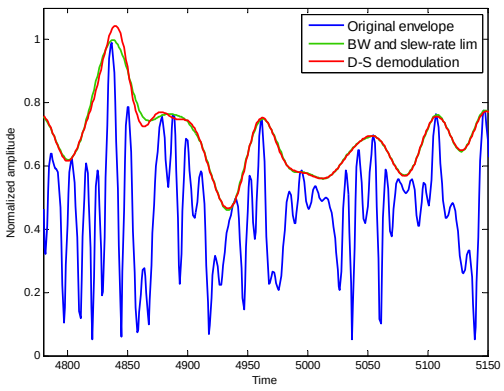


(a) Time representation of the original envelope (blue), its slew-rate/band-limitated version (green) and its demodulation (red) when PWM is used

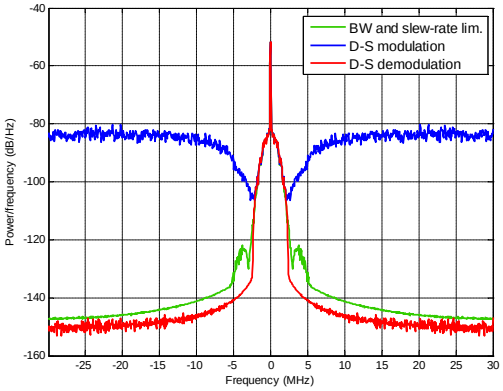
(b) Frequency representation of the original envelope (blue), its slew-rate/band-limitated version (green) and its demodulation (red) when PWM is used

Figure 3.22: Modulation using PWM and the slew-rate/band-limitation process

On the other hand, Figure 3.23 shows the process of modulating and demodulating the slew-rate/bandlimited signal when the $\Delta - \Sigma$M is used. Notice that similar to the result obtained using the bandwidth reduction algorithm the demodulated signal is always above the modulating signal and are very similar in the time domain. Regarding the spectral representation of the signal, it shows that almost all the information have been recovered.



(a) Time representation of the original envelope (blue), its slew-rate/band-limitated version (green) and its demodulation (red) when $\Delta - \Sigma$M is used



(b) Frequency representation of the original envelope (blue), its slew-rate/band-limitated version (green) and its demodulation (red) when $\Delta - \Sigma$M is used

Figure 3.23: Modulation using $\Delta - \Sigma$M and the slew-rate/band-limitation process

3.8 Switching amplifier and filter design

The simulations results presented on the previous sections, showed that the maximum possible bandwidth signal to amplify would be around 2 MHz. However, in order to achieve those 2 MHz bandwidth signal, a high frequency signal had to be amplified up to voltage levels as high as 30 V. As was explained at the beginning of this chapter and showed in Figure 3.1, the switching amplifier has to be driven by the FPGA, the demodulation of the amplified signal has to be performed by a passive filter and the resulting signal has to directly and dynamically supply the voltage of the RFPA. The following section describes the process and criteria used to design and implement the envelope amplifier which is composed by a switching amplifier and a passive filter.

3.8.1 Switching amplifier selection

A switched amplifier consists basically on a transistor, or an array of transistors, that works between cut-off and saturation. The amplification takes place when the transistor is driven by a low voltage signal and its supply voltage is higher in magnitude. However, the driven signal should has enough power to set the amplifier either in cut-off or in saturation. On the other hand, it is important to remark that even when a low voltage signal could goes up to tenths of MHz, like the FPGA output, it is not possible to amplify this signal as much as desired. A rule of thump that describes the restriction is given by the product between the bandwidth and the gain, which is considered as a constant. In this way it is possible either to achieve high frequencies at small gains or

high gains at low frequencies, but not high frequencies and high gains simultaneously.

As was pointed out in the Section 3.2, the driven signal is restricted to be generated by the output of a LED, which does not have enough output power to drive a power transistor. This restriction and the necessity to amplify the signal up to 30 V lead to the selection of an integral solution provided by *Supertex inc.* However, it is important to emphasize that other amplifiers were considered before to make the final decision, but it is difficult to find switched amplifiers that provides high output voltage at high frequencies. Current technologies allow to achieve switching frequencies up to 30 MHz, approximately, for the desired output voltage. The solution here adopted included two integrated circuits: A *high-speed dual MOSFET driver* model MD1211 and an *N-and P-Channel MOSFET pair* model TC6320.

Concerning the MOSFET driver, the more highlighting are:

- 10 ns average rise and fall time with 1000 pF load
- 2.0 A peak output source/sink current
- 1.8 to 5.0 V input CMOS compatible
- 4.5 to 13 V total supply voltage
- Dual matched channels
- Reduced clock skew
- Low input capacitance

On the other hand, the MOSFET pair exhibit the following main characteristics:

- Low threshold
- Low on-resistance
- Low input capacitance
- Fast switching speeds
- Free from secondary breakdown
- Low input and output leakage

- Independent, electrically isolated N- and P-channels

Further and specific details can be found in [60] and [61] respectively.

3.8.2 Filter design

After the simulation results showed in previous sections, it was clear that due to particular restrictions (FPGA clock speed and commutation time for PA) the maximum possible bandwidth signal to recover, when PWM and $\Delta-\Sigma$M is used, would be around 2 MHz. Therefore, in the filter design this cut-off frequency was considered. The filter design was mainly carried out using the tool *Filter solutions* from *Nuhertz technologies* available at [62] in combination with *Cadence Design system* v16.3.

Before giving the filter design's details, it is worth mentioning that it is required to have a flat response in the passband, otherwise, the demodulating process would introduce distortions in the amplification process. On the other hand, the rejection band has to be high enough to eliminate the switching noise, as well as the carrier frequency when PWM is used. This fact led to select a Butterworth filter which offers the maximum flat response until the cut-off frequency. On the other hand, the selection of the cut-off frequency and the order of the filter were a trial-and-error processes because, a priori, the difficulty to remove the unwanted spectral noise was unknown.

The estimation of the input and load impedances was one of the main difficulties regarding the filter design. The filter synthesis software used allows modifying these impedances considering them as purely resistive. However, this is not the case in none of them, instead they are impedances whose values depend on factors like temperature, driven signal and supplied voltage among others. In any case, this impedance had to be estimated and considered as purely resistive, otherwise the filter design becomes very complex. On the other hand, if this impedance was not taken into account, the implementation would have yield very different results compared to the ones observed during the simulation design. This was the case of the first filter design, where a rough estimation of the impedance was done based on the data sheets and it turned out to be very different.

To estimate the input drain impedance of the RFPA, or load impedance of the filter, the device was driven by a 16-QAM signal modulated at 2 GHz and exhibiting a 5 MHz bandwidth. Its voltage supply was dynamically provided by a linear and low efficient amplifier in order to reproduce a realistic scenario. Under these conditions, the voltage and the current consumption of the RFPA were measured and this way

the input drain impedance could be estimated by the ratio of these two. The realized measurements showed that the drain impedance was almost resistive with a value around 120 Ω.

On the other hand, the estimation of the SPA's output impedance, or filter's input impedance, was carried out using an external resistor. The idea used to estimate this impedance is illustrated in Figure 3.24. The SPA could be modeled as an ideal signal generator and an output resistor (R_{gen} in the figure). If an arbitrary load is placed at the output, then the output voltage of the ideal signal generator is going to be distributed between both resistors.

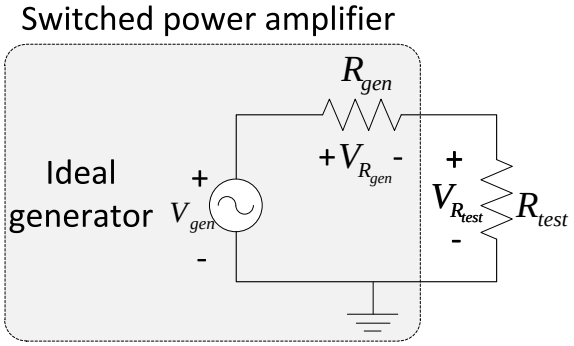


Figure 3.24: Scheme to estimate the output impedance of the SPA

Then the SPA's output impedance (R_{gen}) is estimated by the following relation:

$$R_{gen} = \left(\frac{V_{gen} - V_{R_{test}}}{V_{R_{test}}} \right) R_{test} \tag{3.13}$$

The load resistors (R_{test}) varied from 50 Ω up to 330 Ω because the output impedance is expected to be low. Moreover, since the output impedance could vary with the frequency, different frequencies were included also in the estimation. The measurements showed that the output impedance was almost resistive and constant in frequency exhibiting a value around 25 Ω.

To analyze the influence of the changes in the input and load impedances of the filter, a parametric simulation was performed using the *Cadence Design system* tool. This type of simulation allows to visualize the influence of the changes in one parameter of the circuit. For example, consider the 8^{th} order filter showed in Figure 3.25.

A parametric simulation was performed varying the input impedance from

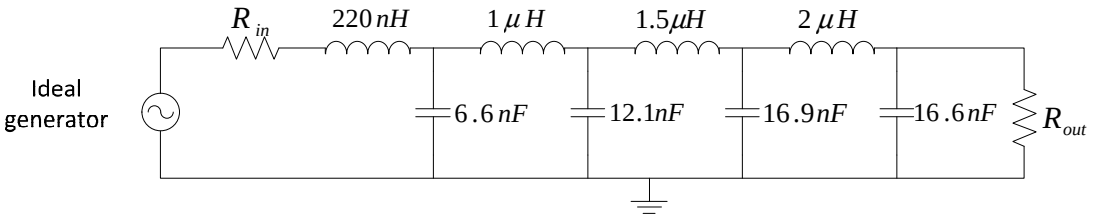
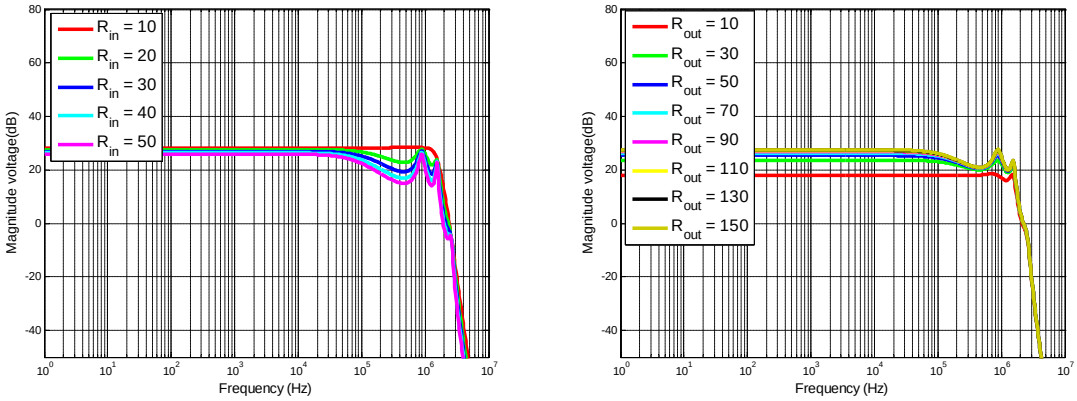


Figure 3.25: An 8th order filter circuit schematic



(a) Parametric simulation of the input impedance. $R_{out} = 120$

(b) Parametric simulation of the output impedance. $R_{in} = 25\Omega$

Figure 3.26: Parametric simulation for an 8^{th} order filter

10 Ω to 50 Ω at steps of 10 Ω while the other components kept the values showed in the Figure 3.25 (output impedance remained at 120 Ω). Similarly, a parametric simulation was performed varying the load impedance from 10 Ω to 160 Ω at steps of 20 Ω while the input impedance remained at 25 Ω. The results are shown in Figures 3.26a and 3.26b respectively. Note that in both simulations, changes in both impedances produce changes on the frequency response of the filter. Moreover, notice that in some cases the flat response of the filter is reduced to few KHz.

Although the filter depicted in Figure 3.25 exhibits drastic changes when the input/output impedance is altered, it has to be emphasized that there is more than one possible solution when a filter is designed. In other words, there exist more than one possible combination of inductors and capacitors to achieve a similar, or the same, frequency response. This gives some flexibility to the final design. However, usually component's values indicated by the filter synthesis software are not the nominal ones; therefore modifications over the design have to be done in order to implement the filter, not to mention the error associated to the values of the components to assemble the circuit. All these factors make the design and implementation of the filter for a switching envelope amplifier a difficult task.

One of the assembled printed circuits is shown in Figure 3.27. In this picture it can be appreciated the SPA (integrated by the IC *MD1211* and the *TC6320*), an 8^{th} order filter and the attenuation network to sample the amplified envelope using the FPGA. Voltage regulators are also included as protection. For space reasons, others implemented designs have not been included in this section. Nevertheless, the simulations of these filters as well as their components are listed in Appendix E.

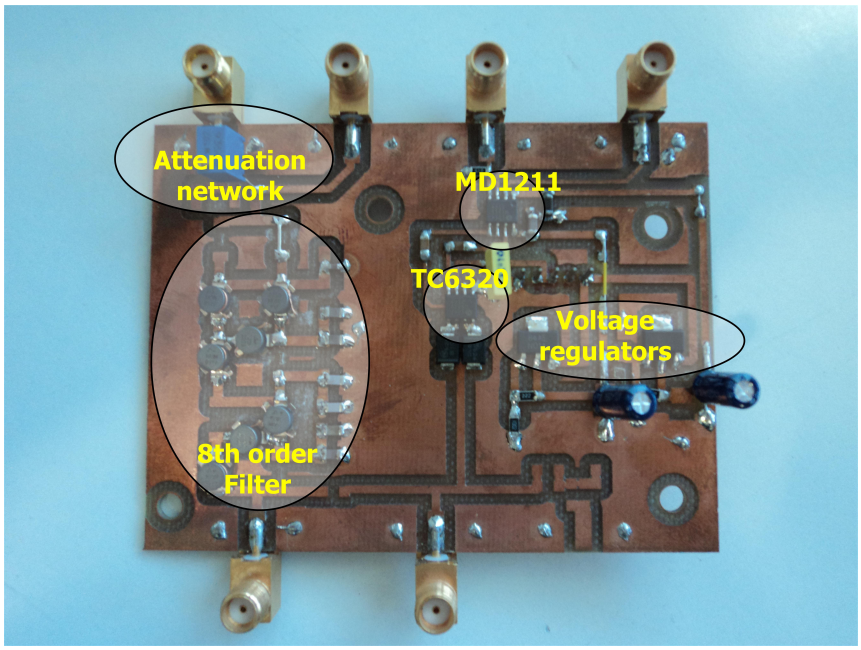


Figure 3.27: Photo of a assembled printed circuit including the SPA and 8^{th} order demodulation filter

3.9 Sampling I-Q components at IF and image spectrum suppression at RF

The restriction of the number of input/output ports of the FPGA explained in Section (3.2) led to the necessity to sample the I-Q components at IF. To do so, one possible solution is to transmit the I-Q components at base-band, perform the up conversion to Radio Frequency (RF) using a local oscillator (LO) at a frequency f_{LO}, and then use a second LO at frequency $f_{LO} - f_{IF}$. However, this solution could lead to undesired rotations in the constellation. Another possible solution is to transmit the I-Q components at IF and perform a mathematical operation such that the upper/lower sideband is kept and the lower/upper sideband is suppressed. This approach could be implemented either by hardware or software. In the first case, usually there is not a complete suppression unless the used components are perfectly matched. On the other hand, the second alternative not only allows to perform the suppression of

the image spectrum but also to correct any possible misadjustment in the modulation path. Moreover, since the FPGA was already considered as part of the design, a cheap and flexible solution was the implementation of the RF image spectrum suppression by using the software approach.

3.9.1 Mathematical formulation

The RF image spectrum suppression consists of performing a mathematical artifice to create two I-Q dependent functions modulated at IF such that when those signals go into the I-Q modulator just one sideband appears at the output. This procedure is graphically depicted on Figure 3.28

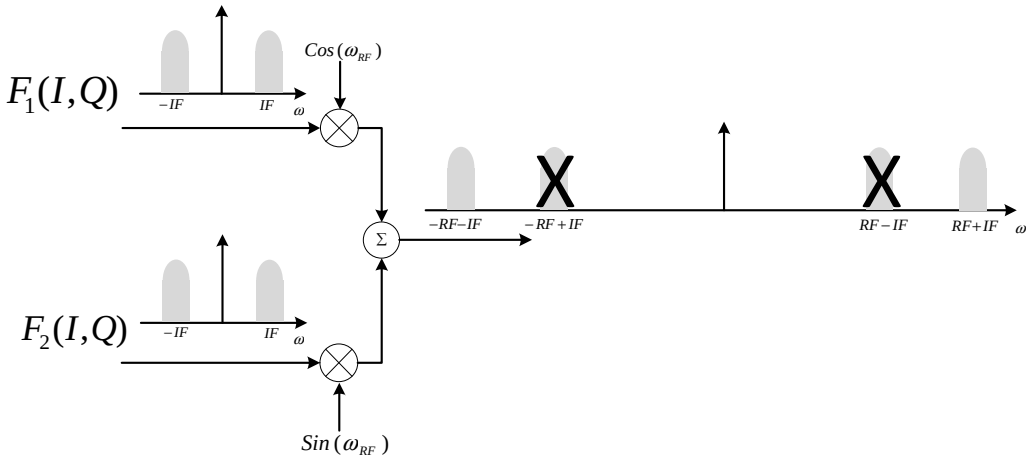


Figure 3.28: Principle of the RF image spectrum suppression

The mathematical artifice consists in adding a phase to one of the I-Q modulator input signals. This process and the mathematical computation involved, is better depicted using a scheme. The Figure 3.29 shows the complete process to achieve the image spectrum cancellation. Initially the I-Q components are at base-band. One path modulates the I-Q components at IF using a common I-Q modulator. On the other hand, the second path introduces a phase shift previously to the I-Q modulation at IF. At this point, there are two I-Q-dependent signals modulated at IF whose are modulated to RF using an I-Q modulator once more.

The image spectrum at RF is cancel out when the proper phase is introduced in one of the I-Q paths. If signals are seen as phasors, it is easy to deduce that the required phase shift is 90^{o} in Figure 3.29. Intruding this phase the lower sidebands of the output spectra are going to be added in-phase, while the upper sidebands are going to be added in counter-phase and therefore disappearing from the spectrum.

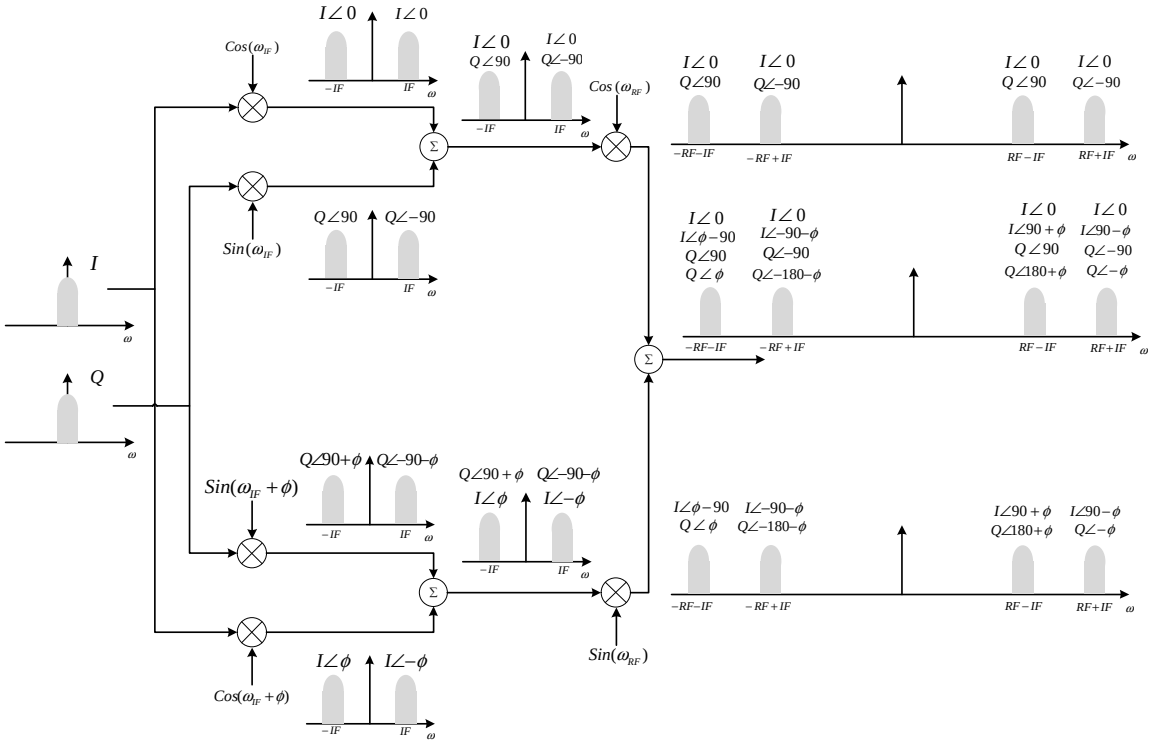


Figure 3.29: Complete diagram of the RF image spectrum suppression

3.9.2 Implementation on the FPGA

The FPGA implementation was realized following the mathematical formulation described in the previous section. However, two main difficulties where found at this stage. In the first place, the up-converter did not have exactly 90^{o} phase shift to modulate the I-Q components. As a consequence, the suppression of the image spectrum was not complete at the output of the modulator. This difficulty was overcome introducing a variable phase shift before the IF modulation and then, by using a spectrum analyzer, this phase shift was tuned until finding the value that better suppress the desired band of the RF spectrum. At this point it has to be emphasized that the resolution of the FPGA used to introduce the phase shift change played an important role, since fine tuning was necessary to compensate the small phase misadjustment.

In the second place, the up-converter limited the bandwidth of its input signal. This imposed restrictions on the frequency used to modulate at IF. Such restriction on the IF also implies a reduction on the maximum base-band bandwidth to modulate, because this bandwidth is then limited to be at most twice the IF. However, in practice it is not feasible to reach this limit because when the demodulation is performed, a digital filter has to remove the IF carrier. If this carrier is too close to the base-band signal, a higher order low pass filter would be required to recover the signal. This led to find the compromise between this two limitations and an IF of 3.75 MHz and

a bandwidth of 5 MHz at IF was chosen, which is a realistic bandwidth for current standards.

A block diagram of the implemented module to remove the image spectrum at RF is shown in Figure 3.30. Notice that the phase is introduced using a complex multiplication. The phase, initially represented in the polar format, is converted to Cartesian representation in MATLAB and then a shared memory is used to transfer this value and perform the complex product in the FPGA.

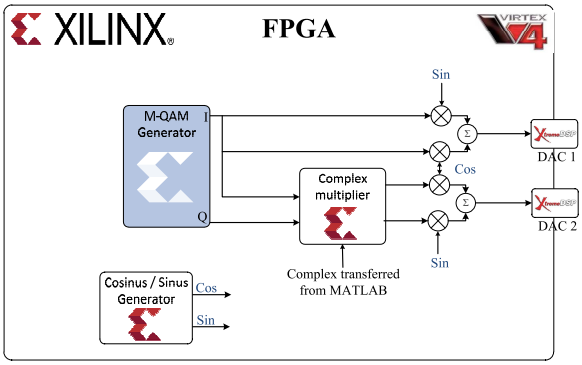


Figure 3.30: Block diagram of the implemented RF image spectrum suppression

Chapter 4

Measurements and experimental results

The restrictions mentioned in previous chapters (number of FPGA I/O ports, FPGA clock speed, etc.) and the proposed solutions to overcome each difficulty led to the scheme shown in Figure 4.1. Concerning the FPGA programming, the blocks depicted in gray represent the implemented blocks. Those include Cartesian-to-polar conversion to detect the envelope of the signal, the modifications over the slew-rate reduction algorithm (bandwidth limitation), the modulation using PWM and $\Delta-\Sigma$M, the process to suppress the RF image spectrum, and the demodulation to base-band.

Concerning the hardware shown in Figure 4.1, the implementations realized in this project include: the envelope amplifier (constituted by the switching amplifier and the passive filter) to amplify the envelope, and the attenuation network to sample the signal using the FPGA. On the other hand, the Up-converter and Down-converter were deployed and configured according with the necessities of this project.

Besides the tests presented in the last chapter, in order to ensure the correct functioning of each part, further verifications were performed before connecting all the parts of the final testbed. This chapter addresses these tests and their results as well as the fgures obtained once all the parts of the testbed are interconnected.

4.1 Testing the image spectrum suppression at RF

In order to test the implementation of the image spectrum suppression, a 16-QAM signal was generated using the FPGA. As described in Section 3.9, the generated signal

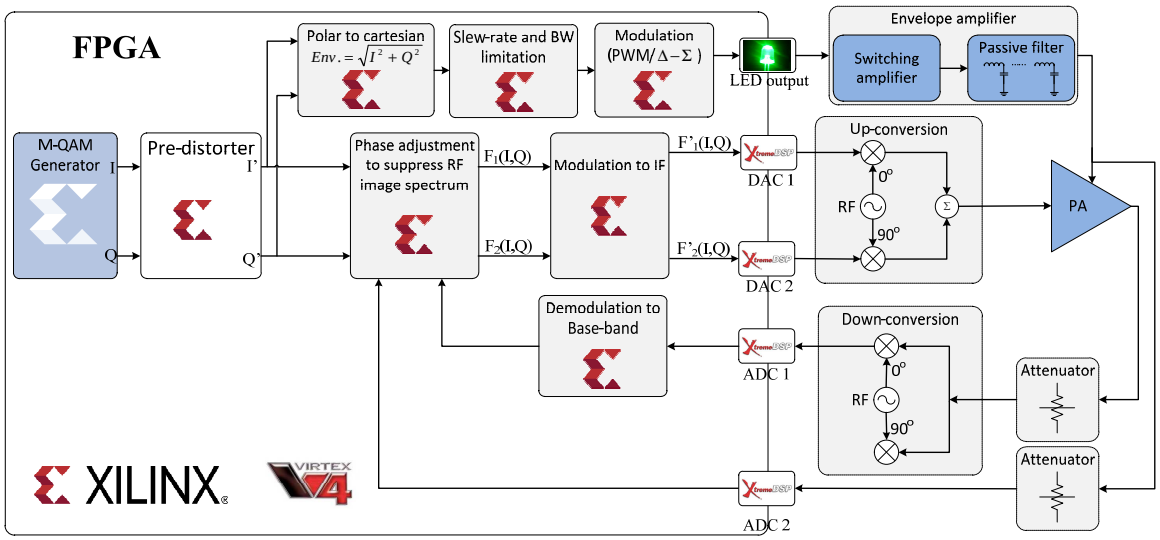


Figure 4.1: Block diagram of the implmented ET transmitter

had 5 MHz bandwidth at IF, that is, 2.5 MHz bandwidth at base-band. The IF was set to 3.75 MHz which gives a 1.25 MHz gap between 0Hz and the beginning of the signal in the spectrum. The up-converter TRF372017EVM (see Section 3.2) was used to modulate the signal using a 2 GHz carrier translating the spectrum as Figure 4.2 shows.

The RF image spectrum suppression was an *try and error* process since the misadjustemt of the I-Q modulator was unknown: A spectrum analyzer was employed to visualize the spectrum while the phase shift was tuned manually. The phase shift that better canceled the image spectrum was 92.5^{o}, which means that there was 2.5^{o} misadjustment on the I-Q modulator. Figure 4.3 shows the resulting spectrum once the phase compensation was introduced, as well as the channel power of the preserved band. As observed in Figure 4.3, the maximum channel power achieved without any distortion introduced by the up-converter was around -24 dBm.

It is important to mention that further improvements can be reached over the band suppression showed in Figure 4.3. This improvement could be achieved using a higher bit-resolution to introduce the phase shift compensation. In the results presented here, a 14-bit fixed-point signal with the binary point at the position 13 was considered.

Without any amplification, the signal shown in Figure 4.3 was demodulated using the dow-converter model TRF371125 (see Section 3.2) in order to evaluate the linearity of the process. Ideally, no additional distortion should be added in the process of up and down conversion. The resulting AM/AM characteristic is shown in Figure 4.4 in red. The ideal input-output characteristic is shown in blue, which exhibits a

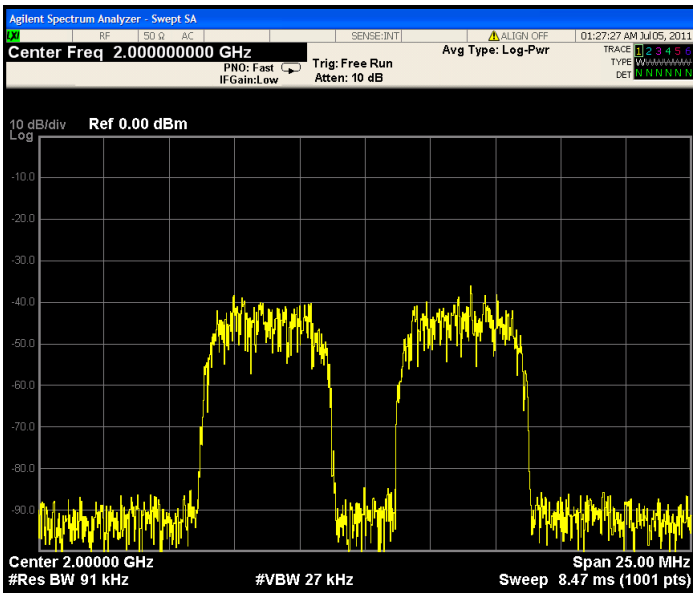


Figure 4.2: Spectrum of a 16-QAM signal without RF image spectrum suppression

perfect correspondence. Notice that the red curve is as straight as the ideal, this implies that there is no non-linear distortion on the process and there is no saturation of any device. On the other hand, it is notable that the received signal is thicker than the ideal one. This phenomenon is caused by memory effects and can be compensated using an equalizer to compensate for this linear distortion..

4.2 Testing the envelope amplifier

Before using the envelope amplifier as the RFPA's voltage supplier, the design was tested without load. Subsequently, a 100 Ω resistor was used to emulate the RFPA impedance. The envelope was generated by the FPGA using a 16-QAM signal exhibiting 2.5 MHz bandwidth at base-band. Before to use either PWM or $\Delta - \Sigma$M, the envelope was processed using the procedure described in section 3.7 (slew-rate and bandwidth reduction). In the following section, the experimental results and the problems faced during this test are fully described.

4.2.1 Implementation using Pulse Width Modulation

Setting the FPGA clock at 60 MHz, the envelope amplifier was driven by a PWM signal. Figure 4.5 shows the amplification when no load is connected to the SPA. As observed, the amplifier is able to follow all the pulses generated by the FPGA. Nevertheless note that the maximum output voltage achieved was 15 V because when

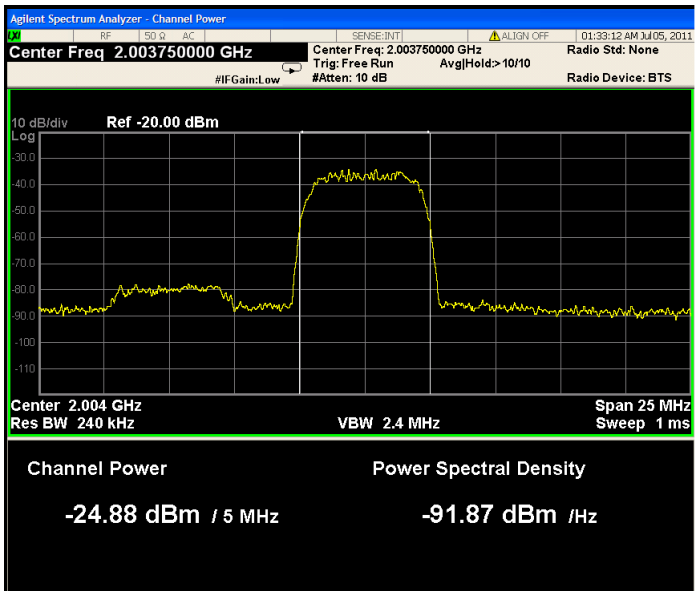


Figure 4.3: Channel power in the non-suppressed spectrum

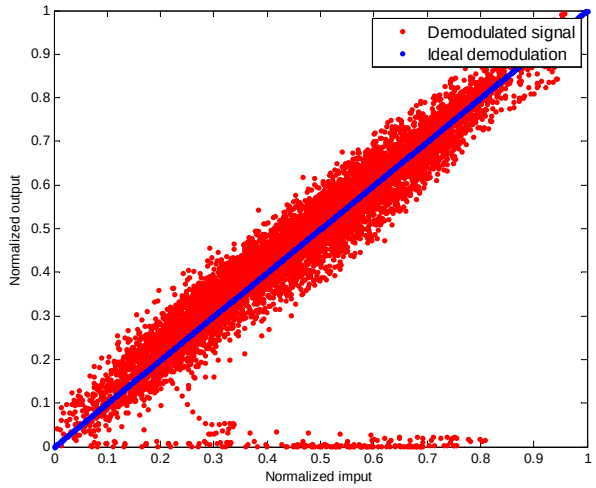


Figure 4.4: AM/AM curve for up and down conversion without RF amplification

higher values were attempted the amplifier melted down. The amplified signal exhibits high variations during the commutations due to the intrinsic transient response and the absence of load. However, the markers placed on its average indicate that the voltage value is 15 V for the amplified signal and around 2.2 V for the signal generated by the FPGA.

The markers placed in Figure 4.5 indicate the duration time of the shortest pulse in the depicted burst. Note that this value is around 62 ns, forcing the SPA to commute between *turned-on* and *turned-off* and vice-verse, in this fraction of time. This condition is considerably relaxed when the FPGA clock speed is lowered to 20 MHz (and keeping the whole configuration used at 60 MHz); in this case the PWM

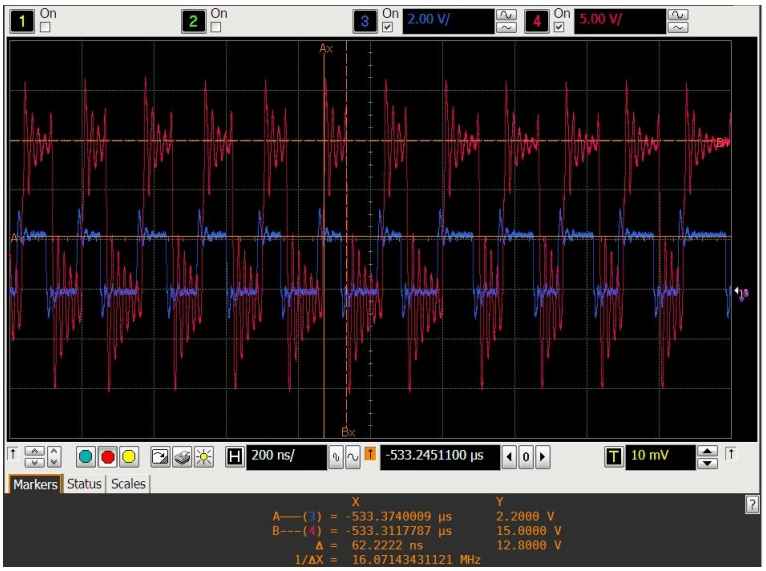


Figure 4.5: Amplification of the PWM signal generated by the FPGA running at 60MHz. No load placed

carrier is lowered to 2 MHz as well. As Figure 4.6 shows, the narrowest pulse is around 100 ns, which gives more time to the SPA's transient response to disappear.

Figure 4.6: Amplification of the PWM signal generated by the FPGA running at 20MHz. No load placed

Once tested the amplification of the signal generated by the FPGA and studied the maximum possible amplification, the next step was to test the demodulation of the signal. Setting the FPGA clock speed to 60 MHz, an analog low pass filter with 1.5 MHz cut off frequency and a 100 Ω resistor were placed at the output of the amplifier. The output signal is shown in Figure 4.8 in color red. For explanatory purposes this Figure also shows the original envelope of the signal (in blue) and the slow envelope (in yellow) that were generated by the DACs. Notice that the demodulated signal

does not follow accurately the modulating signal (slow envelope): at certain points the demodulated signal is located above, which implies an undesired reduction of the efficiency in the envelope tracking architecture. However, the worst problem arises when the demodulated signal is below the slow envelope, as occurs in the highlighted points. In this case, the RFPA would attempt to produce an output greater than its supply voltage and non-linear distortion would occur in the RF signal due to saturation, which is going to be manifested as spectral regrowth in the signal spectrum.

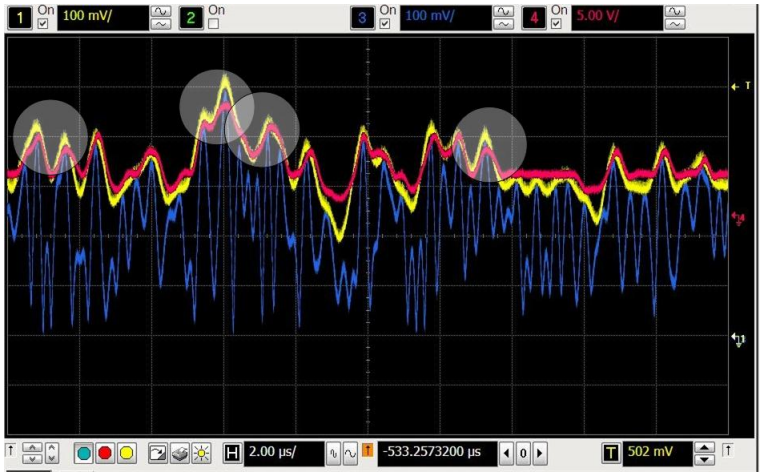
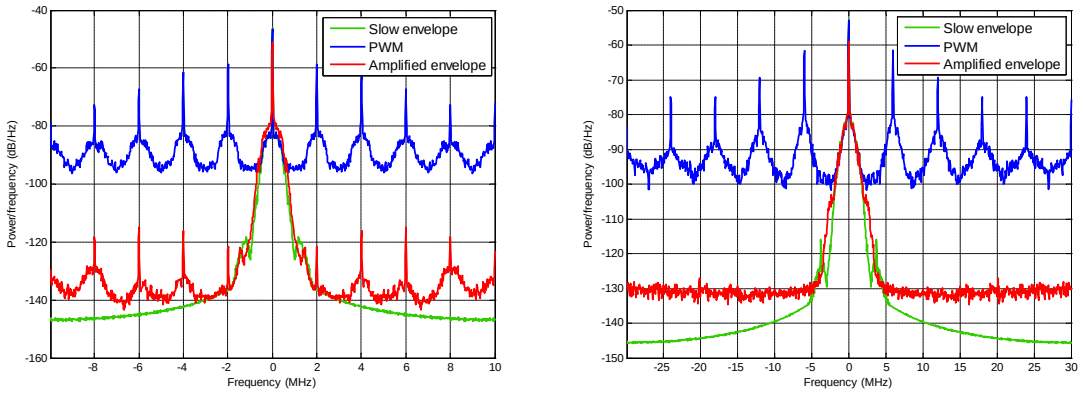


Figure 4.7: Slew-rate/band-limited signal and its amplification using PWM. FPGA working at 60MHz,

The problem of having the demodulated signal below the original envelope cannot be solved lowering the clock speed of the FPGA. As Figure 4.8 shows, even when using a 20 MHz clock the recovered signal does not follow accurately the modulating signal. In fact, in this last case the demodulated signal seems to be worse than the recovered when 60 MHz clock speed was used. The reason of this phenomenon is the frequency response of the filter used to perform the demodulation.

Figure 4.8: Slew-rate/band-limited signal and its amplification using PWM. FPGA working at 20MHz,

If the filter used to perform the demodulation is selective enough and provides high attenuation in the rejected band, then the recovered signal will resemble the original slow envelope. For the shown previously cases, the amplified signals where recovered using the FPGA. The amplified envelope was attenuated and then sampled using one ADC. Results are shown in Figure 4.9a and Figure 4.9b. Notice that in the case of using a clock of 20 MHz the analog filter is not able to attenuate completely the replicas of the PWM carrier. These frequency components introduce distortion that can be appreciated in the time domain, therefore the demodulated signal is unable to follow the changes of the original signal. On the other hand, the filter used in the demodulation when the PGFA clock speed was set to 60 MHz FPGA, attenuated good enough those carrier replicas. In summary, it could be stated that to obtain better results an accurate and selective filter has to be used while having a clear bandwidth limitation in the modulating signal.



(a) Using PWM and FPGA at 20MHz

(b) Using PWM and FPGA at 60MHz

Figure 4.9: Spectrum of the amplified envelope captured by the FPGA when PWM is used

It is worth mentioning that when the FPGA clock speed was lowered to 20 MHz the 16-QAM signal was kept with a 2.5 MHz bandwidth at base-band. Such change was done aimed to show the reduction in efficiency. Notice that in the case of 60 MHz clock speed, the slow envelope tries to follow the envelope changes faster, which is not the case when a 20 MHz clock speed is used. This influences directly on the efficiency of the whole system. Remember that ideally the envelope amplifier should be able to follow accurately the rapid changes of the envelope. However, current technology limitations do not allow performing such task leading to use a slower version of the envelope, as a possible solution, to perform the envelope amplification.

4.2.2 Implementation using Delta-Sigma Modulator

A similar procedure to the used for for testing the PWM was performed in this section, but using the $\Delta - \Sigma$M on the slow envelope. However, the results were different because by setting the FPGA clock speed at 60 MHz, the envelope amplifier was unable to amplify the signal generated by the Delta-Sigma modulator. Moreover, the clock speed had to be reduced up to 20 MHz since the amplifier was unable to follow higher frequencies. Figure 4.10 shows the amplified signal in red, while the $\Delta - \Sigma$ modulated signal generated by the FPGA is shown in blue. As can be observe in this figure, the duration of the pulses can be as short as $533\mu s$, that is, the equivalent to a 20 MHz signal. In other words, the pulses generated by the Delta-Sigma modulation can be as short as the maximum FPGA clock speed. This is the reason why the amplifier was unable to amplify the signal when the FPGA clock speed was set to 60 MHz, because this implies commuting at $t = 1/60MHz = 16ns$.

The data-sheet of the switched amplifier [61] (integrated circuit TC6320) specifies that the *Turn-off delay time* is 20 ns, while the *fall time* is 15 ns. This means that it is required, at least, 35 ns to switch-off the device, or equivalently the device can follow a signal exhibiting a maximum frequency of $f = 1/35$ ns $= 28$ MHz. However, this is an estimated limit because when the amplifier was used for the PWM under a FPGA clock speed of 60 MHz, (see red signal in Figure4.5) the transient response is notable when the amplified pulse is equivalent to a 16 MHz signal.

Figure 4.10: Amplification of the $\Delta - \Sigma$M signal generated by the FPGA running at 20MHz. No load placed

Despite of the limitation on the switching frequency, the demodulated signal followed very well the demodulating signal. Figure 4.11 shows the demodulated signal

(in red) when the filter and the 100 Ω resistive load are placed at the output. The slow envelope is shown in yellow while the original envelope is shown color blue. Notice that compared to the results obtained in the PWM, the demodulated signal follows much better the modulating signal. It should be emphasized that for a better comparison, the filter employed here was the same used when the PWM signal was driven the SPA at 20 MHz FPGA speed clock.

Figure 4.11: Slew-rate/band-limited signal and its amplification using $\Delta - \Sigma$M. FPGA working at 20MHz

Figure 4.12 shows the spectrum of the amplified envelope captured by the FPGA. Notice that the recovered signal spectrum is "cleaner" than the recovered when PWM is used even when it was used the same filter. This coincides with the theory which states that the filter condition is relaxed in $\Delta - \Sigma$M compared with PWM, because the switching noise is pushed to higher frequencies. Moreover, there is no presence of carrier replicas as occurs in the PWM, avoiding additional distortions in the time domain.

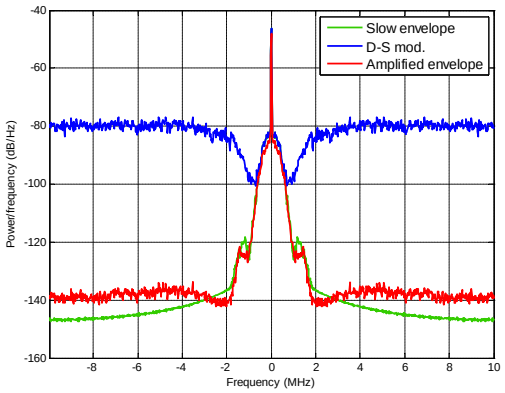


Figure 4.12: Spectrum of the amplified envelope captured by the FPGA when $\Delta - \Sigma$M is used

4.3 Experimental results employing the complete testbed

According to the results obtained using PWM and $\Delta - \Sigma$M it can be stated that the later offers better performance if the criteria is based on the similarity between the modulating and the demodulated signals, or even more critical, if it is desired to avoid that the demodulated signal goes below the original envelope. Nevertheless, it has to be remembered that a switching amplification and envelope reduction is aimed to allow efficient envelope amplification. This was the criteria when the final measurements were acquired, and therefore the PWM at 60 MHz clock speed was used.

After interconnecting all the parts of the Envelope Tracking, the next step was to synchronize the envelope and the RF signals. This step is critical, as was mentioned in Section 2.2.2.1. The alignment was performed using the *Agilent Infinium* oscilloscope model DSO90404A which allows visualizing signals at 2GHz frequency. Figure 4.13 shows the envelope and the RF signal once the signals were synchronized.

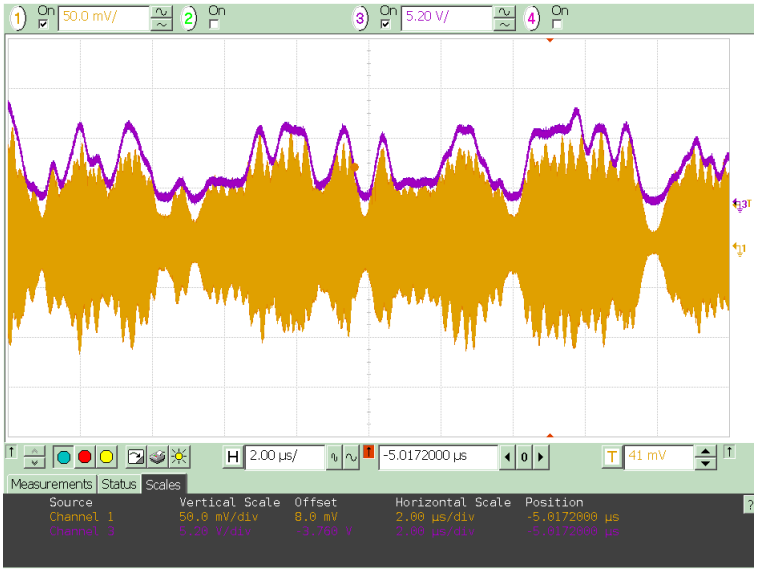
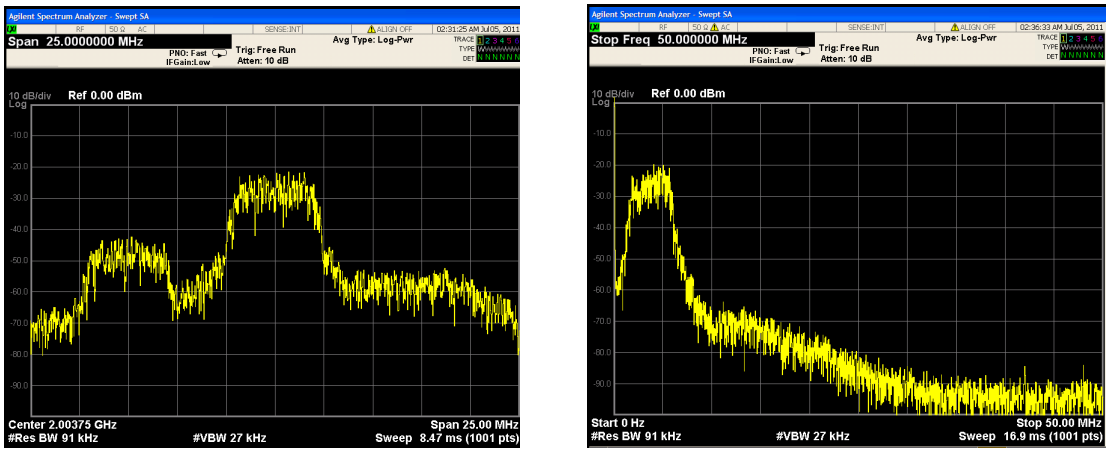


Figure 4.13: Synchronization of the slow-envelope and the RF signal

As can be observed in Figure 4.13, the envelope is always above the RF signal. However, notice that the scales are not the same for both channels, in fact, the envelope has amplitude bigger than the RF signal, but the scales were set for explanatory purposes. By having an envelope much bigger than the RF input signal, the Envelope Tracking architecture is not efficient. As mentioned in Section 2.2 the RFPA works efficiently when works close to the compression point. To bring the RFPA to this point, the output power of the FPGA was increased gradually up to the point when spectral regrowth starts to appear. Besides, it has to be pointed out that there exist spectral regrowth caused by the dynamic supply when considering the slow envelope as well



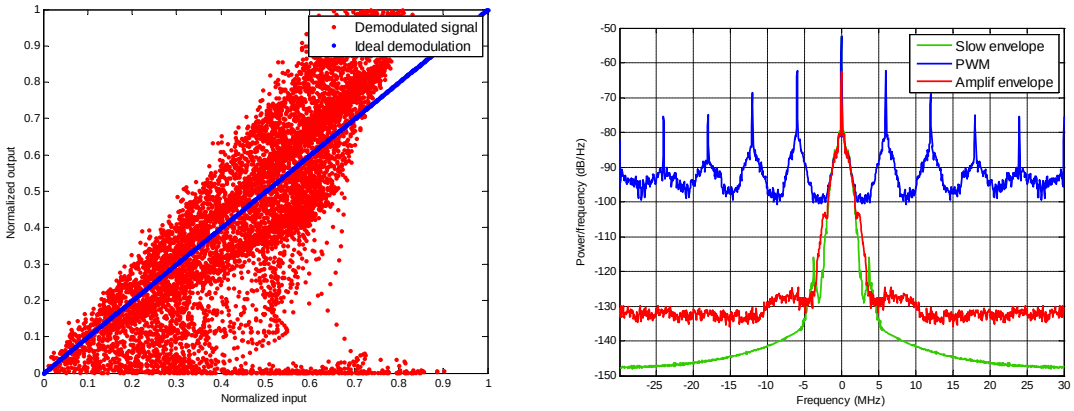
(a) Saturation of the RFPA (b) Spectrum of the RF-demodulated signal

Figure 4.14: Spectrum of the transmitted/received signal

(see Section 2.2.2.1). However, when operating above the compression point is crossed, the spectral regrowth increases much more. This phenomenon can be appreciated in Figure 4.14a. Notice that even the suppressed image RF spectrum has appeared when operating beyond the compression point.

Since DPD can compensate for the distortion introduced by the dynamic supply, the amplitude of the RF signal was set in such way that the RFPA is kept away from the its compression point. This signal was first demodulated to IF using the I-Q demodulator, as Figure 4.14b shows, and then demodulated to base-band using the FPGA.

The AM/AM curve of the demodulated signal is shown in Figure 4.15a in red, whereas the ideal AM/AM curve is shown in blue. Note that in this case the resulting curve is wider than the curve obtained when the up-conversion/down-conversion is performed with no amplification of the RF signal (see Figure 4.4). This difference is caused partially by the non-linearity of the RFPA and partially for the distortion introduced by the dynamic supply (see Section 2.2).



(a) AM/AM curve for up and down conversion with RF amplification

(b) Spectrum of the amplified envelope (using PWM)

Figure 4.15: Data acquired by the FPGA

On the other hand, the amplified envelope was simultaneously sampled by the FPGA. Figure 4.15b shows the spectrum of the amplified envelope in red. The slow envelope is shown in green and the PWM signal generated by the FPGA in blue. Note that besides using the same filter used during the tests with the resistive load, there is a slightly change on the frequency response of the filter, which may be produced by differences between the real and the estimated input and output impedances.

Chapter 5

Conclusions and future work

In this project the complete procedure followed on the design and implementation of an envelope tracking transmitter has been described. The amplification of the envelope has been done using a class S amplifier (SPA followed by a passive low pass filter) and signal processing techniques to reduce the slew-rate and bandwidth characteristics of the envelope have been included to allow its amplification using SPAs.

The slew-rate reduction of the envelope was performed using the algorithm described in [1]. However the spectral characteristics of the signal generated by this algorithm do not allow a straightforward amplification using switching techniques. Instead, it was found that an unclear spectral limitation does not allow recovering considerably well the signal once the PWM or $\Delta - \Sigma$M demodulation is performed. Therefore, an algorithm to reduce the bandwidth of the envelope was developed to overcome this difficulty. As consequence, the PWM or $\Delta - \Sigma$M modulated signal was better recovered after its demodulation. Besides the complexity of this algorithm to be implement in a FPGA, its mathematical bases allowed to introduce modifications to the slew-rate reduction algorithm proposed in [1]. These modifications were implemented on the FPGA and made possible the spectral limitation of the envelope that allowed its amplification using SPA.

Two different modulation techniques were evaluated to perform the switching amplification, namely the pulse width modulation and the delta-sigma modulation. This evaluation led to conclude that the $\Delta - \Sigma$M does not require a high order low pass filter to recover the modulating signal. Moreover, this modulation has more than one parameter that determines the quality of the final output signal and therefore offers various possibilities to achieve the desired result. Nevertheless, as counterpart

this modulation needs a fast switching amplifier capable to follow the rapid changes of the modulated signal, imposing in this way a restriction on the bandwidth of the modulating signal. On the other hand, the PWM technique does not generate pulses as short as those generated on the $\Delta - \Sigma$M which facilitate its implementation using switching amplifiers. However, the two main drawbacks of PWM are the compromise between the resolution of the modulation and the proximity of the first replica, and the requirement of a high order filter to recover the modulating signal due to the strong presence of the spectral replicas. In any case, the PWM could be preferred over the $\Delta - \Sigma$M because current technologies in switching amplification do not allow to amplify high frequencies at high output powers. However, the use of the slew-rate and bandwidth reduction algorithm is a solution that can help to cope with the limitations imposed by current switching technologies.

Special attention should be paid to the design of the low pass filter to demodulate the slow envelope. In particular, to the estimation of the input and load impedances, which are highly influential in the final frequency response of the filter. Cut-off frequency require also attention since it is desired to avoid as much noise as possible but also to recover as much bandwidth as possible keeping a flat response in the passband.

Regarding the image spectrum rejection at RF the results suggest that the bit-resolution used to perform the operations play a fundamental role since increasing this resolution implies a finer tune on the compensation of the I-Q modulator's misadjustment.

The further work will be focused in the improvement of the implemented ET at different levels. Concerning the FPGA programming, finding a suitable and low-complex way to implement the bandwidth reduction algorithm (or an equivalent) could led to find better results in the modulation/demodulation using PWM and $\Delta - \Sigma$M. On the other hand, the presented results could be considerably improved incorporating digital pre-distortion aimed to compensate the distortion introduced by the dynamic supply on the RFPA and the signal processing and amplification suffered by the envelope, as was done in [19].

At hardware level, other alternatives of SPA could be used for the amplification. These alternatives may include the design of a special configuration, as well as trying integrated solutions available in the market.

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APPENDICES

Appendix A

Pulse Width Modulation

The Pulse with modulation technique was simulated using the following MATLAB script in order to estimate quickly and accurately the results expected by the FPGA. The input parameters are:

- f_input: Modulating signal.
- Ts: FPGA clock speed.
- freq_mod: Frequency of the carrier.
- ajust: option that determines if it is desired to adjust the carrier such that the resulting output appears similar like of the input was normalized between 0 and 1 before to be modulated.

On the other hand, the output parameters are:

- f_PWM: Pulse width modulated signal.
- f_carrier: Exact carrier frequency used in the modulation.

```
function [f_PWM,f_carrier]=PWM(f_input,Ts,freq_mod,ajust)

% Translate the carrier frequency into number of samples based on the
% Time Sampling (Ts). If the number of samples does not match exactly,
% then round the freq to the nearest int. towards minus infinite, that is,
% use a freq. slightly higher
N=floor(1/freq_mod/Ts);

% Generate the sawtooth carrier
carrier=linspace(0,1,N);

% Adjust the carrier to match the number of samples of the
% input signal
M=length(f_input)/length(carrier);
carrier=repmat(carrier,[1,floor(M)]);
if rem(length(f_input),length(carrier))~=0
    carrier=[carrier carrier(1:length(f_input)-length(carrier))];
end

% If t is requested, adjust the carrier to produce and output
% similiar to the obtained if the input is normalized between 0 and 1
if ajust==1
    minimum=min(f_input);
    carrier=carrier*(max(f_input)-minimum);
    carrier=carrier+minimum;
    max(carrier)
    max(f_input)
    min(carrier)
    min(f_input)
end

% Compute the modulation
f_PWM=zeros(1,length(f_input));
f_PWM(f_input>carrier)=1;

% Notify the actual carrier frequency used
f_carrier=1/N/Ts;
end
```

Figure A.1: PWM algorithm

Appendix B

Delta Sigma modulation

The following script implements a first and second order Delta sigma modulator. A graphical representation of the second order implementation is depicted in Figure 3.9. Higher orders modulators require special design because not all those systems are stable. The inputs for the below listed code are:

- f_input: Modulating signal.
- order: specifies the order of the delta sigma modulator. Could be either order 1 or 2.

On the other hand, the outputs parameters are:

- funcion_DS: Delta sigma modulated signal.

```
function [f_DS,temp]=Delta_Sigma(f_input,order)

% Pre-allocate memory
f_DS=zeros(size(f_input));
temp=zeros(size(f_input));

% Compute a frst order D-S modulator
if order==1
    for i=2:length(f_input)
        temp(i)=temp(i-1)+f_input(i)-f_DS(i);
        if temp(i)>0.6
            f_DS(i+1)=1;
        else
            f_DS(i+1)=0;
        end
    end

% Compute a second order D-S modulator
else if order==2
        temp1=0;
        for i=2:length(f_input)
            temp1=temp1+f_input(i)-f_DS(i);
            temp(i)=temp(i-1)+temp1-f_DS(i);
            if temp(i)>0.6
                f_DS(i+1)=1;
            else
                f_DS(i+1)=0;
            end
        end
    else % If a higher order was request, launch error message
        fprintf('Invalid filter order');
        return;
    end
end
end
```

Figure B.1: Delta-Sigma modulation algorithm

Appendix C

Slew-rate reduction algorithm

Slew-rate reduction algorithm. For a proper functioning the input signal must be normalized. Input parameters:

- delta: Number of divisions considered for going from zero to one in a normalized range.
- f_input: Input signal

On the other hand, the resulting output is:

- Es: Slew-rate limited signal

```
function [S_R_limited]=slow_envelope(f_input,N)
delta=1/N;
S_R_limited=ones(size(f_input))*max(f_input);
for i = 2:length(f_input)-N
    finding=[f_input(i)];
    for j = 1:N
        finding=[finding f_input(i+j)-j*delta];
    end
    [y,indice]=max(finding);
    S_R_limited(i)=max([y S_R_limited(i-1)-delta]);
end
end
```

Figure C.1: Slew-rate reduction algorithm

Appendix D

Bandwidth reduction algorithm

The theoretical bases of this algorithm are presented in Section 3.6.1. For a proper functioning the input signal must be normalized. The inputs parameter comprises:

- f_input: Input signal.
- Ts: FPGA clock speed.
- Alpha: Constant to regulate the influence of the first derivative.
- Beta: Constant to regulate the influence of the second derivative.
- Gamma: Constant to regulate the influence of the third derivative.
- Delta: Constant to regulate the influence of the fourth derivative.
- k: Constant to regulate the influence of the external force.
- BW: Bandwidth limitation f the resulting signal.
- n_averages: Number of averaging on each iteration
- n_iterations: Number of iterations

On the other hand, the resulting output is:

- Es: Reduced bandwidth signal

```
function [Es]=envelope_reduction(f_input,Ts,alpha,beta,gamma,delta,k,BW...
    ,n_iterations,n_averages)
% Compute the number of samples to be averaged
N=1/BW/Ts; if rem(N,2)==0 N=N+1; end
M=floor(N/2);
Es=ones(size(f_input));
for i=1:n_iterations
    % First derivative
    dEs_dt_1=circshift(Es,[0 -1])-Es;
    dEs_dt_2=circshift(Es,[0 1])-Es;
    % Second derivative
    d2Es_dt2=circshift(Es,[0 -1])-2*Es+circshift(Es,[0 1]);
    % Third derivative
    d3Es_dt3=circshift(Es,[0 -2])-2*circshift(Es,[0 -1])+...
        2*circshift(Es,[0 1])-circshift(Es,[0 2]);
    % Fourth derivative
    d4Es_dt4=circshift(Es,[0 -2])-4*circshift(Es,[0 -1])+...
        6*Es-4*circshift(Es,[0 1])+circshift(Es,[0 2]);
    % External force
    F_ext=(Es-f_input);
    % Averaging
    for j=1:n_averages
        Es2=Es-k*F_ext.^2+(alpha*(abs((dEs_dt_1)-(dEs_dt_2)))+...
            beta*(d2Es_dt2)+gamma*d3Es_dt3+delta*d4Es_dt4).*F_ext;
        F_ext=replicate_samples(M,find(Es2<f_input),F_ext);
        F_ext=central_averaging(M,F_ext);
    end
    % Compute the new envelope
    Es2=Es-k*F_ext.^2+(alpha*(abs((dEs_dt_1)-(dEs_dt_2)))+...
        beta*(d2Es_dt2)+gamma*d3Es_dt3+delta*d4Es_dt4).*F_ext;
    % Verify if the new envelope is above the original envelope
    temp2=find(Es2<f_input);
    if isempty(temp2);
        Es=Es2;
    else
        % Else, correct those points
        temp2=temp2(find((temp2>N & temp2<length(Es)-N)==1));
        F_ext=replicate_samples(M,temp2,F_ext);
        temp=central_averaging(M,F_ext);
        for m=1:length(temp2)
            F_ext(temp2(m)-N:temp2(m)+N)=temp(temp2(m)-N:temp2(m)+N);
        end
        Es=Es-k*F_ext.^2+(alpha*(abs((dEs_dt_1)-(dEs_dt_2)))+...
            beta*(d2Es_dt2)+gamma*d3Es_dt3+delta*d4Es_dt4).*F_ext;
    end
end
end
```

Figure D.1: Bandwidth reduction algorithm

```
function [funcion]=central_averaging(N,funcion)
temp_=zeros(size(funcion));
for j=-N:N
    temp_=temp_+circshift(funcion,[0 j]);
end
funcion=temp_/(2*N+1);
end

function [funcion]=replicate_samples(N, location,funcion)
for m=1:length(location)
    if (location(m)>N &&  location(m)<length(funcion)-N)
        funcion(location(m)-N:location(m)+N)=0;
    end
end
end
```

Figure D.2: Bandwidth reduction algorithm (continuation)

Appendix E

Filters implementations and simulations

Following the scheme showed in the Figure E.1, the most important four filters where designed and implemented using the list of components showed in table E.1.

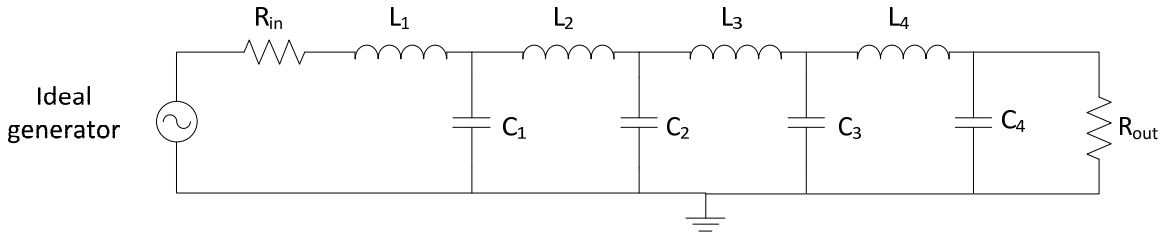


Figure E.1: General schematic considered in the filter design

	Filter 1	Filter 2	Filter 3	Filter 4
R_{in}	10 Ohm	10.00 Ohm	25.00 Ohm	25.00 Ohm
L_1	1.200 uH	220.0 nH	13.30 uH	1.500 uH
C_1	12.00 nF	6.600 nF	1.120 nF	6.600 nF
L_2	1.200 uH	1.000 uH	15.00 uH	6.600 uH
C_2	9.100 nF	12.10 nF	900.0 pF	14.40 nF
L_3	570.0 nH	1.500 uH	11.00 uH	10.00 uH
C_3	2.200 nF	16.90 nF	570.0 pF	16.90 nF
L_4		2.000 uH	4.700 uH	12.20 uH
C_4		16.60 nF	120.0 pF	14.70 nF
R_{out}	10.0 Ohm	120.0 Ohm	120.0 Ohm	120.0 Ohm

Table E.1: Component values for the designed filters

Not all the listed components has commercial value. However combination two, three and even four commercial values allowed the implementation of the filters listed above. The response of the original design for each filter is shown in Figure E.2

However not in all the cases it was consider properly either the input or the output impedance, or in some cases none of them, occasioning a different frequency response in practice than the obtained during the design. To give an idea about the influence of the input and output impedance a parametric simulation was performed

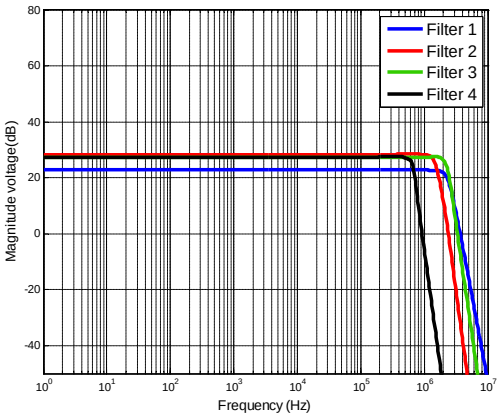
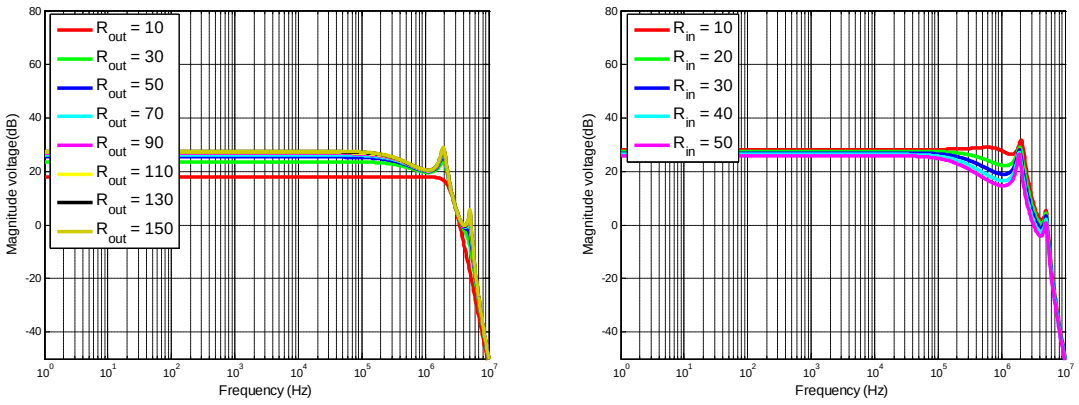


Figure E.2: Original design of the filters

for these five filters. A parametric simulation is a simulation that simulated the behave of a circuit when an specific component change its value. In this case the parametric simulation was performed for a fixed input impedance when the output is varied or for a fixed output when the input is varied. To show a more realistic case, in all the parametric simulations the fixed parameter was either $R_{in} = 25$ or $R_{out} = 120$.

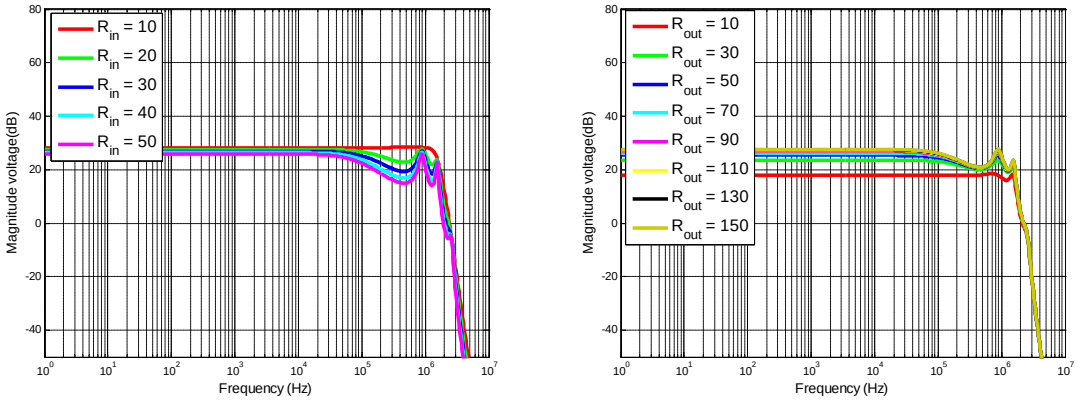
The parametric simulation for the input impedance vary its value from 10Ω to 50Ω at steps of 10Ω while the output impedance remains at 120Ω. On the other hand the parametric simulation for the output impedance vary its value from 10Ω to 160Ω at steps of 20Ω while the input impedance remains at 25Ω.



(a) Parametric simulation for the output impedance

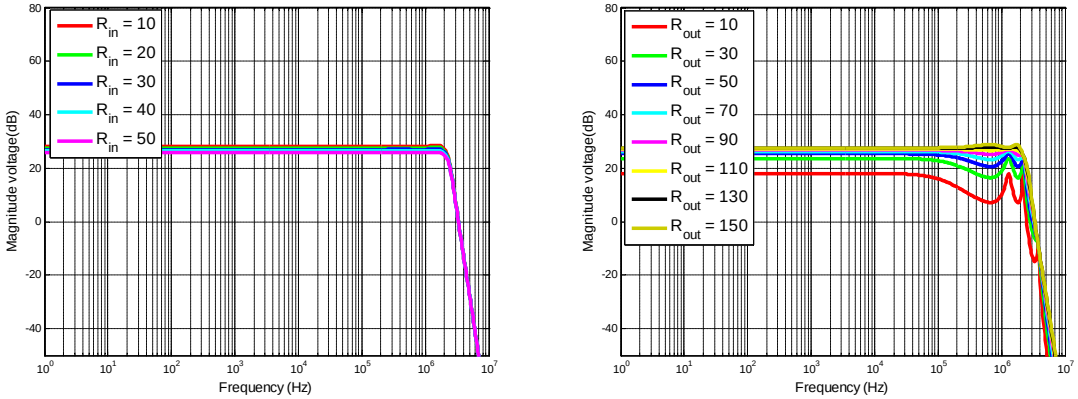
(b) Parametric simulation for the input impedance

Figure E.3: Parametric simulation for Filter 1



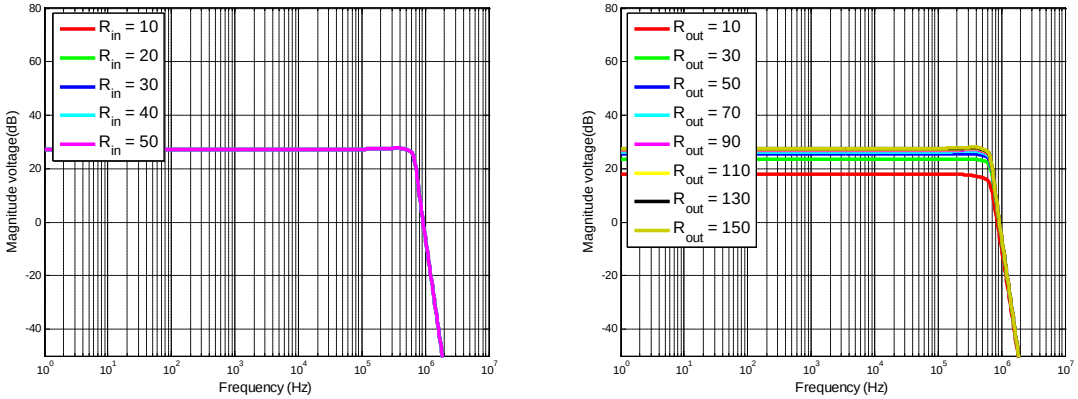
(a) Parametric simulation for the input impedance (b) Parametric simulation for the output impedance

Figure E.4: Parametric simulation for Filter 2



(a) Parametric simulation for the input impedance (b) Parametric simulation for the output impedance

Figure E.5: Parametric simulation for Filter 3



(a) Parametric simulation for the input impedance (b) Parametric simulation for the output impedance

Figure E.6: Parametric simulation for Filter 4