ESCUELA TÉCNICA SUPERIOR DE INGENIERÍA DE TELECOMUNICACIÓN DE BARCELONA

ETSETB

DISEÑO Y REALIZACIÓN DEL SISTEMA DE OSCILADORES PARA UN RECEPTOR DE TELEVISIÓN DIGITAL TERRESTRE (TDT)

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Sumario

El objetivo de este proyecto es explicar todos los pasos necesarios, desde principio a fin, que se utilizan a nivel profesional para el diseño de circuitos electrónicos y de microondas, desde su primera concepción como idea hasta su posterior desarrollo, fabricación y finalmente test y validación.

Para ello se va a realizar la síntesis de diseño de un oscilador local doble de altas prestaciones, utilizando la tecnología que actualmente se nutre la industria electrónica y de telecomunicaciones.

Entre muchas de sus otras aplicaciones, dicho oscilador doble se utiliza comúnmente para implementar receptores profesionales superheterodinos de doble conversión para equipos repetidores y remisores de Televisión Digital Terrena.

Se ha realizado el diseño final de tres osciladores locales basados en bucles PLL. El primero de ellos se utiliza para implementar una frecuencia fija de 30MHz a partir de una referencia externa de 10MHz de gran pureza espectral que comúnmente se encuentra en los centros transmisores procedente de la recepción GPS. Dicha referencia de 30MHz la van a utilizar los siguientes dos osciladores locales para sintetizar frecuencias con buenas prestaciones en ruido de fase que van a utilizarse a posteriori para implementar un receptor complejo de doble conversión.

El primero de los osciladores locales para la doble conversión sintetiza frecuencias de 1GHz a 2GHz con pasos de 5MHz, y se utiliza en el receptor superheterodino para obtener una primera FI elevada y solventar el problema del canal imagen del receptor común. El segundo oscilador local sintetiza frecuencias de 500MHz a 1GHz con pasos de 1MHz y se utiliza para obtener una segunda FI la cual a posteriori va a ser la que se va a demodular y tratar digitalmente en el receptor profesional.

Contenido

Capítulo 1

1. INTRODUCCIÓN TEÓRICA

1.1 TRANSMISIÓN DE SEÑALES DE TV DIGITAL EN EL ESTÁNDAR DVB-T

La Televisión Digital Terrestre viene recogida dentro el estándar denominado DVB-T presente en el documento ETSI EN 300 744 del European Telecommunications Standards Institute. Dicho documento especifica el proceso de codificción del canal y la maodulación del mismo para un correcto funcionamiento de los canales de transmisión terrestre. Al tipo de señal de entrada utilizada se la denomina Trama de Transporte o (Transport Stream) y se estructura multiplexando múltiples programas y añadiendo la información de servicios según la norma ETS 300 468 del ETSI.

A la trama de tranporte TPS se le añade elementos de protección y redundancia para hacerla más robusta debido a las condiciones particulares por donde debe ser transmitida dicha señal. A éste tipo de operaciones se le llama codificación del canal.

Por otra parte, la señal trama de transporte también se modula utilizando un tipo de modulación multiportadora denominada OFDM (Orthogonal Frequency Division Multiplex). El hecho de sumar la modulación con la corrección de errores de la trama se obtiene una señal resultante de transmisión del tipo COFDM (Coded Orthogonal Frequency Division Multiplex).

El estándar define una serie de opciones según la robustez requerida para la transmisión de la señal y la velocidad de los datos. Básicamente las opciones son las siguientes, aunque se van ampliando a medida que se actualiza el estándar:

-Dos modos de transmisión: 2k (1.705 portadoras) y 8k (6.817 portadoras)
-Tres tipos de modulación: QPSK, 16QAM, 64QAM
-Cinco modos de codificación para protección interna de errores: 1/2,2/3,3/4,5/6,7/8
-Cuatro longitudes de intervalo de guarda: 1/4,1/8,1/16,1/32
-Modulación jerárquica o no jerárquica con diferentes valores para alfa 1, 2, y 4.

Una de las grandes propiedades de la señal del tipo COFDM es que puede operar tanto en áreas de cobertura amplias como pequeñas. Dependiendo del caso, la red será del tipo MFN (Multiple Frequency Network) o del tipo SFN (Single Frequency Network). En éste último caso, la recepción es posible cuando se radian idénticos programas desde transmisores o repetidores que operan en la misma frecuencia. En éste caso se obtiene máxima eficiencia del espectro aunque obliga evidentemente a disponer de una sincronización entre los emisores.

En la figura siguiente [1] se muestra el diagrama de bloques funcional del sistema DVB-T.

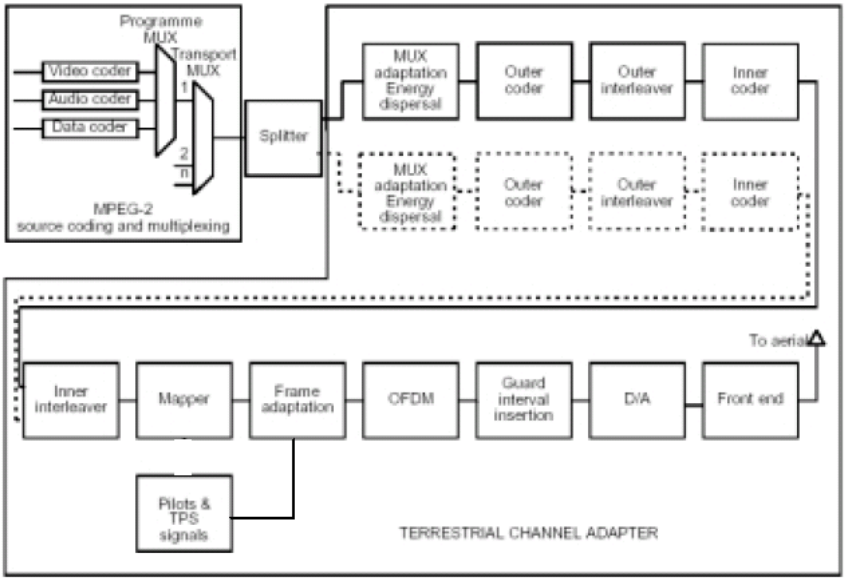


Figura 1. Diagrama de bloques general del sistema DVB-T

Una de las opciones tal y como se ha dicho del sistema DVB-T es la transmisión jerárquica de la señal a transmitir. En éste caso existen dos flujos de transporte TPS, uno de alta prioridad HP y otro de baja prioridad LP. El TPS de alta prioridad se acostumbra a dotar de baja calidad de imagen pero con un modelo de modulación muy robusto del tipo QPSK. En cambio el TPS de baja prioridad se dota con mayor calidad y velocidad de transmisión de datos. A posteriori se combinan los dos flujos para la emisión. En la zona de cobertura donde se reciba bien la señal, eso es con buena relación señal ruido S/N, se recibirá el resultado de la combinación de los dos flujos. En cambio, en zonas de dificil recepción se recibirá la señal solamente correspondiente al flujo de alta prioridad.

1.1.1 SEÑAL TRANSMITIDA

La figura siguiente [2] representa el esquema de bloques de un transmisor típico de DVB-T.

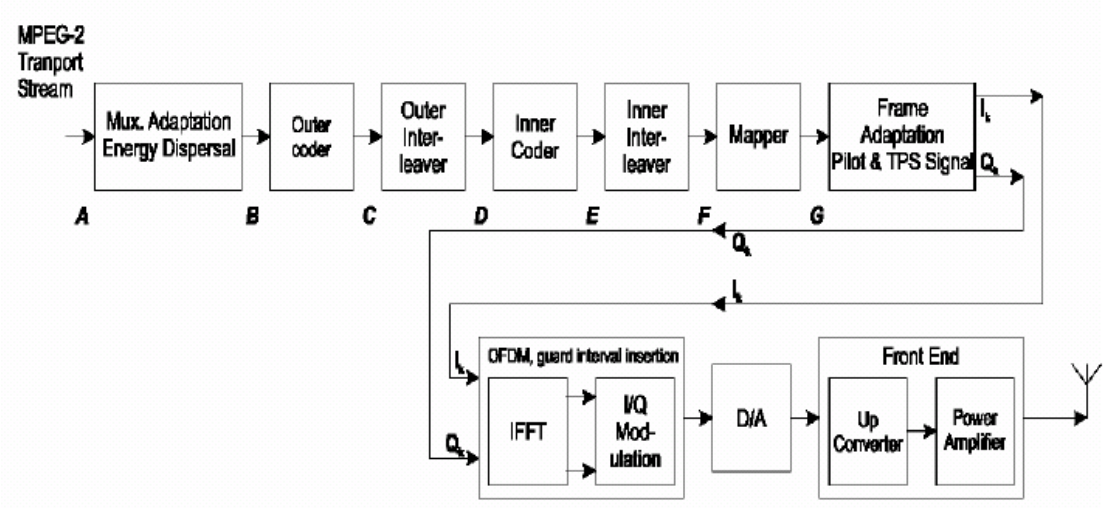


FIGURA 2. DIAGRAMA DE BLOQUES DE UN TRANSMISOR DVB-T

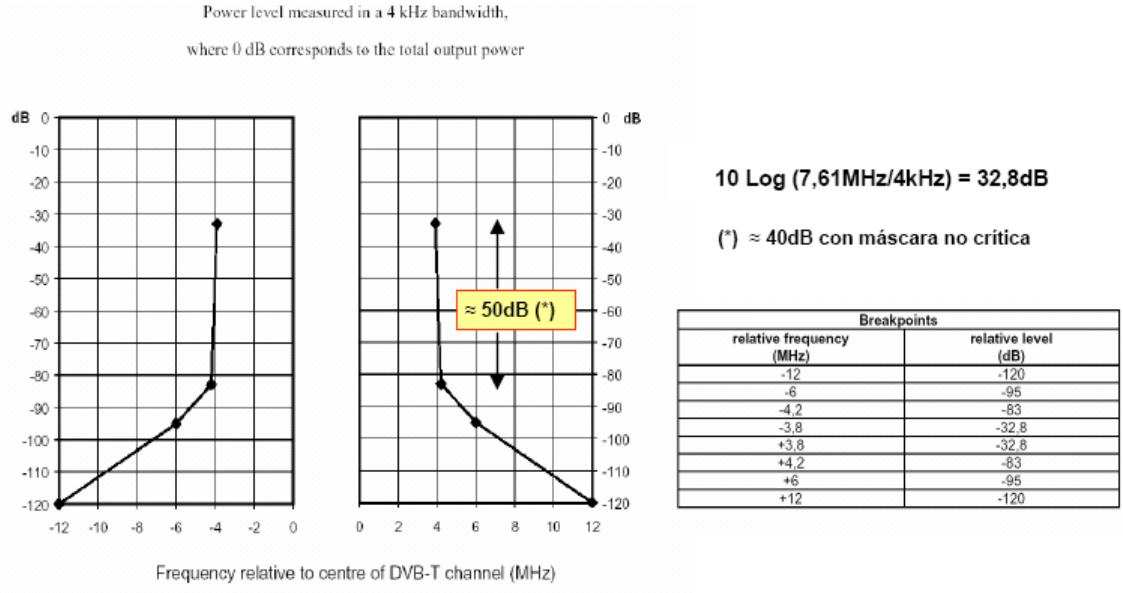
Estan representados todos los bloques que conforman la cadena de transmisión, desde el codificador y el mapeador al convertidor D/A de salida junto con la cadena amplificdora de potencia.

Es muy importante el comportamiento del paso de la señal a través del amplificador de potencia PA pues éste no es un elemento lineal. Al no serlo, genera productos de intermodulación que deben de ser controlados pues afectan a la degradación de la señal, no sólo propia sinó también a las señales de posibles canales adyacentes. Es el llamado efecto de hombreras o shoulders que tienen los amplificadores. Debido a ello es muy importante controlar el nivel de hombreras que puedan tener dichos amplificadores estableciendose como nivel de referencia unos shoulders a -40dB respecto el nivel nominal de la señal una vez precorregidos.

1.1.2 MÁSCARA ESPECTRAL

Para conseguir que la señal radiada por los tranmisores de DVB-T sea con el menor nivel de hombreras posible, se utilizan técnicas de precorreción analógica o digital así como utilizar amplificadores de potencia lineal como los de tecnología LDMOS. Además se emplean filtros a la salida del amplificador para minimizar los efectos de las señales situadas fuera de la banda de canal asignada. El espectro resultante de la señal con sus hombreras seguida del filtrado deberá cumplir con un perfil que se especifica mediante una máscara en el estándar.

La siguiente figura [1] recoge las características de la denominada Máscara Crítica que es siempre la requerida en el caso de presencia de canales adyacentes de televisión digital y analógica.



Breakpoints	
relative frequency (MHz)	relative level (dB)
-12	-120
-6	-95
-4,2	-83
-3,8	-32,8
+3,8	-32,8
+4,2	-83
+6	-95
+12	-120

FIGURA 3. MÁSCARA CRÍTICA PARA SEÑAL DVB-T PARA CANALES DE 8MHZ

En el caso de los canales de 8MHz de ancho de banda, por ejemplo, se expresa el valor para los puntos conflictivos situados a +/-4,2MHz respecto a la freceuncia central. El espectro útil de la señal COFDM ocupa realmente un ancho de banda de 7,61MHz para los canales de 8MHz.

Si se utiliza un filtro de resolución de 4KHz en el analizador de espectros, el nivel de la señal estará situada a 32,8dB por debajo de la referencia de 0dB.

$$10 \log (7{,}61\text{MHz}/4\text{KHz}) = 32{,}8\text{dB}$$

Esto significa que en los puntos separados +/-4,2MHz de la freceuncia central, el nivel del espectro deberá estar a unos 50dB por debajo del nivel de la señal dentro de banda, en el caso de querer cumplir la máscara crítica y de 40dB con máscara no crítica. En un caso general de transmisor en que las hombreras generadas estén a –40dB, un filtro colocado a la salida debería de aportar los 10dB restantes para el cumplimiento de la máscara crítica.

1.1.3 RUIDO DE FASE DE LOS OSCILADORES

La calidad de la señal OFDM se degrada mucho si las portadoras de la señal modulada se ven afectadas por el ruido de fase. Este ruido de fase es introducido principalmente por el oscilador local OL del convertidor de canal tanto de recepción como transmisión. Por esta razón, en los equipos transmisores/reemisores para DVB-T este parámetro de calidad del OL es tan importante y apreciado.

La figura siguiente [2] muestra la máscara recomendada para el ruido de fase de los osciladores locales para DVB-T. Los puntos marcados expresan los niveles de ruido máximos a determinados offset de frecuencia.

Es importante tener en cuenta que los valores específcos para dichos puntos aún están pendientes de especificación en el estándar y que actualemente es el cliente quien especifica el valor de los mismos.

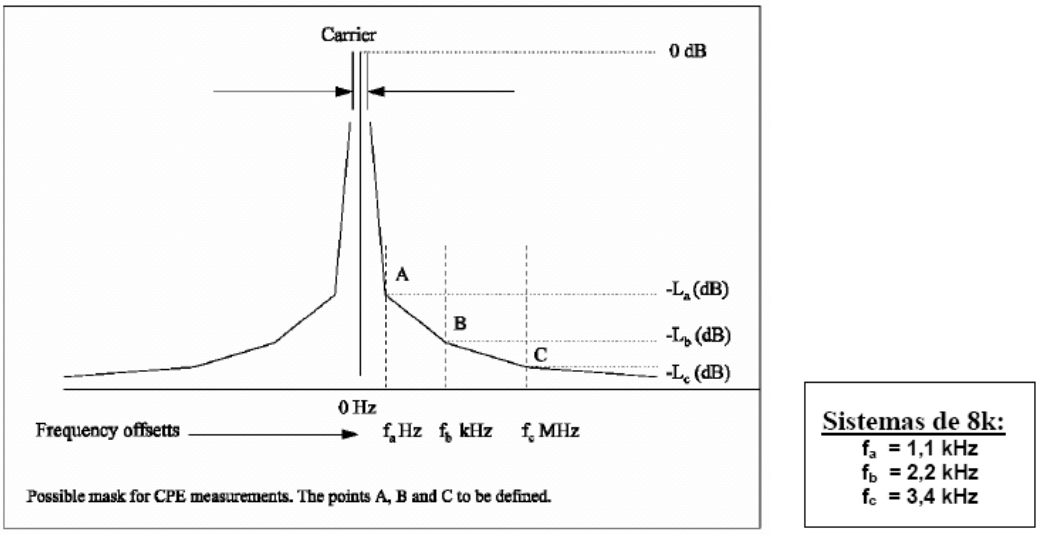


Figura 4. Máscara para el ruido de fase de los osciladores locales

A título orientativo, se considera un nivel adecuado un ruido de fase de –85dBc/Hz a 1,1KHz para sistemas de 8k.

1.2 TOPOLOGÍAS DE RECEPTORES COMERCIALES

El Transport Stream de una onda modulada se vuelve a su forma original mediante un proceso denominado demodulación o detección, por el cual se utiliza un dispositivo receptor. Para recuperar la señal que transporta la información se utilizan dispositivos capaces de atrapar en la manera de lo posible parte de la energía electromagnética y extraer dicha información, estos dispositivos son las denominadas antenas.

Los principios de funcionamiento de los distintos receptores son muy parecidos, siendo el tipo de tecnología utilizada el que marca la diferencia entre un tipo de receptor u otro. Las señales recibidas en las antenas son siempre de niveles bajos y ruidosas con lo que para poder aprovecharlas es importante el uso de amplificadores de bajo ruido antes del detector.

Entre las características más deseables que debe de cumplir un receptor tenemos:

Selectividad: Un receptor debe de ser capaz de separar una señal de cientos de otras señales y ruidos que se encuentran simultáneamente presentes en los terminales de su antena de recepción y que ocupan diferentes espacios del espectro radioeléctrico. Esta capacidad para escoger una pequeña gama de frecuencias se denomina selectividad y es uno de los aspectos más importantes de tener en cuenta en todo diseño de un receptor.

La característica de la selectividad tiene que ir más allá que el simple hecho de separar señales que no nos interesan próximas a la frecuencia de interés, debería de además tener en cuenta el rechazo de las frecuencias no deseadas generadas en el propio receptor, como por ejemplo el rechazo a la frecuencia imagen.

Sensibilidad: Un buen receptor debe de tener un mecanismo capaz de amplificar la señal hasta un valor adecuado para ser aprovechado. A la capacidad de recibir señales débiles se le denomina sensibilidad.

Fidelidad: Es la capacidad para reproducir sin errores la señal original.

Bajo Ruido: La señal recibida desde la antena siempre presenta ruido, tanto atmosférico como procedente de otras señales. Además de este ruido, el receptor contribuye con un ruido propio denominado ruido térmico de los propios componentes. Es muy importante que el ruido interno del receptor sea inferior al ruido mínimo que puede provenir de la antena de recepción.

Estabilidad: Es importante que los sintonizadores del receptor sean precisos en la frecuencia deseada a lo largo del tiempo y en temperatura ambiente.

Resistencia a la sobrecarga: El receptor debe de ser capaz de operar correctamente incluso con la presencia de estaciones potentes cercanas tanto analógicas como digitales.

Como hemos dicho anteriormente, las topologías de receptores pueden ser muchas y muy diversas, en el presente trabajo destacamos las tres más importantes mediante las cuales sirven de punto de partida para la mayoría de receptores comerciales.

No es posible determinar qué arquitectura es mejor que las otras. A la práctica, se escoge una u otra en función de la aplicación, las condiciones de transmisión y los recursos disponibles, tanto de espacio como coste.

1.2.1 SUPERHETERODINO

Se trata de la arquitectura más conocida popularmente por su simplicidad y su facilidad de aplicación. A continuación se presenta el diagrama de bloques básico:

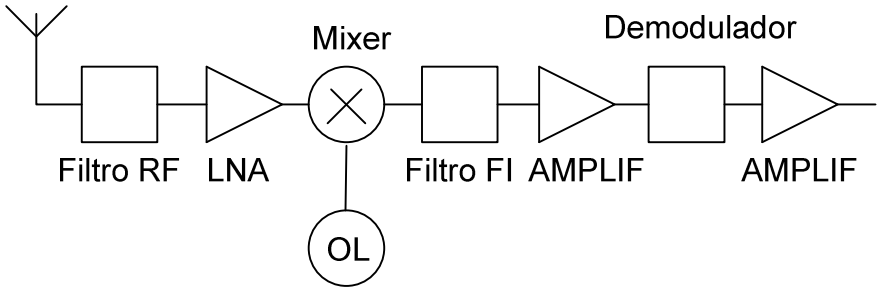


Figura 5. Diagrama de bloques de un receptor superheterodino

La señal en RF recibida en la antena se hace pasar por un filtro paso banda de radiofrecuencia. El objetivo es eliminar el ruido y las señales interferentes situadas fuera de la banda de interés además de mejorar la adaptación de la impedancia entre la antena del receptor y la entrada del amplificador LNA.

La función del amplificador LNA es básicamente incrementar la sensibilidad del receptor teniendo en cuenta que es muy importante que sea de muy bajo ruido. El mixer multiplica la señal de RF amplificada (fRF) con la señal del oscilador local (fOSC) dando lugar a dos señales. La primera de frecuencia fRF+fOSC, la cual en nuestro esquema se filtrará por el filtro FI y la otra de frecuencia fIF=|fRF – fOSC|, de la cual se extraerá la información y denominaremos frecuencia intermedia.

Esta conversión es muy útil pues da mucha selectividad frecuencial empleando un filtro de frecuencia fija. Por lo tanto, se utiliza un filtro paso banda del tipo SAW a fIF, eliminando las señales de diferente frecuencia generados por el mixer.

Un problema de ésta arquitectura hace referencia a la denominada frecuencia imagen.

Un ejemplo sencillo de este problema seria el siguiente: Suponemos que tenemos un receptor sintonizado a 800MHz i la frecuencia del oscilador es de 700MHZ. Entonces como hemos dicho la frecuencia intermedia fIF será de 100MHz. Si a la entrada tenemos una señal interferente a 600MHz (2fOSC-fRF) entonces –fim+fOL caerá también a fIF. Gráficamente:

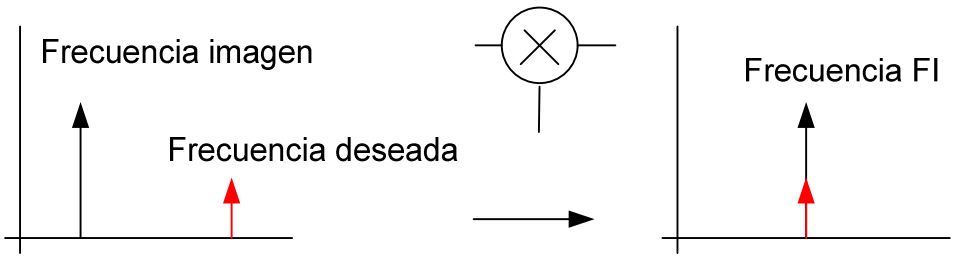


Figura 6. Ejemplo de señal interferente a FI

Para evitarlo el filtro de RF debe de ser lo suficientemente selectivo como para filtrar dicha frecuencia imagen, aunque muchas veces no es posible. El receptor de doble conversión en frecuencia permite la utilización de filtros más en la entrada del receptor pues solventa la problemática de la frecuencia imagen.

En resumen, esta arquitectura permite obtener una buena selectividad en frecuencia, alta sensibilidad y lo más importante, trabajar con diferentes tipos de modulaciones. Por el contrario, el consumo de la arquitectura no tiende a ser leve y presenta el problema de la frecuencia imagen.

1.2.2 SUPERHETERODINO DE CONVERSIÓN DIRECTA

Es un caso particular del receptor superheterodino donde fOL=fRF. Su esquema de bloques funcionales sería el siguiente [3]

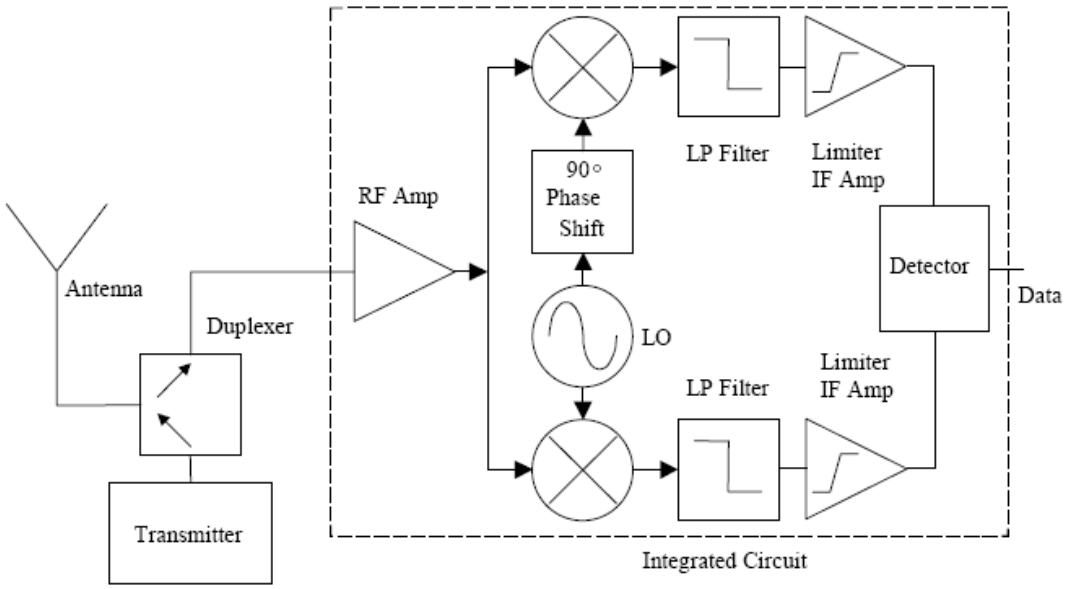


Figura 7. Diagrama de un receptor homodino

La señal de RF modulada se traslada directamente a banda base, cosa que no evita el problema de la frecuencia imagen ya que después de la conversión frecuencial la banda superior a fOSC y la banda inferior se sitúan superpuestas en banda base.

Este problema se soluciona multiplicando la señal de RF modulada de entrada por dos señales desfasadas 90º, con la intención de mantener la información que permita distinguir la banda lateral superior a fOSC de la banda lateral inferior. Esta información se encuentra con la diferencia de fase entre las dos señales resultantes de baja frecuencia.

El gran problema de este tipo de topología es la presencia de una señal denominada '*leakage signal*' a la misma frecuencia de la señal de RF deseada, que se filtra del oscilador local hacia la antena. Esta señal atraviesa el filtro de RF hacia la entrada de los mezcladores la cual cosa genera un offset en DC. Otros problemas de esta arquitectura son la elevada sensibilidad al ruido térmico, típicos a bajas frecuencias y que puede hacer disminuir la sensibilidad del receptor.

Finalmente, esta arquitectura permite obtener alta selectividad en frecuencia y buena sensibilidad. El consumo es inferior al del receptor superheterodino y es adecuado para ser integrado en excepción al filtro RF de entrada. Por ese motivo se suele representar dentro de un encapsulado integrado. Se utiliza en aplicaciones donde se requiere alta selectividad y sensibilidad y donde el consumo no puede ser elevado, como por ejemplo móviles.

1.2.3 SUPERHETERODINO DE DOBLE CONVERSIÓN

Algunos receptores emplean un sistema de doble conversión. Tienen dos osciladores locales, sobre todo cuando la RF es muy alta como es el caso de la UHF. Y si el receptor es digital, el segundo mezclador además separa las componentes I y Q. El diagrama de bloques general de este receptor se muestra en la figura siguiente [4]

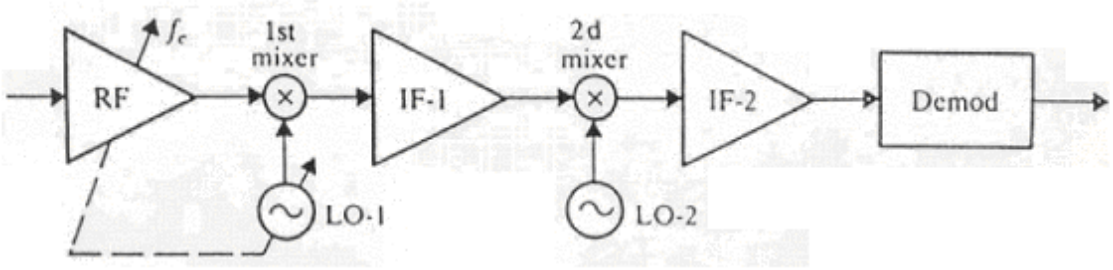


Figura 8. Diagrama de bloques de un receptor con doble conversión

Una FI baja requiere de un buen oscilador local pero no necesita de un buen filtro de FI. Por el contrario una FI alta requiere de un filtro muy selectivo pero mejora el problema al rechazo de la banda imagen. Entonces un receptor con doble conversión utiliza dos FI con el propósito de combinar los beneficios de las dos técnicas anteriores. En un sistema dual de conversión un primer mixer produce una FI elevada para mitigar el efecto de la banda imagen, mientras un segundo mixer con una baja FI mejora el problema de selectividad de canal.

Capítulo 2

2. SÍNTESIS DE FRECUENCIAS EN MICROONDAS

Llamamos síntesis de frecuencias al proceso mediante el cual se consigue generar una señal de una frecuencia específica con gan pureza espectral y muy poca tolerancia de error. Las técnicas utilizadas para la síntesis de frecuencias se clasifican en dos grandes grupos:

1.Sistemas de síntesis directa.
2.Sistemas de síntesis indirecta.

Los sistemas de síntesis indirecta son los más utilizados en equipos transmisores y receptores de DVB-T. Se basan esencialmente en sincronizar la frecuencia de un oscilador normalmente controlado por tensión a la de otra referencia de gran pureza espectral y estabilidad adoptando las características de tolerancia de la referencia a la salida del sintetizador.

Por el contrario, los sistemas de síntesis directa, generan la frecuencia requerida a partir de un proceso matemático de sumas y restas de frecuencias mediante mezcladores. Dentro de éste mismo grupo encontramos los sistemas coherentes, siendo aquellos que utilizan un único oscilador para la síntesis, y los sistemas incoherentes que son aquellos que utilizan osciladores de frecuencias dispares e independientes.

2.1 SÍNTESIS DIRECTA

Este sistema se basa en la síntesis de frecuencia mediante un procesado aritmético de frecuencias, no próximas a la de síntesis, a partir de la utilización de mezcladores y multiplicadores.

2.1.1 SISTEMAS INCOHERENTES

Utilizan osciladores de referencia de distintas frecuencias e independientes entre sí. En la siguiente figura se representa un ejemplo, en forma de diagrama de bloques, de un sistema de síntesis directa incoherente [5]:

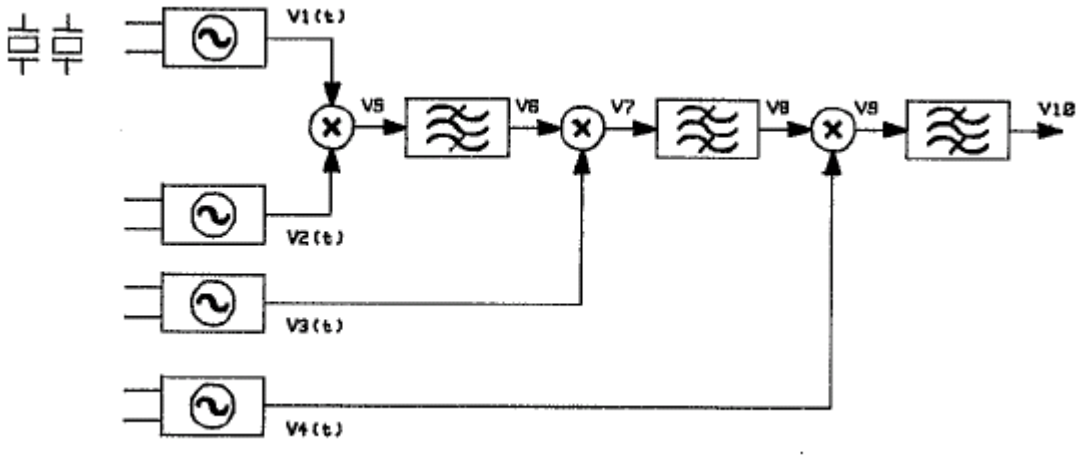


Figura.9 Diagrama de bloques de un sistema incoherente

En éste ejemplo se dispone de cuatro osciladores diferentes los cuales pueden conmutar su frecuencia de oscilación mediante el intercambio de los cristales de cuarzo del resonador. Eligiendo adecuadamente las frecuencias de los osciladores, se puede sintetizar en la salida V10 un número aceptable de frecuencias.

El problema con este tipo de sintetizador es que la obtención de la frecuencia deseada requiere generar otras frecuencias, que podrán superponerse a la señal de salida, degradando sus prestaciones sobretodo pensar que el ruido de fase de la señal de salida V10 corresponderá a la suma de los ruidos de fase de cada una de las fuentes. Entonces el ruido de fase final obtenido será demasiado grande y no resulta interesante.

2.1.2 SISTEMAS COHERENTES

En este caso todos los osciladores se derivan de la misma frecuencia de referencia, por lo tanto la contribución al ruido de fase en la señal de salida se deberá únicamente del oscilador de referencia, efecto que mejora sustancialmente el problema del sistema de síntesis anterior descrito. Se distinguen entre dos tipos de sistemas coherentes:

a. Aproximación por Fuerza Bruta: Genera un cierto número grande de frecuencias. En el proceso se utilizan tanto multiplicadores como divisores de frecuencia [5]

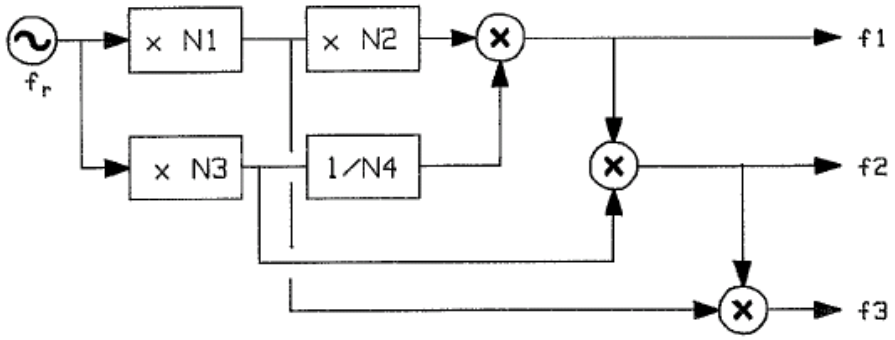


Figura 10. Sintetizador coherente de síntesis directa por fuerza bruta

b. Aproximación Armónica: Se introduce la señal del oscilador de referencia en un dispositivo no lineal que a su vez genera un cierto contenido de armónicos. A posteriori mediante un filtrado se selecciona el armónico de interés [5]

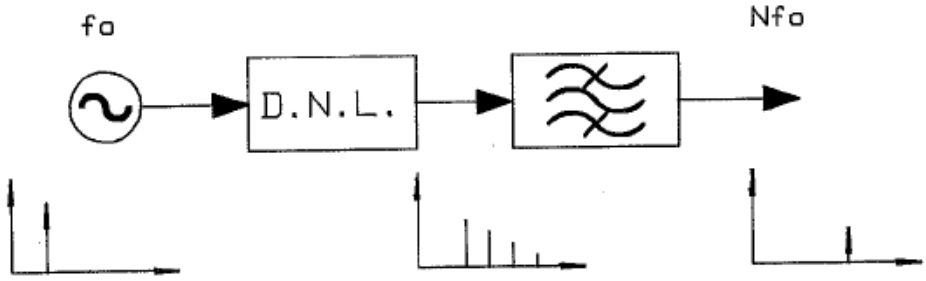


Figura 11. Sintetizador coherente de síntesis directa por aproximación armónica

El modelo sólo sirve si se requiere sintetizar frecuencias fijas. En el caso de querer sintetizar frecuencias variables, debe de modificarse el modelo anterior al siguiente [5]

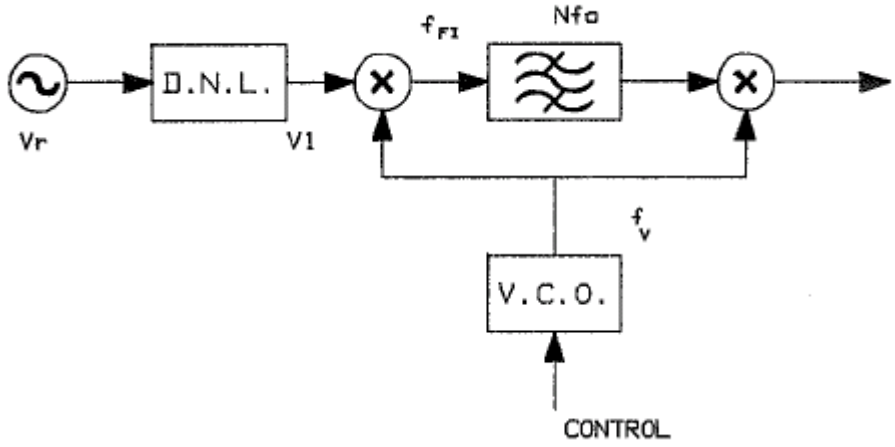


Figura 12. Sintetizador coherente de síntesis directa de frecuencia variable

En este caso el conjunto de armónicos se mezcla con el oscilador local controlado por un VCO (Voltaje Control Oscillator).

2.2 SÍNTESIS INDIRECTA

El sistema de síntesis indirecta de frecuencias se basa en generar una frecuencia deseada a partir de una señal de referencia de un oscilador al que se sincroniza. En este caso la frecuencia deseda adopta las características de ruido de fase del oscilador de referencia aunque añadiendo al ruido de fase las debidas constantes de multiplicación requeridas en el comparador de fase para conseguir generar la frecuencia deseada.

En transmisión de señales UHF el método más utilizado es la sincronización mediante bucle PLL (Phase Locked Loop). Actualmente el método más común para síntesis de frecuencias es el uso de estos dispositivos debido a su bajo precio, altas prestaciones y disponibilidad.

Aparte de las características inherentes de ser un sintetizador de síntesis indirecta, éste dispositivo posee la peculiaridad que permite una variación discreta en forma de pasos de la frecuencia de salida, donde el rango y resolución depende de la frecuencia de salida y del comparador de fase utilizado.

2.2.1 SINCRONIZACIÓN MEDIANTE BUCLE PLL

Un PLL (*Phase locked loop*) es un dispositivo que genera una oscilación cuya fase con respecto a una señal de entrada de referencia se mantiene acotada gracias a una realimentación permanente que compara la fase de las dos señales F1 y F2 y actúa modificando la frecuencia de la oscilación generada.

En la figura 13 se muestra un esquema simplificado del mismo [6]

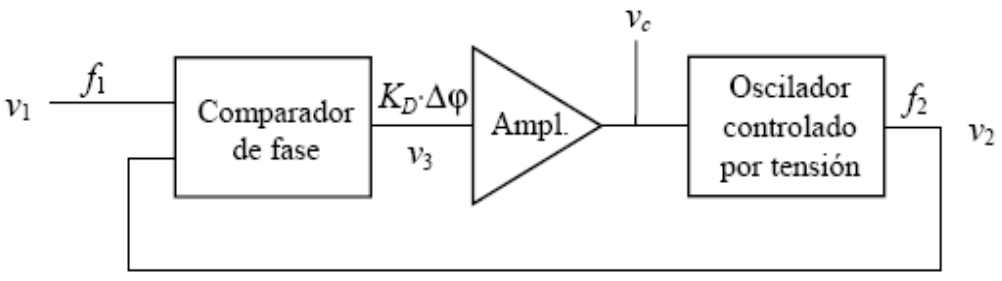


Figura 13. Diagrama esquemático de un PLL

El comparador de fase o PD genera una señal llamada *KD*·Δφ que es proporcional a la diferencia de fase de F1 y F2. La frecuencia F1 proviene de un oscilador de referencia, en cambio F2 proviene de un oscilador controlado por tensión VCO que varía su frecuencia en función de la tensión de entrada Vc. La situación de 'enganche' se produce cuando la señal *KD*·Δφ a la salida del amplificador sea en fase tal que aplicada como tensión al VCO éste genere una frecuencia F2 que sea exactamente igual a la frecuencia de entrada F1.

A continuación se presenta el diagrama de bloques esencial de un bucle PLL:

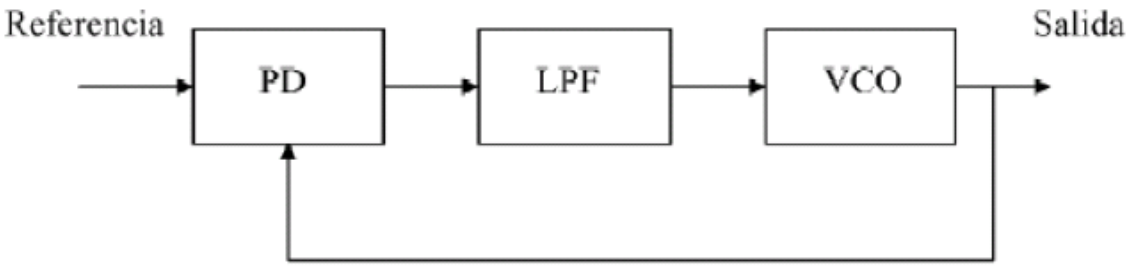


Figura 14. Componentes básicos de un PLL

COMPARADOR DE FASE (PHASE DETECTOR): Es continuo y mide la diferencia de fase entre la oscilación de Referencia y la oscilación de la Salida. Es un generador de impulsos como se observa en la siguiente figura [7]

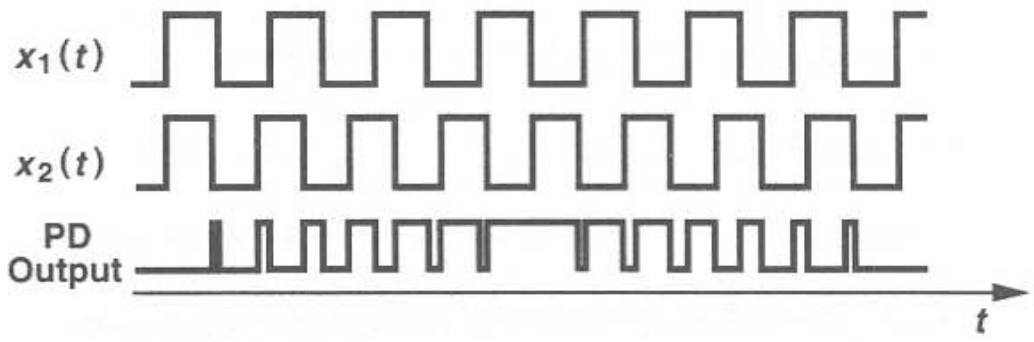


Figura 15. Funcionamiento Comparador de Fase

La duración de los pulsos corresponde a la separación en tiempo del ruido de fase entre las dos señales comparadas.

FILTRO DE BUCLE (LOOP FILTER): Es un filtro pasa bajos y se utiliza para filtrar el ruido de la señal de entrada o del propio sistema. Puede ser un filtro activo o pasivo, En el primer caso introduce mayor ruido pues utiliza operacionales implementados con transistores. En el caso de ser un filtro pasivo es menos ruidoso pero tiene menos posibilidades a la hora de atacar la etapa posterior del VCO.

OSCILADOR CONTROLADO POR VOLTAGE (VCO): Se controla por tensión. Acostumbra a ser la parte más cara del filtro de lazo, y la más sensible en cuestión de ruido de fase.

2.2.2 EFECTOS DEL RUIDO DE FASE EN EL SINTETIZADOR

En la etapa de recepción de un receptor de DVB-T es muy importante limitar los niveles de ruido del sistema pues puede afectar gravemente a la calidad de demodulación de la señal. El ruido de fase de los osciladores es uno de los factores determinantes que contribuyen en éste aspecto. En la figura siguiente [8] se observa la diferencia de espectros entre un oscilador ideal y uno real.

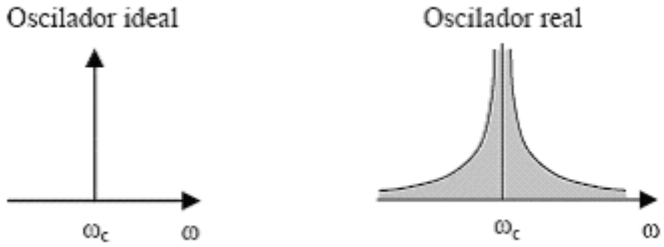


Figura 16. Espectro de salida de un oscilador ideal y real

En el oscilador real se representa con un tono puro a la frecuencia requerida, en cambio en el comportamiento del oscilador real se observan las llamadas faldas o 'skirts' pues el oscilador presenta componentes frecuenciales continuos alrededor de la frecuencia pura.

Esto es debido a las fluctuaciones errantes en la fuente de oscilación. Cuando dos señales RF y OL son multiplicadas en el Mezclador en la etapa de recepción de un receptor de DVB-T, el ruido de fase del OL contribuye en el resultado de dicha conversión dando lugar a dos espectros sobrepuestos.

Si miramos este efecto gráficamente [8]:

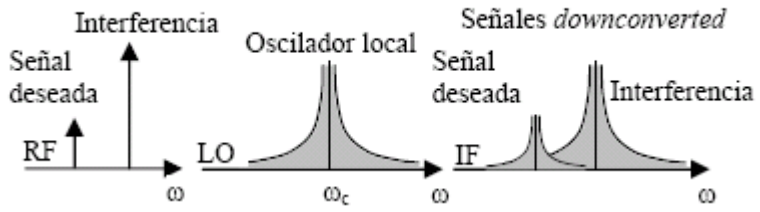


Figura 17. Espectro de entrada, del oscilador local y de FI durante el proceso de conversión

Podemos comprovar como efectivamente la señal deseada en FI se ve afectada por el ruido de fase superpuesto de la señal interferente.

En éste sentido, el ruido combinado del lazo de un PLL que sintetiza un OL específico, normalmente se asemeja al de la figura 18. En éste gráfico se puede apreciar como el ruido dentro de la banda del lazo es principalmente producido por el detector de fase y la referencia. En cambio fuera del lazo el ruido viene producido por el VCO. Entonces, la optimización del ruido de fase resultante es un juego dependiente entre el ancho de banda del lazo, el ruido del detector de fase y el ruido del VCO.

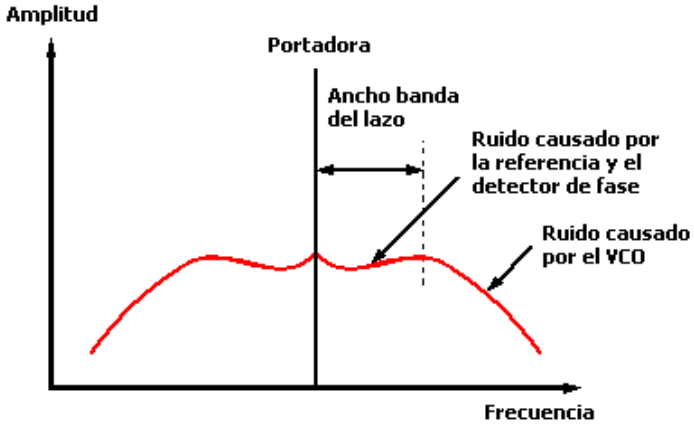


Figura 18.Figura de ruido típica de un sintetizador

Los efectos de una señal OL con un elevado ruido de fase son varios dependiendo si estamos tratando la etapa de recepción o de transmisión. Por una parte, a nivel de sistema de recepción, el efecto de un ruido de fase elevado puede llevar a incrementar errores en el BER (*Bit Error Ratio*) lo que implica una mala calidad de imagen y un empeoramiento del factor de calidad MER (Modulation Error Ratio).

A nivel más detallado dentro de un receptor el efecto negativo se produce durante la mezcla de la señal de RF con el mixer. Si el sintetizador produce una señal OL con mucho ruido de fase podemos encontrarnos que la señal no es capaz de pasar por el filtro de FI de la cadena receptora.

A nivel de transmisión el efecto de un oscilador con mucho ruido de fase provoca que en la etapa de amplificación de la señal se produzcan mayor número de productos de intermodulación con el consiguiento aumento de las hombreras en la señal amplificada y la posibilidad de tener interferencias co-canal entre transmisores de canales próximos.

Capítulo 3

3. DISEÑO DE LOS OSCILADORES LOCALES

3.1 OBJETIVO

El objetivo es diseñar dos osciladores locales sintetizados con una topología de síntesis indirecta mediante bucle PLL que conformará a posteriori la etapa de recepción (Downconverter) de un transmisor/reemisor de televisión digital terrestre o DVB-T.

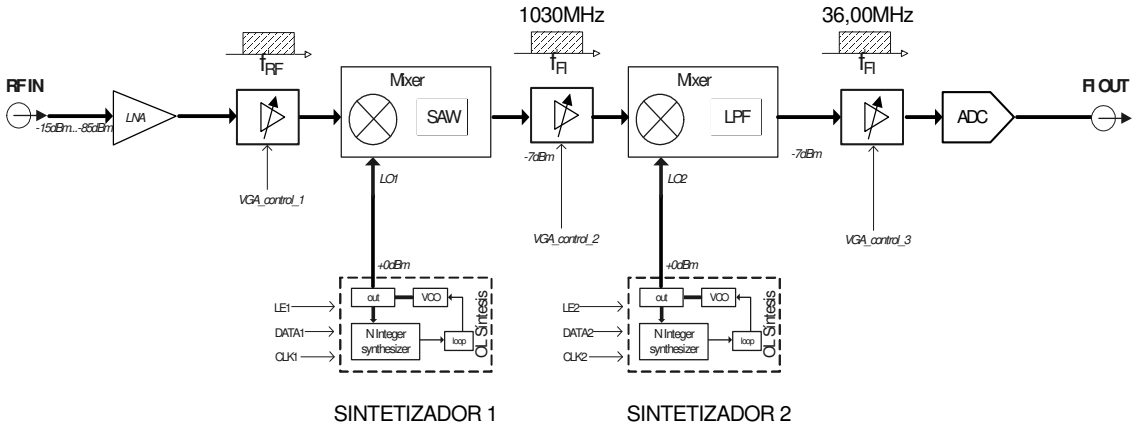


Figura 19. Esquema de bloques de un downconverter con doble conversión

La misma topología presentada puede utilizarse para la implementación del upconverter del transmisor/remisor si se desacoplan las dos salidas de los respectivos osciladores locales, con lo que se obtiene un sistema de conversión completo.

Para la banda UHF del espectro radioeléctrico, pertenecen los canales de televisión del 21 al 69 esto es de la frecuencia inicial de 470MHz a la frecuencia final de 862MHz. Se decide escoger una frecuencia FI1 alta de 1030MHz para solventar el problema de la banda imagen y una FI2 de 36MHz habitual en equipos comerciales repetidores de televisión digital.

El control de los sintetizadores 1 y 2 se puede realizar a partir de la utilización de un micro de control o aún mejor una FPGA pudiéndose utilizar la señal FI de salida de 36MHz posterior a la doble conversión para procesarse en la misma FPGA, una vez digitalizada.

3.2 TABLA DE CANALIZACIONES

CANAL	FRECUENCIA CENTRAL	FI_1	OL_1	IMAGEN FI_1	FI_2	OL_2	IMAGEN FI_2
21	474	1031	1505	1979	36	995	2026
22	482	1028	1510	1992	36	992	2020
23	490	1030	1520	2010	36	994	2024
24	498	1032	1530	2028	36	996	2028
25	506	1029	1535	2041	36	993	2022
26	514	1031	1545	2059	36	995	2026
27	522	1028	1550	2072	36	992	2020
28	530	1030	1560	2090	36	994	2024
29	538	1032	1570	2108	36	996	2028
30	546	1029	1575	2121	36	993	2022
31	554	1031	1585	2139	36	995	2026
32	562	1028	1590	2152	36	992	2020
33	570	1030	1600	2170	36	994	2024
34	578	1032	1610	2188	36	996	2028
35	586	1029	1615	2201	36	993	2022
36	594	1031	1625	2219	36	995	2026
37	602	1028	1630	2232	36	992	2020
38	610	1030	1640	2250	36	994	2024
39	618	1032	1650	2268	36	996	2028
40	626	1029	1655	2281	36	993	2022
41	634	1031	1665	2299	36	995	2026
42	642	1028	1670	2312	36	992	2020
43	650	1030	1680	2330	36	994	2024
44	658	1032	1690	2348	36	996	2028
45	666	1029	1695	2361	36	993	2022
46	674	1031	1705	2379	36	995	2026
47	682	1028	1710	2392	36	992	2020
48	690	1030	1720	2410	36	994	2024
49	698	1032	1730	2428	36	996	2028
50	706	1029	1735	2441	36	993	2022
51	714	1031	1745	2459	36	995	2026
52	722	1028	1750	2472	36	992	2020
53	730	1030	1760	2490	36	994	2024
54	738	1032	1770	2508	36	996	2028
55	746	1029	1775	2521	36	993	2022
56	754	1031	1785	2539	36	995	2026
57	762	1028	1790	2552	36	992	2020
58	770	1030	1800	2570	36	994	2024
59	778	1032	1810	2588	36	996	2028
60	786	1029	1815	2601	36	993	2022
61	794	1031	1825	2619	36	995	2026
62	802	1028	1830	2632	36	992	2020
63	810	1030	1840	2650	36	994	2024
64	818	1032	1850	2668	36	996	2028
65	826	1029	1855	2681	36	993	2022
66	834	1031	1865	2699	36	995	2026
67	842	1028	1870	2712	36	992	2020
68	850	1030	1880	2730	36	994	2024
69	858	1032	1890	2748	36	996	2028

La tabla de canalizaciones nos aporta una visión general y completa de todas las frecuencias a sintetizar para cada uno de los dos sintetizadores a diseñar. Si por ejemplo escogemos el caso del canal 45, la frecuencia central se encuentra a 666MHz con un ancho de banda total de 8MHz, con lo que la frecuencia inferior de canal es 662MHz y la superior 670MHz. Al mezclar la frecuencia de canal con el sintetizador obtenemos las siguientes frecuencias resultantes:

FI1=666MHz+1695MHz = 2361MHz
FI1=| 666MHz-1695MHz | = 1029MHz

Siendo la frecuencia de 2361MHz la banda imagen y la frecuencia de 1029MHz la FI1 que necesitamos.

Las FI1 resultantes de la tabla no están exactamente centradas a la frecuencia de 1030MHz. Esto es debido a que el paso del oscilador que queremos utilizar es de 5MHz con lo que no es posible centrar la FI1 a los 1030MHZ para todos los casos de los canales de la banda UHF. Se podría pretender sintetizar la frecuencia del oscilador local con pasos de 1MHZ, pero resultaría con un empeoramiento del ruido de fase del oscilador pues el abanico de frecuencias del sintetizador es muy amplio en este caso.

Para eliminar la banda imagen de la FI1 se va a utilizar en la cadena de recepción del downconverter un filtro SAW (Surface Acoustic Wave Filter) centrado a 1030MHz.

La FI1 de 1029MHz se mezcla a posteriori con el segundo oscilador local, dando como resultado las siguientes frecuencias:

FI2=1029MHz+993MHz = 2022MHz
FI2=| 1029MHz-993MHz | = 36MHz

Siendo la frecuencia de interés la FI2 de 36MHz. A posteriori del mezclador se añade un filtro paso bajos que es suficiente para rechazar la banda imagen de la señal no siendo necesario un filtro de altas prestaciones.

3.3 VISIÓN DE ALTO NIVEL DEL DOWNCONVERTER

En este proceso se traslada un canal de TV situado dentro de la banda UHF de 470MHz a 862 MHz a la frecuencia intermedia FI de 36MHz.

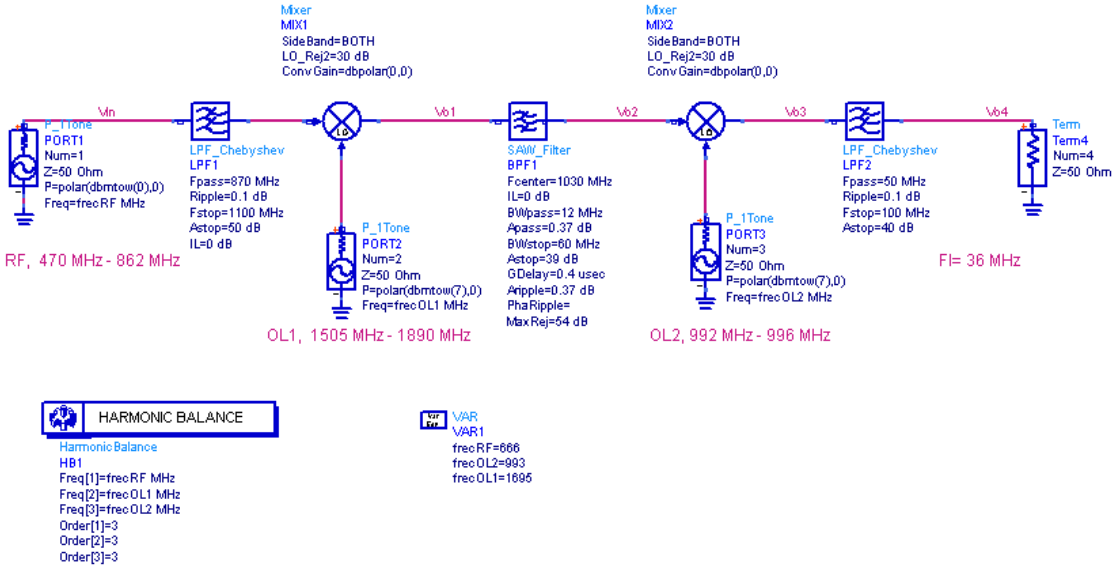


Figura 20.Diagrama general conversor descendente con doble conversión

El filtro paso bajo LPF2 con frecuencia de corte de 870 MHz, rechaza la posible banda imagen de entrada de 2362.5 MHz a 3042 MHz.

Utilizando esta topología no es estrictamente necesario utilizar un filtro de canal a la entrada, siempre que el preamplificador y el primer mezclador MIX1 soporten el nivel conjunto de todos los canales que puedan haber dentro de la banda de 470 a 862 MHz.

El primer mezclador MIX1 traslada el canal de entrada a la primera FI. Por ejemplo, si vamos a la tabla de canalizaciones y escogemos el canal 45 de entrada, la frecuencia central es 666 MHz. Esta frecuencia se bate con OL1 de 1029MHz para obtener la FI2 de 1029 MHz.

La siguiente figura muestra el espectro de señal después de la primera mezcla, antes del filtro paso banda BPF1.

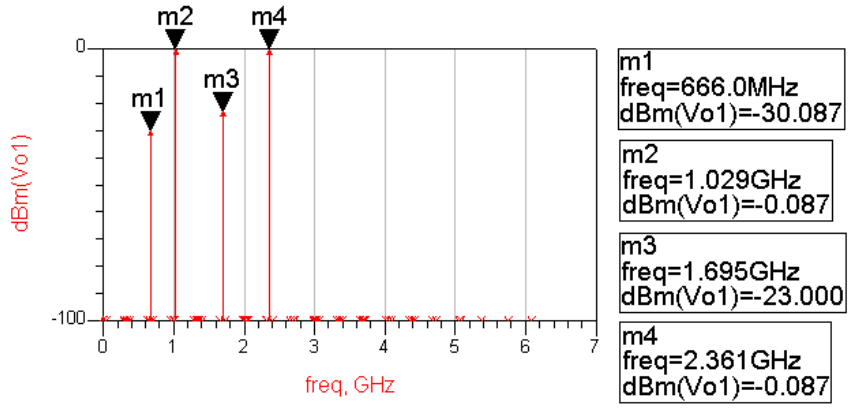


Figura 21. Primer proceso de mezcla del conversor descendente antes de filtro

Después del filtro paso banda obtenemos la siguiente respuesta.

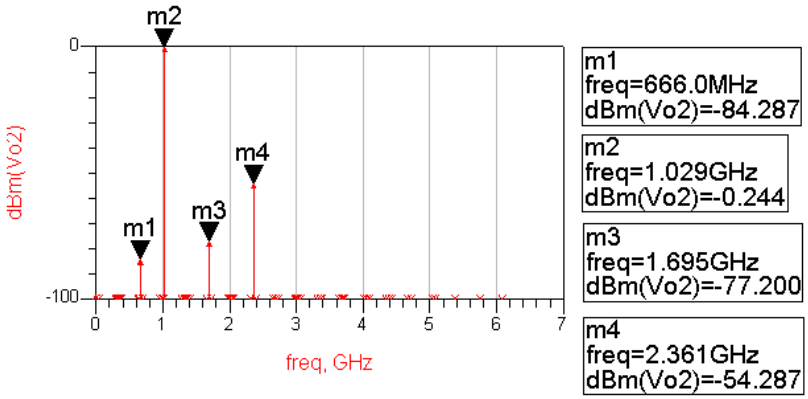


Figura 22. Proceso de la primera mezcla después de filtro

La segunda mezcla tiene lugar en MIX2, donde la FI2 de 1029 MHz se bate con OL2 de 993MHz, generando la frecuencia de FI de 36MHz y una frecuencia imagen de 2022MHz

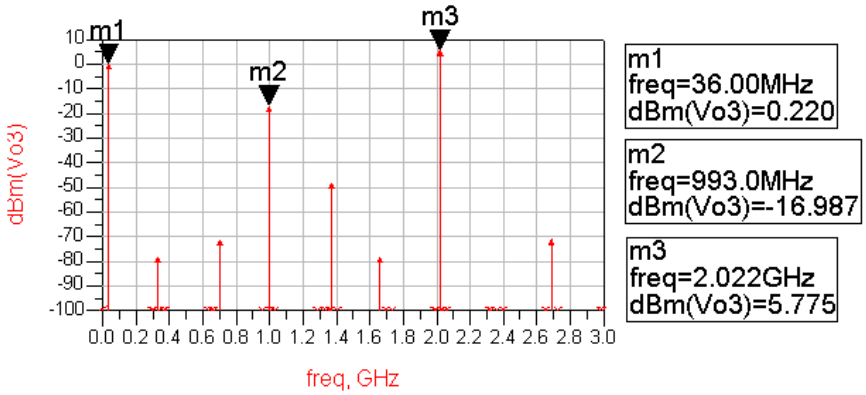


Figura 23. Proceso de segunda mezcla del conversor descendente

Finalmente el filtro paso bajo LPF1 con frecuencia de corte de 50 MHz, limpia el espectro de las componentes de alta frecuencia, dejando pasar la señal de FI.

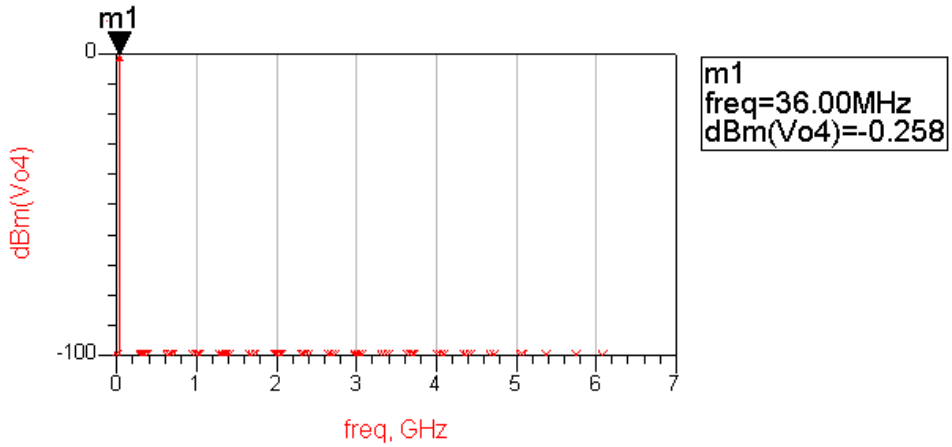


Figura 24. Proceso de segunda mezcla del conversor descendente

3.4 SEÑAL DE REFERENCIA DEL GPS

En el proceso de la radiodifusión de la Televisión Digital Terrestre o TDT se utilizan distintas topologías de emisión de contenidos. Por una parte, se usan las redes en MFN (**Multiple Frequency Networks**) donde la distribución de señales transmitidas se hace en canales de radiofrecuencia distintos y en áreas diferentes, pudiendo ser el contenido de la señal el mismo o diferente.

Otro sistema es el caso de las redes de frecuencia única o SFN (***Single Frecuency Networks***) donde se exige que las señales transmitidas:

a. Radien en la misma frecuencia
b. Emitan la misma información y al mismo tiempo

Para ello necesitan implantar un adaptador SFN a la salida de la cabecera y tanto éste como todos los transmisores deben estar referenciados a las señales de 1pps y 10MHz obtenidas de receptores GPS. Estos receptores profesionales, proporcionan dos señales de referencia, frecuencial y temporal que permiten la correcta sincronización de los equipos transmisores y/o reemisores de televisión. La referencia frecuencial consiste en una señal de 10MHz, mientras que la referencia temporal es una señal de 1PPS (1 pulso por segundo). La referencia de 10MHz se engancha a la

señal de 1pps, con lo cual pasan exactamente 10.000.000 ciclos de señal entre cada evento de 1pps.

A continuación se describe a nivel de bloques la arquitectura típica del cual se conforma un dispositivo GPS, siendo la RF Output la salida de 10MHz.

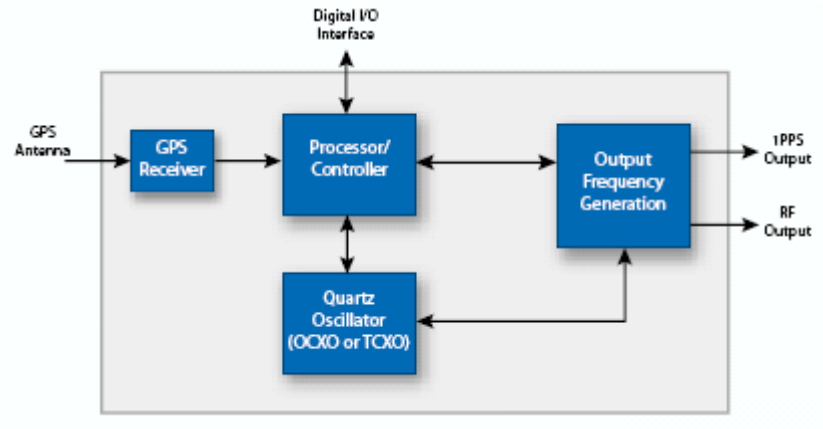


Figura 25. Arquitectura interna de un dispositivo GPS

En equipos profesionales de broadcasting se utiliza por tanto, la referencia de 10MHz procedente del GPS. Esta señal de 10MHz generalmente se caracteriza por:

a. Ruido de fase de altas prestaciones:

Frecuencia (Hz)	Phase Noise(dBc/Hz)
10	-120
100	-135
1000	-145
10.000	-145
100.000	-145

b. Alta estabilidad en frecuencia 1x10-9 y exactitud de señal+/-2Hz

c. Onda del tipo senoidal de 50 ohms

d. Alta pureza espectral con armónicos a –40dBc respecto fundamental.

3.5 SÍNTESIS DE LA REFERENCIA A 30MHZ

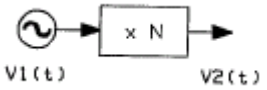
En el diseño de los osciladores locales para implementar la etapa de recepción se parte de la referencia procedente del GPS de 10MHz pues ofrece una muy buena pureza espectral y unas buenas condiciones en cuanto a ruido de fase.

Se procede a realizar el diseño de los sintetizadores mediante una topología de síntesis indirecta mediante bucle PLL, por lo cual, nos engancharemos a la referencia de 10MHz para generar nuestras frecuencias descritas en la tabla de canalizaciones.

En cualquier proceso de multiplicacion de frecuencias, las excursiones de fase se ven magnificadas, por lo que se incrementa el ruido de fase de la señal multiplicada. Este fenómeno se explica en [5]

En un multiplicador de frecuencia de índice N al que se la aplica la señal v1(t) proporcionada por un generador de la forma:

$$v_1(t) = A_1 \cos\left(\omega_1 t + \phi_1(t)\right)$$



con una densidad espectral de potencia de ruido de fase S(f), a su salida se obtiene:

$$v_2(t) = A_2 \cos\left[N\left(\omega_1 t + \phi(t)\right)\right] = A_2 \cos\left(\omega_2 t + \phi_2(t)\right)$$

siendo W2=NW1 y S2(t)=NS1(t), de modo que la densidad espectral del ruido de fase a la salida debe ser:

$$S_{\phi_2}(f) = N^2 S_{\phi_1}(f)$$

Con lo que vemos que realmente el ruido de fase se incrementa a razón de N2.

En nuestro sistema partimos de una señal de 10MHz proviniente de la referencia del GPS. Para mejorar el ruido de fase resultante en nuestros dos osciladores locales, sintetizaremos una frecuencia de referencia intermedia a 30MHz a partir de la

referencia del GPS. De esta manera conseguiremos mejorar las prestaciones de los osciladores a sintetizar.

Veamos un ejemplo comparativo mediante el simulador. Sintetizamos primeramente una frecuencia de 994MHz con una referencia de 10MHz. La contribución al ruido de fase del oscilador por parte de la referencia viene definida en azul por 'Ref'.

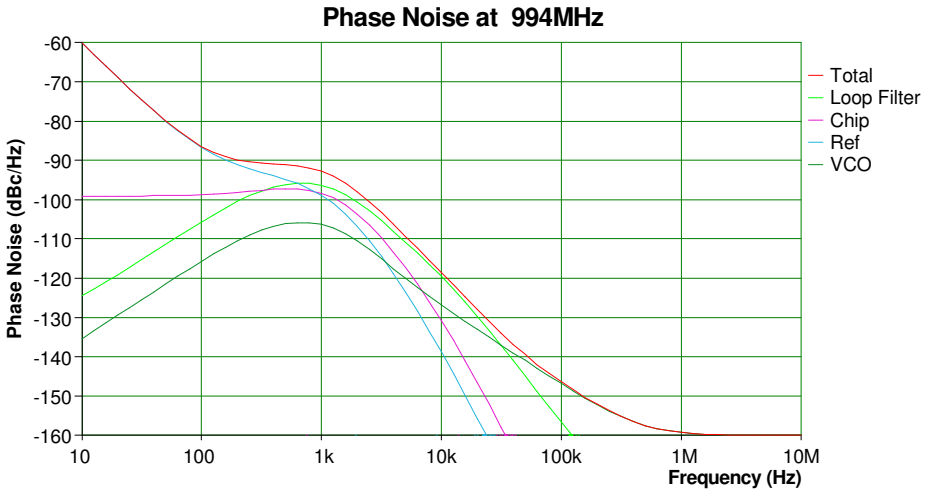


Figura 26. Síntesis de frecuencia a 994MHz usando referencia de 10MHz

Si simulamos la misma situación, simplemente cambiando el valor de la referencia a 30MHz y conservando la misma característica de ruido de fase obtenemos la siguiente simulación:

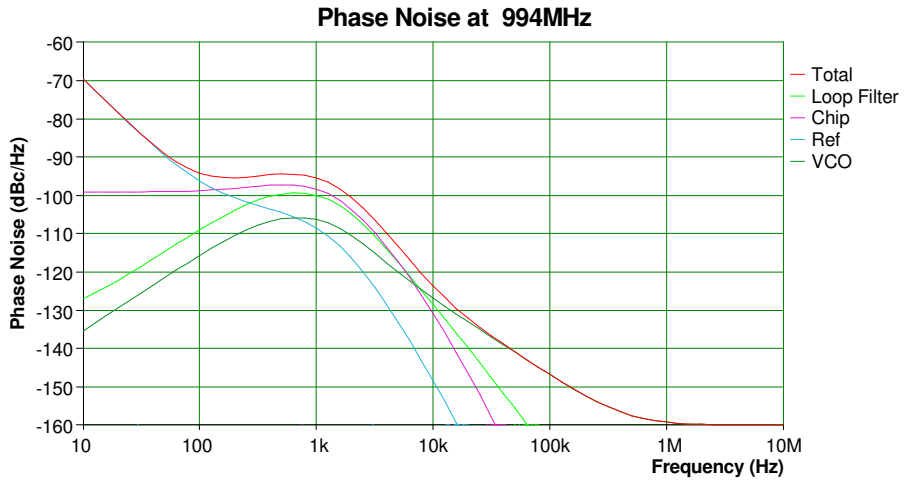


Figura 27. Síntesis de recuencia a 994MHz usando referencia de 30MHz

En este caso observamos como mejoramos el ruido de fase final del sintetizador considerablemente en la zona de 100Hz a 10KHz.

Podemos pensar en aumentar mucho más la frecuencia de la referencia. Así por ejemplo, si simulamos para una referencia de 100MHz obtenemos la siguiente respuesta en la simulación:

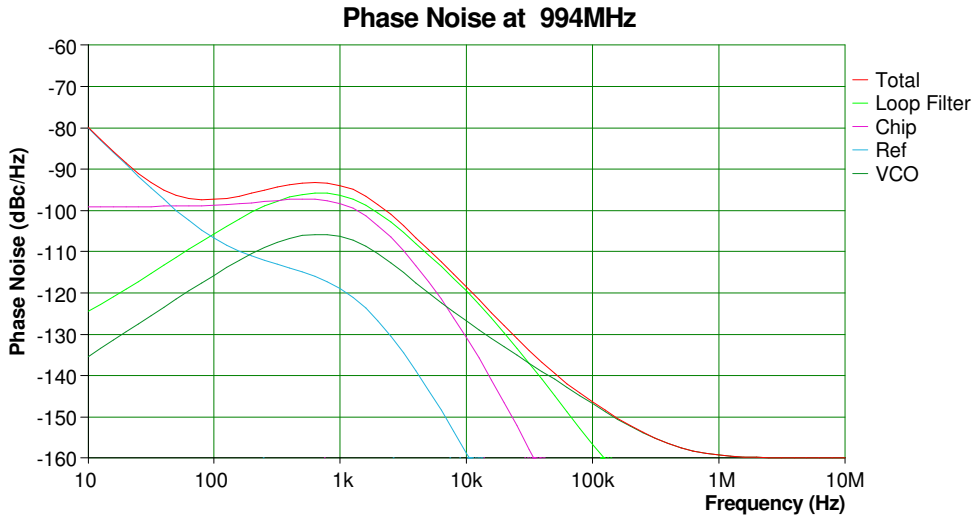


Figura 28.Síntesis de frecuencia a 994MHz utilizando una referencia de 100MHz.

Como puede apreciarse en la gráfica, comparativamente no se obtiene mucha mejoría respecto el anterior caso, de hecho mejoramos el ruido de fase de 100Hz a 1KHz solamente. El problema ahora reside en valorar el coste del VCO necesario para sintetizar la frecuencia de 100MHz mucho más caro que en el caso de utilizar un oscilador de frecuencia menor, con lo que se decide utilizar una solución media, es decir utilizar la referencia a 30MHz.

3.5.1 ELECCIÓN DE COMPONENTES

Existen varios fabricantes que ofrecen integrados para sintetizar frecuencias. Entre los de más embergadura, tenemos National Semiconductor, Linear Technology, Mini-circuits o Analog Devices. Estos últimos son sin duda los que mejores prestaciones tecnológicas y facilidades en la simulación del bucle PLL completo ofrecen.

En el mercado podemos encontrar distintos tipos de integrados PLL :

Enteros de simple y doble salida
Fraccionales de simple y doble salida
Los que integran el Sintetizador+VCO

A continuación se incluye una tabla comparativa de sintetizadores de la marca de ANALOG DEVICES:

	Tipo	Norm Phase Noise (dBc/Hz)	REFin (MHz)	Precio (1000-4999)
AD809	Synthesizer	-	19.44	$3.85
ADF4001	Single Integer-N	-214	104	$1.72
ADF4002	Single Integer-N	-222	300	$1.97
ADF4007	Single Integer-N	-219	240	$2.16
ADF4106	Single Integer-N	-219	300	$2.16
ADF4107	Single Integer-N	-219	250	$2.67
ADF4108	Single Integer-N	-219	250	$3.34
ADF4110	Single Integer-N	-215	104	$2.28
ADF4111	Single Integer-N	-215	104	$2.28
ADF4112	Single Integer-N	-215	104	$2.28
ADF4113	Single Integer-N	-215	104	$2.28
ADF4153	Single Fractional-N	-213	250	$2.28
ADF4154	Single Fractional-N	-213	250	$2.28
ADF4156	Single Fractional-N	-211	250	$3.04
ADF4157	Single Fractional-N	207	300	$3.25
ADF4193	Fast Settling PLL	-216	300	$8.60
ADF4212L	Dual Integer-N	-215	115	$2.45
ADF4218L	Dual Integer-N	-216	110	$2.54
ADF4252	Dual Fractional-N	-214	150	$2.67
ADF4350	Frac-N/Int-N w/ VCO	213	105	$10.30
ADF4360-0	Synthesizer/VCO Integer-N	-214	250	$3.10
ADF4360-1	Synthesizer/VCO Integer-N	-217	250	$3.10
ADF4360-2	Synthesizer/VCO Integer-N	-217	250	$3.10
ADF4360-3	Synthesizer/VCO Integer-N	-217	250	$3.10
ADF4360-4	Synthesizer/VCO Integer-N	-217	250	$3.10
ADF4360-9	Synthesizer/VCO Integer-N	218	250	$3.06

Los PLL del tipo entero ofrece mejor característica en cuestión de ruido de fase. Por el contrario, no podemos sintetizar frecuencias que no sean múltiples enteras de su PFD (Phase Frequency Detector), factor que define el paso de canal de la frecuencia a sintetizar. Los PLL fraccionales pueden sintetizar frecuencias que no sean múltiples enteras de la frecuencia de comparación utilizada pero por el contrario añaden mayor número de espúreos durante la síntesis de la frecuencia que empeoran el ruido de fase del oscilador. Finalmente tenemos los sintetitzadores que integran el VCO y el filtro de lazo, más caros, pero adecuados en el caso de querer sintetizar frecuencias comerciales, típicas en aplicaciones ya estandarizadas, pues no ofrecen mucho juego en terminos de síntesis de frecuencias.

De entre los integrados que ofrecen escogemos el ADF4002 pues es con el que se consigue mejor ruido de fase para nuestra aplicación concreta, además de tener un precio interesante.

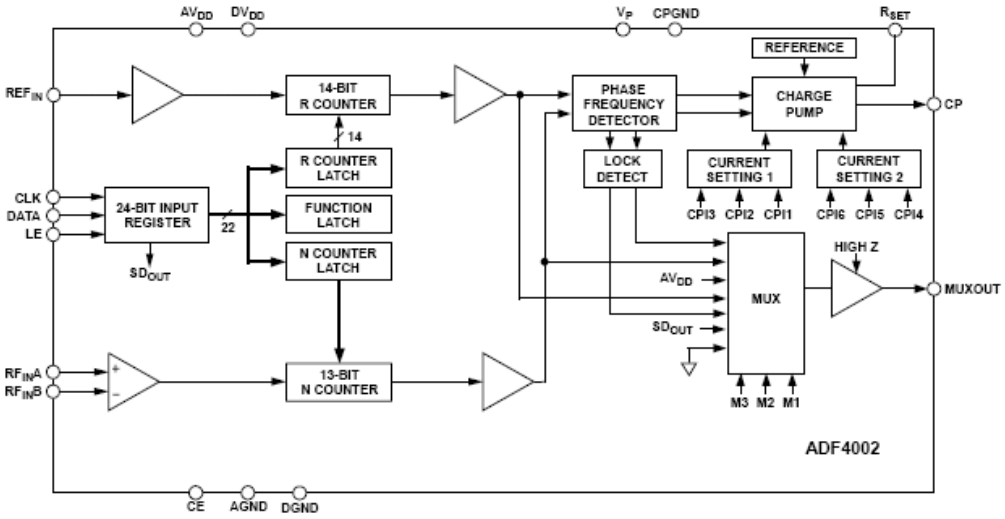


Figura 29. Diagrama de bloques interno del ADF4002

A nivel de VCO '*voltage controlled oscillator*' tenemos igualmente múltiplos fabricantes. Entre ellos: RAKON, CRYSTEK, FOX, etc. A nivel del VCO es importante escoger un componente que tenga muy buen ruido de fase y buena estabilidad en temperatura.

También es importante fijarse que tipo de forma de onda tendremos: una senoide o una onda cuadrada, así como la tensión de control ajustable necesaria para sintetizar la frecuencia de referencia, que determinará en cierto modo el tipo de filtro de lazo utilizar en el PLL.

Haciendo un estudio de varios osciladores tenemos:

FABRICANTE	MODELO	TENSION CONTROL	P.NOISE 10HZ	P.NOISE 1KHZ	P.NOISE 10KHZ
RAKON	VTXO505R	0,5-4,5V	-60dBc/Hz	-140dBc/Hz	-150dBc/Hz
CRYSTEK	CXOSVD4	3,3V-5V	-100dBc/Hz	-140dBc/Hz	-150dBc/Hz
FOX	FVXO-HC52	0,5V-5V	-60dBc/Hz	-110dBc/Hz	-120dBc/Hz
ECLIPTEK	ES51W4	0,5-4,5V	-70dBc/Hz	-130dBc/Hz	-140dBc/Hz

Como oscilador controlado por voltage VCO para sintetizar los 30MHz escogemos el VTXO505R de RAKON pues presenta muy buenas características de ruido de fase y estabilidad tanto en temperatura como en tiempo.

Figura 30. Aspecto físico del VTXO505R

Offset de Frecuencia	Ruido de fase
1Hz	-60dBc/Hz
10Hz	-90dBc/Hz
100Hz	-120dBc/Hz
1kHz	-140dBc/Hz
10kHz	-150dBc/Hz

El filtro de lazo del bucle del PLL en ésta aplicación no es necesario que sea activo, pues la tensión requerida para el VCO es la misma que alimenta el sintetizador de Analog Devices. El tamaño de filtro lo escogemos durante la simulación del sintetizador completo.

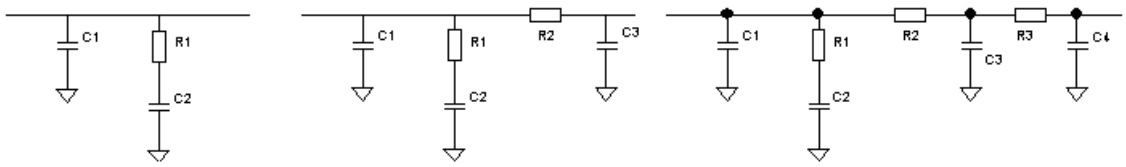


Figura 31. Filtros de lazo disponibles

3.5.2 SIMULACIÓN

Para empezar con la simulación de nuestro sintetizador debemos primero de todo entrar la característica de ruido de fase de nuestra referencia de 10MHz del GPS.

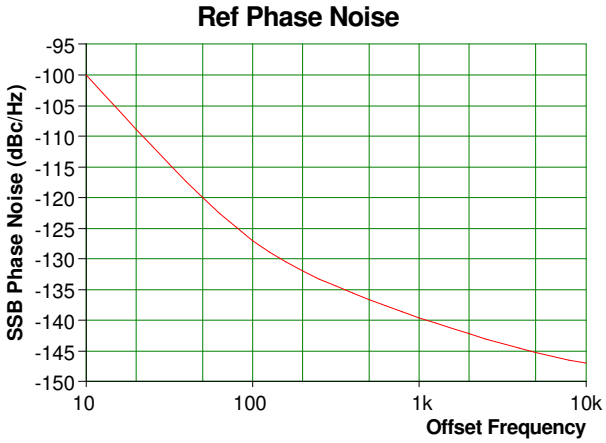


Figura 32. Característica del ruido de fase de la referencia externa

A posteriori introducimos la característica del ruido de fase de nuestro VCO escogido.

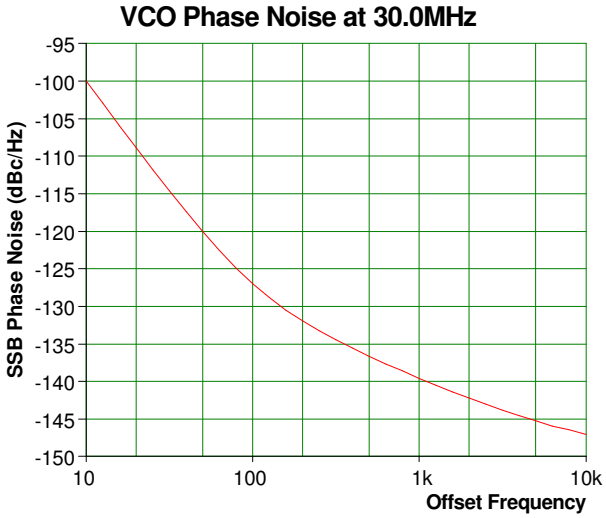


Figura 33. Característica del ruido de fase de la referencia a 30MHz

El sintetizador final simulado es como el que sigue, en este caso utilizando un filtro de orden cuatro como lazo del bucle de PLL

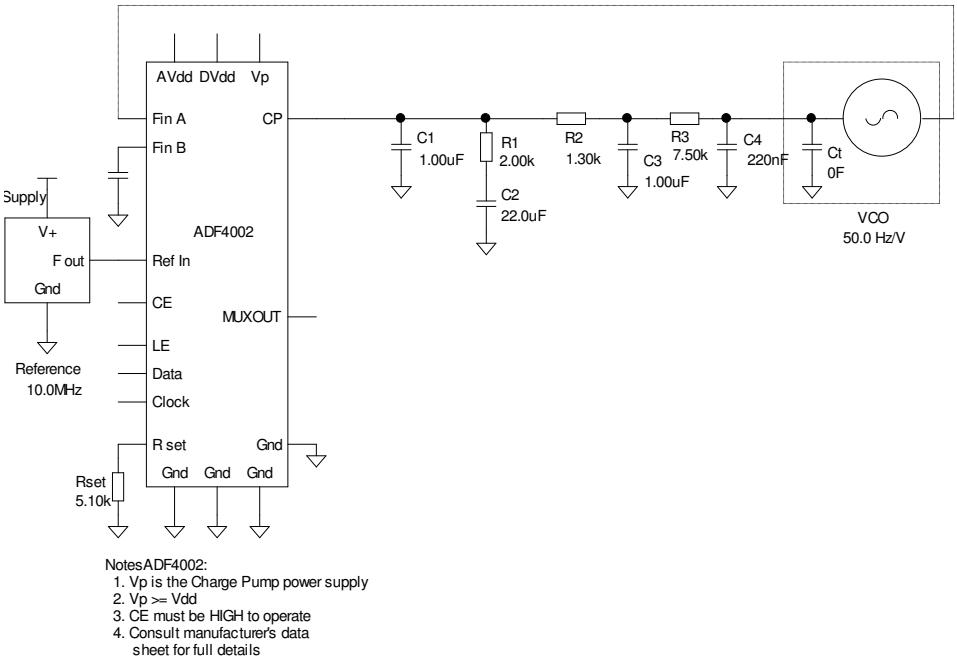
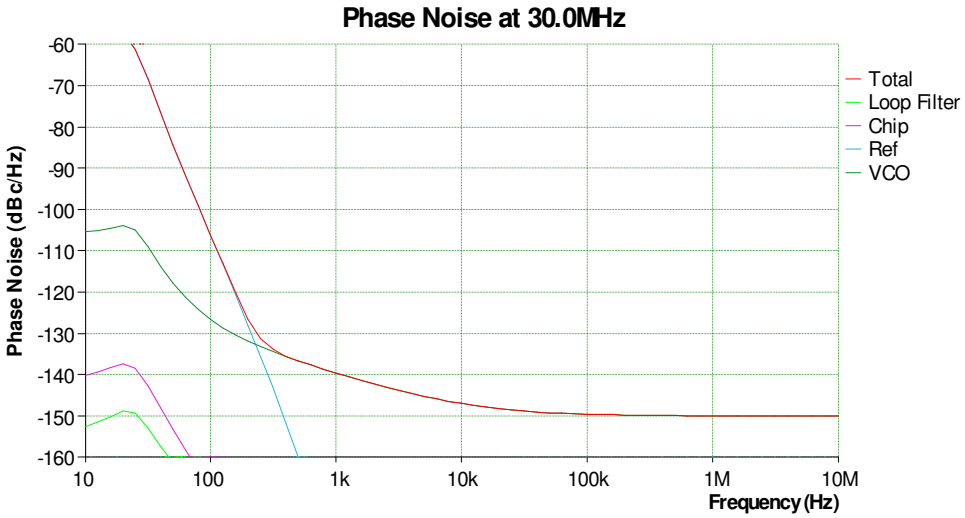


Figura 34. Esquematico del bucle pll completo

Los resultados a nivel de ruido de fase que da el simulador son los siguientes:



Phase Noise Table

Freq	Total	VCO	Ref	Chip	Filter
1.00	-23.37	-109.0	-23.37	-142.4	-165.9
10.0	-51.10	-105.3	-51.10	-140.1	-152.5
100	-106.2	-126.6	-106.2	-168.2	-171.7
1.00k	-139.5	-139.5	-185.9	-235.0	-208.6
10.0k	-147.0	-147.0	-275.5	-299.8	-248.6
100k	-149.6	-149.6	-300.0	-300.0	-288.2
1.00M	-150.0	-150.0	-300.0	-300.0	-300.0

3.6 DIVISOR ACTIVO DE LA SEÑAL DE REFERENCIA

Debemos suministrar la frecuencia de referencia sintetizada de 30MHz a nuestros respectivos osciladores locales para generar la OL1, y OL2 de nuestro sistema. Para ello debemos diseñar un divisor activo para repartir dicha señal, sin pérdidas de nivel. A la salida del sintetizador de 30MHz tenemos un nivel de señal aproximado de –4dB. Esta señal debe repartirse en dos ramas por igual, para la entrada de la referencia de cada uno de nuestros PLL. Este dispositivo necesita de unos +7dBm para funcionar correctamente, con lo cual a parte de dividir la señal debemos ganar nivel.

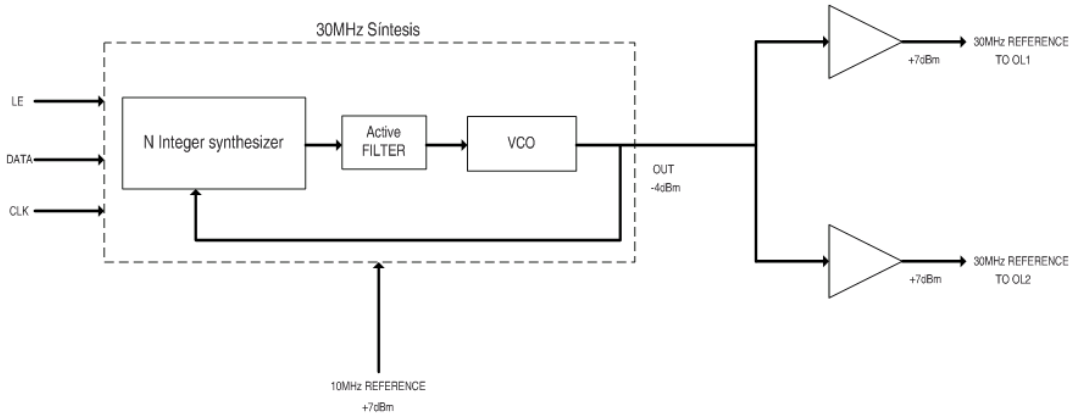


Figura 35. Esquema general de funcionamiento de la división de 30mhz

3.6.1 ANÁLISIS TEMPORAL

A la salida del bucle PLL tenemos una señal de 30MHz con un nivel de –4dBm, esto son aproximadamente 0,4Vpp. Necesitamos una señal de +7dBm, con lo que tendremos que amplificar la señal 3,5dB para conseguir los 1,4Vpp requeridos.

La topología utilizada en el diseño es la descrita a continuación.

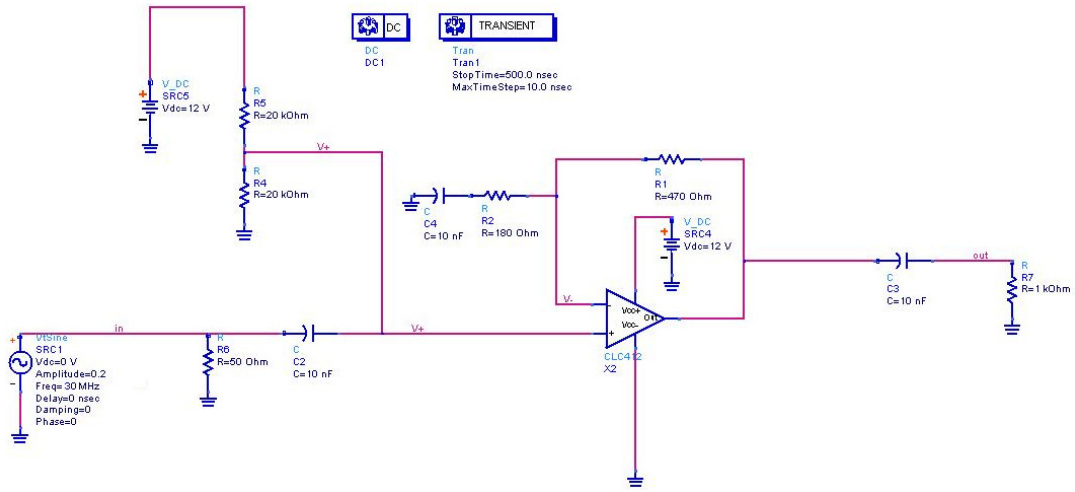


Figura 36. Esquema eléctrico del amplificador

Se decide utilizar el operacional LMH6715 con alimentación no simétrica pues no interesa tener tensiones negativas en el circuito por estar realizadas por generadores de señales cuadradas que pueden producir muchos armónicos difíciles de filtrar en el circuito. Entonces se añade al circuito un offset en DC a la mitad de la tensión de alimentación del operacional para poder hacer trabajar correctamente el operacional a sus límites de funcionamiento.

Si hacemos una simulación del circuito temporal obtenemos una respuesta como la siguiente:

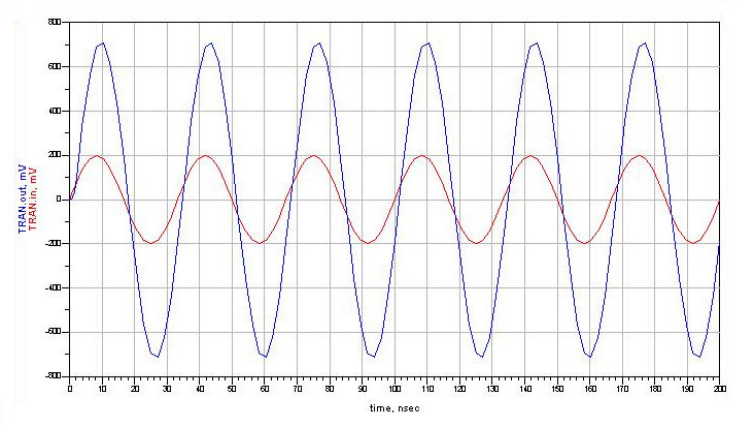


Figura 37. Respuesta a nivel temporal del amplificador

Como puede observarse, el nivel de señal de entrada se establece a 0,4Vpp que son los –4dBm que tendremos a la salida del sintetizador de la frecuencia de 30MHz. A la salida obtenemos la señal amplificada de manera que la señal de salida tiene un nivel de 1,4Vpp, que son los +7dBm requeridos a la entrada de referencia de nuestro PLL.

3.6.2 ANÁLISIS EN AC

Si hacemos el análisis en AC del mismo circuito anterior obtendremos la resupuesta del circuito en frecuencia:

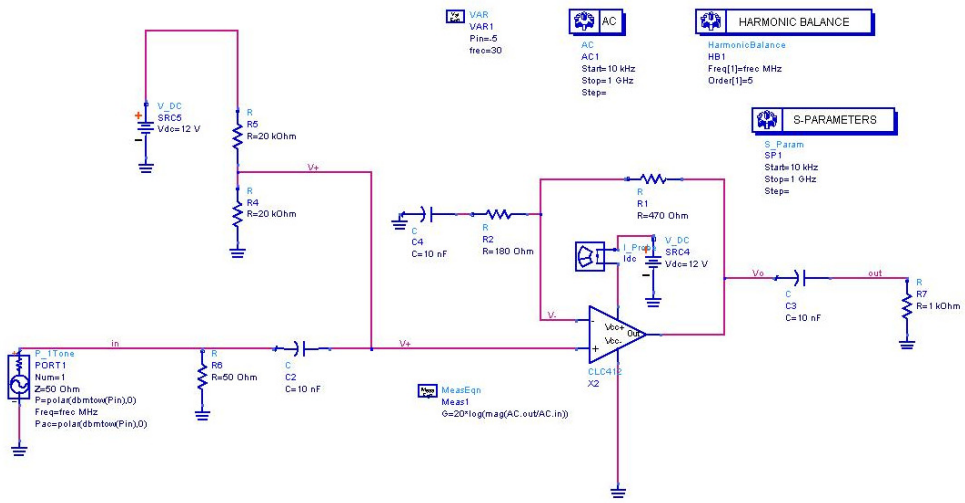


Figura 38. Estudio en AC del amplificador operacional

En la primera gráfica podemos observar que la ganancia que obtenemos es aproximadamente de 11dB para la frecuencia de interés nuestra de 30MHz. En la segunda representación observamos que la tensión en AC del sistema se mantiene a 0,635V hasta llegado los 100MHz aproximadamente, con lo cual nos aseguramos que el integrado funcionará correctamente a 30MHz.

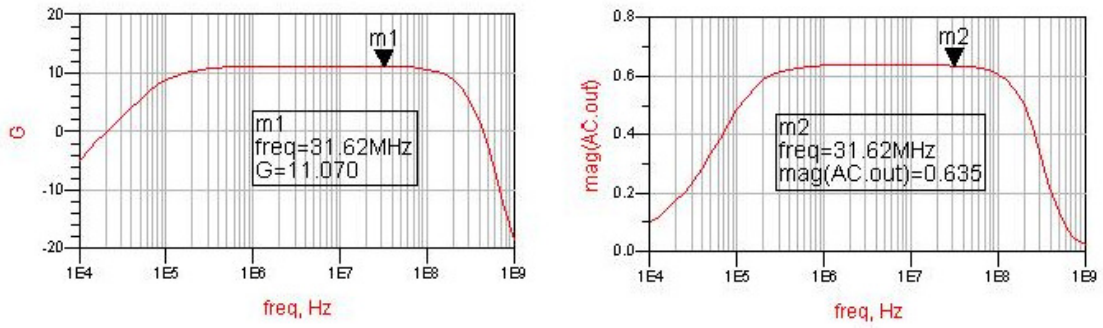


Figura 39. Respuesta en ganancia del amplificador

Finalmente analizamos para qué valores de tensión de entrada conseguimos que el sistema mantenga su ganancia de 11dB. Como puede observarse en la figura, para un nivel de entrada de 12dB que son aproximadamente 2,5Vpp, el integrado empieza a perder su ganancia. Como nosotros nos moveremos con señales de entrada en torno los 0,5Vpp es suficiente la topología utilizada.

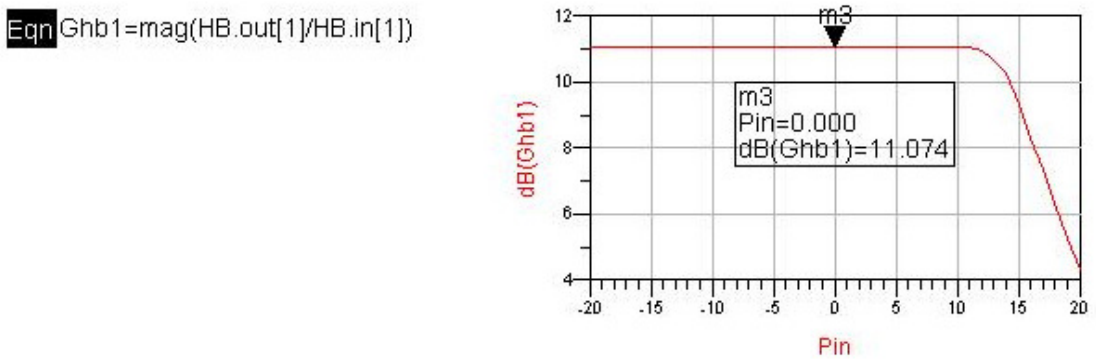


Figura 40. Límites de ganancia del amplificador operacional.

3.6.3 ANÁLISIS CON DOBLE RAMAL

Una vez verificado que nuestro operacional funciona correctamente tanto a nivel frecuencial como temporal y vistos los límites del mismo, simulamos el sistema completo, con los dos ramales de señal que necesitamos para asegurarnos del correcto funcionamiento del sistema completo.

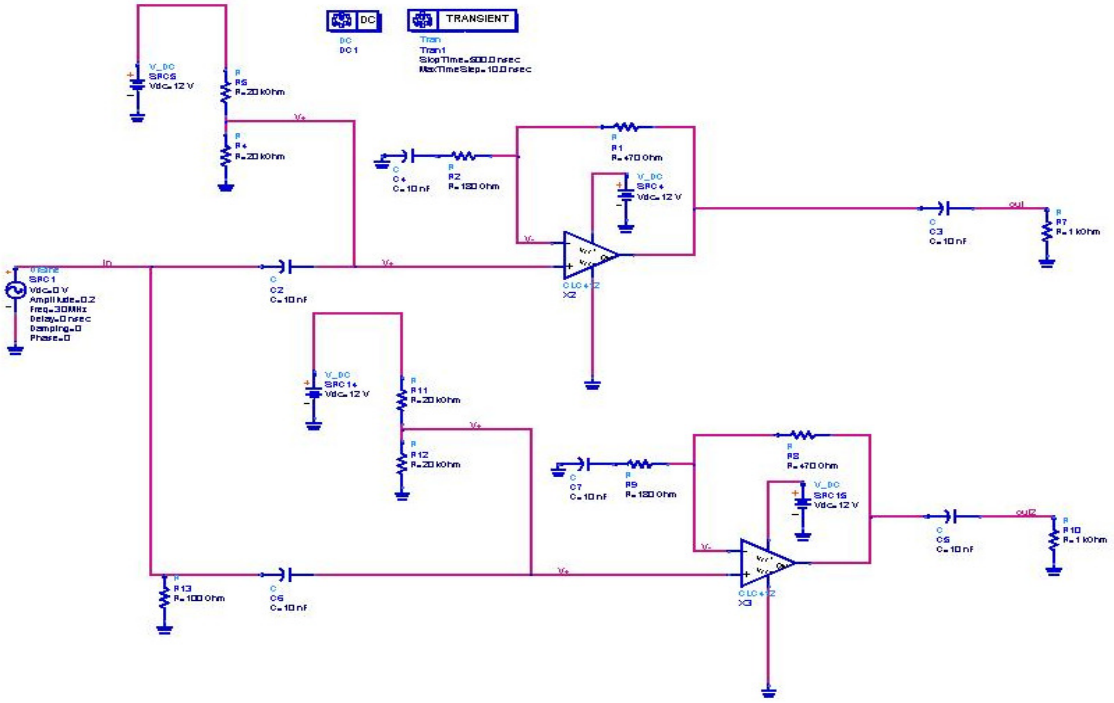


Figura 41. Análisis con doble amplificador operacional

Finalmente observamos a nivel temporal que el sistema sigue funcionando correctamente, obteniendo dos señales de igual magnitud a 30MHz.

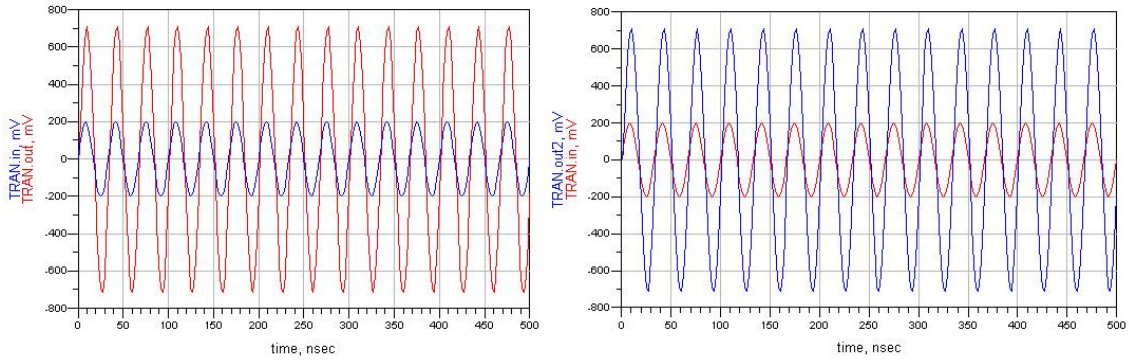


Figura 42. Respuesta temporal de funcionamiento de los dos amplificadores

3.7 PRIMER OSCILADOR LOCAL

3.7.1 ELECCION DE COMPONENTES

Para la realización del sintetizador se escoge el integrado ADF4106 de ANALOG DEVICES, porque es el que proporciona mejor ruido de fase para sintetizar las frecuencias de 1000MHz a 2000MHz con pasos de 5MHz.

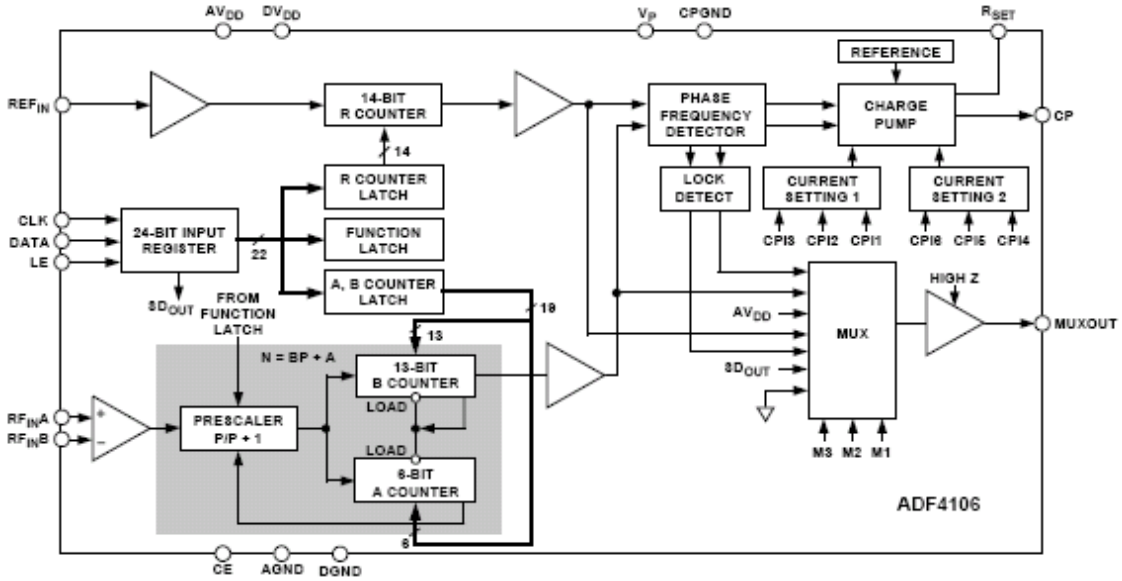
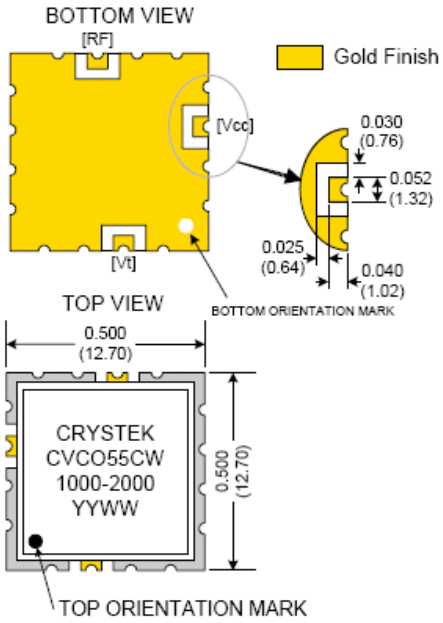


Figura 43. Diagrama de bloques interno del ADF4106

Debemos de sintetizar frecuencias de 1505MHz a 1890MHz. En el mercado encontramos el VCO de CRYSTEK CVCO55CW-1000-2000 que nos sirve para dicho propósito. Entre sus características destacar:



Tuning Sensitivity = 53MHz/V
Phase Noise at 10kHz offset =-100dBc/Hz
Phase Noise at 100kHz offset =-124dBc/Hz
Supply Voltage=+10V
Tuning Voltage= +1V a +20V

Como el VCO escogido tiene un Tuning Voltage de +20V, necesitamos poder llegar a inyectar dicho valor al dispositivo con lo cual debemos de poner un filtro de bucle PLL activo mediante amplificador operacional alimentado a dicho voltage de +20V. Para dicho cometido debemos escoger un operacional de bajo ruido, por ejemplo el OP27 de ANALOG DEVICES con un *voltage noise* de 3nV/Hz.

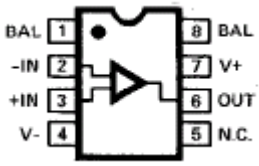


Figura 44. Footprint del integrado OP27

3.7.2 SIMULACIÓN

Escogemos como referencia los valores de ruido de fase de los 30MHz sintetizados anteriormente.

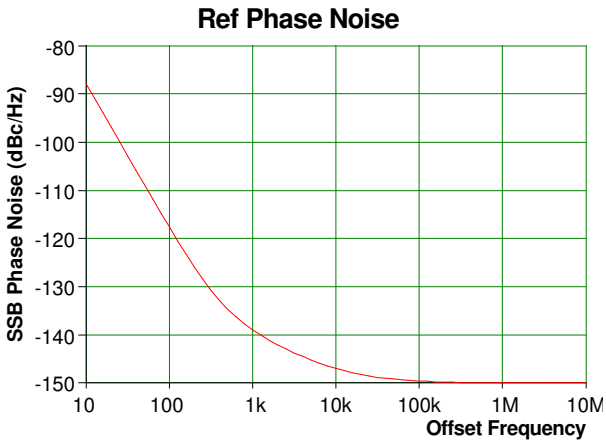


Figura 45. Característica del ruido de fase de los 30MHz sintetitzados

Añadimos el phase noise descrito del fabricante del VCO escogido.

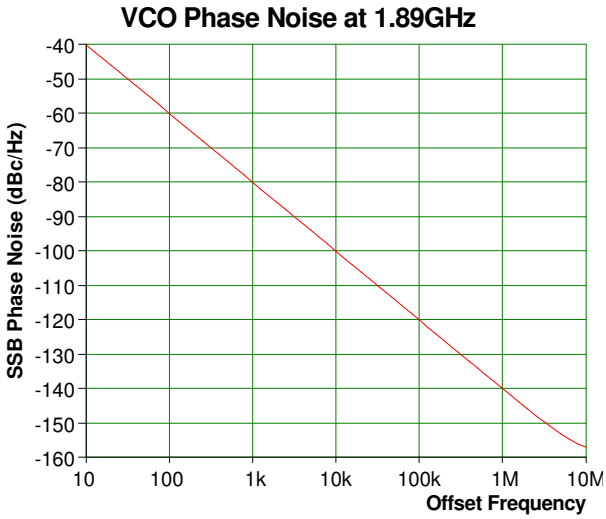


Figura 46. Característica de ruido de fase del VCO

El circuito queda de la siguiente manera:

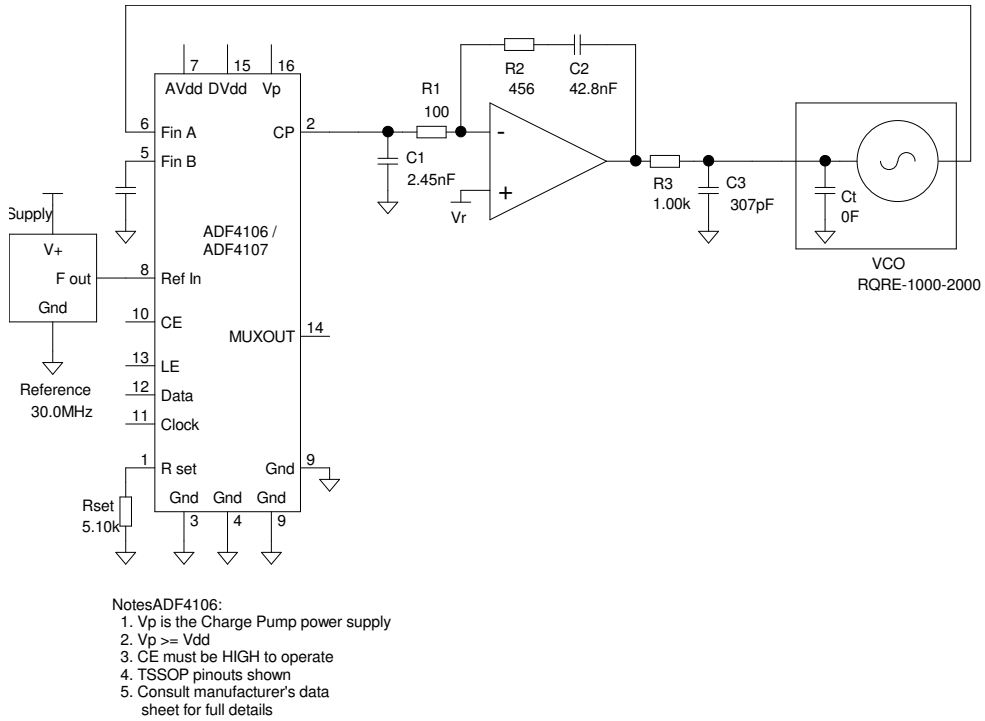
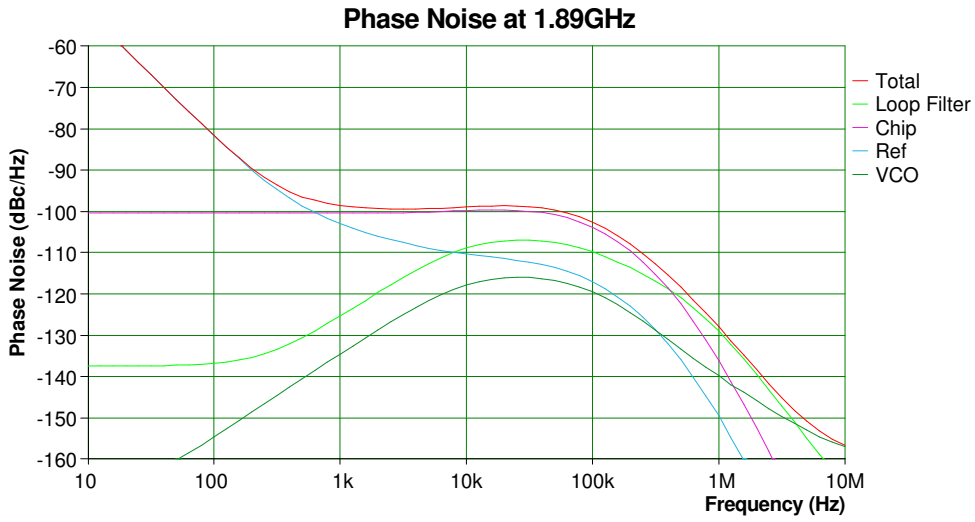


Figura 47. Esquema eléctrico completo del PLL

Y los resultados de la simulación son los siguientes:



Phase Noise Table

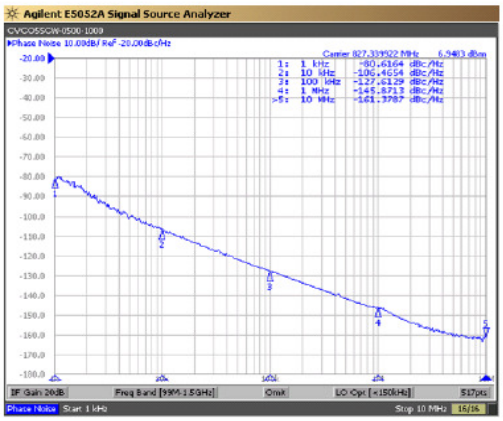
Freq	Total	VCO	Ref	Chip	Filter
1.00	-21.97	-194.5	-21.97	-100.5	-137.4
10.0	-51.96	-174.5	-51.96	-100.5	-137.4
100	-81.61	-154.5	-81.67	-100.5	-136.8
1.00k	-98.49	-134.6	-102.9	-100.4	-125.3
3.00k	-99.46	-125.4	-107.4	-100.3	-116.4
10.0k	-98.90	-117.8	-110.3	-99.79	-108.9
100k	-102.6	-119.4	-117.0	-103.8	-109.8
1.00M	-127.9	-139.8	-149.6	-136.0	-129.0

3.8 SEGUNDO OSCILADOR LOCAL

3.8.1 ELECCIÓN DE COMPONENTES

Para la realización del sintetizador utilizaremos el integrado de ANALOG DEVICES ADF4106. Para obtener las frecuencias del segundo OL requeridas en la tabla de canalizaciones, de 992MHz a 996MHz utilizaremos el VCO de CRYSTEK CVCO55CW-500-1000 que posee las siguientes características:

Phase Noise (1 Hz BW, Typical)



Tuning Sensitivity = 60MHz/V
Phase Noise at 10kHz offset =-104dBc/Hz
Phase Noise at 100kHz offset =-127dBc/Hz
Supply Voltage=+12V
Tuning Voltage= +0,5V a +18V

Como en el caso del oscilador anterior, el *tuning voltage* requerido es de hasta +18V, superior al valor de alimentación del integrado ADF4106. Por lo tanto, tendremos que añadir un filtro de bucle PLL activo mediante el operacional de bajo ruido OP27 de ANALOG DEVICES.

3.8.2 SIMULACIÓN

La señal de referencia es la misma que en el caso del anterior oscilador local realizado.

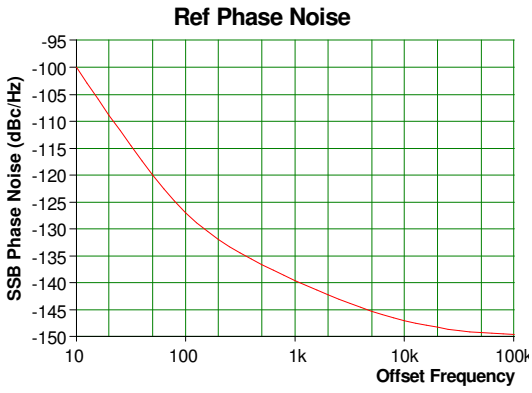


Figura 48. Característica del ruido de fase de la referencia de 30MHz

La característica del VCO es la siguiente:

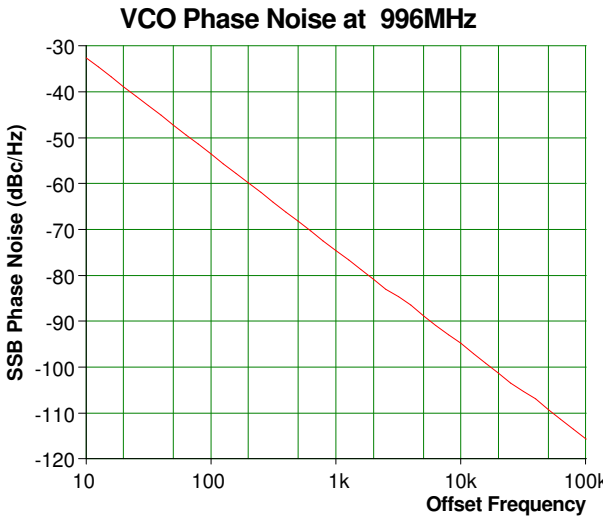


Figura 49. Característica de ruido de fase del VCO para frecuencia de 996MHz

El diseño eléctrico queda como sigue:

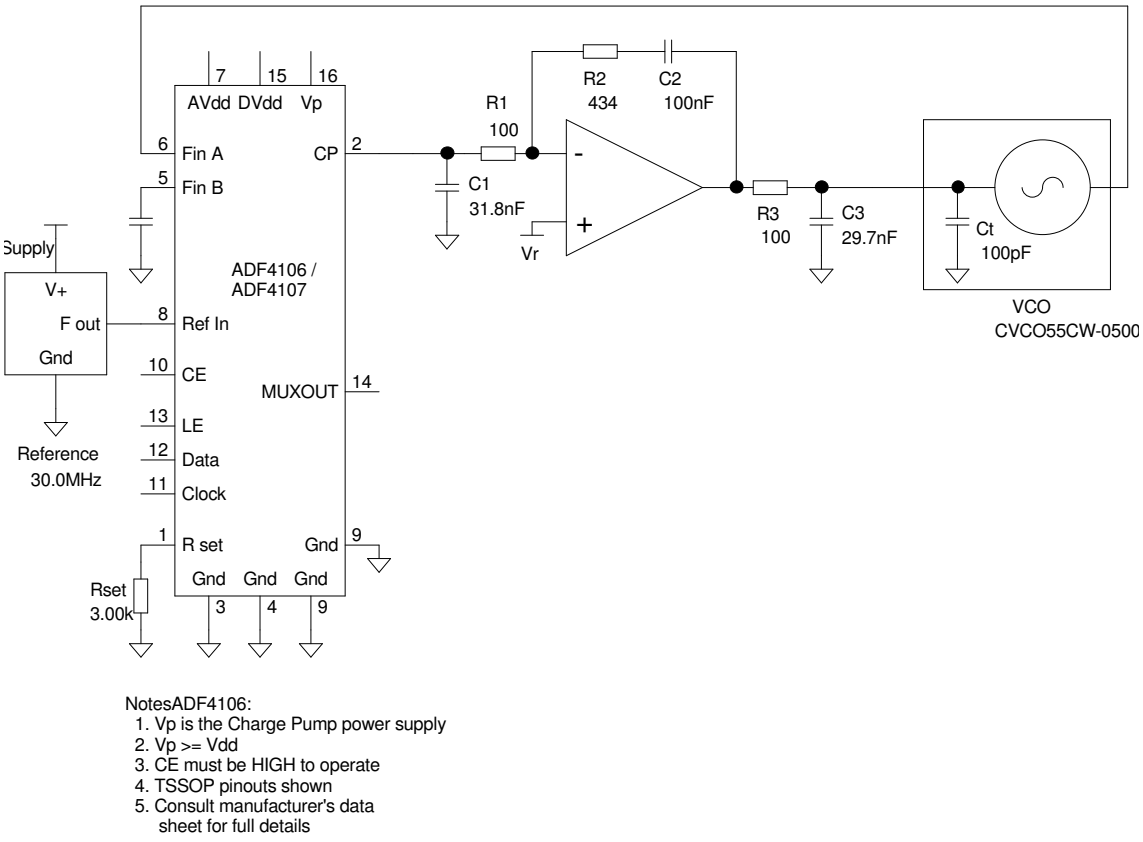
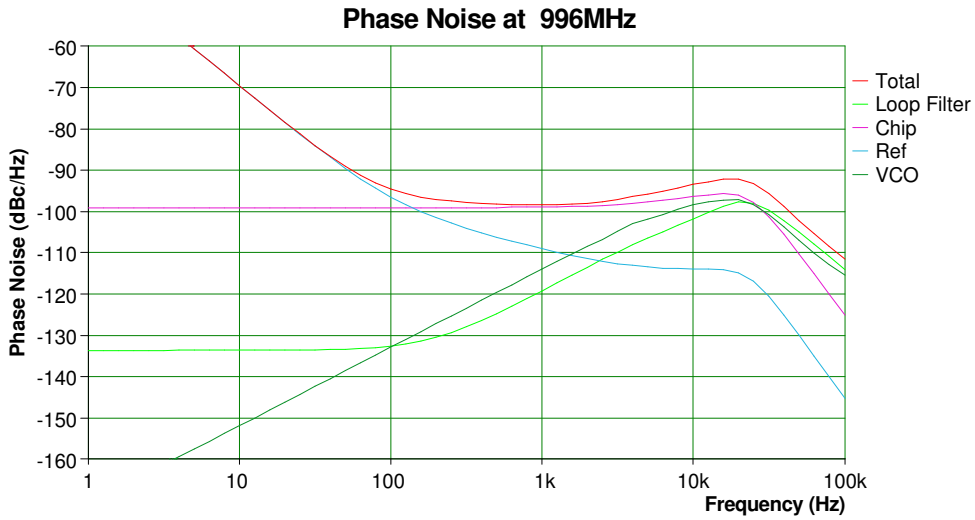


Figura 50. Esquema eléctrico del PLL completo.

Dando como resultado en la simulación la siguiente característica de ruido de fase:



Phase Noise Table

Freq	Total	VCO	Ref	Chip	Filter
1.00	-39.58	-170.8	-39.58	-99.03	-133.6
10.0	-69.52	-151.9	-69.53	-99.03	-133.6
100	-94.59	-132.9	-96.52	-99.03	-132.6
1.00k	-98.38	-114.0	-109.0	-98.94	-119.2
3.00k	-97.21	-105.3	-112.5	-98.37	-110.2
10.0k	-93.51	-98.37	-113.9	-96.36	-101.9
100k	-111.5	-115.4	-145.3	-125.1	-114.1
1.00M	-137.9	-138.1	-203.5	-183.0	-152.0

3.9 ALIMENTACIONES

Partimos de una tensión nominal externa de +24Vdc, habitual en equipos de comunicaciones. A partir de esta tensión tenemos que generar las tensiones necesarias para alimentar toda la estructura electrónica de nuestro circuito PCB.

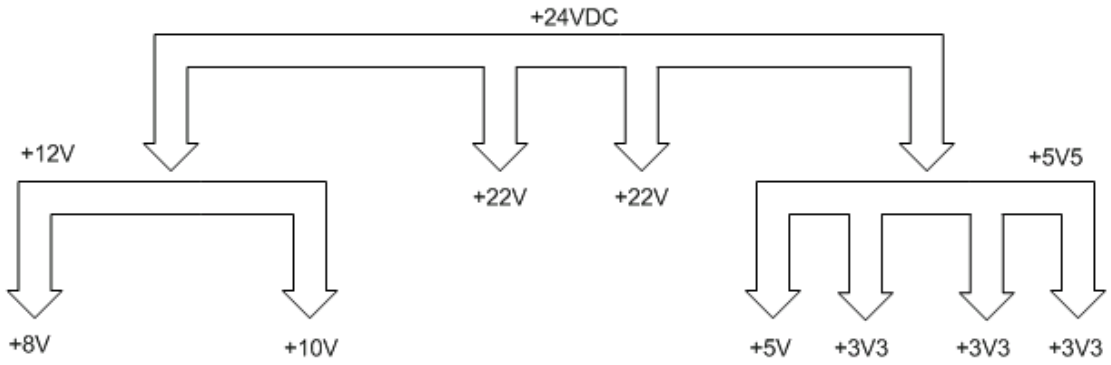


Figura 51. Repartición de tensiones dentro el circuito eléctrico

Utilizamos dos convertidores tipo BUCK para bajar la tensión continua de +24Vdc a las tensiones intermedias de +12Vdc y +5V5. Para ello utilizamos el integrado TPS5450DDA de TEXAS INSTRUMENTS capaz de entregar hasta 2,5A y con tensión de salida regulable mediante divisor de tensión.

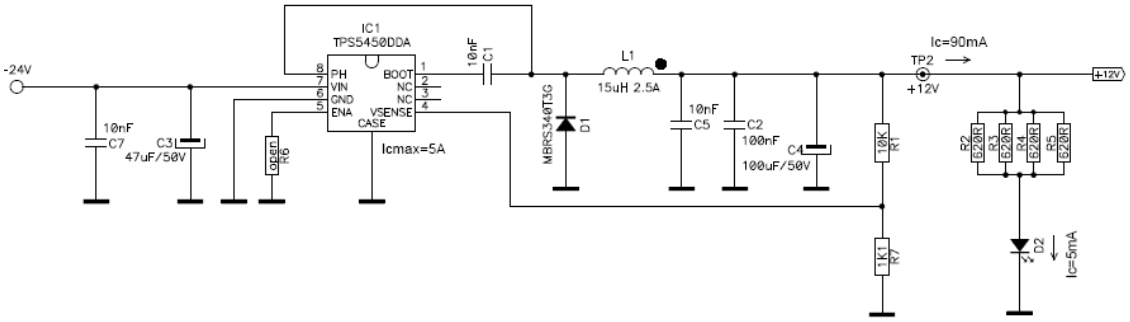


Figura 52. Esquema eléctrico del convertidor dc/dc para entregar 12V

Estas tensiones intermedias las vamos a utilizar para alimentar reguladores de tensión del tipo LDO's (Low Voltage Dropout) que alimentarán respectivamente los integrados del circuito. La razón de utilizar alimentaciones intermedias es disminuir la potencia de disipación de los LDO's utilizados.

Para alimentar los integrados PLL utilizamos los reguladores LP38693SD de voltage fijo de +5V y +3V3. Son reguladores especialmente indicados para alimentar componentes que requieren precisión.

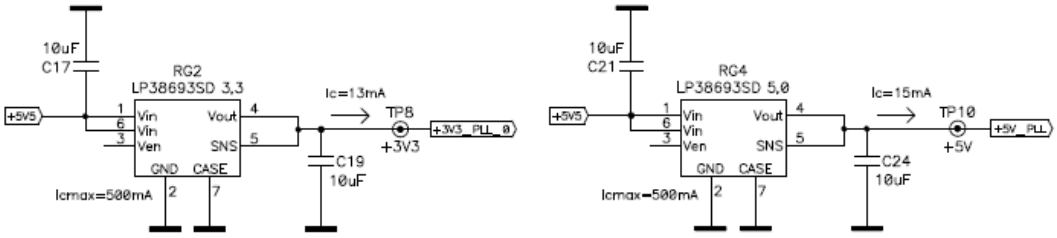


Figura 53. Esquemas eléctricos de los convertidores DC/DC de 3V3 y 5V

Para alimentar los VCO's y los amplificadores operacionales del circuito, utilizamos el regulador lineal TL317CD con tensión de salida ajustable mediante divisor de tensión.

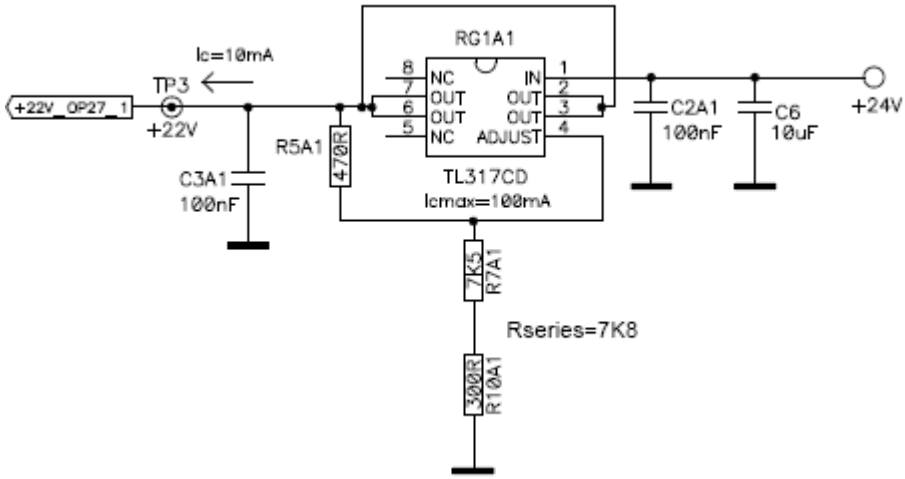
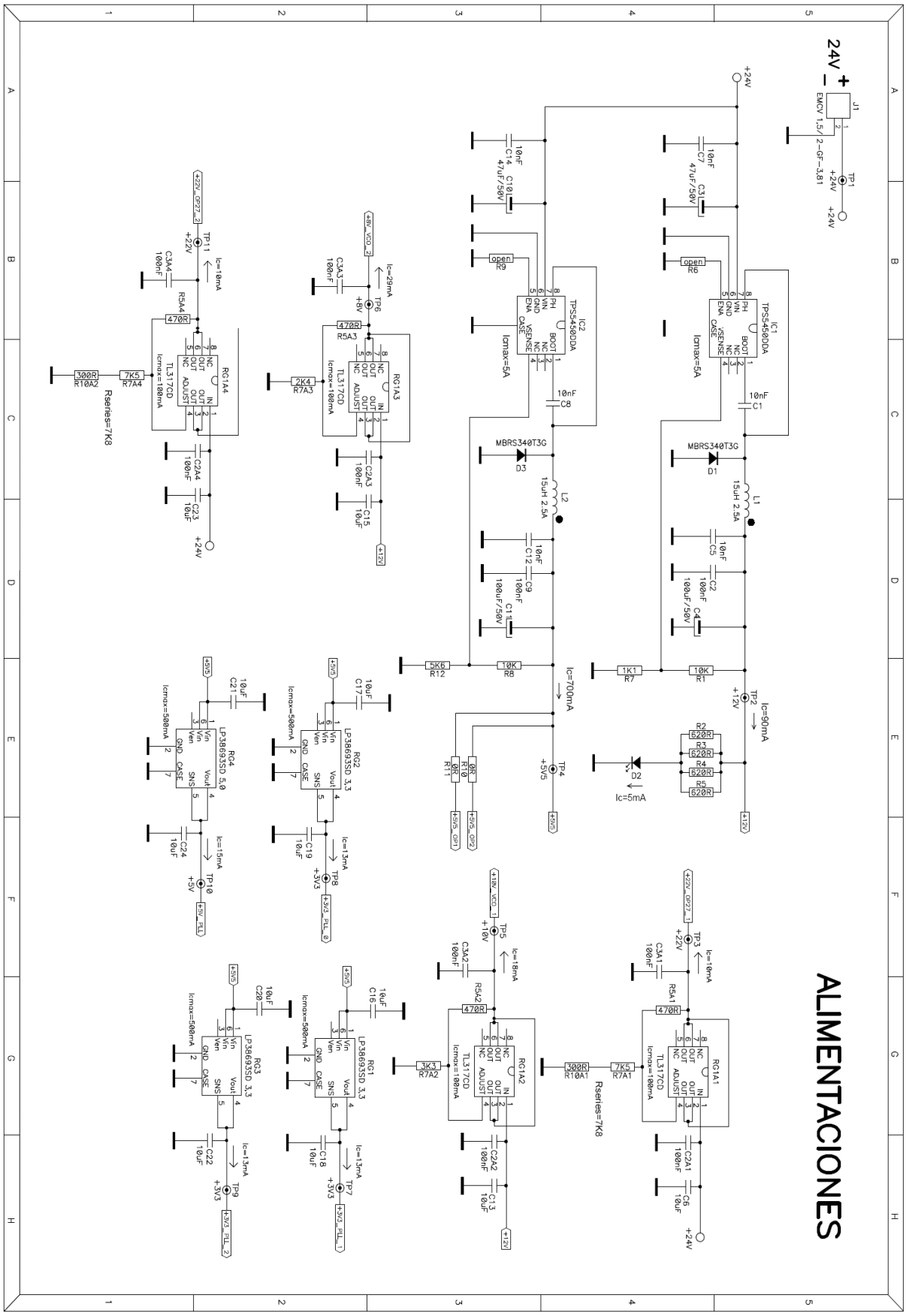


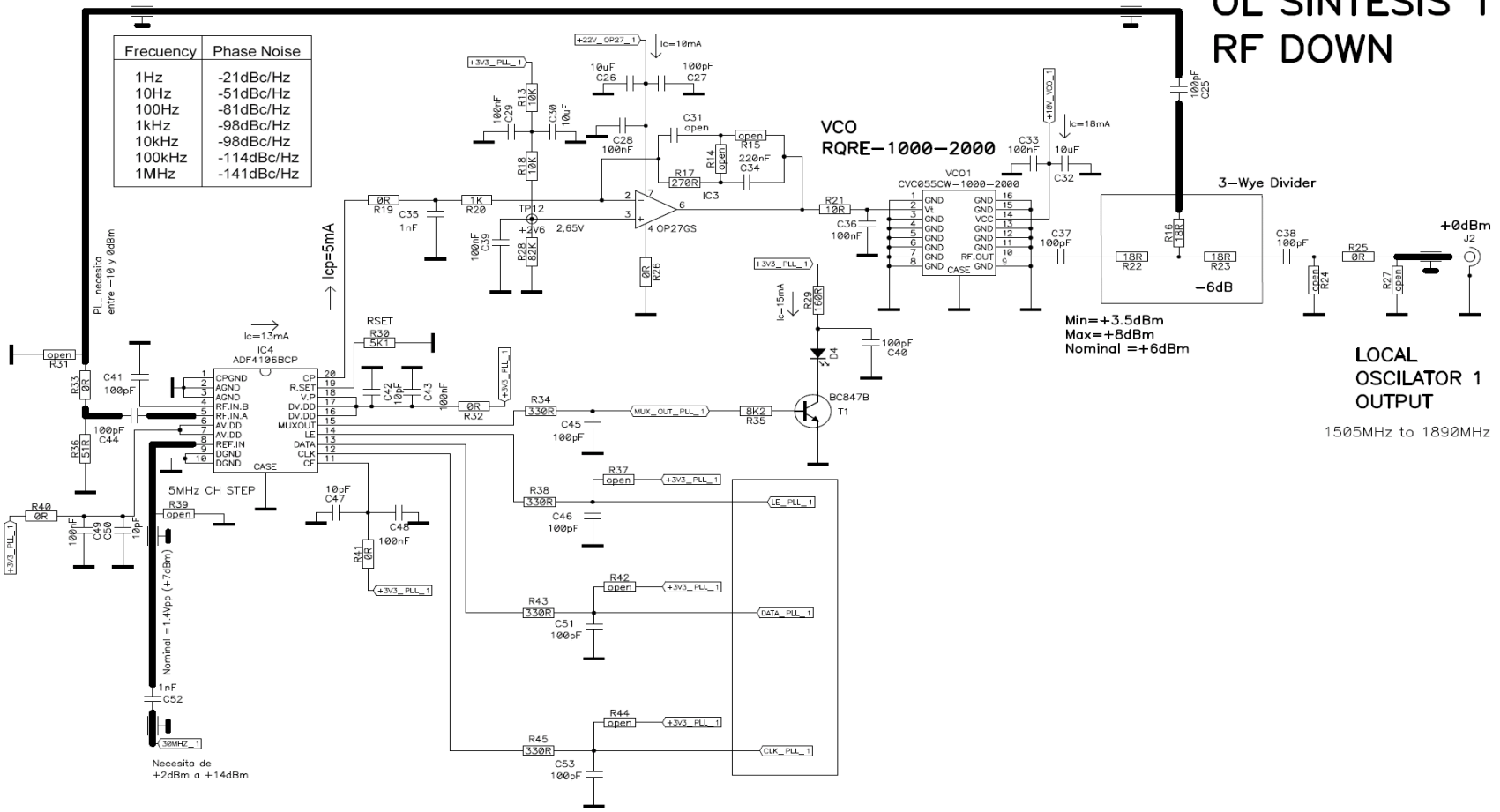
Figura 54. Esquema eléctrico del convertidor dc/dc a 22V

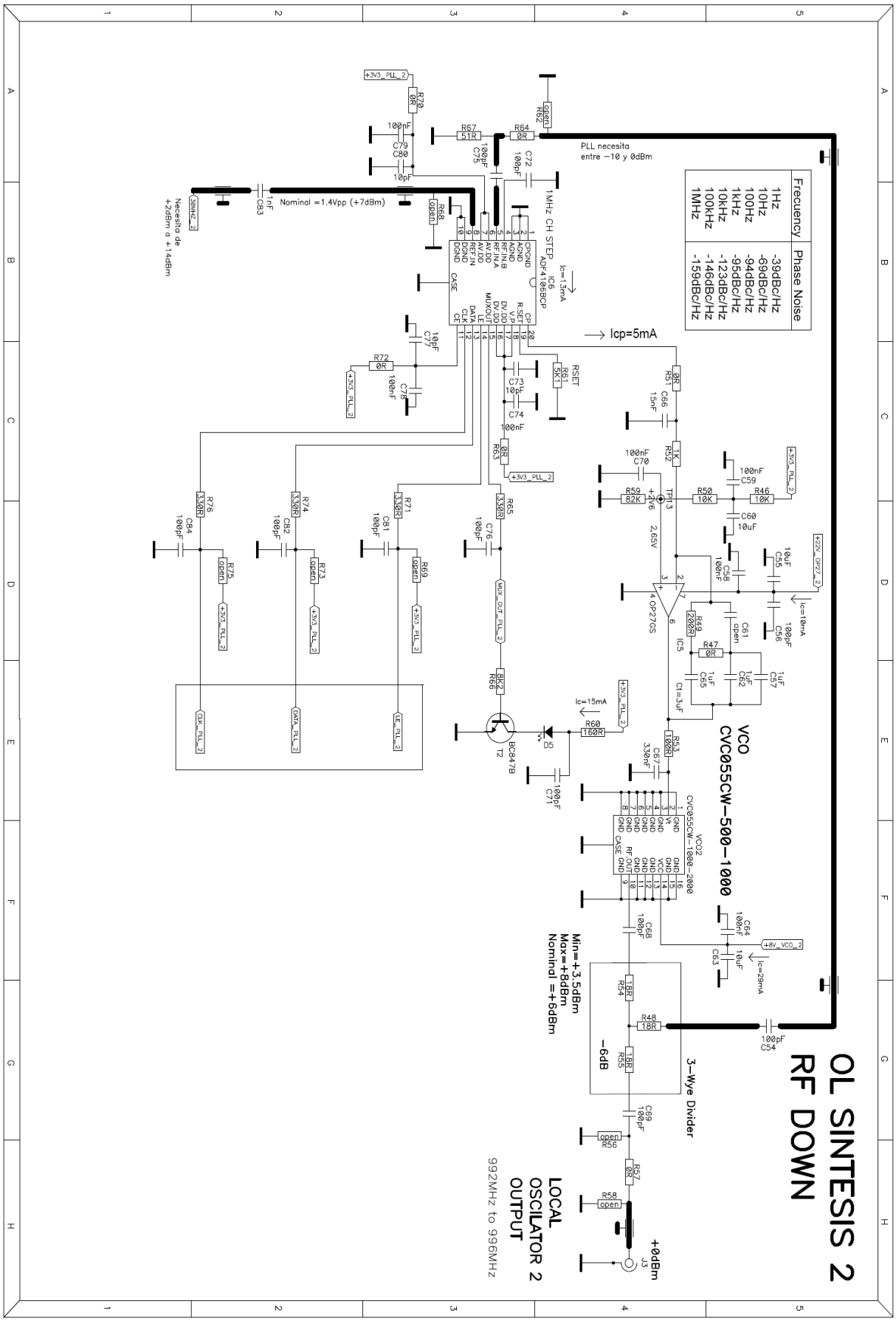
3.10 DISEÑO ESQUEMA ELÉCTRICO

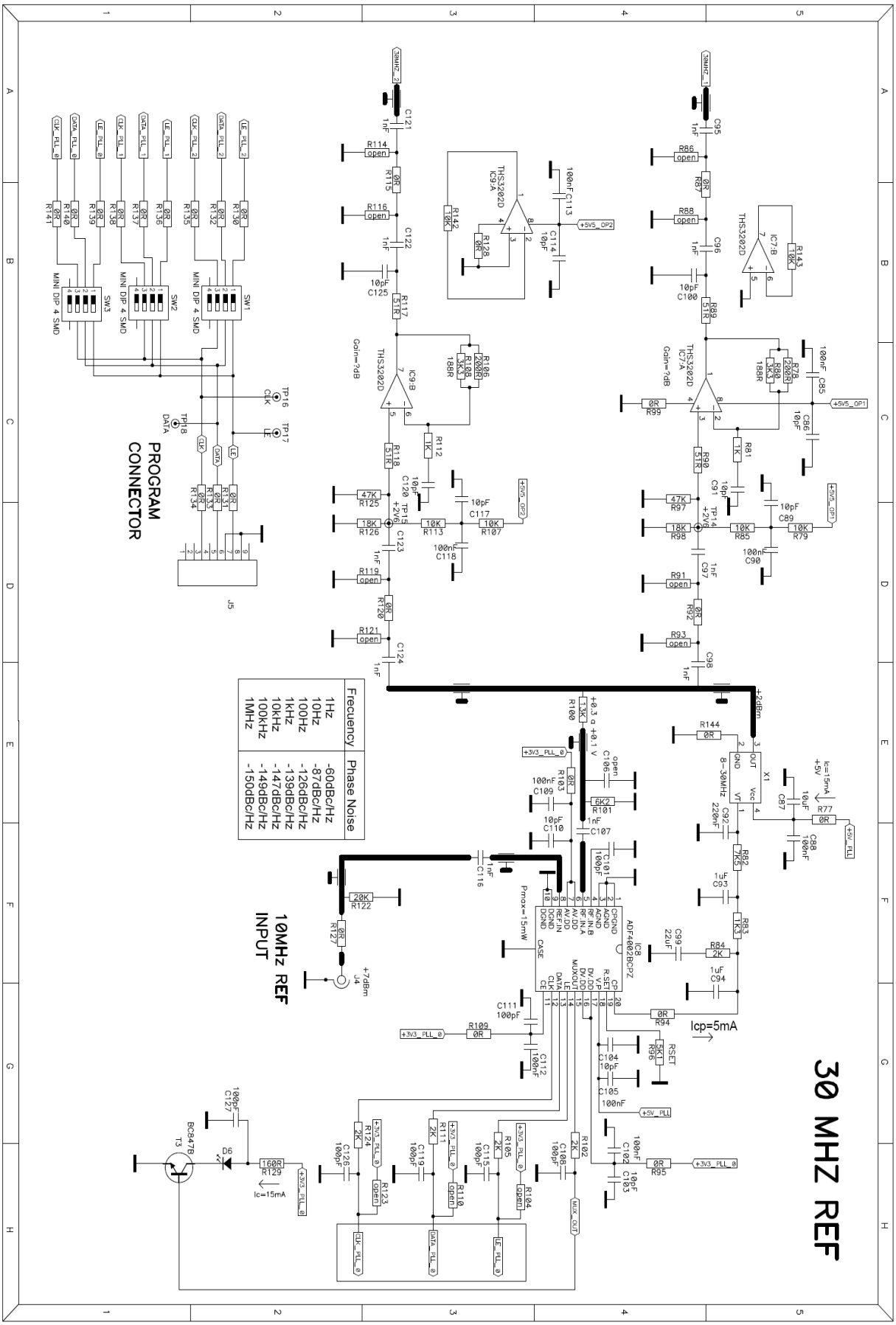


OL SINTESIS 1
RF DOWN

Frecuency	Phase Noise
1Hz	-21dBc/Hz
10Hz	-51dBc/Hz
100Hz	-81dBc/Hz
1kHz	-98dBc/Hz
10kHz	-98dBc/Hz
100kHz	-114dBc/Hz
1MHz	-141dBc/Hz




OL SINTESIS 2
RF DOWN
LOCAL
OSCILATOR 2
OUTPUT
992MHz to 996MHz
VCO
CVC055CW-500-1000
3-Wye Divider
-6dB
+0dBm
Min=+3.5dBm
Max=+8dBm
Nominal =+6dBm
PLL necesita
entre -10 y 0dBm
Nominal =1.4Vpp (+7dBm)
Necesita de
+2dBm a +14dBm
Icp=5mA
1MHz CH STEP
Frecuency
Phase Noise
1Hz -39dBc/Hz
10Hz -69dBc/Hz
100Hz -94dBc/Hz
1kHz -95dBc/Hz
10kHz -123dBc/Hz
100kHz -146dBc/Hz
1MHz -159dBc/Hz

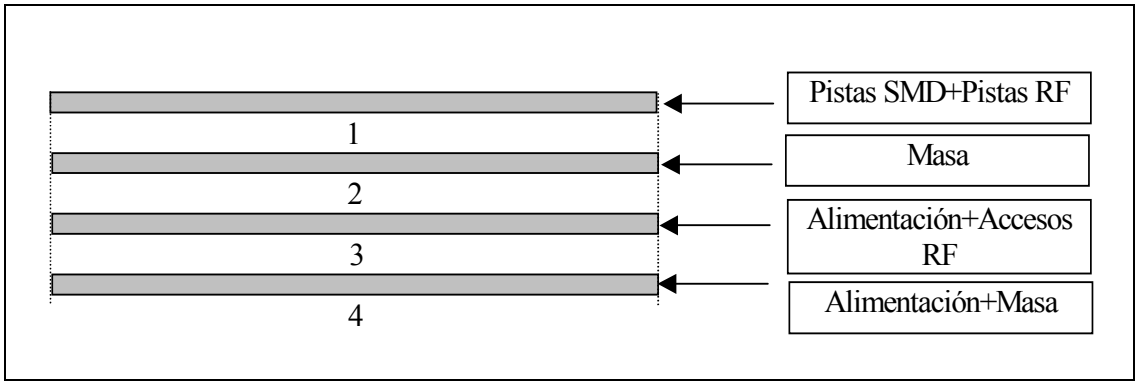

30 MHZ REF
PROGRAM CONNECTOR
10MHz REF INPUT
Icp=5mA
Frecuency
Phase Noise
1Hz -60dBc/Hz
10Hz -87dBc/Hz
100Hz -126dBc/Hz
1kHz -139dBc/Hz
10kHz -147dBc/Hz
100kHz -149dBc/Hz
1MHz -150dBc/Hz

3.11 DESCRIPTIVA DE DISEÑO PCB

Se realiza el diseño de la placa de circuito impreso en multicapa a 4 capas, debido a la complejidad del circuito y de la sensibilidad de pistas de RF. Como material para la realización de la PCB se utiliza FR4 con las siguientes propiedades eléctricas:

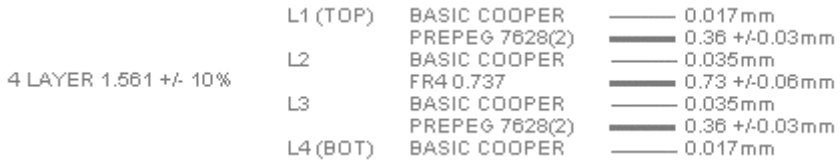
MATERIAL	
DIMENSIONES / CLASE / CORTE: *Size / Class / Panelization*	95 x 130 mm /CLASE 4 / FRESADO
MATERIAL / *Material* :	FR4
GROSOR / *Width*:	1.561 mm ± 15%mm
CONSTANTE DIELÉCTRICA: *Dielectric constant*	4.32
TANGENTES PERDIDAS / *Loss Tangent*:	0.020
GROSOR COBRE ED ORIGINAL: *Copper Original width*	17 µm
GROSOR COBRE FINAL: *Copper final width*	35 µm
TOLERANCIA DE ATACADO: *Attack tolerances*	+- 50 µm

La distribución de pistas en las 4 capas es la siguiente:



Los planos de masa deben de constituir el blindaje necesario para evitar radiaciones debidas a la transmisión de las señales de referencia. Los accesos de las pistas de RF a los conectores deben hacerse por capa interna para evitar el contacto de la pista con la masa del conector.

Las distancias entre los distintos planos de la PCB y sus tolerancias son los siguientes:



Los tamaños para la correcta adaptación de las diferentes pistas de radio frecuencia se calculan a partir de la utilidad LINECALC de AGILENT y deben de ser los siguientes:

Los tramos de pista de la cara TOP son del tipo MICROSTRIP, que corresponde al tipo MLIN del software. Añadimos las variables para el tipo de material que utilizamos para la fabricación de la PCB:

Er = 4,32 (característica del material)

Mur = 1 (ideal)

H = 0,360 (distancia entre pista TOP y el plano de masa)

T=0,035 (grosor cobre final)

Cond=5,8e7 (conducción del cobre)

TanD=0,02 (tangente de pérdidas)

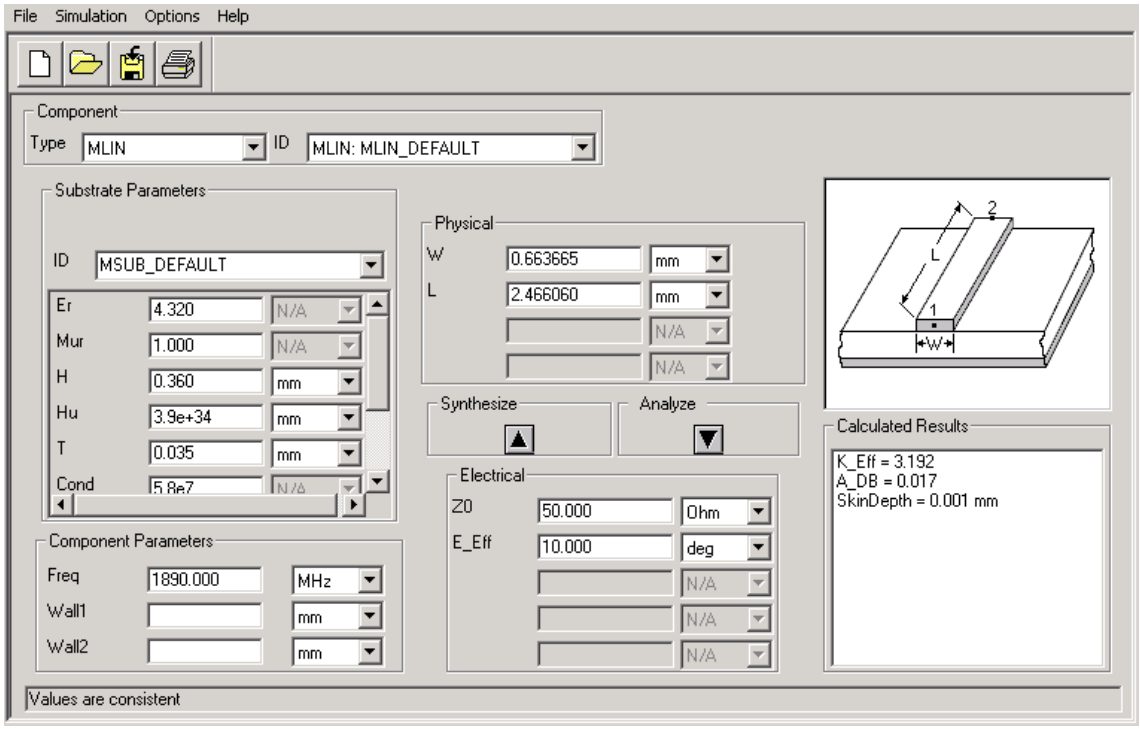


Figura 55. Diseño de pistas adaptadas MICROSTRIP con LINECALC

Como parámetro de frecuencia de análisis a introducir ponemos la frecuencia más alta que necesitamos sintetizar pues será el peor caso, 1890MHz. Si sintetizamos la simulación resulta que necesitamos pistas de grosor 0,66mm si queremos una adaptación de 50 Ohm en la cara TOP de la PCB.

Para adaptar las pistas correspondientes a los accesos a los conectores de RF tenemos que tratar las líneas del tipo STRIPLINE. En este caso la pista de RF pasa entre dos planos de masa y la distancia B entre el plano de masa y la pista de RF es de 1,125mm.

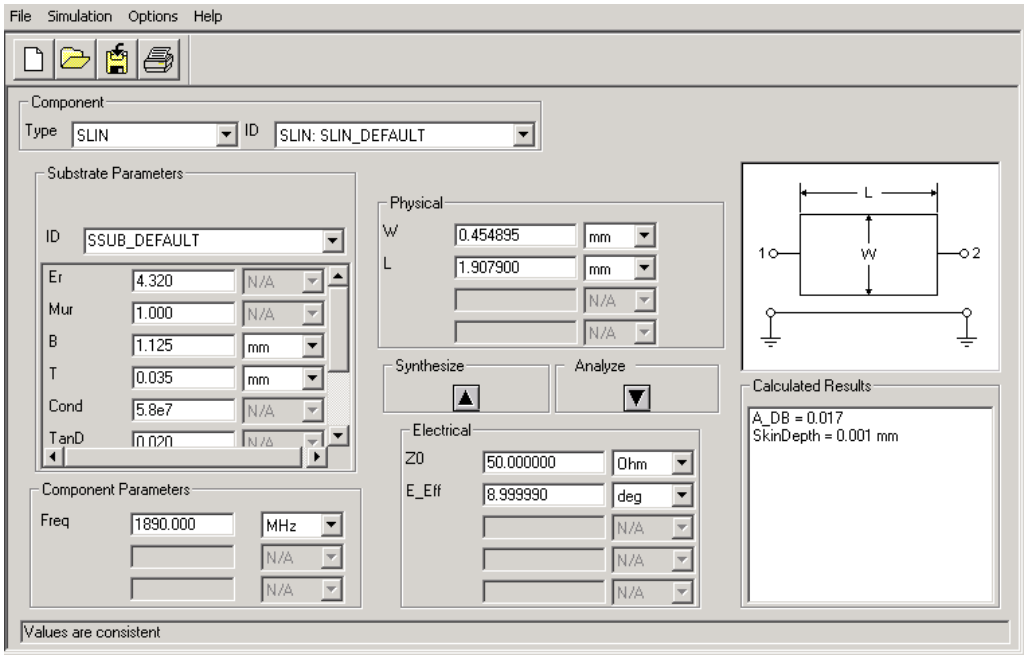


Figura 56. Diseño con LINECALC para pistas STRIPLINE

Si sintetizamos la pista obtenemos que el grosor en este caso de la pista de RF para que tenga una adaptación de 50 Ohms tiene que ser de 0,45mm aproximadamente.

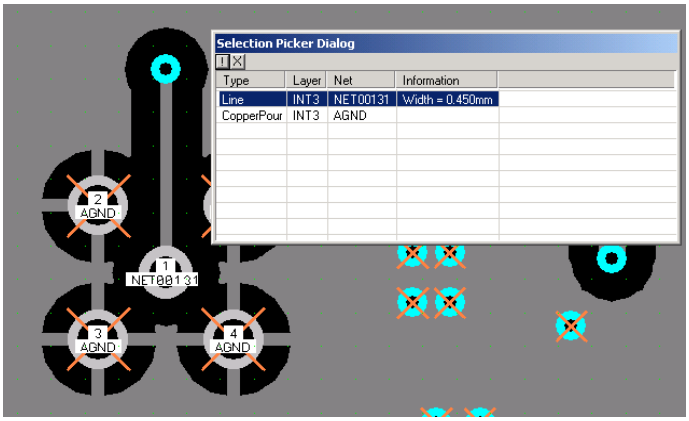


Figura 57. Detalle de acceso a conector de rf en pcb

3.11.1 DISTRIBUCIÓN DE COMPONENTES DENTRO PCB

La disposición de componentes dentro la placa de circuito impreso que se ha seguido es la siguiente:

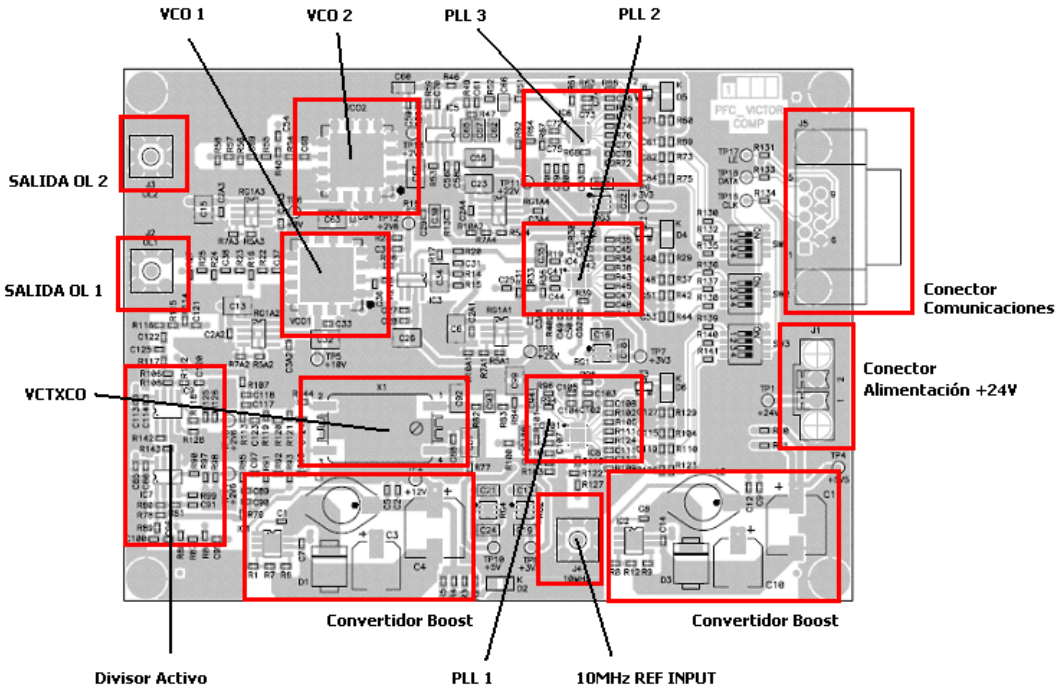


Figura 58. Disposición de componentes dentro la PCB

El conector de Comunicaciones es del tipo DB-9 necesario para la programación externa mediante ordenador de los tres sintetizadores. Los 3 switches de la placa se utilizan para multiplexar las comunicaciones de los 3 integrados PLL's con el conector de comunicaciones.

Los convertidores BOOST son del tipo conmutado capaces de gobernan intensidades superiores a los 5A con lo que es muy importante el diseño layout del mismo para evitar problemas de disipación térmica del mismo y de las propias pistas de alimentación. Para ello se ha seguido las recomendaciones del fabricante del integrado, para su diseño dentro la PCB.

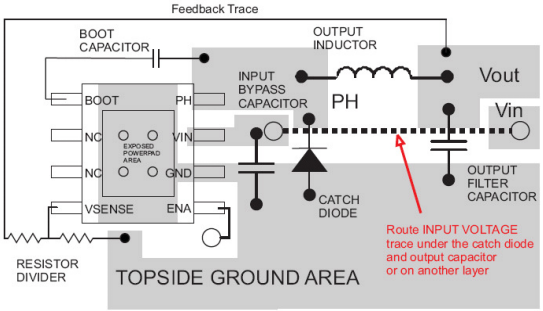


Figura 59. Topología de layout para convertidor boost

3.12 SOFTWARE DE CONTROL DE LOS PLL'S

Para programar los distintos integrados PLL necesitamos un software de control. El propio fabricante de este dispositivo proporciona dicha aplicación software mediante PC gratuitamente. El mismo programa nos sirve para los dos modelos de sintetizadores que utilizamos.

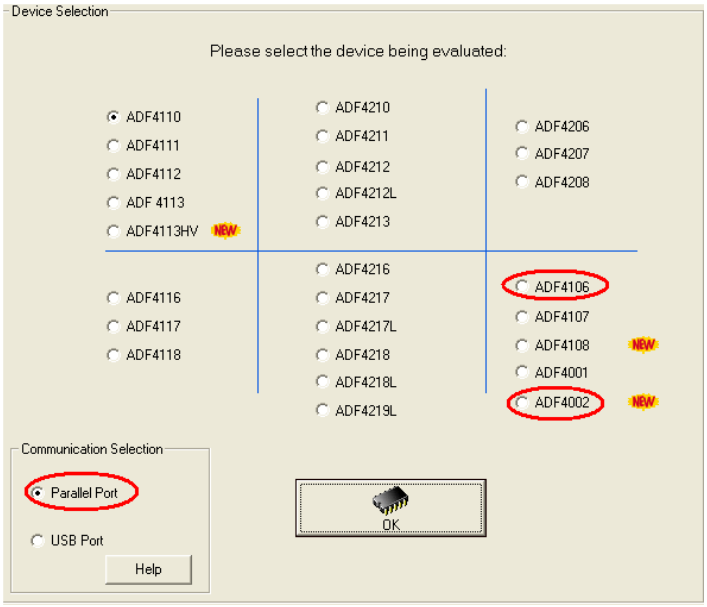


Figura 60. Software de control de los PLL's

En nuestro caso utilizamos el puerto Paralelo de comunicaciones y los integrados ADF4106 y ADF4002 para programar.

El cable utilizado para comunicar la PCB con el ordenador se diseña a partir de las notas de aplicación de ANALOG DEVICES.

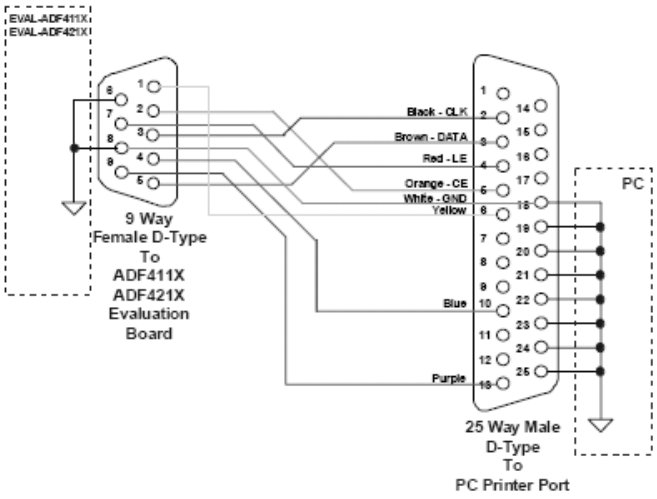


Figura 61. Esquema eléctrico del cable de control del ordenador a la PCB

La página principal de la aplicación de control de los diferentes dispositivos es la siguiente:

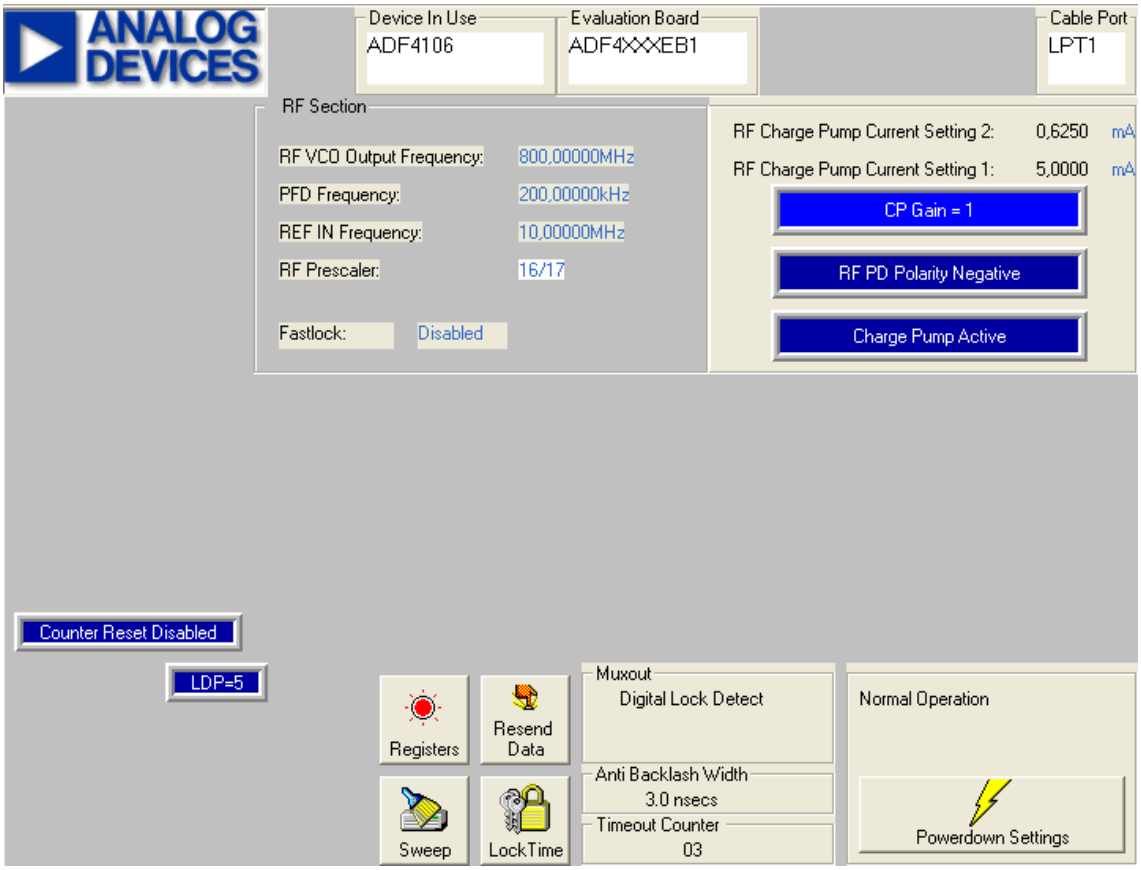


Figura 62. Pantalla de control para los PLL's

En *DEVICE IN USE* se establece el dispositivo que estamos programando, por ejemplo en nuestro caso el ADF4106 o el ADF4002.

En *RF VCO Output Frequency* establecemos el valor de la frecuencia de salida que queremos sintetizar. Así por ejemplo éste valor irá de 1505MHz a 1890MHz para el caso del OL1 y de 992MHz a 996MHz en el caso del OL2.

En *PFD Frequency* establecemos el paso de canal que tiene nuestro sintetizador. Para el OL1 es de 5MHz y para el OL2 es de 1MHz.

En *REF IN Frequency* establecemos nuestra señal de referencia mediante la cual se enganchará el bucle PLL. Para el sintetizador de 30MHz la referencia son los 10MHz del GPS y para los sintetizadores de los dos osciladores locales la referencia pasa a valer 30MHz.

El valor del *RF Prescaler* lo ponemos a partir del valor establecido durante la simulación de los respectivos sintetizadores. Lo mismo para el valor del *RF Charge Pump Current,* ponemos el valor que tengamos simulado.

En *MUXOUT* definimos que se notifique si el sintetizador esta enganchado seleccionando *DIGITAL LOCK DETECT*, de manera que se enciende un led en la nuestra placa indicándonos visualmente que el sintetizador esta correctamente funcionando.

El resto de parámetros de la aplicación son accesorios y no son necesarios para programar los sintetizadores.

Capítulo 4

4. RESULTADOS

4.1 PLACA DE CIRCUITO IMPRESO REALIZADA

En la siguiente figura se representa la placa de circuito impresa realizada con la ubicación de sus componentes. El conector de 8 vías se utiliza como puerto de comunicaciones entre los distintos sintetizadores de la placa y un ordenador local. El conector de 2 vías se utiliza para alimentar a +24V la placa de circuito impreso.

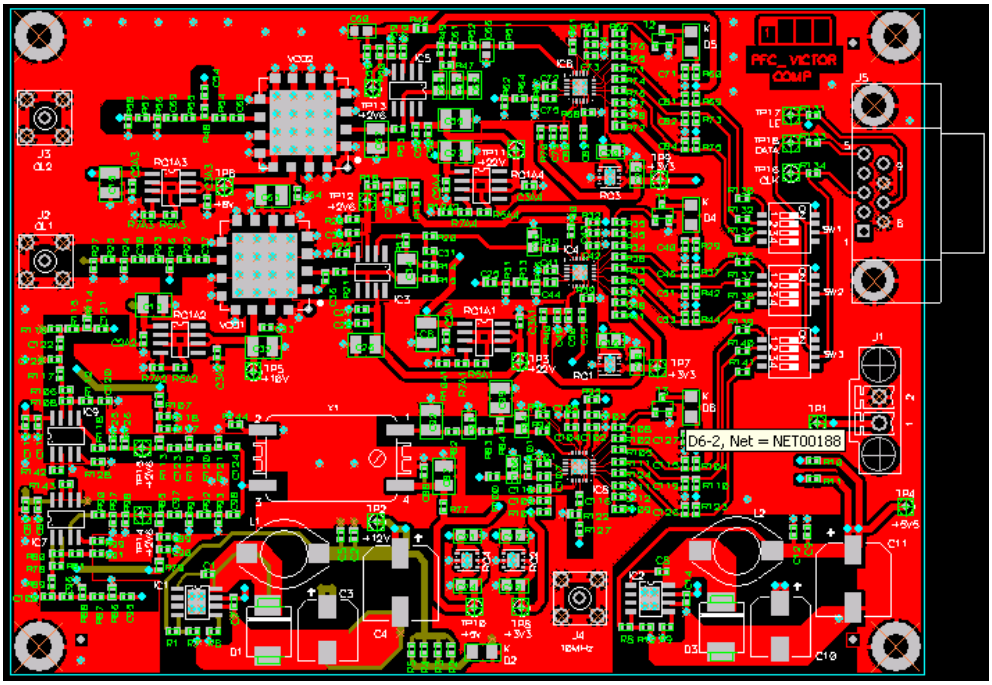


Figura 63. Placa de circuito impreso realizada

La disposición de componentes dentro la PCB no es aleatoria. Los convertidores DC/DC IC1 e IC2, de mayor capacidad de corriente, se distribuyen de manera que puedan disipar el máximo de calor en disipación. Los reguladores LDO se ponen cerca de cada integrado que alimentan para minimizar los efectos parásitos en las alimentaciones debido a pistas largas de alimentación. Los switch SW1, SW2, SW3 se colocan cerca del conector de comunicaciones para facilitar la conmutación de uno a otro dependiendo del sintetizador que se requiera programar. Los 3 sintetizadores se han colocado escalonados dentro la PCB para facilitar la ubicación de los conectores de RF y las pistas de impedancia controlada.

A continuación se detalla el conjunto de capas, un total de cuatro, que conforman la placa de circuito impreso.

En la siguiente figura se detalla la cara TOP de la PCB. En esta capa se distribuyen pistas de RF de impedancia controlada, pistas de alimentaciones y pistas de comunicaciones de datos. Observar como en esta cara se señalan todos los PADS de cada componente SMD y no SMD de la placa, donde a posteriori se soldarán los componentes.

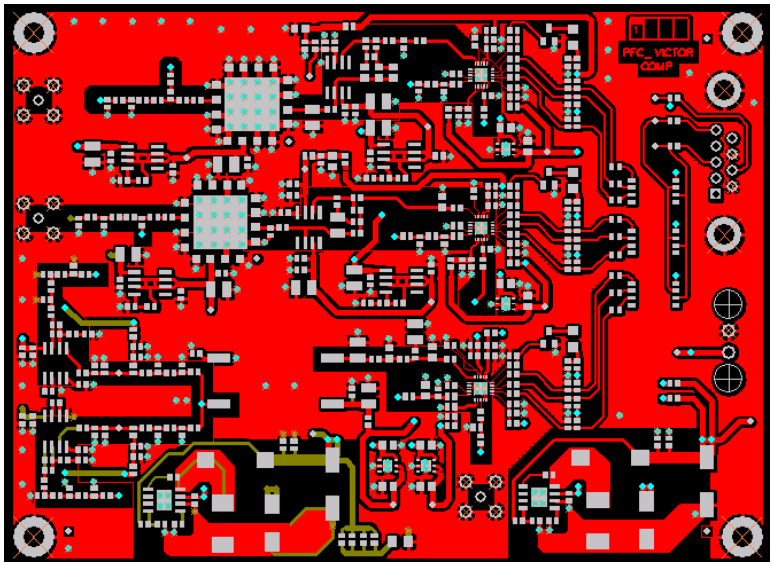


Figura 64. Cara TOP de la PCB

A continuación se detalla la SEGUNDA capa de la PCB. Esta capa constituye un gran plano de masa. De esta forma conseguimos aislar de posibles interferencias las pistas de RF de la cara TOP, así como diseñar las pistas como líneas MICROSTRIP de impedancia 50 Ohms controlada.

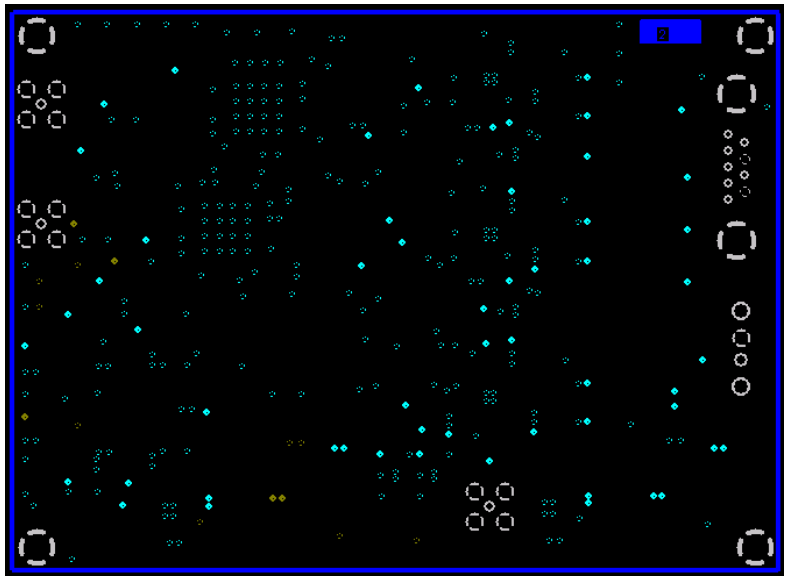


Figura 65. Capa 2 de la PCB

En la capa 3 se distribuyen pistas de alimentaciones y datos así como las pistas de RF con accesos a los conectores de RF. En este caso las pistas son del tipo STRIPLINE.

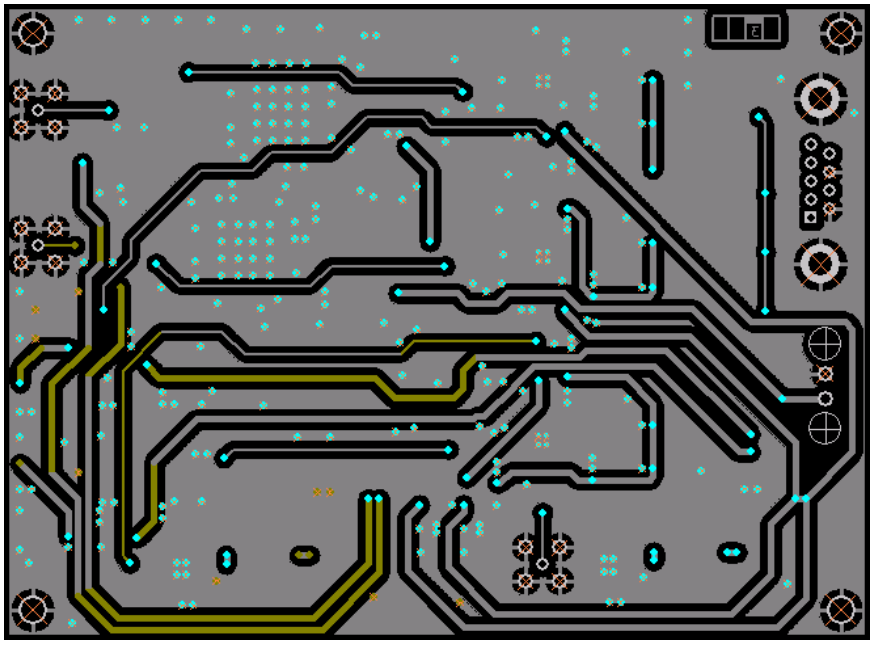


Figura 66. Capa 3 de la PCB

Finalmente la capa BOTTOM de la PCB esta formada por un gran plano de masa para apantallar correctamente las pistas de RF de la capa 3. También se puede observar como se ha aprovechado para pasar las pistas de alimentación de mayor consumo que demandan un mayor grosor de pista.

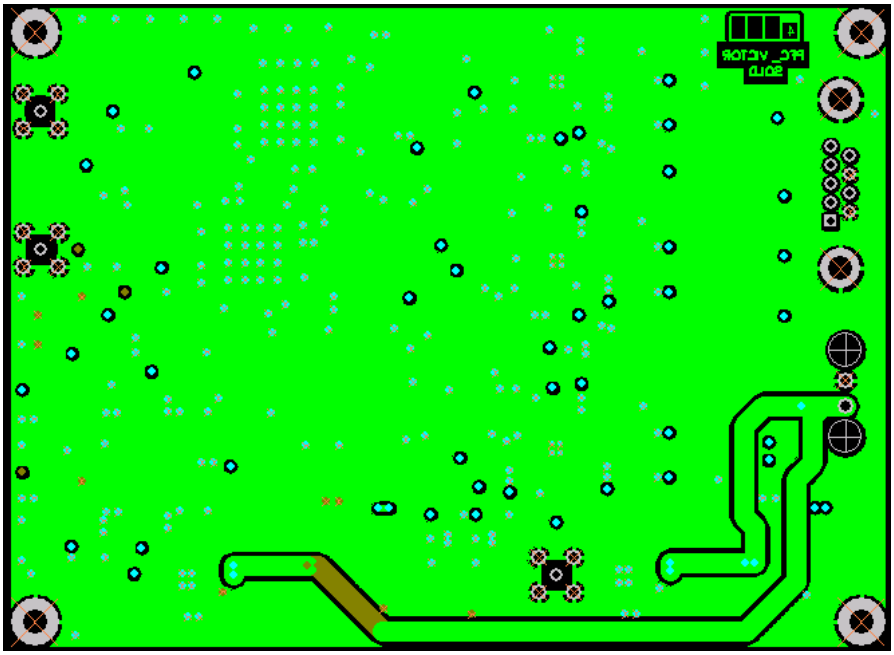


Figura 67. Capa BOTTOM de la PCB

A continuación se incluye un par de fotografías reales de la placa de circuito impreso realizada con todos los componentes soldados en la misma PCB.

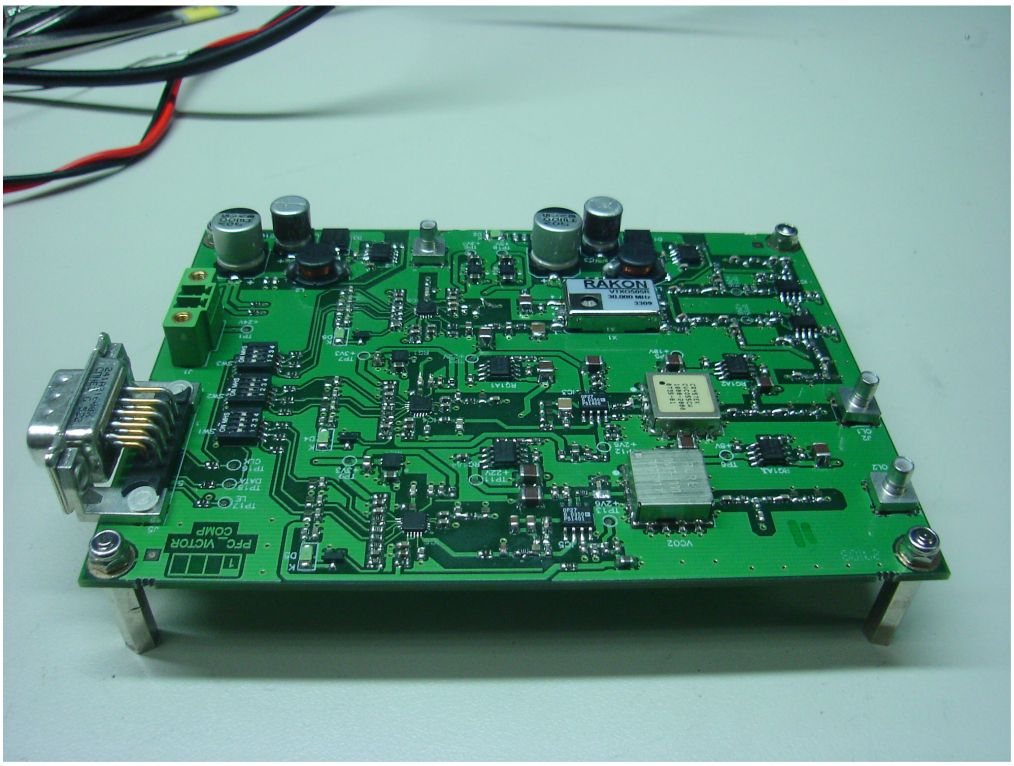


Figura 68. Fotografía en perspectiva de la PCB realizada

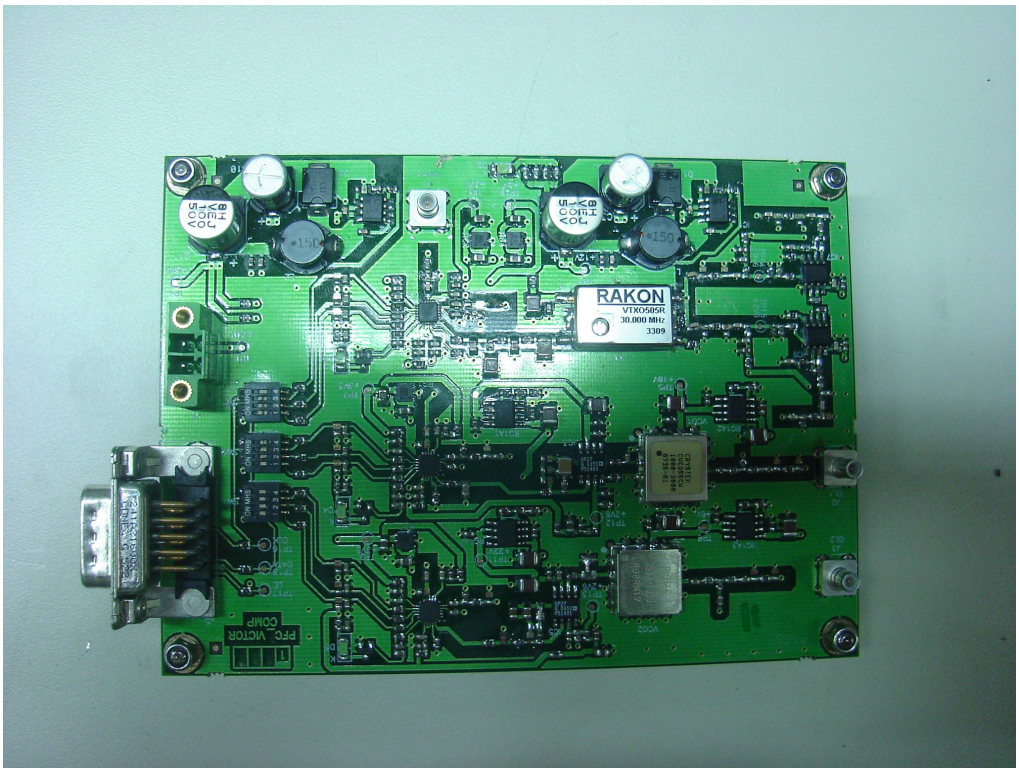


Figura 69. Fotografía frontal de la PCB realizada

A continuación realizamos un estudio térmico de la PCB en funcionamiento. Esto nos ayudará a determinar las zonas más calientes dentro la PCB y por tanto, aquellos componentes más sensibles a posibles fallos a largo plazo.

La temperatura media medida oscila entre los 35.7ºC hasta los 37,9ºC a temperatura ambiente de 25ºC. Los fabricantes de componentes electrónicos normalmente establecen los límites de funcionamiento de sus productos a un valor medio de 80ºC como máximo a nivel industrial, con lo que tenemos un margen aproximado de:

80ºC-38ºC = 42ºC
25ºC+42ºC = 67ºC

Podemos decir entonces que el circuito de la PCB podría funcionar aproximadamente hasta llegar a un valor de temperatura ambiente de 67ºC.

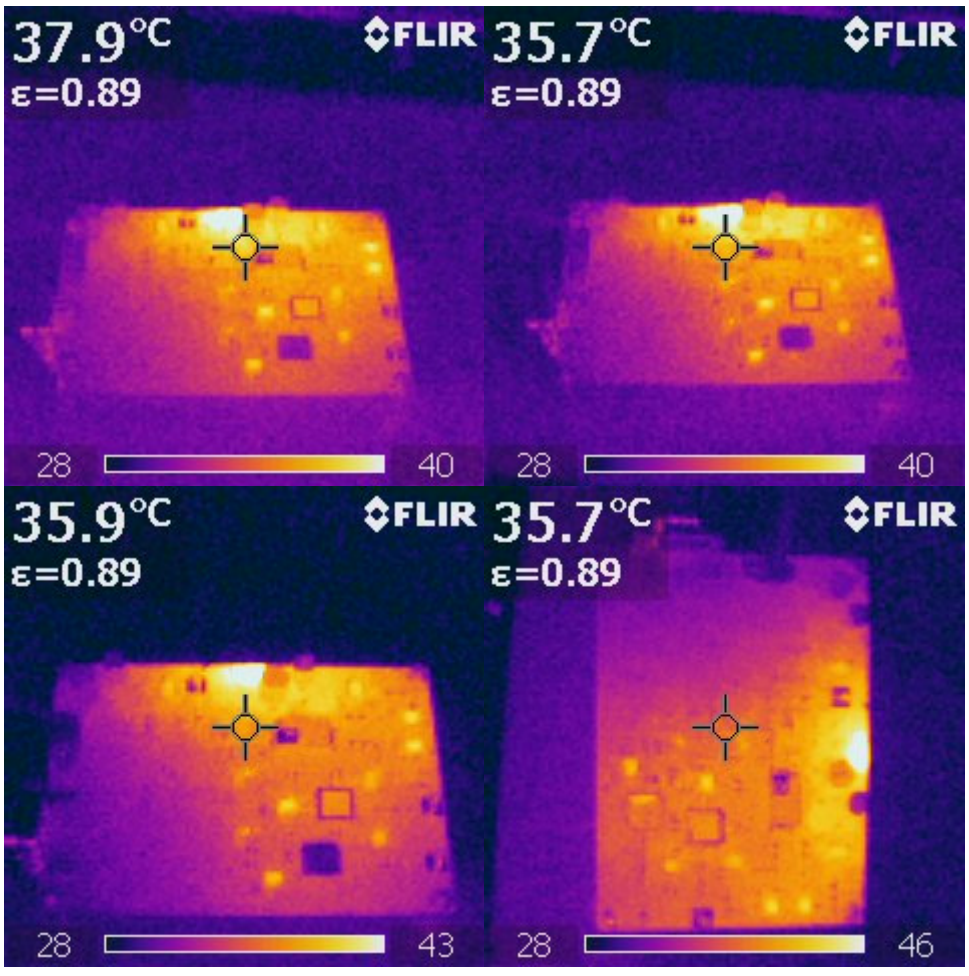


Figura 70. Fotografías térmicas de la PCB

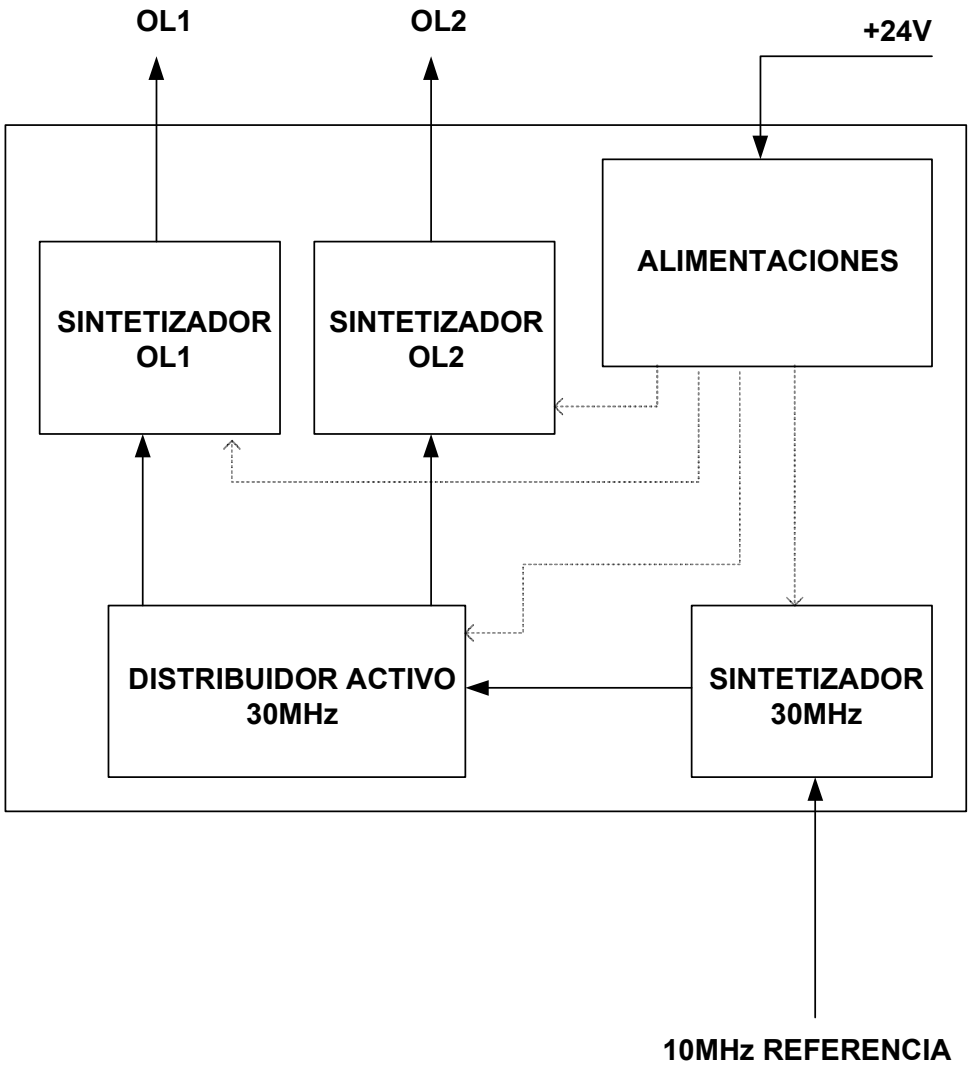
El punto más caliente de la PCB es precisamente el LED. Eso es lógico si pensamos que se ha utilizado un LED de alta eficiencia y se le hace consumir un valor nominal de corriente de 20mA. Se disminuiría el calor en esta parte del circuito disminuyendo el valor de la corriente de paso por el LED.

Otro punto caliente son los LDO's. Eso es comprensible pues son componentes extremadamente miniaturizados y su naturaleza les obliga a disipar el calor de forma permanente.

Finalmente como tercer punto caliente dentro la PCB tenemos los amplificadores operacionales que se calientan debido a su función de amplificación de la señal.

4.2 RESULTADOS PRÁCTICOS

La siguiente figura representa el diagrama funcional del circuito electrónico realizado. Se debe de realizar el test de todas las partes funcionales del mismo para validar el correcto funcionamiento del diseño.



Para ello es necesario montar un banco de test y medidas en el cual se han utilizado los siguientes instrumentos de medida:

Analizador de espectros FSP de ROHDE & SCHWARZ

Entre sus características técnicas destacar las que más nos afectan a nuestra medida:

Rango de Frecuencias de funcionamiento	9KHz a 40GHz
Resolución en frecuencia	0,01Hz
Frecuencia de referencia externa	10MHz
Pureza espectral (100Hz, 1KHz, 10KHz, 100KHz, 1MHz, 10MHz)	-90dBc/Hz, -108dBc/Hz, -113dBc/Hz, -113dBc/Hz, -125dBc/Hz, -145dBc/Hz
Resolución del ancho de banda	10Hz a 10MHz

Este instrumento es especialmente interesante para nuestro propósito pues posee una aplicación específica para la medida del ruido de fase de una señal. Observar que nuestras medidas obtenidas de los osciladores a testear, en cuestión de ruido de fase, vendrán limitadas por la pureza espectral del propio instrumento.

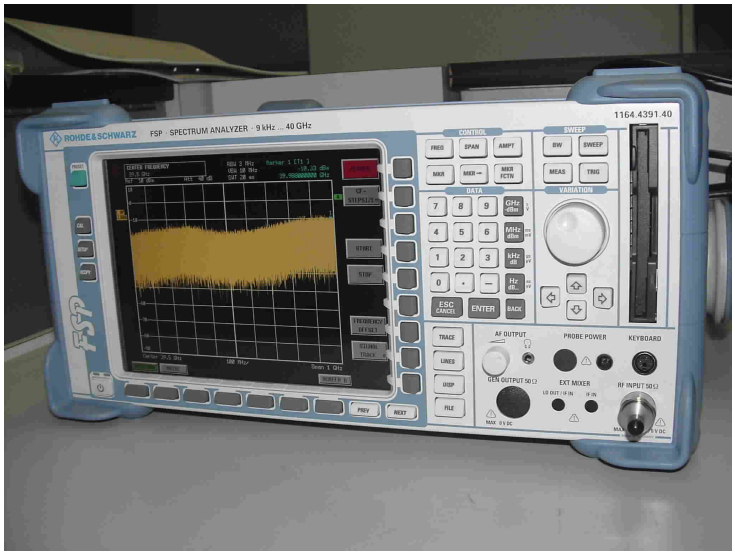


Figura 71. Analizador de espectros FSP

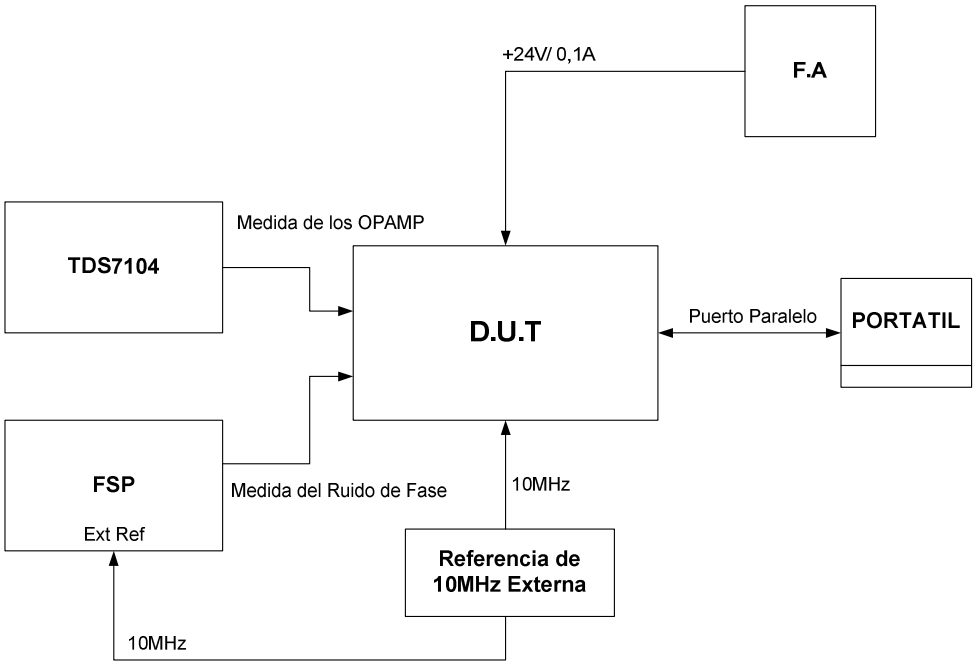
Osciloscopio digital TDS7104 de TEKTRONIX

Lo utilizaremos como instrumento de medida de las señales amplificadas por los operacionales así como ver los rizados en los convertidores DC/DC. Entre sus características técnicas destacar:

Canales de entrada	4
Ancho de banda	1GHz
Impedancia de entrada	1MOhm o 50Ohm
Rapidez en adquisición del señal	10GS/s

Figura 72. Osciloscopio TDS7104 de TEKTRONIX

La descripción del banco de trabajo es la siguiente:



La fuente de alimentación a +24V alimenta nuestra PCB. El consumo es de unos 100mA. El portátil lo utilizamos para programar los distintos sintetizadores mediante cable paralelo y el software que nos entrega el fabricante de los integrados. Es importante que la referencia de 10MHz alimente nuestro circuito, pero también el analizador de espectros del cual sacaremos la medida del ruido de fase de nuestros osciladores. Finalmente con el osciloscopio con una sonda de 1MegaOhm realizaremos las medidas del rizado en las tensiones y las medidas en los operacionales.

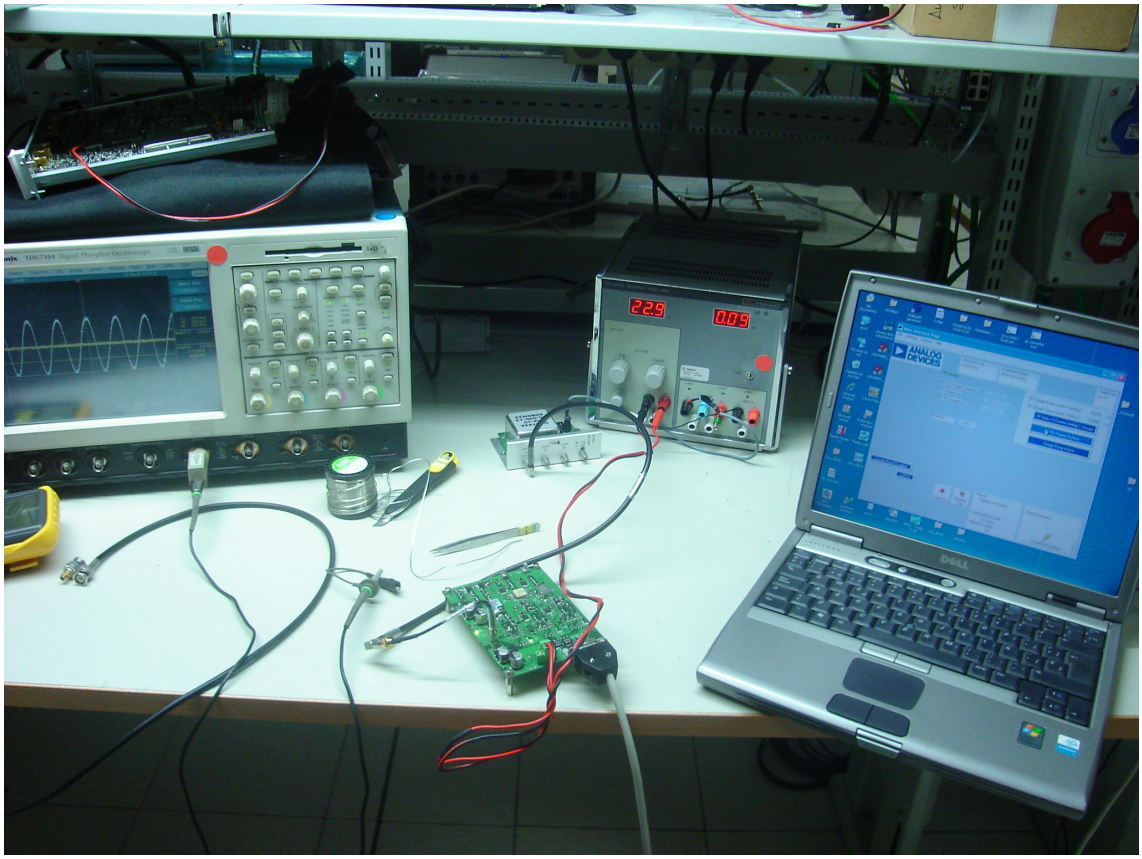


Figura 73. Fotografía del banco de trabajo utilizado.

4.2.1 SÍNTESIS DE LA REFERENCIA DE 30MHZ

Los valores de Ruido de Fase obtenidos mediante la medida con el analizador de espectros FSP son los siguientes:

Frecuencia	Ruido de Fase
100Hz	-100dBc/Hz
1KHz	-112dBc/Hz
10KHz	-110dBc/Hz
100KHz	-120dBc/Hz
1MHz	-125dBc/Hz
10MHz	-140dBc/Hz

Gráficamente el ruido de fase queda de la siguiente manera:

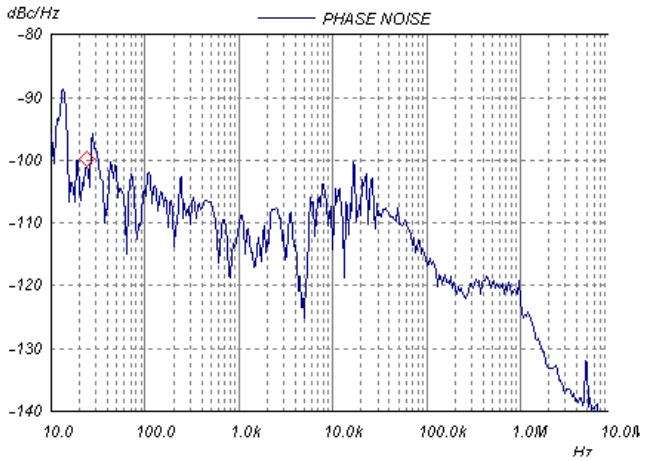


Figura 74. Ruido de fase referencia a 30MHz obtenido

Si comparamos los resultados obtenidos con el simulado de la siguiente figura, observamos que hay bastante divergencia.

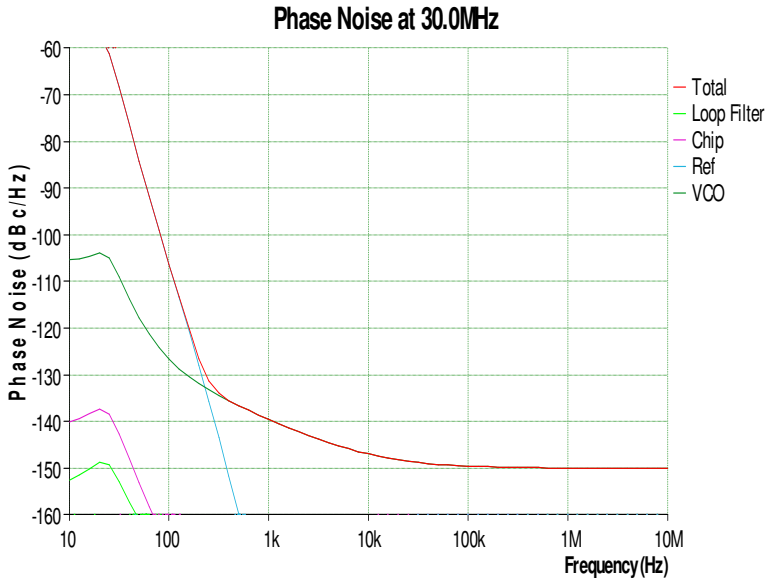


Figura 75. Ruido de fase referencia a 30MHz simulado

Frecuencia	Ruido de Fase Simulado	Ruido de Fase Obtenido
100Hz	-106dBc/Hz	-100dBc/Hz
1KHz	-139dBc/Hz	-112dBc/Hz
10KHz	-147dBc/Hz	-110dBc/Hz
100KHz	-149dBc/Hz	-120dBc/Hz
1MHz	-150dBc/Hz	-125dBc/Hz

Observamos que el ruido de fase sólo se asemeja en los dos primeros valores de la tabla. Esto es debido a las propias limitaciones del analizador de espectros para medir el ruido de fase, referirse a los límites del mismo. Por lo tanto, la lectura obtenida no es la real pues esta enmascarada por el propio ruido de fase del instrumento utilizado para la medida.

4.2.2 FUNCIONAMIENTO DEL DIVISOR ACTIVO DE DOBLE RAMAL

Primeramente medimos el nivel de la señal de referencia de 10MHz del circuito. La amplitud pico a pico de la señal es de 3,5V aproximadamente, eso significa que tenemos un nivel de:

Vdbm=20 x log10(Vpp/ sqrt (0,008x50)) = +14dBm

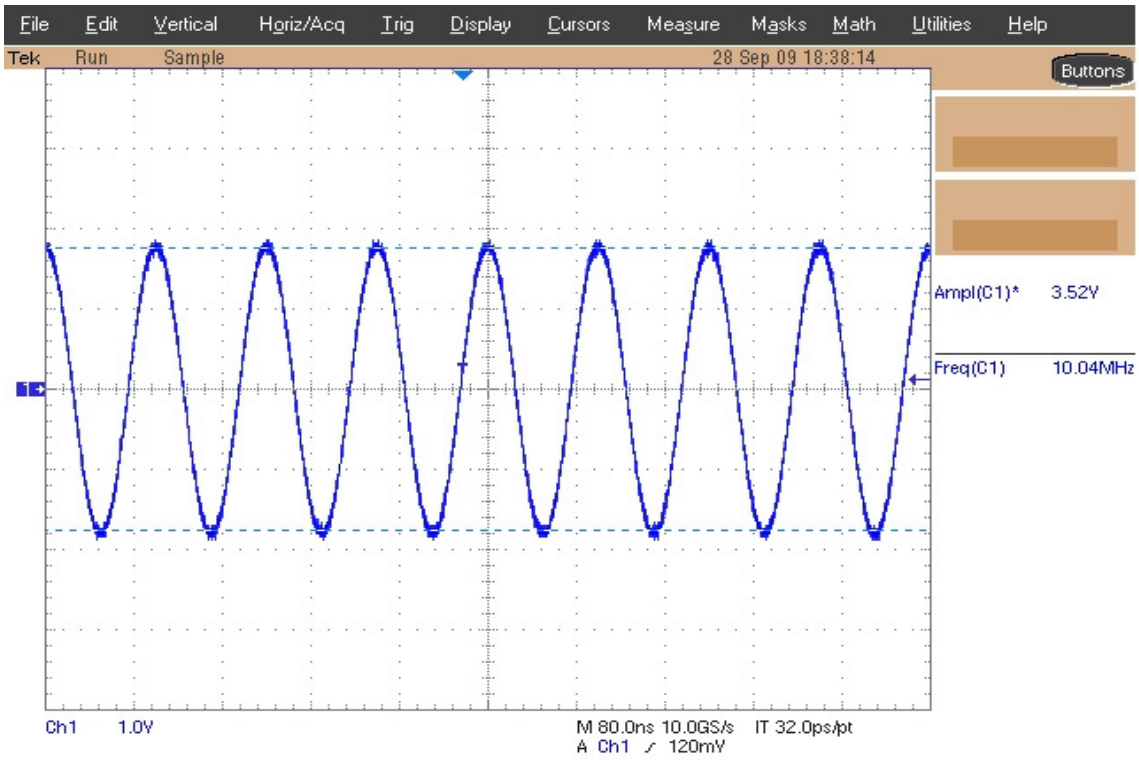


Figura 76. Nivel de entrada de la referencia de 10MHz

La hoja de especificaciones del sintetizador ADF4002 especifica un rango de nivel de entrada pico a pico de 0,8V hasta Vdd+0,3, en consecuencia, estamos dentro del límite de especificaciones.

Medimos la señal a la salida del VCO de 30MHz obteniendo el siguiente gráfico con el osciloscopio digital:

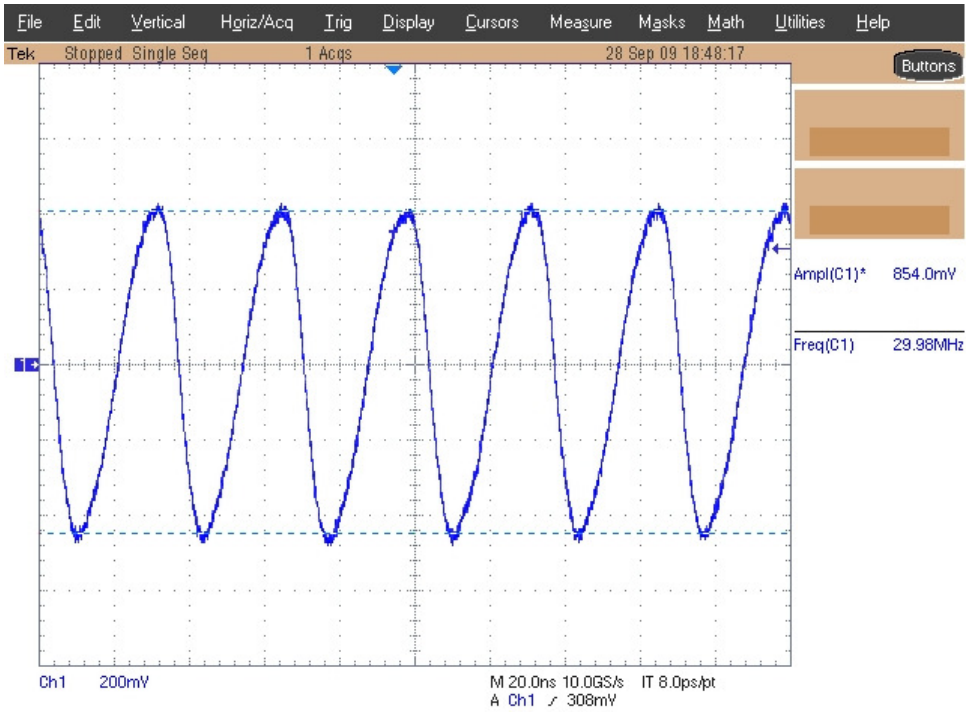


Figura 77. Nivel de salida de la referencia de 30MHz

En este caso el nivel de la señal a la frecuencia de 30MHz es de 850mV pico a pico aproximadamente. Esto equivale a un nivel de señal de:

Vdbm=20 x log10(Vpp/ sqrt (0,008x50)) = +2dBm

Exactamente el valor que nos dice el fabricante del VCO que tendríamos a la salida del integrado. A continuación miramos el nivel de señal a la salida de cada uno de los dos operacionales que actúan como divisores activos de señal, obteniendo la siguiente respuesta:

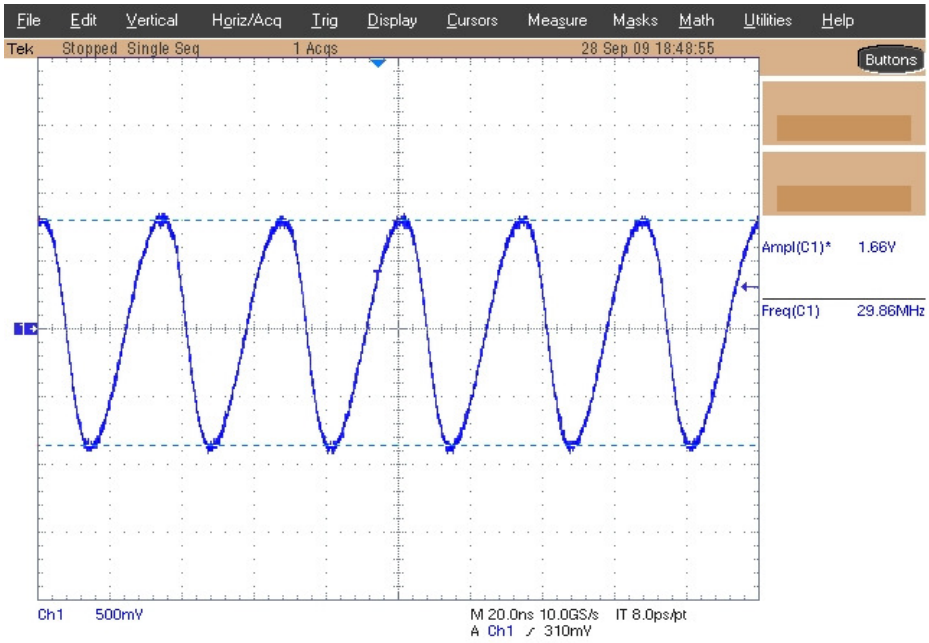


Figura 78. Nivel de salida a 30MHz después de los amplificadores operacionales

Observar como ahora el nivel de señal ha aumentado siendo el valor de 1,6Vpp. Por lo tanto, tenemos un nivel a la salida de los operacionales de:

Vdbm=20 x log10(Vpp/ sqrt (0,008x50)) = +8dBm

Siendo exactamente el nivel medio de señal de entrada de referencia necesario para el correcto funcionamiento de los dos sintetizadores de señal posteriores.
Finalmente adjuntamos gráfica comparativa entre el nivel de señal a la entrada del operacional y a la salida del mismo.

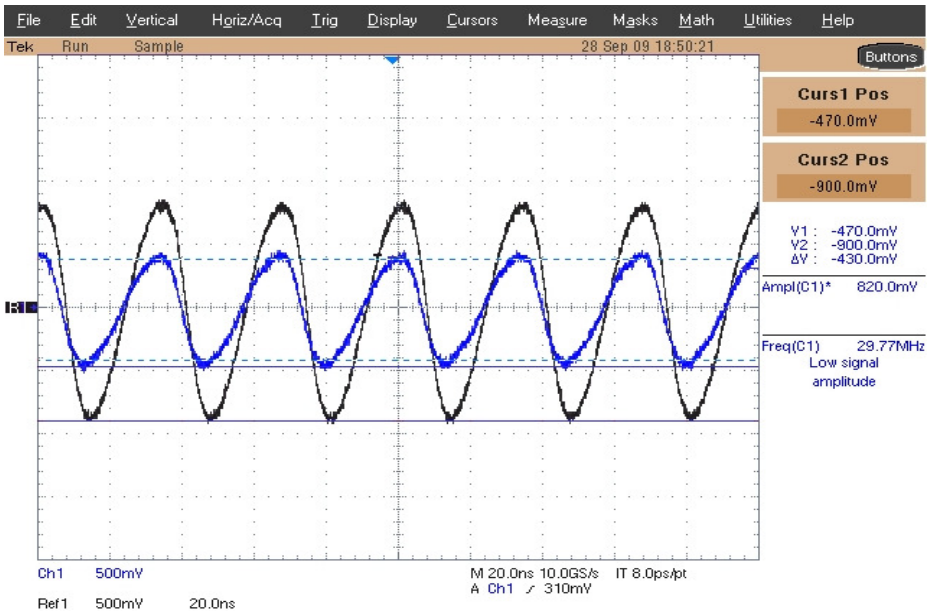


Figura 79. Nivel comparativo entrada/salida

4.2.3 SÍNTESIS DEL PRIMER OSCILADOR LOCAL

El primer oscilador debe poder sintetizar frecuencias de 1505MHz hasta 1890MHz en pasos de 5MHz. La frecuencia mas alta debería de tener peor ruido de fase, aún así medimos el ruido de fase del sintetizador para las dos frecuencias extremas.

En el caso de la síntesis de la frecuencia de 1505MHz obtenemos el siguiente resultado:

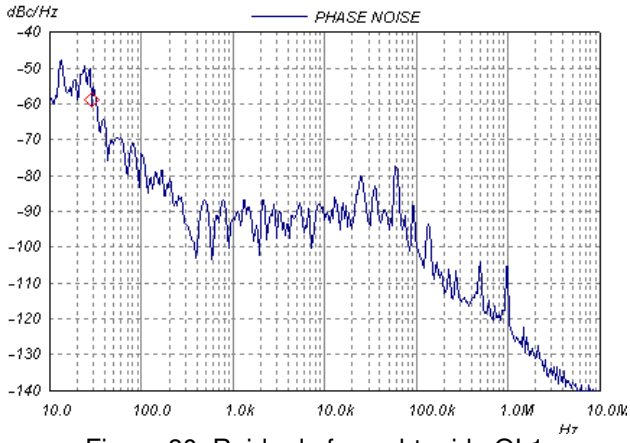


Figura 80. Ruido de fase obtenido OL1

Frecuencia	**Ruido de Fase**
100Hz	-80dBc/Hz
1KHz	-92dBc/Hz
10KHz	-92dBc/Hz
100KHz	-100dBc/Hz
1MHz	-120dBc/Hz
10MHz	-140dBc/Hz

Si comparamos los resultados obtenidos con los simulados, vemos que son muy parecidos.

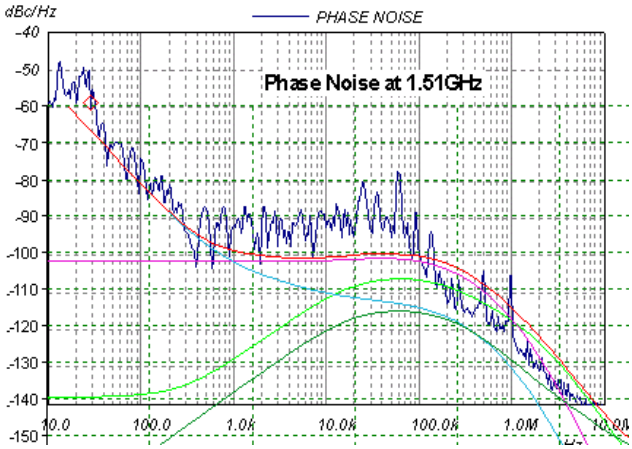


Figura 81. Ruido de fase obtenido vs simulado de OL1

Si hacemos lo mismo para la frecuencia superior a sintetizar:

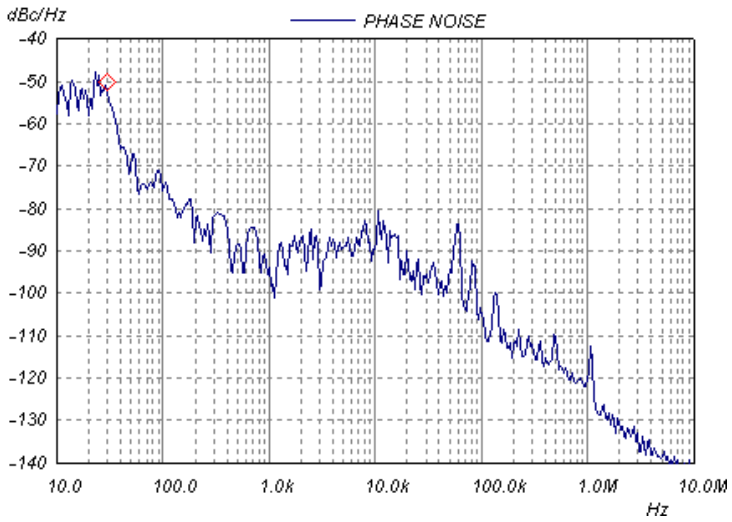


Figura 82. Ruido de fase obtenido de OL1

Frecuencia	Ruido de Fase
100Hz	-75dBc/Hz
1KHz	-92dBc/Hz
10KHz	-90dBc/Hz
100KHz	-105dBc/Hz
1MHz	-120dBc/Hz
10MHz	-140dBc/Hz

Igualmente si comparamos los resultados obtenidos con los de simulación podemos comprobar que efectivamente se obtienen en los dos casos respuestas muy parecidas.

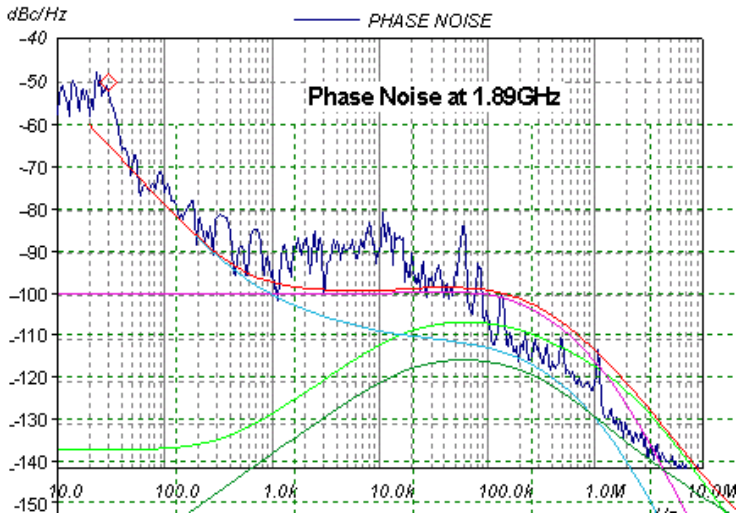


Figura 83. Ruido de fase obtenido vs simulado de OL1

4.2.4 SÍNTESIS DEL SEGUNDO OSCILADOR LOCAL

En este segundo caso, el oscilador local debe sintetizar frecuencias que van de los 992MHz hasta los 996MHz. Si estudiamos los resultados obtenidos para ambos casos, los resultantes para la síntesis de frecuencia a 992MHZ son los siguientes:

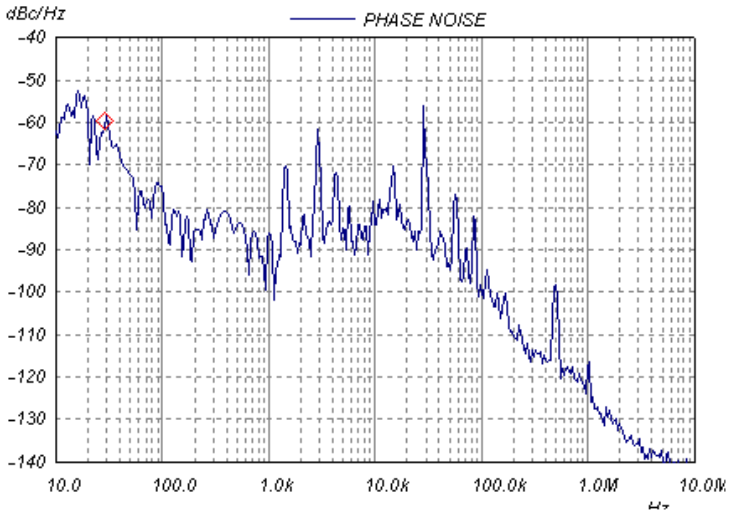


Figura 84. Ruido de fase obtenido de OL2

Frecuencia	Ruido de Fase
100Hz	-80dBc/Hz
1KHz	-92dBc/Hz
10KHz	-85dBc/Hz
100KHz	-100dBc/Hz
1MHz	-125dBc/Hz
10MHz	-140dBc/Hz

Comparando gráficamente los resultados obtenidos con los simulados, vemos que la respuesta es muy parecida.

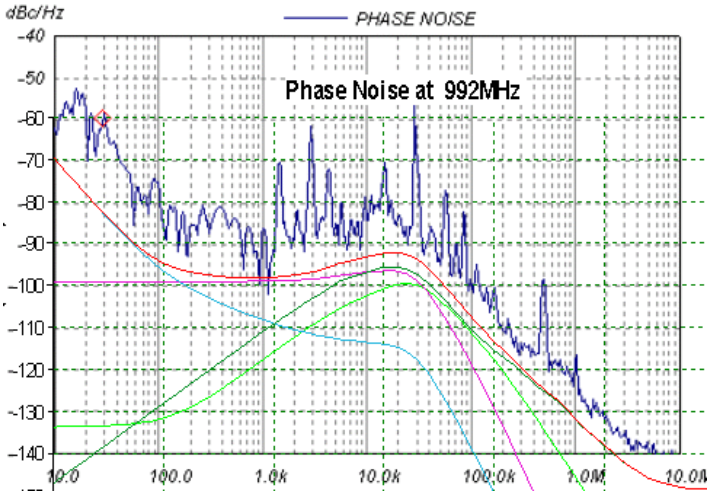


Figura 85. Ruido de fase obtenido vs simulado de OL2

Finalmente los resultados obtenidos de la síntesis de la frecuencia superior a 996MHz son los siguientes:

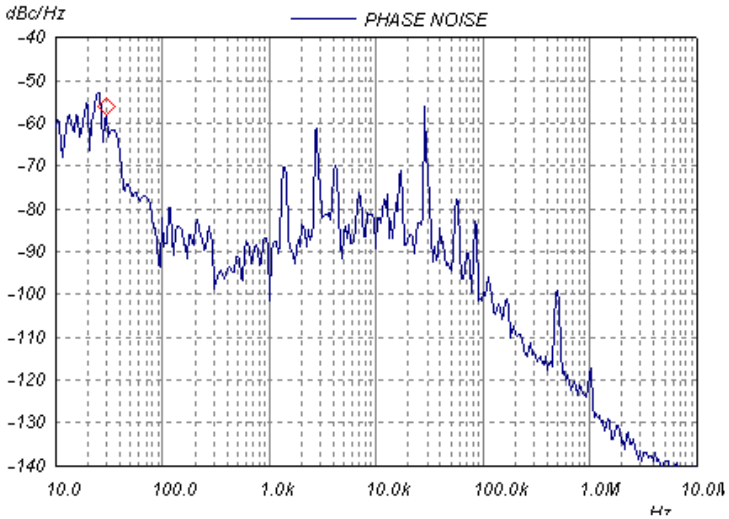


Figura 86. Ruido de fase obtenido de OL2

Frecuencia	Ruido de Fase
100Hz	-90dBc/Hz
1KHz	-90dBc/Hz
10KHz	-85dBc/Hz
100KHz	-100dBc/Hz
1MHz	-123dBc/Hz
10MHz	-140dBc/Hz

Comparando gráficamente los resultados obtenidos con los simulados, vemos que la respuesta es igualmente muy parecida.

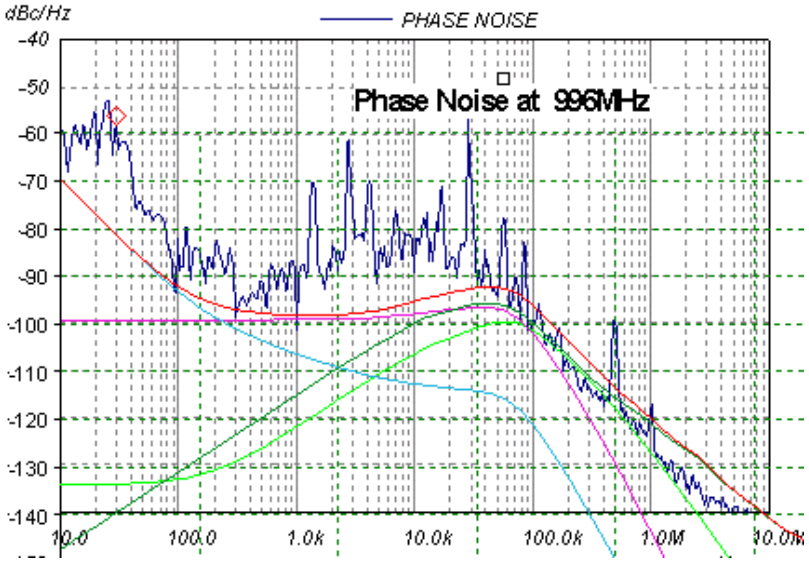


Figura 87. Ruido de fase obtenido vs simulado de OL2

Capítulo 5

5. VIABILIDAD

5.1 ESTUDIO ECONÓMICO

En el esquema siguiente se detalla el coste económico del proyecto en función de los distintos conceptos que han cargado sobre éste: costes de diseño, costes de material y los costes de fabricación.

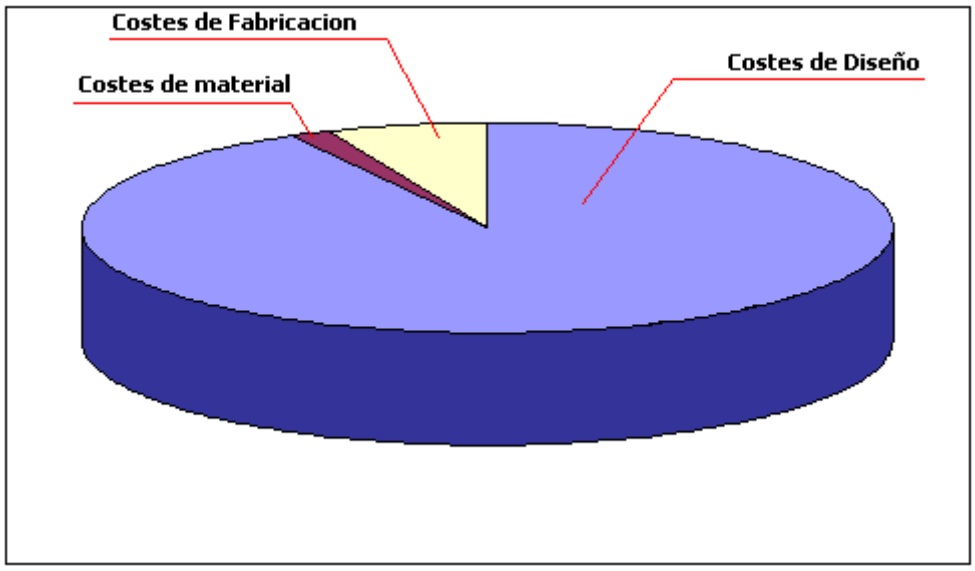


Figura 88. Resumen comparativo de costes del proyecto

Lo que más llama la atención es que los costes de fabricación y material son los menos significativos. Entonces, en cierto modo, lo que añade realmente valor al circuito realizado son los conocimientos tecnológicos para la implementación del producto final, más que el coste de material para la realización del mismo.

Es importante notar que tanto los costes de fabricación como los costes de material van en decrecimiento según las cantidades fabricadas de producto, por tanto, son costes que tienden siempre a reducirse, y más para series grandes. Por otra parte, los costes de diseño son siempre mayores al principio pero sólo deben de realizarse una vez, y se amortizan durante la vida del producto.

5.1.1 COSTES DE DISEÑO

En primer lugar consideramos los costes generados por el ejercicio de diseño del ingeniero de proyecto. Éstos constan en primer lugar de un estudio preliminar en el cual se profundiza en el estudio del ámbito de aplicación del diseño a realizar, así como en el estado del arte del producto a diseñar. A posteriori se procede a simular las diferentes partes del circuito electrónico. Una vez las simulaciones son satisfactorias, se dibuja el esquema eléctrico al completo.

En segundo lugar se añade el coste de realización del diseño de la placa de circuito impreso o PCB por parte del técnico de Layout. Este trabajo consiste en traducir toda la información de alto nivel del diseño eléctrico a una realización física del circuito.

Finalmente se finaliza la etapa de diseño con la creación de la documentación para la creación y fabricación real de la placa de circuito impreso del circuito.

Concepto	**Recurso**	**Coste unitario**	**Tiempo**	**Coste total**
Estudio Preliminar	Ingeniero	40€/h	24h	960€
Concepción, diseño y test de validación	Ingeniero	40€/h	80h	3200€
Delineación PCB	Técnico	33€/h	12h	396€
Creación documentación para fabricación	Técnico	33€/h	2h	66€

El coste total del diseño es de 4.622 euros.

5.1.2 COSTES DE MATERIAL

En la tabla que se describe a continuación se detalla el coste de cada uno de los componentes que conforman el circuito realizado con su coste particular asociado y referencia de fabricante.

	Descripcion	Referencia	Precio
L1	CHOQUE SMD 15uH 2,5A WE-PD4 TYPEL 10%	WÜRTH ELEKTRONIK / REF.: 744 561 15	0,30
L2	CHOQUE SMD 15uH 2,5A WE-PD4 TYPEL 10%	WÜRTH ELEKTRONIK / REF.: 744 561 15	0,30
VCO1	VCO 500-1000MHZ SMD	RALTRON Ref.: RQRE-500-1000	9,10
VCO2	VCO 1000-2000MHZ SMD	RALTRON Ref.: RQRE-1000-2000	10,50
X1	VCTCXO CRYSTAL OSCILLATOR 8-30MHz	RAKON	15,13
IC1	BUCK DC/DC CONVERTER Vin 5.5V to 36V 5A	TEXAS INST. Ref.: TPS5450DDA	2,50
IC2	BUCK DC/DC CONVERTER Vin 5.5V to 36V 5A	TEXAS INST. Ref.: TPS5450DDA	2,50
IC3	CIRCUITO INTEGRADO SMD OP27GS	PMI	1,23
IC4	PLL FREQUENCY SINTHESIZER UP TO 6GHZ	ANALOG DEVICES Ref.: ADF4106BCPZ	1,85
IC5	CIRCUITO INTEGRADO SMD OP27GS	PMI	1,23
IC6	PLL FREQUENCY SINTHESIZER UP TO 6GHZ	ANALOG DEVICES Ref.: ADF4106BCPZ	1,85
IC7	CI 2GHz AMPLIFICADOR OPERA. SMDSOIC8 THS3202D	TEXAS INSTRUMENTS Ref.: THS3202D	3,58
IC8	400MHz INTEGER FREQUENCY SINTHESIZER	ANALOG DEVICES Ref.:ADF4002BCPZ	1,52
IC9	CI 2GHz AMPLIFICADOR OPERA. SMDSOIC8 THS3202D	TEXAS INSTRUMENTS Ref.: THS3202D	3,58
RG1	CMOS LINEAR REGULATOR Vout 3V3 500mA	NATIONAL Ref.: LP38693SD-3,3	0,88
RG2	CMOS LINEAR REGULATOR Vout 3V3 500mA	NATIONAL Ref.: LP38693SD-3,3	0,88
RG3	CMOS LINEAR REGULATOR Vout 3V3 500mA	NATIONAL Ref.: LP38693SD-3,3	0,88
RG4	CMOS LINEAR REGULATOR Vout 5V 500mA	NATIONAL Ref.: LP38693SD-5.0	0,88
RGA11	CIRCUITO INTEGRADO SMD TL317CD	TEXAS INSTRUMENT Ref.: TL317CD	0,06
RGA12	CIRCUITO INTEGRADO SMD TL317CD	TEXAS INSTRUMENT Ref.: TL317CD	0,06
RGA13	CIRCUITO INTEGRADO SMD TL317CD	TEXAS INSTRUMENT Ref.: TL317CD	0,06

RGA14	CIRCUITO INTEGRADO SMD TL317CD	TEXAS INSTRUMENT Ref.: TL317CD	0,06
C1	COND. SMD X7R 10nF 50V 0603 10%	YAGEO Ref.: 2222 586 156 36	0,15
C2	COND. SMD Y5V 100nF 50V 0603 +80-20%	YAGEO Ref.: 2222 586 19812	0,17
C3	COND. SMD ELECTROLITICO 47uF 50V 0810	VISHAY Ref.: 2222 153 71479	0,12
C4	COND. SMD ELECTROLITICO 100uF 50V 1012	VISHAY Ref.: 2222 153 71101	0,14
C5	COND. SMD X7R 10nF 50V 0603 10%	YAGEO Ref.: 2222 586 156 36	0,12
C6	COND. SMD X5R 10uF 35V 1210 20%	TAIYO YUDEN Ref.: GMK325BJ106MH-T	0,17
C7	COND. SMD X7R 10nF 50V 0603 10%	YAGEO Ref.: 2222 586 156 36	0,12
C8	COND. SMD X7R 10nF 50V 0603 10%	YAGEO Ref.: 2222 586 156 36	0,12
C9	COND. SMD Y5V 100nF 50V 0603 +80-20%	YAGEO Ref.: 2222 586 19812	0,17
C10	COND. SMD ELECTROLITICO 47uF 50V 0810	VISHAY Ref.: 2222 153 71479	0,12
C11	COND. SMD ELECTROLITICO 100uF 50V 1012	VISHAY Ref.: 2222 153 71101	0,14
C12	COND. SMD X7R 10nF 50V 0603 10%	YAGEO Ref.: 2222 586 156 36	0,12
C13	COND. SMD X5R 10uF 35V 1210 20%	TAIYO YUDEN Ref.: GMK325BJ106MH-T	0,17
C14	COND. SMD X7R 10nF 50V 0603 10%	YAGEO Ref.: 2222 586 156 36	0,12
C15	COND. SMD X5R 10uF 35V 1210 20%	TAIYO YUDEN Ref.: GMK325BJ106MH-T	0,17
C16	COND. SMD X5R 10uF 16V 0805 10%	TAIYO YUDEN Ref.: EMK212BJ106KG-T	0,04
C17	COND. SMD X5R 10uF 16V 0805 10%	TAIYO YUDEN Ref.: EMK212BJ106KG-T	0,04
C18	COND. SMD X5R 10uF 16V 0805 10%	TAIYO YUDEN Ref.: EMK212BJ106KG-T	0,04
C19	COND. SMD X5R 10uF 16V 0805 10%	TAIYO YUDEN Ref.: EMK212BJ106KG-T	0,04
C20	COND. SMD X5R 10uF 16V 0805 10%	TAIYO YUDEN Ref.: EMK212BJ106KG-T	0,04
C21	COND. SMD X5R 10uF 16V 0805 10%	TAIYO YUDEN Ref.: EMK212BJ106KG-T	0,04
C22	COND. SMD X5R 10uF 16V 0805 10%	TAIYO YUDEN Ref.: EMK212BJ106KG-T	0,04
C23	COND. SMD X5R 10uF 35V 1210 20%	TAIYO YUDEN Ref.: GMK325BJ106MH-T	0,17
C24	COND. SMD X5R 10uF 16V 0805 10%	TAIYO YUDEN Ref.: EMK212BJ106KG-T	0,04
C25	COND. SMD NPO 100pF 50V 0603 5%	YAGEO Ref.: 2222 867 15101	0,10

C26	COND. SMD X5R 10uF 35V 1210 20%	TAIYO YUDEN Ref.: GMK325BJ106MH-T	0,17
C27	COND. SMD NPO 100pF 50V 0603 5%	YAGEO Ref.: 2222 867 15101	0,10
C28	COND. SMD Y5V 100nF 50V 0603 +80-20%	YAGEO Ref.: 2222 586 19812	0,12
C29	COND. SMD Y5V 100nF 50V 0603 +80-20%	YAGEO Ref.: 2222 586 19812	0,12
C30	COND. SMD X5R 10uF 16V 0805 10%	TAIYO YUDEN Ref.: EMK212BJ106KG-T	0,04
C32	COND. SMD X5R 10uF 35V 1210 20%	TAIYO YUDEN Ref.: GMK325BJ106MH-T	0,17
C33	COND. SMD Y5V 100nF 50V 0603 +80-20%	YAGEO Ref.: 2222 586 19812	0,12
C34	COND. SMD X7R 220nF 63V 1210 10%	TEKELEC Ref.: 630S41X224KP	0,07
C35	COND. SMD NP0 N 1nF 63V 0805 5%	TEKELEC Ref.: 630R15N102JP	0,01
C36	COND. SMD X7R 100nF 16V 0603 20%		0,10
C37	COND. SMD NPO 100pF 50V 0603 5%	YAGEO Ref.: 2222 867 15101	0,10
C38	COND. SMD NPO 100pF 50V 0603 5%	YAGEO Ref.: 2222 867 15101	0,10
C39	COND. SMD Y5V 100nF 50V 0603 +80-20%	YAGEO Ref.: 2222 586 19812	0,10
C40	COND. SMD NPO 100pF 50V 0603 5%	YAGEO Ref.: 2222 867 15101	0,10
C41	COND. SMD NPO 100pF 50V 0603 5%	YAGEO Ref.: 2222 867 15101	0,10
C42	COND. SMD NP0 10pF 50V 0603 5%	YAGEO Ref.: 2222 867 15109	0,10
C43	COND. SMD Y5V 100nF 50V 0603 +80-20%	YAGEO Ref.: 2222 586 19812	0,10
C44	COND. SMD NPO 100pF 50V 0603 5%	YAGEO Ref.: 2222 867 15101	0,10
C45	COND. SMD NPO 100pF 50V 0603 5%	YAGEO Ref.: 2222 867 15101	0,10
C46	COND. SMD NPO 100pF 50V 0603 5%	YAGEO Ref.: 2222 867 15101	0,10
C47	COND. SMD NP0 10pF 50V 0603 5%	YAGEO Ref.: 2222 867 15109	0,10
C48	COND. SMD Y5V 100nF 50V 0603 +80-20%	YAGEO Ref.: 2222 586 19812	0,10
C49	COND. SMD Y5V 100nF 50V 0603 +80-20%	YAGEO Ref.: 2222 586 19812	0,10
C50	COND. SMD NP0 10pF 50V 0603 5%	YAGEO Ref.: 2222 867 15109	0,10
C51	COND. SMD NPO 100pF 50V 0603 5%	YAGEO Ref.: 2222 867 15101	0,10

C52	COND. SMD X7R 1nF 50V 0603 10%	YAGEO Ref.: 2222 586 156 23	0,10
C53	COND. SMD NPO 100pF 50V 0603 5%	YAGEO Ref.: 2222 867 15101	0,10
C54	COND. SMD NPO 100pF 50V 0603 5%	YAGEO Ref.: 2222 867 15101	0,10
C55	COND. SMD X5R 10uF 35V 1210 20%	TAIYO YUDEN Ref.: GMK325BJ106MH-T	0,17
C56	COND. SMD NPO 100pF 50V 0603 5%	YAGEO Ref.: 2222 867 15101	0,00
C57	COND. SMD X5R 1uF 16V 0805 10%	TAIYO YUDEN Ref.:EMK212BJ105KG-T	0,12
C58	COND. SMD Y5V 100nF 50V 0603 +80-20%	YAGEO Ref.: 2222 586 19812	0,12
C59	COND. SMD Y5V 100nF 50V 0603 +80-20%	YAGEO Ref.: 2222 586 19812	0,12
C60	COND. SMD X5R 10uF 16V 0805 10%	TAIYO YUDEN Ref.: EMK212BJ106KG-T	0,04
C62	COND. SMD X5R 1uF 16V 0805 10%	TAIYO YUDEN Ref.:EMK212BJ105KG-T	0,12
C63	COND. SMD X5R 10uF 35V 1210 20%	TAIYO YUDEN Ref.: GMK325BJ106MH-T	0,17
C64	COND. SMD Y5V 100nF 50V 0603 +80-20%	YAGEO Ref.: 2222 586 19812	0,12
C65	COND. SMD X5R 1uF 16V 0805 10%	TAIYO YUDEN Ref.:EMK212BJ105KG-T	0,12
C66	COND. SMD X7R 15nF 63V 0504 10%	TEKELEC Ref.: 630R11X153KP	0,07
C67	COND. SMD X7R 330nF 63V 1210 10%	TEKELEC Ref.: 630S41X334KP	0,07
C68	COND. SMD NPO 100pF 50V 0603 5%	YAGEO Ref.: 2222 867 15101	0,10
C69	COND. SMD NPO 100pF 50V 0603 5%	YAGEO Ref.: 2222 867 15101	0,10
C70	COND. SMD Y5V 100nF 50V 0603 +80-20%	YAGEO Ref.: 2222 586 19812	0,10
C71	COND. SMD NPO 100pF 50V 0603 5%	YAGEO Ref.: 2222 867 15101	0,10
C72	COND. SMD NPO 100pF 50V 0603 5%	YAGEO Ref.: 2222 867 15101	0,10
C73	COND. SMD NP0 10pF 50V 0603 5%	YAGEO Ref.: 2222 867 15109	0,10
C74	COND. SMD Y5V 100nF 50V 0603 +80-20%	YAGEO Ref.: 2222 586 19812	0,10
C75	COND. SMD NPO 100pF 50V 0603 5%	YAGEO Ref.: 2222 867 15101	0,10
C76	COND. SMD NPO 100pF 50V 0603 5%	YAGEO Ref.: 2222 867 15101	0,10
C77	COND. SMD NP0 10pF 50V 0603 5%	YAGEO Ref.: 2222 867 15109	0,10
C78	COND. SMD Y5V 100nF 50V 0603 +80-20%	YAGEO Ref.: 2222 586 19812	0,10

C79	COND. SMD Y5V 100nF 50V 0603 +80-20%	YAGEO Ref.: 2222 586 19812	0,10
C80	COND. SMD NP0 10pF 50V 0603 5%	YAGEO Ref.: 2222 867 15109	0,10
C81	COND. SMD NPO 100pF 50V 0603 5%	YAGEO Ref.: 2222 867 15101	0,10
C82	COND. SMD NPO 100pF 50V 0603 5%	YAGEO Ref.: 2222 867 15101	0,10
C83	COND. SMD X7R 1nF 50V 0603 10%	YAGEO Ref.: 2222 586 156 23	0,10
C84	COND. SMD NPO 100pF 50V 0603 5%	YAGEO Ref.: 2222 867 15101	0,10
C85	COND. SMD Y5V 100nF 50V 0603 +80-20%	YAGEO Ref.: 2222 586 19812	0,10
C86	COND. SMD NP0 10pF 50V 0603 5%	YAGEO Ref.: 2222 867 15109	0,10
C87	COND. SMD X5R 10uF 35V 1210 20%	TAIYO YUDEN Ref.: GMK325BJ106MH-T	0,17
C88	COND. SMD Y5V 100nF 50V 0603 +80-20%	YAGEO Ref.: 2222 586 19812	0,10
C89	COND. SMD NP0 10pF 50V 0603 5%	YAGEO Ref.: 2222 867 15109	0,10
C90	COND. SMD Y5V 100nF 50V 0603 +80-20%	YAGEO Ref.: 2222 586 19812	0,10
C91	COND. SMD NP0 10pF 50V 0603 5%	YAGEO Ref.: 2222 867 15109	0,10
C92	COND. SMD X7R 220nF 63V 1210 10%	TEKELEC Ref.: 630S41X224KP	0,07
C93	COND. SMD X5R 1uF 16V 0805 10%	TAIYO YUDEN Ref.:EMK212BJ105KG-T	0,10
C94	COND. SMD X5R 1uF 16V 0805 10%	TAIYO YUDEN Ref.:EMK212BJ105KG-T	0,10
C95	COND. SMD X7R 1nF 50V 0603 10%	YAGEO Ref.: 2222 586 156 23	0,10
C96	COND. SMD X7R 1nF 50V 0603 10%	YAGEO Ref.: 2222 586 156 23	0,10
C97	COND. SMD X7R 1nF 50V 0603 10%	YAGEO Ref.: 2222 586 156 23	0,10
C98	COND. SMD X7R 1nF 50V 0603 10%	YAGEO Ref.: 2222 586 156 23	0,10
C99	COND. SMD MULTICAPA Y BAJA ESR 22uF 16V 1210 X5R 20%	TAIYO YUDEN REF:EMK325BJ226MM-T	0,13
C100	COND. SMD NP0 10pF 50V 0603 5%	YAGEO Ref.: 2222 867 15109	0,10
C101	COND. SMD NPO 100pF 50V 0603 5%	YAGEO Ref.: 2222 867 15101	0,10
C102	COND. SMD Y5V 100nF 50V 0603 +80-20%	YAGEO Ref.: 2222 586 19812	0,10
C103	COND. SMD NP0 10pF 50V 0603 5%	YAGEO Ref.: 2222 867 15109	0,10

C104	COND. SMD NP0 10pF 50V 0603 5%	YAGEO Ref.: 2222 867 15109	0,10
C105	COND. SMD Y5V 100nF 50V 0603 +80-20%	YAGEO Ref.: 2222 586 19812	0,10
C017	COND. SMD X7R 1nF 50V 0603 10%	YAGEO Ref.: 2222 586 156 23	0,10
C018	COND. SMD NPO 100pF 50V 0603 5%	YAGEO Ref.: 2222 867 15101	0,10
C109	COND. SMD Y5V 100nF 50V 0603 +80-20%	YAGEO Ref.: 2222 586 19812	0,10
C110	COND. SMD NP0 10pF 50V 0603 5%	YAGEO Ref.: 2222 867 15109	0,10
C111	COND. SMD NPO 100pF 50V 0603 5%	YAGEO Ref.: 2222 867 15101	0,10
C112	COND. SMD Y5V 100nF 50V 0603 +80-20%	YAGEO Ref.: 2222 586 19812	0,10
C113	COND. SMD Y5V 100nF 50V 0603 +80-20%	YAGEO Ref.: 2222 586 19812	0,10
C114	COND. SMD NP0 10pF 50V 0603 5%	YAGEO Ref.: 2222 867 15109	0,10
C115	COND. SMD NPO 100pF 50V 0603 5%	YAGEO Ref.: 2222 867 15101	0,10
C116	COND. SMD X7R 1nF 50V 0603 10%	YAGEO Ref.: 2222 586 156 23	0,10
C117	COND. SMD NP0 10pF 50V 0603 5%	YAGEO Ref.: 2222 867 15109	0,10
C118	COND. SMD Y5V 100nF 50V 0603 +80-20%	YAGEO Ref.: 2222 586 19812	0,10
C119	COND. SMD NPO 100pF 50V 0603 5%	YAGEO Ref.: 2222 867 15101	0,10
C120	COND. SMD NP0 10pF 50V 0603 5%	YAGEO Ref.: 2222 867 15109	0,10
C121	COND. SMD X7R 1nF 50V 0603 10%	YAGEO Ref.: 2222 586 156 23	0,10
C122	COND. SMD X7R 1nF 50V 0603 10%	YAGEO Ref.: 2222 586 156 23	0,10
C123	COND. SMD X7R 1nF 50V 0603 10%	YAGEO Ref.: 2222 586 156 23	0,10
C124	COND. SMD X7R 1nF 50V 0603 10%	YAGEO Ref.: 2222 586 156 23	0,10
C125	COND. SMD NP0 10pF 50V 0603 5%	YAGEO Ref.: 2222 867 15109	0,10
C126	COND. SMD NPO 100pF 50V 0603 5%	YAGEO Ref.: 2222 867 15101	0,10
C127	COND. SMD NPO 100pF 50V 0603 5%	YAGEO Ref.: 2222 867 15101	0,10
CA21	COND. SMD Y5V 100nF 50V 0603 +80-20%	YAGEO Ref.: 2222 586 19812	0,10
CA22	COND. SMD Y5V 100nF 50V 0603 +80-20%	YAGEO Ref.: 2222 586 19812	0,10
CA23	COND. SMD Y5V 100nF 50V 0603 +80-20%	YAGEO Ref.: 2222 586 19812	0,10

CA24	COND. SMD Y5V 100nF 50V 0603 +80-20%	YAGEO Ref.: 2222 586 19812	0,10
CA31	COND. SMD Y5V 100nF 50V 0603 +80-20%	YAGEO Ref.: 2222 586 19812	0,10
CA32	COND. SMD Y5V 100nF 50V 0603 +80-20%	YAGEO Ref.: 2222 586 19812	0,10
CA33	COND. SMD Y5V 100nF 50V 0603 +80-20%	YAGEO Ref.: 2222 586 19812	0,10
CA34	COND. SMD Y5V 100nF 50V 0603 +80-20%	YAGEO Ref.: 2222 586 19812	0,10
J2	CONEC. SMB MACHO RECTO P/C.I.	SUHNER Ref.: 82SMB-50-0-1/133	0,81
J3	CONEC. SMB MACHO RECTO P/C.I.	SUHNER Ref.: 82SMB-50-0-1/133	0,81
J4	CONEC. SMB MACHO RECTO P/C.I.	SUHNER Ref.: 82SMB-50-0-1/133	0,81
J1	CONNEC. EMCV 1,5/ 2-GF-3,81	PHOENIX Ref.: 1879285	1,10
J5	CONEC. SUB-D MACHO 9 VIAS 90º P/ C.I. METALIC	AMP Ref.: 164492-1	2,07
D1	DIODO SCHOTTKY SMD 40V 3A MBRS340T3G SMC	RS Ref.: 545-2080	0,24
D3	DIODO SCHOTTKY SMD 40V 3A MBRS340T3G SMC	RS Ref.: 545-2080	0,24
SW1	MICROINT. 4 CIRCUITOS SMD	ONDA RADIO Ref.: DIP9704	0,42
SW2	MICROINT. 4 CIRCUITOS SMD	ONDA RADIO Ref.: DIP9704	0,42
SW3	MICROINT. 4 CIRCUITOS SMD	ONDA RADIO Ref.: DIP9704	0,42
D2	LED VERDE SMD (1206) 1206	AVAGO Ref.: HSMG-C150	0,04
D4	LED VERDE SMD (1206) 1206	AVAGO Ref.: HSMG-C150	0,04
D5	LED VERDE SMD (1206) 1206	AVAGO Ref.: HSMG-C150	0,04
D6	LED VERDE SMD (1206) 1206	AVAGO Ref.: HSMG-C150	0,04
R1	RESIST. SMD 100mW 100ppm 10K 0603 1%	YAGEO Ref.: 2322 7046 103	0,01
R2	RESIST. SMD 100mW 100ppm 180R 0603 1%	YAGEO Ref.: 2322 7046 180R	0,01
R3	RESIST. SMD 100mW 100ppm 180R 0603 1%	YAGEO Ref.: 2322 7046 180R	0,01
R4	RESIST. SMD 100mW 100ppm 180R 0603 1%	YAGEO Ref.: 2322 7046 180R	0,01
R5	RESIST. SMD 100mW 100ppm 180R 0603 1%	YAGEO Ref.: 2322 7046 180R	0,01
R7	RESIST. SMD 100mW 1K1 0603 1%	YAGEO Ref.: 2322 7046 1102	0,01

R8	RESIST. SMD 100mW 100ppm 10K 0603 1%	YAGEO Ref.: 2322 7046 103	0,01
R10	RESIST. SMD 0R 0603 1%	YAGEO Ref.: 2322 7049 2006	0,01
R11	RESIST. SMD 0R 0603 1%	YAGEO Ref.: 2322 7049 2006	0,01
R12	RESIST. SMD 100mW 1K1 0603 1%	YAGEO Ref.: 2322 7046 1102	0,01
R13	RESIST. SMD 100mW 100ppm 10K 0603 1%	YAGEO Ref.: 2322 7046 103	0,01
R16	RESIST. SMD 100mW 18R 0603 1%	YAGEO Ref.: 2322 7046 1809	0,01
R17	RESIST. SMD 100mW 270R 0603 1%	YAGEO Ref.: 2322 7046 2701	0,01
R18	RESIST. SMD 100mW 100ppm 10K 0603 1%	YAGEO Ref.: 2322 7046 103	0,01
R19	RESIST. SMD 0R 0603 1%	YAGEO Ref.: 2322 7049 2006	0,01
R20	RESIST. SMD 100mW 100ppm 1K 0603 1%	YAGEO Ref.: 2322 7046 102	0,01
R21	RESIST. SMD 100mW 100ppm 10R 0603 1%	YAGEO Ref.: 2322 7046 109	0,01
R22	RESIST. SMD 100mW 18R 0603 1%	YAGEO Ref.: 2322 7046 1809	0,01
R23	RESIST. SMD 100mW 18R 0603 1%	YAGEO Ref.: 2322 7046 1809	0,01
R25	RESIST. SMD 0R 0603 1%	YAGEO Ref.: 2322 7049 2006	0,01
R26	RESIST. SMD 0R 0603 1%	YAGEO Ref.: 2322 7049 2006	0,01
R28	RESIST. SMD 100mW 82K 0603 1%	YAGEO Ref.: 2322 7046 8203	0,01
R29	RESIST. SMD 100mW 160R 0603 1%	YAGEO Ref.: 2322 7046 1601	0,01
R30	RESIST. SMD 100mW 5K1 0603 1%	YAGEO Ref.: 2322 7046 5102	0,01
R32	RESIST. SMD 0R 0603 1%	YAGEO Ref.: 2322 7049 2006	0,01
R33	RESIST. SMD 0R 0603 1%	YAGEO Ref.: 2322 7049 2006	0,01
R34	RESIST. SMD 100mW 100ppm 330R 0603 1%	YAGEO Ref.: 2322 7046 331	0,01
R35	RESIST. SMD 100mW 8K2 0603 1%	YAGEO Ref.: 2322 7046 8202	0,01
R36	RESIST. SMD 100mW 100ppm 51R 0603 1%	YAGEO Ref.: 2322 7046 519	0,01
R38	RESIST. SMD 100mW 100ppm 330R 0603 1%	YAGEO Ref.: 2322 7046 331	0,01
R40	RESIST. SMD 0R 0603 1%	YAGEO Ref.: 2322 7049 2006	0,01

R41	RESIST. SMD 0R 0603 1%	YAGEO Ref.: 2322 7049 2006	0,01
R43	RESIST. SMD 100mW 100ppm 330R 0603 1%	YAGEO Ref.: 2322 7046 331	0,01
R45	RESIST. SMD 100mW 100ppm 330R 0603 1%	YAGEO Ref.: 2322 7046 331	0,01
R46	RESIST. SMD 100mW 100ppm 10K 0603 1%	YAGEO Ref.: 2322 7046 103	0,01
R47	RESIST. SMD 0R 0603 1%	YAGEO Ref.: 2322 7049 2006	0,01
R48	RESIST. SMD 100mW 18R 0603 1%	YAGEO Ref.: 2322 7046 1809	0,01
R49	RESIST. SMD 100mW 200R 0603 1%	YAGEO Ref.: 2322 7046 2001	0,01
R50	RESIST. SMD 100mW 100ppm 10K 0603 1%	YAGEO Ref.: 2322 7046 103	0,01
R51	RESIST. SMD 0R 0603 1%	YAGEO Ref.: 2322 7049 2006	0,01
R52	RESIST. SMD 100mW 100ppm 1K 0603 1%	YAGEO Ref.: 2322 7046 102	0,01
R53	RESIST. SMD 100mW 100ppm 100R 0603 1%	YAGEO Ref.: 2322 7046 101	0,01
R54	RESIST. SMD 100mW 18R 0603 1%	YAGEO Ref.: 2322 7046 1809	0,01
R55	RESIST. SMD 100mW 18R 0603 1%	YAGEO Ref.: 2322 7046 1809	0,01
R57	RESIST. SMD 0R 0603 1%	YAGEO Ref.: 2322 7049 2006	0,01
R59	RESIST. SMD 100mW 82K 0603 1%	YAGEO Ref.: 2322 7046 8203	0,01
R60	RESIST. SMD 100mW 160R 0603 1%	YAGEO Ref.: 2322 7046 1601	0,01
R61	RESIST. SMD 100mW 5K1 0603 1%	YAGEO Ref.: 2322 7046 5102	0,01
R63	RESIST. SMD 0R 0603 1%	YAGEO Ref.: 2322 7049 2006	0,01
R64	RESIST. SMD 0R 0603 1%	YAGEO Ref.: 2322 7049 2006	0,01
R65	RESIST. SMD 100mW 100ppm 330R 0603 1%	YAGEO Ref.: 2322 7046 331	0,01
R66	RESIST. SMD 100mW 8K2 0603 1%	YAGEO Ref.: 2322 7046 8202	0,01
R67	RESIST. SMD 100mW 100ppm 51R 0603 1%	YAGEO Ref.: 2322 7046 519	0,01
R70	RESIST. SMD 0R 0603 1%	YAGEO Ref.: 2322 7049 2006	0,01
R71	RESIST. SMD 100mW 100ppm 330R 0603 1%	YAGEO Ref.: 2322 7046 331	0,01
R72	RESIST. SMD 0R 0603 1%	YAGEO Ref.: 2322 7049 2006	0,01
R74	RESIST. SMD 100mW 100ppm 330R 0603 1%	YAGEO Ref.: 2322 7046 331	0,01

R76	RESIST. SMD 100mW 100ppm 330R 0603 1%	YAGEO Ref.: 2322 7046 331	0,01
R77	RESIST. SMD 0R 0603 1%	YAGEO Ref.: 2322 7049 2006	0,01
R78	RESIST. SMD 100mW 200R 0603 1%	YAGEO Ref.: 2322 7046 2001	0,01
R79	RESIST. SMD 100mW 100ppm 10K 0603 1%	YAGEO Ref.: 2322 7046 103	0,01
R80	RESIST. SMD 100mW 3K3 0603 1%	YAGEO Ref.: 2322 7046 3302	0,01
R81	RESIST. SMD 100mW 100ppm 1K 0603 1%	YAGEO Ref.: 2322 7046 102	0,01
R82	RESIST. SMD 100mW 7K5 0603 1%	YAGEO Ref.: 2322 7046 7502	0,01
R83	RESIST. SMD 100mW 1K3 0603 1%	YAGEO Ref.: 2322 7046 1302	0,01
R84	RESIST. SMD 100mW 2K 0603 1%	YAGEO Ref.: 2322 7046 2002	0,01
R85	RESIST. SMD 100mW 100ppm 10K 0603 1%	YAGEO Ref.: 2322 7046 103	0,01
R87	RESIST. SMD 0R 0603 1%	YAGEO Ref.: 2322 7049 2006	0,01
R89	RESIST. SMD 100mW 100ppm 51R 0603 1%	YAGEO Ref.: 2322 7046 519	0,01
R90	RESIST. SMD 100mW 100ppm 51R 0603 1%	YAGEO Ref.: 2322 7046 519	0,01
R92	RESIST. SMD 0R 0603 1%	YAGEO Ref.: 2322 7049 2006	0,01
R94	RESIST. SMD 0R 0603 1%	YAGEO Ref.: 2322 7049 2006	0,01
R95	RESIST. SMD 0R 0603 1%	YAGEO Ref.: 2322 7049 2006	0,01
R96	RESIST. SMD 100mW 5K1 0603 1%	YAGEO Ref.: 2322 7046 5102	0,01
R97	RESIST. SMD 100mW 47K 0603 1%	YAGEO Ref.: 2322 7046 4703	0,01
R98	RESIST. SMD 100mW 47K 0603 1%	YAGEO Ref.: 2322 7046 4703	0,01
R99	RESIST. SMD 0R 0603 1%	YAGEO Ref.: 2322 7049 2006	0,01
R100	RESIST. SMD 100mW 13K 0603 1%	YAGEO Ref.: 2322 7046 1303	0,01
R101	RESIST. SMD 100mW 6K2 0603 1%	YAGEO Ref.: 2322 7046 6202	0,01
R102	RESIST. SMD 100mW 2K 0603 1%	YAGEO Ref.: 2322 7046 2002	0,01
R103	RESIST. SMD 0R 0603 1%	YAGEO Ref.: 2322 7049 2006	0,01
R105	RESIST. SMD 100mW 2K 0603 1%	YAGEO Ref.: 2322 7046 2002	0,01

R106	RESIST. SMD 100mW 200R 0603 1%	YAGEO Ref.: 2322 7046 2001	0,01
R107	RESIST. SMD 100mW 100ppm 10K 0603 1%	YAGEO Ref.: 2322 7046 103	0,01
R108	RESIST. SMD 100mW 3K3 0603 1%	YAGEO Ref.: 2322 7046 3302	0,01
R109	RESIST. SMD 0R 0603 1%	YAGEO Ref.: 2322 7049 2006	0,01
R111	RESIST. SMD 100mW 2K 0603 1%	YAGEO Ref.: 2322 7046 2002	0,01
R112	RESIST. SMD 100mW 100ppm 1K 0603 1%	YAGEO Ref.: 2322 7046 102	0,01
R113	RESIST. SMD 100mW 100ppm 10K 0603 1%	YAGEO Ref.: 2322 7046 103	0,01
R115	RESIST. SMD 0R 0603 1%	YAGEO Ref.: 2322 7049 2006	0,01
R117	RESIST. SMD 100mW 100ppm 51R 0603 1%	YAGEO Ref.: 2322 7046 519	0,01
R118	RESIST. SMD 100mW 100ppm 51R 0603 1%	YAGEO Ref.: 2322 7046 519	0,01
R120	RESIST. SMD 0R 0603 1%	YAGEO Ref.: 2322 7049 2006	0,01
R122	RESIST. SMD 100mW 20K 0603 1%	YAGEO Ref.: 2322 7046 2003	0,01
R124	RESIST. SMD 100mW 2K 0603 1%	YAGEO Ref.: 2322 7046 2002	0,01
R125	RESIST. SMD 100mW 47K 0603 1%	YAGEO Ref.: 2322 7046 4703	0,01
R126	RESIST. SMD 100mW 47K 0603 1%	YAGEO Ref.: 2322 7046 4703	0,01
R127	RESIST. SMD 0R 0603 1%	YAGEO Ref.: 2322 7049 2006	0,01
R128	RESIST. SMD 0R 0603 1%	YAGEO Ref.: 2322 7049 2006	0,01
R129	RESIST. SMD 100mW 160R 0603 1%	YAGEO Ref.: 2322 7046 1601	0,01
R130	RESIST. SMD 0R 0603 1%	YAGEO Ref.: 2322 7049 2006	0,01
R131	RESIST. SMD 0R 0603 1%	YAGEO Ref.: 2322 7049 2006	0,01
R132	RESIST. SMD 0R 0603 1%	YAGEO Ref.: 2322 7049 2006	0,01
R133	RESIST. SMD 0R 0603 1%	YAGEO Ref.: 2322 7049 2006	0,01
R134	RESIST. SMD 0R 0603 1%	YAGEO Ref.: 2322 7049 2006	0,01
R135	RESIST. SMD 0R 0603 1%	YAGEO Ref.: 2322 7049 2006	0,01
R136	RESIST. SMD 0R 0603 1%	YAGEO Ref.: 2322 7049 2006	0,01
R137	RESIST. SMD 0R 0603 1%	YAGEO Ref.: 2322 7049 2006	0,01

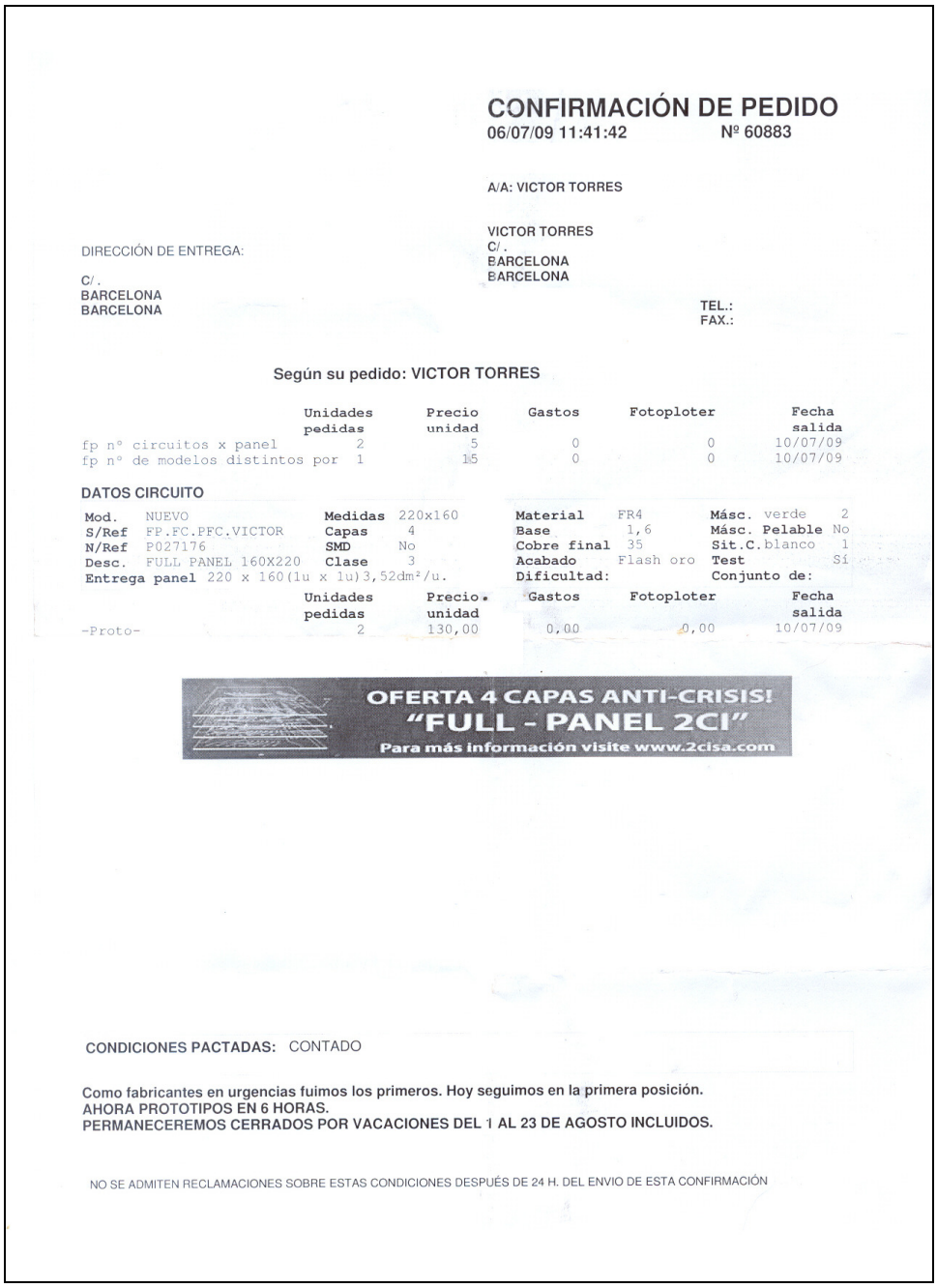
R138	RESIST. SMD 0R 0603 1%	YAGEO Ref.: 2322 7049 2006	0,01
R139	RESIST. SMD 0R 0603 1%	YAGEO Ref.: 2322 7049 2006	0,01
R140	RESIST. SMD 0R 0603 1%	YAGEO Ref.: 2322 7049 2006	0,01
R141	RESIST. SMD 0R 0603 1%	YAGEO Ref.: 2322 7049 2006	0,01
R142	RESIST. SMD 100mW 100ppm 10K 0603 1%	YAGEO Ref.: 2322 7046 103	0,01
R143	RESIST. SMD 100mW 100ppm 10K 0603 1%	YAGEO Ref.: 2322 7046 103	0,01
R144	RESIST. SMD 0R 0603 1%	YAGEO Ref.: 2322 7049 2006	0,01
RA51	RESIST. SMD 100mW 100ppm 470R 0603 1%	YAGEO Ref.: 2322 7046 471	0,01
RA52	RESIST. SMD 100mW 100ppm 470R 0603 1%	YAGEO Ref.: 2322 7046 471	0,01
RA53	RESIST. SMD 100mW 100ppm 470R 0603 1%	YAGEO Ref.: 2322 7046 471	0,01
RA54	RESIST. SMD 100mW 100ppm 470R 0603 1%	YAGEO Ref.: 2322 7046 471	0,01
RA71	RESIST. SMD 100mW 7K5 0603 1%	YAGEO Ref.: 2322 7046 7502	0,01
RA72	RESIST. SMD 100mW 3K3 0603 1%	YAGEO Ref.: 2322 7046 3302	0,01
RA73	RESIST. SMD 100mW 2K4 0603 1%	YAGEO Ref.: 2322 7046 2402	0,01
RA74	RESIST. SMD 100mW 7K5 0603 1%	YAGEO Ref.: 2322 7046 7502	0,01
RA101	RESIST. SMD 100mW 300R 0603 1%	YAGEO Ref.: 2322 7046 3001	0,01
RA102	RESIST. SMD 100mW 300R 0603 1%	YAGEO Ref.: 2322 7046 3001	0,01
T1	TRANSISTOR SMD BC847B SOT23	(PHILIPS)(23N0026)	0,01
T2	TRANSISTOR SMD BC847B SOT23	(PHILIPS)(23N0026)	0,01
T3	TRANSISTOR SMD BC847B SOT23	(PHILIPS)(23N0026)	0,01

El coste total de componentes que forman la placa de circuito impreso sube a 81,26 euros.

5.1.3 COSTES DE FABRICACIÓN

Para la realización física de la placa de circuito impreso se contrata una empresa externa. Se han fabricado cuatro PCB, es la cantidad mínima, a un precio total de 285 euros en conjunto. Existen varias empresas en España dedicadas a la fabricación de circuitos impresos: WÜRTH ELEKTRONIK, 2CI, LABCIRCUITS, son un pequeño ejemplo.

Concretamente la fabricación de la PCB de este proyecto, se ha contratado a la empresa catalana 2CI. A continuación se detalla los diferentes costes de fabricación.



CONFIRMACIÓN DE PEDIDO
06/07/09 11:41:42 Nº 60883

A/A: VICTOR TORRES

VICTOR TORRES
C/.
BARCELONA
BARCELONA

DIRECCIÓN DE ENTREGA:
C/.
BARCELONA
BARCELONA

TEL.:
FAX.:

Según su pedido: VICTOR TORRES

	Unidades pedidas	Precio unidad	Gastos	Fotoploter	Fecha salida
fp nº circuitos x panel	2	5	0	0	10/07/09
fp nº de modelos distintos por	1	15	0	0	10/07/09

DATOS CIRCUITO

Mod. NUEVO	Medidas 220x160	Material FR4	Másc. verde 2		
S/Ref FP.FC.PFC.VICTOR	Capas 4	Base 1,6	Másc. Pelable No		
N/Ref P027176	SMD No	Cobre final 35	Sit.C.blanco 1		
Desc. FULL PANEL 160X220	Clase 3	Acabado Flash oro	Test Sí		
Entrega panel 220 x 160(1u x 1u)3,52dm²/u.		Dificultad:	Conjunto de:		

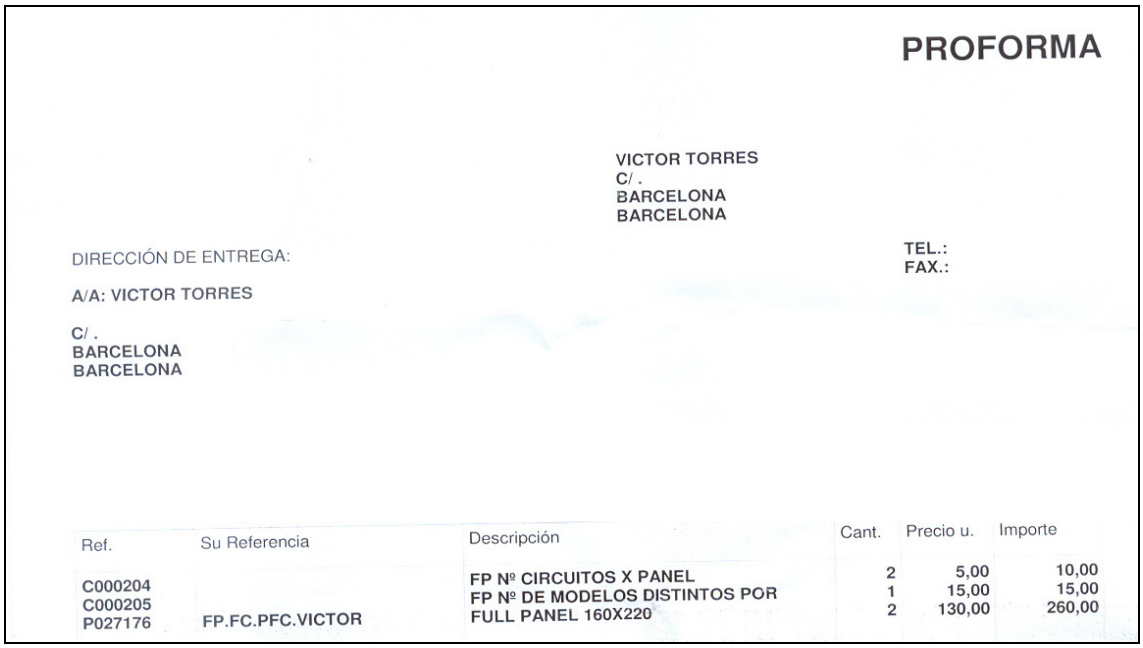
	Unidades pedidas	Precio unidad	Gastos	Fotoploter	Fecha salida
-Proto-	2	130,00	0,00	0,00	10/07/09

CONDICIONES PACTADAS: CONTADO

Como fabricantes en urgencias fuimos los primeros. Hoy seguimos en la primera posición.
AHORA PROTOTIPOS EN 6 HORAS.
PERMANECEREMOS CERRADOS POR VACACIONES DEL 1 AL 23 DE AGOSTO INCLUIDOS.

NO SE ADMITEN RECLAMACIONES SOBRE ESTAS CONDICIONES DESPUÉS DE 24 H. DEL ENVIO DE ESTA CONFIRMACIÓN

En el pedido se detalla el tipo de material a utilizar en la fabricación de la PCB, el precio de fabricación y la fecha de entrega del producto terminado.



PROFORMA

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TEL.:
FAX.:

Ref.	Su Referencia	Descripción	Cant.	Precio u.	Importe
C000204		FP Nº CIRCUITOS X PANEL	2	5,00	10,00
C000205		FP Nº DE MODELOS DISTINTOS POR	1	15,00	15,00
P027176	FP.FC.PFC.VICTOR	FULL PANEL 160X220	2	130,00	260,00

Es interesante observar que estas empresas obligan a fabricar una cantidad mínima de placas siendo las de tipo prototipo mucho más caras que las del tipo para serie. Así por ejemplo, la cantidad mínima de fabricación para PCB del tipo prototipo es de 2 unidades siendo el costo de cada unidad de 130 euros. Si a posteriori quisiéramos fabricar estas PCB, pero no ya en forma de prototipo sino a nivel de serie o pre-serie, entonces el precio por PCB disminuiría a 5 euros la unidad.

5.2 CONCLUSIONES

Los osciladores locales diseñados están pensados para ir incorporados dentro de la cadena de recepción de un receptor de Televisión Digital Terrestre. Dichos sintetizadores irán concatenados con lo cual la figura de ruido del oscilador final será el resultado de la suma de las dos OL obtenidas, OL1 y OL2 por separado.

La norma, como se ha dicho, aún no establece ningún límite específico en cuanto a ruido de fase de los osciladores se refiere. Actualmente, se acostumbra a respetar la máscara crítica que especifica el propio cliente del diseño.

Una especificación común de requerimiento de ruido de fase es la que sigue:

Frecuencia	***Máscara Crítica***
10Hz	-55dBc/Hz
100Hz	-75 dBc/Hz
1KHz	-85 dBc/Hz
10KHz	-95 dBc/Hz
100KHz	-100 dBc/Hz
1MHz	-110 dBc/Hz

Sabiendo que la suma de los ruidos de fase se obtiene mediante la siguiente ecuación:

SUMA OL's=10*LOG10(10^(OL1/10)+10^(OL2/10))

Obtenemos los siguientes resultados para los distintos extremos de frecuencias a sintetizar.

Frecuencia (Hz)	***Máscara (dBc/Hz)***	***OL1(dBc/Hz)***	***OL2(dBc/Hz)***	***Suma_OL(dBc/Hz)***
100	-85	-80	-80	**-76,99**
1K	-85	-92	-92	**-88,99**
10K	-95	-92	-85	**-84,21**
100K	-110	-100	-100	**-96,99**
1M	-130	-120	-125	**-118,81**

Frecuencia (Hz)	***Máscara (dBc/Hz)***	***OL1(dBc/Hz)***	***OL2(dBc/Hz)***	***Suma_OL(dBc/Hz)***
100	-85	-75	-90	**-74,86**
1K	-85	-92	-90	**-87,88**
10K	-95	-90	-85	**-83,81**
100K	-110	-105	-100	**-98,81**
1M	-130	-120	-123	**-118,24**

Viendo los resultados observamos que sumando el ruido de fase de los dos osciladores locales que participan en el proceso de recepción de la señal cumpliríamos prácticamente la máscara espectral especificada, aunque no en su totalidad. Estamos un poco por fuera de especificación para el caso de las frecuencias de 10K y 100K siendo el ruido de fase respectivamente de -95<-84 y -100<-96 en el peor caso.

Mejorar ligeramente el ruido de fase en ésta zona no es difícil, simplemente hay que reconfigurar los valores de los componentes en el filtro de lazo de los osciladores, de manera que relajamos las zonas dónde el ruido de fase actual es sobrante y mejoramos en aquellas zonas donde necesitamos mejor respuesta. La simulación mediante el programa ADIsimPLL es la mejor manera de conseguir dicho objetivo rápidamente.

En conclusión, se ha conseguido simular, realizar y validar los osciladores locales que pueden formar parte de la etapa de recepción de un receptor de Televisión Digital Terrestre.

Los pasos seguidos, desde el inicio de la especificación hasta la comprobación física y diseño de la PCB se pueden utilizar además como guía para diseñar los osciladores locales para distintos receptores profesionales, de bandas diferentes a la descrita, como por ejemplo para las bandas S y L, o bien utilizar las técnicas descritas para implementar osciladores para diferentes tipologías de receptores.

Finalmente se ha validado que el diseño es viable de realizar a nivel económico, y que implica mayormente un coste inicial grande en materia de investigación y desarrollo.

Capítulo 6

6. LÍNEAS FUTURAS

6.1 LÍNEAS FUTURAS

6.1.1 DISEÑO DE LOS OSCILADORES PARA EL UPCONVERTER

En este trabajo se ha diseñado y realizado la síntesis de los osciladores locales para la recepción de un canal de Televisión dentro del estándar DVB-T. Los mismos osciladores locales realizados pueden utilizarse en la etapa de transmisión a la inversa mediante un simple acoplamiento en las dos señales. Visto a alto nivel tendríamos el siguiente sistema:

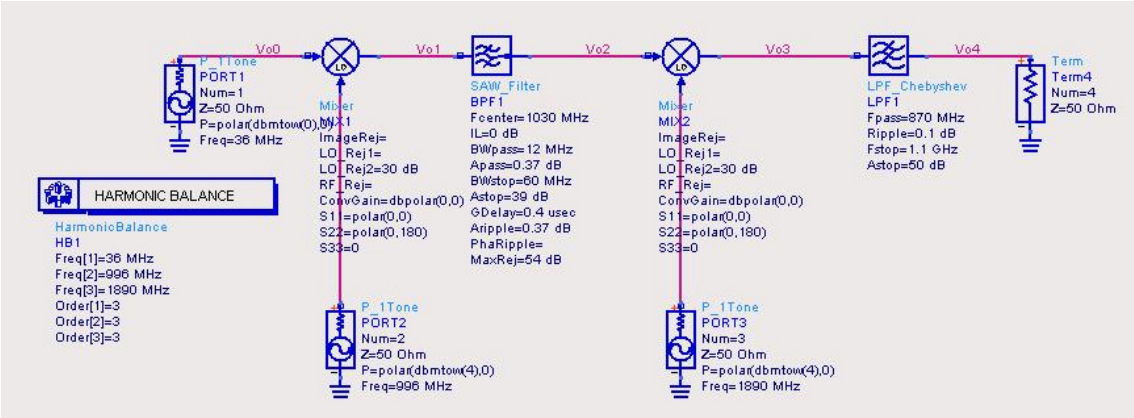

Figura 89. Visión de alto nivel del conversor ascendente

El OL1 traslada la FI de 36MHz a una banda estrecha, cuya frecuencia central es 1030 MHz. La frecuencia central de esta FI2 variará ligeramente en función del canal de salida. El rango de variación del OL1 será de 992MHz a 996MHz.

El filtro SAW paso banda BPF1 selecciona la banda útil, rechazando la banda imagen y el residuo de OL1. En este análisis se ha considerado un rechazo fuera de banda del SAW de 54 dB. Cabe la posibilidad de tener que incrementar este rechazo, cascadeando otro filtro o insertando otro de banda eliminada.

En el análisis se inyecta un tono de 36MHz y puede verse el espectro previo al filtro BPF1 (Vo1) y después del mismo (Vo2).

La frecuencia de OL2 variará de 1505MHZ a 1850MHz dependiendo del canal de salida, en saltos de 5MHz; de forma que en el mezclador MX2 se generará la banda de interés de 474MHz a 862 MHz y la banda imagen superior que será eliminada, junto con el residuo de OL, por el filtro paso bajo de salida, cuya frecuencia de corte será de 870 MHz.

En el análisis se muestra el espectro de salida antes (Vo3) y después del filtro paso bajo (Vo4) para el caso de una frecuencia de salida de 858MHz correspondiente al canal 69 de televisión.

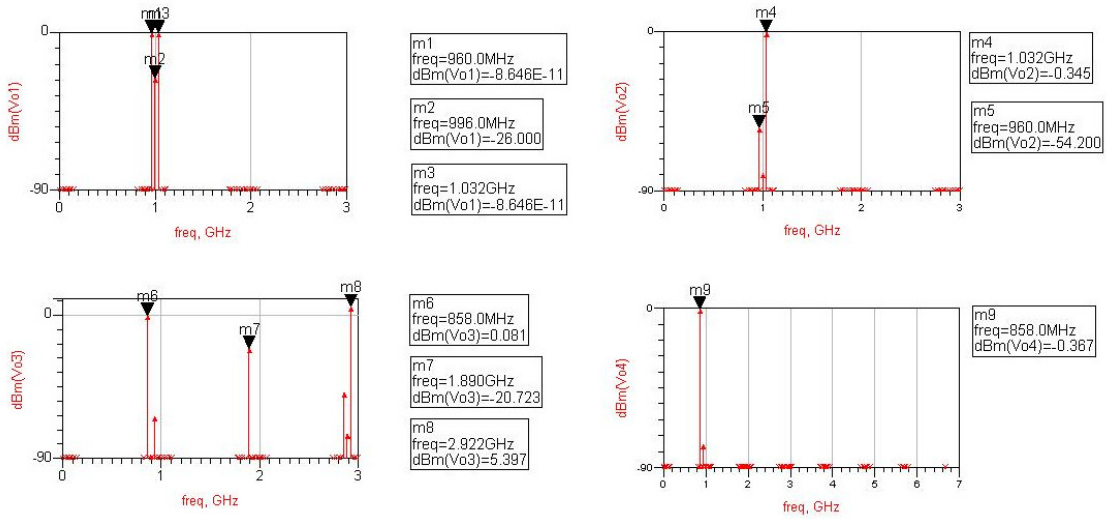

Figura 90. Resultados de la simulación del conversor ascendente

Por lo tanto, el mismo diseño de osciladores para la etapa de recepción realizado nos sirve para la etapa de transmisión.

6.1.2 DISEÑO DE LA CADENA DE RECEPCIÓN

El siguiente paso del proyecto sería realizar la cadena de recepción con doble conversión completa añadiendo la parte ya realizada de osciladores locales. Un estudio general de cómo iría la cadena de recepción es el siguiente:

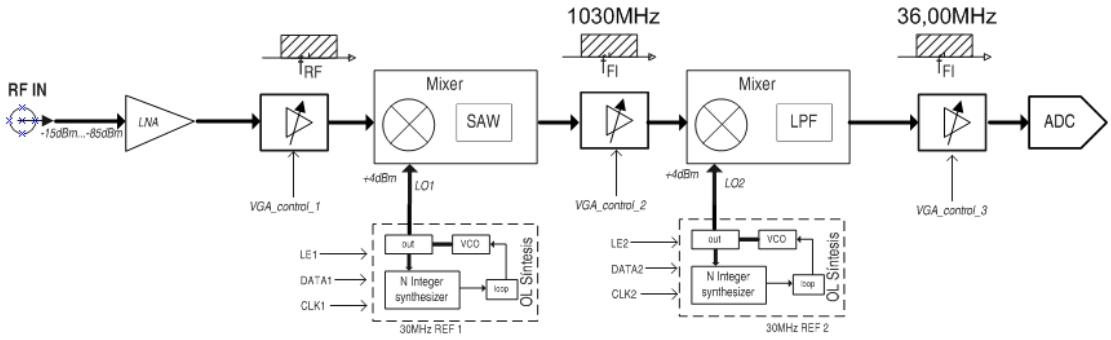

Figura 91. Cadena de recepción de doble conversión

El componente más crítico de la cadena de recepción es el LNA. Se debe utilizar un amplificador con figura de ruido muy baja, un alto valor de IP3, y un buen valor de amplificación. A nivel comercial, tenemos por ejemplo el amplificador SGC-6489ZDS, con las siguientes características eléctricas:

Parameter	Unit	100 MHz	500 MHz	850 MHz	1950 MHz	2140 MHz	2400 MHz	3500 MHz
Small Signal Gain (G)	dB	23.1	22.7	22.2	19.5	19.0	18.3	15.7
Output Third Order Intercept Point (OIP_3)	dBm	35.1	34.3	34.1	32.8	32.7	31.4	27.4
Output Power at 1dB Compression (P_{1dB})	dBm	21.8	20.9	20.6	19.2	19.0	18.4	15.2
input Return Loss (IRL)	dB	37.0	22.0	19.0	18.0	18.0	17.0	16.0
Output Return Loss (ORL)	dB	23.0	22.0	19.0	11.0	11.0	10.0	8.0
Reverse Isolation (S_{12})	dB	25.0	25.0	26.0	25.0	25.0	24.0	22.0
Noise Figure (NF)	dB	1.8	2.0	2.1	2.4	2.4	2.5	2.9

Observemos que tiene una alta ganancia de 22dB, un alto valor de IP3 a 34dB y una muy buena figura de ruido de 2dB. El único inconveniente que tiene es su adaptación S11 que esta justa, entonces debemos prever diseñar una red de adaptación para mejorar los 19dB de adaptación que pose el dispositivo.

Los diferentes *Voltage Gain Amplifiers* se utilizan para paliar las variaciones de los niveles de entrada de señal. Estos amplificadores deben de estar controlados digitalmente para mantener un nivel constante a la entrada del DAC para las distintas variaciones de nivel de señal de entrada.

Los Mixers los utilizamos para mezclar los OL's diseñados con la señal de RF para obtener finalmente la FI final de 36MHz. A la salida del DAC podemos conectar directamente una FPGA para la demodulación y el tratamiento digital de la señal en FI.

CAPÍTULO 7

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CAPÍTULO 8

8. ANEXOS

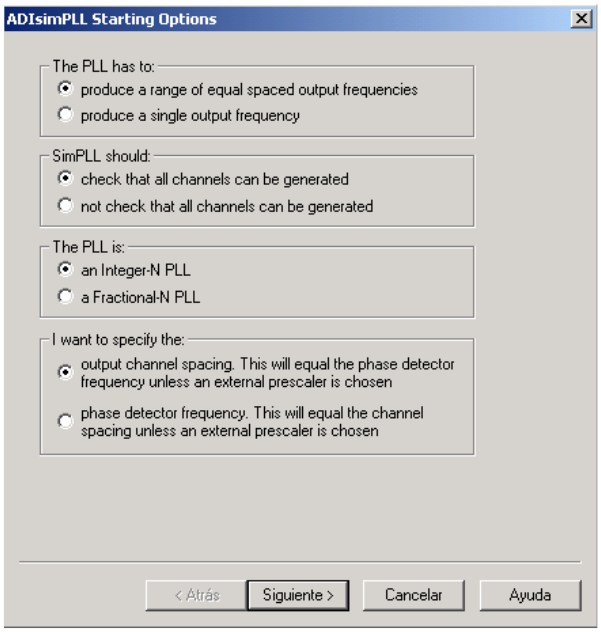
8.1 ADISIMPLL

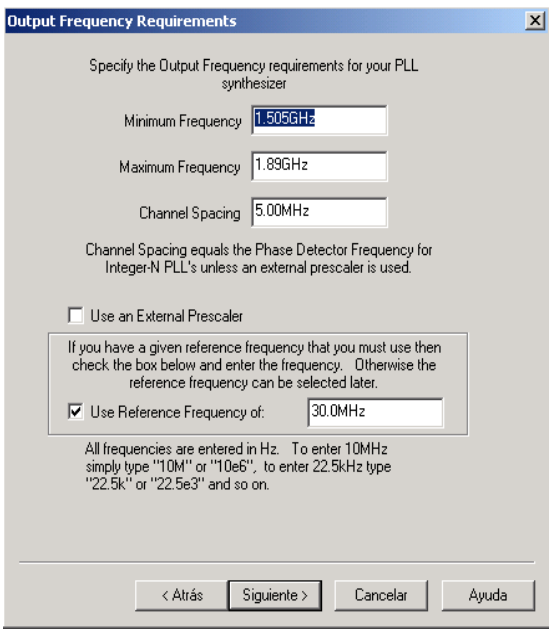
El software de diseño ADIsimPLL es una aplicación gratuita de análisis y diseño de PLL's del fabricante ANALOG DEVICES. El diseñador puede diseñar literalmente un PLL, determinando la frecuencia de síntesis, el tipo de integrado a utilizar, el tipo de VCO y el filtro de lazo. El programa es capaz de sintetizar diferentes resultados del diseño como son el ruido de fase, los espúreos generados, tiempo de cierre del lazo '*lock time*' entre otros.

El programa se basa en una hoja de cálculo sencilla e interactiva para el usuario donde se pueden configurar los distintos parámetros de configuración del PLL. Dichos parámetros se pueden alterar o modificar en tiempo real viendo su inmediato efecto en la simulación.

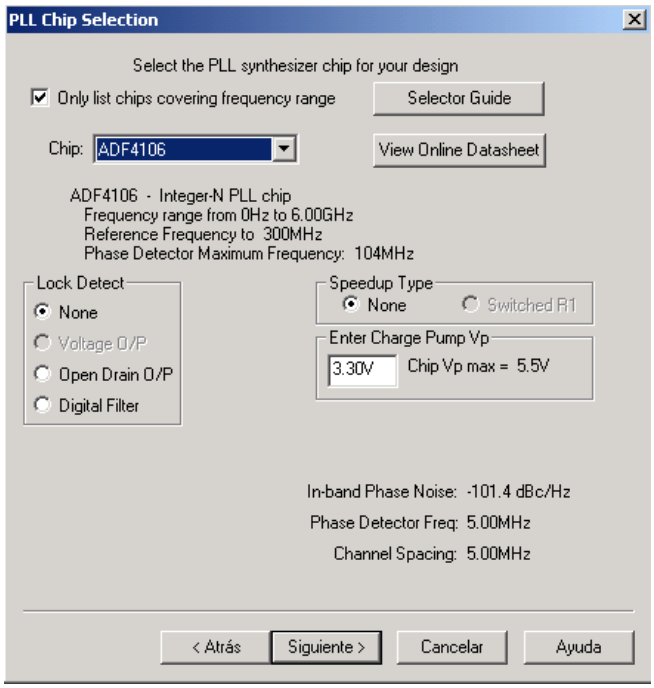
Los pasos básicos a seguir para el diseño del PLL son los siguientes:

1. Escoger una frecuencia de referencia, un rango de frecuencias de salida a sintetizar y el ancho de banda de los pasos de las frecuencias a sintetizar.

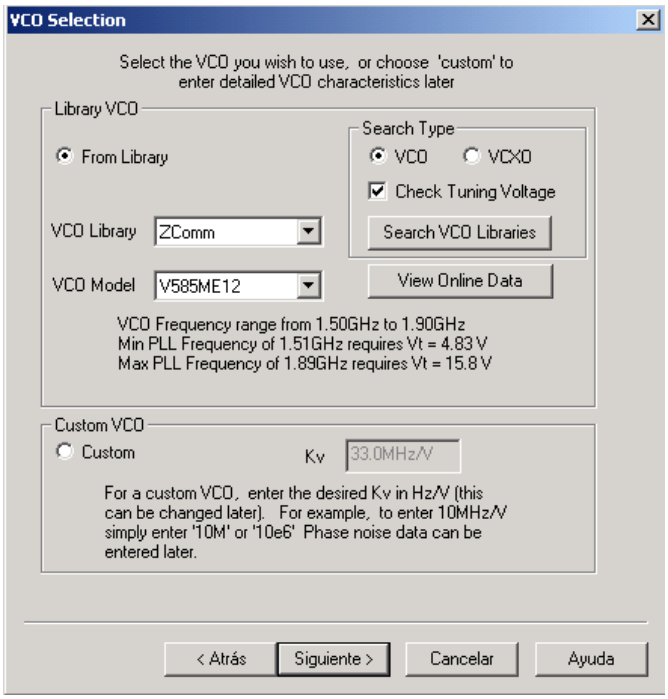




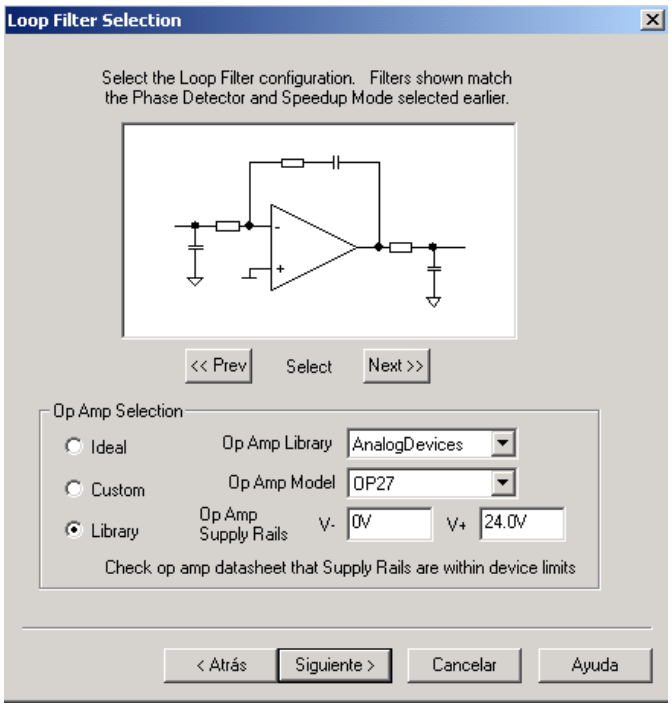
2. Seleccionar un integrado PLL de la biblioteca de componentes disponible.



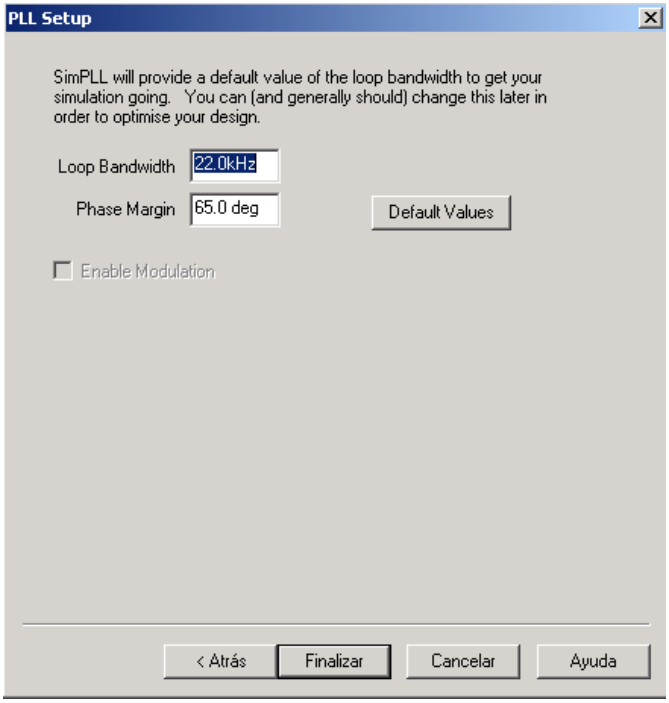
3. Seleccionar un VCO.



4. Seleccionar una topología de filtro.

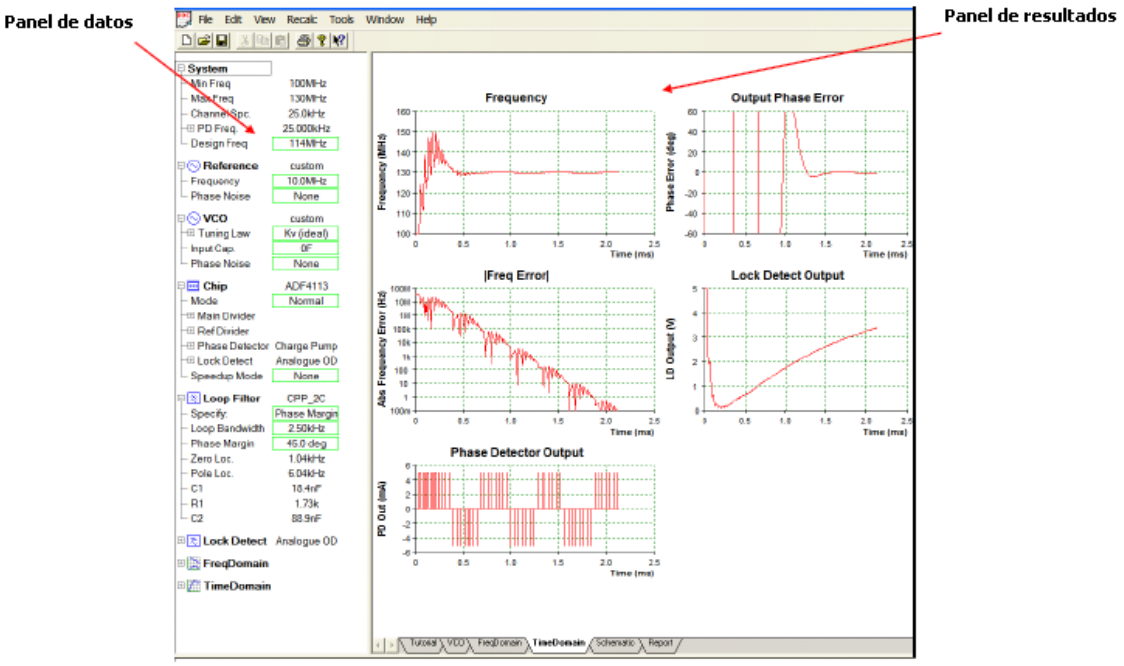


5. Ajustar el ancho de banda del filtro y el margen de fase.

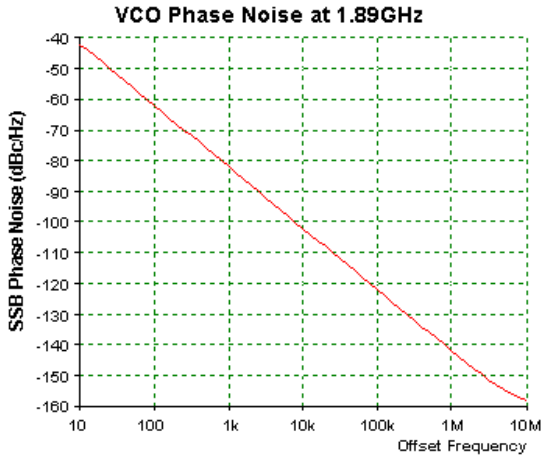


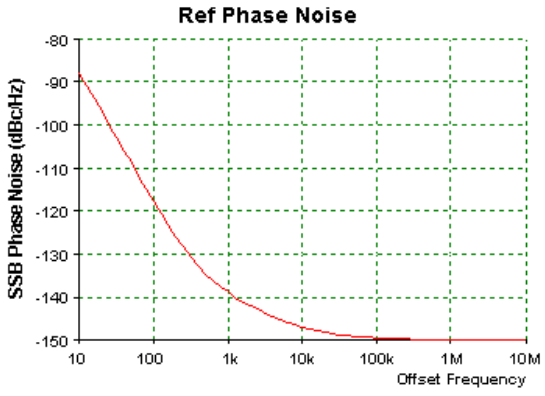
5. Ejecutar la simulación.
6. Evaluar los resultados obtenidos en el dominio del tiempo y la frecuencia.
7. Optimización de los resultados obtenidos

La siguiente figura es una muestra del panel de control de datos y del panel de resultados obtenidos en la simulación en el dominio temporal. Si los valores se cambian en el panel de datos, ese cambio se refleja instantáneamente en el panel de resultados.



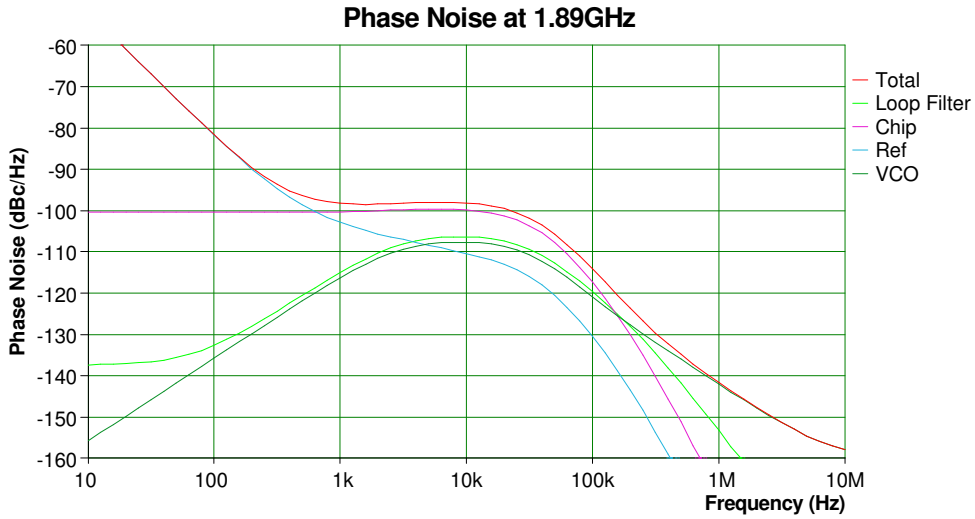
En el apartado '*Components*' observamos la característica de ruido de fase de la referencia así como la del VCO seleccionado.



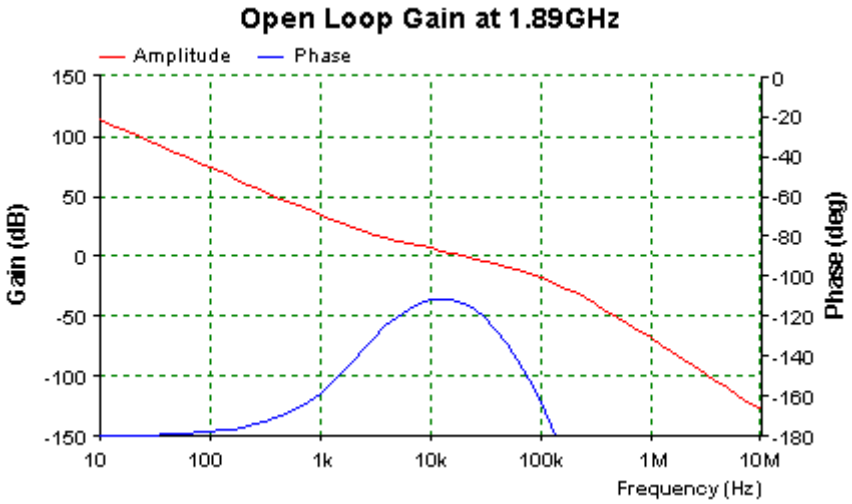


En el apartado '*Frequency domain*' obtenemos los resultados de la simulación en el dominio frecuencial siendo los resultados más importantes:

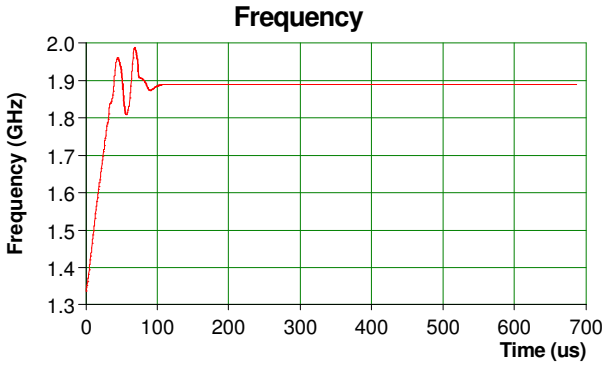
Característica de ruido de fase obtenida de nuestro PLL final con cada una de las contribuciones de cada elemento del bucle.



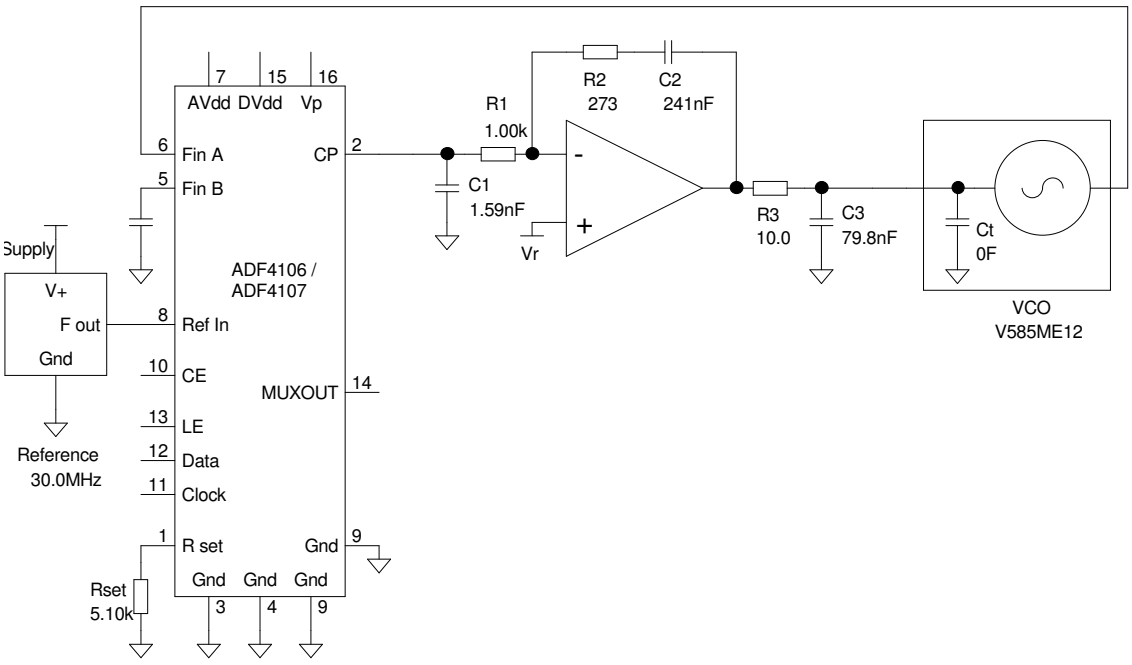
El siguiente gráfico determina el margen de fase y ancho del lazo y es importante para asegurar la estabilidad del lazo del PLL. Para un correcto diseño el margen obtenido debería rondar los 45º.



En el apartado de 'Time *domain*' se observan los resultados obtenidos, pero en el dominio temporal. En este punto, por ejemplo es interesante conocer el tiempo necesario del PLL para cerrar el bucle y quedar 'enganchado'.



En el apartado '*Schematic*' se obtiene el esquema eléctrico del PLL completo utilizando todos los componentes de diseño así como sus valores exactos para su posterior implementación práctica.



NotesADF4106:
1. Vp is the Charge Pump power supply
2. Vp >= Vdd
3. CE must be HIGH to operate
4. TSSOP pinouts shown
5. Consult manufacturer's data sheet for full details

Finalmente en el último de los apartados se resume en forma de datos, los resultados obtenidos siendo el más importante la tabla de ruido de fase en función de la frecuencia y la contribución de cada componente dentro del bucle.

Phase Noise Table

Freq	Total	VCO	Ref	Chip	Filter
1.00	-21.97	-175.8	-21.97	-100.5	-137.4
10.0	-51.96	-155.8	-51.96	-100.5	-137.3
100	-81.61	-135.8	-81.66	-100.5	-132.7
1.00k	-98.20	-116.3	-102.8	-100.3	-115.0
3.00k	-98.22	-109.6	-106.9	-99.80	-108.3
10.0k	-98.15	-107.6	-110.4	-99.85	-106.4
100k	-114.1	-120.9	-130.4	-117.3	-119.6
1.00M	-141.6	-141.9	-182.1	-168.6	-153.2

8.2 DOCUMENTACION PARA ENVIAR A FABRICAR PCB

La documentación que necesitan estas empresas para poder fabricar el circuito impreso es la siguiente:

-Archivos GERBER (Generados en PCAD durante el diseño del layout de PCB).

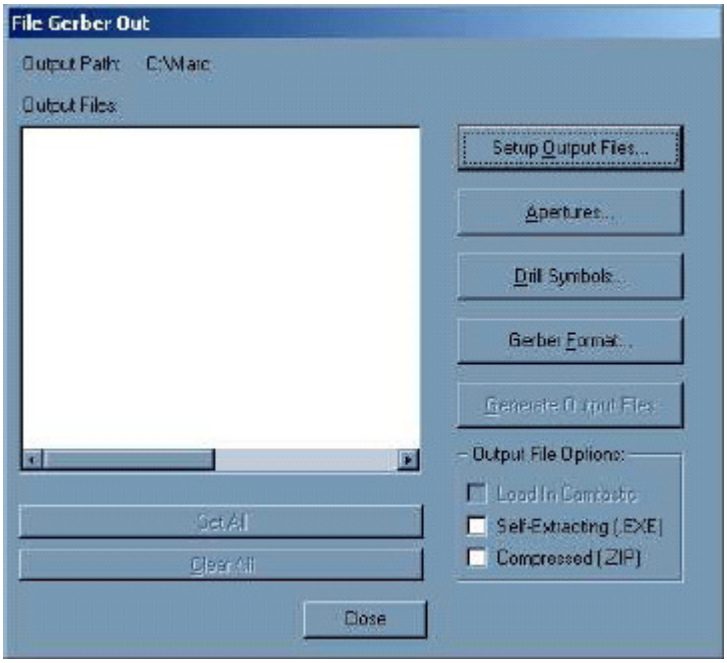
-Cada GERBER debe generarse para cada capa que forma el circuito impreso: capas internas, externas, máscaras, líneas de corte, etc.

-La resolución del GERBER debe ser de 5 cifras con relación 2:5 ó 3:5 para facilitar el uso estandarizado de la maquinaria, si no fuera el caso el coste de fabricación de la placa de circuito impreso sería mayor.

Para exportar los archivos GERBER con PCAD realizar lo siguiente:

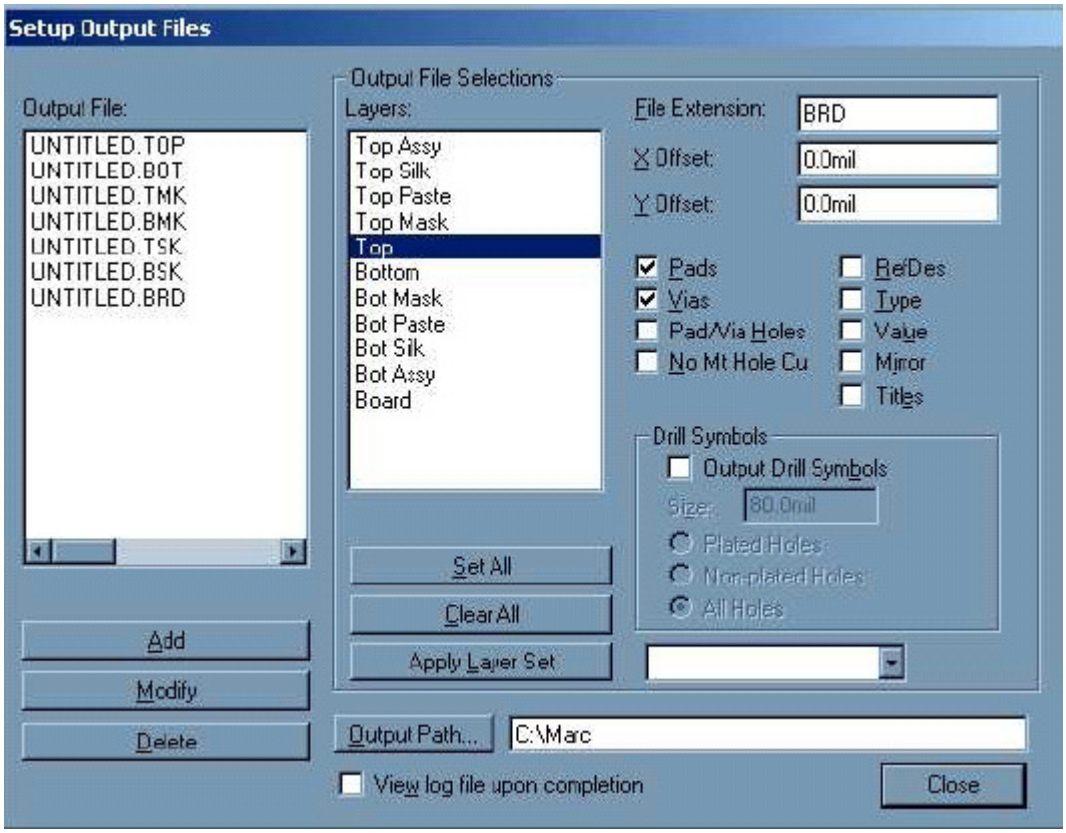
(Información facilitada por la empresa 2CI CIRCUITOS IMPRESOS)

Seleccionar **File** / **Export** / **Gerber**. Para generar los archivos gerber habrá que seguir paso a paso a través de los botones que se encuentran en el lado derecho de la ventana de salida de Gerbers.



Primero pulsaremos sobre **Setup Output Files.** Todas las capas del diseño del circuito están listadas en el centro de la ventana. Aquí se deben añadir todas las capas que se desea exportar. Tanto para exportar las caras de pistas como las caras de máscara de soldaduras, deberemos marcar las casillas **Pads** y **Vías**, y desmarcar todas las

demás. Para exportar las capas de serigrafía deberemos tener marcada la casilla **RefDes**. Iremos añadiendo capa a capa indicando la extensión que le queramos poner a cada una y pulsando el botón de **Add** situado en la izquierda de la ventana. No olvidar indicar la ruta donde queremos que se nos guarden los gerbers que exportemos en **Output Path**.

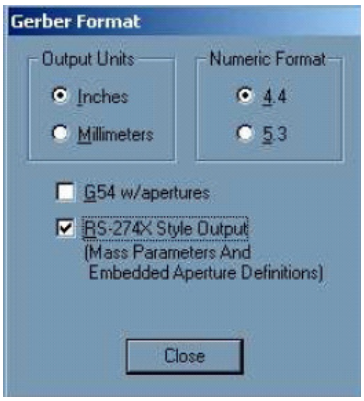


Cuando hayamos terminado se tendrá que cerrar la ventana con el botón **Close** situado en la esquina inferior derecha de la ventana.

Seguidamente pulsaremos en el botón **Apertures.** Aquí sencillamente pulsaremos en el botón **Auto** y nos aseguraremos que tenemos marcada la casilla de **Clear Current Apertures** y tenemos desmarcada la casilla de **Pad/Via Holes**. En **Draw aperture size** pondremos 10 mils. Finalmente cerraremos la ventana con el botón **Close**.

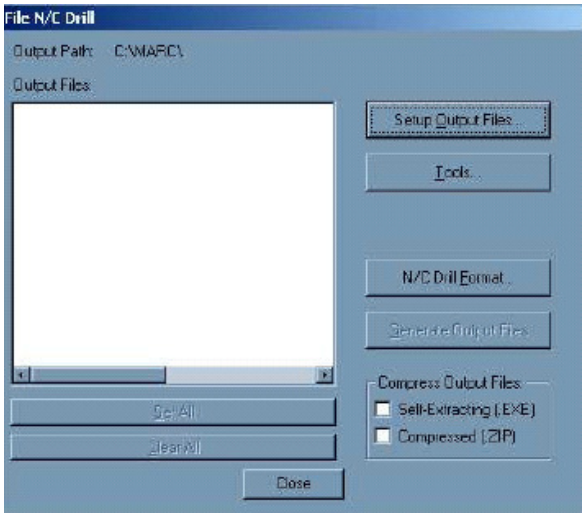
El siguiente botón que nos encontramos es el de **Drill Symbols.** Esto produce una capa conocida como guía de taladrado. Esta capa no se usará para la fabricación del circuito, por lo tanto, podemos saltarnos esta salida y pasar directamente al siguiente paso.

A continuación pulsamos sobre el botón **Gerber Format.** Esto sirve para configurar el formato de las coordenadas X-Y dentro del gerber. Marcaremos las **Output Units** como **Inches** y en **Numeric Format** marcaremos **4.4**. Deberemos tener activadas las casillas **G54 w/apertures** y **Include aperture definitions (as RS-274x mass parameters)**. Luego cerraremos la ventana pulsando sobre el botón **Close**. Ahora ya podemos generar los archivos gerber pulsando sobre el botón **Generate Output Files**.



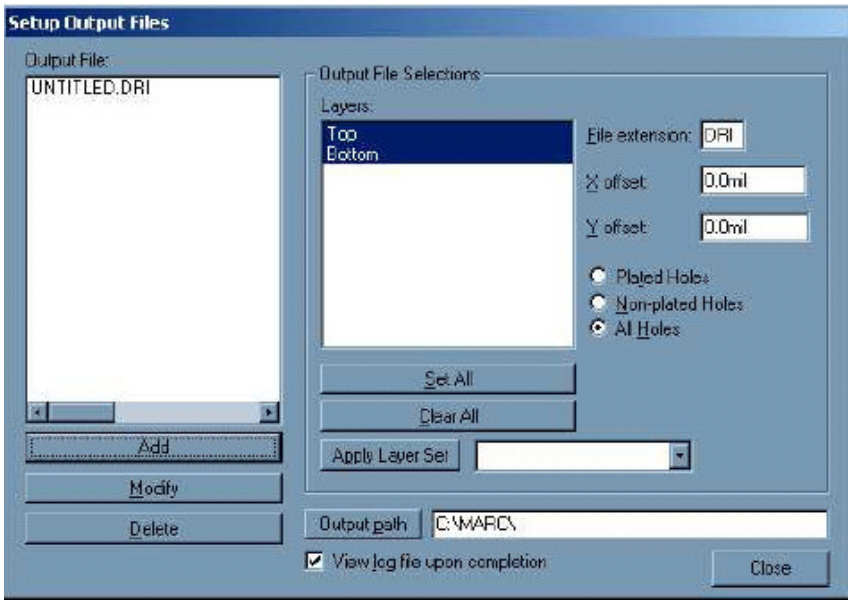
-Archivos de control numérico. Usado para el posicionamiento del taladrado de la placa de circuito impreso. Para exportar los archivos de TALADRADO con PCAD realizar lo siguiente:

Seleccionar **File** / **NC Drill**. Y pulsar sobre el botón **Setup Output Files**.



Pulsar sobre el botón **Set All**, marcar la casilla **All Holes**, poner una extensión para el archivo en **File Extension** e indicar la ruta donde queremos que se nos guarde el archivo de control numérico de taladrado en **Output Path**. Finalmente pulsaremos sobre el botón **Add** en la izquierda de la ventana y cerraremos con **Close**. A

continuación pulsaremos en el botón **Tools**; dentro pulsaremos sobre el botón **Auto** y luego cerraremos con **Close**.



Luego pulsaremos sobre **N/C Drill Format** donde marcaremos **Inches** en **Ouput Units**, **ASCII None** en **Output Code Type**, y **None** en **Zero Supression**; cerraremos con **Close**. Finalmente para generar los archivos pulsaremos sobre **Generate Output Files** y Cerraremos con **Close**. No olvidar comprobar el archivo **Log** para verificar que no haya errores en la exportación.

8.3 MANUALES TÉCNICOS

A continuación se incluye la lista de manuales técnicos o '*datasheets*' de los componentes utilizados para el diseño del circuito electrónico.

COMPONENTE	FABRICANTE	FUNCIÓN
OP27GS	ANALOG DEVICES	OPERACIONAL
ADF4002	ANALOG DEVICES	SINTETIZADOR PLL
ADF4106	ANALOG DEVICES	SINTETIZADOR PLL
VTXO505R-30	RAKON	OSCILADOR CRISTAL
TPS5450DDA	TEXAS INSTRUMENTS	CONVERTIDOR DC/DC
TL317CD	TEXAS INSTRUMENTS	CONVERTIDOR DC/DC
LP38693SD 3,3	NATIONAL SEMICONDUCTOR	CONVERTIDOR DC/DC
LP38693SD 5,0	NATIONAL SEMICONDUCTOR	CONVERTIDOR DC/DC
RQRE-1000-2000	RALTRON	OSCILADOR
RQRE-500-1000	RALTRON	OSCILADOR
THS3202D	TEXAS INSTRUMENTS	OPERACIONAL

ANALOG DEVICES

Low Noise, Precision Operational Amplifier

OP-27

FEATURES

- **Low Noise** ..... **80nV$_{p-p}$ (0.1Hz to 10Hz)**
  ..... **3nV/$\sqrt{Hz}$**
- **Low Drift** ..... **0.2μV/°C**
- **High Speed** ..... **2.8V/μs Slew Rate**
  ..... **8MHz Gain Bandwidth**
- **Low V_{OS}** **10μV**
- **Excellent CMRR** ..... **126dB at V_{CM} of ±11V**
- **High Open-Loop Gain** ..... **1.8 Million**
- **Fits 725, OP-07, OP-05, AD510, AD517, 5534A sockets**
- **Available in Die Form**

ORDERING INFORMATION †

T_A = +25°C V_{OS} MAX (µV)	PACKAGE TO-99	CERDIP 8-PIN	PLASTIC 8-PIN	LCC 20-CONTACT	OPERATING TEMPERATURE RANGE
25	OP27AJ*	OP27AZ*	–	–	MIL
25	OP27EJ	OP27EZ	OP27EP	–	IND/COM
60	OP27BJ*	OP27BZ*	–	OP27BR/883	MIL
60	OP27FJ	OP27FZ	OP27FP	–	IND/COM
100	OP27CJ	OP27CZ	–	–	MIL
100	OP27GJ	OP27GZ	OP27GP	–	XIND
100	–	–	OP27GS††	–	XIND

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† Burn-in is available on commercial and industrial temperature range parts in CerDIP, plastic DIP, and TO-can packages.

†† For availability and burn-in information on SO and PLCC packages, contact your local sales office.

GENERAL DESCRIPTION

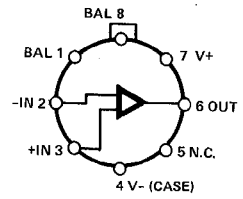
The OP-27 precision operational amplifier combines the low offset and drift of the OP-07 with both high speed and low noise. Offsets down to 25μV and drift of 0.6μV/°C maximum make the OP-27 ideal for precision instrumentation applications. Exceptionally low noise, e_n = 3.5nV/$\sqrt{Hz}$, at 10Hz, a low 1/f noise corner frequency of 2.7Hz, and high gain (1.8 million), allow accurate high-gain amplification of low-level signals. A gain-bandwidth product of 8MHz and a 2.8V/μsec slew rate provides excellent dynamic accuracy in high-speed data-acquisition systems.

A low input bias current of ±10nA is achieved by use of a bias-current-cancellation circuit. Over the military temperature range, this circuit typically holds I_B and I_{OS} to ±20nA and 15nA respectively.

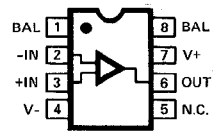
The output stage has good load driving capability. A guaranteed swing of ±10V into 600Ω and low output distortion make the OP-27 an excellent choice for professional audio applications.

PSRR and CMRR exceed 120dB. These characteristics, coupled with long-term drift of 0.2μV/month, allow the circuit designer to achieve performance levels previously attained only by discrete designs.

PIN CONNECTIONS



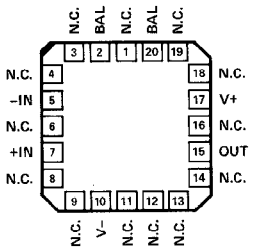
TO-99
(J-Suffix)



8-PIN HERMETIC DIP
(Z-Suffix)

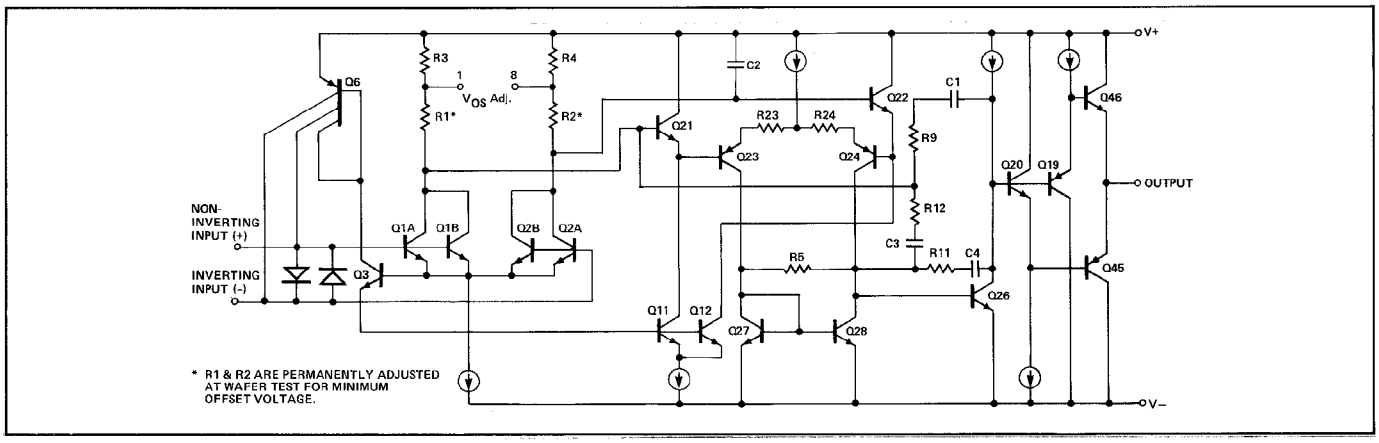
EPOXY MINI-DIP
(P-Suffix)

8-PIN SO
(S-Suffix)



OP-27BRC/883
LCC PACKAGE
(RC-Suffix)

SIMPLIFIED SCHEMATIC



OP-27

Low cost, high-volume production of OP-27 is achieved by using an on-chip zener-zap trimming network. This reliable and stable offset trimming scheme has proved its effectiveness over many years of production history.

The OP-27 provides excellent performance in low-noise high-accuracy amplification of low-level signals. Applications include stable integrators, precision summing amplifiers, precision voltage-threshold detectors, comparators, and professional audio circuits such as tape-head and microphone preamplifiers.

The OP-27 is a direct replacement for 725, OP-06, OP-07 and OP-05 amplifiers; 741 types may be directly replaced by removing the 741's nulling potentiometer.

ABSOLUTE MAXIMUM RATINGS (Note 4)

Supply Voltage ..... ±22V
Input Voltage (Note 1) ..... ±22V
Output Short-Circuit Duration ..... Indefinite
Differential Input Voltage (Note 2) ..... ±0.7V
Differential Input Current (Note 2) ..... ±25mA
Storage Temperature Range ..... –65°C to +150°C

Operating Temperature Range
OP-27A, OP-27B, OP-27C (J, Z, RC)..... –55°C to +125°C
OP-27E, OP-27F (J, Z) ..... –25°C to +85°C
OP-27E, OP-27F (P) ..... 0°C to +70°C
OP-27G (P, S, J, Z) ..... –40°C to +85°C
Lead Temperature Range (Soldering, 60 sec) ..... 300°C
Junction Temperature ..... –65°C to +150°C

PACKAGE TYPE	Θ_{jA} (Note 3)	Θ_{jC}	UNITS
TO-99 (J)	150	18	°C/W
8-Pin Hermetic DIP (Z)	148	16	°C/W
8-Pin Plastic DIP (P)	103	43	°C/W
20-Contact LCC (RC)	98	38	°C/W
8-Pin SO (S)	158	43	°C/W

NOTES:
1. For supply voltages less than ±22V, the absolute maximum input voltage is equal to the supply voltage.
2. The OP-27's inputs are protected by back-to-back diodes. Current limiting resistors are not used in order to achieve low noise. If differential input voltage exceeds ±0.7V, the input current should be limited to 25mA.
3. Θ_{jA} is specified for worst case mounting conditions, i.e., Θ_{jA} is specified for device in socket for TO, CerDIP, P-DIP, and LCC packages; Θ_{jA} is specified for device soldered to printed circuit board for SO package.
4. Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $T_A = 25°C$, unless otherwise noted.

			OP-27A/E			OP-27B/F			OP-27C/G			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Input Offset Voltage	V_{OS}	(Note 1)	—	10	25	—	20	60	—	30	100	µV
Long-Term V_{OS} Stability	V_{OS}/Time	(Notes 2, 3)	—	0.2	1.0	—	0.3	1.5	—	0.4	2.0	µV/Mo
Input Offset Current	I_{OS}		—	7	35	—	9	50	—	12	75	nA
Input Bias Current	I_B		—	±10	±40	—	±12	±55	—	±15	±80	nA
Input Noise Voltage	e_{np-p}	0.1Hz to 10Hz (Notes 3, 5)	—	0.08	0.18	—	0.08	0.18	—	0.09	0.25	µVp-p
Input Noise Voltage Density	e_n	f_O = 10Hz (Note 3)	—	3.5	5.5	—	3.5	5.5	—	3.8	8.0	$nV/\sqrt{Hz}$
		f_O = 30Hz (Note 3)	—	3.1	4.5	—	3.1	4.5	—	3.3	5.6	
		f_O = 1000Hz (Note 3)	—	3.0	3.8	—	3.0	3.8	—	3.2	4.5	
Input Noise Current Density	i_n	f_O = 10Hz (Notes 3,6)	—	1.7	4.0	—	1.7	4.0	—	1.7	—	$pA/\sqrt{Hz}$
		f_O = 30Hz (Notes 3, 6)	—	1.0	2.3	—	1.0	2.3	—	1.0	—	
		f_O = 1000Hz (Notes 3, 6)	—	0.4	0.6	—	0.4	0.6	—	0.4	0.6	
Input Resistance — Differential-Mode	R_{IN}	(Note 7)	1.3	6	—	0.94	5	—	0.7	4	—	MΩ
Input Resistance — Common-Mode	R_{INCM}		—	3	—	—	2.5	—	—	2	—	GΩ
Input Voltage Range	IVR		±11.0	±12.3	—	±11.0	±12.3	—	±11.0	±12.3	—	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 11V$	114	126	—	106	123	—	100	120	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 4V$ to $\pm 18V$	—	1	10	—	1	10	—	2	20	µV/V
Large-Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$, $V_O = \pm 10V$	1000	1800	—	1000	1800	—	700	1500	—	V/mV
		$R_L \geq 600\Omega$, $V_O = \pm 10V$	800	1500	—	800	1500	—	600	1500	—	
Output Voltage Swing	V_O	$R_L \geq 2k\Omega$	±12.0	±13.8	—	±12.0	±13.8	—	±11.5	±13.5	—	V
		$R_L \geq 600\Omega$	±10.0	±11.5	—	±10.0	±11.5	—	±10.0	±11.5	—	
Slew Rate	SR	$R_L \geq 2k\Omega$ (Note 4)	1.7	2.8	—	1.7	2.8	—	1.7	2.8	—	V/µs

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $T_A = 25°C$, unless otherwise noted. (Continued)

PARAMETER	SYMBOL	CONDITIONS	OP-27A/E MIN	OP-27A/E TYP	OP-27A/E MAX	OP-27B/F MIN	OP-27B/F TYP	OP-27B/F MAX	OP-27C/G MIN	OP-27C/G TYP	OP-27C/G MAX	UNITS
Gain Bandwidth Prod.	GBW	(Note 4)	5.0	8.0	—	5.0	8.0	—	5.0	8.0	—	MHz
Open-Loop Output Resistance	R_O	$V_O = 0$, $I_O = 0$	—	70	—	—	70	—	—	70	—	Ω
Power Consumption	P_d	V_O	—	90	140	—	90	140	—	100	170	mW
Offset Adjustment Range		$R_P = 10k\Omega$	—	±4.0	—	—	±4.0	—	—	±4.0	—	mV

NOTES:
1. Input offset voltage measurements are performed ~ 0.5 seconds after application of power. A/E grades guaranteed fully warmed-up.
2. Long-term input offset voltage stability refers to the average trend line of V_{OS} vs. Time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in V_{OS} during the first 30 days are typically 2.5μV — refer to typical performance curve.
3. Sample tested.
4. Guaranteed by design.
5. See test circuit and frequency response curve for 0.1Hz to 10Hz tester.
6. See test circuit for current noise measurement.
7. Guaranteed by input bias current.

ELECTRICAL CHARACTERISTICS for $V_S = \pm 15V$, $-55°C \le T_A \le +125°C$, unless otherwise noted.

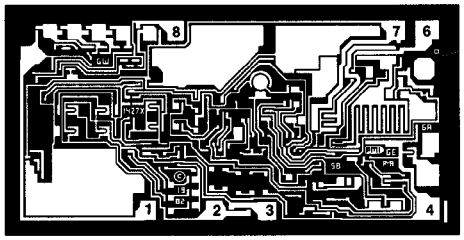
PARAMETER	SYMBOL	CONDITIONS	OP-27A MIN	OP-27A TYP	OP-27A MAX	OP-27B MIN	OP-27B TYP	OP-27B MAX	OP-27C MIN	OP-27C TYP	OP-27C MAX	UNITS
Input Offset Voltage	V_{OS}	(Note 1)	—	30	60	—	50	200	—	70	300	μV
Average Input Offset Drift	TCV_{OS} TCV_{OSn}	(Note 2) (Note 3)	—	0.2	0.6	—	0.3	1.3	—	0.4	1.8	μV/°C
Input Offset Current	I_{OS}		—	15	50	—	22	85	—	30	135	nA
Input Bias Current	I_B		—	±20	±60	—	±28	±95	—	±35	±150	nA
Input Voltage Range	IVR		±10.3	±11.5	—	±10.3	±11.5	—	±10.2	±11.5	—	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 10V$	108	122	—	100	119	—	94	116	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 4.5V$ to $\pm 18V$	—	2	16	—	2	20	—	4	51	μV/V
Large-Signal Voltage Gain	A_{VO}	$R_L \ge 2k\Omega$, $V_O = \pm 10V$	600	1200	—	500	1000	—	300	800	—	V/mV
Output Voltage Swing	V_O	$R_L \ge 2k\Omega$	±11.5	±13.5	—	±11.0	±13.2	—	±10.5	±13.0	—	V

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $-25°C \le T_A \le +85°C$ for OP-27J and OP-27Z, $0°C \le T_A \le +70°C$ for OP-27EP, FP and $-40°C \le T_A \le +85°C$ for OP-27GP, GS, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-27E MIN	OP-27E TYP	OP-27E MAX	OP-27F MIN	OP-27F TYP	OP-27F MAX	OP-27G MIN	OP-27G TYP	OP-27G MAX	UNITS
Input Offset Voltage	V_{OS}		—	20	50	—	40	140	—	55	220	μV
Average Input Offset Drift	TCV_{OS} TCV_{OSn}	(Note 2) (Note 3)	—	0.2	0.6	—	0.3	1.3	—	0.4	1.8	μV/°C
Input Offset Current	I_{OS}		—	10	50	—	14	85	—	20	135	nA
Input Bias Current	I_B		—	±14	±60	—	±18	±95	—	±25	±150	nA
Input Voltage Range	IVR		±10.5	±11.8	—	±10.5	±11.8	—	±10.5	±11.8	—	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 10V$	110	124	—	102	121	—	96	118	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 4.5V$ to $\pm 18V$	—	2	15	—	2	16	—	2	32	μV/V
Large-Signal Voltage Gain	A_{VO}	$R_L \ge 2k\Omega$, $V_O = \pm 10V$	750	1500	—	700	1300	—	450	1000	—	V/mV
Output Voltage Swing	V_O	$R_L \ge 2k\Omega$	±11.7	±13.6	—	±11.4	±13.5	—	±11.0	±13.3	—	V

NOTES:
1. Input offset voltage measurements are performed by automated test equipment approximately 0.5 seconds after application of power. A/E grades guaranteed fully warmed-up.
2. The TCV_{OS} performance is within the specifications unnulled or when nulled with R_P = 8kΩ to 20kΩ. TCV_{OS} is 100% tested for A/E grades, sample tested for B/C/F/G grades.
3. Guaranteed by design.

DICE CHARACTERISTICS



DIE SIZE 0.109 × 0.055 inch, 5995 sq. mils
(2.77 × 1.40mm, 3.88 sq. mm)

1. NULL
2. (–) INPUT
3. (+) INPUT
4. V–
6. OUTPUT
7. V+
8. NULL

WAFER TEST LIMITS at $V_S = \pm 15V$, $T_A = 25°C$ for OP-27N, OP-27G, and OP-27GR devices; $T_A = 125°C$ for OP-27NT and OP-27GT devices, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-27NT LIMIT	OP-27N LIMIT	OP-27GT LIMIT	OP-27G LIMIT	OP-27GR LIMIT	UNITS
Input Offset Voltage	V_{OS}	(Note 1)	60	35	200	60	100	μV MAX
Input Offset Current	I_{OS}		50	35	85	50	75	nA MAX
Input Bias Current	I_B		±60	±40	±95	±55	±80	nA MAX
Input Voltage Range	IVR		±10.3	±11	±10.3	±11	±11	V MIN
Common-Mode Rejection Ratio	CMRR	V_{CM} = IVR	108	114	100	106	100	dB MIN
Power Supply Rejection Ratio	PSRR	$V_S = \pm 4V$ to $\pm 18V$	—	10	—	10	20	μV/V MAX
Large-Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$, $V_O = \pm 10V$ $R_L \geq 600\Omega$, $V_O = \pm 10V$	600 —	1000 800	500 —	1000 800	700 600	V/mV MIN
Output Voltage Swing	V_O	$R_L \geq 2k\Omega$ $R_L \geq 600\Omega$	±11.5 —	±12.0 ±10.0	±11.0 —	±12.0 ±10.0	±11.5 ±10.0	V MIN
Power Consumption	P_d	$V_O = 0$	—	140	—	140	170	mW MAX

NOTE:
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

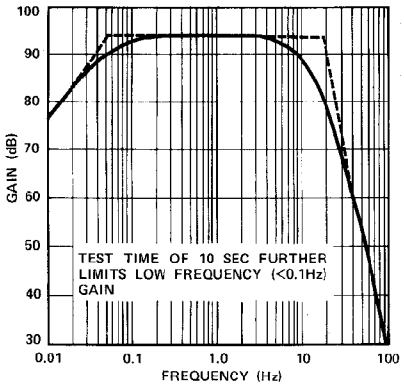
TYPICAL ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $T_A = +25°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-27N TYPICAL	OP-27G TYPICAL	OP-27GR TYPICAL	UNITS
Average Input Offset Voltage Drift	TCV_{OS} or TCV_{OSn}	Nulled or Unnulled $R_P = 8k\Omega$ to $20k\Omega$	0.2	0.3	0.4	μV/°C
Average Input Offset Current Drift	TCI_{OS}		80	130	180	pA/°C
Average Input Bias Current Drift	TCI_B		100	160	200	pA/°C
Input Noise Voltage Density	e_n	$f_O = 10Hz$ $f_O = 30Hz$ $f_O = 1000Hz$	3.5 3.1 3.0	3.5 3.1 3.0	3.8 3.3 3.2	$nV/\sqrt{Hz}$
Input Noise Current Density	i_n	$f_O = 10Hz$ $f_O = 30Hz$ $f_O = 1000Hz$	1.7 1.0 0.4	1.7 1.0 0.4	1.7 1.0 0.4	$pA/\sqrt{Hz}$
Input Noise Voltage	e_{np-p}	0.1Hz to 10Hz	0.08	0.08	0.09	μVp-p
Slew Rate	SR	$R_L \geq 2k\Omega$	2.8	2.8	2.8	V/μs
Gain Bandwidth Product	GBW		8	8	8	MHz

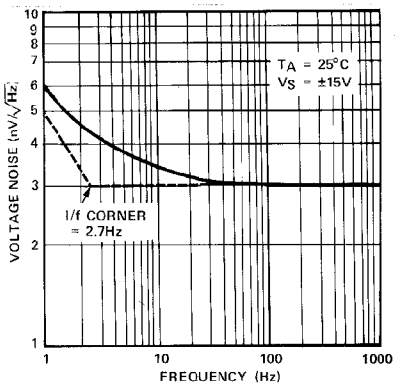
NOTE:
1. Input offset voltage measurements are performed by automated test equipment approximately 0.5 seconds after application of power.

TYPICAL PERFORMANCE CHARACTERISTICS

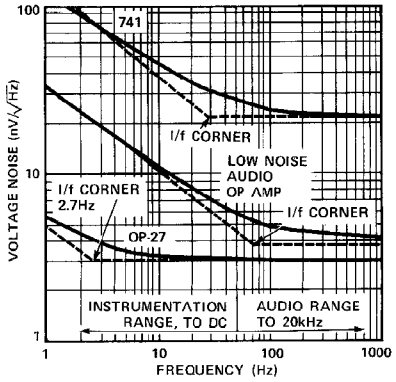
0.1Hz TO 10Hz$_{p-p}$ NOISE TESTER FREQUENCY RESPONSE



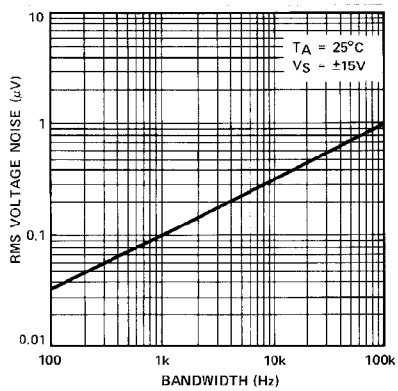
VOLTAGE NOISE DENSITY vs FREQUENCY



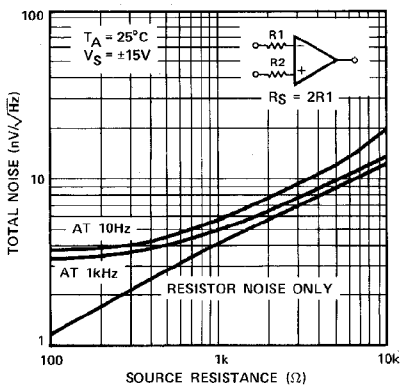
A COMPARISON OF OP AMP VOLTAGE NOISE SPECTRA



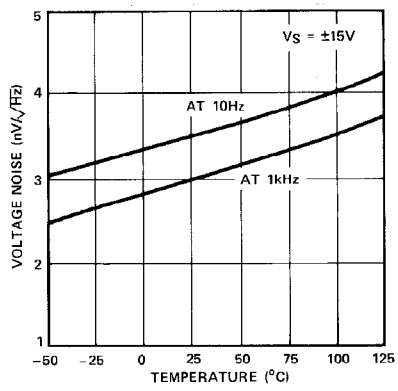
INPUT WIDEBAND VOLTAGE NOISE vs BANDWIDTH (0.1Hz TO FREQUENCY INDICATED)



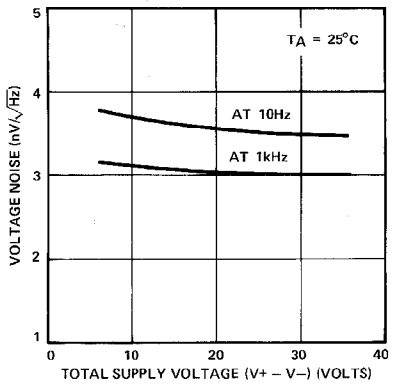
TOTAL NOISE vs SOURCE RESISTANCE



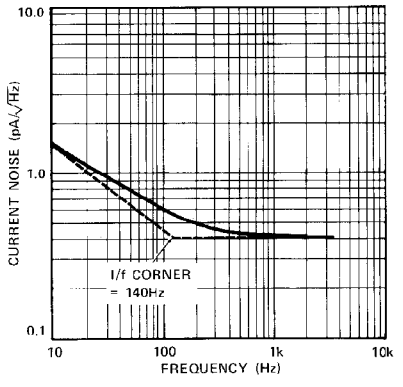
VOLTAGE NOISE DENSITY vs TEMPERATURE



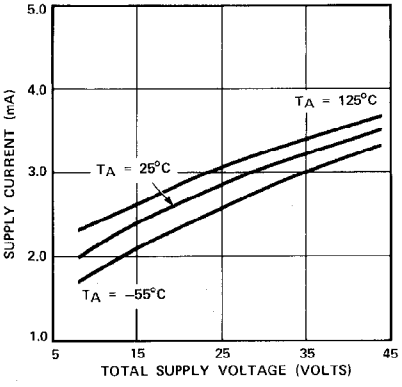
VOLTAGE NOISE DENSITY vs SUPPLY VOLTAGE



CURRENT NOISE DENSITY vs FREQUENCY

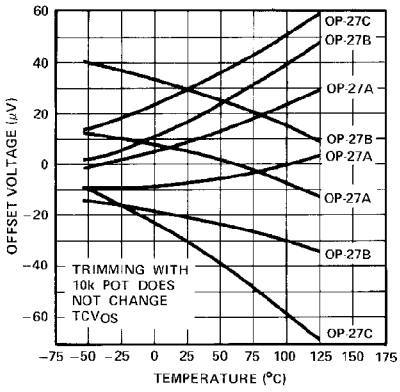


SUPPLY CURRENT vs SUPPLY VOLTAGE

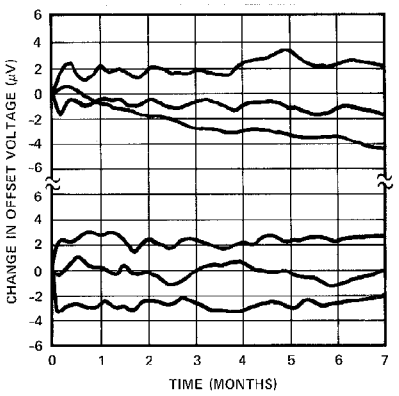


TYPICAL PERFORMANCE CHARACTERISTICS

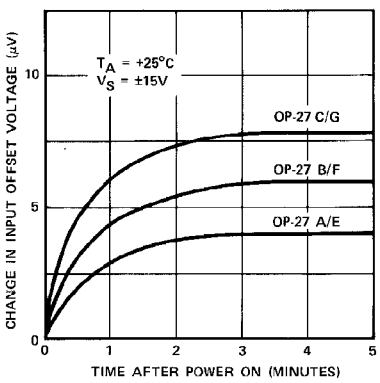
OFFSET VOLTAGE DRIFT OF EIGHT REPRESENTATIVE UNITS vs TEMPERATURE



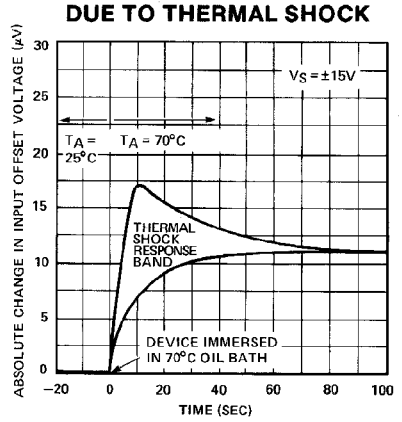
LONG-TERM OFFSET VOLTAGE DRIFT OF SIX REPRESENTATIVE UNITS



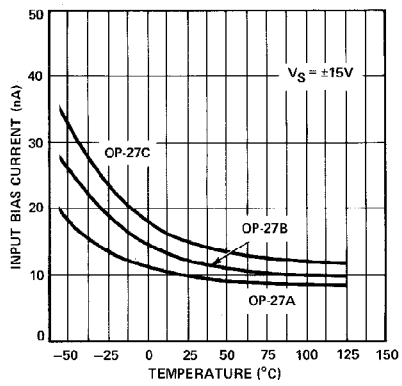
WARM-UP OFFSET VOLTAGE DRIFT



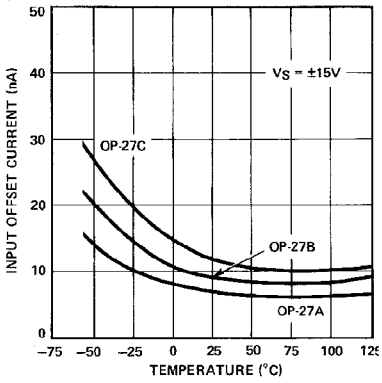
OFFSET VOLTAGE CHANGE DUE TO THERMAL SHOCK



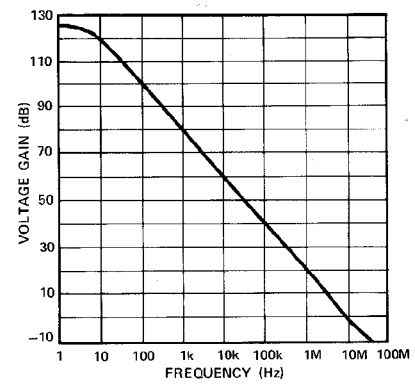
INPUT BIAS CURRENT vs TEMPERATURE



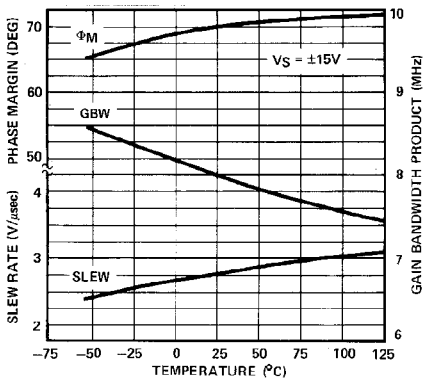
INPUT OFFSET CURRENT vs TEMPERATURE



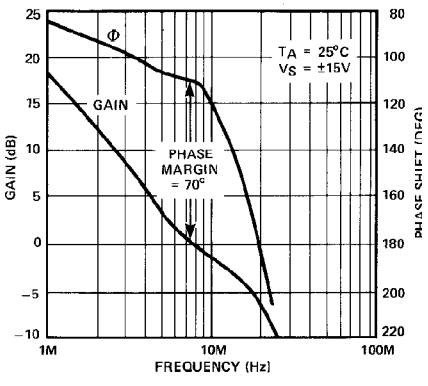
OPEN-LOOP GAIN vs FREQUENCY



SLEW RATE, GAIN-BANDWIDTH PRODUCT, PHASE MARGIN vs TEMPERATURE

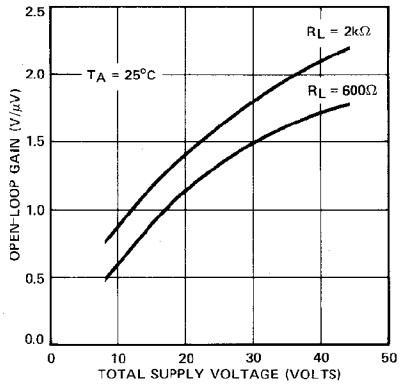


GAIN, PHASE SHIFT vs FREQUENCY

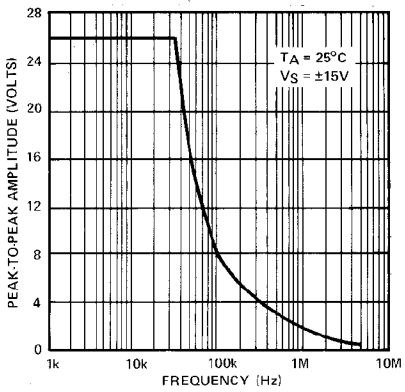


TYPICAL PERFORMANCE CHARACTERISTICS

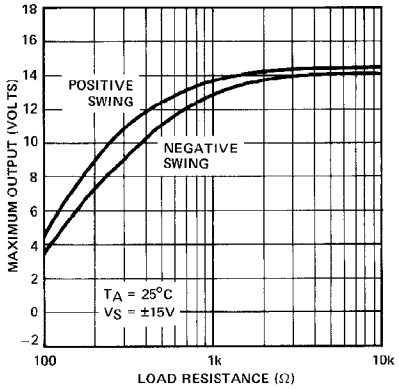
OPEN-LOOP VOLTAGE GAIN vs SUPPLY VOLTAGE



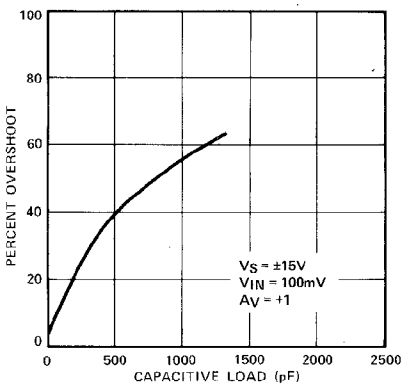
MAXIMUM OUTPUT SWING vs FREQUENCY



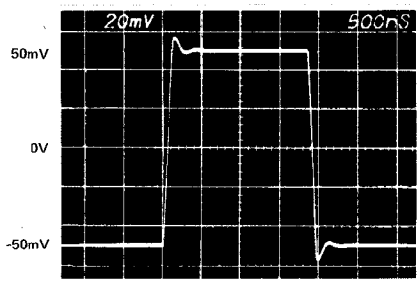
MAXIMUM OUTPUT VOLTAGE vs LOAD RESISTANCE



SMALL-SIGNAL OVERSHOOT vs CAPACITIVE LOAD

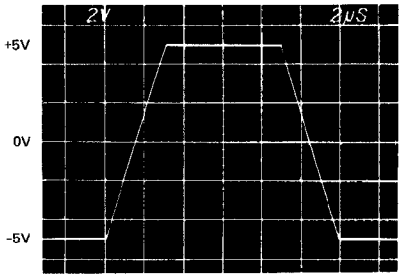


SMALL-SIGNAL TRANSIENT RESPONSE



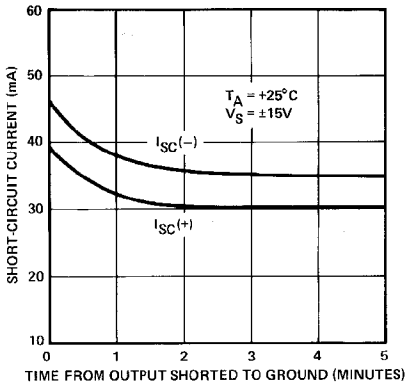
A_{VCL} = +1, C_L = 15pF
V_S = ±15V
T_A = 25°C

LARGE-SIGNAL TRANSIENT RESPONSE

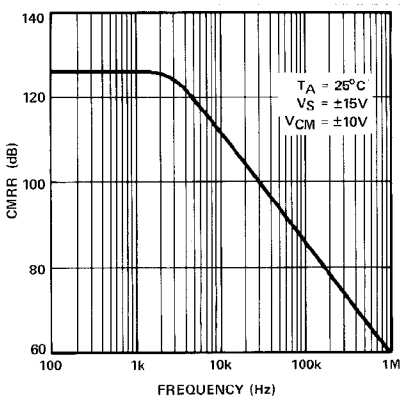


A_{VCL} = +1
V_S = ±15V
T_A = 25°C

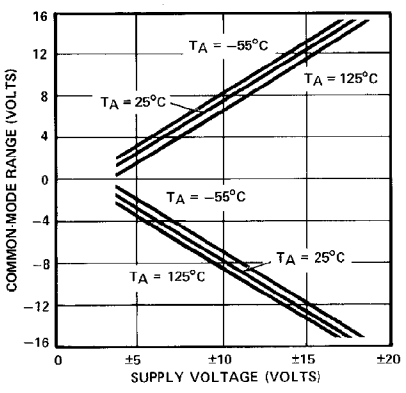
SHORT-CIRCUIT CURRENT vs TIME



CMRR vs FREQUENCY

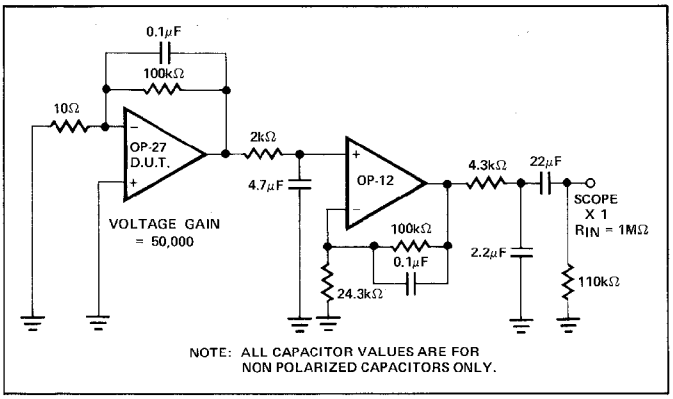


COMMON-MODE INPUT RANGE vs SUPPLY VOLTAGE

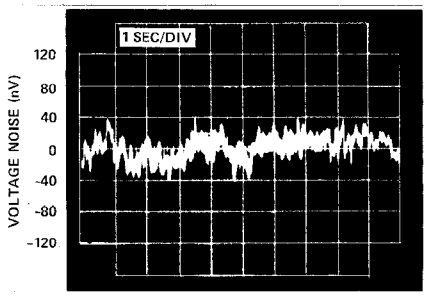


TYPICAL PERFORMANCE CHARACTERISTICS

VOLTAGE NOISE TEST CIRCUIT (0.1Hz-TO-10Hz)



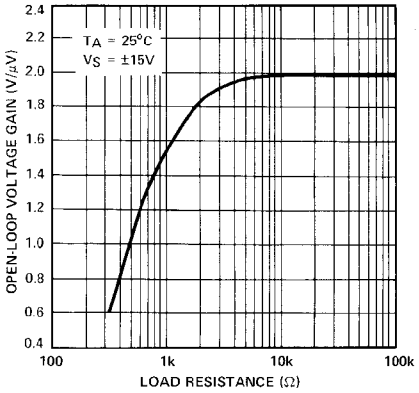
LOW-FREQUENCY NOISE



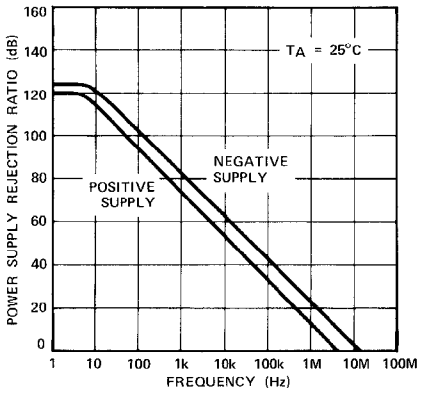
0.1Hz TO 10Hz PEAK-TO-PEAK NOISE

NOTE:
Observation time limited to 10 seconds.

OPEN-LOOP VOLTAGE GAIN vs LOAD RESISTANCE



PSRR vs FREQUENCY



APPLICATIONS INFORMATION

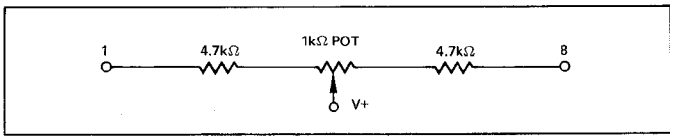
OP-27 Series units may be inserted directly into 725, OP-06, OP-07 and OP-05 sockets with or without removal of external compensation or nulling components. Additionally, the OP-27 may be fitted to unnulled 741-type sockets; however, if conventional 741 nulling circuitry is in use, it should be modified or removed to ensure correct OP-27 operation. OP-27 offset voltage may be nulled to zero (or other desired setting) using a potentiometer (see Offset Nulling Circuit).

The OP-27 provides stable operation with load capacitances of up to 2000pF and ± 10V swings; larger capacitances should be decoupled with a 50Ω resistor inside the feedback loop. The OP-27 is unity-gain stable.

Thermoelectric voltages generated by dissimilar metals at the input terminal contacts can degrade the drift performance. Best operation will be obtained when both input contacts are maintained at the same temperature.

OFFSET VOLTAGE ADJUSTMENT

The input offset voltage of the OP-27 is trimmed at wafer level. However, if further adjustment of V_{OS} is necessary, a 10kΩ trim potentiometer may be used. TCV_{OS} is not degraded (see Offset Nulling Circuit). Other potentiometer values from 1kΩ to 1MΩ can be used with a slight degradation (0.1 to 0.2μV/° C) of TCV_{OS}. Trimming to a value other than zero creates a drift of approximately (V_{OS}/300) μV/° C. For example, the change in TCV_{OS} will be 0.33μV/° C if V_{OS} is adjusted to 100μV. The offset-voltage adjustment range with a 10kΩ potentiometer is ±4mV. If smaller adjustment range is required, the nulling sensitivity can be reduced by using a smaller pot in conjuction with fixed resistors. For example, the network below will have a ±280μV adjustment range.



NOISE MEASUREMENTS

To measure the 80nV peak-to-peak noise specification of the OP-27 in the 0.1Hz to 10Hz range, the following precautions must be observed:

(1) The device has to be warmed-up for at least five minutes. As shown in the warm-up drift curve, the offset voltage

typically changes 4μV due to increasing chip temperature after power-up. In the 10-second measurement interval, these temperature-induced effects can exceed tens-of-nanovolts.

(2) For similar reasons, the device has to be well-shielded from air currents. Shielding minimizes thermocouple effects.

(3) Sudden motion in the vicinity of the device can also "feed-through" to increase the observed noise.

(4) The test time to measure 0.1Hz-to-10Hz noise should not exceed 10 seconds. As shown in the noise-tester frequency-response curve, the 0.1Hz corner is defined by only one zero. The test time of 10 seconds acts as an additional zero to eliminate noise contributions from the frequency band below 0.1Hz.

(5) A noise-voltage-density test is recommended when measuring noise on a large number of units. A 10Hz noise-voltage-density measurement will correlate well with a 0.1Hz-to-10Hz peak-to-peak noise reading, since both results are determined by the white noise and the location of the 1/f corner frequency.

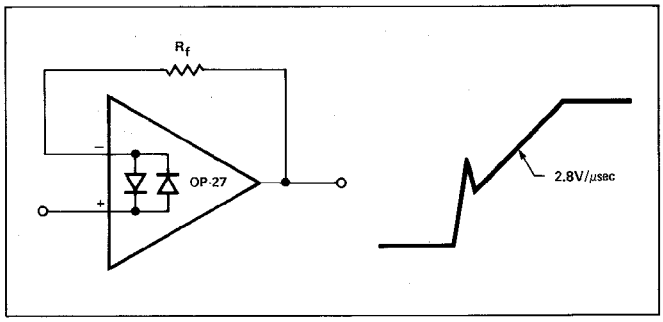
UNITY-GAIN BUFFER APPLICATIONS

When $R_f \leq 100\Omega$ and the input is driven with a fast, large signal pulse (>1V), the output waveform will look as shown in the pulsed operation diagram below.

During the fast feedthrough-like portion of the output, the input protection diodes effectively short the output to the input and a current, limited only by the output short-circuit protection, will be drawn by the signal generator. With $R_f \geq 500\Omega$, the output is capable of handling the current requirements ($I_L \leq 20$mA at 10V); the amplifier will stay in its active mode and a smooth transition will occur.

When $R_f > 2k\Omega$, a pole will be created with R_f and the amplifier's input capacitance (8pF) that creates additional phase shift and reduces phase margin. A small capacitor (20 to 50pF) in parallel with R_f will eliminate this problem.

PULSED OPERATION



COMMENTS ON NOISE

The OP-27 is a very low-noise monolithic op amp. The outstanding input voltage noise characteristics of the OP-27 are achieved mainly by operating the input stage at a high quiescent current. The input bias and offset currents, which would normally increase, are held to reasonable values by the input-bias-current cancellation circuit. The OP-27A/E has I_B and I_{OS} of only ±40nA and 35nA respectively at 25° C. This is particularly important when the input has a high source-resistance. In addition, many audio amplifier designers prefer to use direct coupling. The high I_B, V_{OS}, TCV_{OS} of previous designs have made direct coupling difficult, if not impossible, to use.

Voltage noise is inversely proportional to the square-root of bias current, but current noise is proportional to the square-root of bias current. The OP-27's noise advantage disappears when high source-resistors are used. Figures 1, 2, and 3 compare OP-27 observed total noise with the noise performance of other devices in different circuit applications.

Total noise = $[(\text{Voltage noise})^2 + (\text{current noise} \times R_S)^2 + (\text{resistor noise})^2]^{1/2}$

Figure 1 shows noise-versus-source-resistance at 1000Hz. The same plot applies to wideband noise. To use this plot, just multiply the vertical scale by the square-root of the bandwidth.

NOISE vs SOURCE RESISTANCE (INCLUDING RESISTOR NOISE) AT 1000Hz.

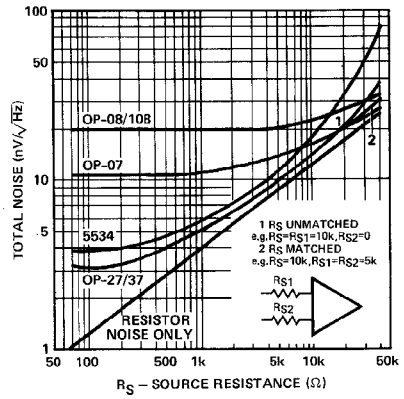


Figure 1

At $R_S < 1k\Omega$, the OP-27's low voltage noise is maintained. With $R_S > 1k\Omega$, total noise increases, but is dominated by the resistor noise rather than current or voltage noise. It is only beyond R_S of 20kΩ that current noise starts to dominate. The argument can be made that current noise is not important for applications with low-to-moderate source resistances. The crossover between the OP-27 and OP-07 and OP-08 noise occurs in the 15-to-40kΩ region.

Figure 2 shows the 0.1Hz-to-10Hz peak-to-peak noise. Here the picture is less favorable; resistor noise is negligible, current noise becomes important because it is inversely proportional to the square-root of frequency. The crossover with the OP-07 occurs in the 3-to-5kΩ range depending on whether balanced or unbalanced source resistors are used (at 3kΩ the I_B, I_{OS} error also can be three times the V_{OS} spec.).

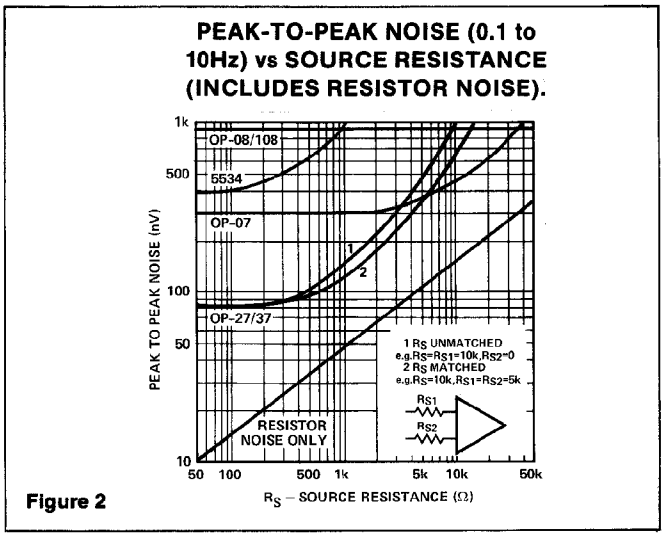


Figure 2

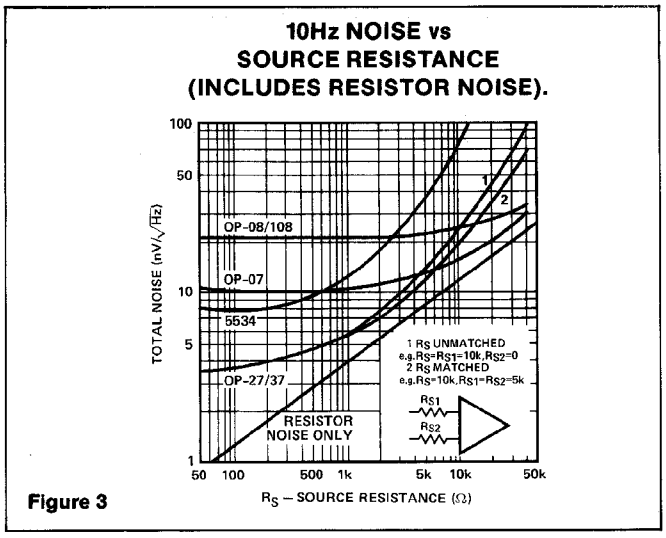


Figure 3

Therefore, for low-frequency applications, the OP-07 is better than the OP-27/37 when $R_S > 3k\Omega$. The only exception is when gain error is important. Figure 3 illustrates the 10Hz noise. As expected, the results are between the previous two figures.

For reference, typical source resistances of some signal sources are listed in Table 1.

Table 1

DEVICE	SOURCE IMPEDANCE	COMMENTS
Strain gauge	<500Ω	Typically used in low-frequency applications.
Magnetic tapehead	<1500Ω	Low I_B very important to reduce self-magnetization problems when direct coupling is used. OP-27 I_B can be neglected.
Magnetic phonograph cartridges	<1500Ω	Similar need for low I_B in direct coupled applications. OP-27 will not introduce any self-magnetization problem.
Linear variable differential transformer	<1500Ω	Used in rugged servo-feedback applications. Bandwidth of interest is 400Hz to 5kHz.

OPEN-LOOP GAIN

FREQUENCY AT:	OP-07	OP-27	OP-37
3Hz	100dB	124dB	125dB
10Hz	100dB	120dB	125dB
30Hz	90dB	110dB	124dB

For further information regarding noise calculations, see "Minimization of Noise in Op-Amp Applications," Application Note AN-15.

AUDIO APPLICATIONS

The following applications information has been abstracted from a PMI article in the 12/20/80 issue of Electronic Design magazine and updated.

Figure 4 is an example of a phono pre-amplifier circuit using the OP-27 for A_1; R_1-R_2-C_1-C_2 form a very accurate RIAA network with standard component values. The popular method to accomplish RIAA phono equalization is to employ frequency-dependent feedback around a high-quality gain block. Properly chosen, an RC network can provide the three necessary time constants of 3180, 318, and 75μs.[1]

For initial equalization accuracy and stability, precision metal-film resistors and film capacitors of polystyrene or polypropylene are recommended since they have low voltage coefficients, dissipation factors, and dielectric absorption.[4] (High-K ceramic capacitors should be avoided here, though low-K ceramics—such as NPO types, which have excellent dissipation factors, and somewhat lower dielectric absorption—can be considered for small values.)

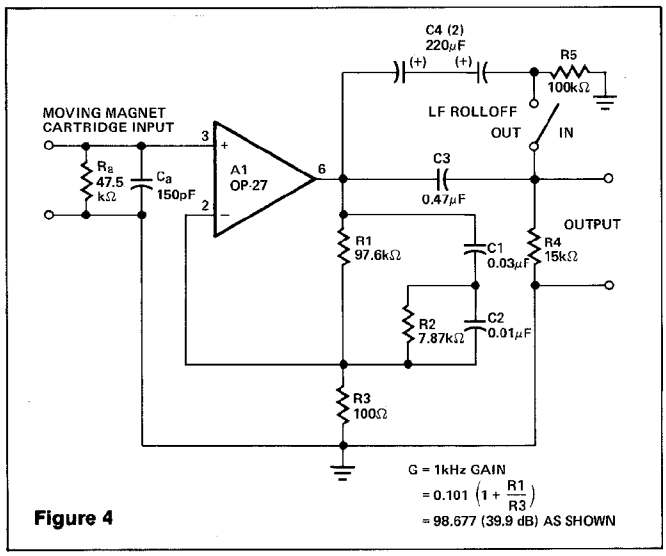


Figure 4

The OP-27 brings a 3.2nV/$\sqrt{Hz}$ voltage noise and 0.45 pA/$\sqrt{Hz}$ current noise to this circuit. To minimize noise from other sources, R_3 is set to a value of 100Ω, which generates a voltage noise of 1.3nV/$\sqrt{Hz}$. The noise increases the 3.2nV/$\sqrt{Hz}$ of the amplifier by only 0.7dB. With a 1kΩ source, the circuit noise measures 63dB below a 1mV reference level, unweighted, in a 20kHz noise bandwidth.

Gain (G) of the circuit at 1kHz can be calculated by the expression:

$$G = 0.101\ (1 + \frac{R_1}{R_3})$$

For the values shown, the gain is just under 100 (or 40dB). Lower gains can be accommodated by increasing R_3, but gains higher than 40dB will show more equalization errors because of the 8MHz gain-bandwidth of the OP-27.

This circuit is capable of very low distortion over its entire range, generally below 0.01% at levels up to 7V rms. At 3V output levels, it will produce less than 0.03% total harmonic distortion at frequencies up to 20kHz.

Capacitor C_3 and resistor R_4 form a simple −6dB-per-octave rumble filter, with a corner at 22Hz. As an option, the switch-selected shunt capacitor C_4, a nonpolarized electrolytic, bypasses the low-frequency rolloff. Placing the rumble filter's high-pass action after the preamp has the desirable result of discriminating against the RIAA-amplified low-frequency noise components and pickup-produced low-frequency disturbances.

A preamplifier for NAB tape playback is similar to an RIAA phono preamp, though more gain is typically demanded, along with equalization requiring a heavy low-frequency boost. The circuit in Fig. 4 can be readily modified for tape use, as shown by Fig. 5.

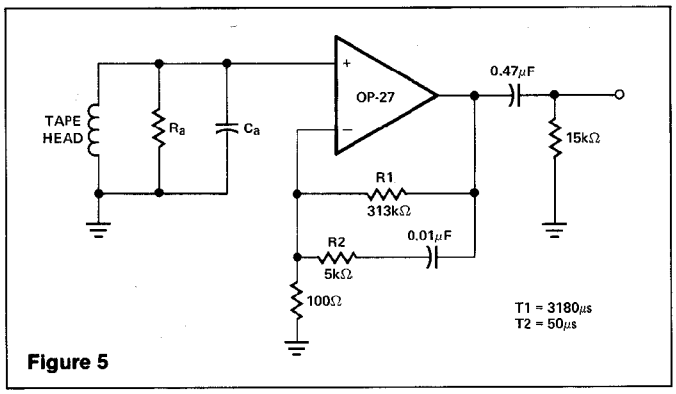


Figure 5

While the tape-equalization requirement has a flat high-frequency gain above 3kHz ($T_2 = 50\mu s$), the amplifier need not be stabilized for unity gain. The decompensated OP-37 provides a greater bandwidth and slew rate. For many applications, the idealized time constants shown may require trimming of R_1 and R_2 to optimize frequency response for nonideal tape-head performance and other factors.[5]

The network values of the configuration yield a 50dB gain at 1kHz, and the dc gain is greater than 70dB. Thus, the worst-case output offset is just over 500mV. A single 0.47μF output capacitor can block this level without affecting the dynamic range.

The tape head can be coupled directly to the amplifier input, since the worst-case bias current of 80nA with a 400mH, 100 μin. head (such as the PRB2H7K) will not be troublesome.

One potential tape-head problem is presented by amplifier bias-current transients which can magnetize a head. The OP-27 and OP-37 are free of bias-current transients upon power up or power down. However, it is always advantageous to control the speed of power supply rise and fall, to eliminate transients.

In addition, the dc resistance of the head should be carefully controlled, and preferably below 1kΩ. For this configuration, the bias-current-induced offset voltage can be greater than the 100μV maximum offset if the head resistance is not sufficiently controlled.

A simple, but effective, fixed-gain transformerless microphone preamp (Fig. 6) amplifies differential signals from low-impedance microphones by 50dB, and has an input impedance of 2kΩ. Because of the high working gain of the circuit, an OP-37 helps to preserve bandwidth, which will be 110kHz. As the OP-37 is a decompensated device (minimum stable gain of 5), a dummy resistor, R_p, may be necessary, if the microphone is to be unplugged. Otherwise the 100% feedback from the open input may cause the amplifier to oscillate.

Common-mode input-noise rejection will depend upon the match of the bridge-resistor ratios. Either close-tolerance (0.1%) types should be used, or R_4 should be trimmed for best CMRR. All resistors should be metal-film types for best stability and low noise.

Noise performance of this circuit is limited more by the input resistors R_1 and R_2 than by the op amp, as R_1 and R_2 each generate a 4nV/$\sqrt{Hz}$ noise, while the op amp generates a 3.2nV/$\sqrt{Hz}$ noise. The rms sum of these predominant noise sources will be about 6nV/$\sqrt{Hz}$, equivalent to 0.9μV in a 20kHz noise bandwidth, or nearly 61dB below a 1mV input signal. Measurements confirm this predicted performance.

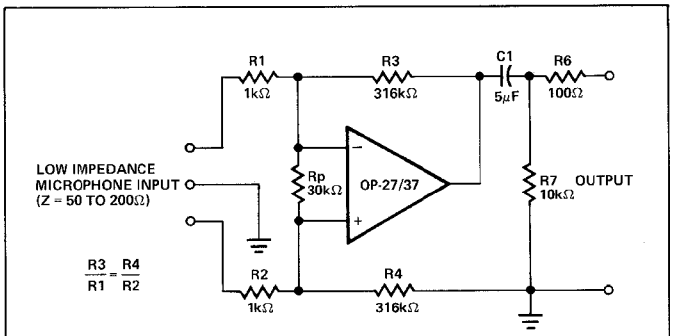
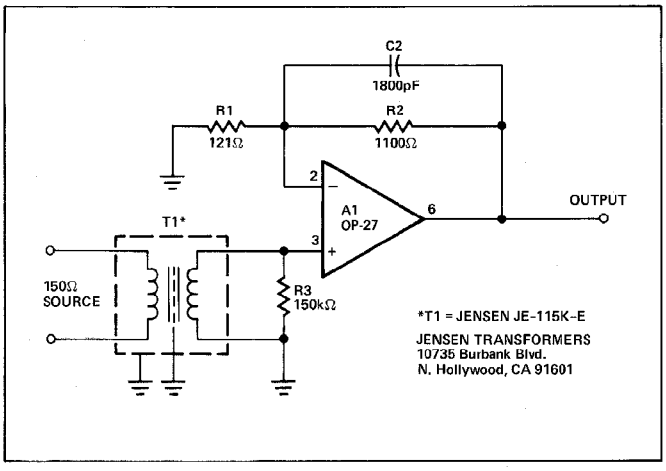


Figure 6

For applications demanding appreciably lower noise, a high-quality microphone-transformer-coupled preamp (Fig. 7) incorporates the internally-compensated OP-27. T_1 is a JE-115K-E 150Ω/15kΩ transformer which provides an optimum source resistance for the OP-27 device. The circuit has an overall gain of 40dB, the product of the transformer's voltage setup and the op amp's voltage gain.



Gain may be trimmed to other levels, if desired, by adjusting R_2 or R_1. Because of the low offset voltage of the OP-27, the output offset of this circuit will be very low, 1.7mV or less, for a 40dB gain. The typical output blocking capacitor can be eliminated in such cases, but is desirable for higher gains to eliminate switching transients.

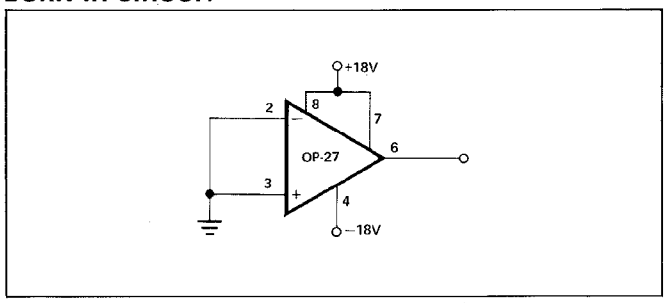
Capacitor C_2 and resistor R_2 form a 2μs time constant in this circuit, as recommended for optimum transient response by the transformer manufacturer. With C_2 in use, A_1 must have unity-gain stability. For situations where the 2μs time constant is not necessary, C_2 can be deleted, allowing the faster OP-37 to be employed.

Some comment on noise is appropriate to understand the capability of this circuit. A 150Ω resistor and R_1 and R_2 gain resistors connected to a noiseless amplifier will generate 220 nV of noise in a 20kHz bandwidth, or 73dB below a 1mV reference level. Any practical amplifier can only approach this noise level; it can never exceed it. With the OP-27 and T_1 specified, the additional noise degradation will be close to 3.6dB (or −69.5 referenced to 1mV).

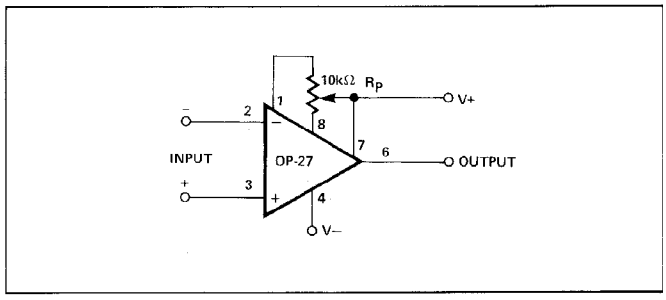
References

1. Lipshitz, S.P., "On RIAA Equalization Networks," *JAES*, Vol. 27, June 1979, p. 458-481.
2. Jung, W.G., *IC Op Amp Cookbook*, 2nd Ed., H.W. Sams and Company, 1980.
3. Jung, W.G., *Audio IC Op Amp Applications*, 2nd Ed., H.W. Sams and Company, 1978.
4. Jung, W.G., and Marsh, R.M., "Picking Capacitors," *Audio*, February & March, 1980.
5. Otala, M., "Feedback-Generated Phase Nonlinearity in Audio Amplifiers," London AES Convention, March 1980, preprint 1976.
6. Stout, D.F., and Kaufman, M., *Handbook of Operational Amplifier Circuit Design*, New York, McGraw Hill, 1976.

BURN-IN CIRCUIT



OFFSET NULLING CIRCUIT



Phase Detector/Frequency Synthesizer

ADF4002

FEATURES

400 MHz bandwidth
2.7 V to 3.3 V power supply
Separate charge pump supply (V_P) allows extended tuning voltage in 3 V systems
Programmable charge pump currents
3-wire serial interface
Analog and digital lock detect
Hardware and software power-down mode
104 MHz phase detector

APPLICATIONS

Clock conditioning
Clock generation
IF LO generation

GENERAL DESCRIPTION

The ADF4002 frequency synthesizer is used to implement local oscillators in the upconversion and downconversion sections of wireless receivers and transmitters. It consists of a low noise digital phase frequency detector (PFD), a precision charge pump, a programmable reference divider, and programmable N divider. The 14-bit reference counter (R counter) allows selectable REFIN frequencies at the PFD input. A complete phase-locked loop (PLL) can be implemented if the synthesizer is used with an external loop filter and voltage controlled oscillator (VCO). In addition, by programming R and N to 1, the part can be used as a standalone PFD and charge pump.

FUNCTIONAL BLOCK DIAGRAM

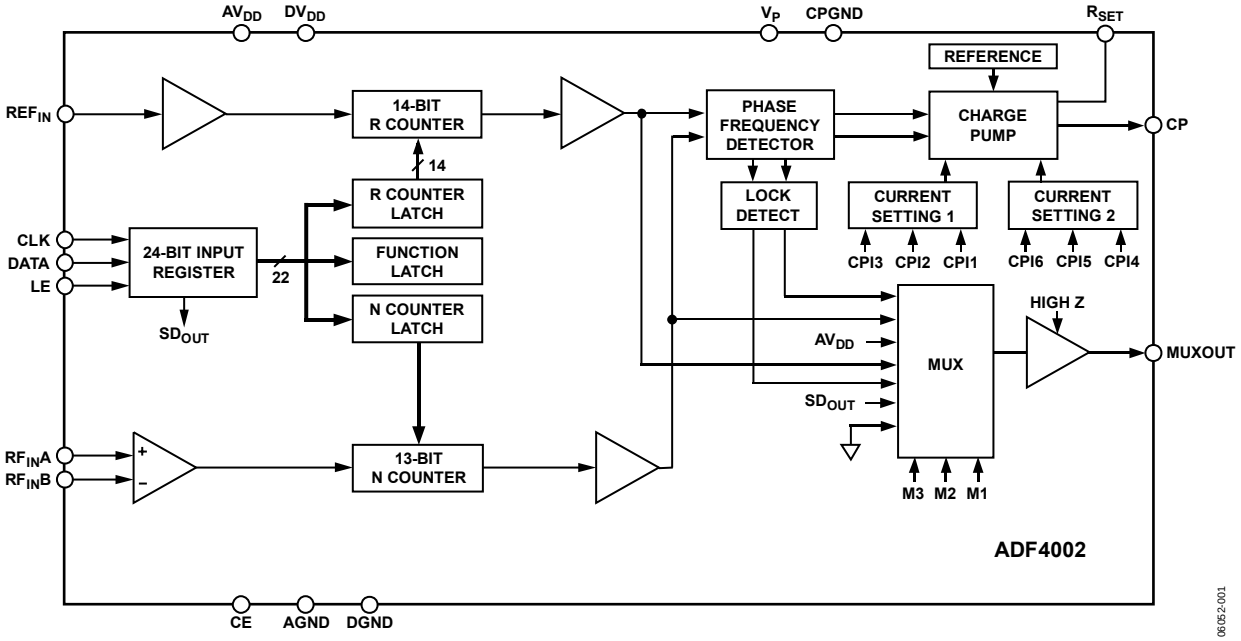


Figure 1.

Rev. A

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Tel: 781.329.4700 **www.analog.com**
Fax: 781.461.3113

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REVISION HISTORY

4/07—Rev. 0 to Rev. A

Changes to Features List 1
Changes to Table 1 3
Deleted Figure 7
Changes to Figure 16 11

4/06—Revision 0: Initial Version

SPECIFICATIONS

AV_{DD} = DV_{DD} = 3 V ± 10%, AV_{DD} ≤ V_P ≤ 5.5 V, AGND = DGND = CPGND = 0 V, R_{SET} = 5.1 kΩ, dBm referred to 50 Ω, T_A = T_{MAX} to T_{MIN}, unless otherwise noted.

Table 1.

	B Version[1]				
Parameter	**Min**	**Typ**	**Max**	**Unit**	**Test Conditions/Comments**
RF CHARACTERISTICS					See Figure 11 for input circuit
RF Input Sensitivity	−10		0	dBm	
RF Input Frequency (RF_{IN})	5		400	MHz	For RF_{IN} < 5 MHz, ensure slew rate (SR) > 4 V/µs
REFIN CHARACTERISTICS					
REFIN Input Frequency	20		300	MHz	For REFIN < 20 MHz, ensure SR > 50 V/µs
REFIN Input Sensitivity[2]	0.8		V_{DD}	V p-p	Biased at $AV_{DD}/2$[3]
REFIN Input Capacitance			10	pF	
REFIN Input Current			±100	µA	
PHASE DETECTOR					
Phase Detector Frequency[4]			104	MHz	ABP = 0, 0 (2.9 ns antibacklash pulse width)
CHARGE PUMP					Programmable, see Figure 18
I_{CP} Sink/Source					
High Value		5		mA	With R_{SET} = 5.1 kΩ
Low Value		625		µA	
Absolute Accuracy		2.5		%	With R_{SET} = 5.1 kΩ
R_{SET} Range	3.0		11	kΩ	See Figure 18
I_{CP} Three-State Leakage		1		nA	T_A = 25°C
I_{CP} vs. V_{CP}		1.5		%	0.5 V ≤ V_{CP} ≤ V_P − 0.5 V
Sink and Source Current Matching		2		%	0.5 V ≤ V_{CP} ≤ V_P − 0.5 V
I_{CP} vs. Temperature		2		%	V_{CP} = V_P/2
LOGIC INPUTS					
V_{IH}, Input High Voltage	1.4			V	
V_{IL}, Input Low Voltage			0.6	V	
I_{INH}, I_{INL}, Input Current			±1	µA	
C_{IN}, Input Capacitance			10	pF	
LOGIC OUTPUTS					
V_{OH}, Output High Voltage	1.4			V	Open-drain output chosen, 1 kΩ pull-up resistor to 1.8 V
V_{OH}, Output High Voltage	V_{DD} − 0.4			V	CMOS output chosen
I_{OH}			100	µA	
V_{OL}, Output Low Voltage			0.4	V	I_{OL} = 500 µA
POWER SUPPLIES					
AV_{DD}	2.7		3.3	V	
DV_{DD}	AV_{DD}				
V_P	AV_{DD}		5.5	V	AV_{DD} ≤ V_P ≤ 5.5 V
I_{DD}[5] (AI_{DD} + DI_{DD})		5.0	6.0	mA	
I_P			0.4	mA	T_A = 25°C
Power-Down Mode		1		µA	AI_{DD} + DI_{DD}
NOISE CHARACTERISTICS					
Normalized Phase Noise Floor[6]		−222		dBc/Hz	

[1] Operating temperature range (B version) is −40°C to +85°C.
[2] AV_{DD} = DV_{DD} = 3 V.
[3] AC coupling ensures $AV_{DD}/2$ bias.
[4] Guaranteed by design. Sample tested to ensure compliance.
[5] T_A = 25°C; AV_{DD} = DV_{DD} = 3 V; RF_{IN} = 350 MHz. The current for any other setup (25°C, 3.0 V) in mA is given by 2.35 + 0.0046 (REFIN) + 0.0062 (RF), RF frequency and REFIN frequency in MHz.
[6] The normalized phase noise floor is estimated by measuring the in-band phase noise at the output of the VCO and subtracting 20logN (where N is the N divider value) and $10\log F_{PFD}$. PN_{SYNTH} = PN_{TOT} − $10\log F_{PFD}$ − 20logN. All phase noise measurements were performed with an Agilent E5500 phase noise test system, using the EVAL-ADF4002EB1 and the HP8644B as the PLL reference.

TIMING CHARACTERISTICS

AV_{DD} = DV_{DD} = 3 V ± 10%, AV_{DD} ≤ V_P ≤ 5.5 V, AGND = DGND = CPGND = 0 V, R_{SET} = 5.1 kΩ, dBm referred to 50 Ω, T_A = T_{MAX} to T_{MIN}, unless otherwise noted.[1]

Table 2.

Parameter	Limit (B Version)[2]	Unit	Test Conditions/Comments
t_1	10	ns min	DATA to CLK setup time
t_2	10	ns min	DATA to CLK hold time
t_3	25	ns min	CLK high duration
t_4	25	ns min	CLK low duration
t_5	10	ns min	CLK to LE setup time
t_6	20	ns min	LE pulse width

[1] Guaranteed by design, but not production tested.
[2] Operating temperature range (B version) is −40°C to +85°C.

Timing Diagram

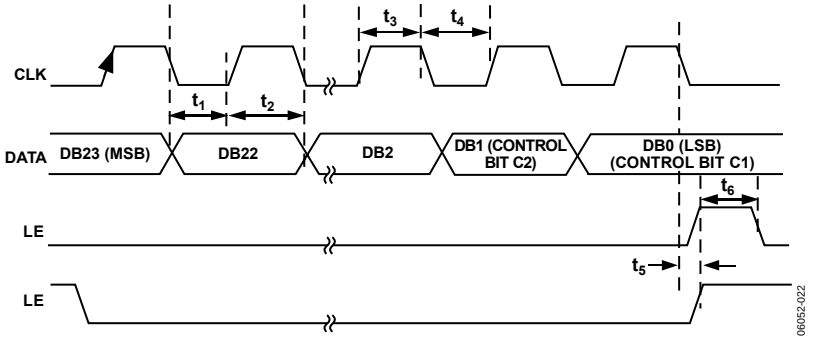

Figure 2. Timing Diagram

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 3.

Parameter	Rating
AV_{DD} to GND[1]	−0.3 V to +3.6 V
AV_{DD} to DV_{DD}	−0.3 V to +0.3 V
V_P to GND	−0.3 V to +5.8 V
V_P to AV_{DD}	−0.3 V to +5.8 V
Digital I/O Voltage to GND	−0.3 V to VDD + 0.3 V
Analog I/O Voltage to GND	−0.3 V to V_P + 0.3 V
REFIN, $RF_{IN}A$, $RF_{IN}B$ to GND	−0.3 V to VDD + 0.3 V
Operating Temperature Range	
Industrial (B Version)	−40°C to +85°C
Storage Temperature Range	−65°C to +125°C
Maximum Junction Temperature	150°C
Lead Temperature, Soldering	
Vapor Phase (60 sec)	215°C
Infrared (15 sec)	220°C
Transistor Count	
CMOS	6425
Bipolar	303

[1] GND = AGND = DGND = 0 V.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device is a high performance RF integrated circuit with an ESD rating of <2 kV, and it is ESD sensitive. Proper precautions should be taken for handling and assembly.

THERMAL CHARACTERISTICS

Table 4. Thermal Impedance

Package Type	θ_{JA}	Unit
TSSOP	150.4	°C/W
LFCSP	122	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

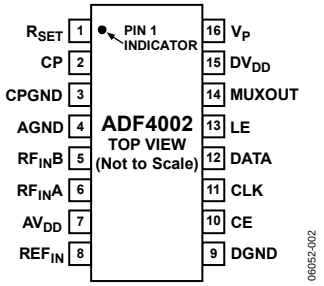

Figure 3. TSSOP Pin Configuration (Top View)

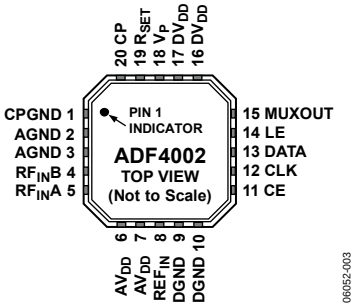

Figure 4. LFCSP Pin Configuration (Top View)

Table 5. Pin Function Descriptions

Pin No.			
TSSOP	**LFCSP**	**Mnemonic**	**Description**
1	19	R_{SET}	Connecting a resistor between this pin and CPGND sets the maximum charge pump output current. The nominal voltage potential at the R_{SET} pin is 0.66 V. The relationship between I_{CP} and R_{SET} is $$I_{CP\,MAX} = \frac{25.5}{R_{SET}}$$ where R_{SET} = 5.1 kΩ and $I_{CP\,MAX}$ = 5 mA.
2	20	CP	Charge Pump Output. When enabled, this provides ±I_{CP} to the external loop filter that, in turn, drives the external VCO.
3	1	CPGND	Charge Pump Ground. This is the ground return path for the charge pump.
4	2, 3	AGND	Analog Ground. This is the ground return path of the RF input.
5	4	$RF_{IN}B$	Complementary Input to the RF Input. This point must be decoupled to the ground plane with a small bypass capacitor, typically 100 pF. See Figure 11.
6	5	$RF_{IN}A$	Input to the RF Input. This small signal input is ac-coupled to the external VCO.
7	6, 7	AV_{DD}	Analog Power Supply. This can range from 2.7 V to 3.3 V. Decoupling capacitors to the analog ground plane should be placed as close as possible to the AV_{DD} pin. AV_{DD} must be the same value as DV_{DD}.
8	8	REF_{IN}	Reference Input. This is a CMOS input with a nominal threshold of V_{DD}/2 and a dc equivalent input resistance of 100 kΩ. See Figure 10. This input can be driven from a TTL or CMOS crystal oscillator or it can be ac-coupled.
9	9, 10	DGND	Digital Ground.
10	11	CE	Chip Enable. A logic low on this pin powers down the device and puts the charge pump output into three-state mode. Taking this pin high powers up the device, depending on the status of the Power-Down Bit F2.
11	12	CLK	Serial Clock Input. This serial clock is used to clock in the serial data to the registers. The data is latched into the 24-bit shift register on the CLK rising edge. This input is a high impedance CMOS input.
12	13	DATA	Serial Data Input. The serial data is loaded MSB first with the two LSBs being the control bits. This input is a high impedance CMOS input.
13	14	LE	Load Enable, CMOS Input. When LE goes high, the data stored in the shift registers is loaded into one of the four latches; the latch is selected using the control bits.
14	15	MUXOUT	Multiplexer Output. This allows either the lock detect, the scaled RF, or the scaled reference frequency to be accessed externally.
15	16, 17	DV_{DD}	Digital Power Supply. This can range from 2.7 V to 3.3 V. Decoupling capacitors to the digital ground plane should be placed as close as possible to this pin. DV_{DD} must be the same value as AV_{DD}.
16	18	V_P	Charge Pump Power Supply. This should be greater than or equal to V_{DD}. In systems where V_{DD} is 3 V, it can be set to 5.5 V and used to drive a VCO with a tuning range of up to 5 V.

TYPICAL PERFORMANCE CHARACTERISTICS

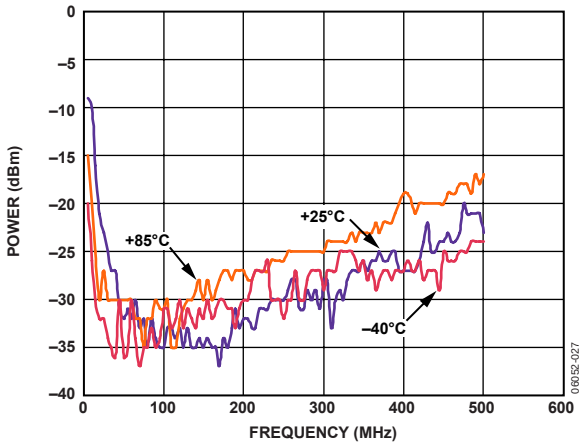

Figure 5. RF Input Sensitivity

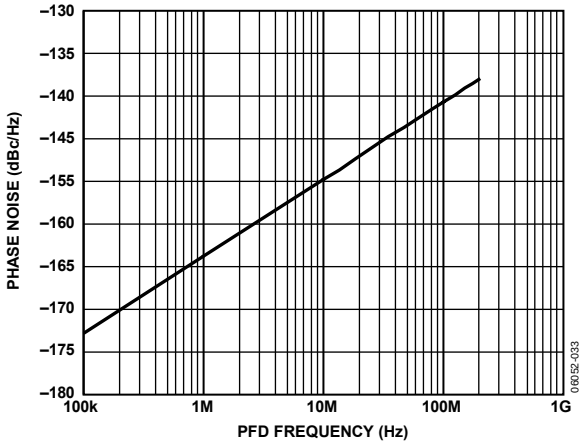

Figure 8. Phase Noise (Referred to CP Output) vs. PFD Frequency

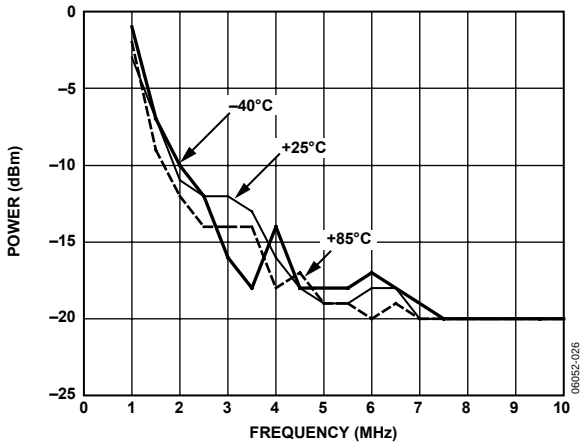

Figure 6. RF Input Sensitivity, Low Frequency

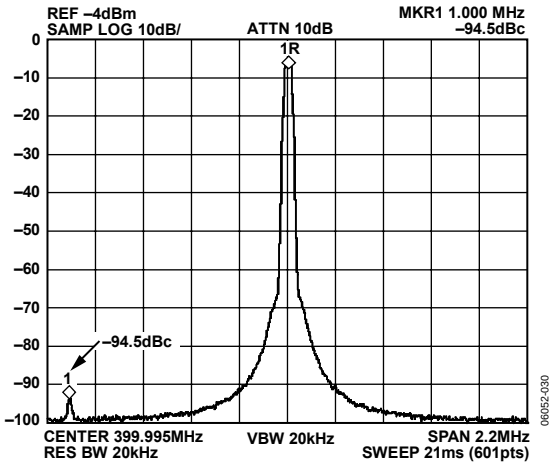

Figure 9. Reference Spurs (400 MHz, 1 MHz, 7 kHz)

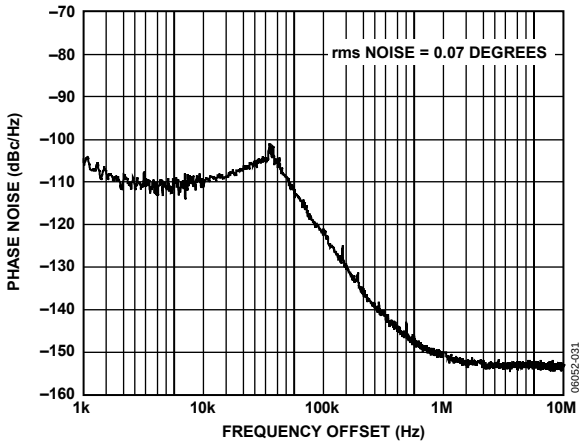

Figure 7. Integrated Phase Noise (400 MHz, 1 MHz, 50 kHz)

THEORY OF OPERATION

REFERENCE INPUT SECTION

The reference input stage is shown in Figure 10. SW1 and SW2 are normally closed switches. SW3 is normally open. When power-down is initiated, SW3 is closed and SW1 and SW2 are opened. This ensures that there is no loading of the REF_{IN} pin on power-down.

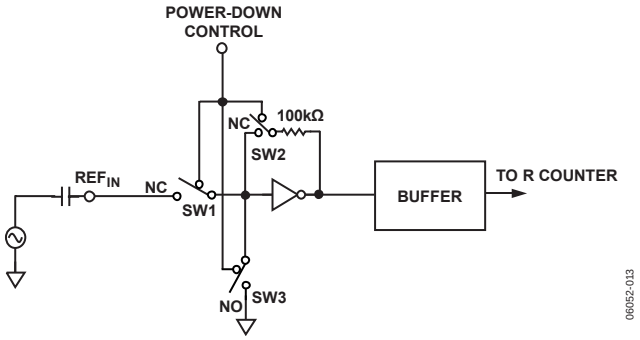

Figure 10. Reference Input Stage

RF INPUT STAGE

The RF input stage is shown in Figure 11. It is followed by a 2-stage limiting amplifier to generate the CML clock levels needed for the N counter.

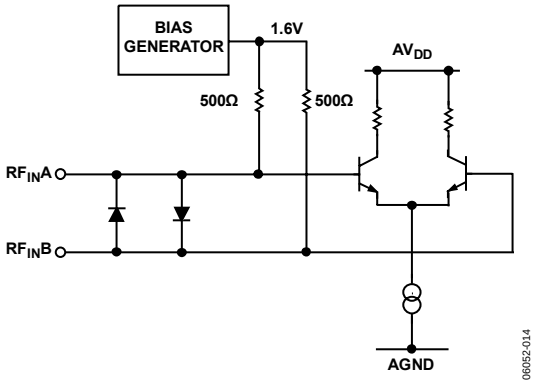

Figure 11. RF Input Stage

N COUNTER

The N CMOS counter allows a wide ranging division ratio in the PLL feedback counter. Division ratios from 1 to 8191 are allowed.

N and R Relationship

The N counter makes it possible to generate output frequencies that are spaced only by the reference frequency divided by R.

The equation for the VCO frequency is

$$f_{VCO} = N \times \frac{f_{REFIN}}{R}$$

where:

f_{VCO} is the output frequency of external voltage controlled oscillator (VCO).
N is the preset divide ratio of binary 13-bit counter (1 to 8191).
f_{REFIN} is the external reference frequency oscillator.

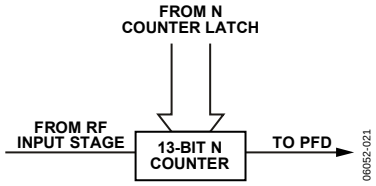

Figure 12. N Counter

R COUNTER

The 14-bit R counter allows the input reference frequency to be divided down to produce the reference clock to the phase frequency detector (PFD). Division ratios from 1 to 16,383 are allowed.

PHASE FREQUENCY DETECTOR (PFD) AND CHARGE PUMP

The PFD takes inputs from the R counter and N counter and produces an output proportional to the phase and frequency difference between them. Figure 13 is a simplified schematic. The PFD includes a programmable delay element that controls the width of the antibacklash pulse. This pulse ensures that there is no dead zone in the PFD transfer function, and minimizes phase noise and reference spurs. Two bits in the reference counter latch (ABP2 and ABP1) control the width of the pulse. See Figure 16 for details. The smallest antibacklash pulse width is not recommended.

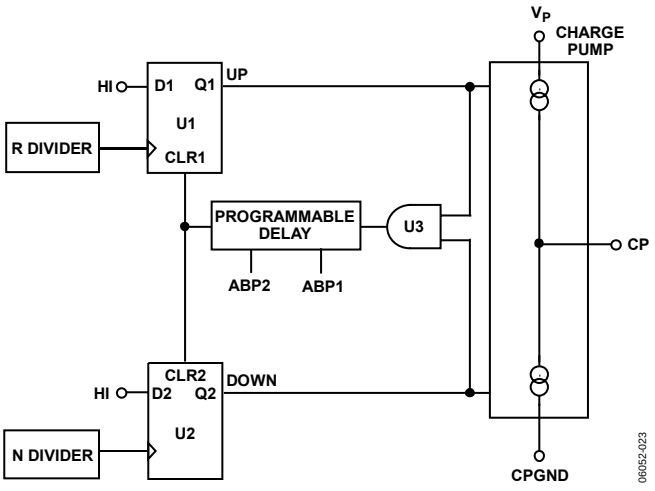

Figure 13. PFD Simplified Schematic and Timing (In Lock)

MUXOUT AND LOCK DETECT

The output multiplexer on the ADF4002 allows the user to access various internal points on the chip. The state of MUXOUT is controlled by M3, M2, and M1 in the function latch. Figure 18 shows the full truth table. Figure 14 shows the MUXOUT section in block diagram form.

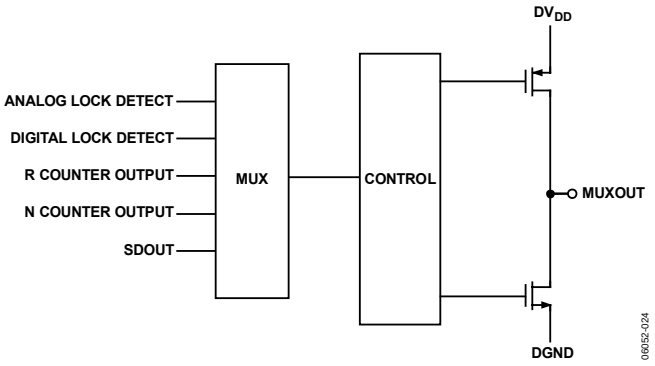

Figure 14. MUXOUT Circuit

Lock Detect

MUXOUT can be programmed for two types of lock detect: digital lock detect and analog lock detect.

Digital lock detect is active high. When LDP in the R counter latch is set to 0, digital lock detect is set high when the phase error on three consecutive phase detector (PD) cycles is less than 15 ns. With LDP set to 1, five consecutive cycles of less than 15 ns are required to set the lock detect. It stays set at high until a phase error of greater than 25 ns is detected on any subsequent PD cycle. For PFD frequencies greater than 10 MHz, analog lock detect is more accurate because of the smaller pulse widths.

The N-channel, open-drain, analog lock detect should be operated with an external pull-up resistor of 10 kΩ nominal. When lock has been detected, this output is high with narrow, low going pulses.

INPUT SHIFT REGISTER

The ADF4002 digital section includes a 24-bit input shift register, a 14-bit R counter, and a 13-bit N counter. Data is clocked into the 24-bit shift register on each rising edge of CLK. The data is clocked in MSB first. Data is transferred from the shift register to one of four latches on the rising edge of LE. The destination latch is determined by the state of the two control bits (C2, C1) in the shift register. These are the two LSBs, DB1 and DB0, as shown in the timing diagram (see Figure 2). Table 6 provides the truth table for these bits. Figure 15 shows a summary of how the latches are programmed.

Table 6. C2, C1 Truth Table

Control Bits		
C2	**C1**	**Data Latch**
0	0	R Counter
0	1	N Counter
1	0	Function Latch
1	1	Initialization Latch

LATCH MAPS AND DESCRIPTIONS

LATCH SUMMARY

REFERENCE COUNTER LATCH

RESERVED			LOCK DETECT PRECISION	TEST MODE BITS		ANTI-BACKLASH WIDTH		14-BIT REFERENCE COUNTER													CONTROL BITS	
DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
X	0	0	LDP	T2	T1	ABP2	ABP1	R14	R13	R12	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	C2 (0)	C1 (0)

N COUNTER LATCH

RESERVED		CP GAIN	13-BIT N COUNTER													RESERVED						CONTROL BITS	
DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
X	X	G1	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	X	X	X	X	X	X	C2 (0)	C1 (1)

FUNCTION LATCH

RESERVED		POWER-DOWN 2	CURRENT SETTING 2			CURRENT SETTING 1			TIMER COUNTER CONTROL				FASTLOCK MODE	FASTLOCK ENABLE	CP THREE-STATE	PD POLARITY	MUXOUT CONTROL			POWER-DOWN 1	COUNTER RESET	CONTROL BITS	
DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
X	X	PD2	CPI6	CPI5	CPI4	CPI3	CPI2	CPI1	TC4	TC3	TC2	TC1	F5	F4	F3	F2	M3	M2	M1	PD1	F1	C2 (1)	C1 (0)

INITIALIZATION LATCH

RESERVED		POWER-DOWN 2	CURRENT SETTING 2			CURRENT SETTING 1			TIMER COUNTER CONTROL				FASTLOCK MODE	FASTLOCK ENABLE	CP THREE-STATE	PD POLARITY	MUXOUT CONTROL			POWER-DOWN 1	COUNTER RESET	CONTROL BITS	
DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
X	X	PD2	CPI6	CPI5	CPI4	CPI3	CPI2	CPI1	TC4	TC3	TC2	TC1	F5	F4	F3	F2	M3	M2	M1	PD1	F1	C2 (1)	C1 (1)

06052-015

Figure 15. Latch Summary

REFERENCE COUNTER LATCH MAP

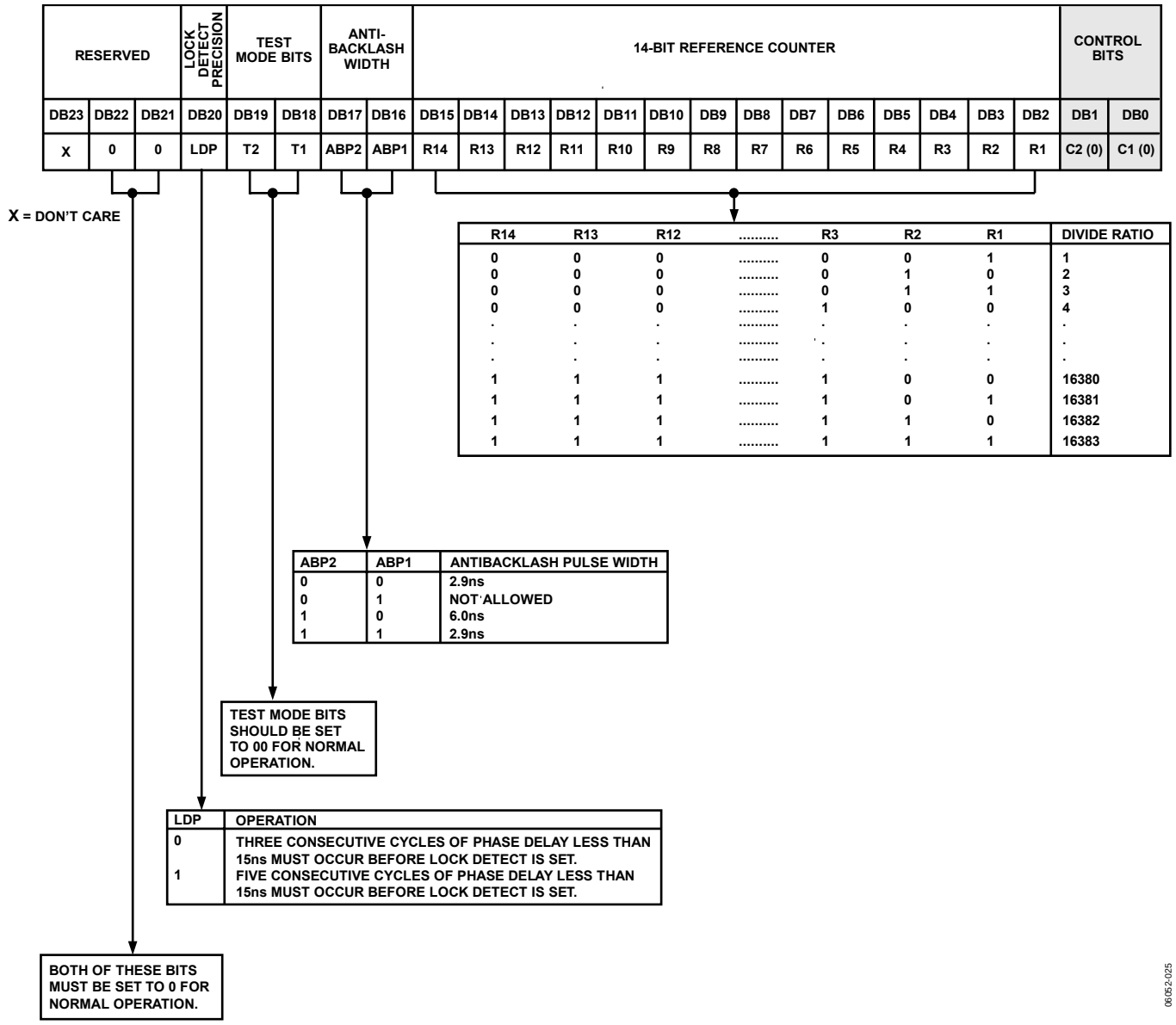

Figure 16. Reference Counter Latch Map

N COUNTER LATCH MAP

RESERVED		CP GAIN	13-BIT N COUNTER													RESERVED						CONTROL BITS	
DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
X	X	G1	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	X	X	X	X	X	X	C2 (0)	C1 (1)

X = DON'T CARE

N13	N12	N11		N3	N2	N1	N COUNTER DIVIDE RATIO
0	0	0	.....	0	0	0	NOT ALLOWED
0	0	0	.....	0	0	1	1
0	0	0	.....	0	1	0	2
0	0	0	.....	0	1	1	3
.	.	.	.....	.	.	.	.
.	.	.	.....	.	.	.	.
.	.	.	.....	.	.	.	.
1	1	1	.....	1	0	0	8188
1	1	1	.....	1	0	1	8189
1	1	1	.....	1	1	0	8190
1	1	1	.....	1	1	1	8191

F4 (FUNCTION LATCH) FASTLOCK ENABLE	CP GAIN	OPERATION
0	0	CHARGE PUMP CURRENT SETTING 1 IS PERMANENTLY USED.
0	1	CHARGE PUMP CURRENT SETTING 2 IS PERMANENTLY USED.
1	0	CHARGE PUMP CURRENT SETTING 1 IS USED.
1	1	CHARGE PUMP CURRENT IS SWITCHED TO SETTING 2. THE TIME SPENT IN SETTING 2 IS DEPENDENT ON WHICH FASTLOCK MODE IS USED. SEE FUNCTION LATCH DESCRIPTION.

THESE BITS ARE NOT USED BY THE DEVICE AND ARE DON'T CARE BITS.

THESE BITS ARE NOT USED BY THE DEVICE AND ARE DON'T CARE BITS.

06052-016

Figure 17. N Counter Latch Map

FUNCTION LATCH MAP

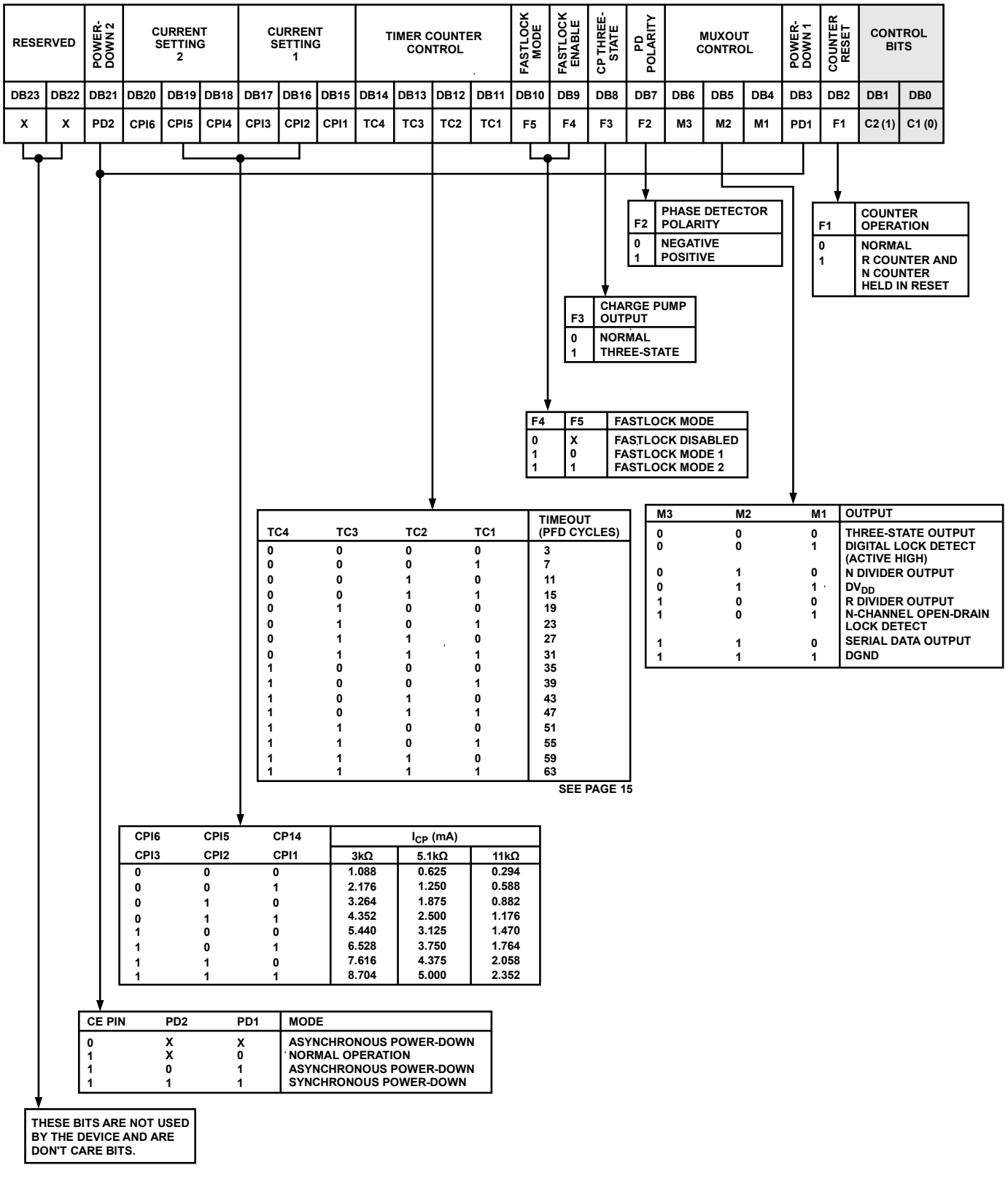

Figure 18. Function Latch Map

INITIALIZATION LATCH MAP

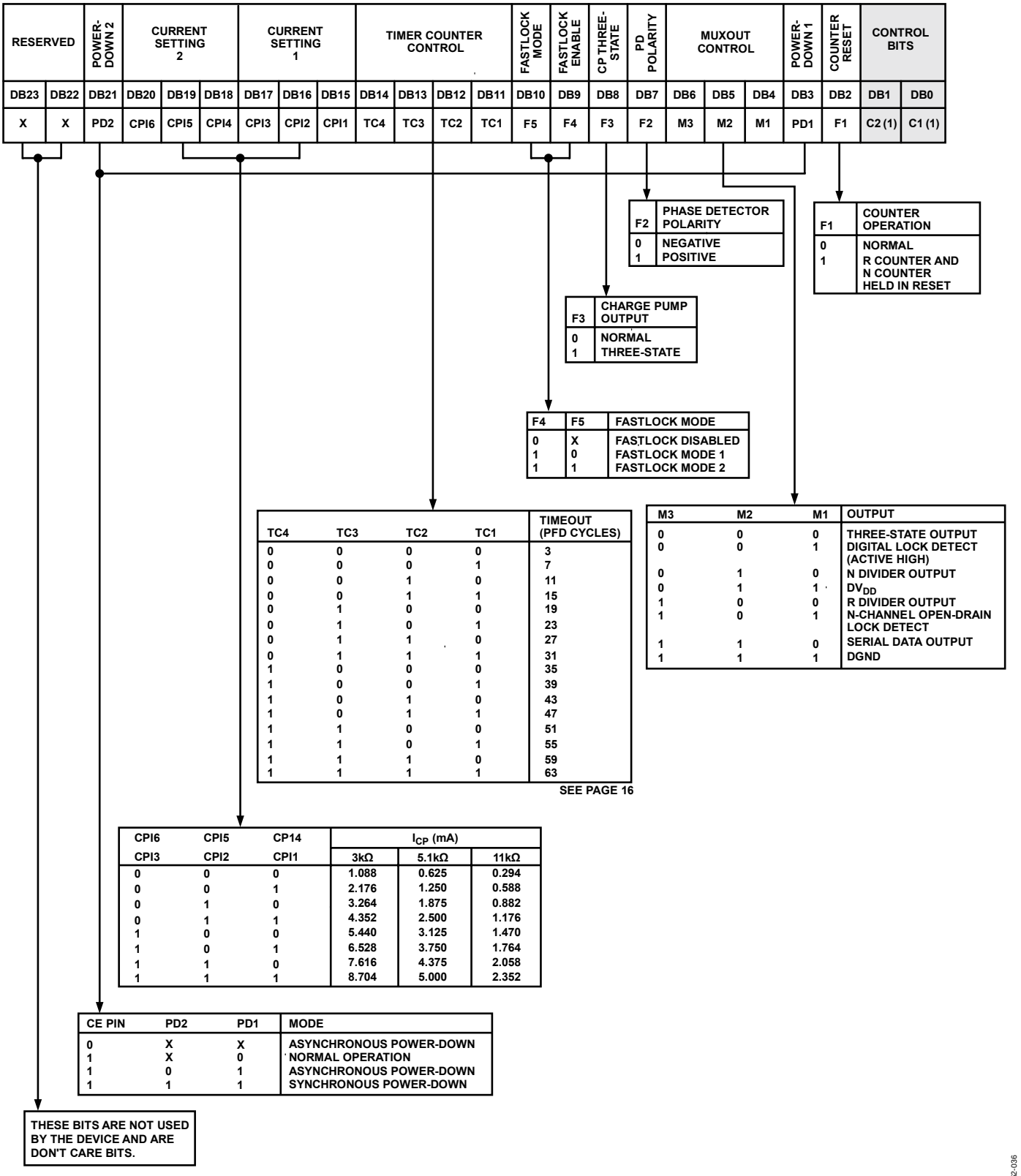

Figure 19. Initialization Latch Map

FUNCTION LATCH

With C2, C1 set to 1, 0, the on-chip function latch is programmed. Figure 18 shows the input data format for programming the function latch.

Counter Reset

DB2 (F1) is the counter reset bit. When this bit is set to 1, the R counter and the N counter are reset. For normal operation, set this bit to 0. Upon powering up, the F1 bit needs to be disabled (set to 0). Then, the N counter resumes counting in close alignment with the R counter (the maximum error is one prescaler cycle).

Power-Down

DB3 (PD1) and DB21 (PD2) provide programmable power-down modes. These bits are enabled by the CE pin.

When the CE pin is low, the device is immediately disabled regardless of the states of the PD2, PD1 bits.

In the programmed asynchronous power-down, the device powers down immediately after latching a 1 into Bit PD1, with the condition that Bit PD2 has been loaded with a 0.

In the programmed synchronous power-down, the device power-down is gated by the charge pump to prevent unwanted frequency jumps. Once the power-down is enabled by writing a 1 into Bit PD1 (on condition that a 1 has also been loaded to Bit PD2), then the device enters power-down on the occurrence of the next charge pump event.

When a power-down is activated (either in synchronous or asynchronous mode, including a CE pin activated power-down), the following events occur:

- All active dc current paths are removed.
- The R, N, and timeout counters are forced to their load state conditions.
- The charge pump is forced into three-state mode.
- The digital lock detect circuitry is reset.
- The RFIN input is debiased.
- The reference input buffer circuitry is disabled.
- The input register remains active and capable of loading and latching data.

MUXOUT Control

The on-chip multiplexer is controlled by M3, M2, and M1 on the ADF4002. Figure 18 shows the truth table.

Fastlock Enable Bit

DB9 of the function latch is the fastlock enable bit. Only when this is 1 is fastlock enabled.

Fastlock Mode Bit

DB10 of the function latch is the fastlock mode bit. When fastlock is enabled, this bit determines the fastlock mode to be used. If the fastlock mode bit is 0, then Fastlock Mode 1 is selected, and if the fastlock mode bit is 1, then Fastlock Mode 2 is selected.

Fastlock Mode 1

In this mode, the charge pump current is switched to the contents of Current Setting 2. The device enters fastlock by having a 1 written to the CP gain bit in the N counter latch. The device exits fastlock by having a 0 written to the CP gain bit in the AB counter latch.

Fastlock Mode 2

In this mode, the charge pump current is switched to the contents of Current Setting 2. The device enters fastlock by having a 1 written to the CP gain bit in the N counter latch. The device exits fastlock under the control of the timer counter. After the timeout period determined by the value in TC4 to TC1, the CP gain bit in the N counter latch is automatically reset to 0 and the device reverts to normal mode instead of fastlock. See Figure 18 for the timeout periods.

Timer Counter Control

The user has the option of programming two charge pump currents. The intent is to use the Current Setting 1 when the RF output is stable and the system is in a static state. Current Setting 2 is meant to be used when the system is dynamic and in a state of change, that is, when a new output frequency is programmed.

The normal sequence of events is as follows:

The user initially decides the referred charge pump currents. For example, the choice can be 2.5 mA as Current Setting 1 and 5 mA as Current Setting 2.

At the same time, the decision must be made as to how long the secondary current is to stay active before reverting to the primary current. This is controlled by Timer Counter Control Bit DB14 to Timer Counter Control Bit DB11 (TC4 to TC1) in the function latch. See Figure 18 for the truth table.

To program a new output frequency, simply program the N counter latch with a new value for N. At the same time, the CP gain bit can be set to 1. This sets the charge pump with the value in CPI6 to CPI4 for a period of time determined by TC4 to TC1. When this time is up, the charge pump current reverts to the value set by CPI3 to CPI1. At the same time, the CP gain bit in the N counter latch is reset to 0 and is ready for the next time that the user wishes to change the frequency.

Note that there is an enable feature on the timer counter. It is enabled when Fastlock Mode 2 is chosen by setting the Fastlock Mode Bit DB10 in the function latch to 1.

Charge Pump Currents

CPI3, CPI2, and CPI1 program Current Setting 1 for the charge pump. CPI6, CPI5, and CPI4 program Current Setting 2 for the charge pump. See Figure 18 for the truth table.

PD Polarity

This bit sets the phase detector polarity bit (see Figure 18).

CP Three-State

This bit controls the CP output pin. Setting the bit high puts the CP output into three-state. With the bit set low, the CP output is enabled.

INITIALIZATION LATCH

The initialization latch is programmed when C2, C1 = 1, 1. This is essentially the same as the function latch (programmed when C2, C1 = 1, 0).

However, when the initialization latch is programmed there is an additional internal reset pulse applied to the R and N counters. This pulse ensures that the N counter is at load point when the N counter data is latched and the device begins counting in close phase alignment.

If the latch is programmed for synchronous power-down (CE pin is high; PD1 bit is high; and PD2 bit is low), the internal pulse also triggers this power-down. The prescaler reference and the oscillator input buffer are unaffected by the internal reset pulse, thereby maintaining close phase alignment when counting resumes.

When the first N counter data is latched after initialization, the internal reset pulse is reactivated. However, successive AB counter loads after this do not trigger the internal reset pulse.

Device Programming After Initial Power-Up

After initially powering up the device, there are three ways to program the device.

Initialization Latch Method

1. Apply V_{DD}.
2. Program the initialization latch (11 in two LSBs of input word). Make sure that the F1 bit is programmed to 0.
3. Conduct a function latch load (10 in two LSBs of the control word). Make sure that the F1 bit is programmed to 0.
4. Perform an R load (00 in two LSBs).
5. Perform an N load (01 in two LSBs).

When the initialization latch is loaded, the following occurs:

- The function latch contents are loaded.
- An internal pulse resets the R, N, and timeout counters to load state conditions and three-states the charge pump. Note that the prescaler band gap reference and the oscillator input buffer are unaffected by the internal reset pulse, allowing close phase alignment when counting resumes.
- Latching the first N counter data after the initialization word activates the same internal reset pulse. Successive N loads do not trigger the internal reset pulse unless there is another initialization.

CE Pin Method

1. Apply V_{DD}.
2. Bring CE low to put the device into power-down. This is an asynchronous power-down because it happens immediately.
3. Program the function latch (10).
4. Program the R counter latch (00).
5. Program the N counter latch (01).
6. Bring CE high to take the device out of power-down. The R and N counters resume counting in close alignment. Note that after CE goes high, a duration of 1 µs can be required for the prescaler band gap voltage and oscillator input buffer bias to reach steady state.

CE can be used to power the device up and down to check for channel activity. The input register does not need to be reprogrammed each time the device is disabled and enabled, as long as it has been programmed at least once after V_{DD} was initially applied.

Counter Reset Method

1. Apply V_{DD}.
2. Do a function latch load (10 in two LSBs). As part of this step, load 1 to the F1 bit. This enables the counter reset.
3. Perform an R counter load (00 in two LSBs).
4. Perform an N counter load (01 in two LSBs).
5. Do a function latch load (10 in two LSBs). As part of this step, load 0 to the F1 bit. This disables the counter reset.

This sequence provides the same close alignment as the initialization method. It offers direct control over the internal reset. Note that counter reset holds the counters at load point and three-states the charge pump, but does not trigger synchronous power-down.

APPLICATIONS

VERY LOW JITTER ENCODE CLOCK FOR HIGH SPEED CONVERTERS

Figure 20 shows the ADF4002 with a VCXO to provide the encode clock for a high speed analog-to-digital converter (ADC).

The converter used in this application is an AD9215-80, a 12-bit converter that accepts up to an 80 MHz encode clock. To realize a stable low jitter clock, use a 77.76 MHz, narrow band VCXO. This example assumes a 19.44 MHz reference clock.

To minimize the phase noise contribution of the ADF4002, the smallest multiplication factor of 4 is used. Thus, the R divider is programmed to 1, and the N divider is programmed to 4.

The charge pump output of the ADF4002 (Pin 2) drives the loop filter. The loop filter bandwidth is optimized for the best possible rms jitter, a key factor in the signal-to-noise ratio (SNR) of the ADC. Too narrow a bandwidth allows the VCXO noise to dominate at small offsets from the carrier frequency. Too wide a bandwidth allows the ADF4002 noise to dominate at offsets where the VCXO noise is lower than the ADF4002 noise. Thus, the intersection of the VCXO noise and the ADF4002 in-band noise is chosen as the optimum loop filter bandwidth.

The design of the loop filter uses the ADIsimPLL (Version 3.0) and is available as a free download from www.analog.com/pll. The rms jitter is measured at <1.2 ps. This level is lower than the maximum allowable 6 ps rms required to ensure the theoretical SNR performance of 59 dB for this converter.

The setup shown in Figure 20 using the ADF4002, AD9215, and HSC-ADC-EVALA-SC allows the user to quickly and effectively determine the suitability of the converter and encode clock. The SPI® interface is used to control the ADF4002, and the USB interface helps control the operation of the AD9215-80. The controller board sends back FFT information to the PC that, if using an ADC analyzer, provides all conversion results from the ADC.

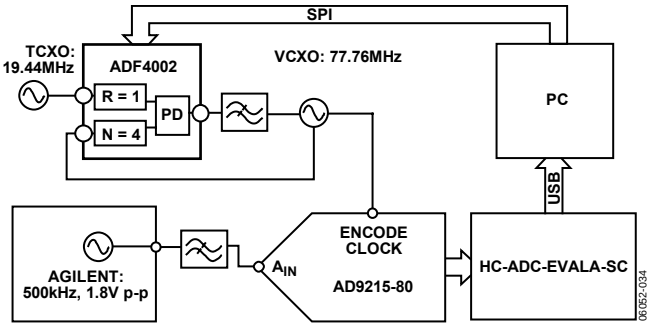

Figure 20. ADF4002 as Encode Clock

PFD

As the ADF4002 permits both R and N counters to be programmed to 1, the part can effectively be used as a standalone PFD and charge pump. This is particularly useful in either a clock cleaning application or a high performance LO. Additionally, the very low normalized phase noise floor (−222 dBc/Hz) enables very low in-band phase noise levels. It is possible to operate the PFD up to a maximum frequency of 104 MHz.

In Figure 21, the reference frequency equals the PFD; therefore, R = 1. The charge pump output integrates into a stable control voltage for the VCXO, and the output from the VCXO is divided down to the desired PFD frequency using an external divider.

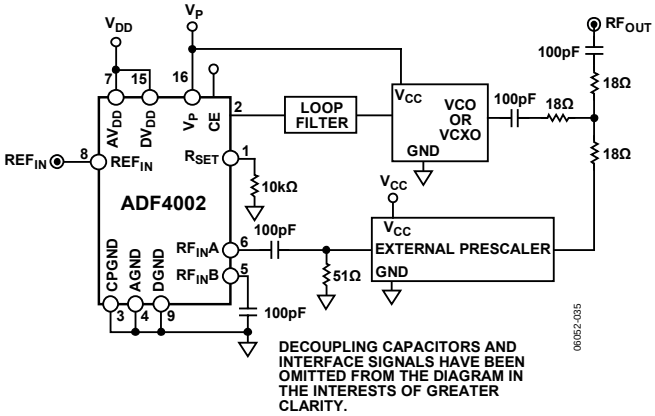

Figure 21. ADF4002 as a PFD

INTERFACING

The ADF4002 has a simple SPI-compatible serial interface for writing to the device. CLK, DATA, and LE control the data transfer. When the latch enable (Pin LE) goes high, the 24 bits that have been clocked into the input register on each rising edge of CLK are transferred to the appropriate latch. For more information, see Figure 2 for the timing diagram and Table 6 for the latch truth table.

The maximum allowable serial clock rate is 20 MHz. This means that the maximum update rate possible for the device is 833 kHz, or one update every 1.2 µs. This is certainly more than adequate for systems that have typical lock times in hundreds of microseconds.

ADuC812 Interface

Figure 22 shows the interface between the ADF4002 and the ADuC812 MicroConverter®. Because the ADuC812 is based on an 8051 core, this interface can be used with any 8051-based microcontroller. The MicroConverter is set up for SPI master mode with CPHA = 0. To initiate the operation, the I/O port driving LE is brought low. Each latch of the ADF4002 needs a 24-bit word. This is accomplished by writing three 8-bit bytes from the MicroConverter to the device. When the third byte has been written, bring the LE input high to complete the transfer.

On first applying power to the ADF4002, it needs four writes (one each to the initialization latch, function latch, R counter latch, and N counter latch) for the output to become active.

I/O port lines on the ADuC812 are also used to control power-down (CE input) and to detect lock (MUXOUT configured as lock detect and polled by the port input).

When operating in the SPI master mode, the maximum SCLOCK rate of the ADuC812 is 4 MHz. This means that the maximum rate at which the output frequency can be changed is 166 kHz.

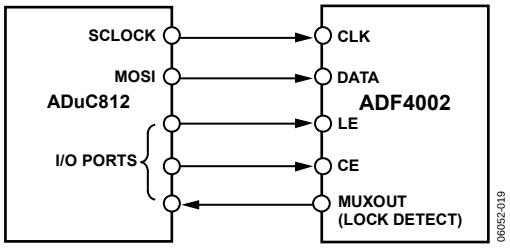

Figure 22. ADuC812 to ADF4002 Interface

ADSP21xx Interface

Figure 23 shows the interface between the ADF4002 and the ADSP21xx digital signal processor. The ADF4002 needs a 24-bit serial word for each latch write. The easiest way to accomplish this using the ADSP21xx family is to use the autobuffered transmit mode of operation with alternate framing. This provides a means for transmitting an entire block of serial data before an interrupt is generated. Set up the word length for eight bits and use three memory locations for each 24-bit word. To program each 24-bit latch, store the three 8-bit bytes, enable the autobuffered mode, and then write to the transmit register of the DSP. This last operation initiates the autobuffer transfer.

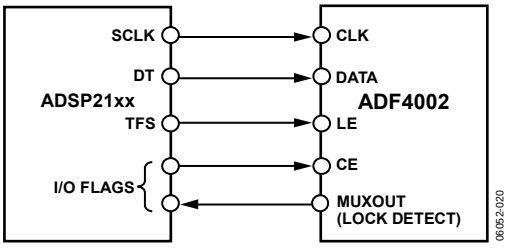

Figure 23. ADSP21xx to ADF4002 Interface

PCB DESIGN GUIDELINES FOR CHIP SCALE PACKAGE

The lands on the lead frame chip scale package (CP-20-1) are rectangular. The printed circuit board pad for these should be 0.1 mm longer than the package land length and 0.05 mm wider than the package land width. The land should be centered on the pad. This ensures that the solder joint size is maximized. The bottom of the lead frame chip scale package has a central thermal pad.

The thermal pad on the printed circuit board should be at least as large as this exposed pad. On the printed circuit board, there should be a clearance of at least 0.25 mm between the thermal pad and the inner edges of the pad pattern. This ensures that shorting is avoided.

Thermal vias can be used on the printed circuit board thermal pad to improve thermal performance of the package. If vias are used, they should be incorporated into the thermal pad at a 1.2 mm pitch grid. The via diameter should be between 0.3 mm and 0.33 mm and the via barrel should be plated with 1 oz copper to plug the via.

The user should connect the printed circuit board thermal pad to AGND.

OUTLINE DIMENSIONS

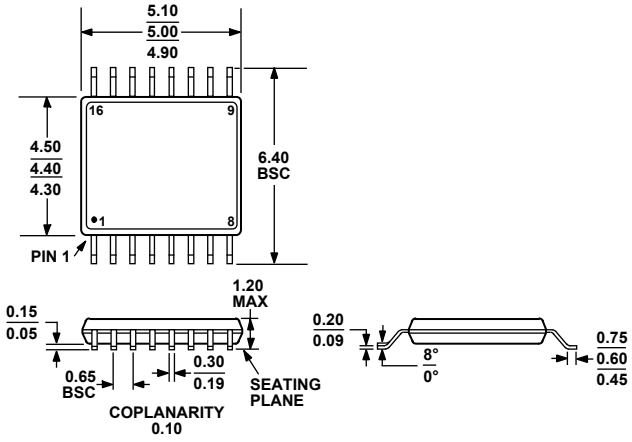

Figure 24. 16-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-16)
Dimensions shown in millimeters

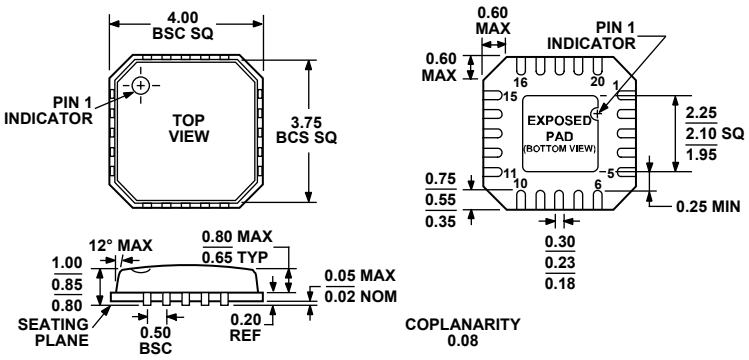

Figure 25. 20-Lead Lead Frame Chip Scale Package [LFCSP_VQ]
(CP-20-1)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
ADF4002BRUZ[1]	−40°C to +85°C	16-Lead TSSOP	RU-16
ADF4002BRUZ-RL[1]	−40°C to +85°C	16-Lead TSSOP	RU-16
ADF4002BRUZ-RL7[1]	−40°C to +85°C	16-Lead TSSOP	RU-16
ADF4002BCPZ[1]	−40°C to +85°C	20-Lead LFCSP_VQ	CP-20-1
ADF4002BCPZ-RL[1]	−40°C to +85°C	20-Lead LFCSP_VQ	CP-20-1
ADF4002BCPZ-RL7[1]	−40°C to +85°C	20-Lead LFCSP_VQ	CP-20-1
EVAL-ADF4002EBZ1[1]		Evaluation Board	
EVAL-ADF411XEBZ1[1]		Evaluation Board	

[1] Z = RoHS Compliant Part.

NOTES

D06052-0-4/07(A)

PLL Frequency Synthesizer

ADF4106

FEATURES

6.0 GHz bandwidth
2.7 V to 3.3 V power supply
Separate charge pump supply (V_P) allows extended tuning voltage in 3 V systems
Programmable dual-modulus prescaler 8/9, 16/17, 32/33, 64/65
Programmable charge pump currents
Programmable antibacklash pulse width
3-wire serial interface
Analog and digital lock detect
Hardware and software power-down mode

APPLICATIONS

Broadband wireless access
Satellite systems
Instrumentation
Wireless LANS
Base stations for wireless radios

GENERAL DESCRIPTION

The ADF4106 frequency synthesizer can be used to implement local oscillators in the up-conversion and down-conversion sections of wireless receivers and transmitters. It consists of a low noise, digital phase frequency detector (PFD), a precision charge pump, a programmable reference divider, programmable A counter and B counter, and a dual-modulus prescaler (P/P + 1). The A (6-bit) counter and B (13-bit) counter, in conjunction with the dual-modulus prescaler (P/P + 1), implement an N divider (N = BP + A). In addition, the 14-bit reference counter (R Counter) allows selectable REF_{IN} frequencies at the PFD input. A complete phase-locked loop (PLL) can be implemented if the synthesizer is used with an external loop filter and voltage controlled oscillator (VCO). Its very high bandwidth means that frequency doublers can be eliminated in many high frequency systems, simplifying system architecture and reducing cost.

FUNCTIONAL BLOCK DIAGRAM

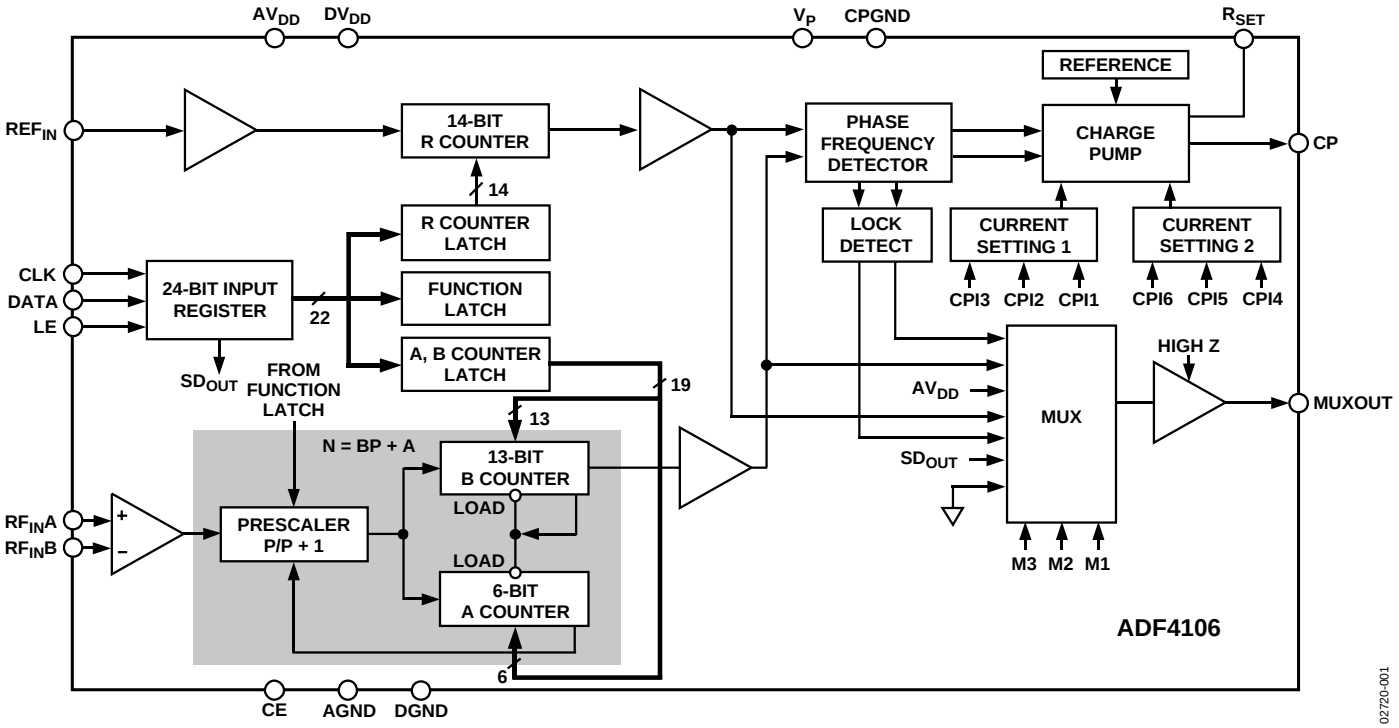

Figure 1.

Rev. B

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SPECIFICATIONS

AV_{DD} = DV_{DD} = 3 V ± 10%, $AV_{DD} \le V_P \le$ 5.5 V, AGND = DGND = CPGND = 0 V, R_{SET} = 5.1 kΩ, dBm referred to 50 Ω, T_A = T_{MAX} to T_{MIN}, unless otherwise noted.

Table 1.

Parameter	B Version[1]	B Chips[2] (typ)	Unit	Test Conditions/Comments
RF CHARACTERISTICS				See Figure 18 for input circuit
RF Input Frequency (RF_{IN})	0.5/6.0	0.5/6.0	GHz min/max	For lower frequencies, ensure slew rate (SR) > 320 V/µs
RF Input Sensitivity	–10/0	–10/0	dBm min/max	
Maximum Allowable Prescaler Output Frequency[3]	300	300	MHz max	P = 8
	325	325	MHz	P = 16
REF_{IN} CHARACTERISTICS				
REF_{IN} Input Frequency	20/300	20/300	MHz min/max	For f < 20 MHz, ensure SR > 50 V/µs
REF_{IN} Input Sensitivity[4]	0.8/V_{DD}	0.8/V_{DD}	V p-p min/max	Biased at AV_{DD}/2 (see Note 5[5])
REF_{IN} Input Capacitance	10	10	pF max	
REF_{IN} Input Current	±100	±100	µA max	
PHASE DETECTOR				
Phase Detector Frequency[6]	104	104	MHz max	ABP = 0, 0 (2.9 ns antibacklash pulse width)
CHARGE PUMP				Programmable, see Table 9
I_{CP} Sink/Source				
High Value	5	5	mA typ	With R_{SET} = 5.1 kΩ
Low Value	625	625	µA typ	
Absolute Accuracy	2.5	2.5	% typ	With R_{SET} = 5.1 kΩ
R_{SET} Range	3.0/11	3.0/11	kΩ typ	See Table 9
I_{CP} Three-State Leakage	2	2	nA max	1 nA typical; T_A = 25°C
Sink and Source Current Matching	2	2	% typ	0.5 V ≤ V_{CP} ≤ V_P – 0.5 V
I_{CP} vs. V_{CP}	1.5	1.5	% typ	0.5 V ≤ V_{CP} ≤ V_P – 0.5 V
I_{CP} vs. Temperature	2	2	% typ	V_{CP} = V_P/2
LOGIC INPUTS				
V_{IH}, Input High Voltage	1.4	1.4	V min	
V_{IL}, Input Low Voltage	0.6	0.6	V max	
I_{INH}, I_{INL}, Input Current	±1	±1	µA max	
C_{IN}, Input Capacitance	10	10	pF max	
LOGIC OUTPUTS				
V_{OH}, Output High Voltage	1.4	1.4	V min	Open-drain output chosen, 1 kΩ pull-up resistor to 1.8 V
V_{OH}, Output High Voltage	V_{DD} – 0.4	V_{DD} – 0.4	V min	CMOS output chosen
I_{OH}	100	100	µA max	
V_{OL}, Output Low Voltage	0.4	0.4	V max	I_{OL} = 500 µA
POWER SUPPLIES				
AV_{DD}	2.7/3.3	2.7/3.3	V min/V max	
DV_{DD}	AV_{DD}	AV_{DD}		
V_P	AV_{DD}/5.5	AV_{DD}/5.5	V min/V max	$AV_{DD} \le V_P \le$ 5.5V
I_{DD}[7] (AI_{DD} + DI_{DD})	11	9.0	mA max	9.0 mA typ
I_{DD}[8] (AI_{DD} + DI_{DD})	11.5	9.5	mA max	9.5 mA typ
I_{DD}[9] (AI_{DD} + DI_{DD})	13	10.5	mA max	10.5 mA typ
I_P	0.4	0.4	mA max	T_A = 25°C
Power-Down Mode[10] (AI_{DD} + DI_{DD})	10	10	µA typ	

Parameter	B Version[1]	B Chips[2] (typ)	Unit	Test Conditions/Comments
NOISE CHARACTERISTICS				
ADF4106 Normalized Phase Noise Floor[11]	–219	–219	dBc/Hz typ	
Phase Noise Performance[12]				@ VCO output
900 MHz[13]	–92.5	–92.5	dBc/Hz typ	@ 1 kHz offset and 200 kHz PFD frequency
5800 MHz[14]	–76.5	–76.5	dBc/Hz typ	@ 1 kHz offset and 200 kHz PFD frequency
5800 MHz[15]	–83.5	–83.5	dBc/Hz typ	@ 1 kHz offset and 1 MHz PFD frequency
Spurious Signals				
900 MHz[13]	–90/–92	–90/–92	dBc typ	@ 200 kHz/400 kHz and 200 kHz PFD frequency
5800 MHz[14]	–65/–70	–65/–70	dBc typ	@ 200 kHz/400 kHz and 200 kHz PFD frequency
5800 MHz[15]	–70/–75	–70/–75	dBc typ	@ 1 MHz/2 MHz and 1 MHz PFD frequency

[1] Operating temperature range (B Version) is –40°C to +85°C.
[2] The B chip specifications are given as typical values.
[3] This is the maximum operating frequency of the CMOS counters. The prescaler value should be chosen to ensure that the RF input is divided down to a frequency that is less than this value.
[4] $AV_{DD} = DV_{DD} = 3$ V.
[5] AC coupling ensures $AV_{DD}/2$ bias.
[6] Guaranteed by design. Sample tested to ensure compliance.
[7] $T_A = 25°C$; $AV_{DD} = DV_{DD} = 3$ V; P = 16; $RF_{IN} = 900$ MHz.
[8] $T_A = 25°C$; $AV_{DD} = DV_{DD} = 3$ V; P = 16; $RF_{IN} = 2.0$ GHz.
[9] $T_A = 25°C$; $AV_{DD} = DV_{DD} = 3$ V; P = 32; $RF_{IN} = 6.0$ GHz.
[10] $T_A = 25°C$; $AV_{DD} = DV_{DD} = 3.3$ V; R = 16383; A = 63; B = 891; P = 32; $RF_{IN} = 6.0$ GHz.
[11] The synthesizer phase noise floor is estimated by measuring the in-band phase noise at the output of the VCO and subtracting 20 log N (where N is the N divider value) and 10 log F_{PFD}. $PN_{SYNTH} = PN_{TOT} - 10 \log F_{PFD} - 20 \log N$.
[12] The phase noise is measured with the EVAL-ADF4106EB1 evaluation board and the Agilent E4440A Spectrum Analyzer. The spectrum analyzer provides the REFIN for the synthesizer (f_{REFOUT} = 10 MHz @ 0 dBm).
[13] $f_{REFIN} = 10$ MHz; $f_{PFD} = 200$ kHz; Offset Frequency = 1 kHz; $f_{RF} = 900$ MHz; N = 4500; Loop B/W = 20 kHz.
[14] $f_{REFIN} = 10$ MHz; $f_{PFD} = 200$ kHz; Offset Frequency = 1 kHz; $f_{RF} = 5800$ MHz; N = 29000; Loop B/W = 20 kHz.
[15] $f_{REFIN} = 10$ MHz; $f_{PFD} = 1$ MHz; Offset Frequency = 1 kHz; $f_{RF} = 5800$ MHz; N = 5800; Loop B/W = 100 kHz.

TIMING CHARACTERISITICS

$AV_{DD} = DV_{DD} = 3$ V ± 10%, $AV_{DD} \le V_P \le 5.5$ V, AGND = DGND = CPGND = 0 V, $R_{SET} = 5.1$ kΩ, dBm referred to 50 Ω, $T_A = T_{MAX}$ to T_{MIN}, unless otherwise noted.

Table 2.

Parameter	Limit[1] (B Version)	Unit	Test Conditions/Comments
t_1	10	ns min	DATA to CLOCK Setup Time
t_2	10	ns min	DATA to CLOCK Hold Time
t_3	25	ns min	CLOCK High Duration
t_4	25	ns min	CLOCK Low Duration
t_5	10	ns min	CLOCK to LE Setup Time
t_6	20	ns min	LE Pulse Width

[1] Operating temperature range (B Version) is –40°C to +85°C.

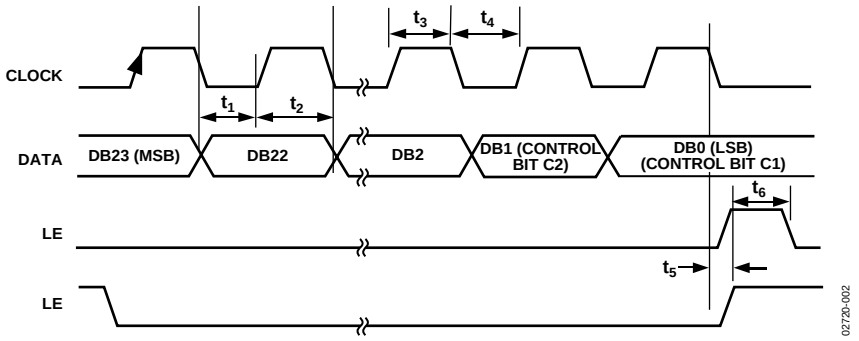

Figure 2. Timing Diagram

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 3.

Parameter	Rating
AV_{DD} to GND[1]	–0.3 V to + 3.6 V
AV_{DD} to DV_{DD}	–0.3 V to + 0.3 V
V_P to GND	–0.3 V to + 5.8 V
V_P to AV_{DD}	–0.3 V to + 5.8 V
Digital I/O Voltage to GND	–0.3 V to V_{DD} + 0.3 V
Analog I/O Voltage to GND	–0.3 V to V_P + 0.3 V
REF_{IN}, $RF_{IN}A$, $RF_{IN}B$ to GND	–0.3 V to V_{DD} + 0.3 V
Operating Temperature Range	
Industrial (B Version)	–40°C to +85°C
Storage Temperature Range	–65°C to +125°C
Maximum Junction Temperature	150°C
TSSOP θ_{JA} Thermal Impedance	112°C/W
LFCSP θ_{JA} Thermal Impedance (Paddle Soldered)	30.4°C/W
Reflow Soldering	
Peak Temperature	260°C
Time at Peak Temperature	40 sec
Transistor Count	
CMOS	6425
Bipolar	303

[1]GND = AGND = DGND = 0 V.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device is a high performance RF integrated circuit with an ESD rating of <2 kV, and it is ESD sensitive. Proper precautions should be taken for handling and assembly.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

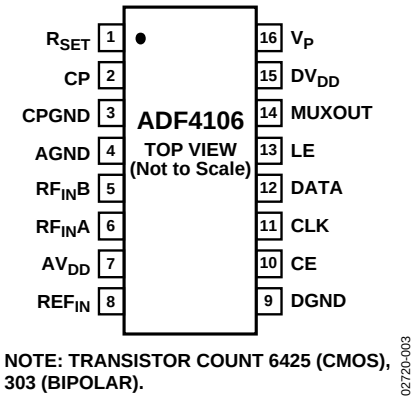

Figure 3. 16-Lead TSSOP Pin Configuration

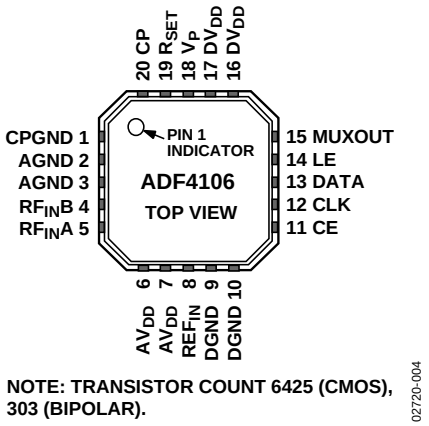

Figure 4. 20-Lead LFCSP_VQ Pin Configuration

Table 4. Pin Function Descriptions

Pin No. TSSOP	Pin No. LFCSP	Mnemonic	Function
1	19	R_{SET}	Connecting a resistor between this pin and CPGND sets the maximum charge pump output current. The nominal voltage potential at the R_{SET} pin is 0.66 V. The relationship between I_{CP} and R_{SET} is $I_{CP\,MAX} = \frac{25.5}{R_{SET}}$ So, with R_{SET} = 5.1 kΩ, $I_{CP\,MAX}$ = 5 mA.
2	20	CP	Charge Pump Output. When enabled, this provides ±I_{CP} to the external loop filter, which in turn drives the external VCO.
3	1	CPGND	Charge Pump Ground. This is the ground return path for the charge pump.
4	2, 3	AGND	Analog Ground. This is the ground return path of the prescaler.
5	4	$RF_{IN}B$	Complementary Input to the RF Prescaler. This point must be decoupled to the ground plane with a small bypass capacitor, typically 100 pF. See Figure 18.
6	5	$RF_{IN}A$	Input to the RF Prescaler. This small signal input is ac-coupled to the external VCO.
7	6, 7	AV_{DD}	Analog Power Supply. This may range from 2.7 V to 3.3 V. Decoupling capacitors to the analog ground plane should be placed as close as possible to this pin. AV_{DD} must be the same value as DV_{DD}.
8	8	REF_{IN}	Reference Input. This is a CMOS input with a nominal threshold of V_{DD}/2 and a dc equivalent input resistance of 100 kΩ. See Figure 18. This input can be driven from a TTL or CMOS crystal oscillator or it can be ac-coupled.
9	9, 10	DGND	Digital Ground.
10	11	CE	Chip Enable. A logic low on this pin powers down the device and puts the charge pump output into three-state mode. Taking the pin high powers up the device, depending on the status of the power-down bit, F2.
11	12	CLK	Serial Clock Input. This serial clock is used to clock in the serial data to the registers. The data is latched into the 24-bit shift register on the CLK rising edge. This input is a high impedance CMOS input.
12	13	DATA	Serial Data Input. The serial data is loaded MSB first with the two LSBs being the control bits. This input is a high impedance CMOS input.
13	14	LE	Load Enable, CMOS Input. When LE goes high, the data stored in the shift registers is loaded into one of the four latches with the latch being selected using the control bits.
14	15	MUXOUT	This multiplexer output allows either the lock detect, the scaled RF, or the scaled reference frequency to be accessed externally.
15	16, 17	DV_{DD}	Digital Power Supply. This may range from 2.7 V to 3.3 V. Decoupling capacitors to the digital ground plane should be placed as close as possible to this pin. DV_{DD} must be the same value as AV_{DD}.
16	18	V_P	Charge Pump Power Supply. This should be greater than or equal to V_{DD}. In systems where V_{DD} is 3 V, it can be set to 5.5 V and used to drive a VCO with a tuning range of up to 5 V.

TYPICAL PERFORMANCE CHARACTERISTICS

FREQ UNIT GHz KEYWORD R
PARAM TYPE S IMPEDANCE 50Ω
DATA FORMAT MA

FREQ	MAGS11	ANGS11	FREQ	MAGS11	ANGS11
0.500	0.89148	–17.2820	3.300	0.42777	–102.748
0.600	0.88133	– 20.6919	3.400	0.42859	–107.167
0.700	0.87152	– 24.5386	3.500	0.43365	–111.883
0.800	0.85855	–27.3228	3.600	0.43849	–117.548
0.900	0.84911	–31.0698	3.700	0.44475	–123.856
1.000	0.83512	– 34.8623	3.800	0.44800	–130.399
1.100	0.82374	–38.5574	3.900	0.45223	–136.744
1.200	0.80871	–41.9093	4.000	0.45555	–142.766
1.300	0.79176	– 45.6990	4.100	0.45313	–149.269
1.400	0.77205	–49.4185	4.200	0.45622	–154.884
1.500	0.75696	–52.8898	4.300	0.45555	–159.680
1.600	0.74234	–56.2923	4.400	0.46108	–164.916
1.700	0.72239	–60.2584	4.500	0.45325	–168.452
1.800	0.69419	–63.1446	4.600	0.45054	–173.462
1.900	0.67288	–65.6464	4.700	0.45200	–176.697
2.000	0.66227	–68.0742	4.800	0.45043	178.824
2.100	0.64758	–71.3530	4.900	0.45282	174.947
2.200	0.62454	–75.5658	5.000	0.44287	170.237
2.300	0.59466	–79.6404	5.100	0.44909	166.617
2.400	0.55932	–82.8246	5.200	0.44294	162.786
2.500	0.52256	–85.2795	5.300	0.44558	158.766
2.600	0.48754	–85.6298	5.400	0.45417	153.195
2.700	0.46411	–86.1854	5.500	0.46038	147.721
2.800	0.45776	–86.4997	5.600	0.47128	139.760
2.900	0.44859	–88.8080	5.700	0.47439	132.657
3.000	0.44588	–91.9737	5.800	0.48604	125.782
3.100	0.43810	–95.4087	5.900	0.50637	121.110
3.200	0.43269	–99.1282	6.000	0.52172	115.400

02720-005

Figure 5. S-Parameter Data for the RF Input

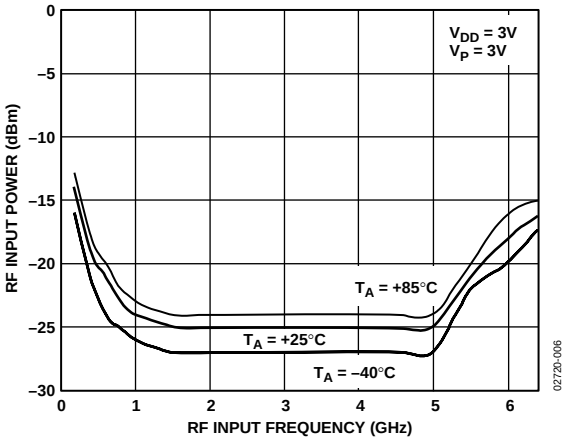

Figure 6. Input Sensitivity

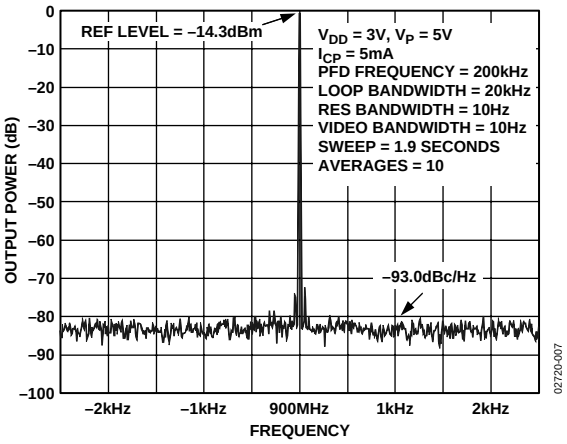

Figure 7. Phase Noise (900 MHz, 200 kHz, and 20 kHz)

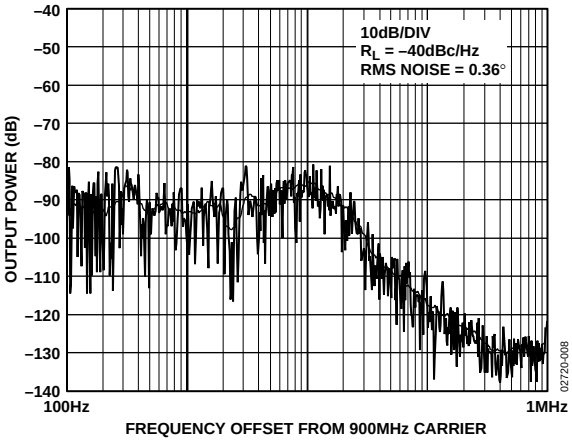

Figure 8. Integrated Phase Noise (900 MHz, 200 kHz, and 20 kHz)

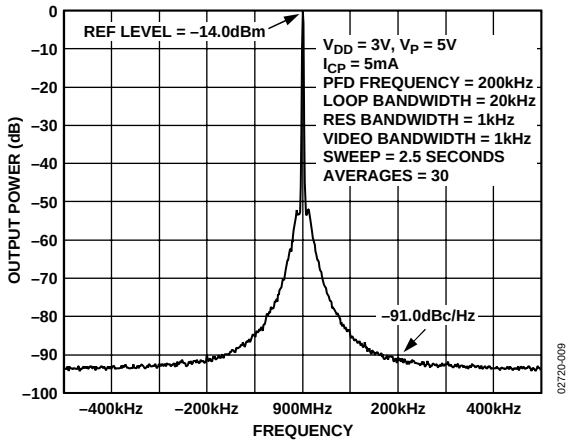

Figure 9. Reference Spurs (900 MHz, 200 kHz, and 20 kHz)

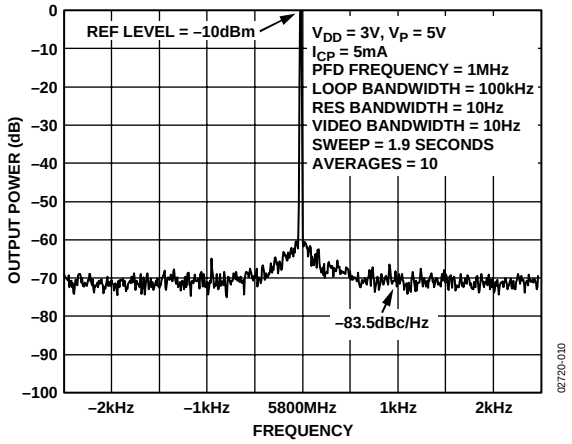

Figure 10. Phase Noise (5.8 GHz,1 MHz, and 100 kHz)

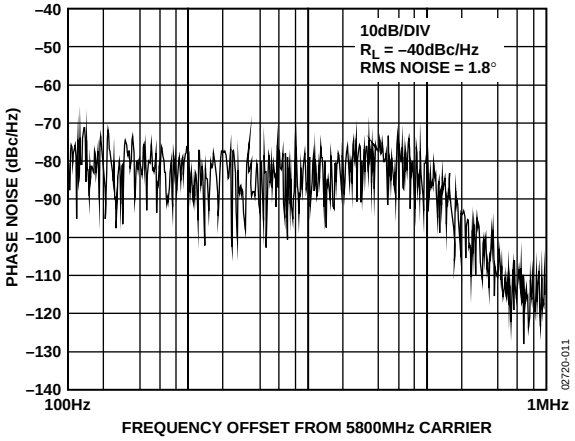

Figure 11. Integrated Phase Noise (5.8 GHz,1 MHz, and 100 kHz)

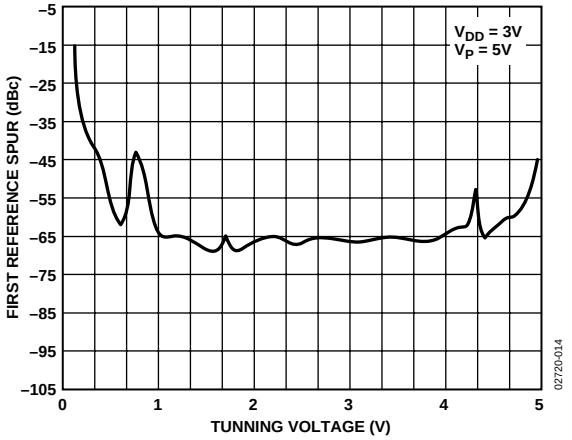

Figure 14. Reference Spurs vs. V_{TUNE} (5.8 GHz,1 MHz, and 100 kHz)

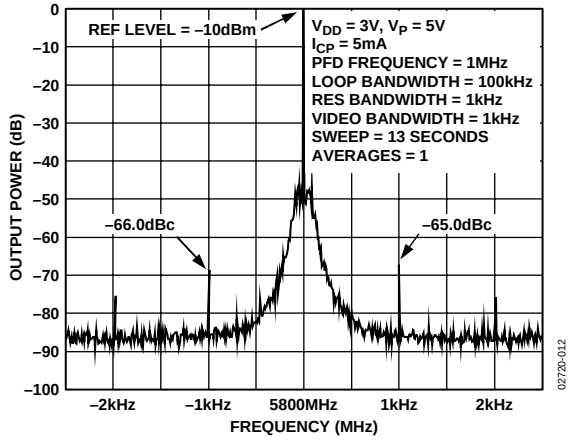

Figure 12. Reference Spurs (5.8 GHz,1 MHz, and 100 kHz)

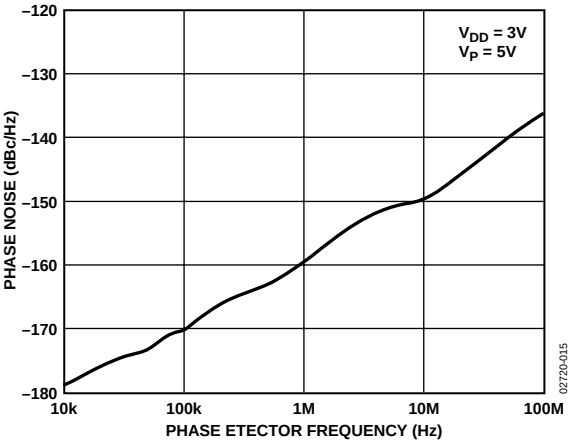

Figure 15. Phase Noise (Referred to CP Output) vs. PFD Frequency

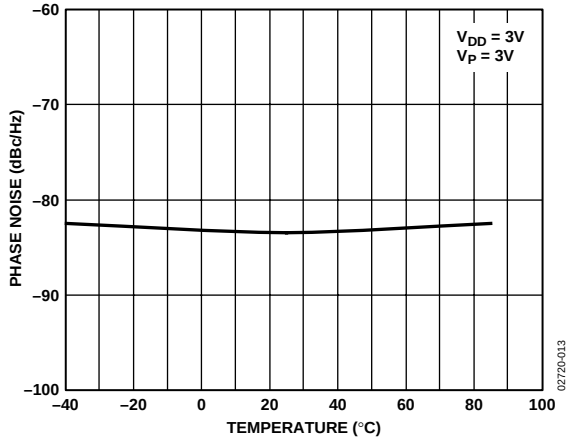

Figure 13. Phase Noise (5.8 GHz,1 MHz, and 100 kHz) vs. Temperature

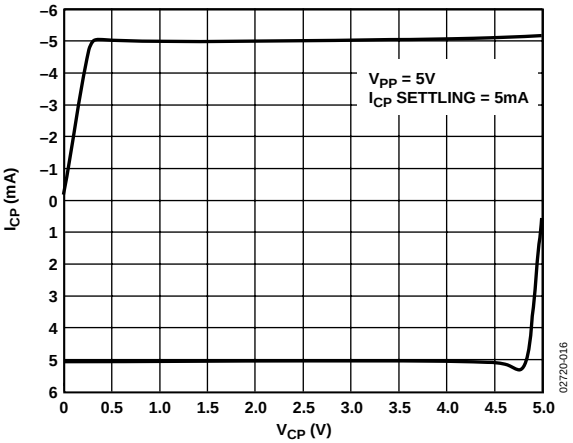

Figure 16. Charge Pump Output Characteristics

GENERAL DESCRIPTION

REFERENCE INPUT SECTION

The reference input stage is shown in Figure 17. SW1 and SW2 are normally closed switches. SW3 is a normally open switch. When power-down is initiated, SW3 is closed and SW1 and SW2 are opened. This ensures that there is no loading of the REF_{IN} pin on power-down.

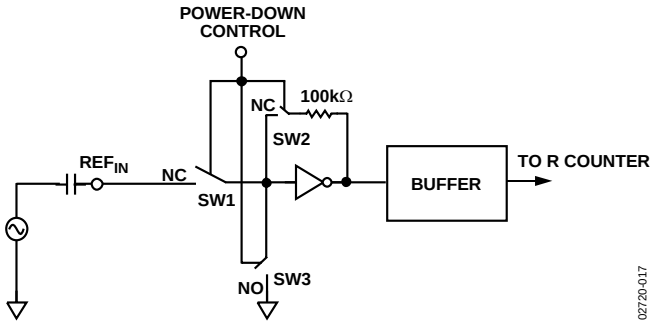

Figure 17. Reference Input Stage

RF INPUT STAGE

The RF input stage is shown in Figure 18. It is followed by a 2-stage limiting amplifier to generate the CML clock levels needed for the prescaler.

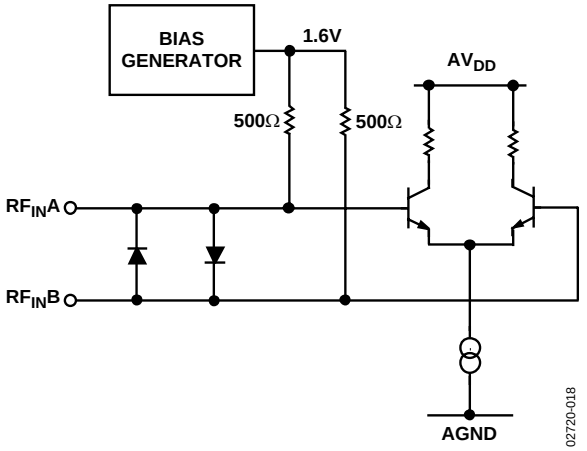

Figure 18. RF Input Stage

PRESCALER (P/P +1)

The dual-modulus prescaler (P/P + 1), along with the A counter and B counter, enables the large division ratio, N, to be realized (N = BP + A). The dual-modulus prescaler, operating at CML levels, takes the clock from the RF input stage and divides it down to a manageable frequency for the CMOS A counter and B counter. The prescaler is programmable. It can be set in software to 8/9, 16/17, 32/33, or 64/65. It is based on a synchronous 4/5 core. There is a minimum divide ratio possible for fully contiguous output frequencies. This minimum is determined by P, the prescaler value, and is given by ($P^2 - P$).

A COUNTER AND B COUNTER

The A counter and B CMOS counter combine with the dual modulus prescaler to allow a wide ranging division ratio in the PLL feedback counter. The counters are specified to work when the prescaler output is 325 MHz or less. Thus, with an RF input frequency of 4.0 GHz, a prescaler value of 16/17 is valid, but a value of 8/9 is not valid.

Pulse Swallow Function

The A counter and B counter, in conjunction with the dual-modulus prescaler, make it possible to generate output frequencies that are spaced only by the reference frequency divided by R. The equation for the VCO frequency is

$$f_{VCO} = \left[\left(P \times B\right) + A\right] \times \frac{f_{REFIN}}{R}$$

where:

f_{VCO} is the output frequency of the external voltage controlled oscillator (VCO).

P is the preset modulus of the dual-modulus prescaler (8/9, 16/17, etc.).

B is the preset divide ratio of the binary 13-bit counter (3 to 8191).

A is the preset divide ratio of the binary 6-bit swallow counter (0 to 63).

f_{REFIN} is the external reference frequency oscillator.

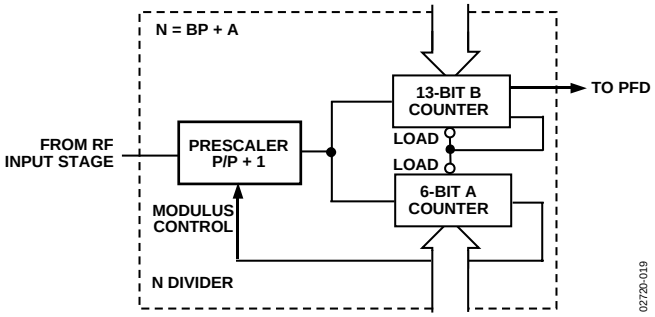

Figure 19. A and B Counters

R COUNTER

The 14-bit R counter allows the input reference frequency to be divided down to produce the reference clock to the phase frequency detector (PFD). Division ratios from 1 to 16,383 are allowed.

PHASE FREQUENCY DETECTOR (PFD) AND CHARGE PUMP

The PFD takes inputs from the R counter and N counter (N = BP + A) and produces an output proportional to the phase and frequency difference between them. Figure 20 is a simplified schematic. The PFD includes a programmable delay element that controls the width of the antibacklash pulse. This pulse ensures that there is no dead zone in the PFD transfer function and minimizes phase noise and reference spurs. Two bits in the reference counter latch, ABP2 and ABP1, control the width of the pulse. See Table 7.

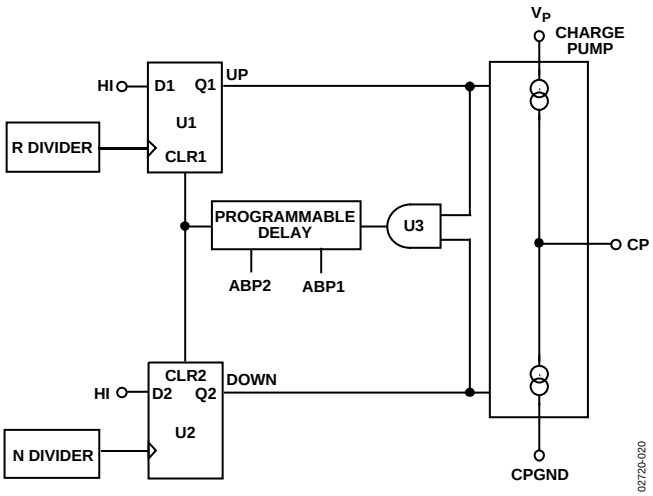

Figure 20. PFD Simplified Schematic

MUXOUT AND LOCK DETECT

The output multiplexer on the ADF4106 allows the user to access various internal points on the chip. The state of MUXOUT is controlled by M3, M2, and M1 in the function latch. Table 9 shows the full truth table. Figure 21 shows the MUXOUT section in block diagram form.

Lock Detect

MUXOUT can be programmed for two types of lock detect: digital lock detect and analog lock detect.

Digital lock detect is active high. When LDP in the R counter latch is set to 0, digital lock detect is set high when the phase error on three consecutive phase detector cycles is less than 15 ns. With LDP set to 1, five consecutive cycles of less than 15 ns are required to set the lock detect. It stays set high until a phase error of greater than 25 ns is detected on any subsequent PD cycle.

The N-channel, open-drain, analog lock detect should be operated with an external pull-up resistor of 10 kΩ nominal. When lock is detected, this output is high with narrow, low-going pulses.

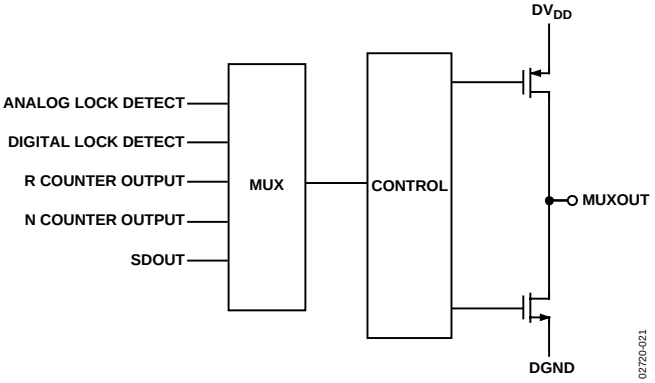

Figure 21. MUXOUT Circuit

INPUT SHIFT REGISTER

The ADF4106 digital section includes a 24-bit input shift register, a 14-bit R counter, and a 19-bit N counter, comprising a 6-bit A counter and a 13-bit B counter. Data is clocked into the 24-bit shift register on each rising edge of CLK. The data is clocked in MSB first. Data is transferred from the shift register to one of four latches on the rising edge of LE. The destination latch is determined by the state of the two control bits (C2, C1) in the shift register. These are the two LSBs, DB1 and DB0, as shown in the timing diagram of Figure 2. The truth table for these bits is shown in Table 5. Table 6 shows a summary of how the latches are programmed.

Table 5. C1, C2 Truth Table

Control Bits		
C2	**C1**	**Data Latch**
0	0	R Counter
0	1	N Counter (A and B)
1	0	Function Latch (Including Prescaler)
1	1	Initialization Latch

Table 6. Latch Summary

REFERENCE COUNTER LATCH

RESERVED			LOCK DETECT PRECISION	TEST MODE BITS		ANTI-BACKLASH WIDTH		14-BIT REFERENCE COUNTER													CONTROL BITS	
DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
X	0	0	LDP	T2	T1	ABP2	ABP1	R14	R13	R12	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	C2 (0)	C1 (0)

N COUNTER LATCH

RESERVED		CP GAIN	13-BIT B COUNTER													6-BIT A COUNTER						CONTROL BITS	
DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
X	X	G1	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	A6	A5	A4	A3	A2	A1	C2 (0)	C1 (1)

FUNCTION LATCH

PRESCALER VALUE		POWER-DOWN 2	CURRENT SETTING 2			CURRENT SETTING 1			TIMER COUNTER CONTROL				FASTLOCK MODE	FASTLOCK ENABLE	CP THREE-STATE	PD POLARITY	MUXOUT CONTROL			POWER-DOWN 1	COUNTER RESET	CONTROL BITS	
DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
P2	P1	PD2	CPI6	CPI5	CPI4	CPI3	CPI2	CPI1	TC4	TC3	TC2	TC1	F5	F4	F3	F2	M3	M2	M1	PD1	F1	C2 (1)	C1 (0)

INITIALIZATION LATCH

PRESCALER VALUE		POWER-DOWN 2	CURRENT SETTING 2			CURRENT SETTING 1			TIMER COUNTER CONTROL				FASTLOCK MODE	FASTLOCK ENABLE	CP THREE-STATE	PD POLARITY	MUXOUT CONTROL			POWER-DOWN 1	COUNTER RESET	CONTROL BITS	
DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
P2	P1	PD2	CPI6	CPI5	CPI4	CPI3	CPI2	CPI1	TC4	TC3	TC2	TC1	F5	F4	F3	F2	M3	M2	M1	PD1	F1	C2 (1)	C1 (1)

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Table 7. Reference Counter Latch Map

RESERVED			LOCK DETECT PRECISION	TEST MODE BITS		ANTI-BACKLASH WIDTH		14-BIT REFERENCE COUNTER												CONTROL BITS	
DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
X	0	0	LDP	T2	T1	ABP2	ABP1	R14	R13	R12	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	C2 (0)	C1 (0)

X = DON'T CARE

R14	R13	R12	.....	R3	R2	R1	DIVIDE RATIO
0	0	0	.....	0	0	1	1
0	0	0	.....	0	1	0	2
0	0	0	.....	0	1	1	3
0	0	0	.....	1	0	0	4
.	.	.	.....	.	.	.	.
.	.	.	.....	.	.	.	.
.	.	.	.....	.	.	.	.
1	1	1	.....	1	0	0	16380
1	1	1	.....	1	0	1	16381
1	1	1	.....	1	1	0	16382
1	1	1	.....	1	1	1	16383

ABP2	ABP1	ANTIBACKLASH PULSE WIDTH
0	0	2.9ns
0	1	1.3ns
1	0	6.0ns
1	1	2.9ns

TEST MODE BITS SHOULD BE SET TO 00 FOR NORMAL OPERATION.

LDP	OPERATION
0	THREE CONSECUTIVE CYCLES OF PHASE DELAY LESS THAN 15ns MUST OCCUR BEFORE LOCK DETECT IS SET.
1	FIVE CONSECUTIVE CYCLES OF PHASE DELAY LESS THAN 15ns MUST OCCUR BEFORE LOCK DETECT IS SET.

BOTH OF THESE BITS MUST BE SET TO 0 FOR NORMAL OPERATION.

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Table 8. N (A, B) Counter Latch Map

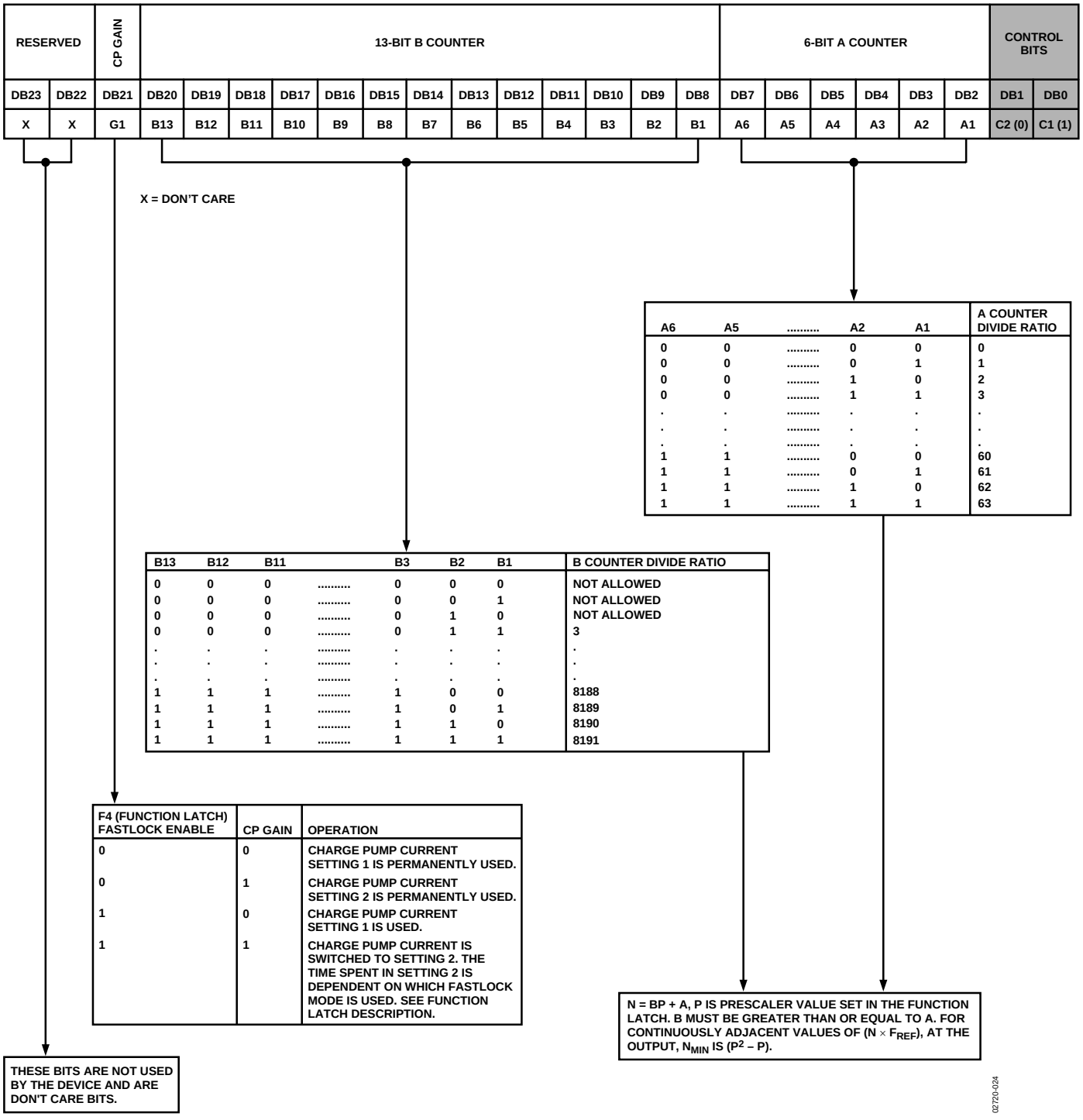
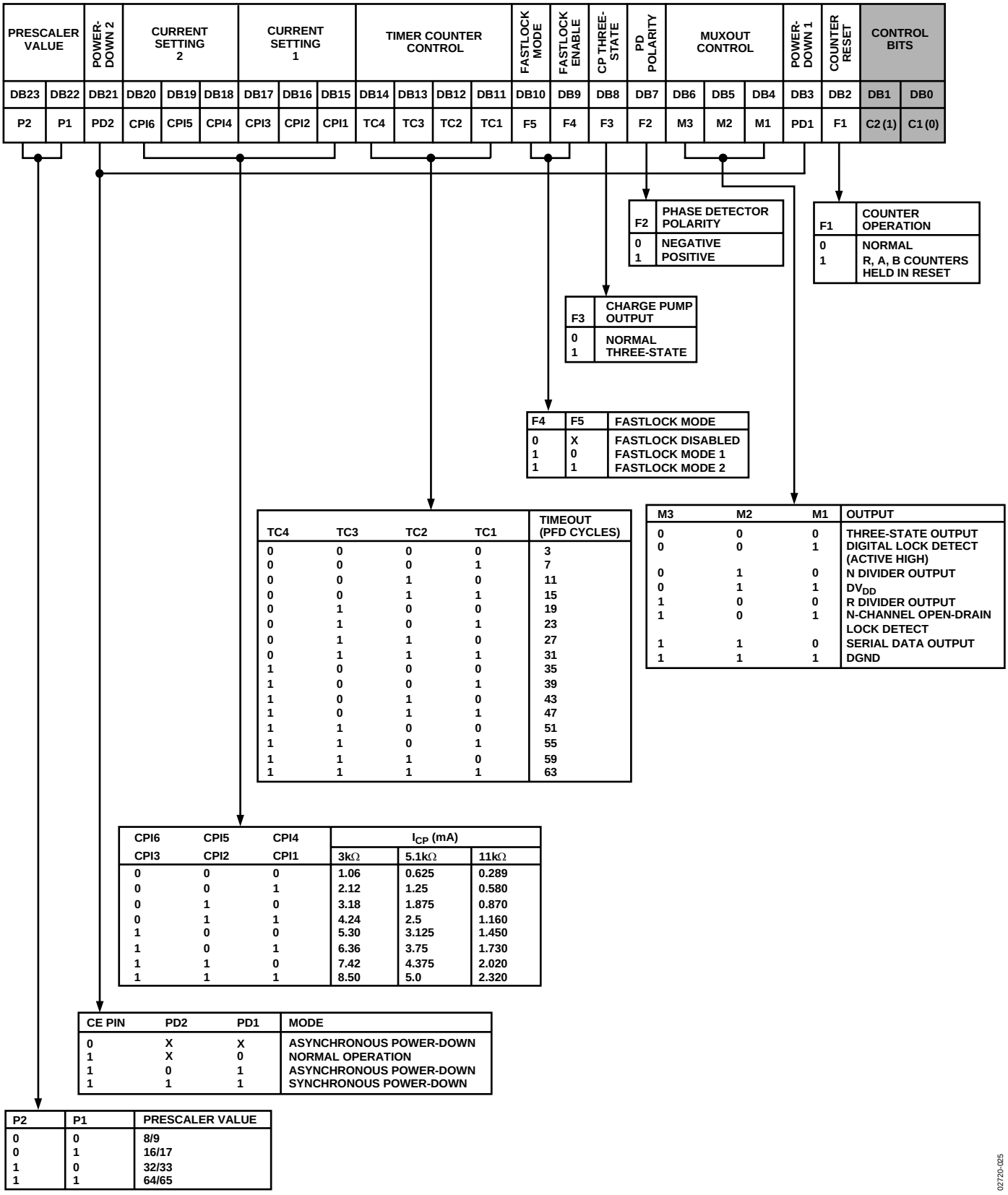


Table 9. Function Latch Map

PRESCALER VALUE		POWER-DOWN 2	CURRENT SETTING 2			CURRENT SETTING 1			TIMER COUNTER CONTROL				FASTLOCK MODE	FASTLOCK ENABLE	CP THREE-STATE	PD POLARITY	MUXOUT CONTROL			POWER-DOWN 1	COUNTER RESET	CONTROL BITS	
DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
P2	P1	PD2	CPI6	CPI5	CPI4	CPI3	CPI2	CPI1	TC4	TC3	TC2	TC1	F5	F4	F3	F2	M3	M2	M1	PD1	F1	C2 (1)	C1 (0)



F2	PHASE DETECTOR POLARITY
0	NEGATIVE
1	POSITIVE

F1	COUNTER OPERATION
0	NORMAL
1	R, A, B COUNTERS HELD IN RESET

F3	CHARGE PUMP OUTPUT
0	NORMAL
1	THREE-STATE

F4	F5	FASTLOCK MODE
0	X	FASTLOCK DISABLED
1	0	FASTLOCK MODE 1
1	1	FASTLOCK MODE 2

TC4	TC3	TC2	TC1	TIMEOUT (PFD CYCLES)
0	0	0	0	3
0	0	0	1	7
0	0	1	0	11
0	0	1	1	15
0	1	0	0	19
0	1	0	1	23
0	1	1	0	27
0	1	1	1	31
1	0	0	0	35
1	0	0	1	39
1	0	1	0	43
1	0	1	1	47
1	1	0	0	51
1	1	0	1	55
1	1	1	0	59
1	1	1	1	63

M3	M2	M1	OUTPUT
0	0	0	THREE-STATE OUTPUT
0	0	1	DIGITAL LOCK DETECT (ACTIVE HIGH)
0	1	0	N DIVIDER OUTPUT
0	1	1	DV_{DD}
1	0	0	R DIVIDER OUTPUT
1	0	1	N-CHANNEL OPEN-DRAIN LOCK DETECT
1	1	0	SERIAL DATA OUTPUT
1	1	1	DGND

CPI6 CPI3	CPI5 CPI2	CPI4 CPI1	I_{CP} (mA) 3kΩ	5.1kΩ	11kΩ
0	0	0	1.06	0.625	0.289
0	0	1	2.12	1.25	0.580
0	1	0	3.18	1.875	0.870
0	1	1	4.24	2.5	1.160
1	0	0	5.30	3.125	1.450
1	0	1	6.36	3.75	1.730
1	1	0	7.42	4.375	2.020
1	1	1	8.50	5.0	2.320

CE PIN	PD2	PD1	MODE
0	X	X	ASYNCHRONOUS POWER-DOWN
1	X	0	NORMAL OPERATION
1	0	1	ASYNCHRONOUS POWER-DOWN
1	1	1	SYNCHRONOUS POWER-DOWN

P2	P1	PRESCALER VALUE
0	0	8/9
0	1	16/17
1	0	32/33
1	1	64/65

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Table 10. Initialization Latch Map

PRESCALER VALUE		POWER-DOWN 2	CURRENT SETTING 2			CURRENT SETTING 1			TIMER COUNTER CONTROL				FASTLOCK MODE	FASTLOCK ENABLE	CP THREE-STATE	PD POLARITY	MUXOUT CONTROL			POWER-DOWN 1	COUNTER RESET	CONTROL BITS	
DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
P2	P1	PD2	CPI6	CPI5	CPI4	CPI3	CPI2	CPI1	TC4	TC3	TC2	TC1	F5	F4	F3	F2	M3	M2	M1	PD1	F1	C2 (1)	C1 (1)

F2	PHASE DETECTOR POLARITY
0	NEGATIVE
1	POSITIVE

F1	COUNTER OPERATION
0	NORMAL
1	R, A, B COUNTERS HELD IN RESET

F3	CHARGE PUMP OUTPUT
0	NORMAL
1	THREE-STATE

F4	F5	FASTLOCK MODE
0	X	FASTLOCK DISABLED
1	0	FASTLOCK MODE 1
1	1	FASTLOCK MODE 2

TC4	TC3	TC2	TC1	TIMEOUT (PFD CYCLES)
0	0	0	0	3
0	0	0	1	7
0	0	1	0	11
0	0	1	1	15
0	1	0	0	19
0	1	0	1	23
0	1	1	0	27
0	1	1	1	31
1	0	0	0	35
1	0	0	1	39
1	0	1	0	43
1	0	1	1	47
1	1	0	0	51
1	1	0	1	55
1	1	1	0	59
1	1	1	1	63

M3	M2	M1	OUTPUT
0	0	0	THREE-STATE OUTPUT
0	0	1	DIGITAL LOCK DETECT (ACTIVE HIGH)
0	1	0	N DIVIDER OUTPUT
0	1	1	DV_{DD}
1	0	0	R DIVIDER OUTPUT
1	0	1	N-CHANNEL OPEN-DRAIN LOCK DETECT
1	1	0	SERIAL DATA OUTPUT
1	1	1	DGND

CPI6	CPI5	CPI4	I_{CP} (mA)		
CPI3	CPI2	CPI1	3kΩ	5.1kΩ	11kΩ
0	0	0	1.06	0.625	0.289
0	0	1	2.12	1.25	0.580
0	1	0	3.18	1.875	0.870
0	1	1	4.24	2.5	1.160
1	0	0	5.30	3.125	1.450
1	0	1	6.36	3.75	1.730
1	1	0	7.42	4.375	2.020
1	1	1	8.50	5.0	2.320

CE PIN	PD2	PD1	MODE
0	X	X	ASYNCHRONOUS POWER-DOWN
1	X	0	NORMAL OPERATION
1	0	1	ASYNCHRONOUS POWER-DOWN
1	1	1	SYNCHRONOUS POWER-DOWN

P2	P1	PRESCALER VALUE
0	0	8/9
0	1	16/17
1	0	32/33
1	1	64/65

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THE FUNCTION LATCH

With C2 and C1 set to 1 and 0, respectively, the on-chip function latch is programmed. Table 9 shows the input data format for programming the function latch.

Counter Reset

DB2 (F1) is the counter reset bit. When this is 1, the R counter and the N (A, B) counter are reset. For normal operation, this bit should be 0. When powering up, disable the F1 bit (set to 0). The N counter will then resume counting in close alignment with the R counter. (The maximum error is one prescaler cycle).

Power-Down

DB3 (PD1) and DB21 (PD2) provide programmable power-down modes. They are enabled by the CE pin.

When the CE pin is low, the device is immediately disabled regardless of the states of PD2, PD1.

In the programmed asynchronous power-down, the device powers down immediately after latching 1 into the PD1 bit, with the condition that PD2 is loaded with 0.

In the programmed synchronous power-down, the device power-down is gated by the charge pump to prevent unwanted frequency jumps. Once the power-down is enabled by writing 1 into the PD1 bit (provided that 1 has also been loaded to PD2), then the device goes into power-down during the next charge pump event.

When a power-down is activated (either synchronous or asynchronous mode, including CE pin activated power-down), the following events occur:

- All active dc current paths are removed.
- The R, N, and timeout counters are forced to their load state conditions.
- The charge pump is forced into three-state mode.
- The digital clock detect circuitry is reset.
- The RF_{IN} input is debiased.
- The reference input buffer circuitry is disabled.
- The input register remains active and capable of loading and latching data.

MUXOUT Control

The on-chip multiplexer is controlled by M3, M2, and M1 on the ADF4106 family. Table 9 shows the truth table.

Fastlock Enable Bit

DB9 of the function latch is the fastlock enable bit. When this bit is 1, fastlock is enabled.

Fastlock Mode Bit

DB10 of the function latch is the fastlock mode bit. When fastlock is enabled, this bit determines which fastlock mode is used. If the fastlock mode bit is 0, then Fastlock Mode 1 is selected; and if the fastlock mode bit is 1, then Fastlock Mode 2 is selected.

Fastlock Mode 1

The charge pump current is switched to the contents of Current Setting 2. The device enters fastlock when 1 is written to the CP gain bit in the N (A, B) counter latch. The device exits fastlock when 0 is written to the CP gain bit in the N (A, B) counter latch.

Fastlock Mode 2

The charge pump current is switched to the contents of Current Setting 2. The device enters fastlock when 1 is written to the CP gain bit in the N (A, B) counter latch. The device exits fastlock under the control of the timer counter. After the timeout period, which is determined by the value in TC4 to TC1, the CP gain bit in the N (A, B) counter latch is automatically reset to 0, and the device reverts to normal mode instead of fastlock. See Table 9 for the timeout periods.

Timer Counter Control

The user has the option of programming two charge pump currents. The intent is that Current Setting 1 is used when the RF output is stable and the system is in a static state. Current Setting 2 is used when the system is dynamic and in a state of change (that is, when a new output frequency is programmed). The normal sequence of events follows.

The user initially decides what the preferred charge pump currents are going to be. For example, the choice may be 2.5 mA as Current Setting 1 and 5 mA as the Current Setting 2.

Simultaneously, the decision must be made as to how long the secondary current stays active before reverting to the primary current. This is controlled by the timer counter control bits, DB14 to DB11 (TC4 to TC1), in the function latch. The truth table is given in Table 9.

To program a new output frequency, simply program the N (A, B) counter latch with new values for A and B. Simultaneously, the CP gain bit can be set to 1, which sets the charge pump with the value in CPI6 to CPI4 for a period of time determined by TC4 to TC1. When this time is up, the charge pump current reverts to the value set by CPI3 to CPI1. At the same time, the CP gain bit in the N (A, B) counter latch is reset to 0 and is now ready for the next time the user wishes to change the frequency.

Note that there is an enable feature on the timer counter. It is enabled when Fastlock Mode 2 is chosen by setting the fastlock mode bit (DB10) in the function latch to 1.

Charge Pump Currents

CPI3, CPI2, and CPI1 program Current Setting 1 for the charge pump. CPI6, CPI5, and CPI4 program Current Setting 2 for the charge pump. The truth table is given in Table 9.

Prescaler Value

P2 and P1 in the function latch set the prescaler values. The prescaler value should be chosen so that the prescaler output frequency is always less than or equal to 325 MHz. Therefore, with an RF frequency of 4 GHz, a prescaler value of 16/17 is valid, but a value of 8/9 is not valid.

PD Polarity

This bit sets the phase detector polarity bit. See Table 9.

CP Three-State

This bit controls the CP output pin. With the bit set high, the CP output is put into three-state. With the bit set low, the CP output is enabled.

THE INITIALIZATION LATCH

When C2 and C1 = 1 and 1, respectively, the initialization latch is programmed. This is essentially the same as the function latch (programmed when C2 and C1 = 1 and 0, respectively).

However, when the initialization latch is programmed, there is an additional internal reset pulse applied to the R and N (A, B) counters. This pulse ensures that the N (A, B) counter is at the load point when the N (A, B) counter data is latched and the device begins counting in close phase alignment.

If the latch is programmed for synchronous power-down (CE pin is high, PD1 bit is high, and PD2 bit is low), the internal pulse also triggers this power-down. The prescaler reference and the oscillator input buffer are unaffected by the internal reset pulse; therefore, close phase alignment is maintained when counting resumes.

When the first N (A, B) counter data is latched after initialization, the internal reset pulse is again activated. However, successive N (A, B) counter loads after this will not trigger the internal reset pulse.

Device Programming After Initial Power-Up

After initial power up of the device, there are three methods for programming the device: initialization latch, CE pin, and counter reset.

Initialization Latch Method

- Apply V_{DD}.
- Program the initialization latch (11 in two LSBs of input word). Make sure that the F1 bit is programmed to 0.
- Do a function latch load (10 in two LSBs of the control word), making sure that the F1 bit is programmed to a 0.
- Do an R load (00 in two LSBs).
- Do an N (A, B) load (01 in two LSBs).

When the initialization latch is loaded, the following occurs:

- The function latch contents are loaded.
- An internal pulse resets the R, N (A, B), and timeout counters to load-state conditions and also three-states the charge pump. Note that the prescaler band gap reference and the oscillator input buffer are unaffected by the internal reset pulse, allowing close phase alignment when counting resumes.
- Latching the first N (A, B) counter data after the initialization word activates the same internal reset pulse. Successive N (A, B) loads will not trigger the internal reset pulse, unless there is another initialization.

CE PIN METHOD

- Apply V_{DD}.
- Bring CE low to put the device into power-down. This is an asychronous power-down in that it happens immediately.
- Program the function latch (10).
- Program the R counter latch (00).
- Program the N (A, B) counter latch (01).
- Bring CE high to take the device out of power-down. The R and N (A, B) counters now resume counting in close alignment.

Note that after CE goes high, a 1 µs duration may be required for the prescaler band gap voltage and oscillator input buffer bias to reach steady state.

CE can be used to power the device up and down to check for channel activity. The input register does not need to be reprogrammed each time the device is disabled and enabled as long as it is programmed at least once after V_{DD} is initially applied.

COUNTER RESET METHOD

- Apply V_{DD}.
- Do a function latch load (10 in two LSBs). As part of this, load 1 to the F1 bit. This enables the counter reset.
- Do an R counter load (00 in two LSBs).
- Do an N (A, B) counter load (01 in two LSBs).
- Do a function latch load (10 in two LSBs). As part of this, load 0 to the F1 bit. This disables the counter reset.

This sequence provides the same close alignment as the initialization method. It offers direct control over the internal reset. Note that counter reset holds the counters at load point and three-states the charge pump but does not trigger synchronous power-down.

APPLICATIONS

LOCAL OSCILLATOR FOR LMDS BASE STATION TRANSMITTER

Figure 22 shows the ADF4106 being used with a VCO to produce the LO for an LMDS base station.

The reference input signal is applied to the circuit at $FREF_{IN}$ and, in this case, is terminated in 50 Ω. A typical base station system would have either a TCXO or an OCXO driving the reference input without any 50 Ω termination.

To achieve a channel spacing of 1 MHz at the output, the 10 MHz reference input must be divided by 10, using the on-chip reference divider of the ADF4106.

The charge pump output of the ADF4106 (Pin 2) drives the loop filter. In calculating the loop filter component values, a number of items need to be considered. In this example, the loop filter was designed so that the overall phase margin for the system would be 45°.

Other PLL system specifications include:

K_D = 2.5 mA

K_V = 80 MHz/V

Loop Bandwidth = 50 kHz

F_{PFD} = 1 MHz

N = 5800

Extra Reference Spur Attenuation = 10 dB

These specifications are needed and used to derive the loop filter component values shown in Figure 22.

The circuit in Figure 22 shows a typical phase noise performance of −83.5 dBc/Hz at 1 kHz offset from the carrier. Spurs are better than −62 dBc.

The loop filter output drives the VCO, which in turn is fed back to the RF input of the PLL synthesizer and also drives the RF output terminal. A T-circuit configuration provides 50 Ω matching between the VCO output, the RF output, and the RF_{IN} terminal of the synthesizer.

In a PLL system, it is important to know when the system is in lock. In Figure 22, this is accomplished by using the MUXOUT signal from the synthesizer. The MUXOUT pin can be programmed to monitor various internal signals in the synthesizer. One of these is the LD or lock-detect signal.

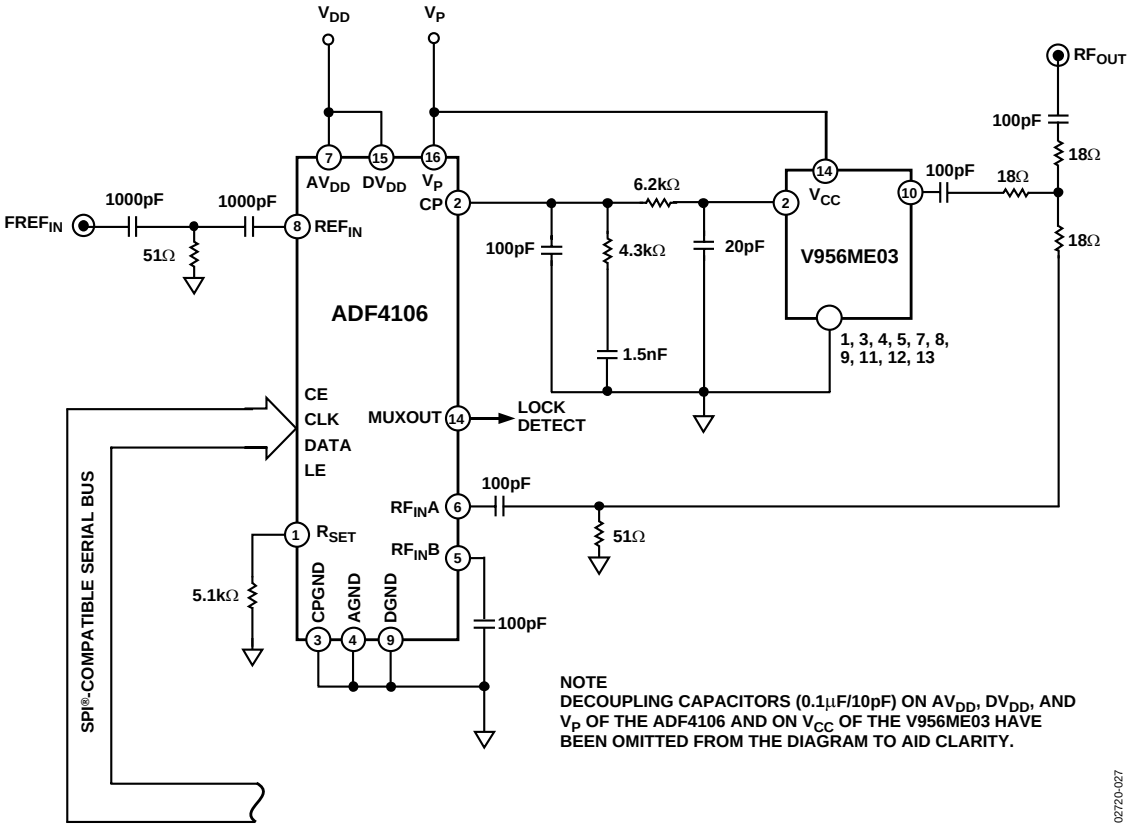


Figure 22. Local Oscillator for LMDS Base Station

INTERFACING

The ADF4106 has a simple SPI-compatible serial interface for writing to the device. CLK, DATA, and LE control the data transfer. When LE goes high, the 24 bits clocked into the input register on each rising edge of CLK are transferred to the appropriate latch. See Figure 2 for the timing diagram and Table 5 for the latch truth table.

The maximum allowable serial clock rate is 20 MHz. This means that the maximum update rate for the device is 833 kHz, or one update every 1.2 µs. This is certainly more than adequate for systems that have typical lock times in hundreds of microseconds.

ADuC812 Interface

Figure 23 shows the interface between the ADF4106 and the ADuC812 MicroConverter®. Since the ADuC812 is based on an 8051 core, this interface can be used with any 8051-based microcontroller. The MicroConverter is set up for SPI master mode with CPHA = 0. To initiate the operation, the I/O port driving LE is brought low. Each latch of the ADF4106 needs a 24-bit word. This is accomplished by writing three 8-bit bytes from the MicroConverter to the device. When the third byte is written, the LE input should be brought high to complete the transfer.

On first applying power to the ADF4106, it needs four writes (one each to the initialization latch, function latch, R counter latch, and N counter latch) for the output to become active.

I/O port lines on the ADuC812 are also used to control power-down (CE input) and to detect lock (MUXOUT configured as lock detect and polled by the port input).

When operating in the mode described, the maximum SCLOCK rate of the ADuC812 is 4 MHz. This means that the maximum rate at which the output frequency can be changed is 166 kHz.

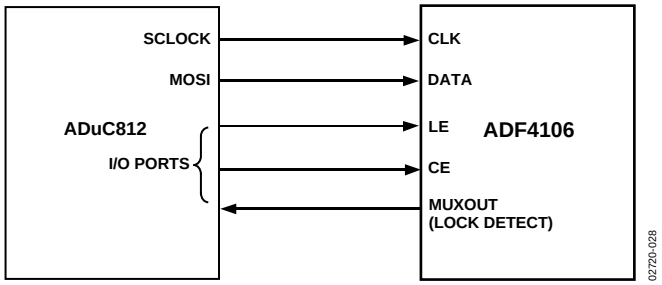


Figure 23. ADuC812-to-ADF4106 Interface

ADSP2181 Interface

Figure 24 shows the interface between the ADF4106 and the ADSP21xx digital signal processor (DSP). The ADF4106 needs a 24-bit serial word for each latch write. The easiest way to accomplish this using the ADSP21xx family is to use the autobuffered transmit mode of operation with alternate framing. This provides a means for transmitting an entire block of serial data before an interrupt is generated. Set up the word length for 8 bits and use three memory locations for each 24-bit word. To program each 24-bit latch, store the three 8-bit bytes, enable the autobuffered mode, and write to the transmit register of the DSP. This last operation initiates the autobuffer transfer.

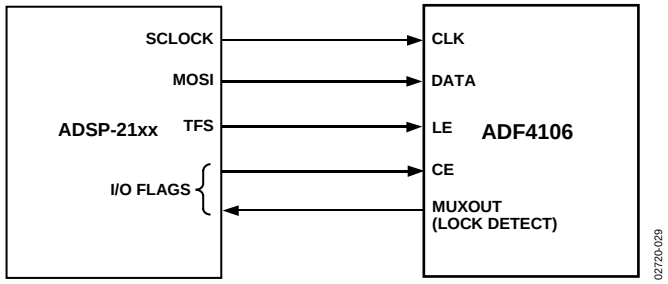


Figure 24. ADSP-21xx-to-ADF4106 Interface

PCB DESIGN GUIDELINES FOR CHIP SCALE PACKAGE

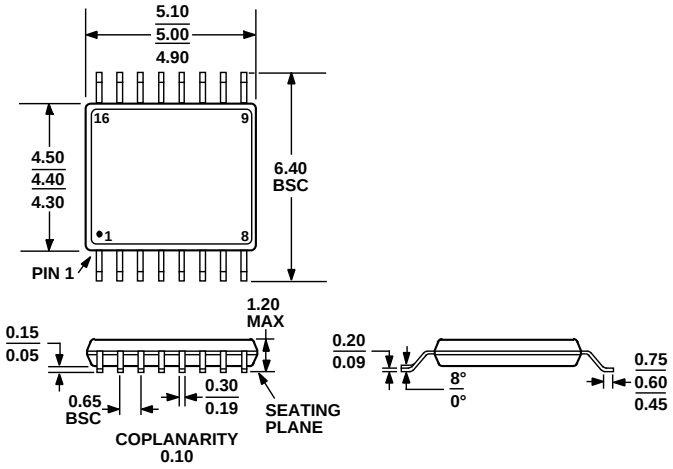
The lands on the LFCSP (CP-20) are rectangular. The printed circuit board (PCB) pad for these should be 0.1 mm longer than the package land length and 0.05 mm wider than the package land width. The land should be centered on the pad. This ensures that the solder joint size is maximized. The bottom of the LFCSP has a central thermal pad.

The thermal pad on the PCB should be at least as large as this exposed pad. On the PCB, there should be a clearance of at least 0.25 mm between the thermal pad and the inner edges of the pad pattern. This ensures that shorting is avoided.

Thermal vias may be used on the PCB thermal pad to improve thermal performance of the package. If vias are used, they should be incorporated in the thermal pad at 1.2 mm pitch grid. The via diameter should be between 0.3 mm and 0.33 mm, and the via barrel should be plated with 1 oz. copper to plug the via.

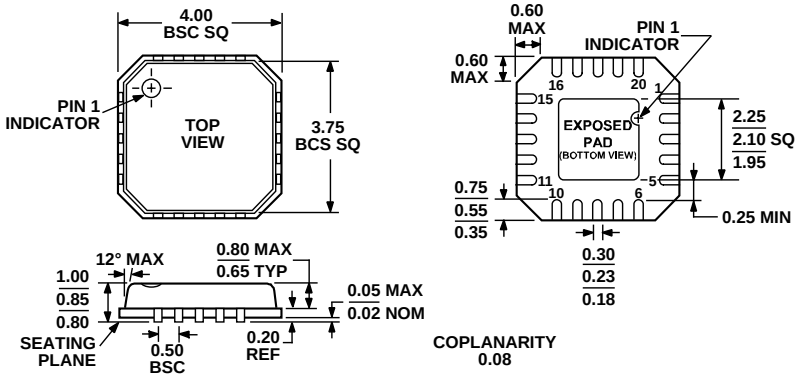
The user should connect the PCB thermal pad to AGND.

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-153-AB

Figure 25. 16-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-16)
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-220-VGGD-1

Figure 26. 20-Lead Lead Frame Chip Scale Package [LFCSP_VQ]
4 mm × 4 mm Body, Very Thin Quad
(CP-20-1)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
ADF4106BRU	–40°C to + 85°C	16-Lead Thin Shrink Small Outline Package (TSSOP)	RU-16
ADF4106BRU-REEL	–40°C to + 85°C	16-Lead Thin Shrink Small Outline Package (TSSOP)	RU-16
ADF4106BRU-REEL7	–40°C to + 85°C	16-Lead Thin Shrink Small Outline Package (TSSOP)	RU-16
ADF4106BRUZ[1]	–40°C to + 85°C	16-Lead Thin Shrink Small Outline Package (TSSOP)	RU-16
ADF4106BRUZ-RL[1]	–40°C to + 85°C	16-Lead Thin Shrink Small Outline Package (TSSOP)	RU-16
ADF4106BRUZ-R7[1]	–40°C to + 85°C	16-Lead Thin Shrink Small Outline Package (TSSOP)	RU-16
ADF4106BCP	–40°C to + 85°C	20-Lead Lead Frame Chip Scale Package (LFCSP_VQ)	CP-20
ADF4106BCP-REEL	–40°C to + 85°C	20-Lead Lead Frame Chip Scale Package (LFCSP_VQ)	CP-20
ADF4106BCP-REEL7	–40°C to + 85°C	20-Lead Lead Frame Chip Scale Package (LFCSP_VQ)	CP-20
ADF4106BCPZ[1]	–40°C to + 85°C	20-Lead Lead Frame Chip Scale Package (LFCSP_VQ)	CP-20
ADF4106BCPZ-RL[1]	–40°C to + 85°C	20-Lead Lead Frame Chip Scale Package (LFCSP_VQ)	CP-20
ADF4106BCPZ-R7[1]	–40°C to + 85°C	20-Lead Lead Frame Chip Scale Package (LFCSP_VQ)	CP-20
EVAL-ADF4106EB1		Evaluation Board	
EVAL-ADF411XEB1		Evaluation Board	

[1] Z = Pb-free part.

NOTES

NOTES

NOTES

C02720–0–6/05(B)

MODEL VTXO500

Voltage Controlled Temperature Compensated Crystal Oscillators

Surface mountable VCTCXO suited to hand soldering. Custom frequencies from 8.2MHz to 32MHz with a clipped sinewave output.

Product Description

This Colpitts oscillator uses the direct two−port temperature compensation method. Operating on the fundamental mode, the circular AT−cut crystal is housed in the environmentally rugged UM−1 SLIM resistance weld package.

The product can be configured to operate on any voltage between 2.7V and 5V. A mechanical trimmer is available for adjusting the frequency.

Customized frequencies readily available make this model suitable for many timing and frequency applications.

Features

- Excellent temperature stability performance
- Able to operate over industrial temperature ranges
- Low hysteresis
- Low power consumption
- Excellent vibration performance
- Very good phase noise performance
- Frequency control ranges from 6 to 50ppm available

1.0 *SPECIFICATION REFERENCES*

1.1	**Model Description**	VTXO505R 30.0 MHz
1.2	**Reference Number**	73524
1.3	**Company**	Rakon Limited

2.0 *FREQUENCY CHARACTERISTICS*

Line	*Parameter*	*Test Condition*	*Min.*	*Max.*	*Units*
2.1	**Nominal Frequency**			30.0	MHz
2.2	**Frequency calibration**	Frequency at 23ºC ±2ºC (Note 1)		1.0	±ppm
2.3	**Frequency stability over temperature**	Referenced to frequency reading at 25ºC. Temperature varied at maximum of 2ºC per minute. Control voltage held at control voltage (VCO) mid−point		0.5	±ppm
2.4	**Temperature range**	The operating temperature range over which the frequency stability is measured (Note 3)	−10.0	45.0	ºC
2.5	**Frequency slope of perturbations**	Minimum of 1 frequency reading every 2ºC, over the operating temperature range (Note 1)		0.5	ppm/ºC
2.6	**Static temperature hysteresis**	Frequency change after reciprocal temperature ramped over the operating range. Frequency measured before and after at 25ºC.		0.4	±ppm
2.7	**Supply voltage stability**	Supply voltage varied ±5% at 25ºC. Frequencies above 25MHz are not able to be specified below the maximum value given (Note 1)		0.3	±ppm
2.8	**Load sensitivity**	±10% load change		0.2	±ppm

2.9	**Root Allan Variance**	1 second Tau. (Note 1)		1.0	ppb
2.10	**Long term stability**	Frequency drift over 1 year (Note 1)		1.0	±ppm
2.11	**G Sensitivity**	Gamma vector of all three axes from 30Hz to 1500Hz, typical values (Note 1)		2.0	ppb/G
2.12	**Trimmer adjustment**	Manual adjustment using trimmer tool	3.0		±ppm

3.0 *POWER SUPPLY*

Line	*Parameter*	*Test Condition*	*Min.*	*Max.*	*Units*
3.1	**Supply voltage**	Supply voltage range based on nominal 5V	4.75	5.25	V
3.2	**Current**	At maximum supply voltage		2.0	mA

4.0 *CONTROL VOLTAGE*

Line	*Parameter*	*Test Condition*	*Min.*	*Max.*	*Units*
4.1	**Control voltage range**	Determined by supply voltage (Note 5). The nominal control voltage value is midway between the minimum and maximum.	0.5	4.5	V
4.2	**Frequency tuning**	Frequency shift from minimum to maximum control voltages (Note 6)	10.0		ppm
4.3	**Frequency tuning linearity**	Deviation from straight line curve fit (Note 1)		20.0	%
4.4	**Port input impedance**		100.0		kOhm

5.0 *OSCILLATOR OUTPUT*

Line	*Parameter*	*Test Condition*	*Min.*	*Max.*	*Units*
5.1	**Output waveform**	Clipped sinewave			
5.2	**Output voltage level**	At minimum supply voltage	1.0		V
5.3	**Output load resistance**	Operating range	18.0	22.0	kOhm
5.4	**Output load capacitance**	Operating range	4.5	5.5	pF

6.0 *SSB PHASE NOISE*

Line	*Parameter*	*Test Condition*	*Min.*	*Max.*	*Units*
6.1	**Typical SSB phase noise density**	1Hz offset		−60.0	dBc/Hz
6.2	**Typical SSB phase noise density**	10Hz offset		−90.0	dBc/Hz
6.3	**Typical SSB phase noise density**	100Hz offset		−120.0	dBc/Hz
6.4	**Typical SSB phase noise density**	1KHz offset		−140.0	dBc/Hz

6.5	**Typical SSB phase noise density**	10KHz offset	−150.0	dBc/Hz

7.0 *ENVIRONMENTAL*

7.1	**Shock**	Half sinewave acceleration of 100G peak amplitude for 11ms duration, 3 cycles each plane.
7.2	**Random Vibration**	10G RMS 30Hz to 1500Hz duration of 6 hours.
7.3	**Humidity**	After 48 hours at 85ºC ±2ºC 85% relative humidity non−condensing
7.4	**Thermal shock test**	Exposed at −40ºC for 30 minutes then to 85ºC for 30 minutes constantly for a period of 5 days.
7.5	**Storage temperature**	−40 to 85ºC

8.0 *MARKING*

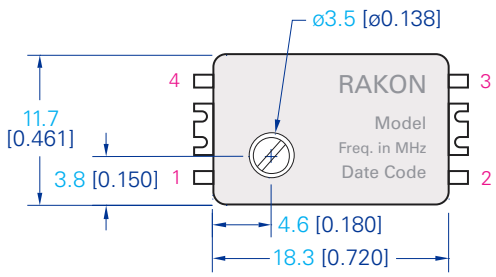
8.1	**Type**	Label
8.2	**Line 1**	Rakon logo
8.3	**Line 2**	Model descriptive
8.4	**Line 3**	Frequency in MHz (to 3 decimal places or greater depending on the no. of significant digits after the decimal point)
8.5	**Line 4**	Date code WWYY

9.0 *MANUFACTURING INFORMATION*

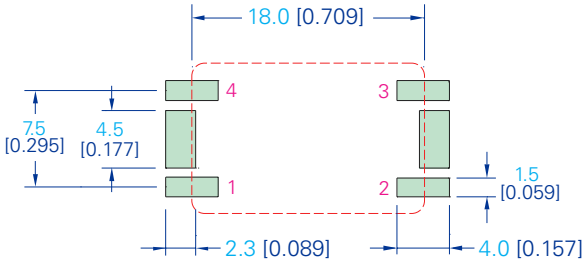
9.1	**Washing**	Unit is not able to go through any washing process, due to presence of manual trimmer with open dielectric exposure.
9.2	**Packaging description**	Anti−static trays, 50 per tray, 10 trays per inner box, 4 inner boxes per out box.
9.3	**Hand soldering**	The unit is hand or laser soldered only. Not to be reflow soldered.

10.0 *SPECIFICATION NOTES*

10.1	**Note 1**	The maximum value is the specification. A minimum value, if present, indicates the tightest specification available.
10.2	**Note 2**	A max. frequency stability over the temperature is required to be specified. For this model, values between to +/−1ppm and +/−10ppm are available. Standard options are +/−1ppm, +/−1.5ppm, +/−2ppm and +/−2.5ppm.
10.3	**Note 3**	The operating temperature range needs to be specified. The extremes for this model are −40 and +85 deg C. If either or both ends of the operating temperature range are at these extremes, then the frequency stability options are limited to greater than +/−1.5ppm.
10.4	**Note 4**	Standard power supply options are 2.7V, 3V, 3.3V, 4V or 5V.
10.5	**Note 5**	Standard VCO control voltage options include 1.5V±1V, 2.5V±2V.
10.6	**Note 6**	The minimum value is the specification. A maximum value, if present, indicates the widest tuning range available for this model (subject to other parameters).

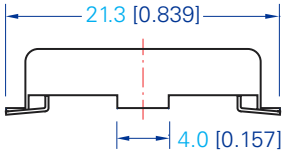


TOP VIEW

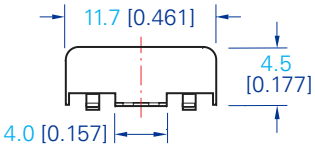


TOP VIEW

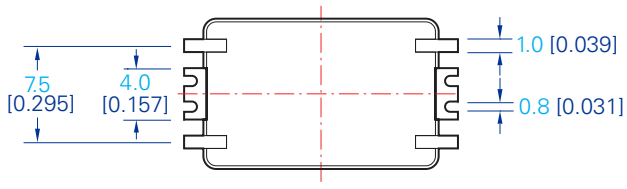
RECOMMENDED PAD LAYOUT
TRACKS NOT RECOMMENDED UNDER OSCILLATOR



SIDE VIEW



END VIEW



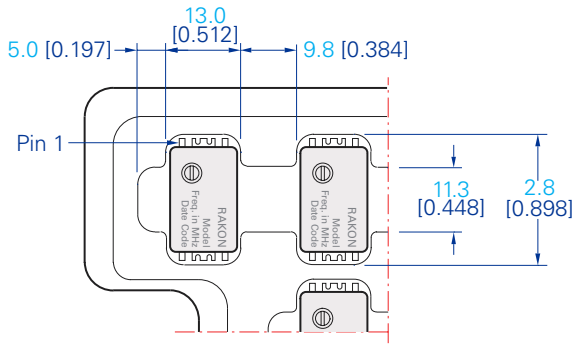
BOTTOM VIEW

PIN CONNECTIONS	
1	CONTROL VOLTAGE
2	COMMON AND CASE
3	OUTPUT
4	+Vcc

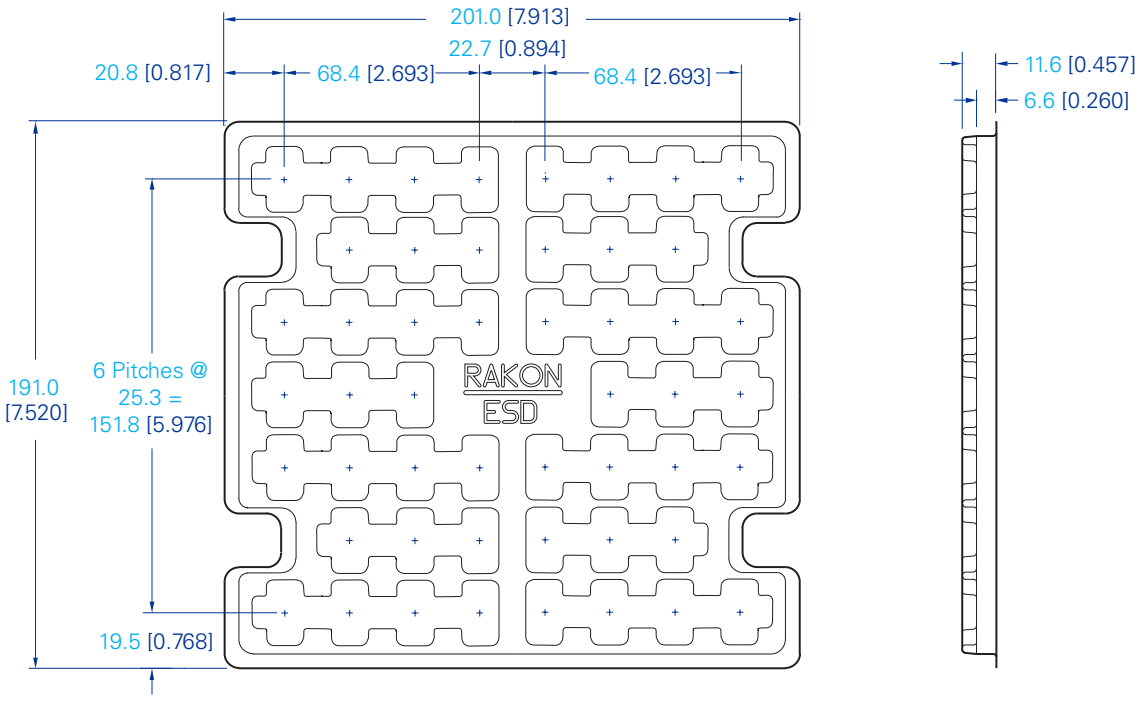
TITLE: VTXO500 MODEL
FILENAME: CAT025
REVISION: B
RELATED DRAWINGS:
DATE: 13-May-05
SCALE: 2 : 1
Millimetres [inch]

Tolerances:
XX =±0.5
X.X =±0.2
X.XX =±0.10
X.XXX =±0.05
X° =±1.0°
Hole =±0.10

RAKON PRECISION QUARTZ CRYSTALS



POCKETS DETAIL (Scale 1:1)

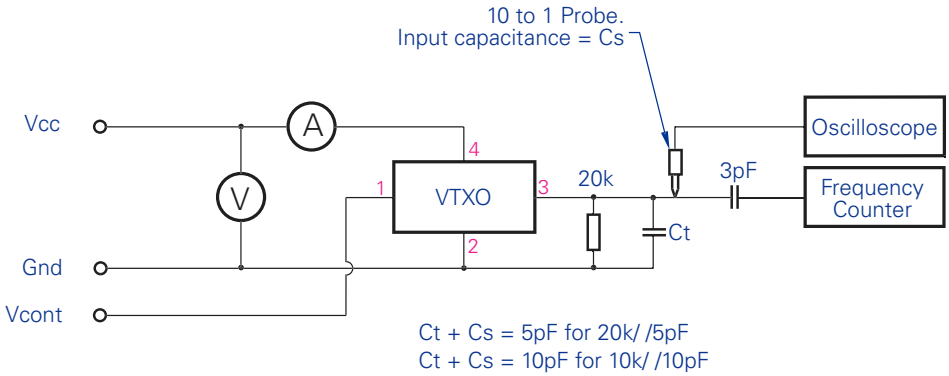


TRAY DETAIL (Scale 1:2)

Note: 50 Oscilators Per Tray. 21 (20+1 top) Trays Per Small Box. 4 Small Boxes Per Large Box.

TITLE: 500 SERIES TRAY	FILENAME: CAT094	REVISION: B	Tolerances:
RELATED DRAWINGS:		DATE: 13-May-05	XX =±0.5 X.X =±0.2 X.XX =±0.10 X.XXX =±0.05 X° =±1.0° Hole =±0.10
		SCALE: See Above	
		Millimetres [inch]	

RAKON PRECISION QUARTZ CRYSTALS



TITLE: VTXO CLIPPED SINEWAVE TEST CIRCUIT FILENAME: CAT135 REVISION: B

RELATED DRAWINGS:

DATE: 03-Nov-03

SCALE: NTS

Millimetres [inch]

RAKON PRECISION QUARTZ CRYSTALS

5-A, WIDE INPUT RANGE, STEP-DOWN SWIFT™ CONVERTER

FEATURES

- **Wide Input Voltage Range: 5.5 V to 36 V**
- **Up to 5-A Continuous (6-A Peak) Output Current**
- **High Efficiency Greater than 90% Enabled by 110-mΩ Integrated MOSFET Switch**
- **Wide Output Voltage Range: Adjustable Down to 1.22 V with 1.5% Initial Accuracy**
- **Internal Compensation Minimizes External Parts Count**
- **Fixed 500 kHz Switching Frequency for Small Filter Size**
- **18 µA Shut Down Supply Current**
- **Improved Line Regulation and Transient Response by Input Voltage Feed Forward**
- **System Protected by Overcurrent Limiting, Overvoltage Protection and Thermal Shutdown**
- **–40°C to 125°C Operating Junction Temperature Range**
- **Available in Small Thermally Enhanced 8-Pin SOIC PowerPAD™ Package**
- **For SWIFT™ Documentation, Application Notes and Design Software, See the TI Website at www.ti.com/swift**

APPLICATIONS

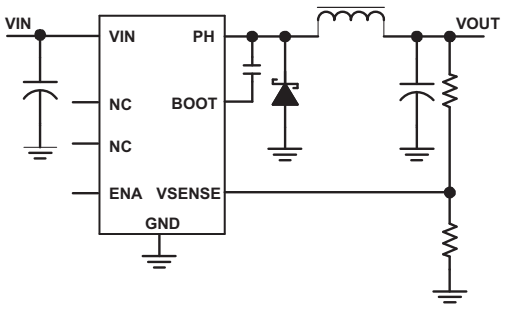
- **High Density Point-of-Load Regulators**
- **LCD Displays, Plasma Displays**
- **Battery Chargers**
- **12-V/24-V Distributed Power Systems**

DESCRIPTION

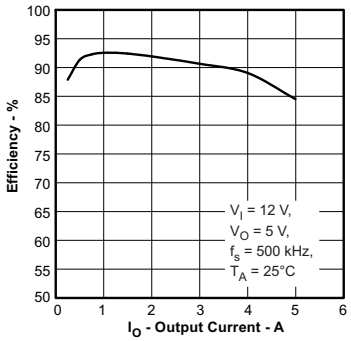
As a member of the SWIFT™ family of DC/DC regulators, the TPS5450 is a high-output-current PWM converter that integrates a low resistance high side N-channel MOSFET. Included on the substrate with the listed features are a high performance voltage error amplifier that provides tight voltage regulation accuracy under transient conditions; an undervoltage-lockout circuit to prevent start-up until the input voltage reaches 5.5 V; an internally set slow-start circuit to limit inrush currents; and a voltage feed-forward circuit to improve the transient response. Using the ENA pin, shutdown supply current is reduced to 18 µA typically. Other features include an active-high enable, overcurrent limiting, overvoltage protection and thermal shutdown. To reduce design complexity and external component count, the TPS5450 feedback loop is internally compensated.

The TPS5450 device is available in a thermally enhanced, 8-pin SOIC PowerPAD™ package. TI provides evaluation modules and software tool to aid in achieving high-performance power supply designs to meet aggressive equipment development cycles.

Simplified Schematic



Efficiency vs Output Current



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

SWIFT, PowerPAD are trademarks of Texas Instruments.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION

T_J	INPUT VOLTAGE	OUTPUT VOLTAGE	PACKAGE(1)	PART NUMBER
–40°C to 125°C	5.5 V to 36 V	Adjustable to 1.22 V	Thermally Enhanced SOIC (DDA)(2)	TPS5450DDA

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.
(2) The DDA package is also available taped and reeled. Add an R suffix to the device type (i.e., TPS5450DDAR). See applications section of data sheet for PowerPAD™ drawing and layout information.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted) (1) (2)

			VALUE	UNIT
V_I	Input voltage range	VIN	–0.3 to 40(3)	V
		BOOT	–0.3 to 50	
		PH (steady-state)	–0.6 to 40(3)	
		ENA	–0.3 to 7	
		BOOT-PH	10	
		VSENSE	–0.3 to 3	
		PH (transient < 10 ns)	–1.2	
I_O	Source current	PH	Internally Limited	
I_{lkg}	Leakage current	PH	10	µA
T_J	Operating virtual junction temperature range		–40 to 150	°C
T_{stg}	Storage temperature		–65 to 150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.
(3) Approaching the absolute maximum rating for the VIN pin may cause the voltage on the PH pin to exceed the absolute maximum rating.

DISSIPATION RATINGS(1) (2)

PACKAGE	THERMAL IMPEDANCE JUNCTION-TO-AMBIENT
8 Pin DDA (4-layer board with solder)(3)	30°C/W

(1) Maximum power dissipation may be limited by overcurrent protection.
(2) Power rating at a specific ambient temperature T_A should be determined with a junction temperature of 125°C. This is the point where distortion starts to substantially increase. Thermal management of the final PCB should strive to keep the junction temperature at or below 125°C for best performance and long-term reliability. See *Thermal Calculations* in applications section of this data sheet for more information.
(3) Test board conditions:
a. 2 in x 1.85 in, 4 layers, thickness: 0.062 inch (1,57 mm).
b. 2 oz. copper traces located on the top and bottom of the PCB.
c. 2 oz. copper ground planes on the 2 internal layers.
d. 4 thermal vias in the PowerPAD area under the device package.

RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
V_I	Input voltage range	5.5		36	V
T_J	Operating junction temperature	–40		125	°C

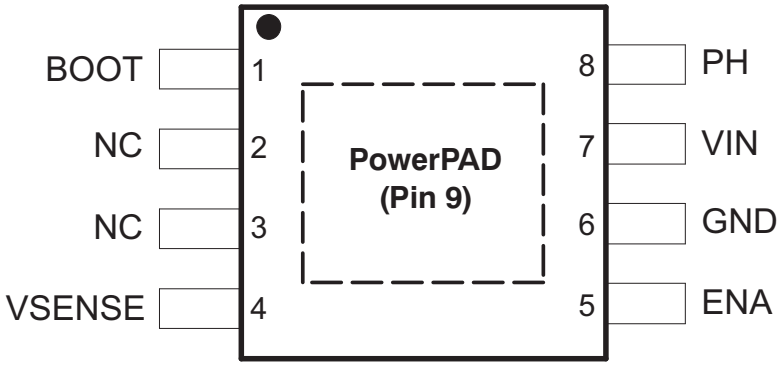
ELECTRICAL CHARACTERISTICS

T_J = –40°C to 125°C, VIN = 5.5 V - 36 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE (VIN PIN)						
I_Q	Quiescent current	VSENSE = 2 V, Not switching, PH pin open		3	4.4	mA
		Shutdown, ENA = 0 V		18	50	µA
UNDERVOLTAGE LOCK OUT (UVLO)						
	Start threshold voltage, UVLO			5.3	5.5	V
	Hysteresis voltage, UVLO			330		mV
VOLTAGE REFERENCE						
	Voltage reference accuracy	T_J = 25°C	1.202	1.221	1.239	V
		I_O = 0 A – 5 A	1.196	1.221	1.245	
OSCILLATOR						
	Internally set free-running frequency		400	500	600	kHz
	Minimum controllable on time			150	200	ns
	Maximum duty cycle		87	89		%
ENABLE (ENA PIN)						
	Start threshold voltage, ENA				1.3	V
	Stop threshold voltage, ENA		0.5			V
	Hysteresis voltage, ENA			450		mV
	Internal slow-start time (0~100%)		6.6	8	10	ms
CURRENT LIMIT						
	Current limit		6.0	7.5	9.0	A
	Current limit hiccup time		13	16	20	ms
THERMAL SHUTDOWN						
	Thermal shutdown trip point		135	162		°C
	Thermal shutdown hysteresis			14		°C
OUTPUT MOSFET						
$r_{DS(on)}$	High-side power MOSFET switch	VIN = 5.5 V		150		mΩ
				110	230	

PIN ASSIGNMENTS

DDA PACKAGE
(TOP VIEW)



TERMINAL FUNCTIONS

TERMINAL		DESCRIPTION
NAME	NO.	
BOOT	1	Boost capacitor for the high-side FET gate driver. Connect 0.01 µF low ESR capacitor from BOOT pin to PH pin.
NC	2, 3	Not connected internally.
VSENSE	4	Feedback voltage for the regulator. Connect to output voltage divider.
ENA	5	On/off control. Below 0.5 V, the device stops switching. Float the pin to enable.
GND	6	Ground. Connect to PowerPAD.
VIN	7	Input supply voltage. Bypass VIN pin to GND pin close to device package with a high quality, low ESR ceramic capacitor.
PH	8	Source of the high side power MOSFET. Connected to external inductor and diode.
PowerPAD	9	GND pin must be connected to the exposed pad for proper operation.

TYPICAL CHARACTERISTICS

OSCILLATOR FREQUENCY vs JUNCTION TEMPERATURE

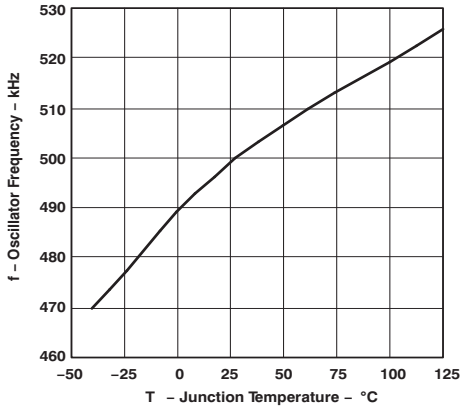


Figure 1.

NON-SWITCHING QUIESCENT CURRENT vs JUNCTION TEMPERATURE

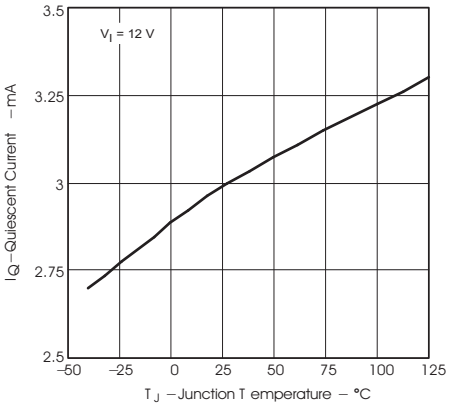


Figure 2.

SHUTDOWN QUIESCENT CURRENT vs INPUT VOLTAGE

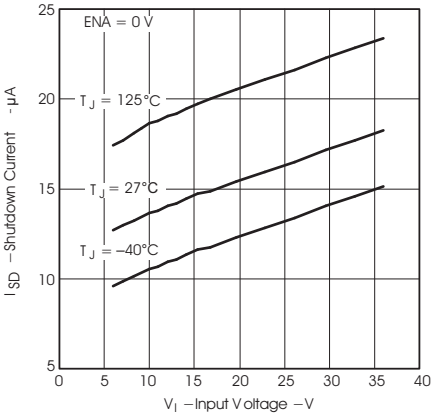


Figure 3.

VOLTAGE REFERENCE vs JUNCTION TEMPERATURE

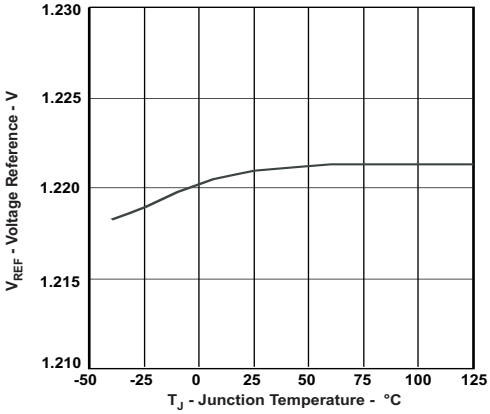


Figure 4.

ON RESISTANCE vs JUNCTION TEMPERATURE

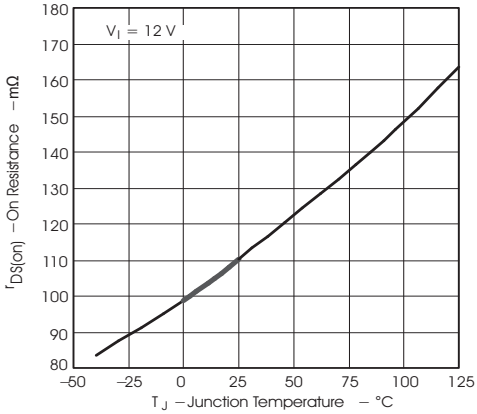


Figure 5.

INTERNAL SLOW START TIME vs JUNCTION TEMPERATURE

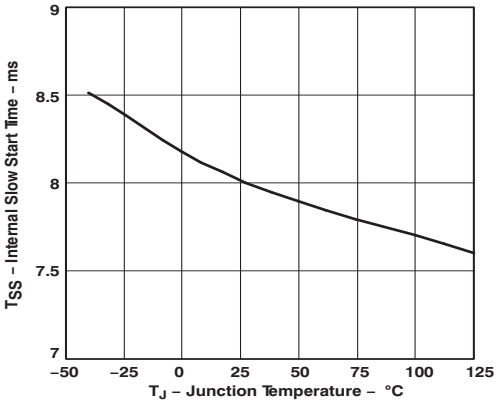


Figure 6.

TYPICAL CHARACTERISTICS (continued)

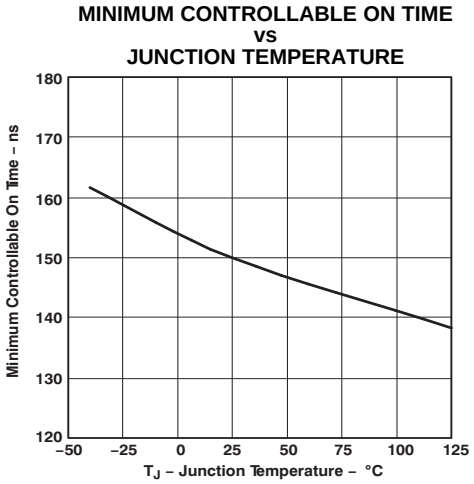


Figure 7.

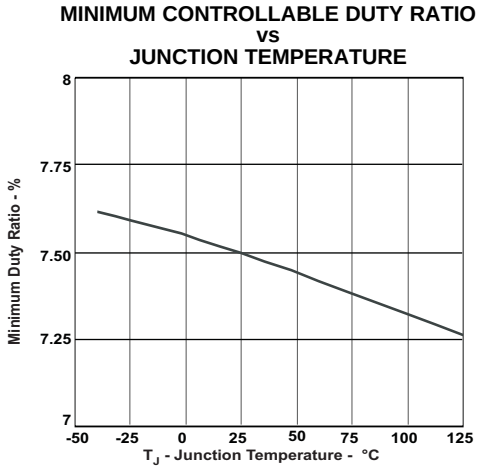
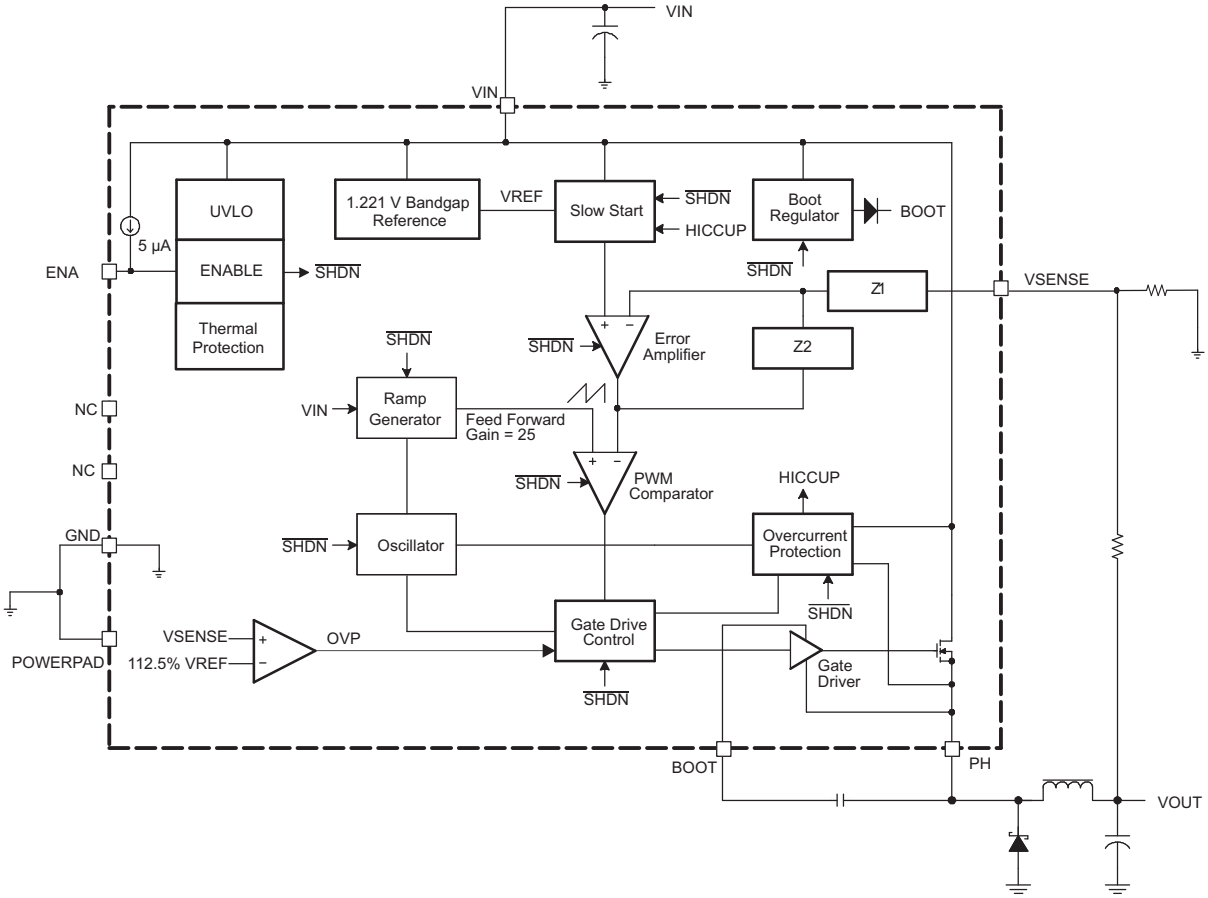


Figure 8.

APPLICATION INFORMATION

FUNCTIONAL BLOCK DIAGRAM



DETAILED DESCRIPTION

Oscillator Frequency

The internal free running oscillator sets the PWM switching frequency at 500 kHz. The 500 kHz switching frequency allows less output inductance for the same output ripple requirement resulting in a smaller output inductor.

Voltage Reference

The voltage reference system produces a precision reference signal by scaling the output of a temperature stable bandgap circuit. The bandgap and scaling circuits are trimmed during production testing to an output of 1.221 V at room temperature.

Enable (ENA) and Internal Slow Start

The ENA pin provides electrical on/off control of the regulator. Once the ENA pin voltage exceeds the threshold voltage, the regulator starts operation and the internal slow start begins to ramp. If the ENA pin voltage is pulled below the threshold voltage, the regulator stops switching and the internal slow start resets. Connecting the pin to ground or to any voltage less than 0.5 V will disable the regulator and activate the shutdown mode. The quiescent current of the TPS5450 in shutdown mode is typically 18 µA.

The ENA pin has an internal pullup current source, allowing the user to float the ENA pin. If an application requires controlling the ENA pin, use open drain or open collector output logic to interface with the pin. To limit the start-up inrush current, an internal slow-start circuit is used to ramp up the reference voltage from 0 V to its final value, linearly. The internal slow start time is 8 ms typically.

Undervoltage Lockout (UVLO)

The TPS5450 incorporates an undervoltage lockout circuit to keep the device disabled when VIN (the input voltage) is below the UVLO start voltage threshold. During power up, internal circuits are held inactive and the internal slow start is grounded until VIN exceeds the UVLO start threshold voltage. Once the UVLO start threshold voltage is reached, the internal slow start is released and device start-up begins. The device operates until VIN falls below the UVLO stop threshold voltage. The typical hysteresis in the UVLO comparator is 330 mV.

Boost Capacitor (BOOT)

Connect a 0.01 µF low-ESR ceramic capacitor between the BOOT pin and PH pin. This capacitor provides the gate drive voltage for the high-side MOSFET. X7R or X5R grade dielectrics are recommended due to their stable values over temperature.

Output Feedback (VSENSE) and Internal Compensation

The output voltage of the regulator is set by feeding back the center point voltage of an external resistor divider network to the VSENSE pin. In steady-state operation, the VSENSE pin voltage should be equal to the voltage reference 1.221 V.

The TPS5450 implements internal compensation to simplify the regulator design. Since the TPS5450 uses voltage mode control, a type 3 compensation network has been designed on chip to provide a high crossover frequency and a high phase margin for good stability. See the *Internal Compensation Network* in the applications section for more details.

Voltage Feed Forward

The internal voltage feed forward provides a constant dc power stage gain despite any variations with the input voltage. This greatly simplifies the stability analysis and improves the transient response. Voltage feed forward varies the peak ramp voltage inversely with the input voltage so that the modulator and power stage gain are constant at the feed forward gain, i.e.

$$\text{Feed Forward Gain} = \frac{\text{VIN}}{\text{Ramp}_{\text{pk}-\text{pk}}} \tag{1}$$

The typical feed forward gain of TPS5450 is 25.

Pulse-Width-Modulation (PWM) Control

The regulator employs a fixed frequency pulse-width-modulator (PWM) control method. First, the feedback voltage (VSENSE pin voltage) is compared to the constant voltage reference by the high gain error amplifier and compensation network to produce a error voltage. Then, the error voltage is compared to the ramp voltage by the PWM comparator. In this way, the error voltage magnitude is converted to a pulse width which is the duty cycle. Finally, the PWM output is fed into the gate drive circuit to control the on-time of the high-side MOSFET.

Overcurrent Limiting

Overcurrent limiting is implemented by sensing the drain-to-source voltage across the high-side MOSFET. The drain to source voltage is then compared to a voltage level representing the overcurrent threshold limit. If the drain-to-source voltage exceeds the overcurrent threshold limit, the overcurrent indicator is set true. The system will ignore the overcurrent indicator for the leading edge blanking time at the beginning of each cycle to avoid any turn-on noise glitches.

Once overcurrent indicator is set true, overcurrent limiting is triggered. The high-side MOSFET is turned off for the rest of the cycle after a propagation delay. The overcurrent limiting mode is called cycle-by-cycle current limiting.

Sometimes under serious overload conditions such as short-circuit, the overcurrent runaway may still happen when using cycle-by-cycle current limiting. A second mode of current limiting is used, i.e. hiccup mode overcurrent limiting. During hiccup mode overcurrent limiting, the voltage reference is grounded and the high-side MOSFET is turned off for the hiccup time. Once the hiccup time duration is complete, the regulator restarts under control of the slow start circuit.

Overvoltage Protection

The TPS5450 has an overvoltage protection (OVP) circuit to minimize voltage overshoot when recovering from output fault conditions. The OVP circuit includes an overvoltage comparator to compare the VSENSE pin voltage and a threshold of 112.5% x VREF. Once the VSENSE pin voltage is higher than the threshold, the high-side MOSFET will be forced off. When the VSENSE pin voltage drops lower than the threshold, the high-side MOSFET will be enabled again.

Thermal Shutdown

The TPS5450 protects itself from overheating with an internal thermal shutdown circuit. If the junction temperature exceeds the thermal shutdown trip point, the voltage reference is grounded and the high-side MOSFET is turned off. The part is restarted under control of the slow start circuit automatically when the junction temperature drops 14°C below the thermal shutdown trip point.

PCB Layout

Connect a low ESR ceramic bypass capacitor to the VIN pin. Care should be taken to minimize the loop area formed by the bypass capacitor connections, the VIN pin, and the TPS5450 ground pin. The best way to do this is to extend the top side ground area from under the device adjacent to the VIN trace, and place the bypass capacitor as close as possible to the VIN pin. The minimum recommended bypass capacitance is 4.7 µF ceramic with a X5R or X7R dielectric.

There should be a ground area on the top layer directly underneath the IC, with an exposed area for connection to the PowerPAD. Use vias to connect this ground area to any internal ground planes. Use additional vias at the ground side of the input and output filter capacitors as well. The GND pin should be tied to the PCB ground by connecting it to the ground area under the device as shown below.

The PH pin should be routed to the output inductor, catch diode and boot capacitor. Since the PH connection is the switching node, the inductor should be located very close to the PH pin and the area of the PCB conductor minimized to prevent excessive capacitive coupling. The catch diode should also be placed close to the device to minimize the output current loop area. Connect the boot capacitor between the phase node and the BOOT pin as shown. Keep the boot capacitor close to the IC and minimize the conductor trace lengths. The component placements and connections shown work well, but other connection routings may also be effective.

Connect the output filter capacitor(s) as shown between the VOUT trace and GND. It is important to keep the loop formed by the PH pin, Lout, Cout and GND as small as is practical.

Connect the VOUT trace to the VSENSE pin using the resistor divider network to set the output voltage. Do not route this trace too close to the PH trace. Due to the size of the IC package and the device pin-out, the trace may need to be routed under the output capacitor. Alternately, the routing may be done on an alternate layer if a trace under the output capacitor is not desired.

If using the grounding scheme shown in Figure 9, use a via connection to a different layer to route to the ENA pin.

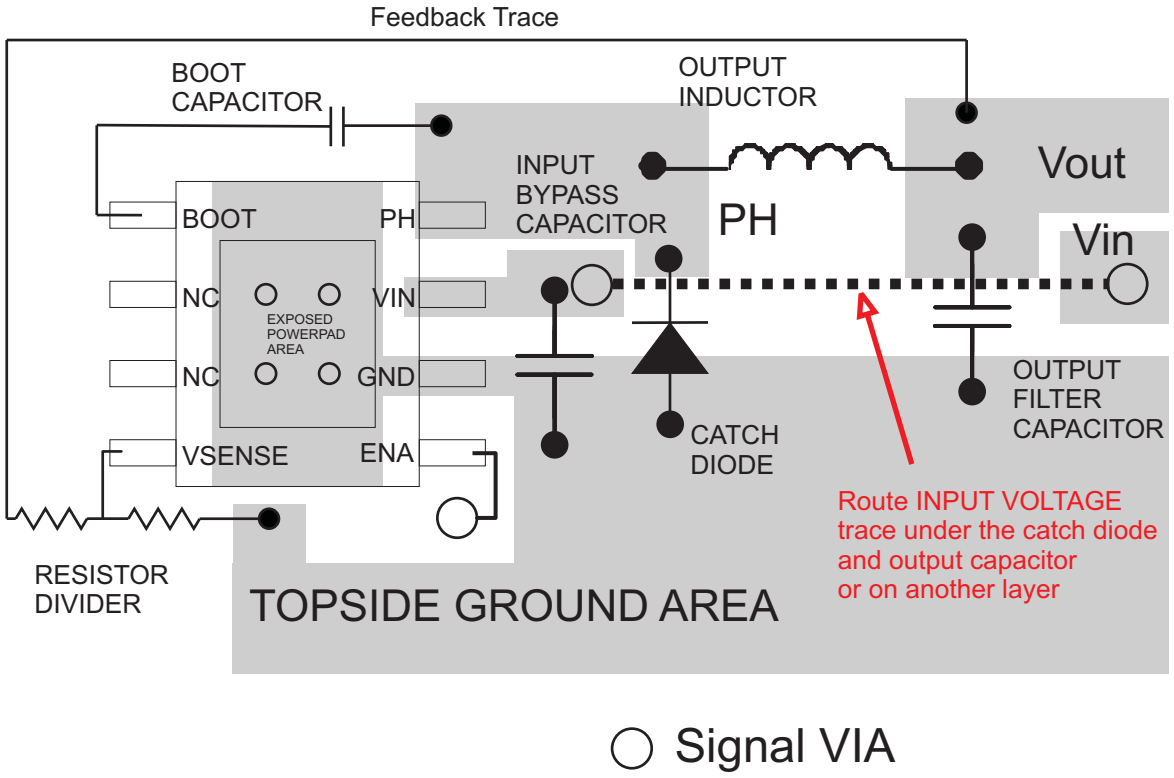


Figure 9. Design Layout

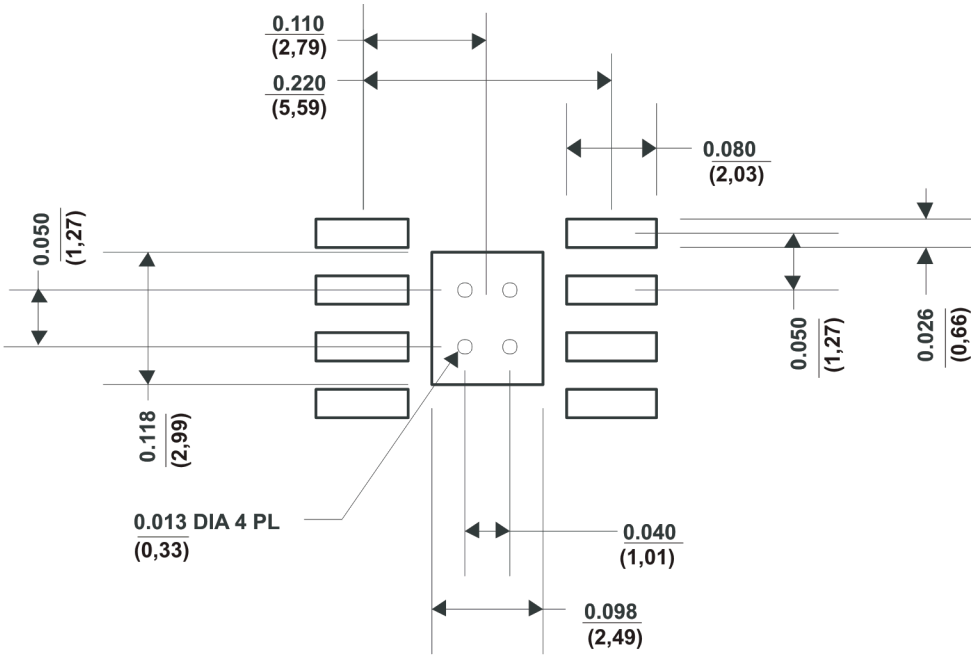


Figure 10. TPS5450 Land Pattern

Application Circuits

Figure 11 shows the schematic for a typical TPS5450 application. The TPS5450 can provide up to 5-A output current at a nominal output voltage of 5 V. For proper thermal performance, the exposed PowerPAD™ underneath the device must be soldered down to the printed-circuit board.

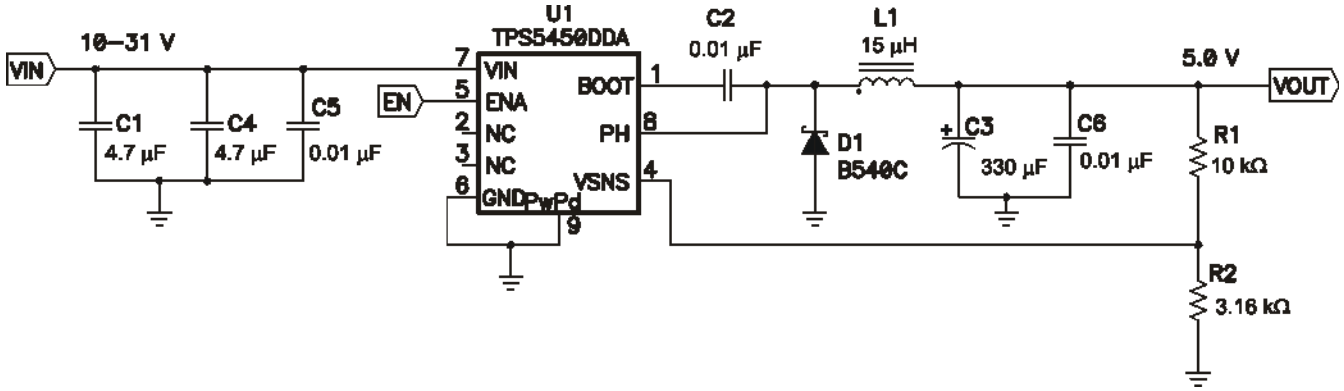


Figure 11. Application Circuit, 12-V to 5.0-V

Design Procedure

The following design procedure can be used to select component values for the TPS5450. Alternately, the SWIFT™ Designer Software may be used to generate a complete design. The SWIFT™ Designer Software uses an iterative design procedure and accesses a comprehensive database of components when generating a design. This section presents a simplified discussion of the design process.

To begin the design process a few parameters must be decided upon. The designer needs to know the following:

- Input voltage range
- Output voltage
- Input ripple voltage
- Output ripple voltage
- Output current rating
- Operating frequency

Design Parameters

For this design example, use the following as the input parameters:

DESIGN PARAMETER(1)	EXAMPLE VALUE
Input voltage range	10 V to 31 V
Output voltage	5 V
Input ripple voltage	400 mV
Output ripple voltage	30 mV
Output current rating	5 A
Operating frequency	500 kHz

(1) As an additional constraint, the design is set up to be small size and low component height.

Switching Frequency

The switching frequency for the TPS5450 is internally set to 500 kHz. It is not possible to adjust the switching frequency.

Input Capacitors

The TPS5450 requires an input decoupling capacitor and, depending on the application, a bulk input capacitor. The minimum recommended decoupling capacitance is 4.7 µF. A high quality ceramic type X5R or X7R is required. For some applications, a smaller value decoupling capacitor may be used, so long as the input voltage and current ripple ratings are not exceeded. The voltage rating must be greater than the maximum input voltage, including ripple.

This input ripple voltage can be approximated by Equation 2 :

$$\Delta V_{IN} = \frac{I_{OUT(MAX)} \times 0.25}{C_{BULK} \times f_{sw}} + \left(I_{OUT(MAX)} \times ESR_{MAX}\right) \quad (2)$$

Where $I_{OUT(MAX)}$ is the maximum load current, f_{SW} is the switching frequency, C_{IN} is the input capacitor value and ESR_{MAX} is the maximum series resistance of the input capacitor. For this design, the input capacitance consists of two 4.7 µF capacitors, C1 and C4, in parallel. An additional high frequency bypass capacitor, C5 is also used.

The maximum RMS ripple current also needs to be checked. For worst case conditions, this can be approximated by Equation 3 :

$$I_{CIN} = \frac{I_{OUT(MAX)}}{2} \quad (3)$$

In this case the input ripple voltage would be 281 mV and the RMS ripple current would be 2.5 A. The maximum voltage across the input capacitors would be VIN max plus delta VIN/2. The chosen input decoupling capacitor is rated for 50 V and the ripple current capacity is greater than 2.5 A each, providing ample margin. It is very important that the maximum ratings for voltage and current are not exceeded under any circumstance.

Additionally some bulk capacitance may be needed, especially if the TPS5450 circuit is not located within about 2 inches from the input voltage source. The value for this capacitor is not critical but it also should be rated to handle the maximum input voltage including ripple voltage and should filter the output so that input ripple voltage is acceptable.

Output Filter Components

Two components need to be selected for the output filter, L1 and C2. Since the TPS5450 is an internally compensated device, a limited range of filter component types and values can be supported.

Inductor Selection

To calculate the minimum value of the output inductor, use Equation 4:

$$L_{MIN} = \frac{V_{OUT(MAX)} \times \left(V_{IN(MAX)} - V_{OUT}\right)}{V_{IN(MAX)} \times K_{IND} \times I_{OUT} \times F_{SW(MIN)}} \quad (4)$$

K_{IND} is a coefficient that represents the amount of inductor ripple current relative to the maximum output current. Three things need to be considered when determining the amount of ripple current in the inductor: the peak to peak ripple current affects the output ripple voltage amplitude, the ripple current affects the peak switch current and the amount of ripple current determines at what point the circuit becomes discontinuous. For designs using the TPS5450, K_{IND} of 0.2 to 0.3 yields good results. Low output ripple voltages can be obtained when paired with the proper output capacitor, the peak switch current will be well below the current limit set point and relatively low load currents can be sourced before discontinuous operation.

For this design example use K_{IND} = 0.2 and the minimum inductor value is calculated to be 10.4 µH. A higher standard value is 15 µH, which is used in this design.

For the output filter inductor it is important that the RMS current and saturation current ratings not be exceeded. The RMS inductor current can be found from Equation 5:

$$I_{L(RMS)} = \sqrt{I^2_{OUT(MAX)} + \frac{1}{12} \times \left(\frac{V_{OUT} \times \left(V_{IN(MAX)} - V_{OUT}\right)}{V_{IN(MAX)} \times L_{OUT} \times F_{SW(MIN)}} \right)^2} \quad (5)$$

and the peak inductor current can be determined with Equation 6:

$$I_{L(PK)} = I_{OUT(MAX)} + \frac{V_{OUT} \times \left(V_{IN(MAX)} - V_{OUT}\right)}{1.6 \times V_{IN(MAX)} \times L_{OUT} \times F_{SW(MIN)}} \quad (6)$$

For this design, the RMS inductor current is 5.004 A, and the peak inductor current is 5.34 A. The chosen inductor is a Sumida CDRH1127/LD-150 15µH. It has a minimum rated current of 5.65 A for both saturation and RMS current. In general, inductor values for use with the TPS5450 are in the range of 10 µH to 100 µH.

Capacitor Selection

The important design factors for the output capacitor are dc voltage rating, ripple current rating, and equivalent series resistance (ESR). The dc voltage and ripple current ratings cannot be exceeded. The ESR is important because along with the inductor ripple current it determines the amount of output ripple voltage. The actual value of the output capacitor is not critical, but some practical limits do exist. Consider the relationship between the desired closed loop crossover frequency of the design and LC corner frequency of the output filter. Due to the design of the internal compensation, it is desirable to keep the closed loop crossover frequency in the range 3 kHz to 30 kHz as this frequency range has adequate phase boost to allow for stable operation. For this design example, it is assumed that the intended closed loop crossover frequency will be between 2590 Hz and 24 kHz and also below the ESR zero of the output capacitor. Under these conditions the closed loop crossover frequency is related to the LC corner frequency by:

$$f_{CO} = \frac{f_{LC}^2}{85\, V_{OUT}} \quad (7)$$

And the desired output capacitor value for the output filter to:

$$C_{OUT} = \frac{1}{3357 \times L_{OUT} \times f_{CO} \times V_{OUT}} \quad (8)$$

For a desired crossover of 12 kHz and a 15-µH inductor, the calculated value for the output capacitor is 330 µF. The capacitor type should be chosen so that the ESR zero is above the loop crossover. The maximum ESR should be:

$$ESR_{MAX} = \frac{1}{2\pi \times C_{OUT} \times f_{CO}} \quad (9)$$

The maximum ESR of the output capacitor also determines the amount of output ripple as specified in the initial design parameters. The output ripple voltage is the inductor ripple current times the ESR of the output filter. Check that the maximum specified ESR as listed in the capacitor data sheet results in an acceptable output ripple voltage:

$$V_{PP}\,(MAX) = \frac{ESR_{MAX} \times V_{OUT} \times \left(V_{IN(MAX)} - V_{OUT}\right)}{N_C \times V_{IN(MAX)} \times L_{OUT} \times F_{SW}} \quad (10)$$

Where:

ΔV_{PP} is the desired peak-to-peak output ripple.
N_C is the number of parallel output capacitors.
F_{SW} is the switching frequency.

For this design example, a single 330-µF output capacitor is chosen for C3. The calculated RMS ripple current is 143 mA and the maximum ESR required is 40 mΩ. A capacitor that meets these requirements is a Sanyo Poscap 10TPB330M, rated at 10 V with a maximum ESR of 35 mΩ and a ripple current rating of 3 A. An additional small 0.1-µF ceramic bypass capacitor, C6 is also used in this design.

The minimum ESR of the output capacitor should also be considered. For good phase margin, the ESR zero when the ESR is at a minimum should not be too far above the internal compensation poles at 24 kHz and 54 kHz.

The selected output capacitor must also be rated for a voltage greater than the desired output voltage plus one half the ripple voltage. Any derating amount must also be included. The maximum RMS ripple current in the output capacitor is given by Equation 11:

$$I_{COUT(RMS)} = \frac{1}{\sqrt{12}} \times \left(\frac{V_{OUT} \times \left(V_{IN(MAX)} - V_{OUT} \right)}{V_{IN(MAX)} \times L_{OUT} \times F_{SW} \times N_C} \right) \quad (11)$$

Where:

N_C is the number of output capacitors in parallel.

F_{SW} is the switching frequency.

Other capacitor types can be used with the TPS5450, depending on the needs of the application.

Output Voltage Setpoint

The output voltage of the TPS5450 is set by a resistor divider (R1 and R2) from the output to the VSENSE pin. Calculate the R2 resistor value for the output voltage of 5 V using Equation 12:

$$R2 = \frac{R1 \times 1.221}{V_{OUT} - 1.221} \quad (12)$$

For any TPS5450 design, start with an R1 value of 10 kΩ. For an output voltage closest to but at least 5 V, R2 is 3.16 kΩ.

Boot Capacitor

The boot capacitor should be 0.01 µF.

Catch Diode

The TPS5450 is designed to operate using an external catch diode between PH and GND. The selected diode must meet the absolute maximum ratings for the application: Reverse voltage must be higher than the maximum voltage at the PH pin, which is VINMAX + 0.5 V. Peak current must be greater than IOUTMAX plus on half the peak to peak inductor current. Forward voltage drop should be small for higher efficiencies. It is important to note that the catch diode conduction time is typically longer than the high-side FET on time, so attention paid to diode parameters can make a marked improvement in overall efficiency. Additionally, check that the device chosen is capable of dissipating the power losses. For this design, a Diodes, Inc. B540A is chosen, with a reverse voltage of 40 V, forward current of 5 A, and a forward voltage drop of 0.5 V.

ADVANCED INFORMATION

Output Voltage Limitations

Due to the internal design of the TPS5450, there are both upper and lower output voltage limits for any given input voltage. The upper limit of the output voltage set point is constrained by the maximum duty cycle of 87% and is given by:

$$V_{OUTMAX} = 0.87 \times \left(\left(V_{INMIN} - I_{OMAX} \times 0.230 \right) + V_D \right) - \left(I_{OMAX} \times R_L \right) - V_D \quad (13)$$

Where

V_{INMIN} = minimum input voltage

I_{OMAX} = maximum load current

V_D = catch diode forward voltage.

R_L= output inductor series resistance.

This equation assumes maximum on resistance for the internal high side FET.

The lower limit is constrained by the minimum controllable on time which may be as high as 200 ns. The approximate minimum output voltage for a given input voltage and minimum load current is given by:

$$V_{OUTMIN} = 0.12 \times \left(\left(V_{INMAX} - I_{OMIN} \times 0.110\right) + V_D\right) - \left(I_{OMIN} \times R_L\right) - V_D \quad (14)$$

Where

V_{INMAX} = maximum input voltage

I_{OMIN} = minimum load current

V_D = catch diode forward voltage.

R_L= output inductor series resistance.

This equation assumes nominal on resistance for the high side FET and accounts for worst case variation of operating frequency set point. Any design operating near the operational limits of the device should be carefully checked to assure proper functionality.

Internal Compensation Network

The design equations given in the example circuit can be used to generate circuits using the TPS5450. These designs are based on certain assumptions and will tend to always select output capacitors within a limited range of ESR values. If a different capacitor type is desired, it may be possible to fit one to the internal compensation of the TPS5450. Equation 15 gives the nominal frequency response of the internal voltage-mode type III compensation network:

$$H(s) = \frac{\left(1 + \frac{s}{2\pi \times Fz1}\right) \times \left(1 + \frac{s}{2\pi \times Fz2}\right)}{\left(\frac{s}{2\pi \times Fp0}\right) \times \left(1 + \frac{s}{2\pi \times Fp1}\right) \times \left(1 + \frac{s}{2\pi \times Fp2}\right) \times \left(1 + \frac{s}{2\pi \times Fp3}\right)} \quad (15)$$

Where

Fp0 = 2165 Hz, Fz1 = 2170 Hz, Fz2 = 2590 Hz

Fp1 = 24 kHz, Fp2 = 54 kHz, Fp3 = 440 kHz

Fp3 represents the non-ideal parasitics effect.

Using this information along with the desired output voltage, feed forward gain and output filter characteristics, the closed loop transfer function can be derived.

Thermal Calculations

The following formulas show how to estimate the device power dissipation under continuous conduction mode operations. They should not be used if the device is working at light loads in the discontinuous conduction mode.

Conduction Loss: Pcon = I_{OUT}^2 x $R_{DS(on)}$ x V_{OUT}/V_{IN}

Switching Loss: Psw = V_{IN} x I_{OUT} x 0.01

Quiescent Current Loss: Pq = V_{IN} x 0.01

Total Loss: Ptot = Pcon + Psw + Pq

Given T_A => Estimated Junction Temperature: $T_J = T_A$ + Rth x Ptot

Given T_{JMAX} = 125°C => Estimated Maximum Ambient Temperature: $T_{AMAX} = T_{JMAX}$ – Rth x Ptot

PERFORMANCE GRAPHS

The performance graphs (Figure 12 through Figure 18) are applicable to the circuit in Figure 11. Ta = 25 °C. unless otherwise specified.

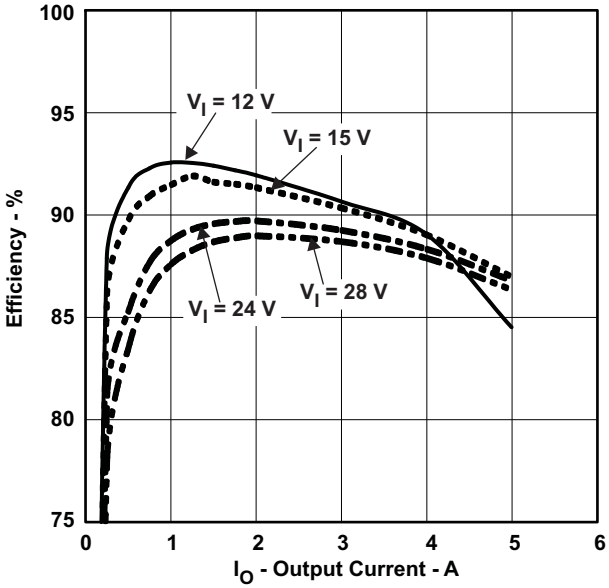


Figure 12. Efficiency vs. Output Current

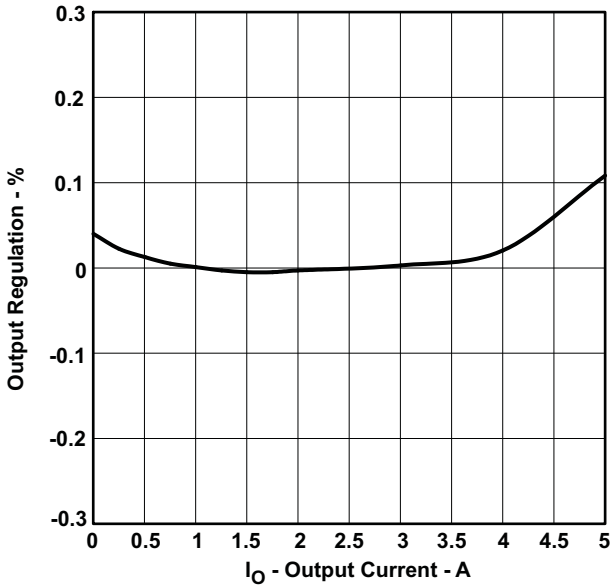


Figure 13. Output Regulation % vs. Output Current

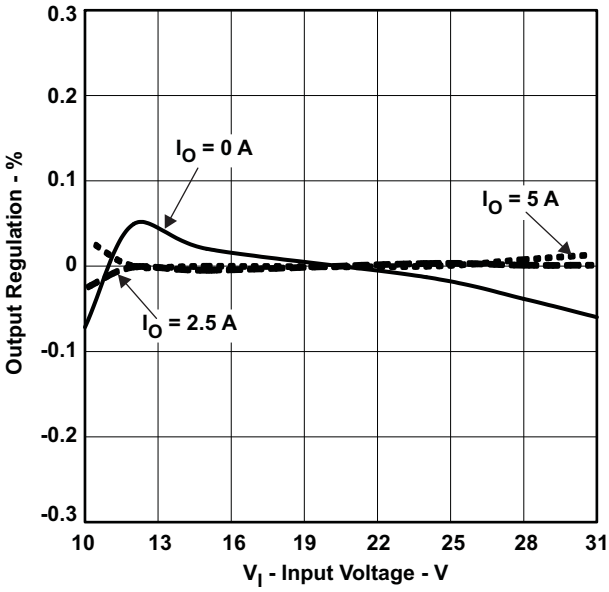


Figure 14. Output Regulation % vs. Input Voltage

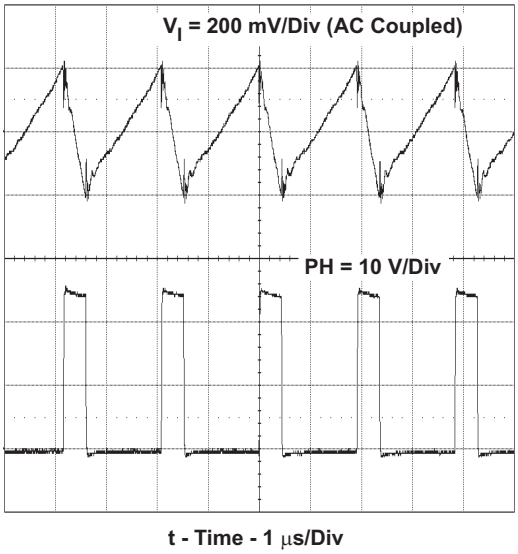


Figure 15. Input Voltage Ripple and PH Node, Io = 5 A.

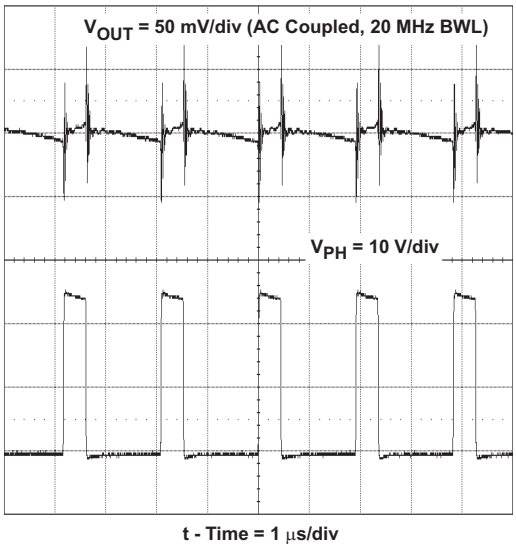


Figure 16. Output Voltage Ripple and PH Node, Io = 5 A

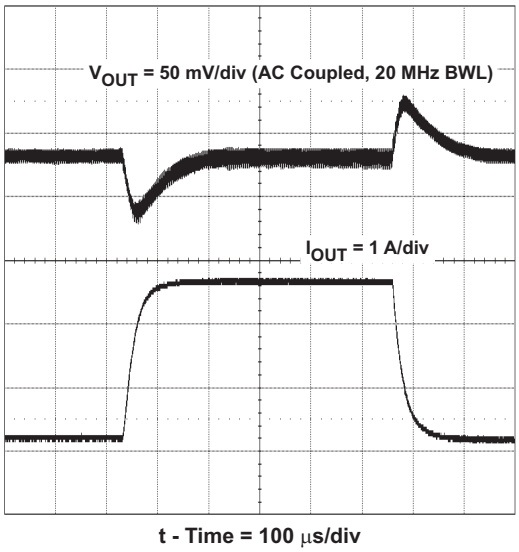


Figure 17. Transient Response, Io Step 1.25 to 3.75 A.

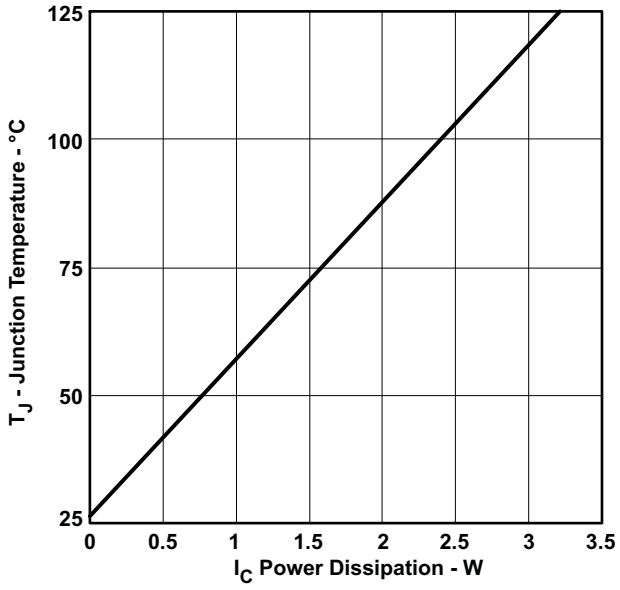


Figure 18. TPS5450 Power Dissipation vs Junction Temperature.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
TPS5450DDA	ACTIVE	SO Power PAD	DDA	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS5450DDAG4	ACTIVE	SO Power PAD	DDA	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS5450DDAR	ACTIVE	SO Power PAD	DDA	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS5450DDARG4	ACTIVE	SO Power PAD	DDA	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

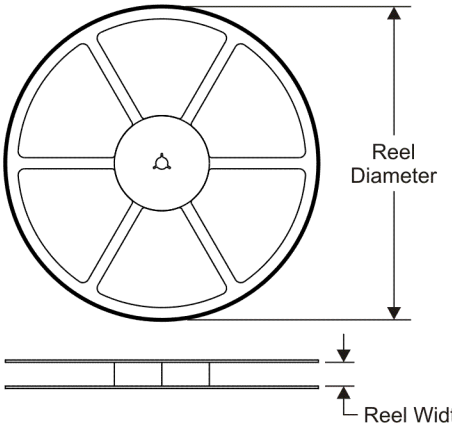
(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

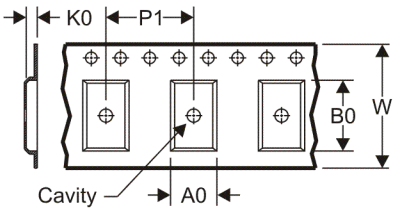
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

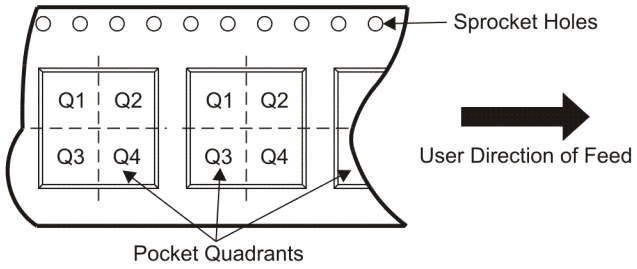


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

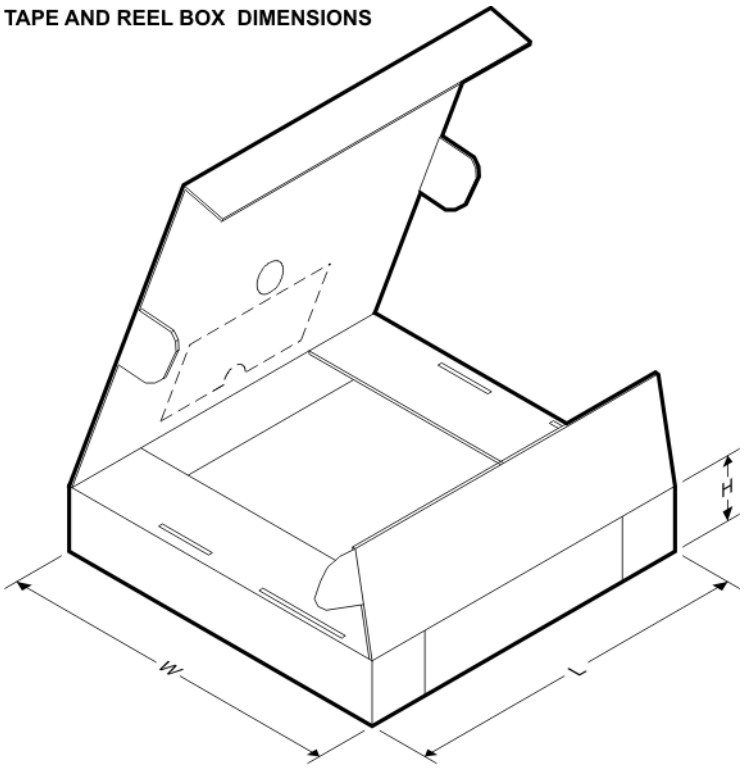
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS5450DDAR	SO Power PAD	DDA	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

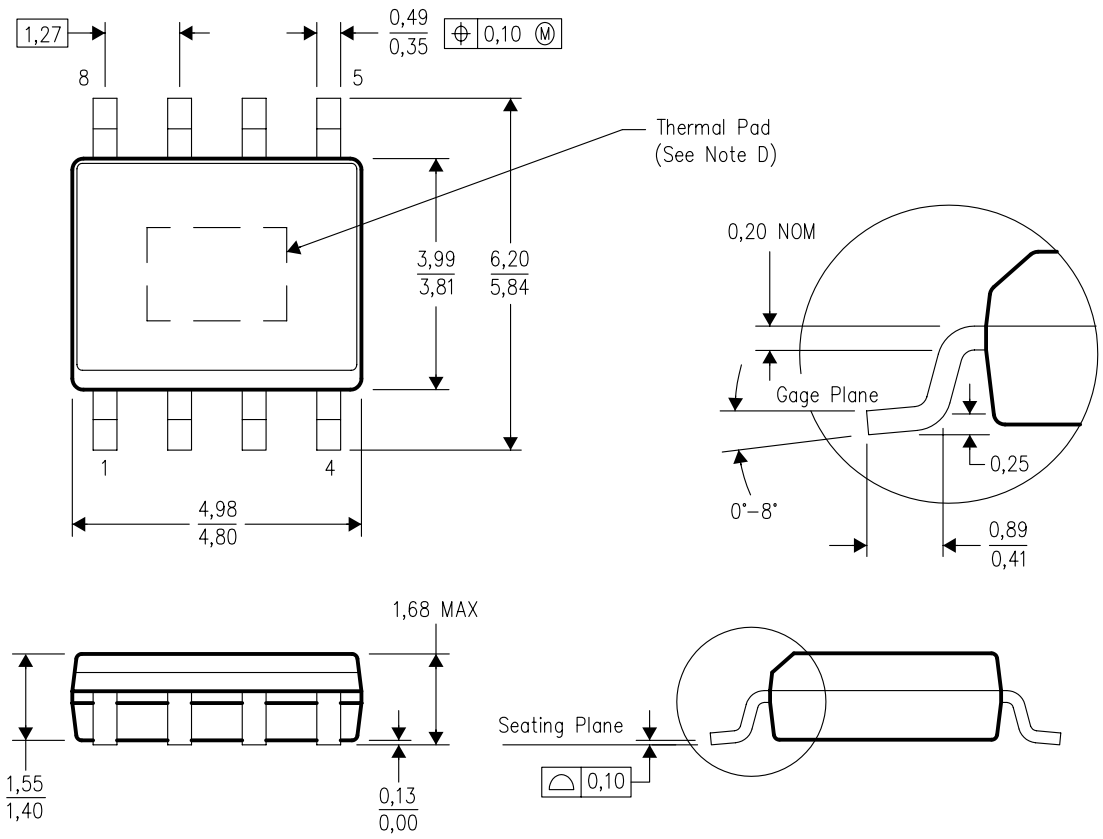
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS5450DDAR	SO PowerPAD	DDA	8	2500	346.0	346.0	29.0

DDA (R–PDSO–G8) PowerPAD™ PLASTIC SMALL–OUTLINE PACKAGE



4202561/D 04/04

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.

PowerPAD is a trademark of Texas Instruments.

THERMAL PAD MECHANICAL DATA

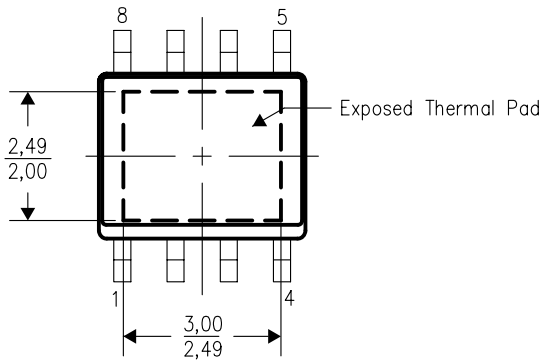
DDA (R–PDSO–G8)

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

NOTE: All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions

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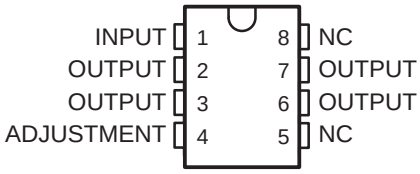
SLVS004C – APRIL 1979 – REVISED JULY 1999

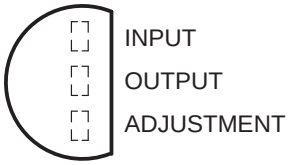
- **Output Voltage Range Adjustable From 1.2 V to 32 V When Used With an External Resistor Divider**
- **Output Current Capability of 100 mA**
- **Input Regulation Typically 0.01% Per Input-Voltage Change**
- **Output Regulation Typically 0.5%**
- **Ripple Rejection Typically 80 dB**

D PACKAGE
(TOP VIEW)



NC – No internal connection
OUTPUT terminals are all internally connected.

LP PACKAGE
(TOP VIEW)



description

The TL317 is an adjustable three-terminal positive-voltage regulator capable of supplying 100 mA over an output-voltage range of 1.2 V to 32 V. It is exceptionally easy to use and requires only two external resistors to set the output voltage.

In addition to higher performance than fixed regulators, this regulator offers full overload protection available only in integrated circuits. Included on the chip are current-limiting and thermal-overload protection. All overload-protection circuitry remains fully functional, even when ADJUSTMENT is disconnected. Normally, no capacitors are needed unless the device is situated far from the input filter capacitors, in which case an input bypass is needed. An optional output capacitor can be added to improve transient response. ADJUSTMENT can be bypassed to achieve very high ripple rejection, which is difficult to achieve with standard three-terminal regulators.

In addition to replacing fixed regulators, the TL317 regulator is useful in a wide variety of other applications. Since the regulator is floating and sees only the input-to-output differential voltage, supplies of several hundred volts can be regulated as long as the maximum input-to-output differential is not exceeded. Its primary application is that of a programmable output regulator, but by connecting a fixed resistor between ADJUSTMENT and OUTPUT, this device can be used as a precision current regulator. Supplies with electronic shutdown can be achieved by clamping ADJUSTMENT to ground, programming the output to 1.2 V, where most loads draw little current.

The TL317C is characterized for operation over the virtual junction temperature range of 0°C to 125°C.

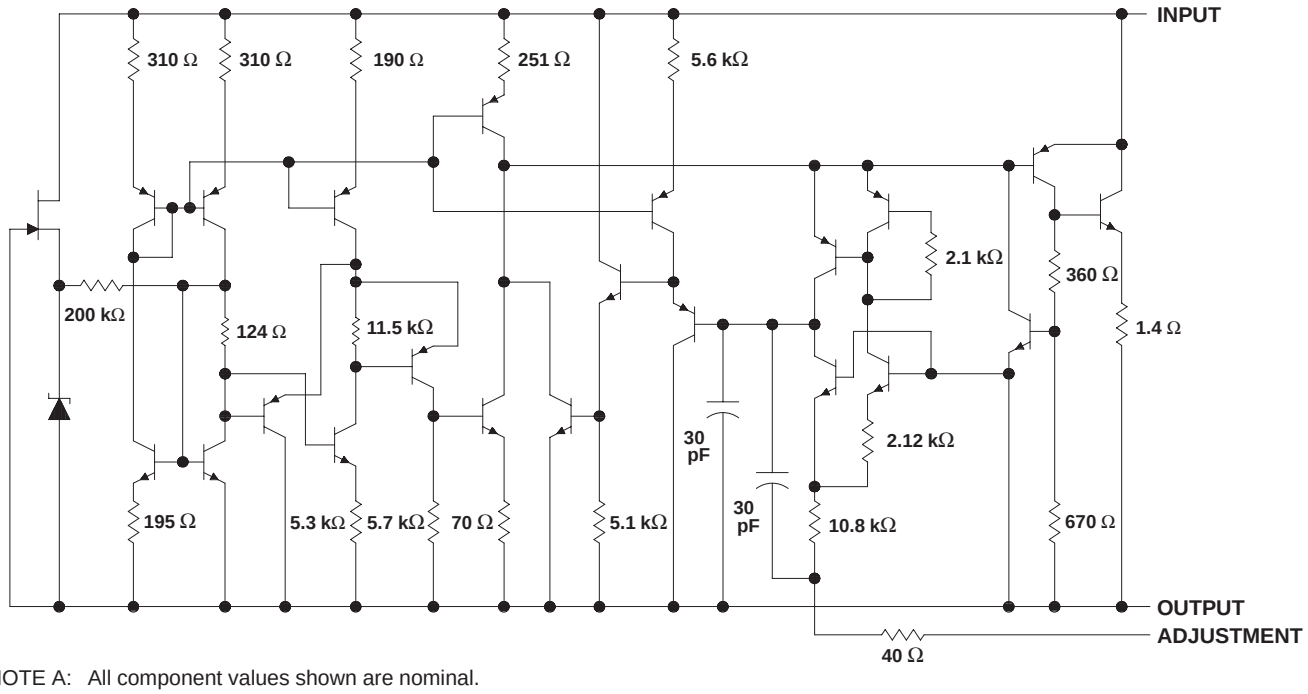
AVAILABLE OPTIONS

T_J	PACKAGED DEVICES		CHIP FORM (Y)
	SMALL OUTLINE (D)	PLASTIC (LP)	
0°C to 125°C	TL317CD	TL317CLP	TL317Y

The D and LP packages are available taped and reeled. Add the suffix R to device type (e.g., TL317CDR). Chip forms are tested at 25°C.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

schematic



NOTE A: All component values shown are nominal.

absolute maximum ratings over operating temperature range (unless otherwise noted)†

Input-to-output differential voltage, $V_I – V_O$ . . . . . 35 V
Operating free-air, T_A, case, or virtual-junction temperature range, T_J: TL317C . . . . . 0°C to 150°C
Package thermal impedance, θ_{JA} (see Notes 1 and 2): D package . . . . . 97°C/W
LP package . . . . . 156°C/W
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. Maximum power dissipation is a function of $T_J(max)$, θ_{JA}, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(max) – T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can impact reliability.
2. The package thermal impedance is calculated in accordance with JESD 51, except for through-hole packages, which use a trace length of zero.

recommended operating conditions

		MIN	MAX	UNIT
Input-to-output voltage differential, $V_I – V_O$			35	V
Output current, I_O		2.5	100	mA
Operating virtual-junction temperature, T_J	TL317C	0	125	°C

electrical characteristics over recommended operating virtual-junction temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†		TL317C			UNIT
			MIN	TYP	MAX	
Input voltage regulation (see Note 3)	$V_I - V_O$ = 5 V to 35 V	T_J = 25°C		0.01	0.02	%V
		I_O = 2.5 mA to 100 mA		0.02	0.05	
Ripple regulation	V_O = 10 V,	f = 120 Hz		65		dB
	V_O = 10 V, 10-μF capacitor between ADJUSTMENT and ground		66	80		
Output voltage regulation	V_I = 5 V to 35 V, I_O = 2.5 mA to 100 mA, T_J = 25°C	$V_O \le 5$ V		25		mV
		$V_O \ge 5$ V		5		mV/V
	V_I = 5 V to 35 V, I_O = 2.5 mA to 100 mA	$V_O \le 5$ V		50		mV
		$V_O \ge 5$ V		10		mV/V
Output voltage change with temperature	T_J = 0°C to 125°C			10		mV/V
Output voltage long-term drift	After 1000 hours at T_J = 125°C and $V_I - V_O$ = 35 V			3	10	mV/V
Output noise voltage	f = 10 Hz to 10 kHz,	T_J = 25°C		30		μV/V
Minimum output current to maintain regulation	$V_I - V_O$ = 35 V			1.5	2.5	mA
Peak output current	$V_I - V_O \le 35$ V		100	200		mA
ADJUSTMENT current				50	100	μA
Change in ADJUSTMENT current	$V_I - V_O$ = 2.5 V to 35 V,	I_O = 2.5 mA to 100 mA		0.2	5	μA
Reference voltage (output to ADJUSTMENT)	$V_I - V_O$ = 5 V to 35 V, P ≤ rated dissipation	I_O = 2.5 mA to 100 mA,	1.2	1.25	1.3	V

† Unless otherwise noted, these specifications apply for the following test conditions: $V_I - V_O$ = 5 V and I_O = 40 mA. Pulse-testing techniques must be used that maintain the junction temperature as close to the ambient temperature as possible. All characteristics are measured with a 0.1-μF capacitor across the input and a 1-μF capacitor across the output.

NOTE 3: Input voltage regulation is expressed here as the percentage change in output voltage per 1-V change at the input.

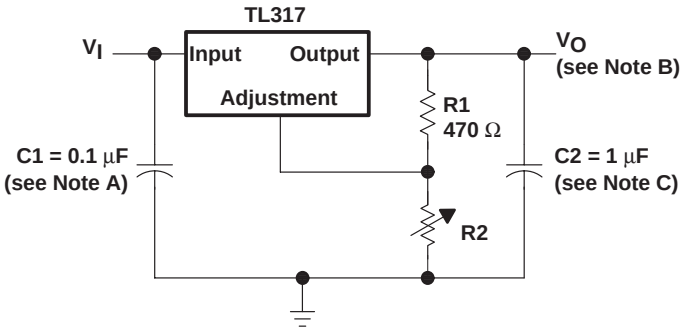
electrical characteristics over recommended operating conditions, T_J = 25°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS†		TL317Y			UNIT
			MIN	TYP	MAX	
Input voltage regulation (see Note 3)	$V_I - V_O$ = 5 V to 35 V			0.01		%V
Ripple regulation	V_O = 10 V,	f = 120 Hz		65		dB
	V_O = 10 V, 10-μF capacitor between ADJUSTMENT and ground			80		
Output voltage regulation	I_O = 2.5 mA to 100 mA	$V_O \le 5$ V		25		mV
		$V_O \ge 5$ V		5		mV/V
Output noise voltage	f = 10 Hz to 10 kHz			30		μV/V
Minimum output current to maintain regulation	$V_I - V_O$ = 35 V			1.5		mA
Peak output current	$V_I - V_O \le 35$ V			200		mA
ADJUSTMENT current				50		μA
Change in ADJUSTMENT current	$V_I - V_O$ = 2.5 V to 35 V,	I_O = 2.5 mA to 100 mA		0.2		μA
Reference voltage (output to ADJUSTMENT)	$V_I - V_O$ = 5 V to 35 V, P ≤ rated dissipation	I_O = 2.5 mA to 100 mA,		1.25		V

† Unless otherwise noted, these specifications apply for the following test conditions: $V_I - V_O$ = 5 V and I_O = 40 mA. Pulse-testing techniques must be used that maintain the junction temperature as close to the ambient temperature as possible. All characteristics are measured with a 0.1-μF capacitor across the input and a 1-μF capacitor across the output.

NOTE 3: Input voltage regulation is expressed here as the percentage change in output voltage per 1-V change at the input.

APPLICATION INFORMATION



NOTES: A. Use of an input bypass capacitor is recommended if regulator is far from the filter capacitors.

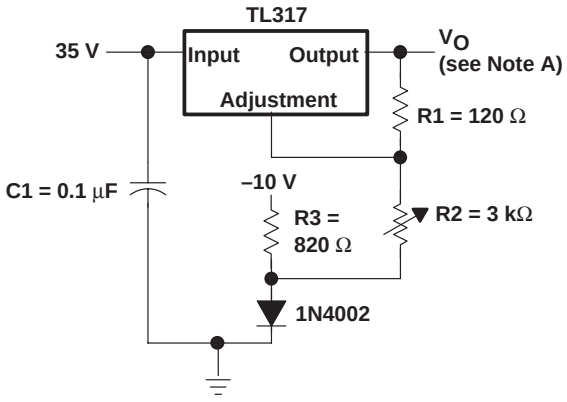
B. Output voltage is calculated from the equation:

$$V_O = V_{ref}\left(1 + \frac{R2}{R1}\right)$$

where: V_{ref} equals the difference between OUTPUT and ADJUSTMENT voltages (≈1.25 V).

C. Use of an output capacitor improves transient response but is optional.

Figure 1. Adjustable Voltage Regulator

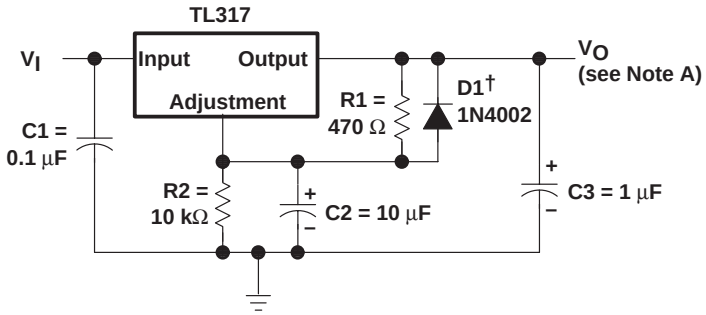


NOTE A: Output voltage is calculated from the equation:

$$V_O = V_{ref}\left(1 + \frac{R2 + R3}{R1}\right) - 10\ V$$

where: V_{ref} equals the difference between OUTPUT and ADJUSTMENT voltages (≈1.25 V).

Figure 2. 0-V to 30-V Regulator Circuit



† D1 discharges C2 if output is shorted to ground.

NOTE A: Use of an output capacitor improves transient response but is optional.

Figure 3. Regulator Circuit With Improved Ripple Rejection

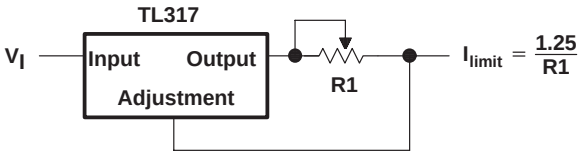


Figure 4. Precision Current-Limiter Circuit

APPLICATION INFORMATION

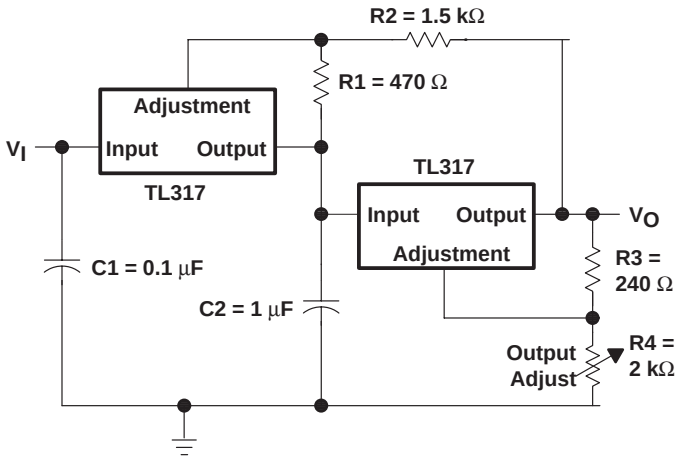


Figure 5. Tracking Preregulator Circuit

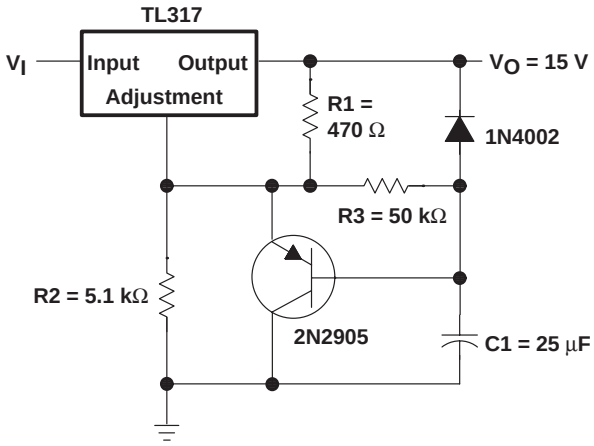


Figure 6. Slow Turnon 15-V Regulator Circuit

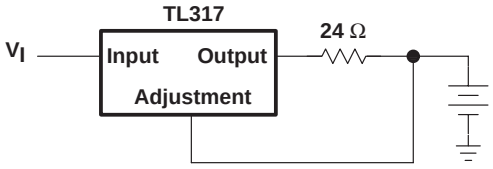


Figure 7. 50-mA Constant-Current Battery Charger Circuit

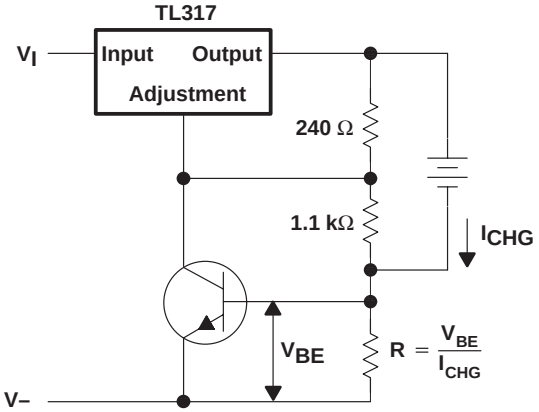
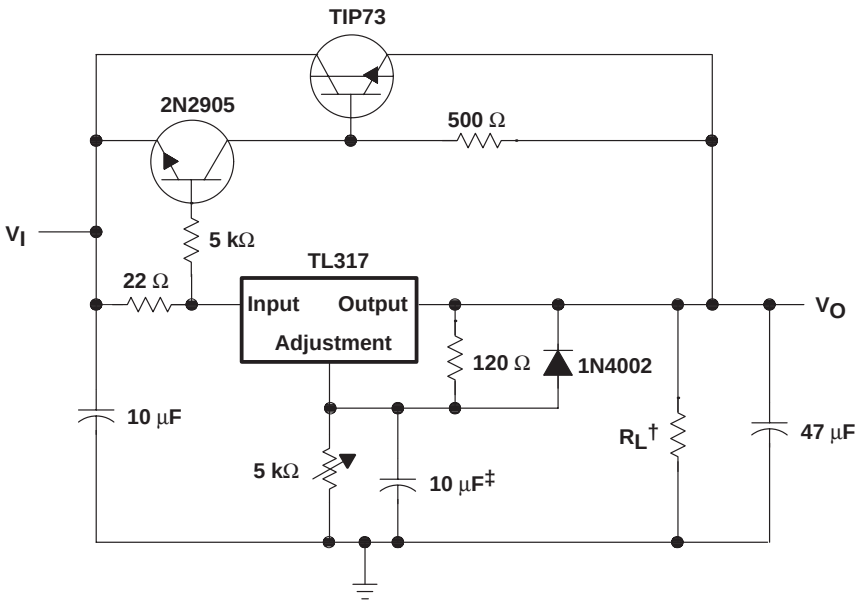


Figure 8. Current-Limited 6-V Charger

APPLICATION INFORMATION



† Minimum load current is 30 mA.
‡ Optional capacitor improves ripple rejection

Figure 9. High-Current Adjustable Regulator

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National Semiconductor

February 5, 2009

LP38691/LP38693

500mA Low Dropout CMOS Linear Regulators
Stable with Ceramic Output Capacitors

General Description

The LP38691/3 low dropout CMOS linear regulators provide tight output tolerance (2.0% typical), extremely low dropout voltage (250 mV @ 500mA load current, V_{OUT} = 5V), and excellent AC performance utilizing ultra low ESR ceramic output capacitors.

The low thermal resistance of the LLP, SOT-223 and TO-252 packages allow the full operating current to be used even in high ambient temperature environments.

The use of a PMOS power transistor means that no DC base drive current is required to bias it allowing ground pin current to remain below 100 µA regardless of load current, input voltage, or operating temperature.

Dropout Voltage: 250 mV (typ) @ 500mA (typ. 5V out).

Ground Pin Current: 55 µA (typ) at full load.

Precision Output Voltage: 2.0% (25°C) accuracy.

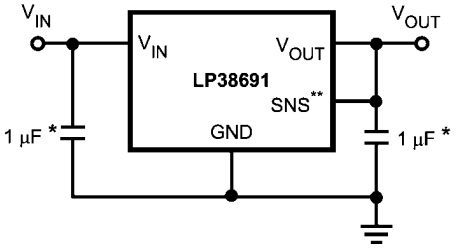
Features

- 2.0% output accuracy (25°C)
- Low dropout voltage: 250 mV @ 500mA (typ, 5V out)
- Wide input voltage range (2.7V to 10V)
- Precision (trimmed) bandgap reference
- Guaranteed specs for -40°C to +125°C
- 1µA off-state quiescent current
- Thermal overload protection
- Foldback current limiting
- T0-252, SOT-223 and 6-Lead LLP packages
- Enable pin (LP38693)

Applications

- Hard Disk Drives
- Notebook Computers
- Battery Powered Devices
- Portable Instrumentation

Typical Application Circuits



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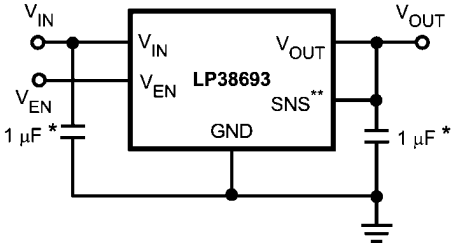

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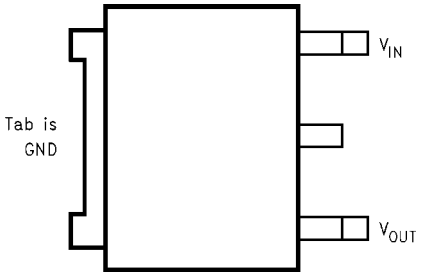
Note: * Minimum value required for stability.
**LLP package devices only.

Connection Diagrams



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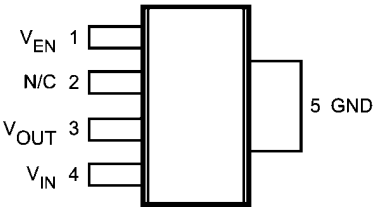
TO-252, Top View
LP38691DT-X.X



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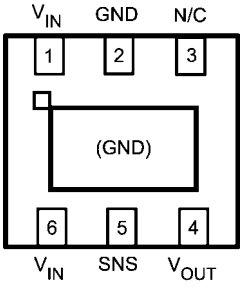
SOT-223, Top View
LP38693MP-X.X



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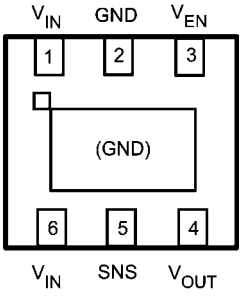
6-Lead LLP, Bottom View
LP38691SD-X.X



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6-Lead LLP, Bottom View
LP38693SD-X.X

Pin Descriptions

Pin	Description
V_{IN}	This is the input supply voltage to the regulator. For LLP devices, both V_{IN} pins must be tied together for full current operation (250mA maximum per pin).
GND	Circuit ground for the regulator. This is connected to the die through the lead frame, and also functions as the heat sink when the large ground pad is soldered down to a copper plane.
SNS	Output sense pin allows remote sensing at the load which will eliminate the error in output voltage due to voltage drops caused by the resistance in the traces between the regulator and the load. This pin must be tied to V_{OUT}.
V_{EN}	The enable pin allows the part to be turned ON and OFF by pulling this pin high or low.
V_{OUT}	Regulated output voltage

Ordering Information

Order Number	Package Marking	Package Type	Package Drawing	Supplied As
LP38691SD-1.8	L118B	6-Lead LLP	SDE06A	1000 Units Tape and Reel
LP38691SD-2.5	L119B	6-Lead LLP	SDE06A	1000 Units Tape and Reel
LP38691SD-3.3	L120B	6-Lead LLP	SDE06A	1000 Units Tape and Reel
LP38691SD-5.0	L121B	6-Lead LLP	SDE06A	1000 Units Tape and Reel
LP38691DT-1.8	LP38691DT-1.8	TO-252	TD03B	75 Units per Rail
LP38691DT-2.5	LP38691DT-2.5	TO-252	TD03B	75 Units per Rail
LP38691DT-3.3	LP38691DT-3.3	TO-252	TD03B	75 Units per Rail
LP38691DT-5.0	LP38691DT-5.0	TO-252	TD03B	75 Units per Rail
LP38693SD-1.8	L128B	6-Lead LLP	SDE06A	1000 Units Tape and Reel
LP38693SD-2.5	L129B	6-Lead LLP	SDE06A	1000 Units Tape and Reel
LP38693SD-3.3	L130B	6-Lead LLP	SDE06A	1000 Units Tape and Reel
LP38693SD-5.0	L131B	6-Lead LLP	SDE06A	1000 Units Tape and Reel
LP38693MP-1.8	LJVB	SOT-223	MP05A	1000 Units Tape and Reel
LP38693MP-2.5	LJXB	SOT-223	MP05A	1000 Units Tape and Reel
LP38693MP-3.3	LJYB	SOT-223	MP05A	1000 Units Tape and Reel
LP38693MP-5.0	LJZB	SOT-223	MP05A	1000 Units Tape and Reel
LP38691SDX-1.8	L118B	6-Lead LLP	SDE06A	4500 Units Tape and Reel
LP38691SDX-2.5	L119B	6-Lead LLP	SDE06A	4500 Units Tape and Reel
LP38691SDX-3.3	L120B	6-Lead LLP	SDE06A	4500 Units Tape and Reel
LP38691SDX-5.0	L121B	6-Lead LLP	SDE06A	4500 Units Tape and Reel
LP38691DTX-1.8	LP38691DT-1.8	TO-252	TD03B	2500 Units Tape and Reel
LP38691DTX-2.5	LP38691DT-2.5	TO-252	TD03B	2500 Units Tape and Reel
LP38691DTX-3.3	LP38691DT-3.3	TO-252	TD03B	2500 Units Tape and Reel
LP38691DTX-5.0	LP38691DT-5.0	TO-252	TD03B	2500 Units Tape and Reel
LP38693SDX-1.8	L128B	6-Lead LLP	SDE06A	4500 Units Tape and Reel
LP38693SDX-2.5	L129B	6-Lead LLP	SDE06A	4500 Units Tape and Reel
LP38693SDX-3.3	L130B	6-Lead LLP	SDE06A	4500 Units Tape and Reel
LP38693SDX-5.0	L131B	6-Lead LLP	SDE06A	4500 Units Tape and Reel
LP38693MPX-1.8	LJVB	SOT-223	MP05A	2000 Units Tape and Reel
LP38693MPX-2.5	LJXB	SOT-223	MP05A	2000 Units Tape and Reel
LP38693MPX-3.3	LJYB	SOT-223	MP05A	2000 Units Tape and Reel
LP38693MPX-5.0	LJZB	SOT-223	MP05A	2000 Units Tape and Reel

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Storage Temperature Range	−65°C to +150°C
Lead Temp. (Soldering, 5 seconds)	260°C
ESD Rating (Note 3)	2 kV
Power Dissipation (Note 2)	Internally Limited
V(max) All pins (with respect to GND)	-0.3V to 12V
I_{OUT}	Internally Limited
Junction Temperature	−40°C to +150°C

Operating Ratings

V_{IN} Supply Voltage	2.7V to 10V
Operating Junction Temperature Range	−40°C to +125°C

Electrical Characteristics

Limits in standard typeface are for T_J = 25°C, and limits in **boldface type** apply over the full operating temperature range. Unless otherwise specified: $V_{IN} = V_{OUT} + 1V$, $C_{IN} = C_{OUT} = 10\ \mu F$, I_{LOAD} = 10mA. Min/Max limits are guaranteed through testing, statistical correlation, or design.

Symbol	Parameter	Conditions	Min	Typ (Note 4)	Max	Units
V_O	Output Voltage Tolerance		-2.0		2.0	$\%V_{OUT}$
		100 µA < I_L < 0.5A $V_O + 1V \le V_{IN} \le 10V$	**-4.0**		**4.0**	
$\Delta V_O/\Delta V_{IN}$	Output Voltage Line Regulation (Note 6)	$V_O + 0.5V \le V_{IN} \le 10V$ I_L = 25mA		0.03	**0.1**	%/V
$\Delta V_O/\Delta I_L$	Output Voltage Load Regulation (Note 7)	1 mA < I_L < 0.5A $V_{IN} = V_O + 1V$		1.8	**5**	%/A
$V_{IN} - V_{OUT}$	Dropout Voltage (Note 8)	(V_O = 2.5V) I_L = 0.1A I_L = 0.5A		80 430	**145** **725**	mV
		(V_O = 3.3V) I_L = 0.1A I_L = 0.5A		65 330	**110** **550**	
		(V_O = 5V) I_L = 0.1A I_L = 0.5A		45 250	**100** **450**	
I_Q	Quiescent Current	$V_{IN} \le 10V$, I_L =100 µA - 0.5A		55	**100**	µA
		$V_{EN} \le 0.4V$, (LP38693 Only)		0.001	1	
I_L(MIN)	Minimum Load Current	$V_{IN} - V_O \le 4V$			**100**	
I_{FB}	Foldback Current Limit	$V_{IN} - V_O > 5V$		350		mA
		$V_{IN} - V_O < 4V$		850		
PSRR	Ripple Rejection	$V_{IN} = V_O$ + 2V(DC), with 1V(p-p) / 120Hz Ripple		55		dB
T_{SD}	Thermal Shutdown Activation (Junction Temp)			160		°C
T_{SD} (HYST)	Thermal Shutdown Hysteresis (Junction Temp)			10		

Symbol	Parameter	Conditions	Min	**Typ** (Note 4)	Max	Units
e_n	Output Noise	BW = 10Hz to 10kHz V_O = 3.3V		0.7		$\mu V/\sqrt{Hz}$
V_O (LEAK)	Output Leakage Current	$V_O = V_O(NOM) + 1V$ @ $10V_{IN}$		0.5	12	µA
V_{EN}	Enable Voltage (LP38693 Only)	Output = OFF			**0.4**	V
		Output = ON, V_{IN} = 4V	**1.8**			
		Output = ON, V_{IN} = 6V	**3.0**			
		Output = ON, V_{IN} = 10V	**4.0**			
I_{EN}	Enable Pin Leakage (LP38693 Only)	V_{EN} = 0V or 10V, V_{IN} = 10V	-1	0.001	1	µA

Note 1: Absolute maximum ratings indicate limits beyond which damage to the component may occur. Operating ratings indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits. For guaranteed specifications, see Electrical Characteristics. Specifications do not apply when operating the device outside of its rated operating conditions.

Note 2: At elevated temperatures, device power dissipation must be derated based on package thermal resistance and heatsink values (if a heatsink is used). The junction-to-ambient thermal resistance (θ_{J-A}) for the TO-252 is approximately 90°C/W for a PC board mounting with the device soldered down to minimum copper area (less than 0.1 square inch). If one square inch of copper is used as a heat dissipator for the TO-252, the θ_{J-A} drops to approximately 50°C/W. The SOT-223 package has a θ_{J-A} of approximately 125°C/W when soldered down to a minimum sized pattern (less than 0.1 square inch) and approximately 70°C/W when soldered to a copper area of one square inch. The θ_{J-A} values for the LLP package are also dependent on trace area, copper thickness, and the number of thermal vias used (refer to application note AN-1187). If power disspation causes the junction temperature to exceed specified limits, the device will go into thermal shutdown.

Note 3: ESD is tested using the human body model which is a 100pF capacitor discharged through a 1.5k resistor into each pin.

Note 4: Typical numbers represent the most likely parametric norm for 25°C operation.

Note 5: If used in a dual-supply system where the regulator load is returned to a negative supply, the output pin must be diode clamped to ground.

Note 6: Output voltage line regulation is defined as the change in output voltage from nominal value resulting from a change in input voltage.

Note 7: Output voltage load regulation is defined as the change in output voltage from nominal value as the load current increases from 1mA to full load.

Note 8: Dropout voltage is defined as the minimum input to output differential required to maintain the output within 100mV of nominal value.

Block Diagrams

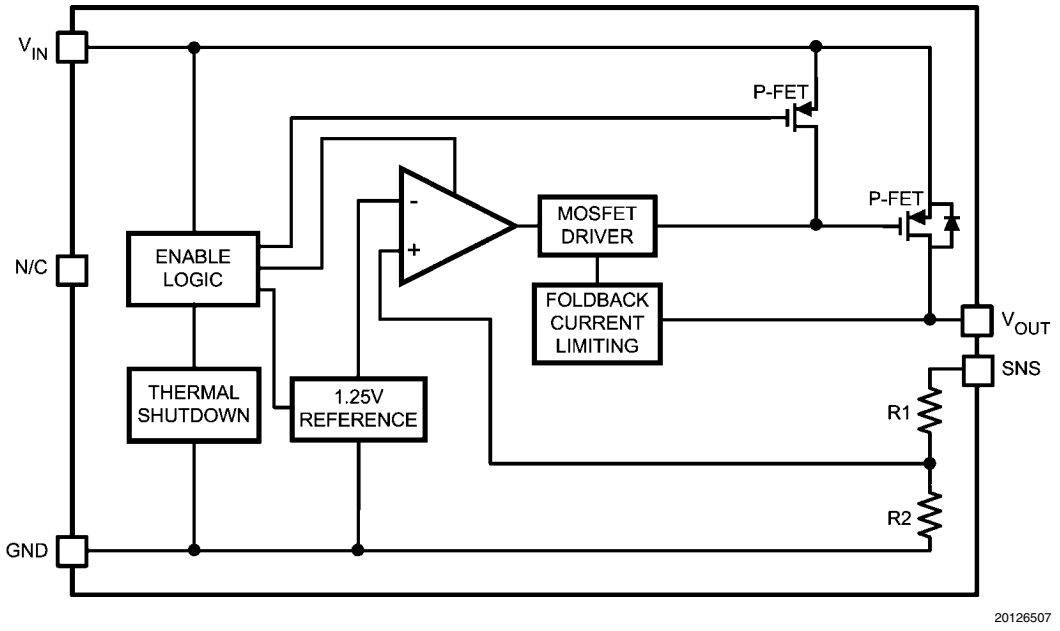


FIGURE 1. LP38691 Functional Diagram (LLP)

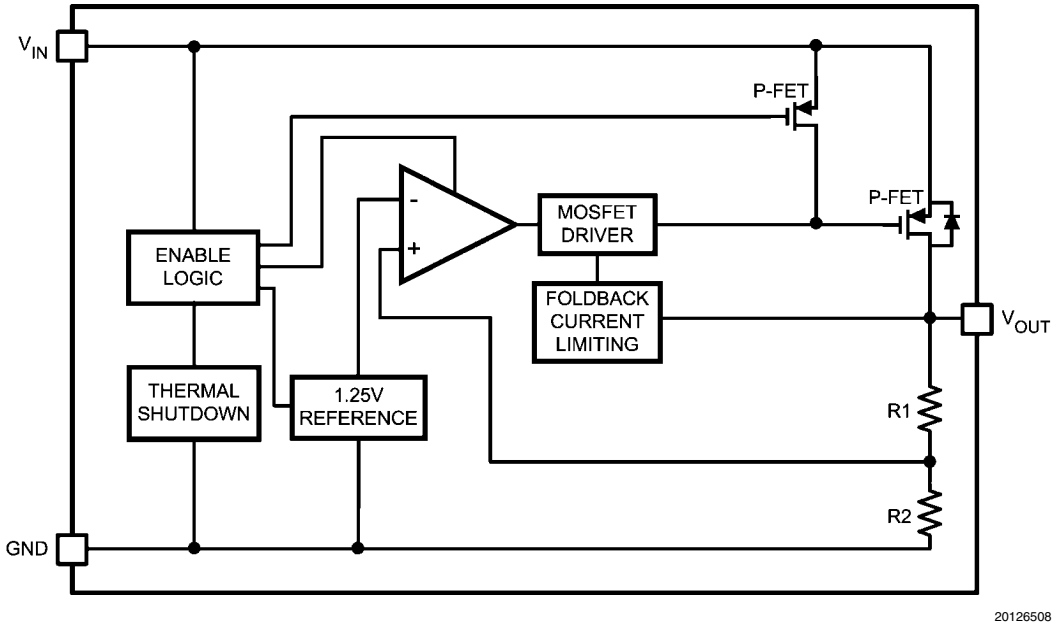


FIGURE 2. LP38691 Functional Diagram (TO-252)

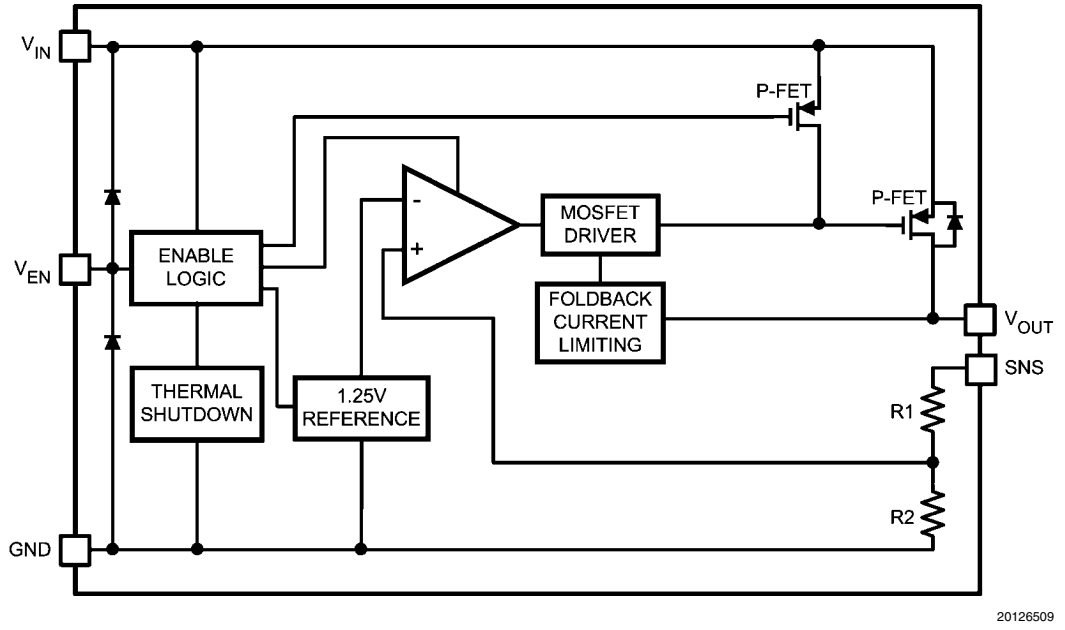


FIGURE 3. LP38693 Functional Diagram (LLP)

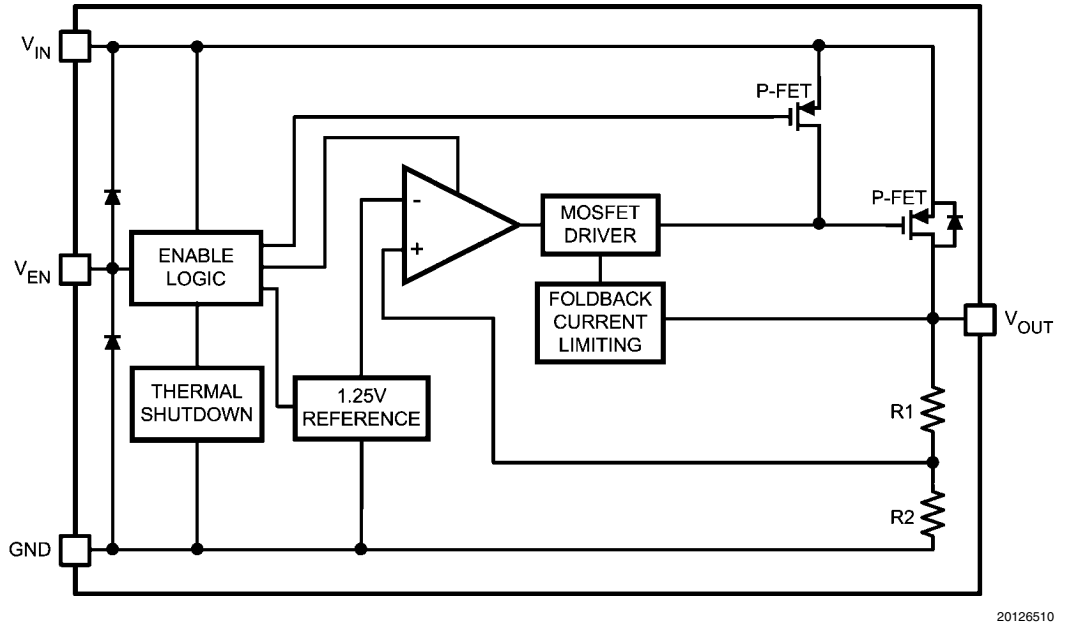
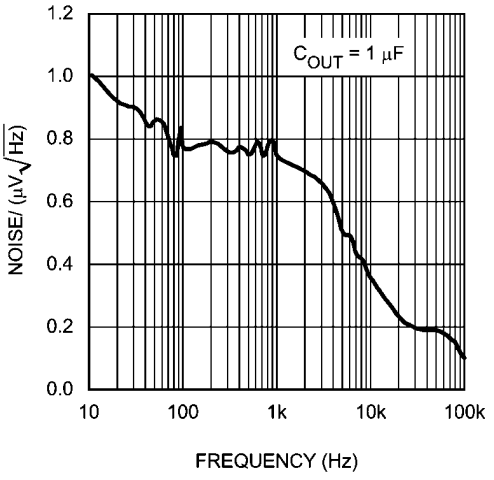


FIGURE 4. LP38693 Functional Diagram (SOT-223)

Typical Performance Characteristics

Unless otherwise specified: $T_J = 25°C$, $C_{IN} = C_{OUT} = 10\ \mu F$, Enable pin is tied to V_{IN} (LP38693 only), $V_{OUT} = 1.8V$, $V_{IN} = V_{OUT} + 1V$, $I_L = 10mA$.

Noise vs Frequency



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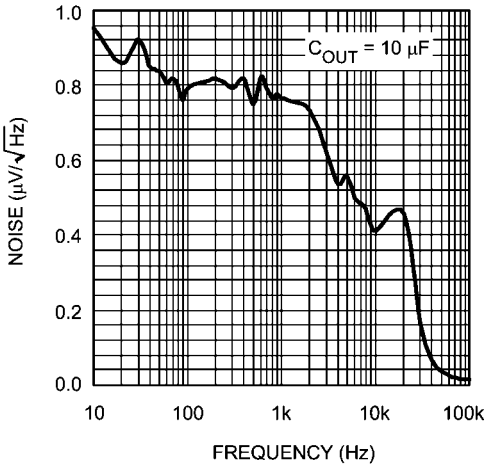
Noise vs Frequency



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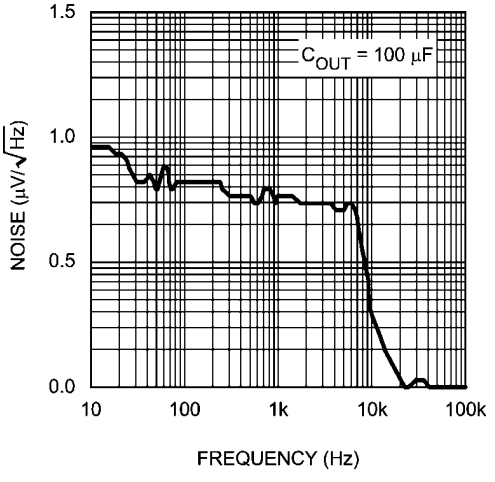
Noise vs Frequency



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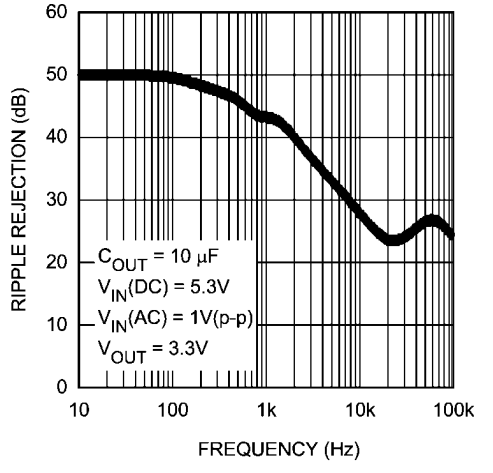
Ripple Rejection



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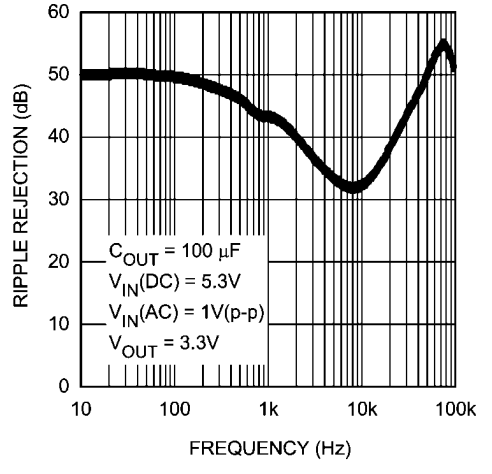
Ripple Rejection



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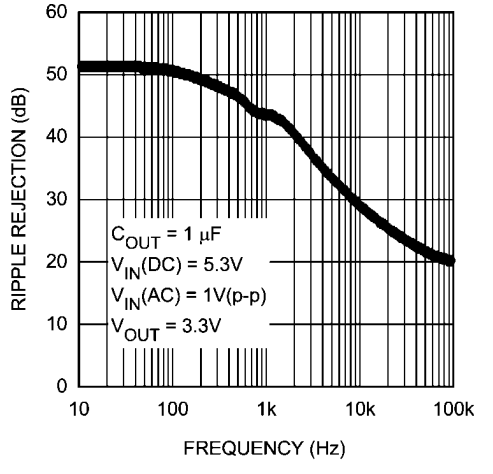
Ripple Rejection



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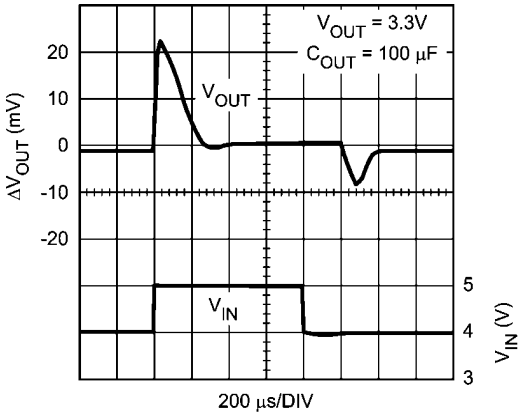
Line Transient Response



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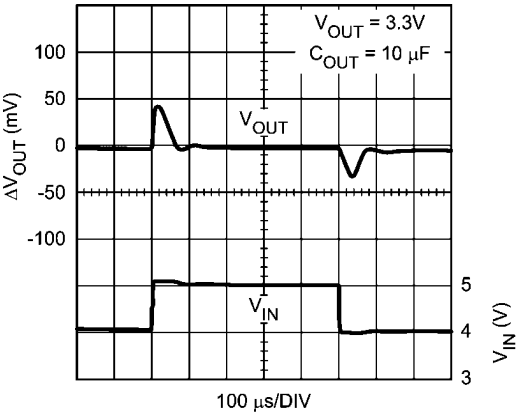
Line Transient Response



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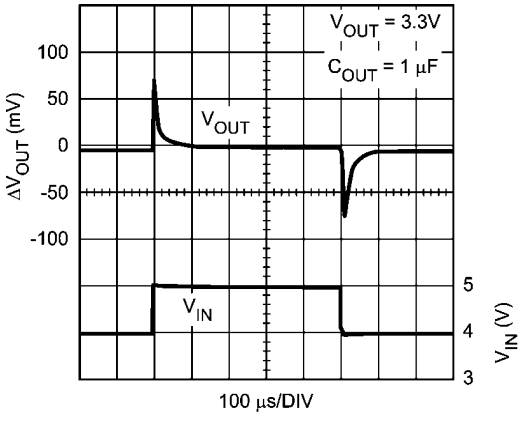
Line Transient Response



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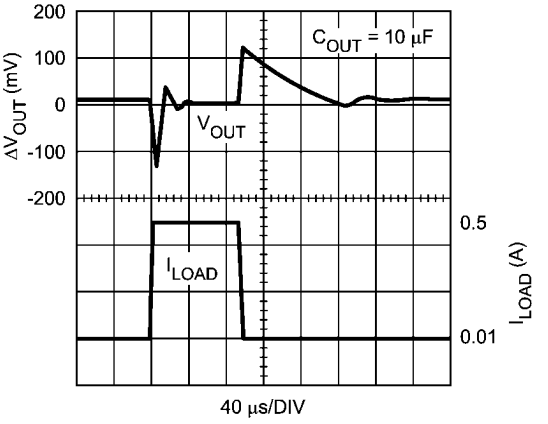
Load Transient Response



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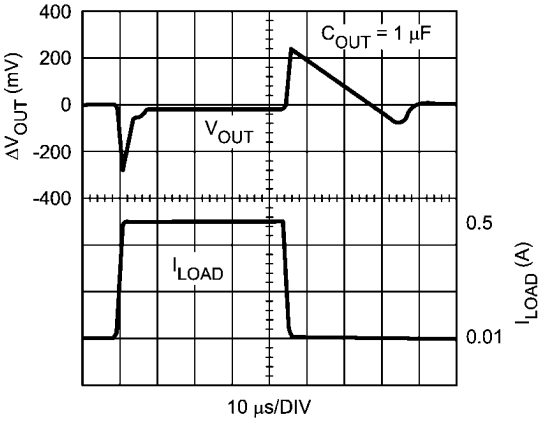
Load Transient Response



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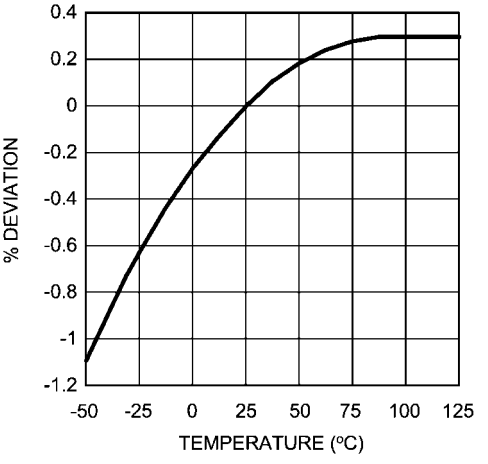
V_{OUT} vs Temperature (5.0V)



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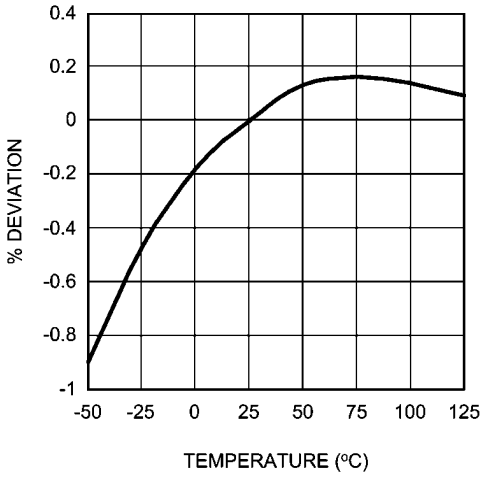
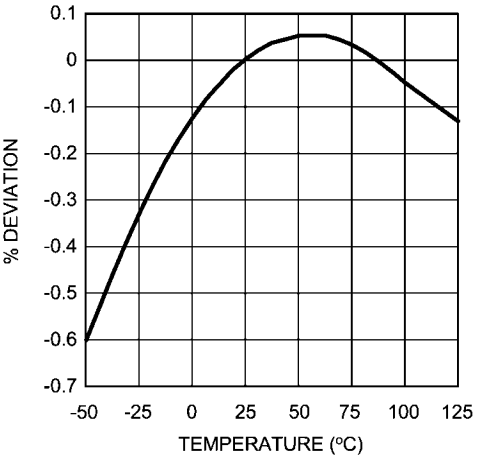
V_{OUT} vs Temperature (3.3V)



20126531

V_{OUT} vs Temperature (2.5V)



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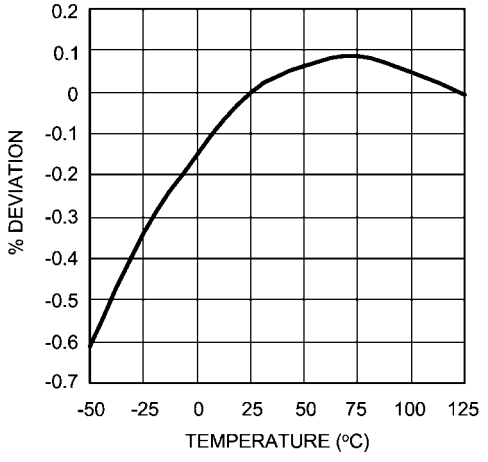
V_{OUT} vs Temperature (1.8V)



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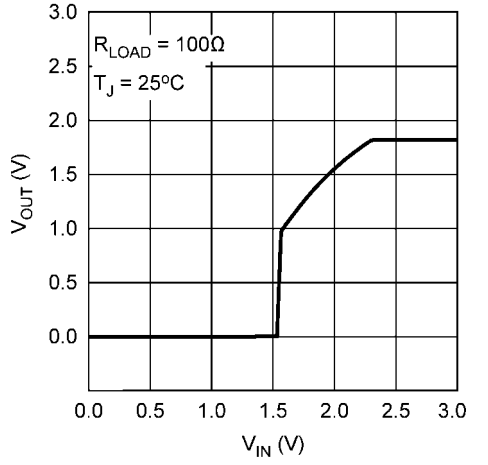
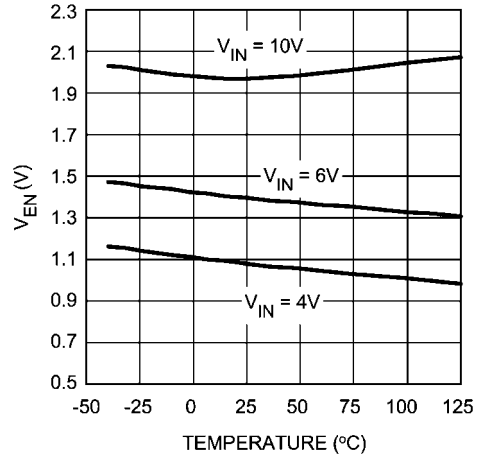
V_{OUT} vs V_{IN} (1.8V)



20126559

Enable Voltage vs Temperature



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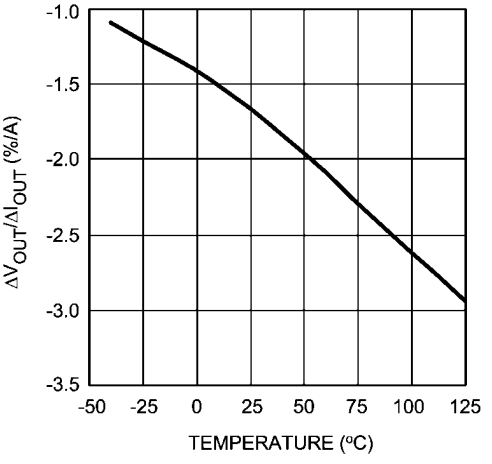
Load Regulation vs Temperature



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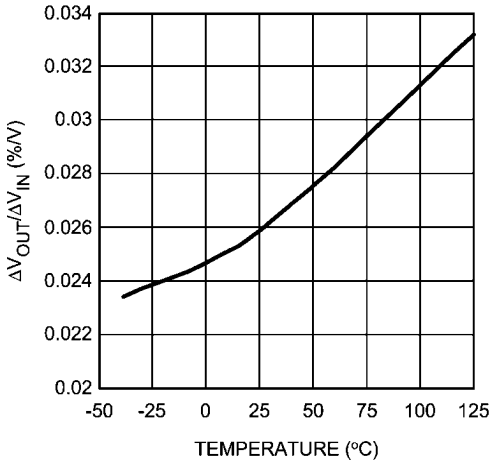
Line Regulation vs Temperature



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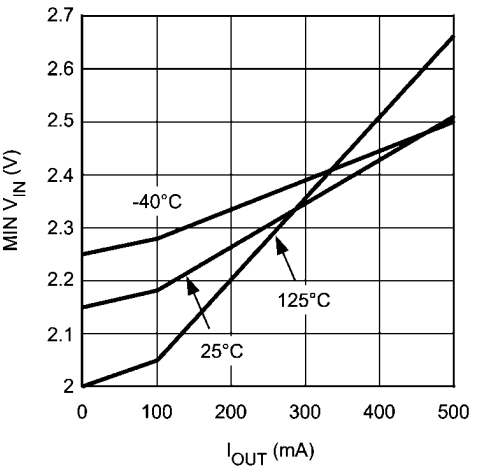
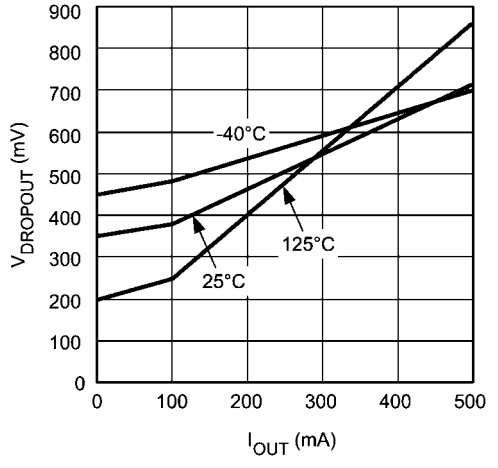
MIN V_{IN} vs I_{OUT}



20126557

Dropout Voltage vs I_{OUT}



20126556

Application Hints

EXTERNAL CAPACITORS

Like any low-dropout regulator, external capacitors are required to assure stability. These capacitors must be correctly selected for proper performance.

INPUT CAPACITOR: An input capacitor of at least 1µF is required (ceramic recommended). The capacitor must be located not more than one centimeter from the input pin and returned to a clean analog ground.

OUTPUT CAPACITOR: An output capacitor is required for loop stability. It must be located less than 1 centimeter from the device and connected directly to the output and ground pins using traces which have no other currents flowing through them.

The minimum amount of output capacitance that can be used for stable operation is 1µF. Ceramic capacitors are recommended (the LP38691/3 was designed for use with ultra low ESR capacitors). The LP38691/3 is stable with any output capacitor ESR between zero and 100 Ohms.

ENABLE PIN (LP38693 only): The LP38693 has an Enable pin (EN) which allows an external control signal to turn the regulator output On and Off. The Enable On/Off threshold has no hysteresis. The voltage signal must rise and fall cleanly, and promptly, through the ON and OFF voltage thresholds. The Enable pin has no internal pull-up or pull-down to establish a default condition and, as a result, this pin must be terminated either actively or passively. If the Enable pin is driven from a source that actively pulls high and low, the drive voltage should not be allowed to go below ground potential or higher than V_{IN}. If the application does not require the Enable function, the pin should be connected directly to the V_{IN} pin.

Foldback Current Limiting: Foldback current limiting is built into the LP38691/3 which reduces the amount of output current the part can deliver as the output voltage is reduced. The amount of load current is dependent on the differential voltage between V_{IN} and V_{OUT}. Typically, when this differential voltage exceeds 5V, the load current will limit at about 350 mA. When the V_{IN} - V_{OUT} differential is reduced below 4V, load current is limited to about 850 mA.

SELECTING A CAPACITOR

It is important to note that capacitance tolerance and variation with temperature must be taken into consideration when selecting a capacitor so that the minimum required amount of capacitance is provided over the full operating temperature range.

Capacitor Characteristics

CERAMIC

For values of capacitance in the 10 to 100 µF range, ceramics are usually larger and more costly than tantalums but give superior AC performance for bypassing high frequency noise because of very low ESR (typically less than 10 mΩ). However, some dielectric types do not have good capacitance characteristics as a function of voltage and temperature.

Z5U and Y5V dielectric ceramics have capacitance that drops severely with applied voltage. A typical Z5U or Y5V capacitor can lose 60% of its rated capacitance with half of the rated voltage applied to it. The Z5U and Y5V also exhibit a severe temperature effect, losing more than 50% of nominal capacitance at high and low limits of the temperature range.

X7R and X5R dielectric ceramic capacitors are strongly recommended if ceramics are used, as they typically maintain a capacitance range within ±20% of nominal over full operating ratings of temperature and voltage. Of course, they are typically larger and more costly than Z5U/Y5U types for a given voltage and capacitance.

TANTALUM

Solid Tantalum capacitors have good temperature stability: a high quality Tantalum will typically show a capacitance value that varies less than 10-15% across the full temperature range of -40°C to +125°C. ESR will vary only about 2X going from the high to low temperature limits.

PCB LAYOUT

Good PC layout practices must be used or instability can be induced because of ground loops and voltage drops. The input and output capacitors must be directly connected to the input, output, and ground pins of the regulator using traces which do not have other currents flowing in them (Kelvin connect).

The best way to do this is to lay out C_{IN} and C_{OUT} near the device with short traces to the V_{IN}, V_{OUT}, and ground pins. The regulator ground pin should be connected to the external circuit ground so that the regulator and its capacitors have a "single point ground".

It should be noted that stability problems have been seen in applications where "vias" to an internal ground plane were used at the ground points of the IC and the input and output capacitors. This was caused by varying ground potentials at these nodes resulting from current flowing through the ground plane. Using a single point ground technique for the regulator and it's capacitors fixed the problem. Since high current flows through the traces going into V_{IN} and coming from V_{OUT}, Kelvin connect the capacitor leads to these pins so there is no voltage drop in series with the input and output capacitors.

RFI/EMI SUSCEPTIBILITY

RFI (radio frequency interference) and EMI (electromagnetic interference) can degrade any integrated circuit's performance because of the small dimensions of the geometries inside the device. In applications where circuit sources are present which generate signals with significant high frequency energy content (> 1 MHz), care must be taken to ensure that this does not affect the IC regulator.

If RFI/EMI noise is present on the input side of the regulator (such as applications where the input source comes from the output of a switching regulator), good ceramic bypass capacitors must be used at the input pin of the IC.

If a load is connected to the IC output which switches at high speed (such as a clock), the high-frequency current pulses required by the load must be supplied by the capacitors on the IC output. Since the bandwidth of the regulator loop is less than 100 kHz, the control circuitry cannot respond to load changes above that frequency. This means the effective output impedance of the IC at frequencies above 100 kHz is determined only by the output capacitor(s).

In applications where the load is switching at high speed, the output of the IC may need RF isolation from the load. It is recommended that some inductance be placed between the output capacitor and the load, and good RF bypass capacitors be placed directly across the load.

PCB layout is also critical in high noise environments, since RFI/EMI is easily radiated directly into PC traces. Noisy circuitry should be isolated from "clean" circuits where possible, and grounded through a separate path. At MHz frequencies, ground planes begin to look inductive and RFI/ EMI can cause ground bounce across the ground plane. In multi-layer PCB applications, care should be taken in layout so that noisy

power and ground planes do not radiate directly into adjacent layers which carry analog power and ground.

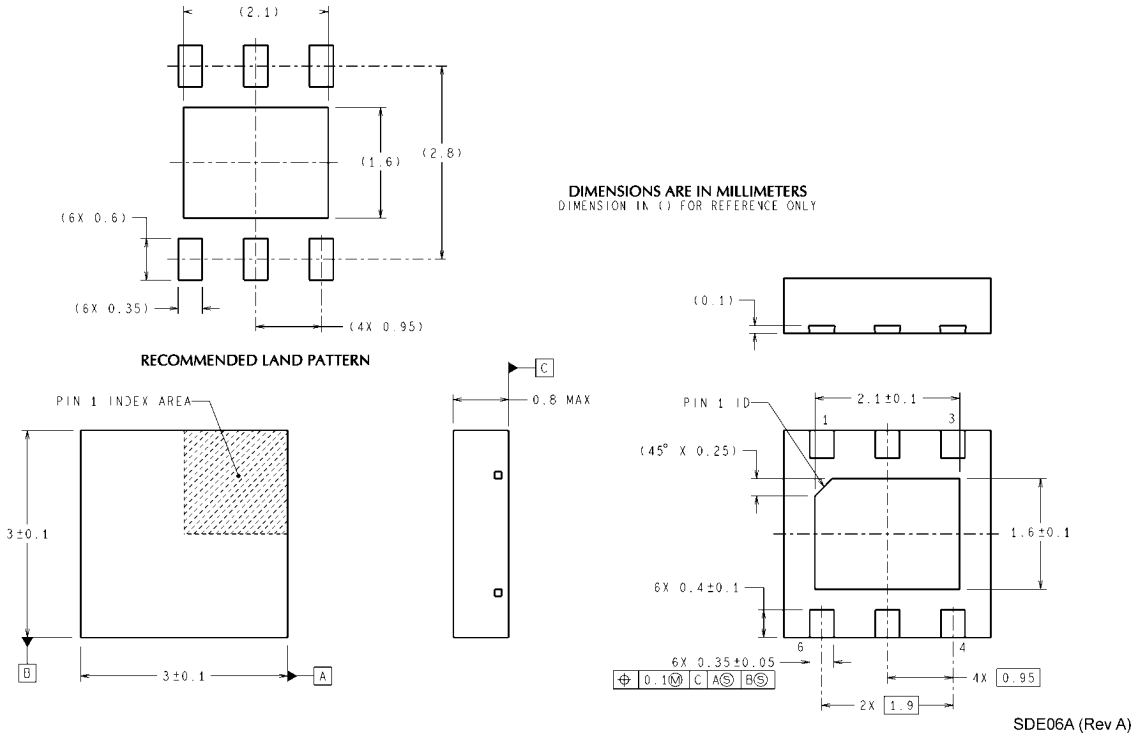
OUTPUT NOISE

Noise is specified in two ways: **Spot Noise** or **Output Noise Density** is the RMS sum of all noise sources, measured at the regulator output, at a specific frequency (measured with a 1Hz bandwidth). This type of noise is usually plotted on a curve as a function of frequency. **Total Output Noise** or **Broad-Band Noise** is the RMS sum of spot noise over a specified bandwidth, usually several decades of frequencies.

Attention should be paid to the units of measurement. Spot noise is measured in units µV/root-Hz or nV/root-Hz and total output noise is measured in µV(rms)

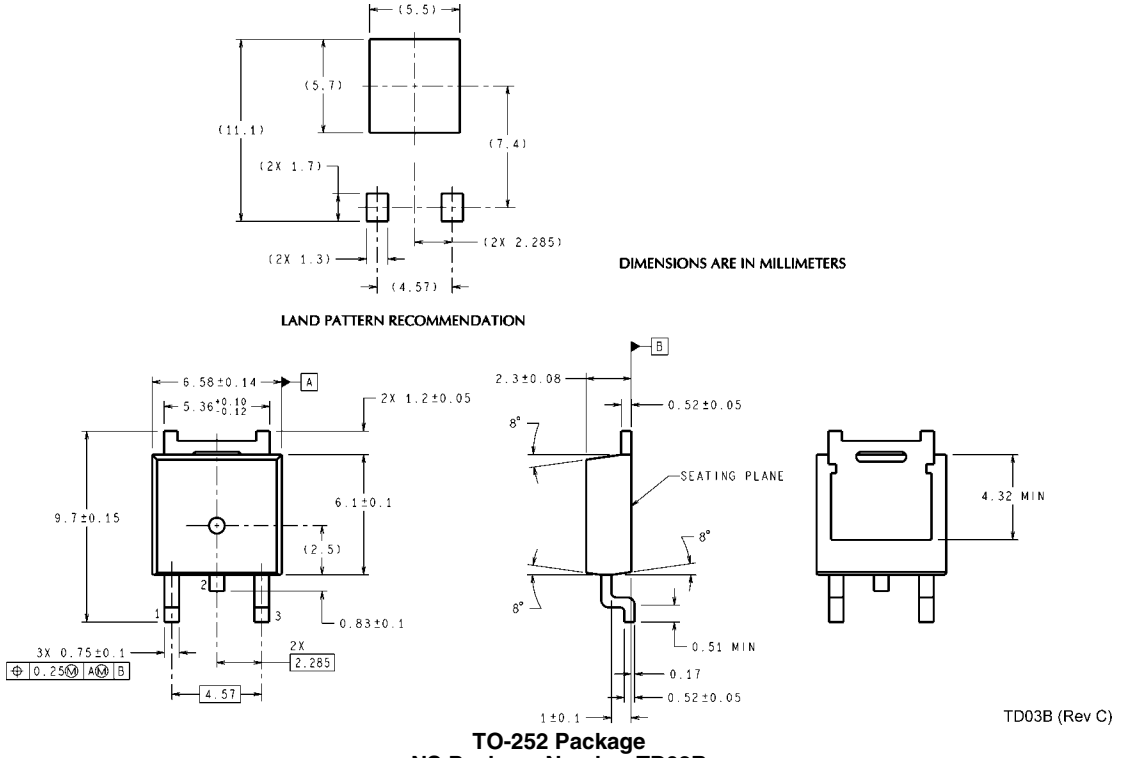
The primary source of noise in low-dropout regulators is the internal reference. Noise can be reduced in two ways: by increasing the transistor area or by increasing the current drawn by the internal reference. Increasing the area will decrease the chance of fitting the die into a smaller package. Increasing the current drawn by the internal reference increases the total supply current (ground pin current).

Physical Dimensions inches (millimeters) unless otherwise noted



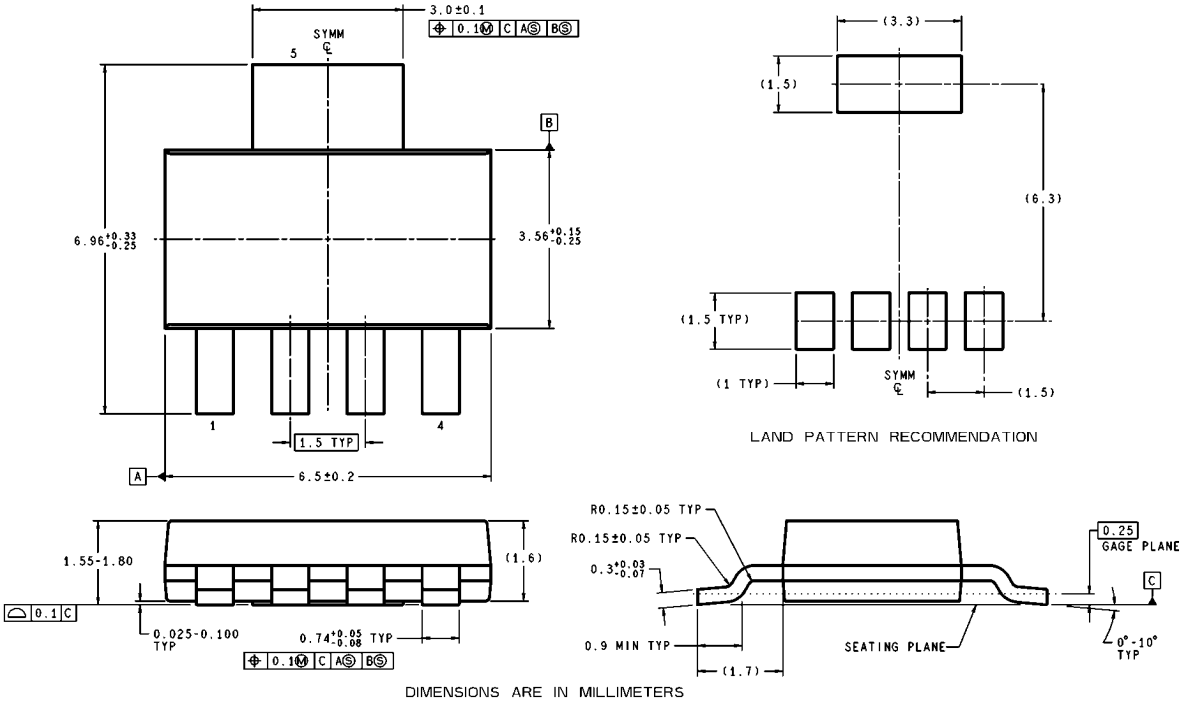
SDE06A (Rev A)

6-lead, LLP Package
NS Package Number SDE06A



TD03B (Rev C)

TO-252 Package
NS Package Number TD03B



MP05A (Rev A)

SOT-223 Package
NS Package Number MP05A

Notes

For more National Semiconductor product information and proven design tools, visit the following Web sites at:

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Interface	www.national.com/interface	Eval Boards	www.national.com/evalboards
LVDS	www.national.com/lvds	Packaging	www.national.com/packaging
Power Management	www.national.com/power	Green Compliance	www.national.com/quality/green
Switching Regulators	www.national.com/switchers	Distributors	www.national.com/contacts
LDOs	www.national.com/ldo	Quality and Reliability	www.national.com/quality
LED Lighting	www.national.com/led	Feedback/Support	www.national.com/feedback
Voltage Reference	www.national.com/vref	Design Made Easy	www.national.com/easy
PowerWise® Solutions	www.national.com/powerwise	Solutions	www.national.com/solutions
Serial Digital Interface (SDI)	www.national.com/sdi	Mil/Aero	www.national.com/milaero
Temperature Sensors	www.national.com/tempsensors	SolarMagic™	www.national.com/solarmagic
Wireless (PLL/VCO)	www.national.com/wireless	Analog University®	www.national.com/AU

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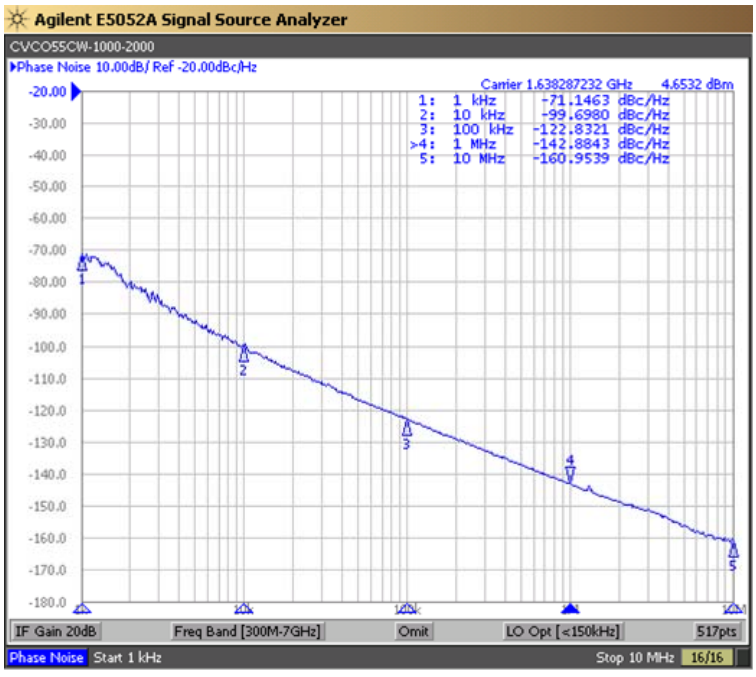
National Semiconductor Japan Technical Support Center
Email: jpn.feedback@nsc.com

Voltage Controlled Oscillator-VCO
CVCO55CW-1000-2000

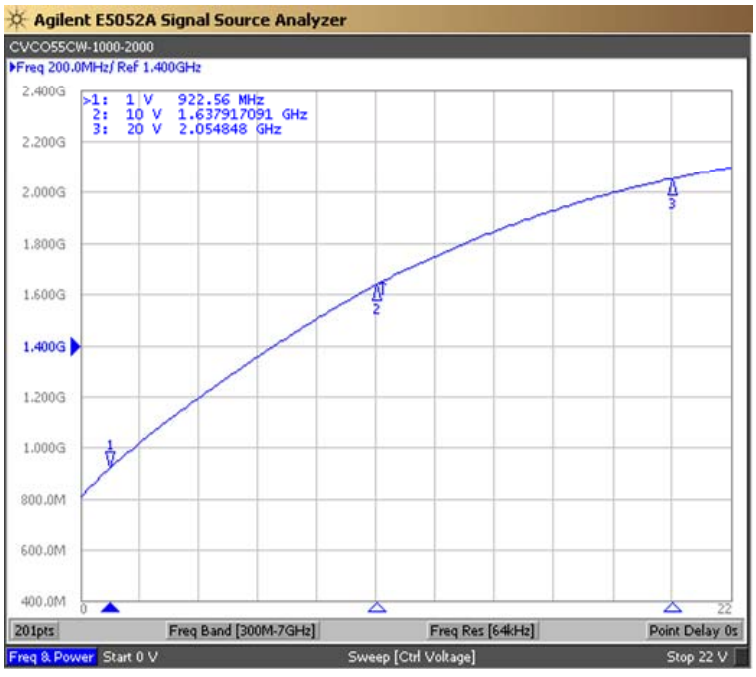
PERFORMANCE SPECIFICATION	MIN	TYP	MAX	UNITS
Lower Frequency:			1000	MHz
Upper Frequency:	2000			MHz
Tuning Voltage:	1.0		20.0	VDC
Supply Voltage:	9.75	10.0	10.25	VDC
Output Power:	+3.0	+5.5	+8.0	dBm
Supply Current:		15	25	mA
Harmonic Suppression (2nd Harmonic):		-10	-5	dBc
Pushing:		2.5	5.0	MHz/V
Pulling, all Phases:		7.5	15.0	MHz pk-pk
Tuning Sensitivity:		53		MHz/V
Phase Noise @ 10kHz offset:		-100	-95	dBc/Hz
Phase Noise @ 100kHz offset:		-124	-119	dBc/Hz
Load Impedance:		50		Ω
Input Capacitance:			33	pF
Operating Temperature Range:	-40		+80	°C
Storage Temperature Range:	-45		+90	°C

RoHS Compliant

Phase Noise (1 Hz BW, Typical)



Tuning Curve (Typical)



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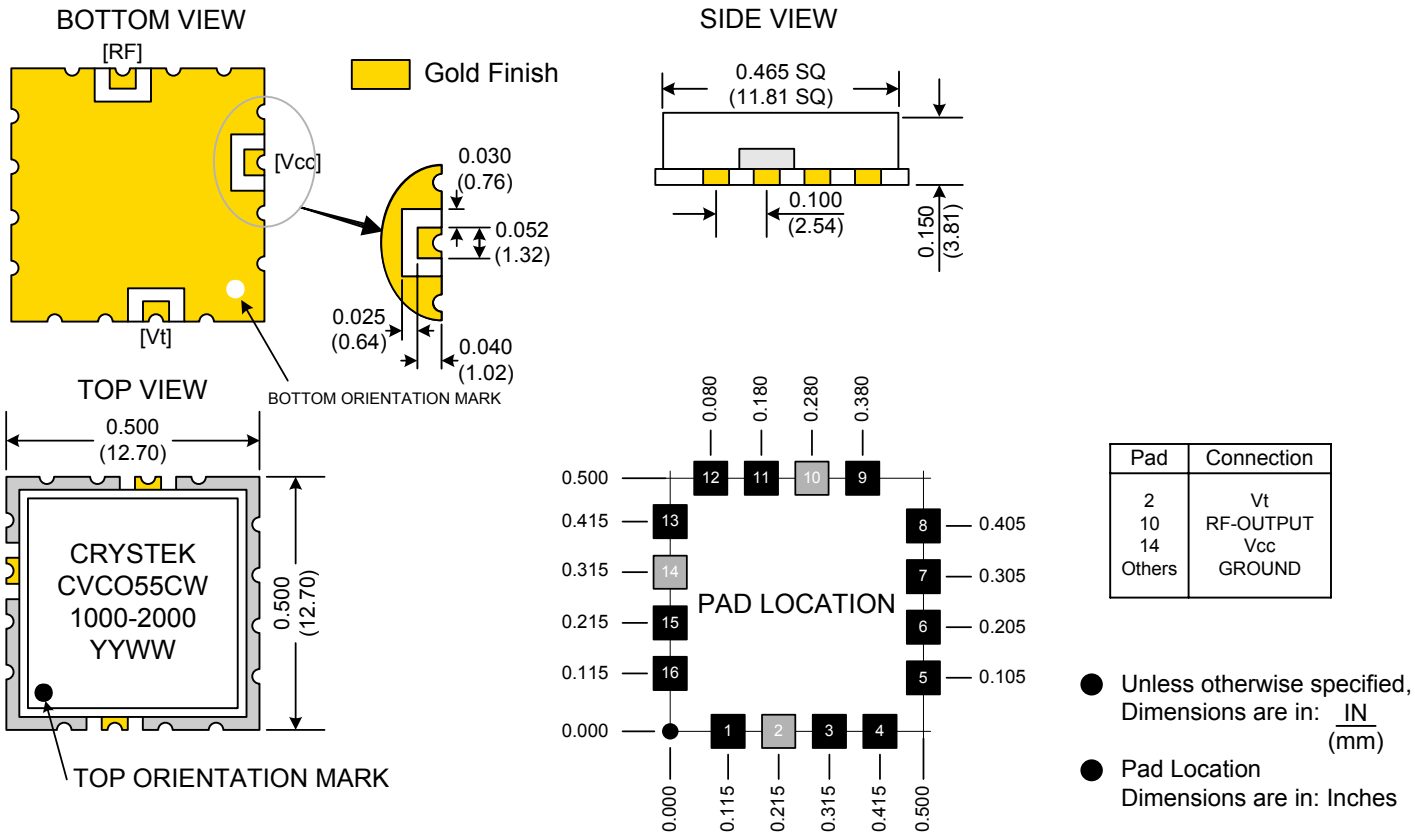
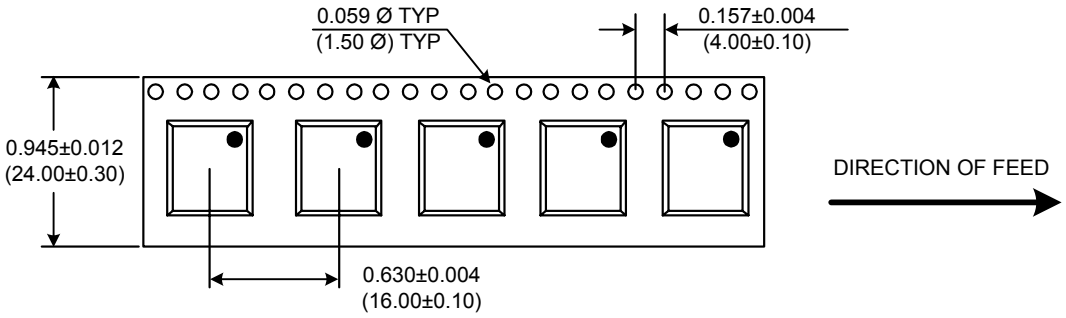
Voltage Controlled Oscillator-VCO
CVCO55CW-1000-2000



Pad	Connection
2	Vt
10	RF-OUTPUT
14	Vcc
Others	GROUND

- Unless otherwise specified, Dimensions are in: IN / (mm)
- Pad Location Dimensions are in: Inches

TAPE AND REEL



Drawing not to scale

Product Control:			
Crystek Part Number:	CVCO55CW-1000-2000	Release Date:	19-March-08
Revision Level:	D	Responsible:	C. Vales

Specification is subject to change without notice

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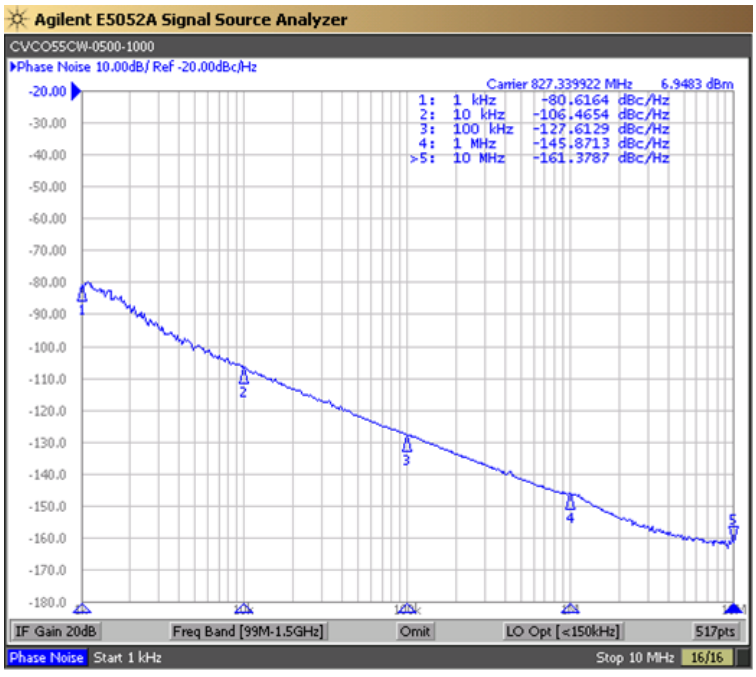
Voltage Controlled Oscillator-VCO
CVCO55CW-0500-1000

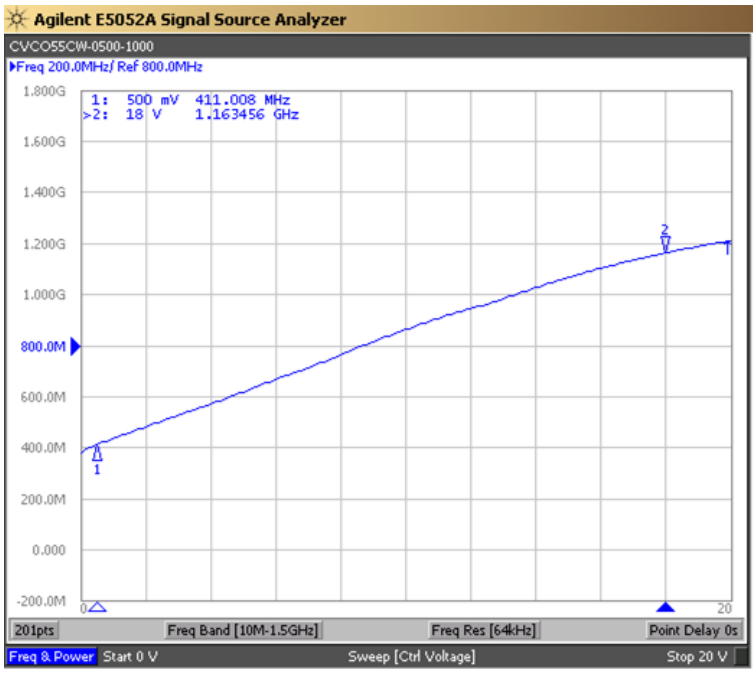
PERFORMANCE SPECIFICATION	MIN	TYP	MAX	UNITS
Lower Frequency:			500	MHz
Upper Frequency:	1000			MHz
Tuning Voltage:	0.5		18	VDC
Supply Voltage:	11.4	12.0	12.6	VDC
Output Power:	+4.0	+7.0	+10.0	dBm
Supply Current:		14	20	mA
Harmonic Suppression (2nd Harmonic):		-5		dBc
Pushing:			2.0	MHz/V
Pulling, all Phases:			4.0	MHz pk-pk
Tuning Sensitivity:		60		MHz/V
Phase Noise @ 10kHz offset:		-104		dBc/Hz
Phase Noise @ 100kHz offset:		-127		dBc/Hz
Load Impedance:		50		Ω
Input Capacitance:			120	pF
Operating Temperature Range:	-40		+85	°C
Storage Temperature Range:	-45		+90	°C

RoHS Compliant

Phase Noise (1 Hz BW, Typical)



Tuning Curve (Typical)



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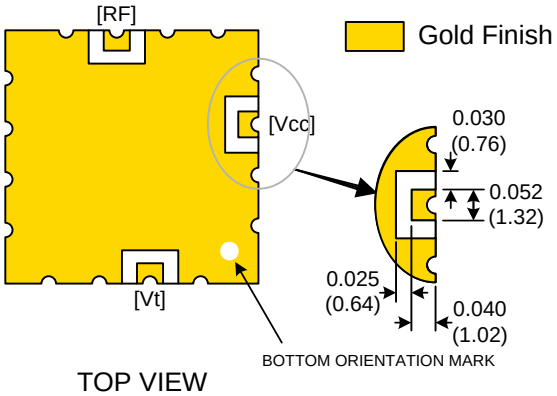
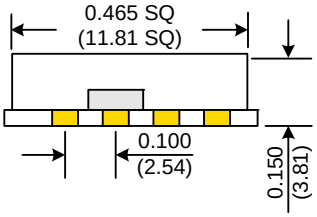
Voltage Controlled Oscillator-VCO
CVCO55CW-0500-1000

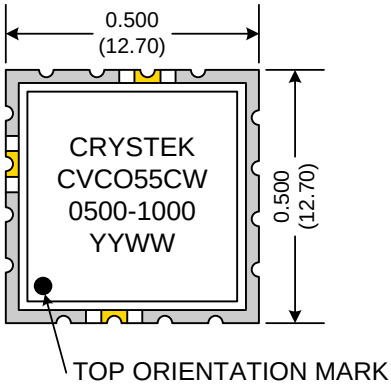
BOTTOM VIEW

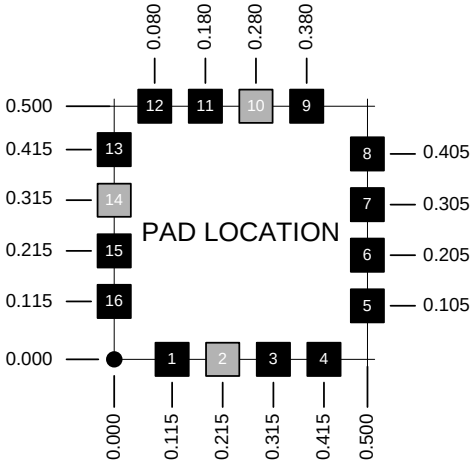


SIDE VIEW



TOP VIEW

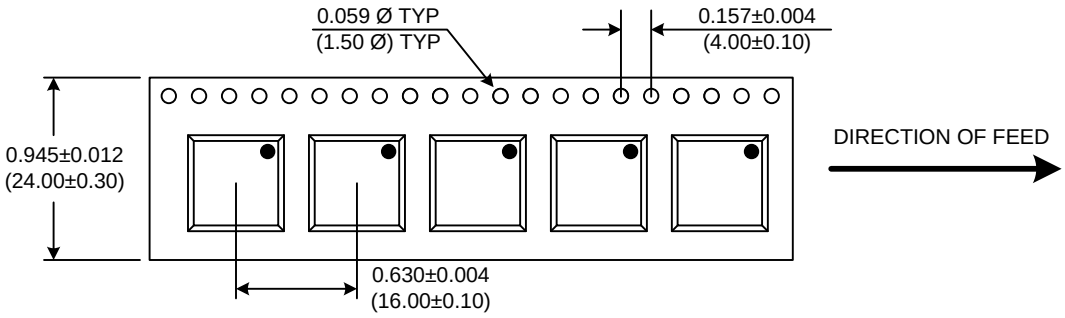




Pad	Connection
2	Vt
10	RF-OUTPUT
14	Vcc
Others	GROUND

- Unless otherwise specified, Dimensions are in: IN / (mm)
- Pad Location Dimensions are in: Inches

TAPE AND REEL



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Product Control:			
Crystek Part Number:	CVCO55CW-0500-1000	Release Date:	10-Feb-09
Revision Level:	E	Responsible:	C. Vales

Specification is subject to change without notice

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2-GHz, LOW DISTORTION, CURRENT FEEDBACK AMPLIFIERS

FEATURES

- **Unity Gain Bandwidth: 2 GHz**
- **High Slew Rate: 9000 V/μs**
- **IMD3 at 120 MHz: –89 dBc (G = 5, R_L = 100 Ω, V_{CC} = 15 V)**
- **OIP3 at 120 MHz: 44 dBm (G = 5, R_L = 100 Ω, V_{CC} = 15 V)**
- **High Output Current: ±115 mA into 20 Ω R_L**
- **Power Supply Voltage Range: 6.6 V to 15 V**

APPLICATIONS

- **High-Speed Signal Processing**
- **Test and Measurement Systems**
- **High-Voltage ADC Preamplifier**
- **RF and IF Amplifier Stages**
- **Professional Video**

DESCRIPTION

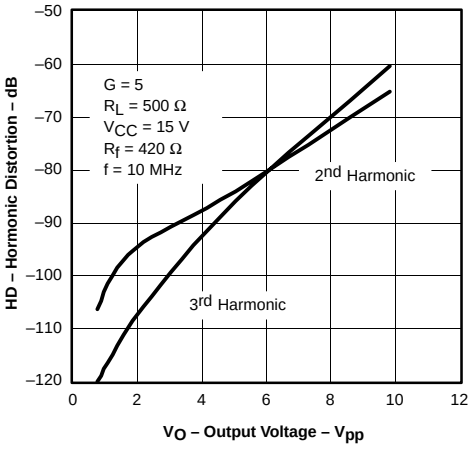
The THS3202 is part of the high performing current feedback amplifier family developed in BiCOM–II technology. Designed for low-distortion with a high slew rate of 9000 V/μs, the THS320x family is ideally suited for applications driving loads sensitive to distortion at high frequencies.

The THS3202 provides well-regulated ac performance characteristics with power supplies ranging from single-supply 6.6-V operation up to a 15-V supply. The high unity gain bandwidth of up to 2 GHz is a major contributor to the excellent distortion performance. The THS3202 offers an output current drive of ±115 mA and a low differential gain and phase error that make it suitable for applications such as video line drivers.

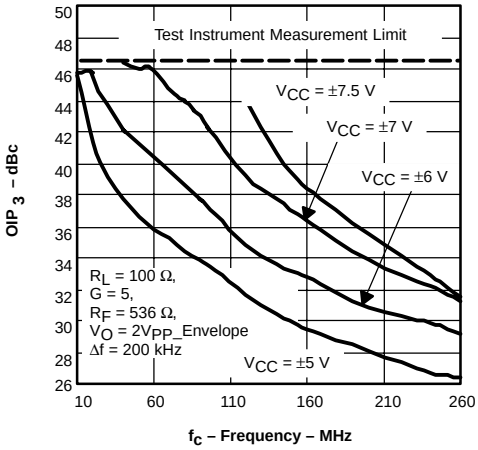
The THS3202 is available in an 8 pin SOIC and an 8 pin MSOP with PowerPAD™ packages.

RELATED DEVICES AND DESCRIPTIONS	
THS3001	±15-V 420-MHz Low Distortion CFB Amplifier
THS3061/2	±15-V 300-MHz Low Distortion CFB Amplifier
THS3122	±15-V Dual CFB Amplifier With 350 mA Drive
THS4271	+15-V 1.4-GHz Low Distortion VFB Amplifier

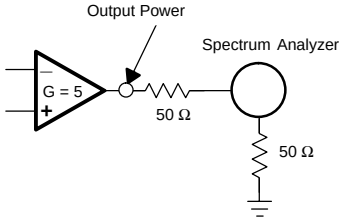
HARMONIC DISTORTION vs OUTPUT VOLTAGE



THS3202 OIP3 vs FREQUENCY



TEST CIRCUIT FOR IMD3 / OIP3



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PowerPAD is a trademark of Texas Instruments Incorporated.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted(1)

	UNIT
Supply voltage, V_{S-} to V_{S+}	16.5 V
Input voltage, V_I	$\pm V_S$
Differential input voltage, V_{ID}	±3 V
Output current, I_O(2)	175 mA
Continuous power dissipation	See Dissipation Rating Table
Maximum junction temperature, T_J	150°C
Operating free-air temperature range, T_A	–40°C to 85°C
Storage temperature range, T_{stg}	–65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	300°C
ESD ratings: HBM CDM MM	 3000 V 1500 V 200 V

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.

(2) The THS3202 may incorporate a PowerPAD on the underside of the chip. This acts as a heatsink and must be connected to a thermally dissipative plane for proper power dissipation. Failure to do so may result in exceeding the maximum junction temperature which could permanently damage the device. See TI technical brief SLMA002 for more information about utilizing the PowerPAD thermally enhanced package.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE DISSIPATION RATINGS

PACKAGE	θ_{JC} (°C/W)	θ_{JA} (°C/W)	POWER RATING (T_J = 125°C)	
			$T_A \le 25°C$	T_A = 85°C
D (SOIC–8)(1)	38.3	95	1.32 W	0.68 W
DGN (MSOP–8)(2)	4.7	58.4	2.14 W	1.11 W

(1) This data was taken using the JEDEC High-K test PCB. For the JEDEC Low-K test PCB, θ_{JA} is 324°C/W for the DBV5 and 167°C/W for the D.

(2) This data was taken using 2 oz. trace and copper pad that is soldered directly to a 3 in. x 3 in. PCB.

RECOMMENDED OPERATING CONDITIONS

		MIN	MAX	UNIT
Supply voltage	Dual supply	±3.3	±7.5	V
	Single supply	6.6	15	
Operating free-air temperature, T_A		–40	85	°C

PACKAGE/ORDERING INFORMATION

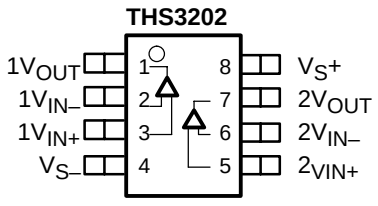
NUMBER OF CHANNELS	ORDERABLE PACKAGE AND NUMBER (OPERATING RANGE FROM –40°C TO 85°C)			
	PLASTIC SOIC-8(1) (D)	PACKAGE MARKING	PLASTIC MSOP-8(1) PowerPAD (DGN)	PACKAGE MARKING
2	THS3202D	–	THS3202DGN	BEP

(1) This package is available taped and reeled. To order this packaging option, add an R suffix to the part number (e.g., THS3202DR).

(2) This package is available taped and reeled. For standard quantities (3000 pieces per reel), add an R-suffix to the part number (e.g., THS3202DBVR). For smaller quantities (250 pieces per mini-reel), add a T-suffix to the part number (e.g., THS3202DBVT).

PIN ASSIGNMENTS

TOP VIEW **D, DGN**



ELECTRICAL CHARACTERISTICS

V_S = ±5 V: R_f = 500 Ω, R_L = 100 Ω, and G = +2 unless otherwise noted

PARAMETER	TEST CONDITIONS	THS3202					
		TYP	OVER TEMPERATURE				
		25°C	25°C	0°C to 70°C	–40°C to 85°C	UNITS	MIN/TYP/MAX
AC PERFORMANCE							
Small-signal bandwidth, –3 dB (V_O = 100 mV_{PP})	G = +1, R_f = 500 Ω	1800				MHz	Typ
	G = +2, R_f = 402 Ω	975					
	G = +5, R_f = 300 Ω	780					
	G = +10, R_f = 200 Ω	550					
Bandwidth for 0.1 dB flatness	G = +2, V_O = 100 mV_{pp}, R_f = 536 Ω	380				MHz	Typ
Large-signal bandwidth	G = +2, V_O = 4 V_{pp}, R_f = 536 Ω	875				MHz	Typ
Slew rate (25% to 75% level)	G = –1, 5-V step	5100				V/µs	Typ
	G = +2, 5-V step	4400					
Rise and fall time	G = +2, V_O = 5-V step	0.45				ns	Typ
Settling time to 0.1%	G = –2, V_O = 2-V step	19				ns	Typ
0.01%	G = –2, V_O = 2-V step	118					
Harmonic distortion	G = +2, f = 16 MHz, V_O = 2 V_{pp}						
2nd harmonic	R_L = 100 Ω	–64				dBc	Typ
	R_L = 500 Ω	–67					
3rd harmonic	R_L = 100 Ω	–67				dBc	Typ
	R_L = 500 Ω	–69					
3rd order intermodulation distortion	G = +5, f_c = 120 MHz, Δf = 200 kHz, $V_{O(envelope)}$ = 2 V_{pp}	–64				dBc	Typ
Input voltage noise	f > 10 MHz	1.65				nV/√Hz	Typ
Input current noise (noninverting)	f > 10 MHz	13.4				pA/√Hz	Typ
Input current noise (inverting)	f > 10 MHz	20				pA/√Hz	Typ
Crosstalk	G = +2, f = 100 MHz	–60				dB	Typ
Differential gain (NTSC, PAL)	G = +2, R_L = 150 Ω	0.008%					Typ
Differential phase (NTSC, PAL)	G = +2, R_L = 150 Ω	0.03°					Typ
DC PERFORMANCE							
Open-loop transimpedance gain	V_O = ±1 V, R_L = 1 kΩ	300	200	140	120	kΩ	Min
Input offset voltage	V_{CM} = 0 V	±0.7	±3	±3.8	±4	mV	Max
Average offset voltage drift	V_{CM} = 0 V			±10	±13	µV/°C	Typ
Input bias current (inverting)	V_{CM} = 0 V	±13	±60	±80	±85	µA	Max
Average bias current drift (–)	V_{CM} = 0 V			±300	±400	nA/°C	Typ
Input bias current (noninverting)	V_{CM} = 0 V	±14	±35	±45	±50	µA	Max
Average bias current drift (+)	V_{CM} = 0 V			±300	±400	nA/°C	Typ

ELECTRICAL CHARACTERISTICS

V_S = ±5 V: R_f = 500 Ω, R_L = 100 Ω, and G = +2 unless otherwise noted

PARAMETER	TEST CONDITIONS	THS3202					
		TYP	OVER TEMPERATURE				
		25°C	25°C	0°C to 70°C	–40°C to 85°C	UNITS	MIN/TYP/MAX
INPUT							
Common-mode input range		±2.6	±2.5	±2.5	±2.5	V	Min
Common-mode rejection ratio	V_{CM} = ±2.5 V	71	60	58	58	dB	Min
Input resistance	Noninverting	780				kΩ	Typ
	Inverting	11				Ω	Typ
Input capacitance	Noninverting	1				pF	Typ
OUTPUT							
Voltage output swing	R_L = 1 kΩ	±3.65	±3.5	±3.45	±3.4	V	Min
	R_L = 100 Ω	±3.45	±3.3	±3.25	±3.2		
Current output, sourcing	R_L = 20 Ω	115	105	100	100	mA	Min
Current output, sinking	R_L = 20 Ω	100	85	80	80	mA	Min
Closed-loop output impedance	G = +1, f = 1 MHz	0.01				Ω	Typ
POWER SUPPLY							
Minimum operating voltage	Absolute minimum		±3	±3	±3	V	Min
Maximum quiescent current	Per amplifier	14	16.8	19	20	mA	Max
Power supply rejection (+PSRR)	V_{S+} = 4.5 V to 5.5 V	69	63	60	60	dB	Min
Power supply rejection (–PSRR)	$V_{S–}$ = –4.5 V to –5.5 V	65	58	55	55	dB	Min

ELECTRICAL CHARACTERISTICS

V_S = 15 V: R_f = 500 Ω, R_L = 100 Ω, and G = +2 unless otherwise noted

PARAMETER	TEST CONDITIONS	THS3202					
		TYP	OVER TEMPERATURE				
		25°C	25°C	0°C to 70°C	–40°C to 85°C	UNITS	MIN/TYP/MAX
AC PERFORMANCE							
Small-signal bandwidth, –3dB (V_O = 100 mV_{PP})	G = +1, R_f= 550 Ω	2000				MHz	Typ
	G = +2, R_f = 550 Ω	1100					
	G = +5, R_f = 300 Ω	850					
	G = +10, R_f = 200 Ω	750					
Bandwidth for 0.1 dB flatness	G = +2, V_O = 100 mV_{pp}, R_f= 536 Ω	500				MHz	Typ
Large-signal bandwidth	G = +2, V_O = 4 V_{pp}, R_f= 536 Ω	1000				MHz	Typ
Slew rate (25% to 75% level)	G = +5, 5-V step	7500				V/µs	Typ
	G = +2, 10-V step	9000					
Rise and fall time	G = +2, V_O = 10-V step	0.45				ns	Typ
Settling time to 0.1%	G = –2, V_O = 2-V step	23				ns	Typ
0.01%	G = –2, V_O = 2-V step	112				ns	Typ
Harmonic distortion	G = +2, f = 16 MHz, V_O = 2 V_{pp}						
2nd harmonic	R_L = 100 Ω	–69				dBc	Typ
	R_L = 500 Ω	–73					
3rd harmonic	R_L = 100 Ω	–80				dBc	Typ
	R_L = 500 kΩ	–90					
3rd order intermodulation distortion	G = +5, f_c = 120 MHz, Δf = 200 kHz, $V_{O(envelope)}$ = 2 V_{pp}	–89				dBc	Typ
Input voltage noise	f > 10 MHz	1.65				nV/√Hz	Typ
Input current noise (noninverting)	f > 10 MHz	13.4				pA/√Hz	Typ
Input current noise (inverting)	f > 10 MHz	20				pA/√Hz	Typ
Crosstalk	G = +2, f = 100 MHz	–60				dB	Typ
Differential gain (NTSC, PAL)	G = +2, R_L = 150 Ω	0.004%					Typ
Differential phase (NTSC, PAL)	G = +2, R_L = 150 Ω	0.006°					Typ
DC PERFORMANCE							
Open-loop transimpedance gain	V_O = 6.5 V to 8.5 V, R_L = 1 kΩ	300	200	140	120	kΩ	Min
Input offset voltage	V_{CM} = 7.5 V	±1.3	±4	±4.8	±5	mV	Max
Average offset voltage drift	V_{CM} = 7.5 V			±10	±13	µV/°C	Typ
Input bias current (inverting)	V_{CM} = 7.5 V	±16	±60	±80	±85	µA	Max
Average bias current drift (–)	V_{CM} = 7.5 V			±300	±400	nA/°C	Typ
Input bias current (noninverting)	V_{CM} = 7.5 V	±14	±35	±45	±50	µA	Max
Average bias current drift (+)	V_{CM} = 7.5 V			±300	±400	nA/°C	Typ

ELECTRICAL CHARACTERISTICS continued

V_S = 15 V: R_f = 500 Ω, R_L = 100 Ω, and G = +2 unless otherwise noted

PARAMETER	TEST CONDITIONS	THS3202					
		TYP	OVER TEMPERATURE				
		25°C	25°C	0°C to 70°C	–40°C to 85°C	UNITS	MIN/TYP/MAX
INPUT							
Common-mode input range		2.4 to 12.6	2.5 to 12.5	2.5 to 12.5	2.5 to 12.5	V	Min
Common-mode rejection ratio	V_{CM} = 5 V to 10 V	69	60	58	58	dB	Min
Input resistance	Noninverting	780				kΩ	Typ
	Inverting	11				Ω	Typ
Input capacitance	Noninverting	1				pF	Typ
OUTPUT							
Voltage output swing	R_L = 1 kΩ	1.5 to 13.5	1.6 to 13.4	1.7 to 13.3	1.7 to 13.3	V	Min
	R_L = 100 Ω	1.7 to 13.3	1.8 to 13.2	2.0 to 13.0	2.0 to 13.0		
Current output, sourcing	R_L = 20 Ω	120	105	100	100	mA	Min
Current output, sinking	R_L = 20 Ω	115	95	90	90	mA	Min
Closed-loop output impedance	G = +1, f = 1 MHz	0.01				Ω	Typ
POWER SUPPLY							
Maximum quiescent current/channel	Per amplifier	15	18	21	21	mA	Max
Power supply rejection (+PSRR)	V_{S+} = 14.50 V to 15.50 V	69	63	60	60	dB	Min
Power supply rejection (–PSRR)	$V_{S–}$ = –0.5 V to +0.5 V	65	58	55	55	dB	Min

TYPICAL CHARACTERISTICS

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SMALL SIGNAL FREQUENCY RESPONSE

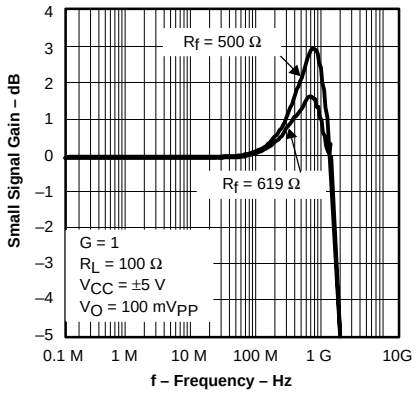


Figure 1

SMALL SIGNAL FREQUENCY RESPONSE

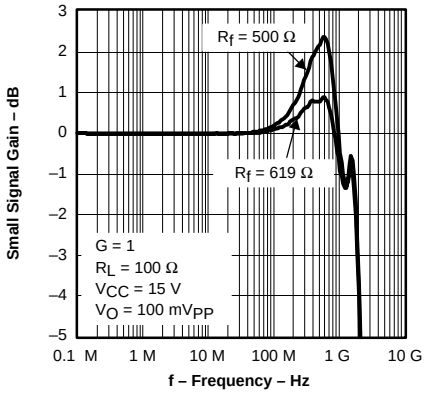


Figure 2

SMALL SIGNAL FREQUENCY RESPONSE

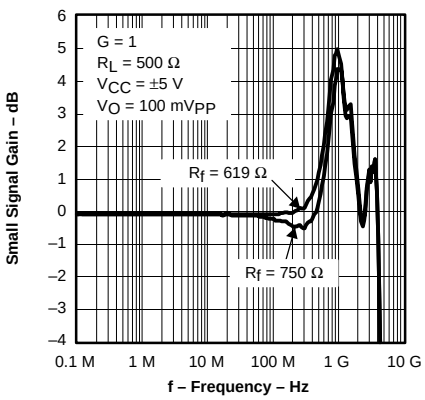


Figure 3

SMALL SIGNAL FREQUENCY RESPONSE

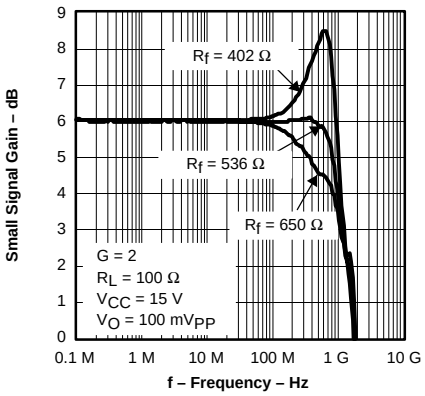


Figure 4

SMALL SIGNAL FREQUENCY RESPONSE

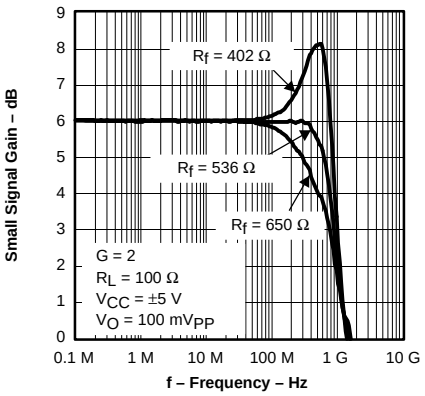


Figure 5

SMALL SIGNAL FREQUENCY RESPONSE

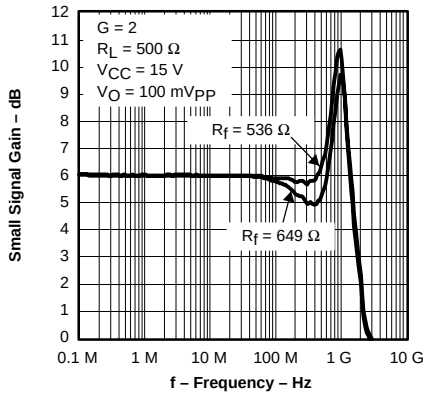


Figure 6

SMALL SIGNAL FREQUENCY RESPONSE

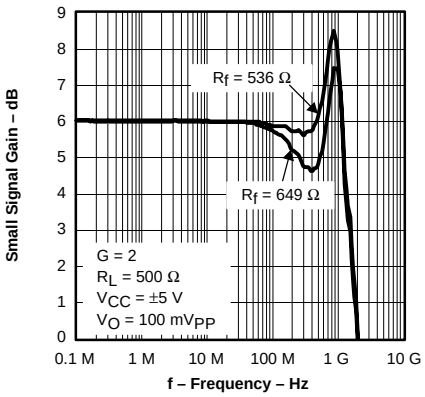


Figure 7

SMALL SIGNAL FREQUENCY RESPONSE

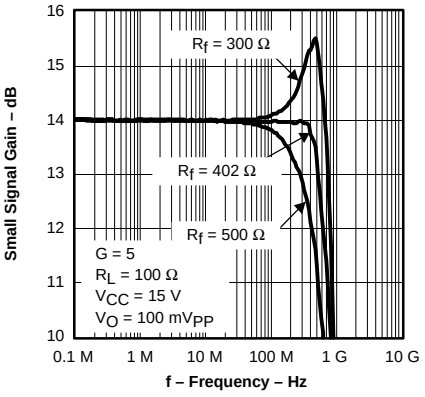


Figure 8

SMALL SIGNAL FREQUENCY RESPONSE

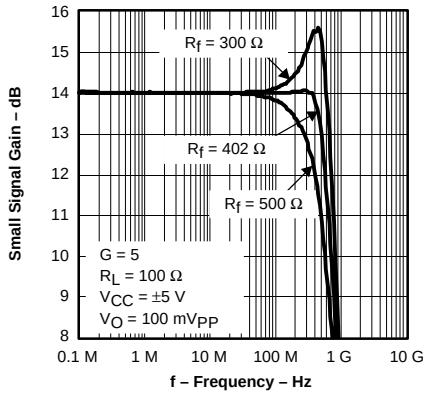


Figure 9

SMALL SIGNAL FREQUENCY RESPONSE

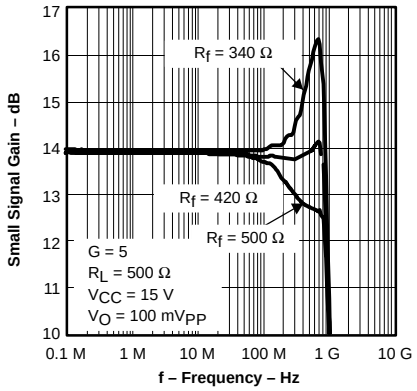


Figure 10

SMALL SIGNAL FREQUENCY RESPONSE

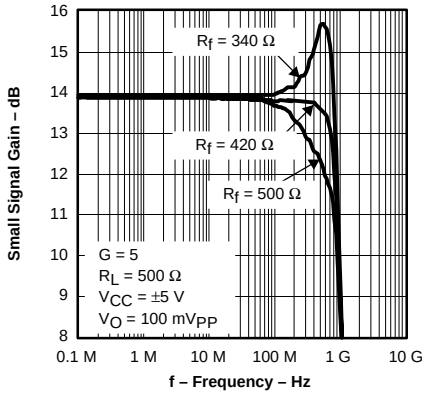


Figure 11

SMALL SIGNAL FREQUENCY RESPONSE

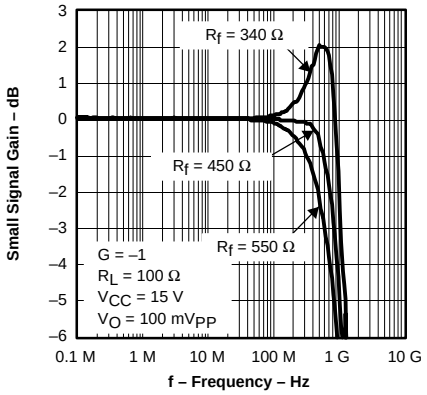


Figure 12

SMALL SIGNAL FREQUENCY RESPONSE

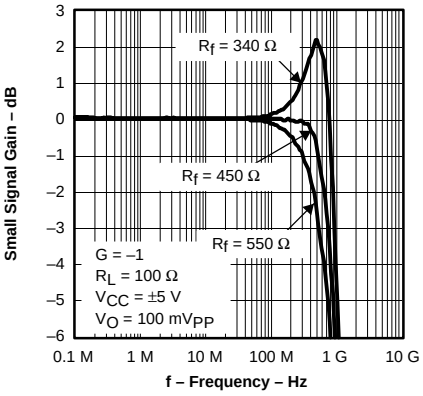


Figure 13

SMALL SIGNAL FREQUENCY RESPONSE

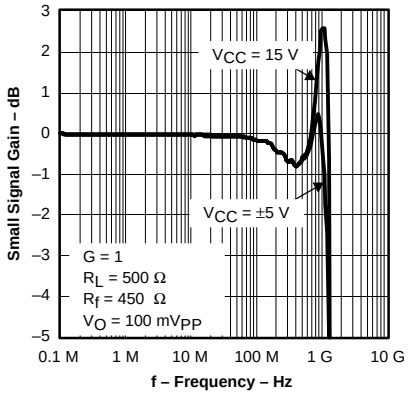


Figure 14

LARGE SIGNAL FREQUENCY RESPONSE

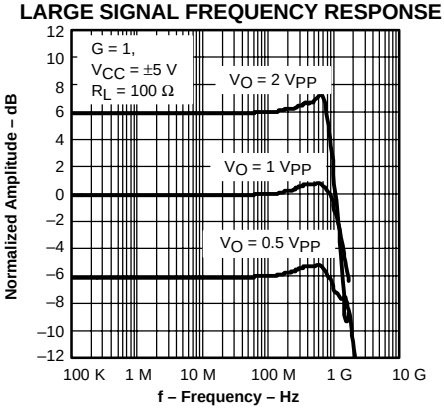


Figure 15

LARGE SIGNAL FREQUENCY RESPONSE

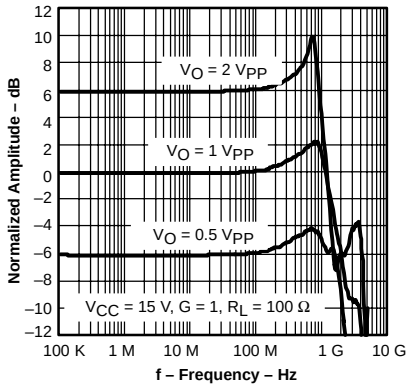


Figure 16

LARGE SIGNAL FREQUENCY RESPONSE

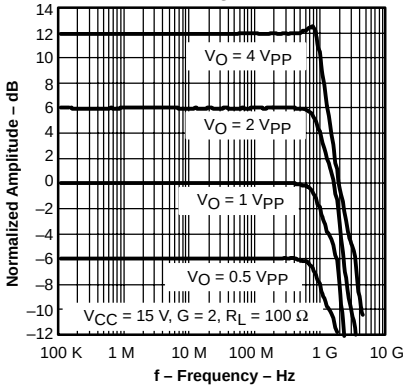


Figure 17

LARGE SIGNAL FREQUENCY RESPONSE

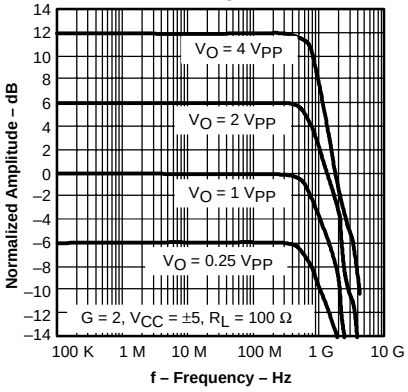


Figure 18

HARMONIC DISTORTION vs FREQUENCY

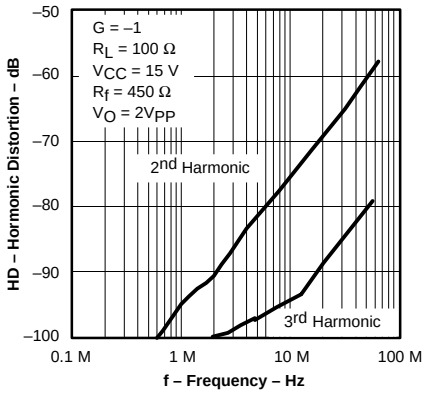


Figure 19

HARMONIC DISTORTION vs FREQUENCY

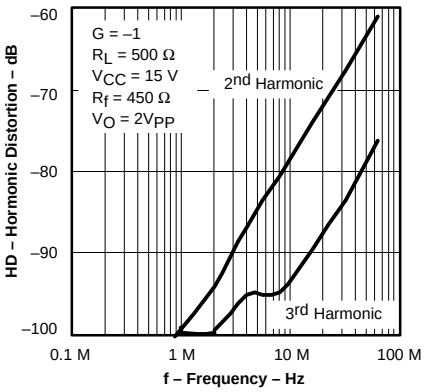


Figure 20

HARMONIC DISTORTION vs FREQUENCY

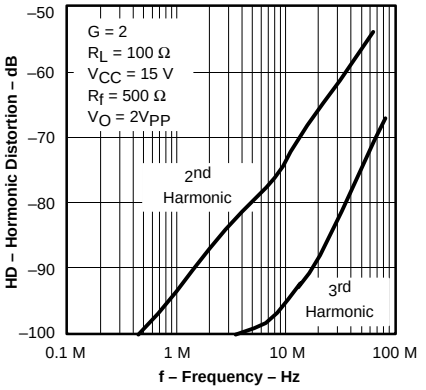


Figure 21

HARMONIC DISTORTION vs FREQUENCY

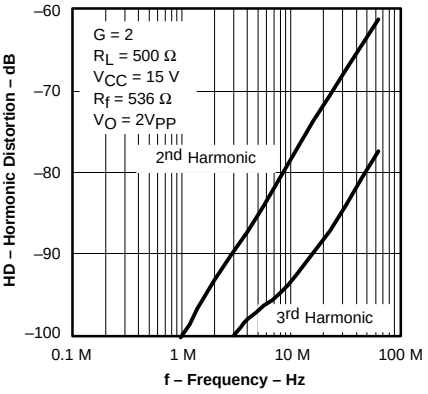


Figure 22

HARMONIC DISTORTION vs FREQUENCY

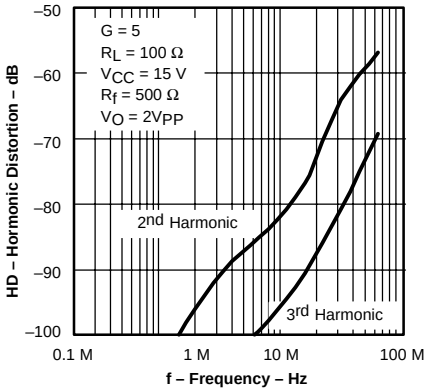


Figure 23

HARMONIC DISTORTION vs FREQUENCY

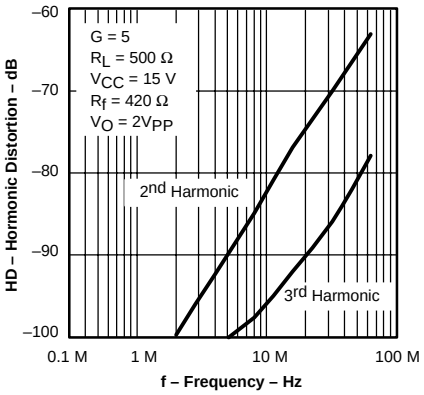


Figure 24

HARMONIC DISTORTION vs FREQUENCY

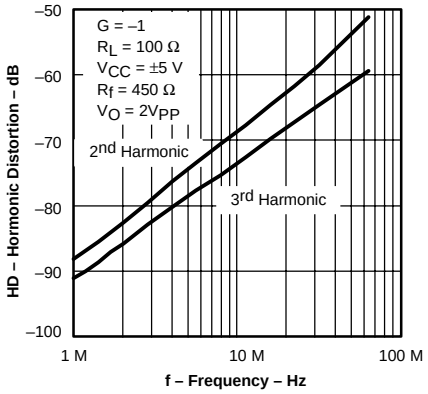


Figure 25

HARMONIC DISTORTION vs FREQUENCY

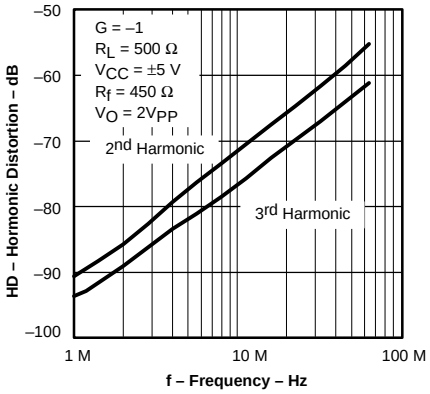


Figure 26

HARMONIC DISTORTION vs FREQUENCY

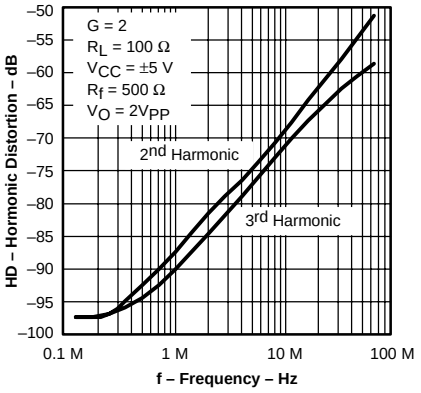


Figure 27

HARMONIC DISTORTION vs FREQUENCY

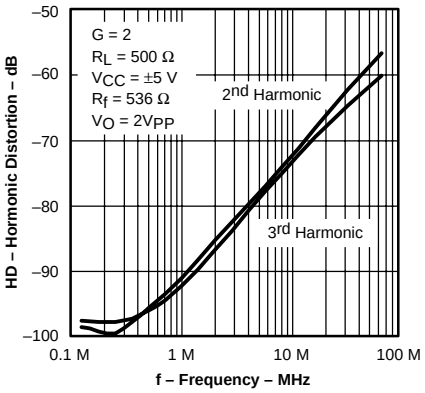


Figure 28

HARMONIC DISTORTION vs FREQUENCY

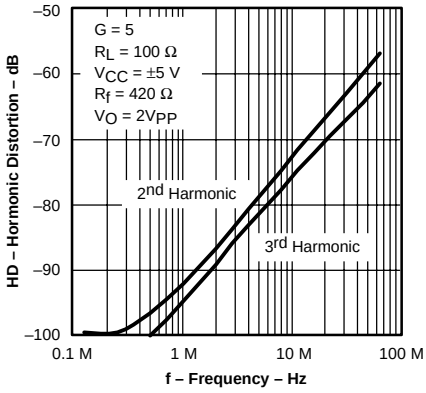


Figure 29

HARMONIC DISTORTION vs FREQUENCY

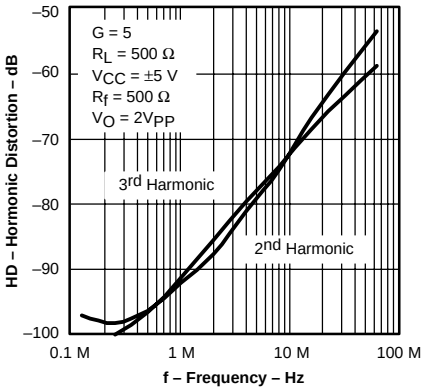


Figure 30

HARMONIC DISTORTION vs OUTPUT VOLTAGE

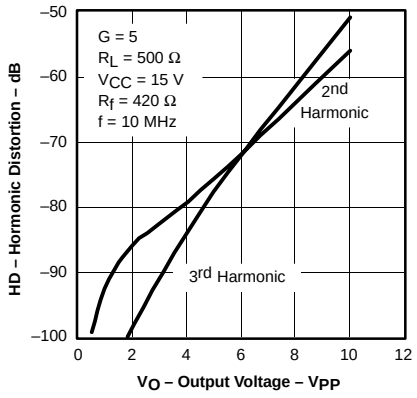


Figure 31

HARMONIC DISTORTION vs OUTPUT VOLTAGE

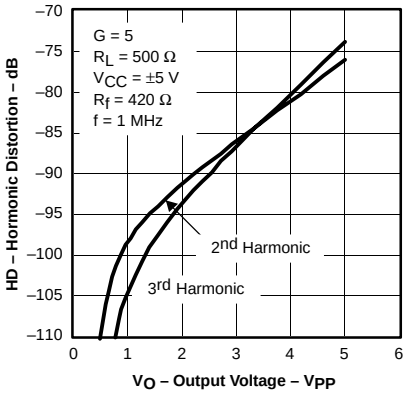


Figure 32

HARMONIC DISTORTION vs OUTPUT VOLTAGE

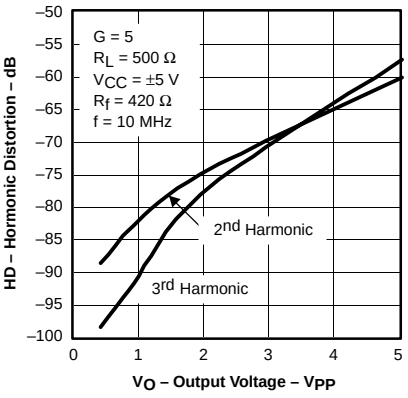


Figure 33

HARMONIC DISTORTION vs OUTPUT VOLTAGE

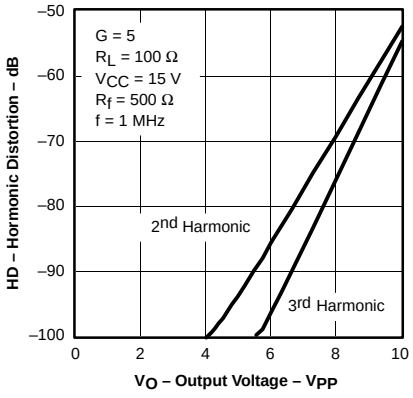


Figure 34

HARMONIC DISTORTION vs OUTPUT VOLTAGE

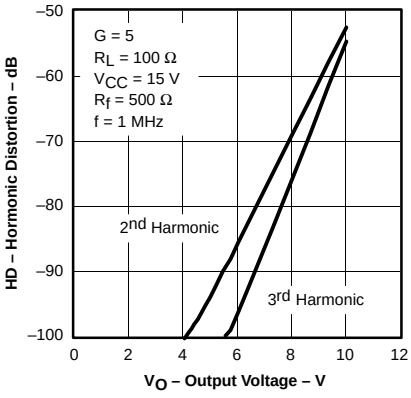


Figure 35

HARMONIC DISTORTION vs OUTPUT VOLTAGE

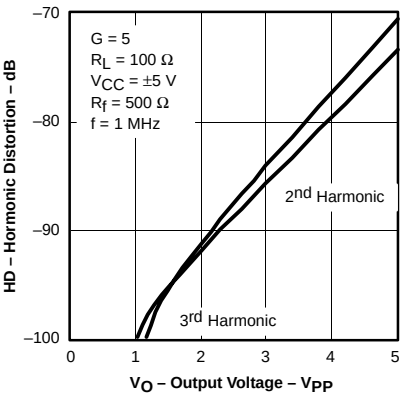


Figure 36

HARMONIC DISTORTION vs OUTPUT VOLTAGE

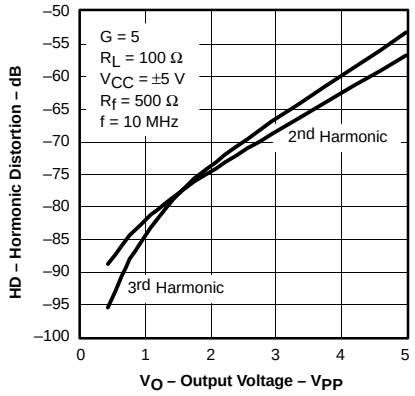


Figure 37

HARMONIC DISTORTION vs OUTPUT VOLTAGE

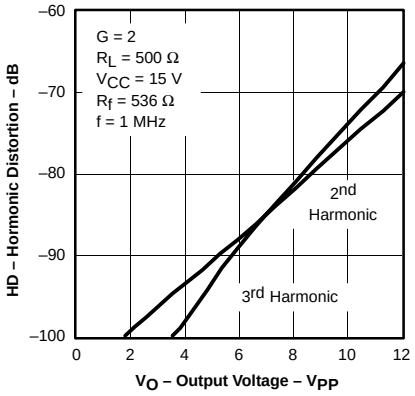


Figure 38

HARMONIC DISTORTION vs OUTPUT VOLTAGE

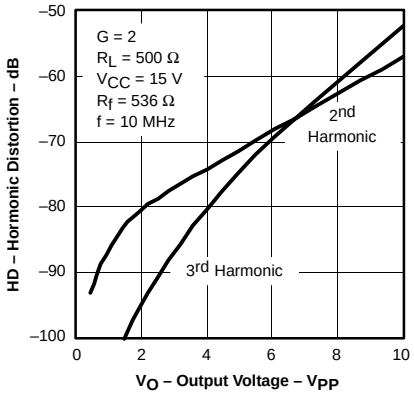


Figure 39

HARMONIC DISTORTION vs OUTPUT VOLTAGE

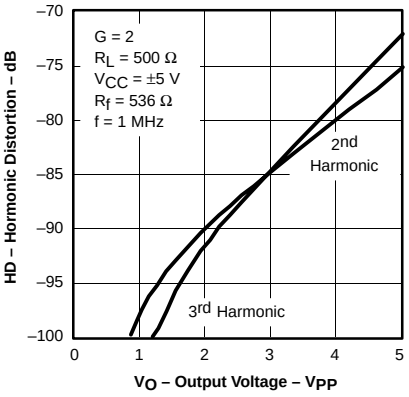


Figure 40

HARMONIC DISTORTION vs OUTPUT VOLTAGE

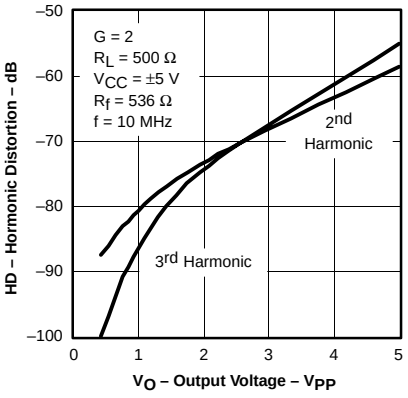


Figure 41

HARMONIC DISTORTION vs OUTPUT VOLTAGE

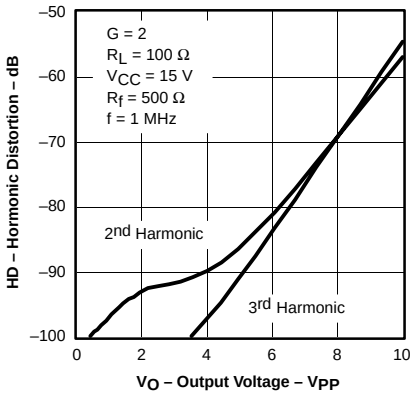


Figure 42

HARMONIC DISTORTION vs OUTPUT VOLTAGE

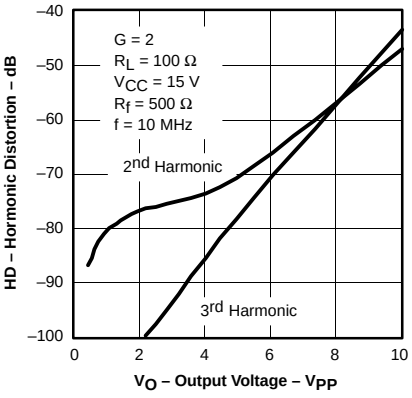


Figure 43

HARMONIC DISTORTION vs OUTPUT VOLTAGE

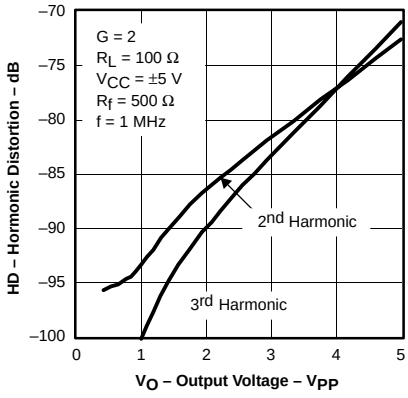


Figure 44

HARMONIC DISTORTION vs OUTPUT VOLTAGE

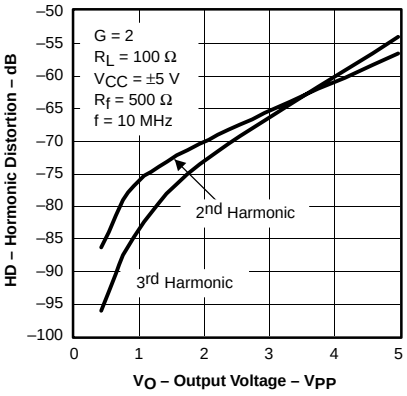


Figure 45

THS3202
IMD_3
vs
FREQUENCY

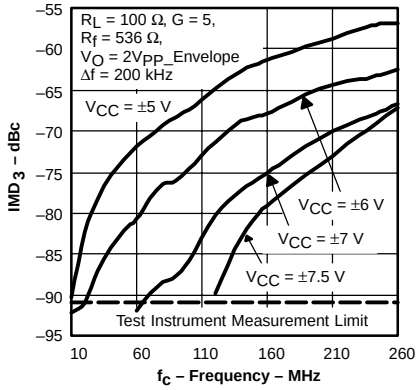


Figure 46

THS3202
IMD_3
vs
FREQUENCY

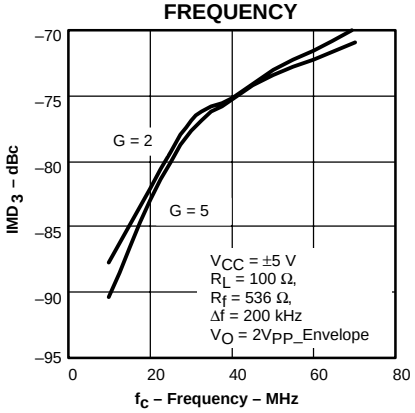


Figure 47

THS3202
OIP_3
vs
FREQUENCY

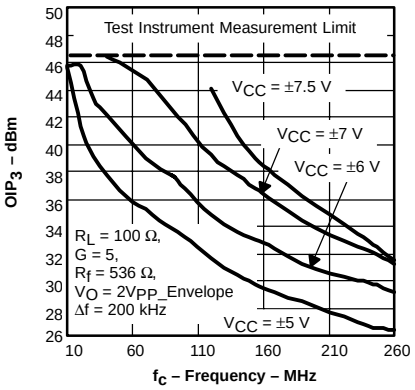


Figure 48

THS3202
OIP_3
vs
FREQUENCY

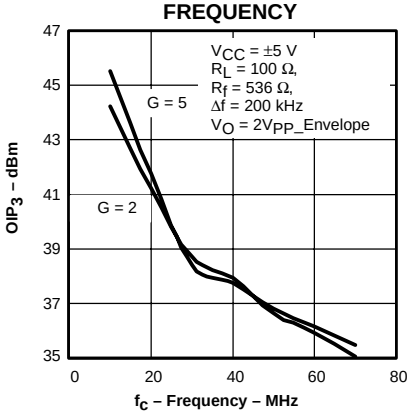
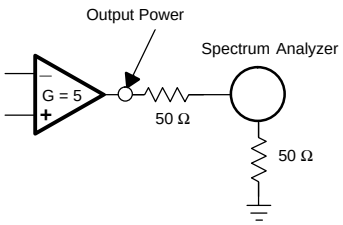


Figure 49

TEST CIRCUIT FOR
IMD_3 / OIP_3



This circuit applies to figures 46 through 49

Figure 50

S PARAMETER
vs
FREQUENCY

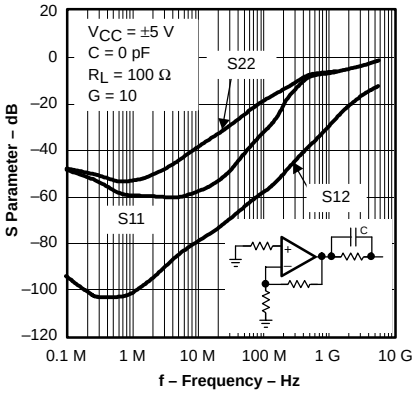


Figure 51

S PARAMETER
vs
FREQUENCY

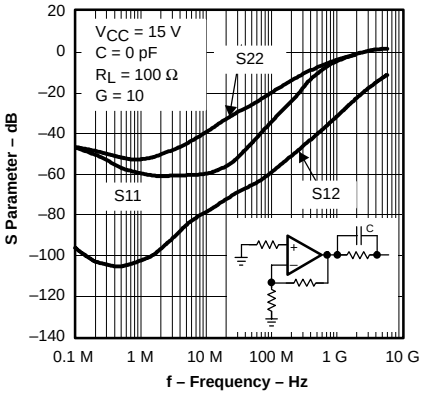


Figure 52

S PARAMETER
vs
FREQUENCY

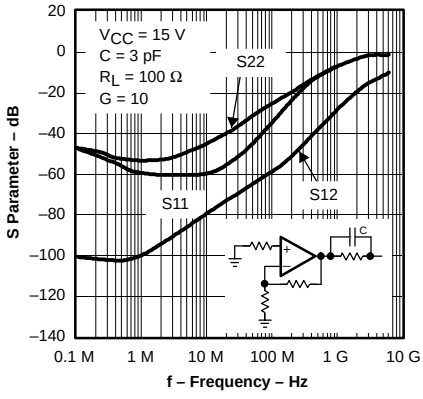


Figure 53

S PARAMETER
vs
FREQUENCY

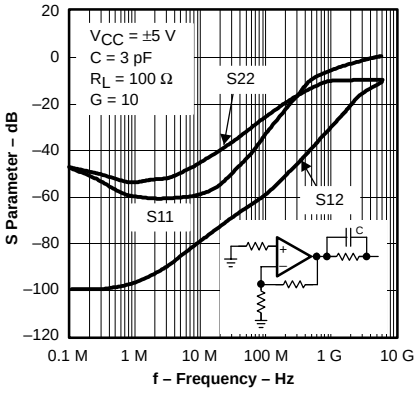


Figure 54

INPUT CURRENT NOISE DENSITY vs FREQUENCY

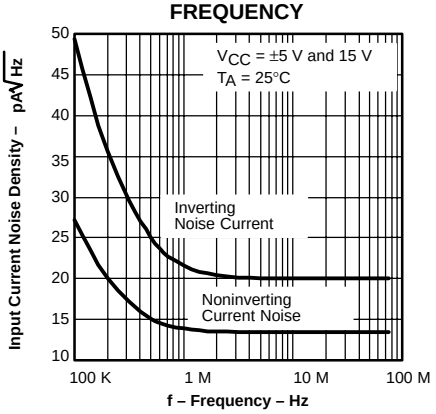


Figure 55

VOLTAGE NOISE DENSITY vs FREQUENCY

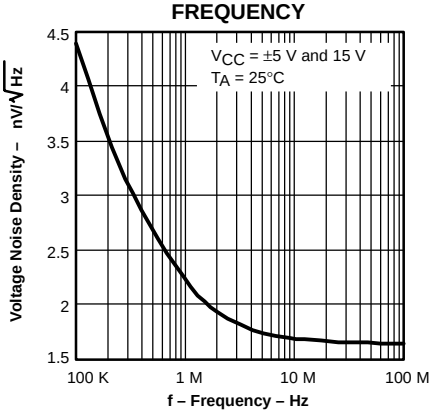


Figure 56

TRANSIMPEDANCE vs FREQUENCY

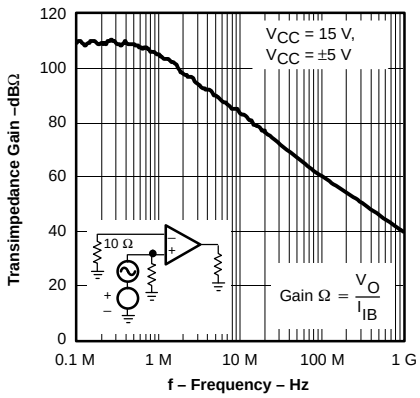


Figure 57

OUTPUT IMPEDANCE vs FREQUENCY

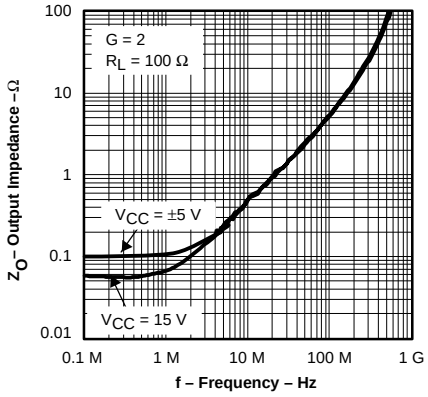


Figure 58

THS3202 IMPEDANCE OF INVERTING INPUT

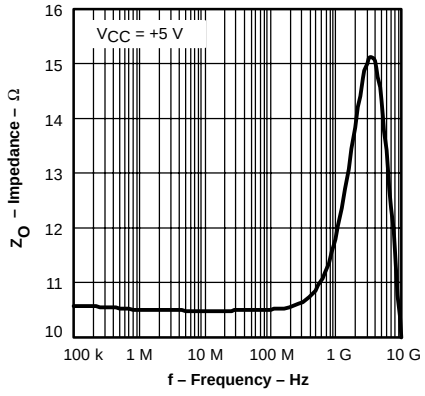


Figure 59

SUPPLY CURRENT/CHANNEL vs SUPPLY VOLTAGE

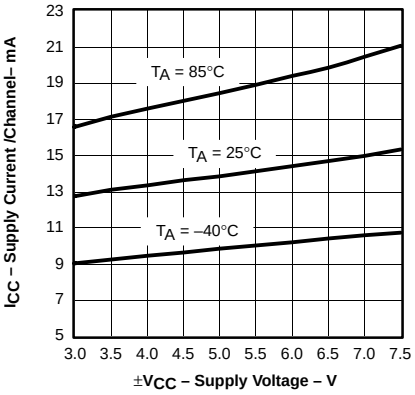


Figure 60

INPUT OFFSET VOLTAGE vs FREE-AIR TEMPERATURE

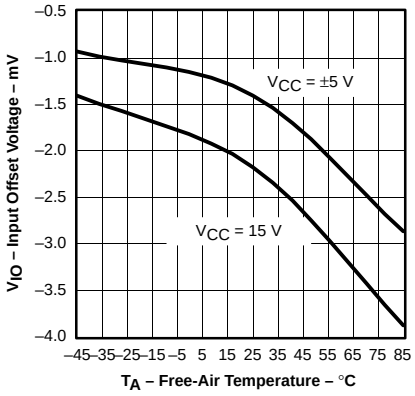


Figure 61

OFFSET VOLTAGE vs COMMON-MODE INPUT VOLTAGE RANGE

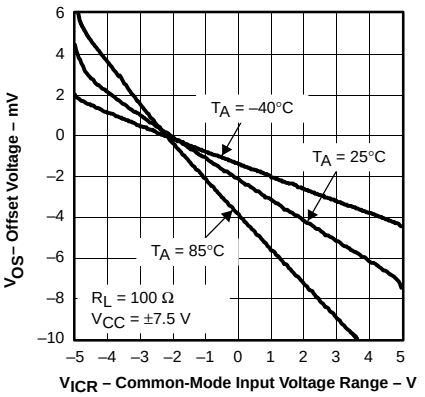


Figure 62

INPUT BIAS CURRENT vs FREE-AIR TEMPERATURE

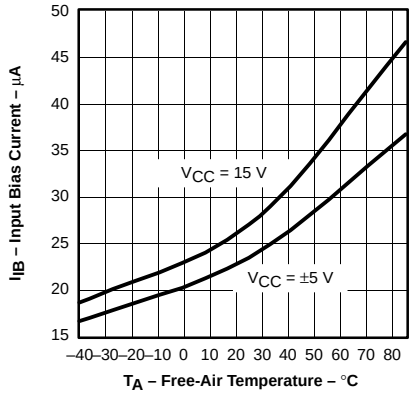


Figure 63

INPUT BIAS CURRENT vs INPUT COMMON MODE RANGE

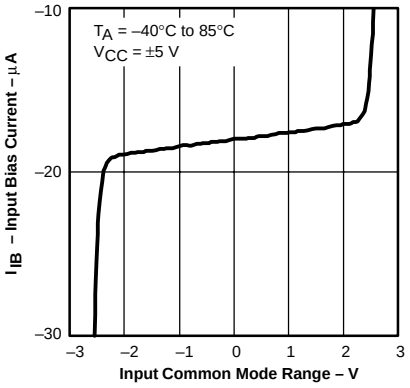


Figure 64

POSITIVE POWER SUPPLY REJECTION RATIO vs POSITIVE POWER SUPPLY

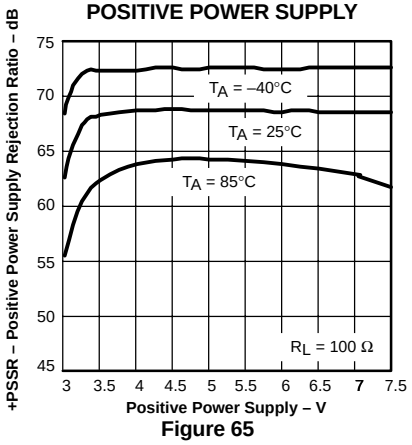


Figure 65

NEGATIVE POWER SUPPLY REJECTION RATIO vs NEGATIVE POWER SUPPLY

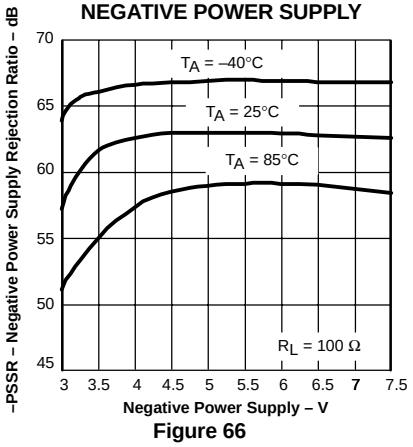


Figure 66

POSITIVE OUTPUT VOLTAGE SWING vs FREE-AIR TEMPERATURE

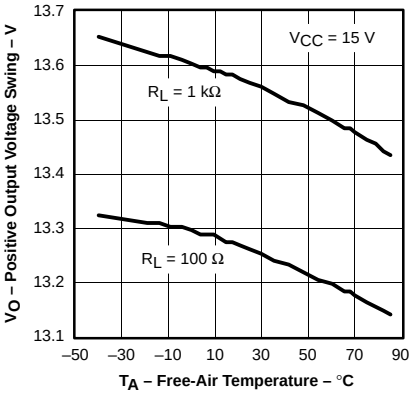


Figure 67

POSITIVE OUTPUT VOLTAGE SWING vs FREE-AIR TEMPERATURE

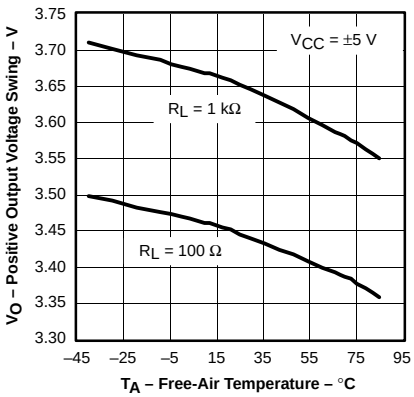


Figure 68

NEGATIVE OUTPUT VOLTAGE SWING vs FREE-AIR TEMPERATURE

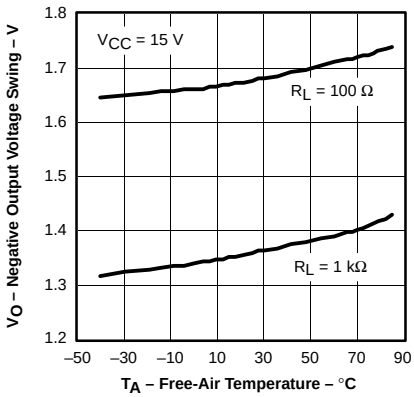


Figure 69

NEGATIVE OUTPUT VOLTAGE SWING vs FREE-AIR TEMPERATURE

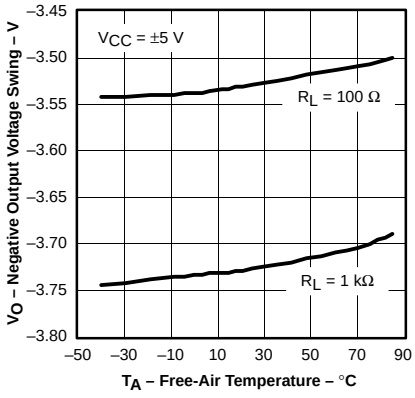


Figure 70

OUTPUT CURRENT SINKING vs POWER SUPPLY

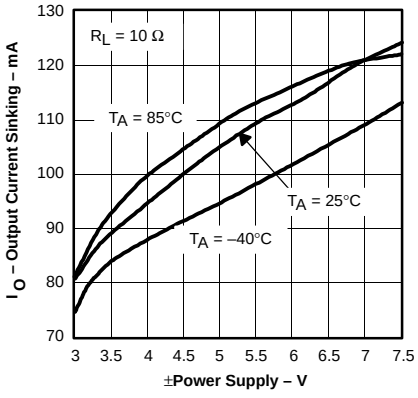


Figure 71

OUTPUT CURRENT SOURCING vs POWER SUPPLY

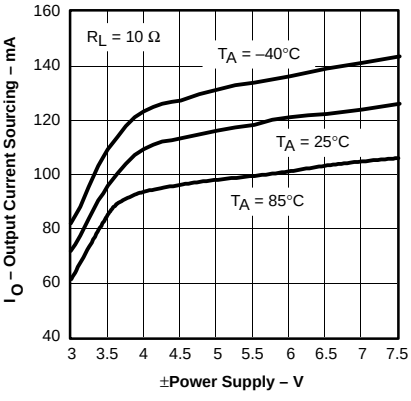


Figure 72

OVERDRIVE RECOVERY TIME

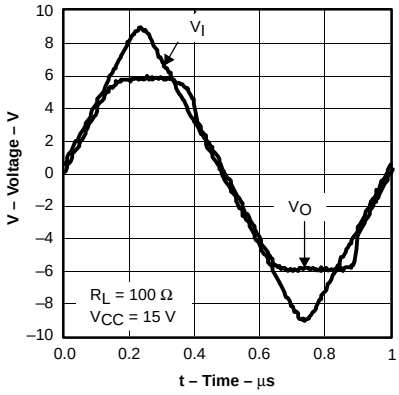


Figure 73

OVERDRIVE RECOVERY TIME

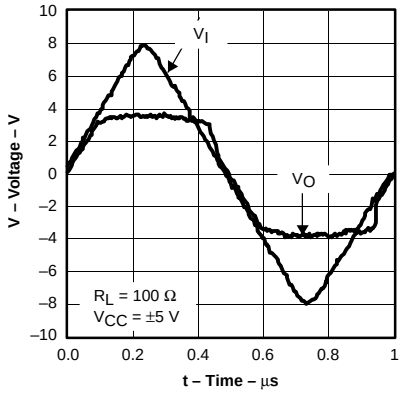


Figure 74

SLEW RATE vs OUTPUT VOLTAGE

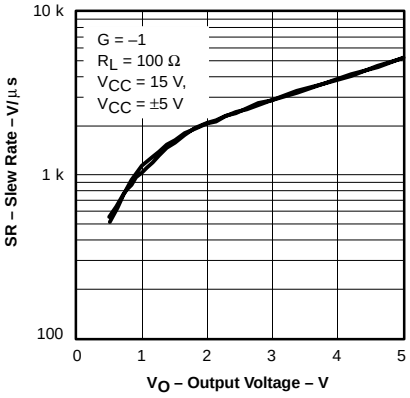


Figure 75

SLEW RATE vs OUTPUT VOLTAGE

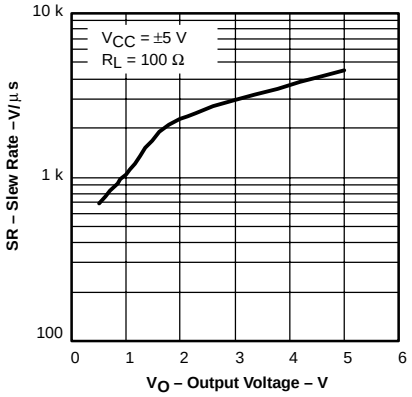


Figure 76

SLEW RATE vs OUTPUT VOLTAGE

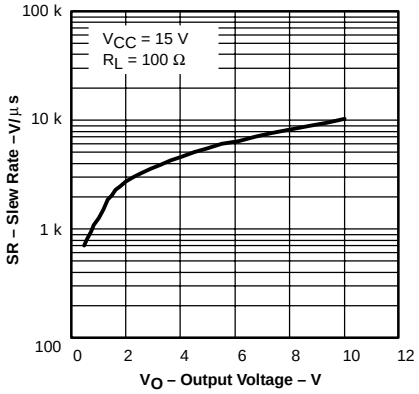


Figure 77

OUTPUT VOLTAGE TRANSIENT RESPONSE

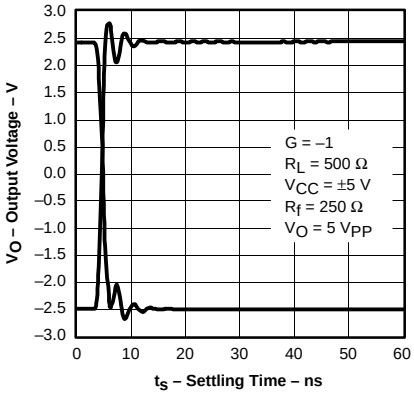


Figure 78

SETTLING TIME

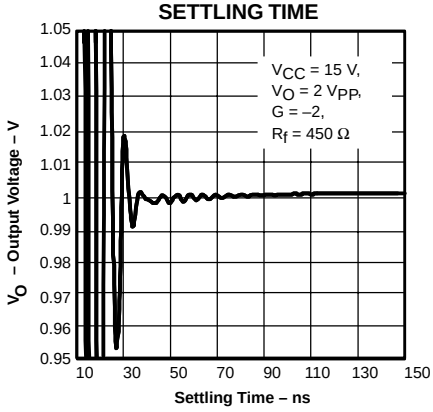


Figure 79

SETTLING TIME

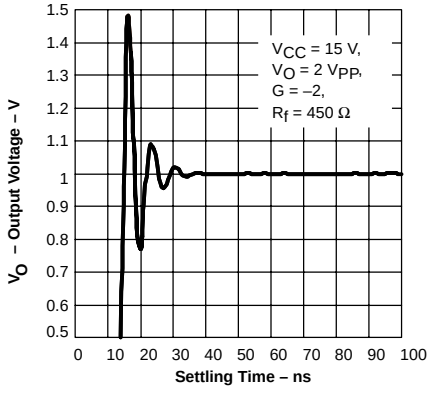


Figure 80

DC COMMON-MODE REJECTION RATIO HIGH vs INPUT COMMON MODE RANGE

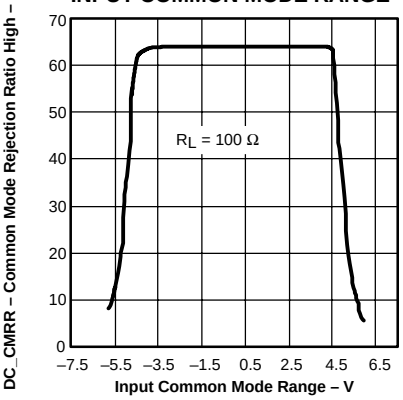


Figure 81

POWER SUPPLY REJECTION RATIO vs FREQUENCY

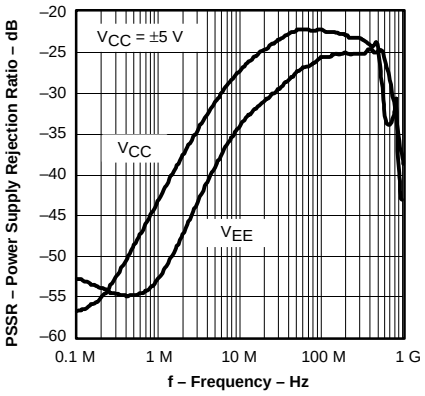


Figure 82

POWER SUPPLY REJECTION RATIO vs FREQUENCY

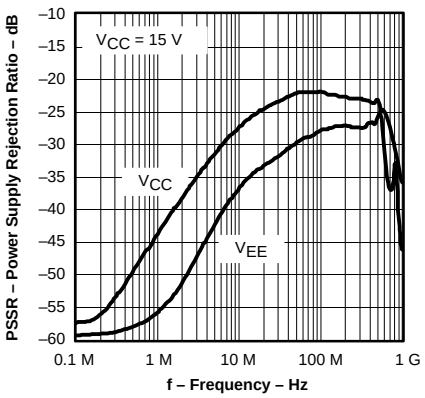


Figure 83

DIFFERENTIAL GAIN ERROR vs 150-Ω LOADS

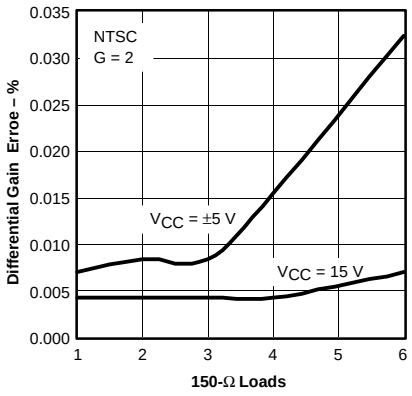


Figure 84

DIFFERENTIAL GAIN ERROR vs 150-Ω LOADS

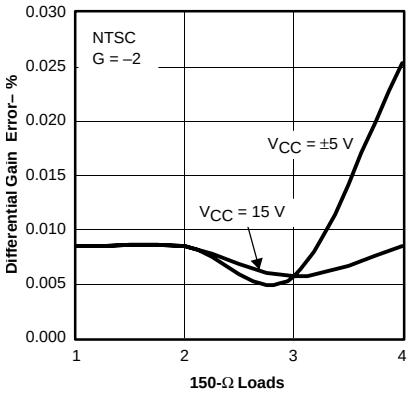


Figure 85

DIFFERENTIAL PHASE ERROR vs 150-Ω LOADS

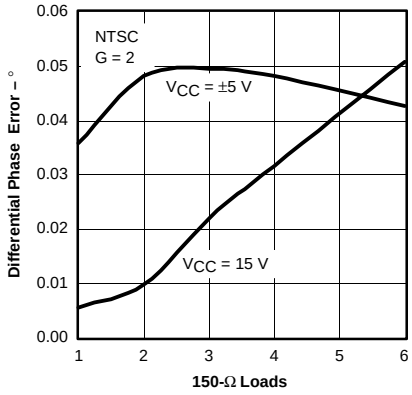


Figure 86

DIFFERENTIAL PHASE ERROR vs 150-Ω LOADS

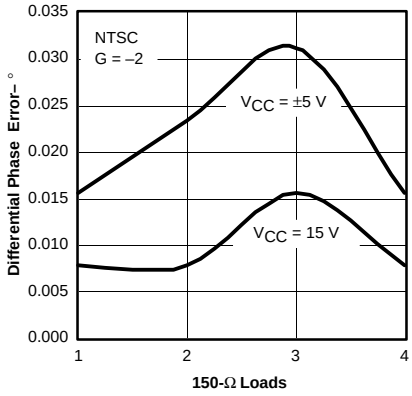


Figure 87

DIFFERENTIAL GAIN ERROR vs 150-Ω LOADS

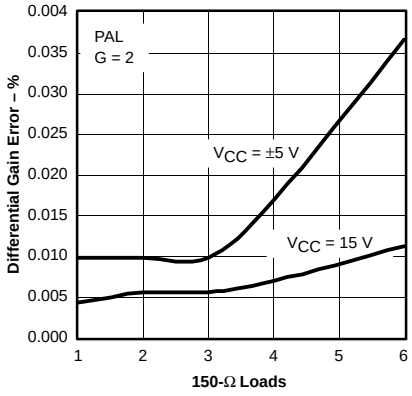


Figure 88

DIFFERENTIAL PHASE ERROR vs 150-Ω LOADS

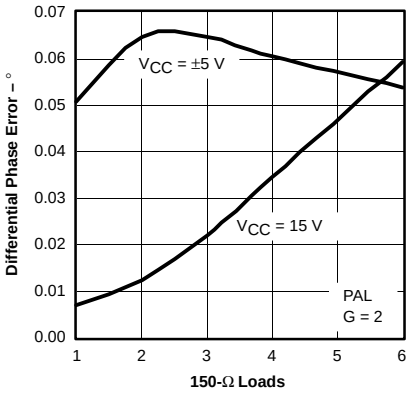


Figure 89

APPLICATION INFORMATION

INTRODUCTION

The THS3202 is a high-speed, operational amplifier configured in a current-feedback architecture. The device is built using Texas Instruments BiCOM–II process, a 15-V, dielectrically isolated, complementary bipolar process with NPN and PNP transistors possessing f_Ts of several GHz. This configuration implements an exceptionally high-performance amplifier that has a wide bandwidth, high slew rate, fast settling time, and low distortion.

RECOMMENDED FEEDBACK AND GAIN RESISTOR VALUES

As with all current-feedback amplifiers, the bandwidth of the THS3202 is an inversely proportional function of the value of the feedback resistor. The recommended resistors for the optimum frequency response are shown in Table 1. These should be used as a starting point and once optimum values are found, 1% tolerance resistors should be used to maintain frequency response characteristics. For most applications, a feedback resistor value of 750 Ω is recommended—a good compromise between bandwidth and phase margin that yields a very stable amplifier.

Table 1. Recommended Resistor Values for Optimum Frequency Response

THS3202 R_F for AC When R_{load} = 100 Ω			
GAIN	V_{sup}	Peaking	R_F Value
1	15	Optimum	619
	±5	Optimum	619
2	15	Optimum	536
	±5	Optimum	536
5	15	Optimum	402
	±5	Optimum	402
10	15	Optimum	200
	±5	Optimum	200
–1	15	Optimum	450
	±5	Optimum	450

As shown in Table 1, to maintain the highest bandwidth with an increasing gain, the feedback resistor is reduced. The advantage of dropping the feedback resistor (and the gain resistor) is the noise of the system is also reduced compared to no reduction of these resistor values, see noise calculations section. Thus, keeping the bandwidth as high as possible maintains very good distortion performance of the amplifier by keeping the excess loop gain as high as possible.

Care must be taken to not drop these values too low. The amplifier's output must drive the feedback resistance (and gain resistance) and may place a burden on the amplifier. The end result is that distortion may actually increase due to the low impedance load presented to the amplifier. Careful management of the amplifier bandwidth and the associated loading effects needs to be examined by the designer for optimum performance.

The THS3202 amplifier exhibit very good distortion performance and bandwidth with the capability of utilizing up to 15 V power supplies. Their excellent current drive capability of up to 115 mA driving into a 20-Ω load allows for many versatile applications. One application is driving a twisted pair line (i.e., telephone line). Figure 90 shows a simple circuit for driving a twisted pair differentially.

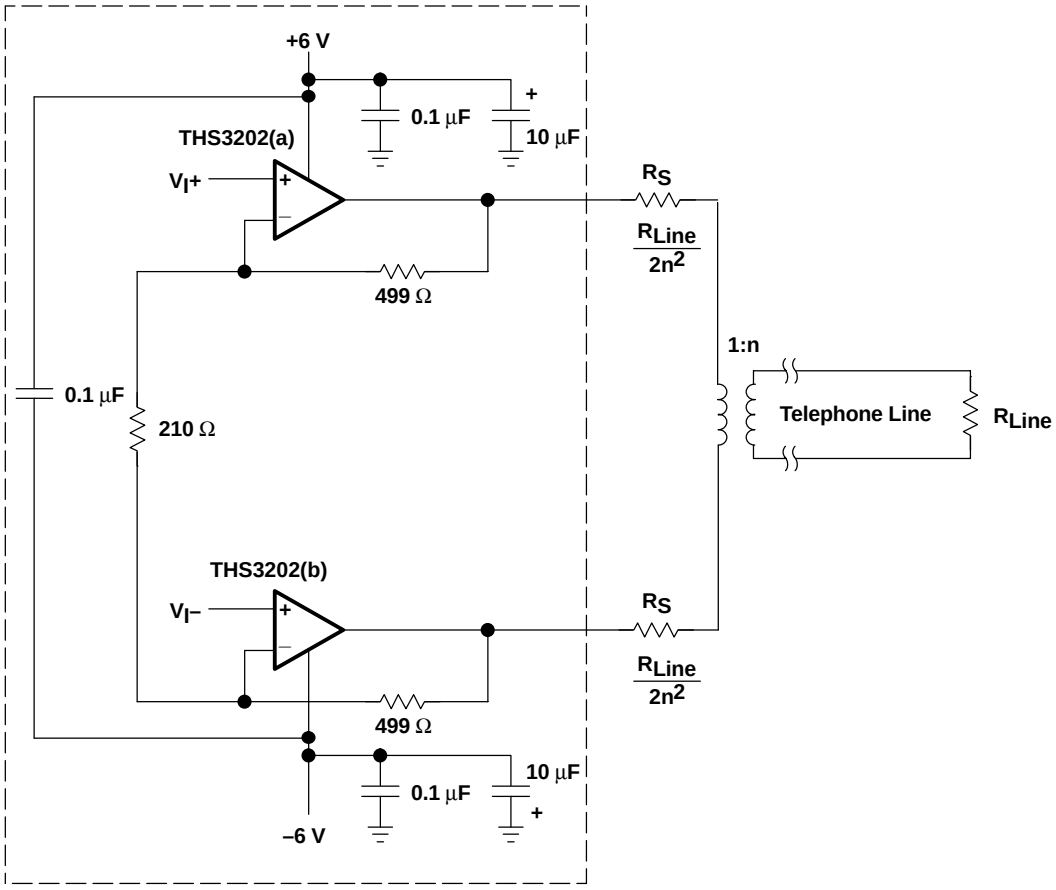


Figure 90. Simple Line Driver With THS3202

Due to the large power supply voltages and the large current drive capability, power dissipation of the amplifier must not be neglected. To have as much power dissipation as possible in a small package, the THS3202 is available only in a MSOP–8 PowerPAD package (DGN) and SOIC–8 package (D). Again, power dissipation of the amplifier must be carefully examined or else the amplifiers could become too hot and performance can be severely degraded. See the *Power Dissipation and Thermal Considerations* section for more information on thermal management.

NOISE CALCULATIONS

Noise can cause errors on very small signals. This is especially true for amplifying small signals coming over a transmission line or an antenna. The noise model for current-feedback amplifiers (CFB) is the same as for voltage feedback amplifiers (VFB). The only difference between the two is that CFB amplifiers generally specify different current-noise parameters for each input, while VFB amplifiers usually only specify one noise-current parameter. The noise model is shown in Figure 91. This model includes all of the noise sources as follows:

- e_n = Amplifier internal voltage noise (nV/$\sqrt{Hz}$)
- IN+ = Noninverting current noise (pA/$\sqrt{Hz}$)
- IN– = Inverting current noise (pA/$\sqrt{Hz}$)
- e_{Rx} = Thermal voltage noise associated with each resistor (e_{Rx} = 4 kTR_x)

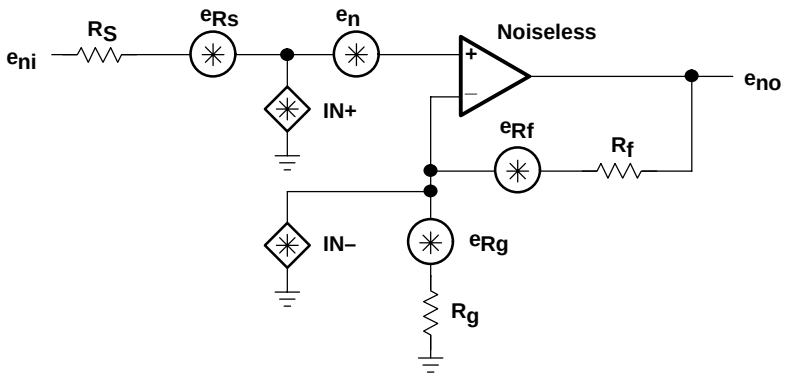


Figure 91. Noise Model

The total equivalent input noise density (e_{ni}) is calculated by using the following equation:

$$e_{ni} = \sqrt{(e_n)^2 + \left(IN+ \times R_S\right)^2 + \left(IN- \times \left(R_f \parallel R_g\right)\right)^2 + 4\,kTR_s + 4\,kT\left(R_f \parallel R_g\right)}$$

where:

k = Boltzmann's constant = 1.380658×10^{-23}
T = Temperature in degrees Kelvin (273 +°C)
$R_f \parallel R_g$ = Parallel resistance of R_f and R_g

To get the equivalent output noise of the amplifier, just multiply the equivalent input noise density (e_{ni}) by the overall amplifier gain (A_V).

$$e_{no} = e_{ni}\,A_V = e_{ni}\left(1 + \frac{R_f}{R_g}\right) \text{ (Noninverting Case)}$$

As the previous equations show, to keep noise at a minimum, small value resistors should be used. As the closed-loop gain is increased (by reducing R_F and R_G), the input noise is reduced considerably because of the parallel resistance term. This leads to the general conclusion that the most dominant noise sources are the source resistor (R_S) and the internal amplifier noise voltage (e_n). Because noise is summed in a root-mean-squares method, noise sources smaller than 25% of the largest noise source can be effectively ignored. This can greatly simplify the formula and make noise calculations much easier.

This brings up another noise measurement usually preferred in RF applications, the noise figure (NF). Noise figure is a measure of noise degradation caused by the amplifier. The value of the source resistance must be defined and is typically 50 Ω in RF applications.

$$NF = 10\log\left[\frac{e_{ni}^2}{e_{Rs}^2}\right]$$

Because the dominant noise components are generally the source resistance and the internal amplifier noise voltage, we can approximate noise figure as:

$$NF = 10\log\left[1 + \frac{\left[\left(e_n\right)^2 + \left(IN+ \times R_S\right)^2\right]}{4\,kTR_S}\right]$$

PRINTED-CIRCUIT BOARD LAYOUT TECHNIQUES FOR OPTIMAL PERFORMANCE

Achieving optimum performance with high frequency amplifier-like devices in the THS320x family requires careful attention to board layout parasitic and external component types.

Recommendations that optimize performance include:

- Minimize parasitic capacitance to any ac ground for all of the signal I/O pins. Parasitic capacitance on the output and input pins can cause instability. To reduce unwanted capacitance, a window around the signal I/O pins should be opened in all of the ground and power planes around those pins. Otherwise, ground and power planes should be unbroken elsewhere on the board.
- Minimize the distance (< 0.25”) from the power supply pins to high frequency 0.1-μF and 100 pF decoupling capacitors. At the device pins, the ground and power plane layout should not be in close proximity to the signal I/O pins. Avoid narrow power and ground traces to minimize inductance between the pins and the decoupling capacitors. The power supply connections should always be decoupled with these capacitors. Larger (6.8 μF or more) tantalum decoupling capacitors, effective at lower frequency, should also be used on the main supply pins. These may be placed somewhat farther from the device and may be shared among several devices in the same area of the PC board. The primary goal is to minimize the impedance seen in the differential-current return paths. For driving differential loads with the THS3202, adding a capacitor between the power supply pins improves 2nd order harmonic distortion performance. This also minimizes the current loop formed by the differential drive.
- Careful selection and placement of external components preserve the high frequency performance of the THS320x family. Resistors should be a very low reactance type. Surface-mount resistors work best and allow a tighter overall layout. Again, keep their leads and PC board trace length as short as possible. Never use wirebound type resistors in a high frequency application. Since the output pin and inverting input pins are the most sensitive to parasitic capacitance, always position the feedback and series output resistors, if any, as close as possible to the inverting input pins and output pins. Other network components, such as input termination resistors, should be placed close to the gain-setting resistors. Even with a low parasitic capacitance shunting the external resistors, excessively high resistor values can create significant time constants that can degrade performance. Good axial metal-film or surface-mount resistors have approximately 0.2 pF in shunt with the resistor. For resistor values > 2.0 kΩ, this parasitic capacitance can add a pole and/or a zero that can effect circuit operation. Keep resistor values as low as possible, consistent with load driving considerations.
- Connections to other wideband devices on the board may be made with short direct traces or through onboard transmission lines. For short connections, consider the trace and the input to the next device as a lumped capacitive load. Relatively wide traces (50 mils to 100 mils) should be used, preferably with ground and power planes opened up around them. Estimate the total capacitive load and determine if isolation resistors on the outputs are necessary. Low parasitic capacitive loads (< 4 pF) may not need an R_S since the THS320x family is nominally compensated to operate with a 2-pF parasitic load. Higher parasitic capacitive loads without an R_S are allowed as the signal gain increases (increasing the unloaded phase margin). If a long trace is required, and the 6-dB signal loss intrinsic to a doubly-terminated transmission line is acceptable, implement a matched impedance transmission line using microstrip or stripline techniques (consult an ECL design handbook for microstrip and stripline layout techniques).

  A 50-Ω environment is not necessary onboard, and in fact, a higher impedance environment improves distortion as shown in the distortion versus load plots. With a characteristic board trace impedance based on board material and trace dimensions, a matching series resistor into the trace from the output of the THS320x is used as well as a terminating shunt resistor at the input of the destination device.

  Remember also that the terminating impedance is the parallel combination of the shunt resistor and the input impedance of the destination device: this total effective impedance should be set to match the trace impedance. If the 6-dB attenuation of a doubly terminated transmission line is unacceptable, a long trace can be series-terminated at the source end only. Treat the trace as a capacitive load in this case. This does not preserve signal integrity as well as a doubly-terminated line. If the input impedance of the destination device is low, there is some signal attenuation due to the voltage divider formed by the series output into the terminating impedance.
- Socketing a high speed part like the THS320x family is not recommended. The additional lead length and pin-to-pin capacitance introduced by the socket can create an extremely troublesome parasitic network which can make it almost impossible to achieve a smooth, stable frequency response. Best results are obtained by soldering the THS320x family parts directly onto the board.

PowerPAD DESIGN CONSIDERATIONS

The THS320x family is available in a thermally-enhanced PowerPAD family of packages. These packages are constructed using a downset leadframe upon which the die is mounted [see Figure 92(a) and Figure 92(b)]. This arrangement results in the lead frame being exposed as a thermal pad on the underside of the package [see Figure 92(c)]. Because this thermal pad has direct thermal contact with the die, excellent thermal performance can be achieved by providing a good thermal path away from the thermal pad.

The PowerPAD package allows for both assembly and thermal management in one manufacturing operation. During the surface-mount solder operation (when the leads are being soldered), the thermal pad can also be soldered to a copper area underneath the package. Through the use of thermal paths within this copper area, heat can be conducted away from the package into either a ground plane or other heat dissipating device.

The PowerPAD package represents a breakthrough in combining the small area and ease of assembly of surface mount with the, heretofore, awkward mechanical methods of heatsinking.

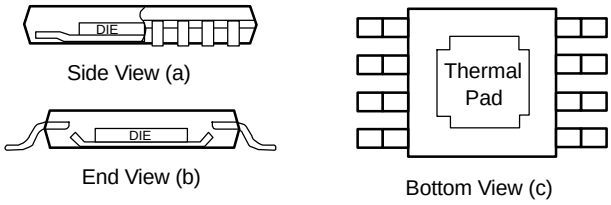


Figure 92. Views of Thermally Enhanced Package

Although there are many ways to properly heatsink the PowerPAD package, the following steps illustrate the recommended approach.

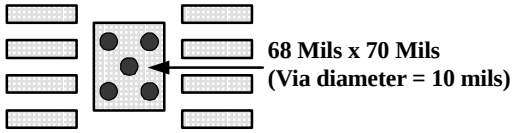


Figure 93. DGN PowerPAD PCB Etch and Via Pattern

PowerPAD PCB LAYOUT CONSIDERATIONS

1. Prepare the PCB with a top side etch pattern as shown in Figure 93. There should be etch for the leads as well as etch for the thermal pad.
2. Place five holes in the area of the thermal pad. These holes should be 10 mils in diameter. Keep them small so that solder wicking through the holes is not a problem during reflow.
3. Additional vias may be placed anywhere along the thermal plane outside of the thermal pad area. This helps dissipate the heat generated by the THS320x family IC. These additional vias may be larger than the 10-mil diameter vias directly under the thermal pad. They can be larger because they are not in the thermal pad area to be soldered so that wicking is not a problem.
4. Connect all holes to the internal ground plane.
5. When connecting these holes to the ground plane, **do not** use the typical web or spoke via connection methodology. Web connections have a high thermal resistance connection that is useful for slowing the heat transfer during soldering operations. This makes the soldering of vias that have plane connections easier. In this application, however, low thermal resistance is desired for the most efficient heat transfer. Therefore, the holes under the THS320x family PowerPAD package should make their connection to the internal ground plane with a complete connection around the entire circumference of the plated-through hole.
6. The top-side solder mask should leave the terminals of the package and the thermal pad area with its five holes exposed. The bottom-side solder mask should cover the five holes of the thermal pad area. This prevents solder from being pulled away from the thermal pad area during the reflow process.
7. Apply solder paste to the exposed thermal pad area and all of the IC terminals.
8. With these preparatory steps in place, the IC is simply placed in position and run through the solder reflow operation as any standard surface-mount component. This results in a part that is properly installed.

POWER DISSIPATION AND THERMAL CONSIDERATIONS

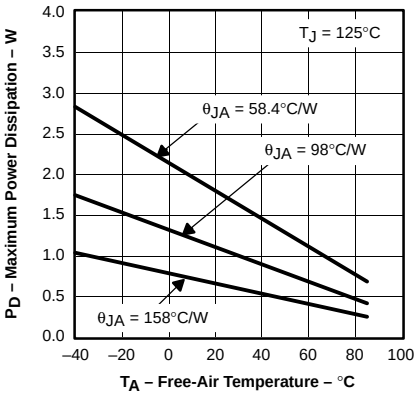
To maintain maximum output capabilities, the THS3202 does not incorporate automatic thermal shutoff protection. The designer must take care to ensure that the design does not violate the absolute maximum junction temperature of the device. Failure may result if the absolute maximum junction temperature of 150°C is exceeded. For best performance, design for a maximum junction temperature of 125°C. Between 125°C and 150°C, damage does not occur, but the performance of the amplifier begins to degrade.

The thermal characteristics of the device are dictated by the package and the PC board. Maximum power dissipation for a given package can be calculated using the following formula.

$$P_{Dmax} = \frac{T_{max} - T_A}{\theta_{JA}}$$

where:
P_{Dmax} is the maximum power dissipation in the amplifier (W).
T_{max} is the absolute maximum junction temperature (°C).
T_A is the ambient temperature (°C).
$\theta_{JA} = \theta_{JC} + \theta_{CA}$
θ_{JC} is the thermal coefficient from the silicon junctions to the case (°C/W).
θ_{CA} is the thermal coefficient from the case to ambient air (°C/W).

For systems where heat dissipation is more critical, the THS320x family of devices is offered in an 8-pin MSOP with PowerPAD and the THS3202 is available in the SOIC–8 PowerPAD package offering even better thermal performance. The thermal coefficient for the PowerPAD packages are substantially improved over the traditional SOIC. Maximum power dissipation levels are depicted in the graph for the available packages. The data for the PowerPAD packages assume a board layout that follows the PowerPAD layout guidelines referenced above and detailed in the PowerPAD application note number SLMA002. The following graph also illustrates the effect of not soldering the PowerPAD to a PCB. The thermal impedance increases substantially which may cause serious heat and performance issues. Be sure to always solder the PowerPAD to the PCB for optimum performance.



Results are With No Air Flow and PCB Size = 3”x3”
θ_{JA} = 58.4°C/W for 8-Pin MSOP w/PowerPad (DGN)
θ_{JA} = 98°C/W for 8-Pin SOIC High Test PCB (D)
θ_{JA} = 158°C/W for 8-Pin MSOP w/PowerPad w/o Solder

Figure 94. Maximum Power Dissipation vs Ambient Temperature

When determining whether or not the device satisfies the maximum power dissipation requirement, it is important to not only consider quiescent power dissipation, but also dynamic power dissipation. Often times, this is difficult to quantify because the signal pattern is inconsistent, but an estimate of the RMS power dissipation can provide visibility into a possible problem.

DRIVING A CAPACITIVE LOAD

Driving capacitive loads with high-performance amplifiers is not a problem as long as certain precautions are taken. The first is to realize that the THS3202 has been internally compensated to maximize its bandwidth and slew-rate performance. When the amplifier is compensated in this manner, capacitive loading directly on the output decreases the device’s phase margin leading to high-frequency ringing or oscillations. Therefore, for capacitive loads of greater than 10 pF, it is recommended that a resistor be placed in series with the output of the amplifier, as shown in Figure 95. A minimum value of 10 Ω should work well for most applications. For example, in 75-Ω transmission systems, setting the series resistor value to 75 Ω both isolates any capacitance loading and provides the proper line impedance matching at the source end.

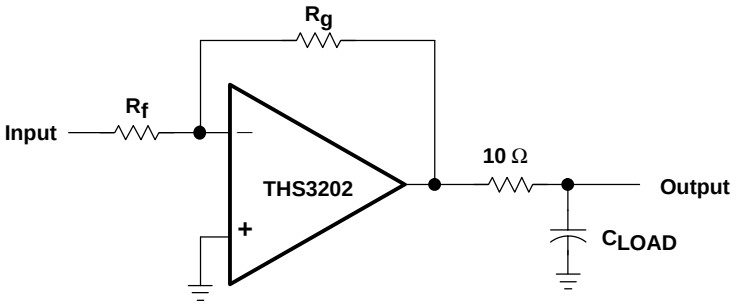
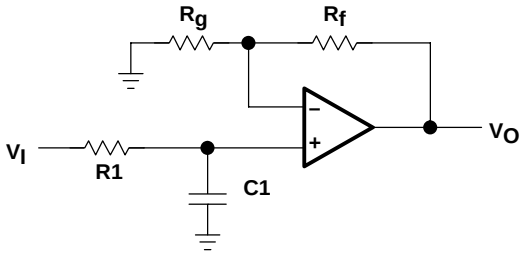


Figure 95. Driving a Capacitive Load

GENERAL CONFIGURATIONS

A common error for the first-time CFB user is creating a unity gain buffer amplifier by shorting the output directly to the inverting input. A CFB amplifier in this configuration oscillates and is *not* recommended. The THS3202, like all CFB amplifiers, *must* have a feedback resistor for stable operation. Additionally, placing capacitors directly from the output to the inverting input is not recommended. This is because, at high frequencies, a capacitor has a very low impedance. This results in an unstable amplifier and should not be considered when using a current-feedback amplifier. Because of this, integrators and simple low-pass filters, which are easily implemented on a VFB amplifier, have to be designed slightly differently. If filtering is required, simply place an RC-filter at the noninverting terminal of the operational-amplifier (see Figure 96).

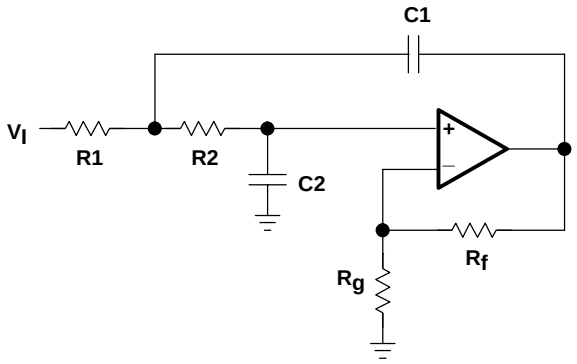


$$f_{-3dB} = \frac{1}{2\pi R1C1}$$

$$\frac{V_O}{V_I} = \left(1 + \frac{R_f}{R_g}\right)\left(\frac{1}{1 + sR1C1}\right)$$

Figure 96. Single-Pole Low-Pass Filter

If a multiple-pole filter is required, the use of a Sallen-Key filter can work very well with CFB amplifiers. This is because the filtering elements are not in the negative feedback loop and stability is not compromised. Because of their high slew-rates and high bandwidths, CFB amplifiers can create very accurate signals and help minimize distortion. An example is shown in Figure 97.



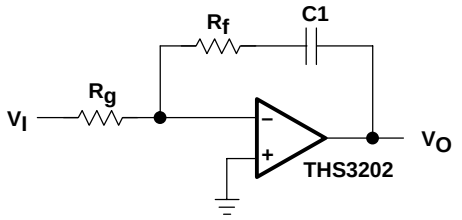
R1 = R2 = R
C1 = C2 = C
Q = Peaking Factor
(Butterworth Q = 0.707)

$$f_{-3dB} = \frac{1}{2\pi RC}$$

$$R_g = \frac{R_f}{\left(2 - \frac{1}{Q}\right)}$$

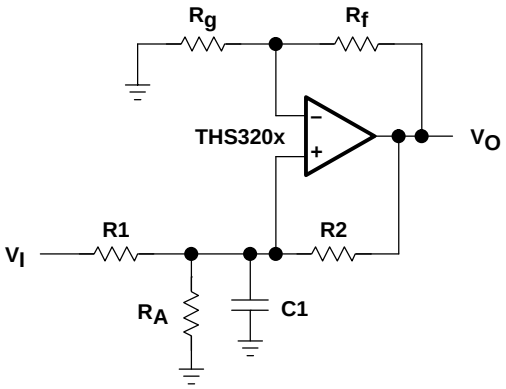
Figure 97. 2-Pole Low-Pass Sallen-Key Filter

There are two simple ways to create an integrator with a CFB amplifier. The first, shown in Figure 98, adds a resistor in series with the capacitor. This is acceptable because at high frequencies, the resistor is dominant and the feedback impedance never drops below the resistor value. The second, shown in Figure 99, uses positive feedback to create the integration. Caution is advised because oscillations can occur due to the positive feedback.



$$\frac{V_O}{V_I} = \left(\frac{R_f}{R_g}\right)\left[\frac{S + \frac{1}{R_f C1}}{S}\right]$$

Figure 98. Inverting CFB Integrator



For Stable Operation:

$$\frac{R2}{R1 \parallel R_A} \geq \frac{R_f}{R_g}$$

$$V_O \cong V_I \left(\frac{1 + \frac{R_f}{R_g}}{sR1C1}\right)$$

Figure 99. Noninverting CFB Integrator

The THS3202 may also be employed as a very good video distribution amplifier. One characteristic of distribution amplifiers is the fact that the differential phase (DP) and the differential gain (DG) are compromised as the number of lines increases and the closed-loop gain increases. Be sure to use termination resistors throughout the distribution system to minimize reflections and capacitive loading.

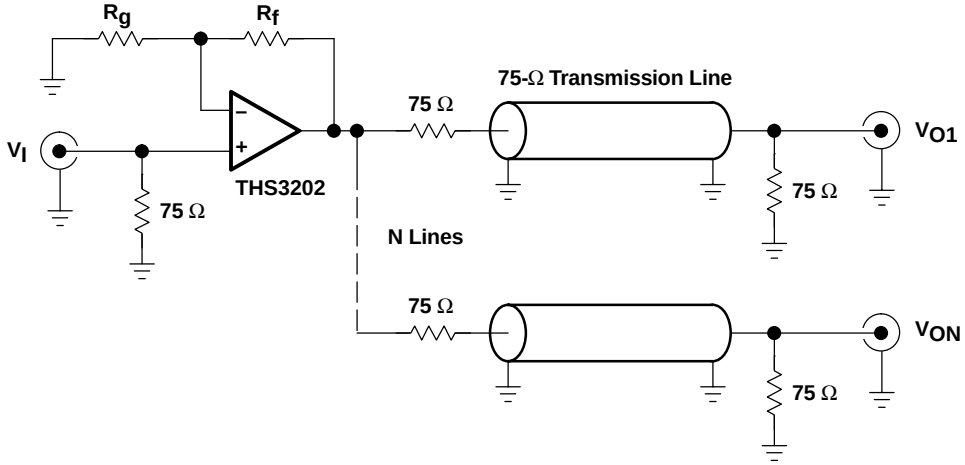
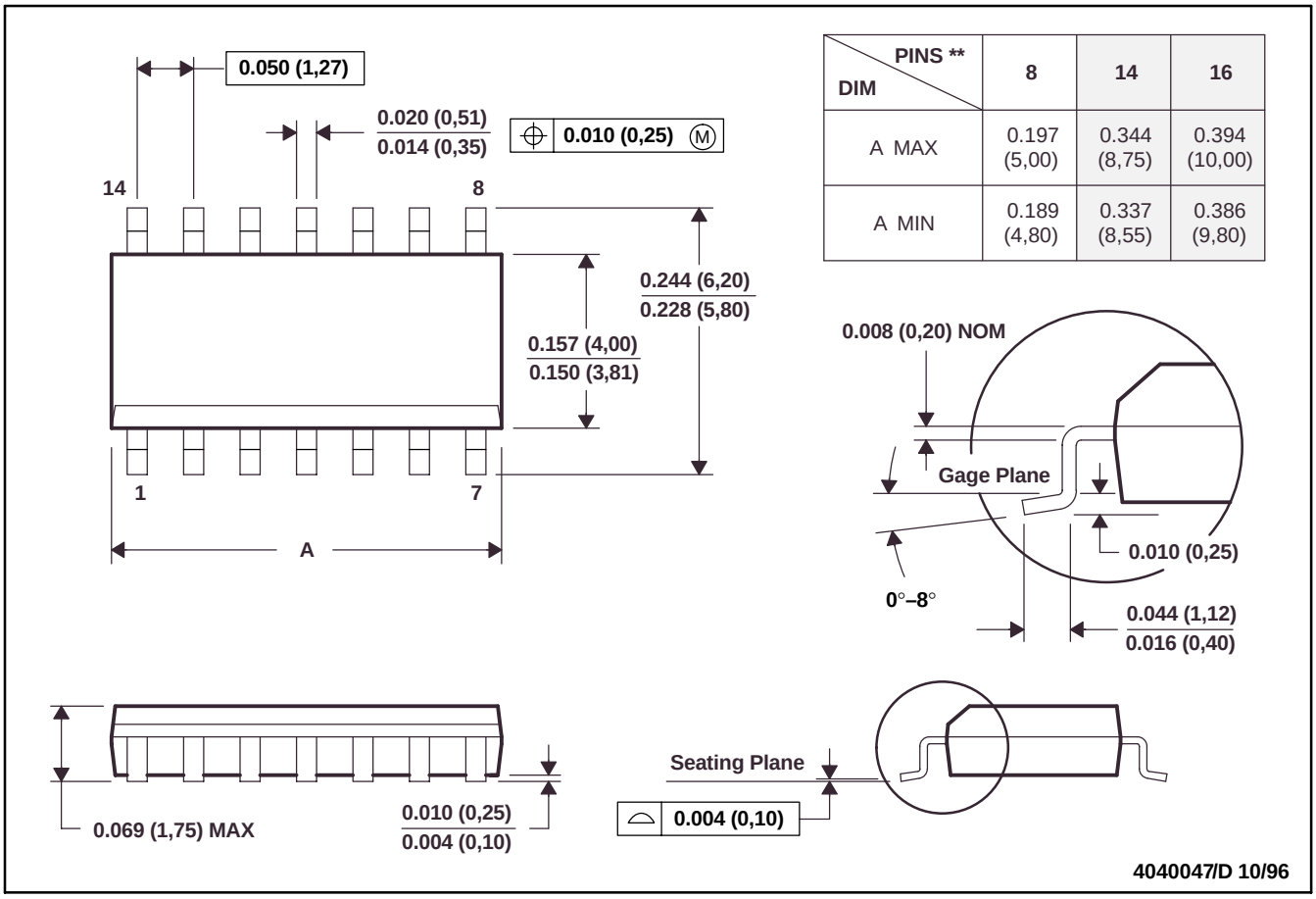


Figure 100. Video Distribution Amplifier Application

MECHANICAL INFORMATION

D (R-PDSO-G**) PLASTIC SMALL-OUTLINE PACKAGE

14 PIN SHOWN

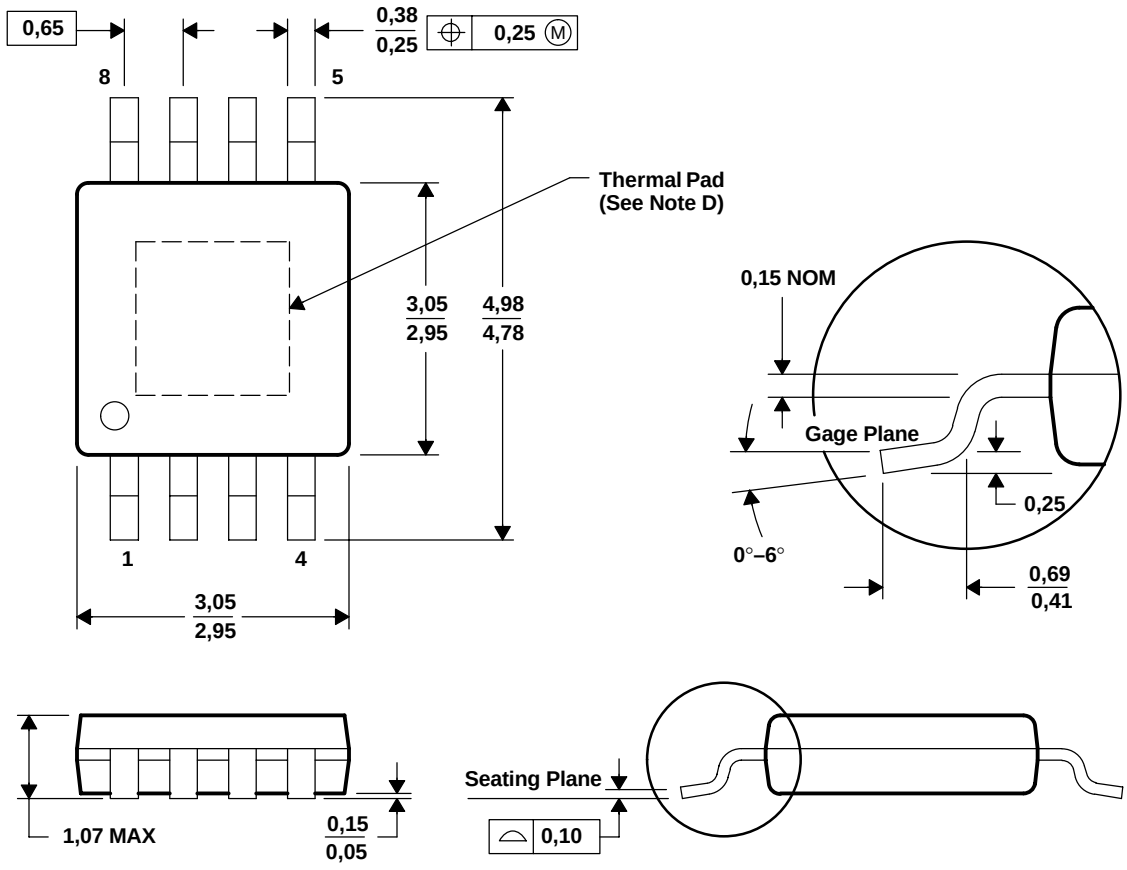


DIM \ PINS **	8	14	16
A MAX	0.197 (5,00)	0.344 (8,75)	0.394 (10,00)
A MIN	0.189 (4,80)	0.337 (8,55)	0.386 (9,80)

NOTES:A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0.006 (0,15).
D. Falls within JEDEC MS-012

MECHANICAL INFORMATION

DGN (S-PDSO-G8) **PowerPAD™ PLASTIC SMALL-OUTLINE PACKAGE**



NOTES:A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions include mold flash or protrusions.
D. The package thermal performance may be enhanced by attaching an external heat sink to the thermal pad. This pad is electrically and thermally connected to the backside of the die and possibly selected leads.
E. Falls within JEDEC MO-187

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