

Master in Photonics

MASTER THESIS WORK

**Development of nanocrystal based light
sources in silicon**

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Development of nanocrystal based light sources in silicon

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Abstract. In the present work we have fabricated capacitors with silicon nanocrystals embedded in a dielectric matrix. All the techniques used in the fabrication process are fully compatible with CMOS technology. We will show the luminescence of the device when a continuous voltage is applied between the top and bottom contacts. Also, we will see how the intensity–current curve suggests charge trapping in silicon nanocrystals and the creation of conductive paths within the dielectric matrix.

1. Introduction: light emission in silicon

It is difficult to overstate the importance of the role played by microelectronics in our everyday life. Silicon has been the material of choice by the microelectronics industry. The effort invested in silicon microelectronics has lead to high levels of integration, which make possible the high performance and interconnections of today’s microelectronic circuits. However, several issues arise due to the current integration, such as overheating, propagation delays and information latency between single devices.

Photonic circuits are the answer to those issues. Information can be encoded in light using intensity, polarization, wavelength, phase or frequency, and allows high bandwidths. Optical devices consume less power than electronic devices and photon–photon interactions are negligible compared to electron–electron interactions, which makes interconnections simpler. Of course, a light source is needed. Moreover, if we want the light source to be integrated in the circuit its fabrication should be compatible with the technologies used in microelectronics fabrication processes.

In the mid 80s D.J. DiMaria observed electroluminescence in silicon rich silicon dioxide layers [1] and related the effect to quantum confinement. At that time, nanocrystals were reported in silicon rich silicon oxide layers [2]. In the early 90s photoluminescence was observed and related to silicon [3] and germanium [4] nanocrystals embedded in silicon dioxide matrices and porous silicon layers [5]. In the mid 90s silicon nanoclusters in silica matrices received more attention and the first memory device based on silicon nanoclusters was proposed [6]. This has led to floating nanocluster-gate transistors and electro-optical memory cells both in silicon oxide [7]

and silicon nitride [8]. At this point, three milestones were established: integration with CMOS, optical gain and a silicon laser. The first one was achieved with porous silicon [9]. Optical gain was achieved using erbium doped silicon nanoclusters [10]. Finally, a silicon laser based on the Raman effect was demonstrated in 2005 [11]. But there is still work to be done.

Silicon has not been the semiconductor of choice for photonic circuits due to its low efficiency as a light emitter. The low efficiency comes as a consequence of its indirect band gap, which renders radiative electron–hole recombination highly improbable. It is indeed possible to enhance the probability of radiative recombination in bulk crystalline silicon [12], but the results show very low power as well as poor efficiency [13]. Silicon nanostructures seem to be the path to follow in order to achieve practical silicon based light sources.

Nowadays, light emitting silicon nanocrystals embedded in dielectric matrices are obtained by a wide range of techniques. In particular, ion implantation, chemical vapor deposition and sputtering are CMOS compatible. The use of CMOS compatible techniques is of outmost importance in order to achieve integration with standard electronic circuits.

Luminescence in silicon nanocrystals is related to the spatial localization of the wave function of the charge carriers. According to the Heisenberg uncertainty principle, the wave function in the reciprocal space should be delocalized when the wave function in the real space is localized. If the reciprocal wave functions of an electron at the minimum of the conduction band and a hole at the maximum of the valence band spread enough due to the localization in the direct space, then the overlap between the two wave functions might be nonzero, thus leading to an increased probability of a radiative recombination taking place.

In the present work a set of capacitors with embedded silicon nanocrystals in its dielectric layer has been fabricated. We will show the intensity–voltage response of the devices as well as the spectrum of the emitted light.

2. Fabrication

The fabrication process has been carried out in the clean room facilities at the *Institut de Microelectrònica de Barcelona (IMB–CNM–CSIC)*.

The process starts with p-type silicon wafers ($0.1\text{--}1.4\ \Omega\cdot\text{cm}$). The main fabrication steps are described in the following list. The evolution of the layers on the wafer along the process is pictured in figure 1. Note that the thicknesses of different layers do not have the same proportions as the real devices.

- a *Growing an oxide layer (figure 1(a)).* The oxide growth takes place in a furnace at $1000\ ^\circ\text{C}$ using pure oxygen as the oxidation agent. The thickness of the grown layer is controlled by the duration of the process. The oxide grows on both sides of the wafer, so we will have to remove the oxide on the back side later.

- b *Silicon implantation (figure 1(b))*. Silicon ions are added to the front oxide layer by ion implantation. The dose is $1.8 \cdot 10^{16} \text{ cm}^{-2}$ at an energy of 25 KeV. After the implantation a thermal anneal is necessary in order to activate the implanted ions (move them from interstitial position to points that belong to the crystalline lattice) and also to restore the damage produced by the implantation process.
- c *Thermal anneal (figure 1(c))*. The wafers stay in a furnace at 1100 °C during four hours. This process induces the agglomeration of the excess silicon atoms in the oxide matrix into approximately spherical silicon nanocrystals with a radius of several nanometers.
- d *Doping the back contact (figure 1(d))*. In order to get a good contact on the back of the wafer, Boron is implanted by ion implantation. The dose is $5.0 \cdot 10^{14} \text{ cm}^{-2}$ at 80 KeV. The back oxide layer is thin enough so as not to affect the implantation process.
- e *Depositing polysilicon (figure 1(e))*. A 350 nm thick polycrystalline silicon layer will act as a front contact once n-doped until degeneracy. The high doping will change the behavior of the polysilicon layer to make it almost metallic. Moreover, polycrystalline silicon shows a good transparency, which will allow the light emitted in the underlying layer to escape. If a regular aluminium contact was used light would not be transmitted through due to its high reflectivity and absorbance, resulting in a confinement of the emitted light between the silicon and the aluminium.
- f *Depositing UV-patternable photoresist (figure 1(f))*. We will define our structures by means of photolithography. The first step in this process is to deposit a UV-patternable photoresist layer by spinning.
- g *Exposing to light (figure 1(g))*. The photoresist is exposed to UV light through a mask showing the pattern we want to transfer to the wafer. The exposed regions of the photoresist will change so as to make them soluble.
- h *Removing the photoresist (figure 1(h))*. The illuminated regions of the photoresist are removed by a suitable solvent. The remaining regions will act as a protection layer when we etch the underlying polysilicon and oxide layers as well as the silicon substrate.
- i *Etching the layers (figure 1(i))*. A dry etching process will remove the polysilicon and oxide layers. We will etch further to get a 100 nm deep trench on the silicon substrate.
- j *Removing the photoresist (figure 1(j))*. The remaining photoresist is removed by means of plasma oxygen.
- k *Removing the back layers and metalizing the back contact (figure 1(k))*. The back layers (polysilicon and oxide) are etched away. After that, a 1 micron thick aluminum layer is deposited by sputtering to make the back contact.

In figure 2 a 3D model of the device is shown. It is worth noting that the X-Y dimensions are at scale, but not so the Z dimension. The thickness of the silicon substrate is about 500 microns. The silicon trench is 100 nm deep while the oxide and polysilicon layers are 30 nm and 350 nm respectively. Note also that the contact pads

have an aluminum layer in the picture but we did not use it since we put the probe directly on the capacitor. The lateral sizes of the five square capacities are (in microns) 1000, 500, 200, 100 and 50. Also, some features that we do not use on the right side of the device are missing from the picture.

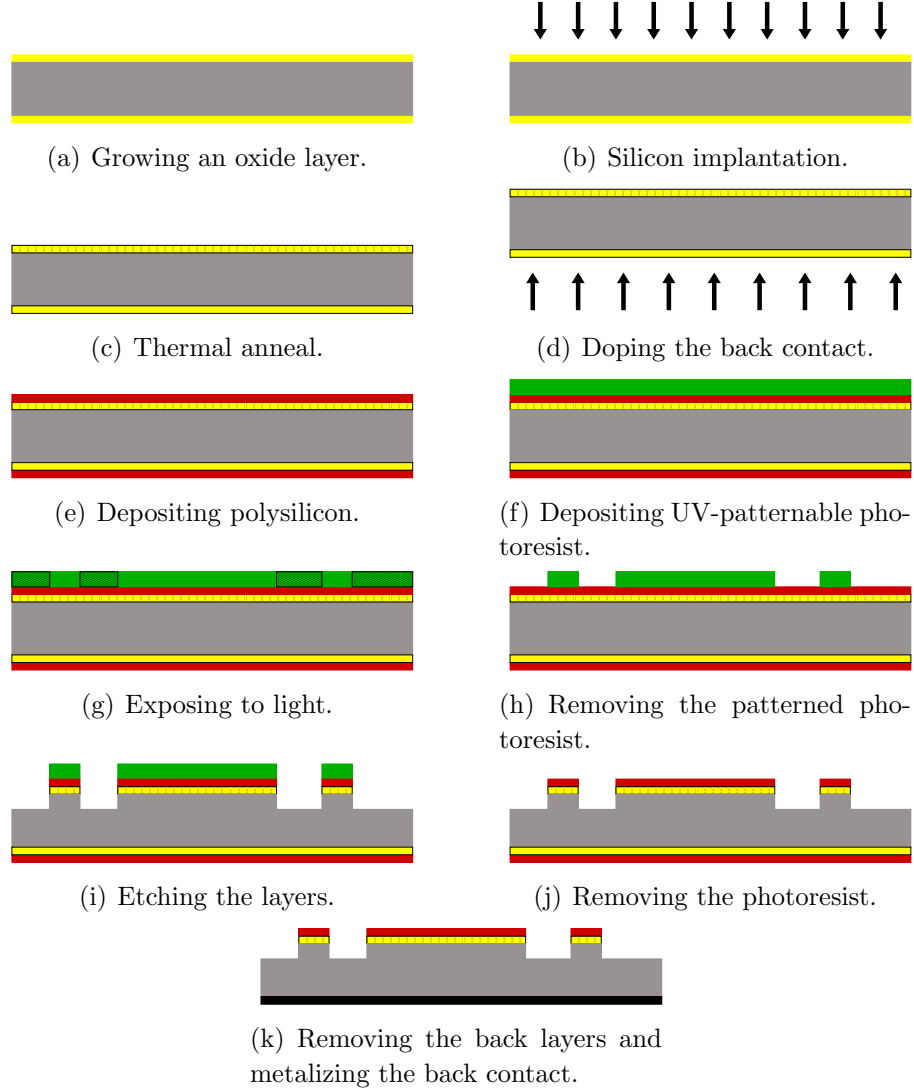


Figure 1: Schematic of the steps needed to get our devices.

3. Experimental setup and results

3.1. Setup

The measurements have been carried out in a probe system Karl Suss PA200 (see figure 3(a)) since the chips do not have any external connection. An HP 4155B semiconductor parameter analyzer (figure 3(b)) is used to set a voltage between the probe and the plate where the wafer lays. The plate will be kept at ground voltage and so will be the back

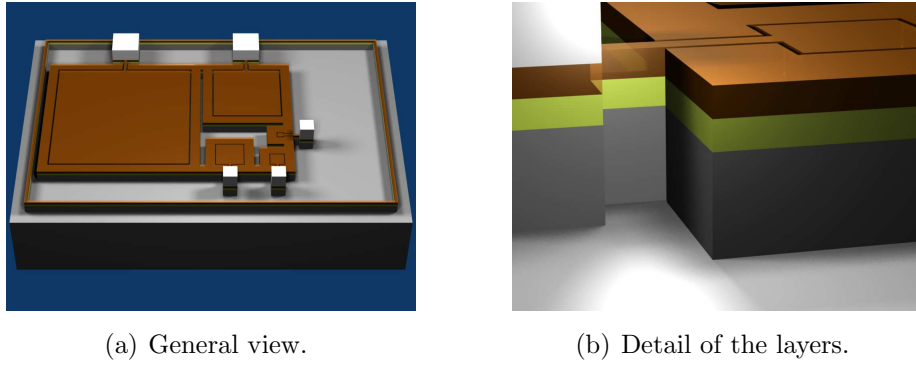


Figure 2: 3D model of the devices used in the present work.

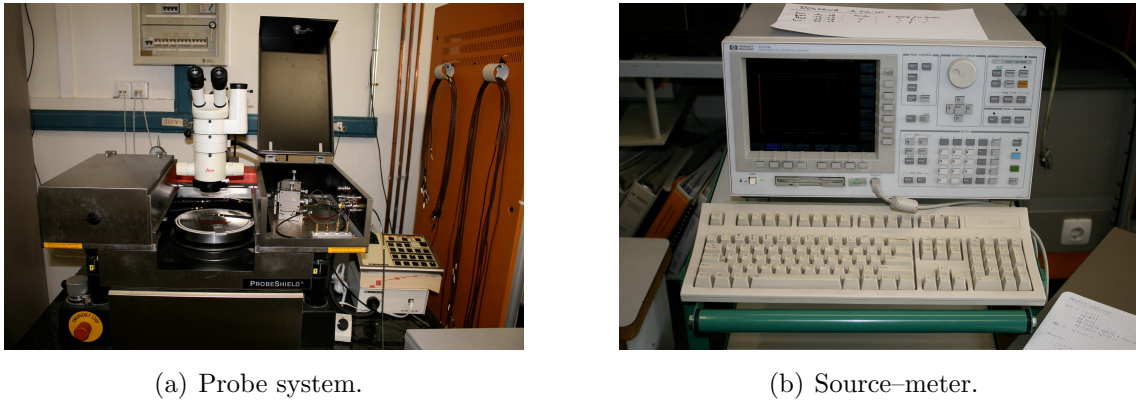


Figure 3: The probe system and the source-meter used to carry out the experiments.

contact of the wafer. The probe will be used to set the gate voltage. Figure 4 shows the probe laying on the polysilicon surface as seen through a microscope.

We will perform voltage sweeps from 0 V to the voltage for which the current reaches the maximum compliance limit of the source (100 mA). For positive voltages the limit will be reached at about 17 V. For negative voltages the limit appears at approximately -7 V. We can also perform complete sweeps from the negative limit to the positive one. The delay between points is 100 ms.

Also, at each sweep we will monitor both the current entering (exiting) the device through the polysilicon contact and the current exiting (entering) the device through the back contact.

In order to acquire the spectrum of the emitted light, a $200\text{ }\mu\text{m}$ optical fiber has been used. One end points to the light source and the other end is connected to a spectrometer Ocean Optics HR4000, which in turn is connected to a personal computer (see figure 5).

3.2. Results

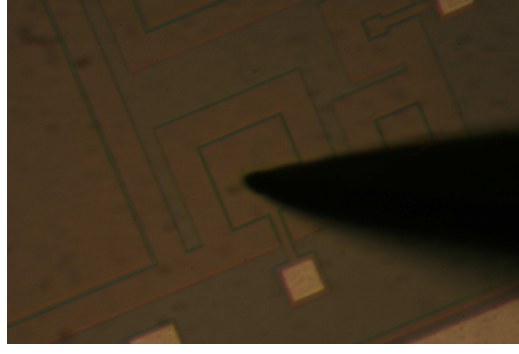
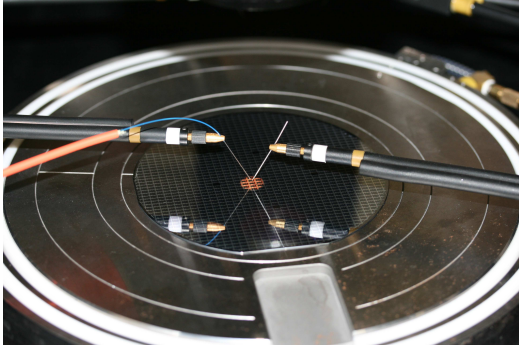
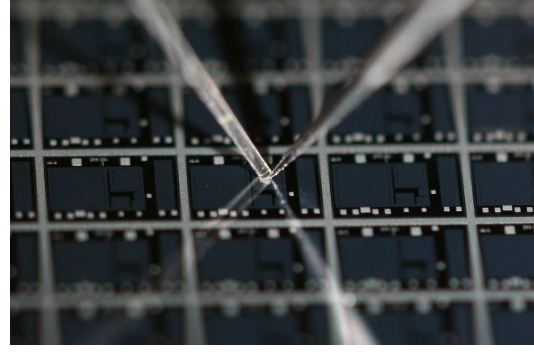


Figure 4: Probe laying on the polysilicon contact of a capacitor. The picture has been taken with an ordinary digital camera focusing the objective at the focal point of a microscope ocular.



(a) The picture shows the probe used to electrically stress the device (right) and the optical fiber used to collect the emitted light (left).

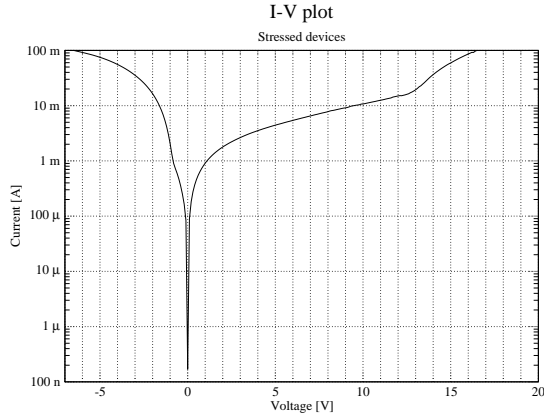


(b) Detail of the probe and the fiber close to the device.

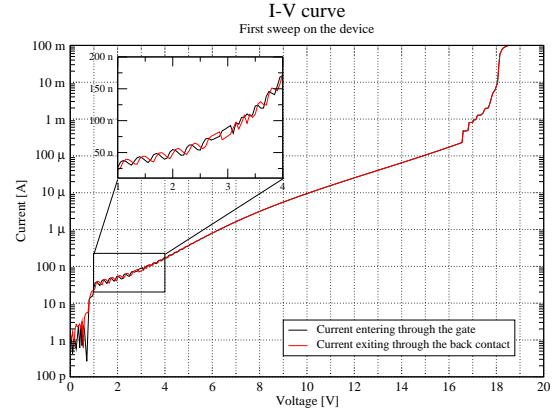
Figure 5: The probe system and the source-meter used to carry out the experiments.

3.2.1. I-V characteristics. Current-voltage curves have been measured for different devices and different capacitance areas. No relevant differences are observed between them. A typical current-voltage plot is shown in figure 6(a). The sign of the current has been omitted to clarify the plot. For positive voltages the current flows from the gate to the back contact. It is worth noting the asymmetry between the curve for positive and negative voltages. Since the substrate is p-doped the majority carriers are holes in the valence band. On the other hand, the polysilicon top contact is n-doped so that the majority carriers are electrons in the conduction band. Therefore, under negative bias (accumulation) the current will increase faster than for positive bias (inversion).

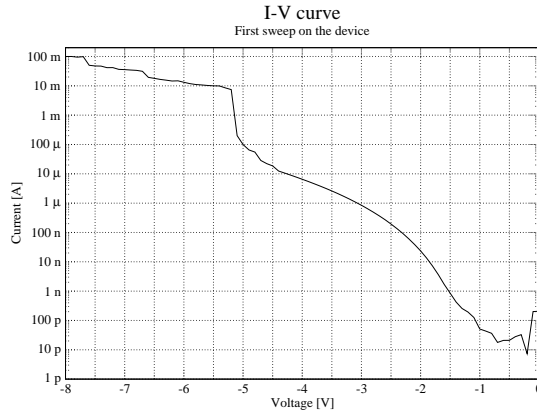
In figure 6(b) we can see the current-voltage curve measured during the very first sweep. The sweep starts at 0 volts and increases until the maximum compliance limit imposed by the source-meter. Two curves are plotted. The black one is the current entering the device through the polysilicon top contact, while the red one accounts



(a) A typical current–voltage plot for our devices. The voltage is set between the gate and the back contact, positive meaning higher voltage at the gate and negative meaning higher voltage at the back contact.



(b) Current–voltage curve of the first sweep. The sudden increase in the conduction at $\simeq 16.6$ V suggests the creation of conductive paths within the dielectric matrix. The behavior shown in the inset plot might be related to charge trapping in silicon nanocrystals and a Coulomb blockade on the charges trying to tunnel behind.



(c) Current–voltage curve of the first sweep measured at negative voltages. The behavior is similar to that of positive voltages, although the conductive paths start to appear at lower voltages, $\simeq -5$ V.

Figure 6: Current–voltage curves.

for the current exiting through the back contact. The delay time between consecutive measurements is 100 ms. Between 1 and 5 V we can see a mismatch between both currents. This might be related to charge trapping in silicon nanocrystals and a subsequent Coulomb blockade on the charges trying to tunnel behind. At 16.6 V the current suddenly increases, suggesting the creation of conductive paths through the dielectric matrix. Once the paths are created, subsequent sweeps show curves similar to the general curve shown in figure 6(a). If the first sweep is carried out starting at

the maximum voltage and decreasing we will directly get a curve similar to the general one, since the high starting current creates conductive paths right away.

If the first sweep on the device is carried over negative voltages the effect is similar, although the conductive paths start to appear at lower voltages (see figure 6(c)) and we do not see traces of charge trapping such those observed at low positive voltages. Once the conductive paths are created we will get a behavior such as the one shown in figure 6(a) regardless of how the paths have been created (using a forward or backward sweep over positive or negative voltages).

3.2.2. Electroluminescence. Luminescence is observed at positive bias for currents above several milliamperes and is never observed for negative bias. Luminescence appears through a bunch of glowing dots around the position where the probe contacts the polysilicon, the affected area being about $150 \mu\text{m}^2$. Other clusters may appear at other positions. Moreover, if we change the position of the probe a new bunch of glowing dots appears around the new position although the dots around the previous position still glow. The dots around the first position fade down with further measurements.

The spectral composition of the emitted light is shown in figure 7. We can see that it spreads over the visible region with three clear peaks.

Light emission in materials with embedded silicon nanocrystals is not completely understood yet. Defects, silicon nanocrystals or the SiO_2 /nanocrystal interface have been proposed to act as recombination centers at different wavelengths. Luminescent peaks below 600 nm are mainly due to defects [14–19]. The origin of peaks at longer wavelengths is still controversial and two main models have been proposed. According to the first model luminescence takes place inside silicon nanocrystals due to quantum confinement effects, emission coming from band to band radiative recombinations. The second model relates luminescence to the presence of defects in the SiO_2 /nanocrystal interface.

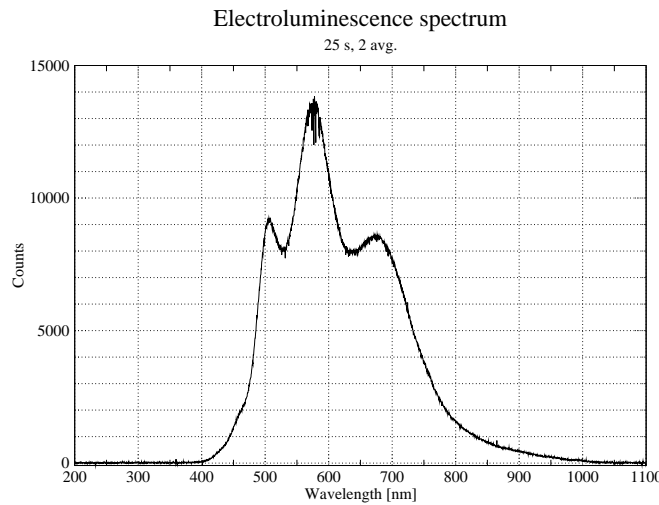


Figure 7: Spectrum of the emitted light.

4. Conclusions

In this work we have shown that we can get visible light from silicon nanocrystals embedded in dielectric matrices in CMOS compatible devices. The current–voltage curves suggest the creation of conductive paths through silicon nanocrystals, where radiative recombination can take place. We observe luminescence when the current flowing through the device is above several milliamperes.

It is possible to get usable silicon based light sources using CMOS compatible technology. However, there is still much to do in order to increase the emitted power and to better understand the mechanisms by which luminescence is produced. Future work includes the experimentation with new materials and structures.

Acknowledgments

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