Escola Tècnica Superior d'Enginyeria de Telecomunicació de Barcelona
UNIVERSITAT POLITÈCNICA DE CATALUNYA

Low-Power CMOS Circuit Design for Fast Infrared Imagers

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En record del meu germà Pere.

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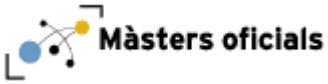

Master thesis dissertation

Low-Power CMOS Circuit Design for Fast Infrared Imagers

presented by Josep Maria Margarit Taulé in order to obtain the Electronics Engineering Research Master Degree, directed by Dr. Francesc Serra Graells, full-time associate professor at Microelectronics and Electronics Systems Department of *Universitat Autònoma de Barcelona*

and advised at Escola Tècnica Superior d'Enginyeria de Telecomunicació de Barcelona by Dr. Jordi Madrenas Boadas, full-time associate professor at Electronics Engineering Department of *Universitat Politècnica de Catalunya*.

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Abstract

This Master Thesis presents in detail state-of-the-art circuit techniques for compact, fully tunable, low-power design of uncooled, fast IR digital Read-Out Integrated Circuits in CMOS technologies. Following this general premises, the work embraces and significantly extends the research started with the Final Career Project "*Tècniques de disseny CMOS per a sistemes de visió híbrids de pla focal modular*" obtaining specific results in three different areas:

Research on the optimum FPA architecture is achieved from the functional to the physical construction approach. As a result, two main focal plane construction processes are presented: a compact, monolithic proposal and a modular, hybrid innovative solution based on in-house CNM multi-chip technologies. Functional simulation is also performed in order to evaluate a general ROIC system design strategy.

A complete set of CMOS basic building blocks are proposed for self-biasing, built-in capacitance and dark current compensation, A/D conversion and a truly digital I/O interface, all at pixel level. Furthermore, full FPN cancellation is supplied by the tuning of both the individual offset and gain of each DPS, either by auto-calibration or external programming, during read-out at no speed costs.

Finally, a real industrial application is presented as the main demonstrator of all the proposed basic building blocks. In this sense, three circuit implementations for IR PbSe sensors and the related monolithic, hybrid ROIC modules have been integrated in standard 0.35μm 2-polySi 4-metal CMOS technology. Electrical and preliminary optical characterization of the up-to-date existing design libraries exhibits not only very low-power operation (sub-μW), high flexibility through digital programmability and high crosstalk immunity, but fine sensitivity and fast response to incident radiation.

Resum

La present tesi de màster detalla novedoses tècniques circuitals per al disseny de circuits integrats digitals CMOS de lectura compactes, de baixa potència i completament programables, destinats a aplicacions d'IR d'alta velocitat operant a temperatura ambient. En aquest sentit, el treball recull i amplia notablement la recerca iniciada en el Projecte Final de Carrera "Tècniques de disseny CMOS per a sistemes de visió híbrids de pla focal modular" obtenint resultats específics en tres diferents àrees:

Es procedeix a la recerca de l'arquitectura òptima d'FPA, tant des del punt de vista funcional com des del de construcció física, resultant-ne dos processos diferents de fabricació del pla focal: una proposta compacte-monolítica i una altra modular-híbrida basada en tecnologies multixip desenvolupades recentment al CNM. Complementàriament, l'ús de simulacions funcionals permet avaluar l'estratègia general de disseny del sistema ROIC.

Es mostra un conjunt complet de blocs bàsics d'autopolarització, compensació de la capacitat d'entrada i del corrent d'obscuritat, conversió A/D i interfície d'E/S exclusivament digital. A més, es proporciona un mecanisme de compensació de l'FPN mitjançant l'ajust individual de l'offset i el guany en cadascun dels DPS, usant autocalibració o programació externa, durant el cicle de lectura i sense cap cost de velocitat.

Finalment, es presenta una aplicació industrial real com a demostrador principal de tots els blocs bàsics estructurals proposats anteriorment. Amb aquest objectiu s'han integrat tres versions diferents de píxel per sensors PbSe d'IR, fabricant-se mòduls ROIC monolítics i híbrids en tecnologia CMOS estàndard 0.35μm 2-PoliSi 4-metall. La caracterització elèctrica i òptica-preliminar de les actuals llibreries de disseny mostra un molt baix consum (inferior al μW), una elevada flexibilitat d'ús gràcies a la programabilitat digital i una forta immunitat als acoblaments interpíxel, a més d'una bona sensibilitat i una ràpida resposta a la radiació incident.

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Acronyms

AC	Alternating Current.
ADC	Analog-to-Digital Converter.
AER	Addressed-Event Representation
AGC	Automatic Gain Control.
AMS	Austria MicroSystems.
APS	Active Pixel Sensor.
ASIC	Application Specific Integrated Circuit.
BDI	Buffered Direct Injection..
BGMI	Buffered Gate Modulation Input.
BLIP	Background Limit IR Performance
CAD	Computer –Aided Design..
CCD	Charge Coupled Devices.
CDS	Correlated Double Sampling.
CIDA	*Centro de Investigación De la Armada*
CPU	Central Processing Unit.
CM	Compact-Monolithic.
CMOS	Complemmentary Metal-Oxide-Semiconductor.
CNM	*Centre Nacional de Microelectrònica.*
CSIC	*Consejo Superior de Investigaciones Científicas*.
CTIA	Capacitive Trans-Impedance Amplifier.
DI	Direct Injection.
DAC	Digital-to-Analog Converter**.**
DC	Direct Current.
DPS	Digital Pixel Sensor.
DRC	Design Rules Check.
ERC	Electrical Rules Check.
FPA	Focal Plane Array.
FPGA	Field Programmable Gate Array**.**
FPN	Fixed-Pattern Noise.
FSK	Frequency Shift Keying.
GPIB	General Purpose Instrumentation Bus.
GMI	Gate Modulation Input.
IC(1)	Integrated Circuit.
IC(2)	Inversion Coefficient.
IEE	Institute of Electrical Engineers.
IEEE	Institute of Electrical and Electronics Engineers.
IMB	Institut de Microelectrònica de Barcelona.
IR	Infra-Red.
ISCAS	IEEE International Symposium on Circuits and Systems.

LVS	Layout Versus Schematic.
LWIR	Long Wavelength Infra-Red.
MCM	Multi-Chip Module.
MCS	Multiple Correlated Sampling.
MH	Modular-Hybrid.
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor.
MWIR	Medium Wavelength Infra-red.
NMOS	N-type Metal-Oxide-Semiconductor.
NIT	New Infra-Red Technologies.
PC(1)	Photo-Conductive.
PC(2)	Personal Computer.
PCM	Pulse-Code Modulation.
PMOS	P-type Metal-Oxide-Semiconductor.
PTAT	Proportional-to-Absolute Temperature.
PSD	Power Spectral Density.
PSRR	Power Supply Rejection Ratio.
PV	Photo-Voltaic.
ROIC	Read-Out Integrated Circuit.
SBDI	Share-Buffered Direct Injection.
SCI	Switched Current Integration.
SFD	Source Follower per Detector.
SPICE	Simulation Program with Integrated Circuits Emphasis.
SPIE	Society of Photo-Optical Instrumentation Engineers
SOC	System-On-Chip.
TCAS	Transactions on Circuits and Systems
VLSI	Very Large Scale Integration.
VPD	Vapor Phase Deposition.

Chapter 1

Introduction

This chapter is devoted to introduce the reader into the project context. In this general sense, motivations for CMOS implementations of low-power and fast imagers are explained. Moreover, industrial applications of these systems are presented, leading to high-density, high-flexibility, low-cost architecture requirements with a strong influence on the design. Hence, the final goal of this work is defined as the research on novel system and circuit techniques, focused on actual necessities, which should exploit the capabilities of CMOS technology for the design of uncooled infrared fast imagers.

1.1. Motivation

In recent years, the imagers market has experimented an emerging demand of low-cost integrated systems, which are in constant evolution in terms of resolution and scanning velocity. These specifications lead to the use of focal plane array (FPA) architectures as depicted in Figure 1.1. In this scenario, a matrix of optical sensors are monolithically or hybridly joined to an equivalent array of CMOS circuits (read-out integrated circuit, ROIC) [HSI97] for the parallel reading of each individual pixel (active pixel sensor, APS).

Imagers' research is currently focused on increasing the focal plane resolution, by means of either reducing pixel sensor and read-out area, or physically increasing FPA matrix size. The first strategy requires progressive scaling of integration technologies, especially in CMOS ROIC circuits, reduction of the APS power consumption and optical refinements of the complete system. The second strategy is applied either through a great fabrication performance of the ROIC, in case of monolithic implementations, or the use of new experimental, modular, hybrid technologies, as explained in Chapter 4.1.

In general, CMOS implementations are preferred due to the following advantages:

- ✓ **Low cost** technology, if last generation sub-micron CMOS processes are not required. This is the case of the circuit techniques presented in this work, which can be manufactured in small series of full-custom ASIC designs at an affordable cost by using advanced, but mature technology.

- ✓ Full compatibility with **mixed A/D design** integration under the same Silicon substrate.

- ✓ **Monolithic µSystems** can be implemented, increasing the performance and reducing the total package cost.

- ✓ **Large scalability**, leading the industry sector of compact devices.

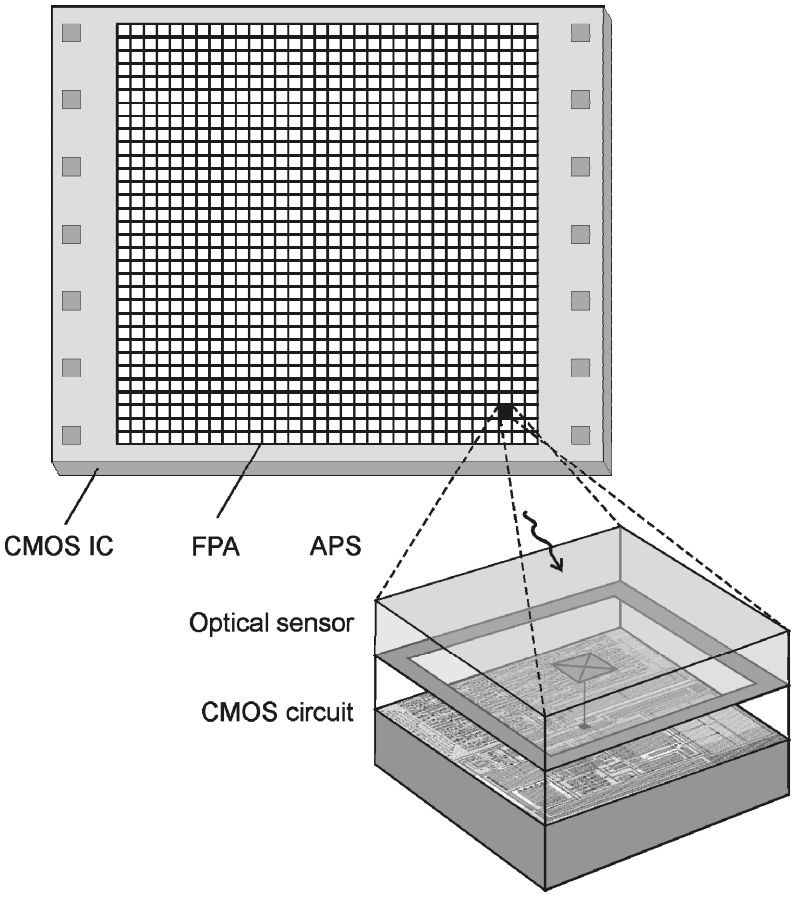


Figure 1.1 General concept of an uncooled CMOS imager

This project is referred to non-visible spectrum applications, is particular to mid-wavelength infrared (MWIR) systems. Infrared vision systems are commonly used for key applications like automotive, medical, scientific and strategic equipments. In this sense, the pixel-by-pixel combination of PbSe detectors and CMOS read-out circuits are a promising technology for uncooled and fast (i.e. real time video) IR imagers, like [VER07]. In this case, the non-Silicon detector FPA layer is attached to the ROIC CMOS circuitry either through technology post-processing or by bump bonding.

Compared to fully integrated Silicon sensors, these transducers exhibit higher dark-to-signal current ratios (e.g. sensors operating at room Temperature) and a larger parasitic capacitance, due to the device geometry, a likely hybrid interconnection and the CMOS circuit itself. These two specific characteristics are added to other common video APS design specifications (reduced integration time, A/D conversion, crosstalk reduction, detector compatibility …), resulting in the final characteristics that define the work.

1.2. Objectives

This Master Thesis, "Low-Power CMOS Circuit Design for Fast Infrared Imagers", is based on the microelectronics research work done at the *Institut de Microelectrònica de Barcelona* (IMB) site of the *Centre Nacional de Microelectrònica* (CNM), belonging to the *Consejo Superior de Investigaciones científicas* (CSIC), and it extends the PFC study previously presented in "*Tècniques de disseny CMOS per a sistemes de visió híbrids de pla focal modular*" [PFC05]. The aim is to develop novel, scalable, low-area, low-power system and CMOS circuit techniques for the design of uncooled infrared fast imagers. Such imagers are addressed to industrial, real-time applications, operating at room temperature, and will be implemented by both monolithic and hybrid technologies. Moreover, the mentioned techniques will exploit the capabilities of standard, moderate scale, CMOS technology in order to create ROIC modules that will integrate and digitally convert the effective signal (i.e. current) provided by a FPA of PbSe sensors that will be explained in Chapter 2.

The main tasks of this work cover from sensor physics to system architecture, focusing on CMOS circuit design:

- ✓ Analysis and modeling of the IR sensor.
- ✓ Vision module specification.
- ✓ High level optimal architecture study for the FPA.
- ✓ Full-custom digital pixel sensor (DPS) CMOS circuit design.
- ✓ Experimental characterization of the resulting DPS cells.
- ✓ Industrial ROIC module construction for both monolithic (i.e. detector attachment by direct deposition) and hybrid (i.e. by bump bonding) system implementations.

This document is conceived as a self-contained project report where not only the latest results, but also the entire research process are described. In this sense, the referred PFC document [PFC05] already reports some general development of the ROIC architecture and a preliminary DPS design for feasibility purposes only. In contrast, this work strongly extends the know-how introducing important design

contributions in the DPS and in the ROIC array integration scheme using standard CMOS technologies. Thus, further research centered on functional block operation, transistor-level design and focal plane implementation is described along the text, resulting in a two-year design-characterization activity in order to obtain a robust read-out circuitry for industrial applications. The work presented here is intended to result in a future doctoral thesis and will be continued with additional research oriented to further DPS scaling and to the final full-system construction and test.

1.3. Structure of the Work

In order to present the study, analysis, design and results of this Master Thesis, the report is structured in the following seven main chapters:

Chapter 1 - Introduction: An overview of the IR CMOS imagers context of the work, its motivation and project objectives.

Chapter 2 - Technology Background: A detailed description of both the infrared detectors theory and the applied detector modeling. The MOSFET equations used in this research are also presented in order to provide a handy analytical tool for the design.

Chapter 3 - IR System Design Overview: A general review of the current IR FPAs structures and its operational requirements, completed with an introduction to the existing read-out topologies and a system design methodology proposal.

Chapter 4 - FPA Architecture: Both monolithic and hybrid FPA construction processes are explained in this point. Furthermore, focal plane architectures are discussed and a global operation strategy is finally defined.

Chapter 5 - DPS Design: Novel CMOS circuit techniques devoted to every active pixel functional block, from self-biasing to the I/O interface. A set of active stages, ready for its integration in full DPS cells.

Chapter 6 - Industrial Application. Uncooled IR Fast Cameras: Implementation of several pixel, matrix size monolithic and hybrid FPAs for real customers. Test vehicle design and results.

Chapter 7 - Conclusions: General knowledge and results derived from master thesis research and foreseeing work in this field.

At the end, a list of the publications referred all through the study is presented, and the annex section provides the schematics related to the circuits described in Chapter 6.

Chapter 2

Technology Background

It is essential in every single design process to acquire fine background knowledge of the technologies related to its synthesis. One of the main goals in this sense is to find simplified mathematical models in order to manage complex system analysis. This project is not an exception, being indeed a must to study and model its two major technologies: the IR PbSe detector and the MOSFET.

2.1. Infrared Detectors

The infrared term refers to radiation located just above the red end of visible spectrum. All objects radiate some energy in the infrared, and the higher the temperature of the object, the higher the spectral radiant energy (i.e. emittance) at all wavelengths and the shorter the peak wavelength of the emissions. Peak emissions of objects at room temperature occur at 10μm, whereas sun has a peak wavelength of 0.53μm, and emits copious amounts of energy from the ultraviolet to beyond the far IR region (Figure 2.1).

Much of the IR emission spectrum is unusable for detection systems because the radiation is absorbed by water or carbon dioxide in the atmosphere. There are several wavelength bands, however, with good transmission:

Long Wavelength IR (LWIR): This band expands roughly 8-14μm, with nearly 100% transmission on the 9-12μm band. LWIR offers excellent visibility of most terrestrial objects.

Medium Wavelength IR (MWIR): This wavelength also offers nearly 100% transmission for in the spectrum between 3.3-5.0μm, with the added benefit of lower ambient, background noise.

Short Wavelength IR (SWIR): A band of high atmospherical transmission and peak solar illumination (0.35-2.5μm), yielding detectors with the best clarity and resolution of the three bands. Without moonlight or artificial illumination, however, SWIR images provide poor or no imagery of objects at 300K.

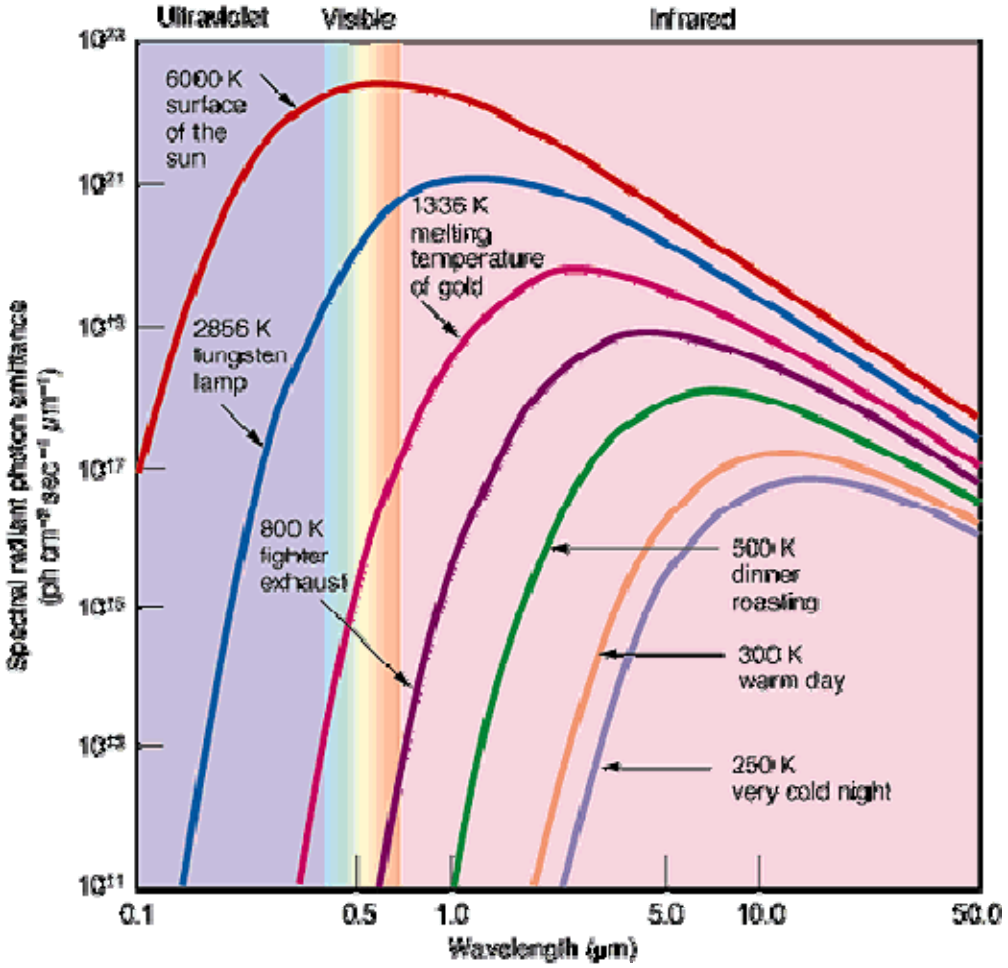


Figure 2.1 Spectral radiant photon emittance of known objects [XEN05]

Since infrared radiation was discovered in 1900, various IR detectors have been developed to convert incident radiation, directly or indirectly, into electrical signals. The detected energy is translated into imagery, even in the dark, allowing an otherwise obscured scene to be seen (Figure 2.3). Hot objects such as people stand out from the typically cooler backgrounds regardless of the available visible light, and revealing features not apparent under regular visible radiation. People and animals are easily seen in total darkness, weaknesses are revealed in structures, components close to failure glow brighter and visibility is improved in adverse conditions such as smoke or fog.

There are two fundamental methods of IR detection, each one based on either thermal or photon effects. Energy (i.e. thermal) detectors respond to temperature changes generated from incident IR radiation through changes in their physical or electrical properties. Thermal detectors are low cost and operated at room temperature, having a wide spectral response. Since the operation of energy detectors involves a change in temperature, they have an inherently slow response and a relatively low sensitivity compared to photon detectors. The response time and sensitivity of a thermal detector are influenced by the heat capacity of detector structure as well as the optical

radiation wavelength. In some applications of these transducers, an optical chopper is also needed.

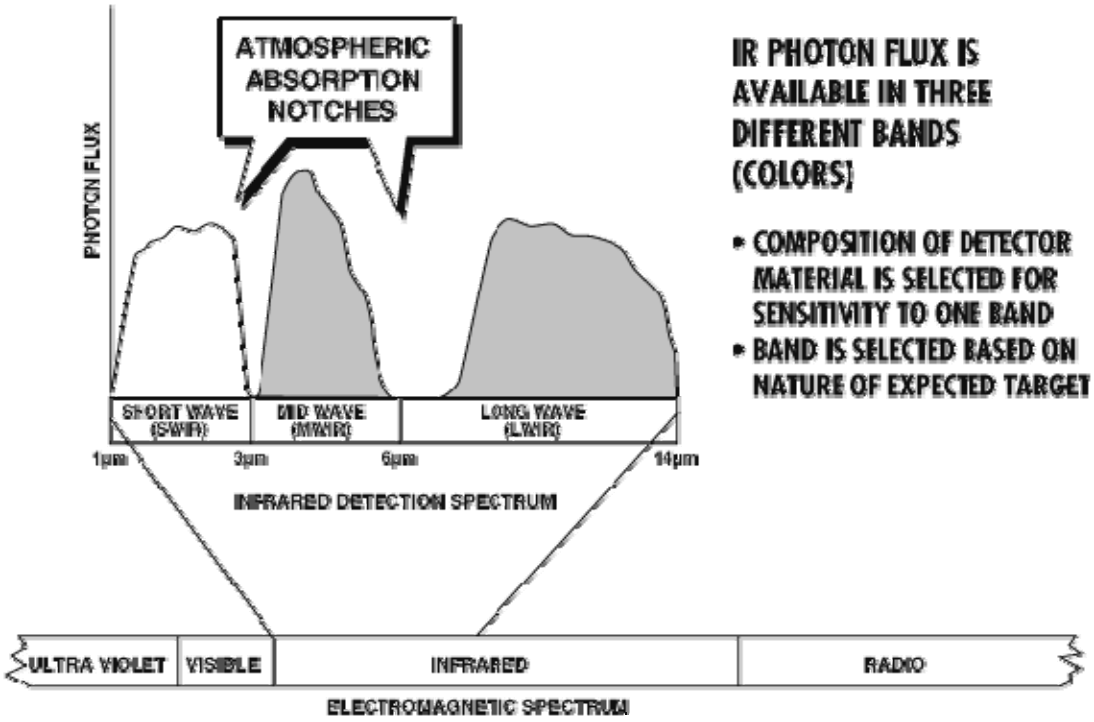


Figure 2.2 IR wavelength bands and characteristics [XEN05]

Figure 2.3 Human scene night vision using conventional camera (left) and IR camera (right) [XEN05]

In photon detectors, photons are converted directly into free current carriers by photoexciting electrons across the energy bandgap of the semiconductor to the conduction band. This effect produces a current, voltage or resistance change on the transducers. The photoexcitation is caused by the sufficiently short wavelength radiation interacting directly with the lattice sites. Therefore, the temperature of the detector must be low enough so that the number of carriers thermally excited across the referred bandgap is negligible. To maintain a low temperature, a cooling system or a dewar is required, which increases the system cost. Generally the sensitivity of photon detectors depends on the energy gap of the semiconductor as well as the optical radiation

wavelength. The following subSection discuss the most commonly used IR radiation sensing structures in arrays, for both energy and photon detectors.

2.1.1. Thermal Detectors

Energy detectors contain two elements, an IR energy absorber and a thermal transducer. Several examples of these sorts of transducers are presented in the next paragraphs.

Thermocouples/Thermopiles

Thermocouples are formed by joining two similar metals which create a voltage at their junction. When a scene is optically focused into a thermocouple, its temperatures increases or decreases as the incident IR flux does, generating a voltage that can be monitored for detection. For sensitive detection, the thermocouple must be thermally insulated from its surroundings, while to obtain a fast response the thermocouple must be able to quickly release build up heat. This trade off between sensitivity and response time is inherent to all thermal detectors.

Pyroelectric Detectors

Pyroelectric detectors consist of special dielectric material with spontaneous and permanent polarization. In the pyroelectric material, the change of dielectric constant is proportional to the temperature dependent spontaneous polarization. When IR radiation is incident and absorbed, the resultant heating makes a change in electrical polarization which causes charges to flow to the connected external read-out circuit. Since the polarization is temperature dependent, a chopper is needed to cut the heat source and reset the polarization condition. The ambient operating temperature and the flat spectral response make the pyroelectric detector useful in some IR imagers. If this dipole can be reversed by the application of an electric field, the material is said to be ferroelectric.

Thermistors/(μ)Bolometers

In thermistors, the resistance of the material varies with temperature. One specific type of thermistor is a bolometer. Unlike photoconductive detectors, the resistance change in bolometer detectors is caused directly by the heating produced by IR radiation on material, instead of photon-lattice interaction and carrier generation. The general structure of bolometer detectors using the micromatching technology (e.g. μbolometers) is shown in Figure 2.4(f). The X-Y metals are used as interconnection tracks and the transistor switch beneath each pixel enables addressing. The application of superconducting materials on bolometer detectors is under development, whereas the dramatic resistance change versus temperature in superconducting materials leads to a high sensitivity on this kind of transducers.

(μ)Cantilevers

(μ)Cantilevers are based on the bimetal effect to measure IR radiation. This effect exploits the difference in thermal expansion coefficients of two different bimetals

to cause a displacement of a (μ)cantilever which, in combination with a reference plate, deflects and alters the equivalent capacitance of the structure.

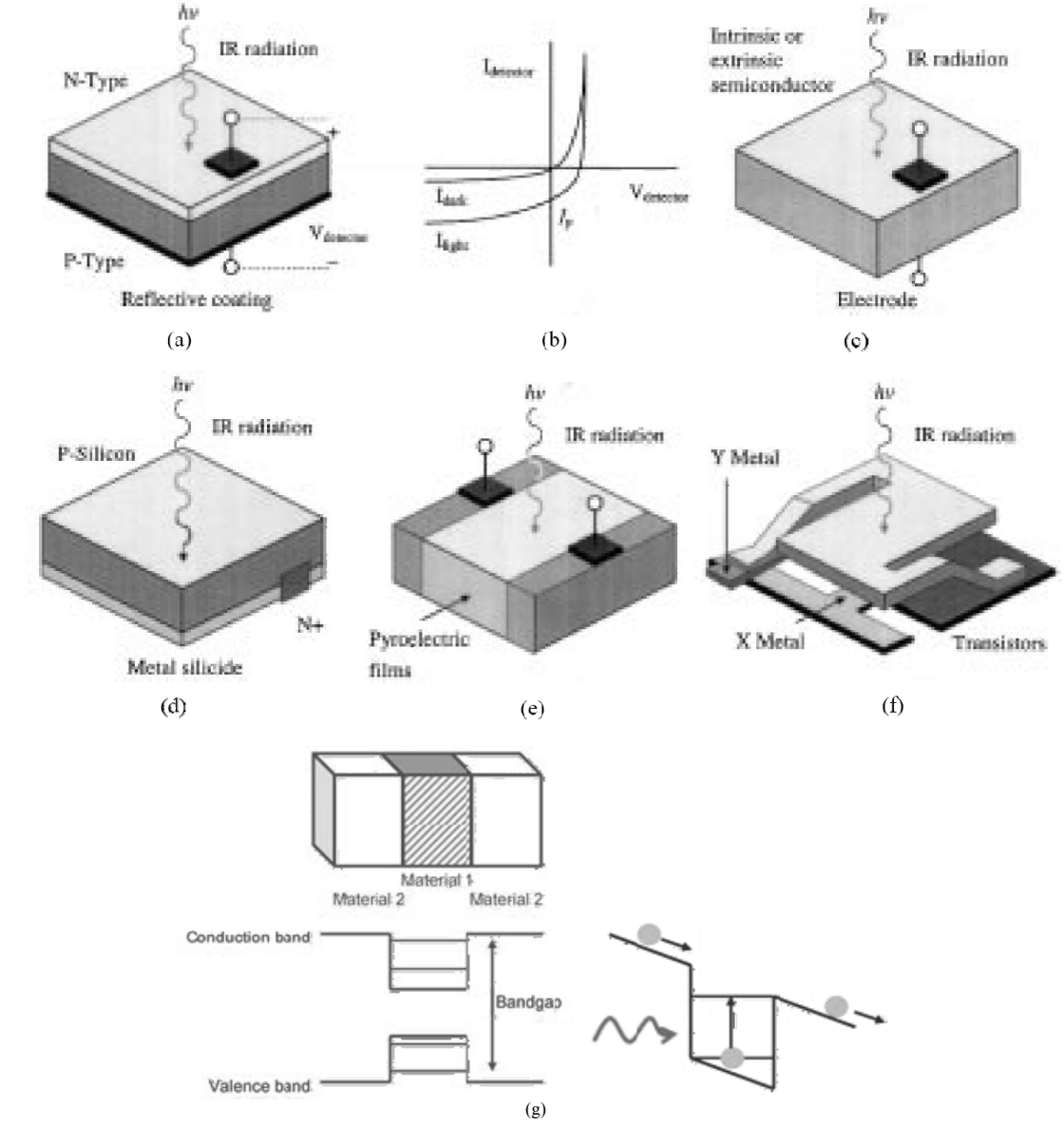


Figure 2.4 Device structure of (a) PV detector, (c) PC detector, (d) Schottky barrier detector, (e) pyroelectric detector, (f) bolometer, (g) QWIP, and (b) I-V curve of PV detector [HSI97]

2.1.2. Photon Detectors

Because these detectors do not function by changing temperature, but by directly interaction with the light, they respond faster than energy detectors. However, they may be cooled to cryogenic temperatures in order to minimize background noise. The following are examples of photon detectors.

PhotoVoltaic (PV) Detectors

The structure of a fotovoltaic (PV) detector is based on a P-N junction device as shown in Figure 2.4(a). The reflective coating on the bottom of the detector provides the double chances (injection and reflection) of photon absorption. Under the IR radiation, the potential barrier of the P-N junction leads to the photovoltaic (PV) effect. An incident photon with the energy greater than the energy band gap of the junction generates e-h pairs and the photocurrent is excited. The resultant I-V curve of the PV detector when exposed to IR radiation is similar to a P-N junction device but shifted downward as shown in Figure 2.4(b). The amount of the photon excited current is denoted by I_p, the photocurrent. Normally, the photovoltaic detector is operated near zero biasing condition to obtain a large output shunt resistance without the device output treat. This resistance is expressed as R_0A (i.e. the shunt resistance normalized to the detector area A under zero bias), and is desirable to be high in order to achieve high sensitivity and good input injection. The zero biasing condition of PV detectors leads to a power consumption near zero, which avoids the heat generation problem.

The thermal and the flicker noise are the major noise sources of the PV detector, degrading the performance of the sensor. Ideal performance of a detector is defined as the Background-limit-IR-performance (BLIP). All other noises in detectors should be kept below the photon noise to achieve the BLIP performance.

PhotoConductive (PC) Detectors

The mechanism of photoconductive (PC) sensors is to produce the conductance change under IR radiation. In PC detectors, the increase of the conductance of photoconductive material under an applied constant dielectric field is caused by the free carriers generated by the photon energy. The structure of PC detectors is shown in Figure 2.4(c). The detector material can be either an intrinsic or an extrinsic semiconductor. The spectral response of a semiconductor material can be controlled by the doping of the intrinsic semiconductor to make PC detectors applicable in LWIR and MWIR radiation. In the case of an intrinsic semiconductor, the incident IR radiation is absorbed to generate holes and electrons. In the case of extrinsic semiconductors, the photon energy is absorbed by the impurity, and only the major carriers are excited. Under the applied constant bias, the resultant current level is proportional to the incident photon flux.

In PC detectors, the photoconductive gain is defined as the ratio of carrier lifetime to detector transit time, and usually varies from 0.5 to greater than unity. Since the current flows under a constant dielectric field, the photoconductive detector consumes power and generates heat. This makes it not suitable for large IR array applications. Moreover, an additional noise source called generation-recombination noise exists in PC detectors besides the thermal and flicker noises.

Photo-Emissive/Schottky-Barrier Detectors

The structure of this type of sensors with the silicide (PtSi) thin film which can be fabricated by using the traditional CMOS process is shown in Figure 2.4(d). The IR

radiation photons injected from the backside of the silicon substrate are absorbed in the silicide layer. The accumulated charges can be transferred out through a structure like a charge-coupled-device (CCD). Due to process compatibility of schottky barrier detector with CMOS, it is easy to merge detector arrays with read-out circuits and other circuits monolithically. The problems of bonding and hybrid process can be solved in high-density IR FPA applications. However, low quantum efficiency and slow spectral response limit the application of Schottky barrier detectors on the MWIR imagers.

Quantum Well Infrared Photodetector (QWIP)

The Quantum Well Infrared Photodetector (QWIP) is an infrared detector that consists of multiple alternating thin gallium arsenide (GaAs) and aluminum gallium arsenide (AlGaAs) layers (Figure 2.4(g)). Carriers are generated by absorption of IR light inside quantum wells. Thus, the energy band level (i.e. the wavelength absorption band) depends on the well width, whereas the amount of generated photocurrent relies mainly on the potential barriers width and the number of wells.

As an overview, the Table 2.1 summarizes the main detector types and materials of IR detectors:

Photon Detectors		Energy Detectors	
Intrinsic, PV	- MCT - Si, Ge - InGaAs - InSb, InAsSb	**Bolometers**	- Vanadium Oxide (V_2O_5) - Poly-SiGe - Poly-Si - Amorph Si
Intrinsic, PC	- MCT - PbS, PbSe	**Thermopiles**	- Bi/Sb
Extrinsic	- SiX	**Pyroelectric**	- Lithium Tantalite (LiTa) - Lead Zirconium Titanite (PbZT)
Photo-emissive	- PtSi	**Ferroelectric**	- Barium Strontium Titanite (BST)
QWIP	- GaAs/AlGaAs	**Microcantilever**	- Bimetals

Table 2.1 Overview of IR detector types and materials

Many of these IR materials are based on compound semiconductors made of III-V elements such as indium, gallium, arsenic, antimony, or on the II-VI elements mercury, cadmium and telluride, or on the IV-VI elements lead, sulfur and selenide. They can be combined into binary compounds such as GaAs, InSb, PbS and PbSe or into ternaries such as InGaAs or HgCdTe.

2.1.3. The PbSe Detector

A novel, low density technology of polycrystalline PbSe [VER07] is used on the present work. This technology has been developed for uncooled MWIR FPAs, where the PbSe is deposited, processed and sensitized, by specific thermal treatments, on a

silicon substrate with two levels of metal separated by a thin dielectric layer of SiO_2. The use of polycrystalline lead salt PC detectors is proved to result on high performance/cost ratios. These ratios are still better than other related uncooled FPA technologies, such as the previously described thermal detectors (µbolometers, ferroelectrics), overcoming their traditional long response time and low detectivity drawbacks, in the photonic field, without neither the use of expensive hemispherical/hyperhemispherical lenses nor non-equilibrium-mode detectors.

Chalcogenide salt arrays have, although, two main drawbacks: their high dielectric constant, which results in a high diode capacitance, and their high thermal expansion coefficients, due to the crystalline character of the material grown, that leads to the appearance of significant dark current. The chosen polycrystalline structures take advantage of the naturally formed intergrain potential barriers to reduce generation-recombination effects on the dark current, showing good performance at room temperature. Moreover, the new method for processing the presented detector, based on a Vapor Phase Deposition (VPD), yields to a manufacturing process optimized and adapted to high volume requirements, with a considerable unitary cost reduction.

Contact layout for detector biasing is shown in Figure 2.5; interdigitation is maximized through a straight metallic structure, so as to reduce its equivalent internal resistance. Such a structure implies notorious capacity between both polarization nodes.

Electrical Modeling

In order to obtain an estimate value for the referred parasitic capacitance the software FastCap is employed. FastCap is a free, electrostatic solver tool optimized for conductor-dielectric and dielectric-dielectric surface structures, as seen in Figure 2.6. Moreover, an infrared detector model has been developed to obtain a practical and flexible circuit, taking into account the main non-idealities of the PbSe sensor. This circuit will be used in the design methodology of the ROIC, and will consider not only the optical responsivity (R_{opt}), as a function of the sensor current (I_{sens}) with the incident light power (P_{in}), but also:

Dark current: Even under no illumination conditions, but non-cryogenic temperature, the sensor presents a certain value of dark current that can be represented, with no thermal drift, as a DC component (I_{dark}) independent from the IR illumination. As the measured ratio between the offset and the effective current is relatively high (µA/nA), it is strongly desirable to obtain a fine model for this phenomena.

Noise: This stochastic process is present in all physical devices, and must be modeled as a thermal, white noise or as a flicker, pink component depending on the frequency operation.

Non-lineal output resistance: Even under constant IR radiation, there is I_{sens} dependence on the differential voltage applied to the detector (V_{sens}). This finite resistance effect can also behave as a non-lineal device. Thus, a conductance curve $I_{sens}=g(V_{sens})$ is used.

Output capacitance: As its own name suggests, this electric component (C_{sens}) characterizes the I_{sens}-V_{sens} dynamics.

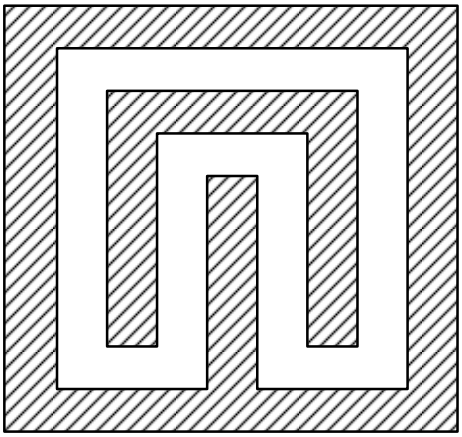


Figure 2.5 PbSe biasing contacts layout

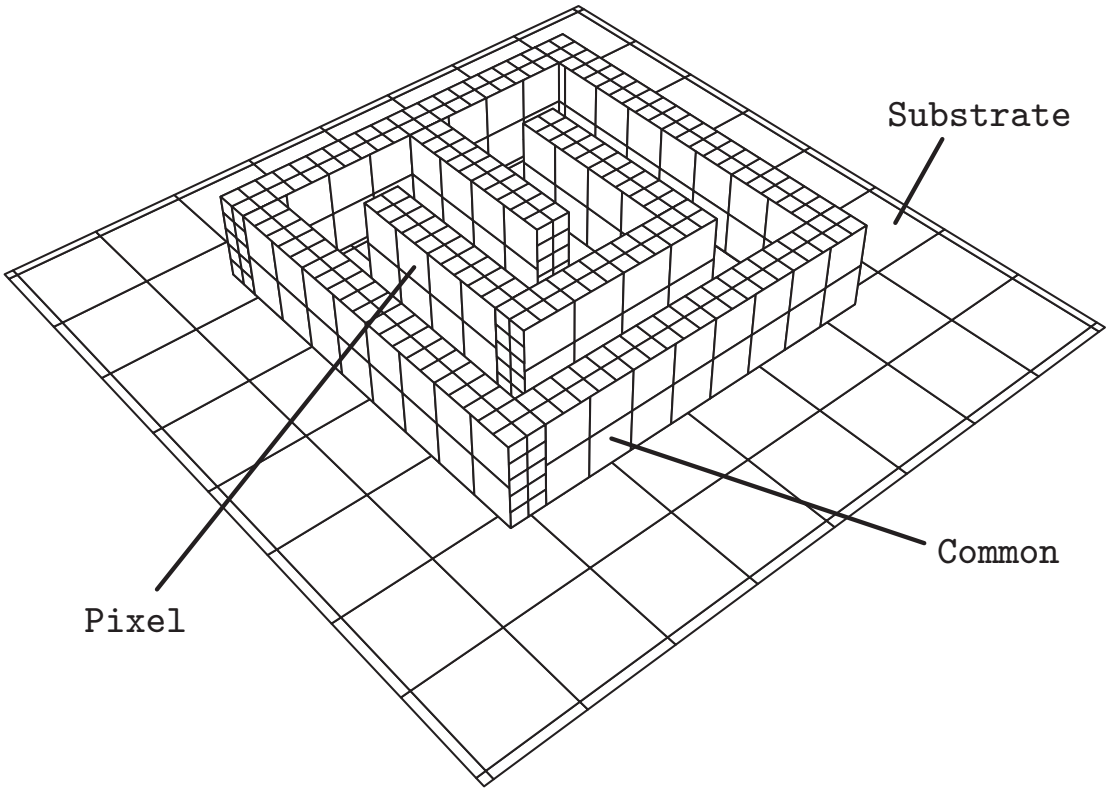


Figure 2.6 PbSe sensor FastCap analysis example

Based on the previous detector parameters, an equivalent circuit is proposed for global system simulation. Its key features are:

- ✓ Inclusion of all the effects previously related
- ✓ SPICE language compatibility
- ✓ Easily-configurable detector variables
- ✓ Direct tuning based on experimental characterization

The result is shown in Figure 2.7, where I_{gen} is the photogenerated current, R_{neq} is the equivalent noise resistance, f_c is the flicker noise corner frequency, $\bar{g}$ is the normalized output conductance and C_{out} is the output capacitance.

The suggested model is made of two main subcircuits, referred to the current generation (e.g. dark and noise currents) and to the output port (e.g. non-lineal resistance and capacitance). Concerning first Section, R_{neq} is also used for I_{dark} generation, creating noise dependence on current biasing. The second part of the circuit is composed of an output resistance, as a function of I_{gen}, ensuring no I_{sens} under zero V_{sens} condition.

SPICE implementation of Figure 2.7 is made through the schematic of Figure 2.8, where each component function can be easily recognized.

The model use also two additional files:

sens_Rneq: R_noise resistance model in which frequency power density (PSD) and thermal component ($\frac{\partial I_{nth}^{\ 2}}{\partial f}$) and flicker frequency corner, f_c, ($\frac{\partial I_{nfk}^{\ 2}}{\partial f}$) parameters are included:

$$\frac{\partial I_{nth}^{\ 2}}{\partial f} = \frac{4KT}{R_{neq}} = \frac{4KT}{R_n}\frac{W}{L}$$
$$\frac{\partial I_{nfk}^{\ 2}}{\partial f} = \frac{K_F I_{dark}^{\ 2}}{WL}\frac{1}{f} \qquad \textbf{(2.1)}$$
$$f_c = \frac{K_F I_{dark}^{\ 2}}{W^2}\frac{R_n}{4qU_t}$$

Where W, L, and R_n are the width, length and square resistivity of the equivalent resistance, respectively, whereas K_f is the flicker constant.

sens_Rout: Normalized output conductance ($\bar{g}$) table. Such a format allows to directly including experimental curves.

Figure 2.9 and Figure 2.10 depict electrical simulation examples of both PSD noise and DC resistance with $\frac{\partial I_{nth}}{\sqrt{\partial f}} = 1\frac{pArms}{\sqrt{Hz}}$ and $f_c = 1KHz$.

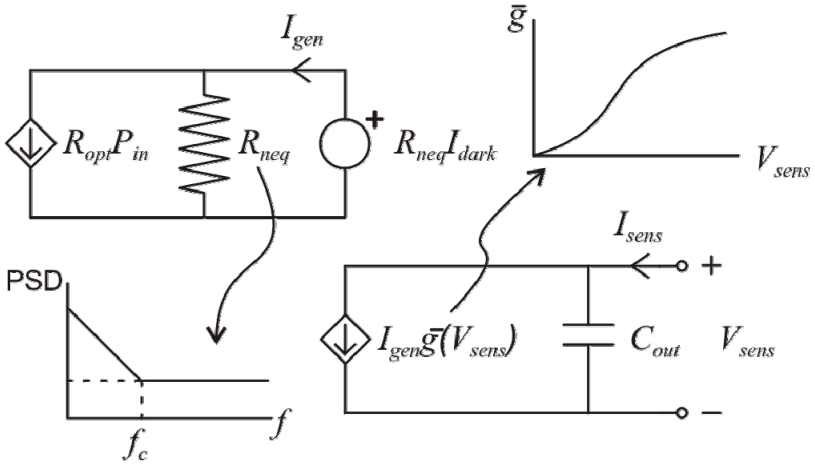


Figure 2.7 Equivalent PbSe detector circuit

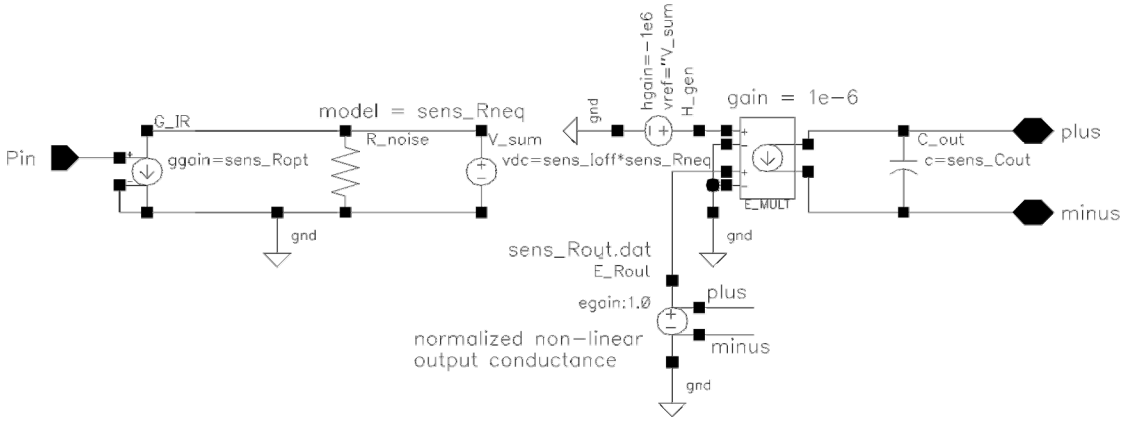


Figure 2.8 Equivalent PbSe detector schematic

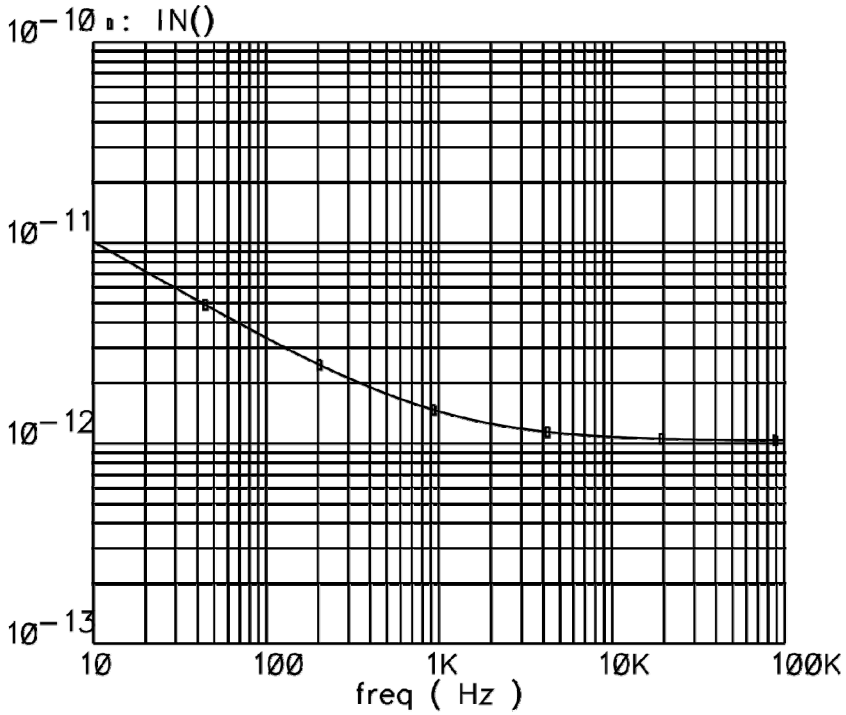


Figure 2.9 PSD output noise electrical simulation result example

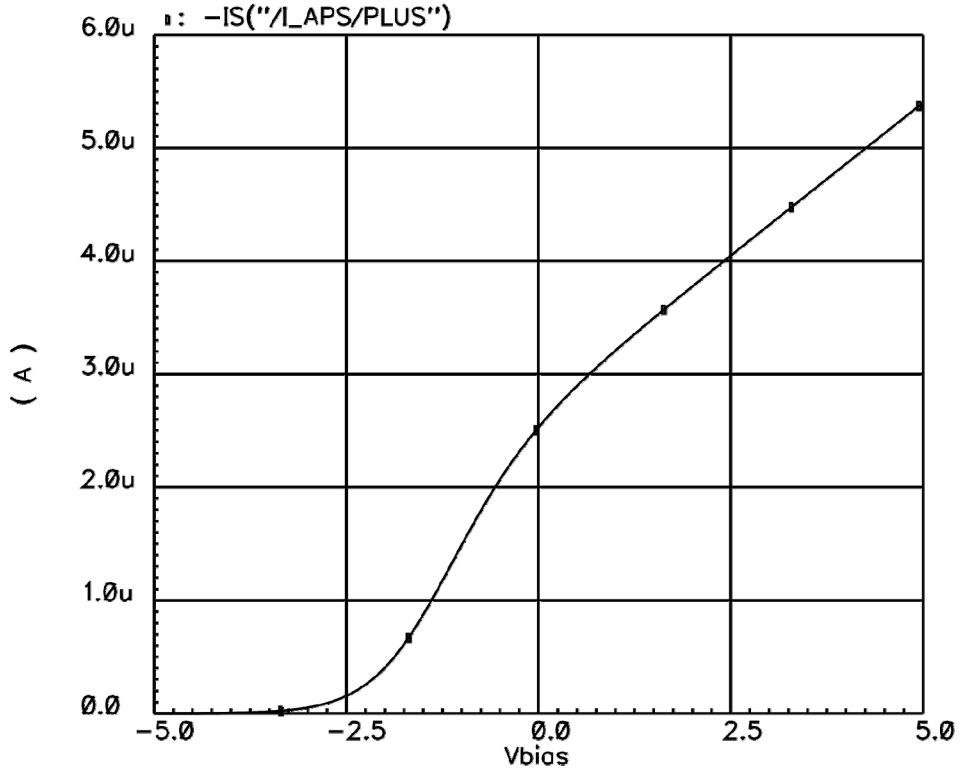


Figure 2.10 DC output resistance electrical simulation result example

2.2. The MOSFET

Even though conventional modeling of MOSFET transistors is widely known by electronic engineers, the present chapter cannot be finished without presenting an analytical, simple model for the design synthesis procedure. If the designer has no access to a simple set of device equations to operate mathematically with them in a friendly way, the analog design becomes a kind of try-and-error procedure between hand work and numerical simulation, which is largely time-consuming and does not return any optimum circuit topology.

Since the analog topologies researched in this work will operate the MOS devices mainly in the subthreshold region, the accuracy and ease-of-use of the EKV model [EKV95] suggest there is no better analytical way for the design work here presented. Thus, all CMOS circuits presented in the thesis are conceived using this model, here presented under the bibliographic interpretation [SER04]. The following characteristics convert EKV to a model reference:

- ✓ **All** nodal **voltages** are **referred to** the **bulk**, instead of using classical common source structures. In this way, more powerful expressions are obtained for non-grounded terminal devices.
- ✓ The MOSFET is considered as a **bidirectional device**, due to its physical symmetry.
- ✓ A **single expression** is used, mathematically simple and valid for all regions. The asymptotic behavior of this model in each particular region match with the range limited equations of classical models.
- ✓ All expressions have **continuous** first derivatives around all the boundaries of the different regions of operation, which avoid discontinuity in any small signal parameter.

In this sense, all the equations that will be described are based on the nomenclature of the MOS device shown in Figure 2.11 where I_D is the drain current, and V_{DB}, V_{GB} and V_{SB} are the drain-to-bulk, gate-to-bulk and source-to-bulk voltage, respectively.

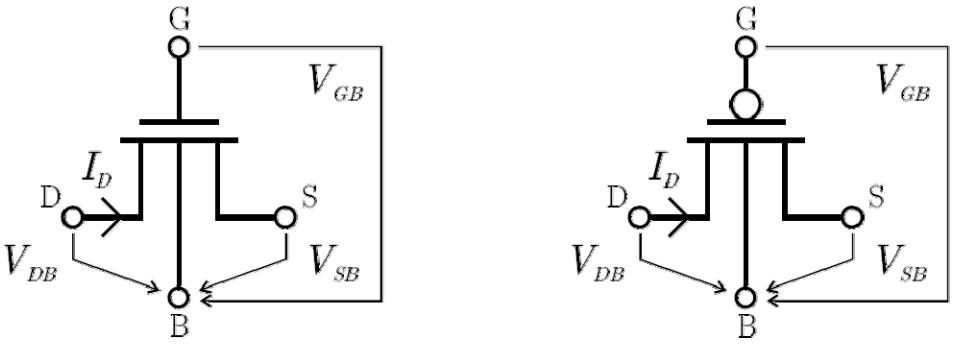


Figure 2.11 Basic nomenclature for NMOS (left) and PMOS (right)

2.2.1. Large Signal Equations

In order to avoid redundant formulation, only NMOS equations will be described, and the PMOS case can be directly obtained supposing opposite sign in the threshold voltage and the following symmetry:

$$I_D(V_{GB},V_{SB},V_{DB})\big|_{PMOS} \equiv -I_D(-V_{GB},-V_{SB},-V_{DB})\big|_{NMOS} \quad \textbf{(2.2)}$$

DC Drain Current

One of the most interesting design circuit equations relates drain current dependence on every single transistor nodal voltage. The total current I_D can be understood as the sum of two opposite components, forward (I_{DF}) which depends on (V_{GB}, V_{SB}), and reverse (I_{DR}), which depends on the (V_{GB},V_{DB}).

$$I_D = I_{DF} - I_{DR} = I_S\left[\mathrm{F}\left(\frac{V_P - V_{SB}}{U_T}\right) - \mathrm{F}\left(\frac{V_P - V_{DB}}{U_T}\right)\right] \quad \textbf{(2.3)}$$

$$\text{considering} \quad V_P = \frac{V_{GB} - V_{TO}}{n} \quad \textbf{(2.4)}$$

$$\text{and} \quad I_S = 2n\beta U_T{}^2 = 2n\mu C_{OX}\frac{W}{L}U_T{}^2 \quad \textbf{(2.5)}$$

Where V_P is the pinch-off voltage and V_{TO} is the threshold voltage, while I_S, n, β and U_t are the specific current, the subthreshold slope, the current factor for a specific W/L ratio and the thermal potential (25 mV at room temperature).

F must be a continuous function, valid for all MOS operating regions. In this sense, EKV suggests the following expression:

$$\mathrm{y} = \mathrm{F}(x) = \ln^2\left(1 + e^{x/2}\right) = \begin{cases} e^x & \text{si } x \ll 0 \\ \left(\frac{x}{2}\right)^2 & \text{si } x \gg 0 \end{cases} \quad \textbf{(2.6)}$$

Thus, the drain current can be now expressed as:

$$I_D = I_S\left[\ln^2\left(1 + e^{\frac{V_{GB} - V_{TO} - nV_{SB}}{2nU_t}}\right) - \ln^2\left(1 + e^{\frac{V_{GB} - V_{TO} - nV_{DB}}{2nU_t}}\right)\right] \quad \textbf{(2.7)}$$

Approximate expressions for each single region can be obtained if expression (2.6) is applied. Table 2.2 contains I_D expressions for all known transistor operation regions: weak, moderate and strong inversion, with both components contribution (conduction), only forward (forward saturation) or reverse contribution (reverse saturation). Figure 2.12 shows operation region vs. a specific terminal voltage.

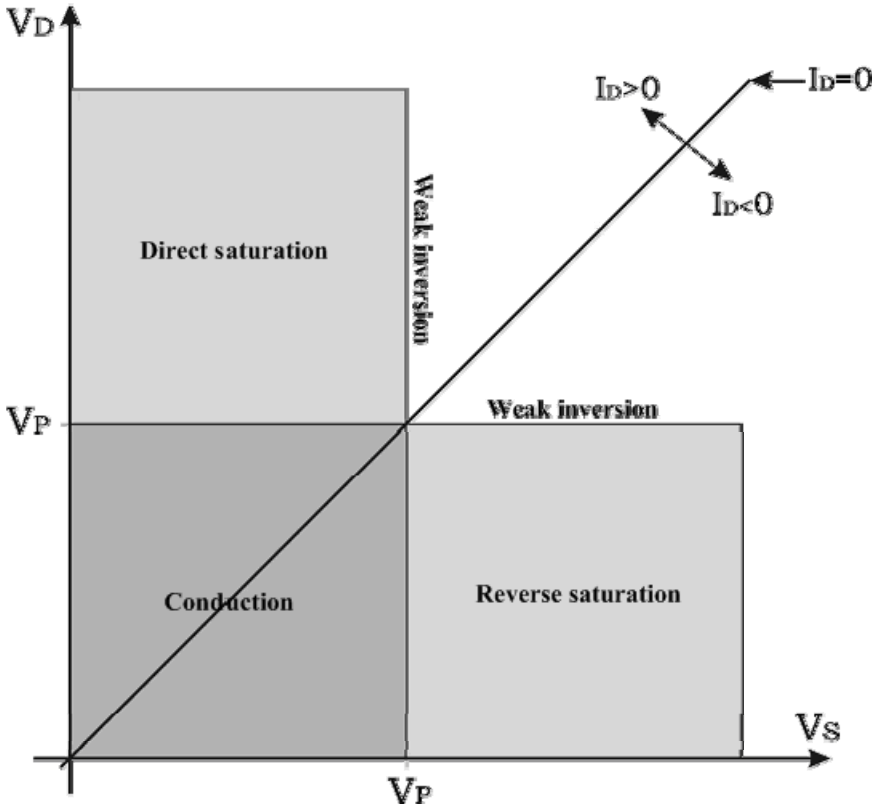


Figure 2.12 Transistor operation regions versus pinch-off voltage

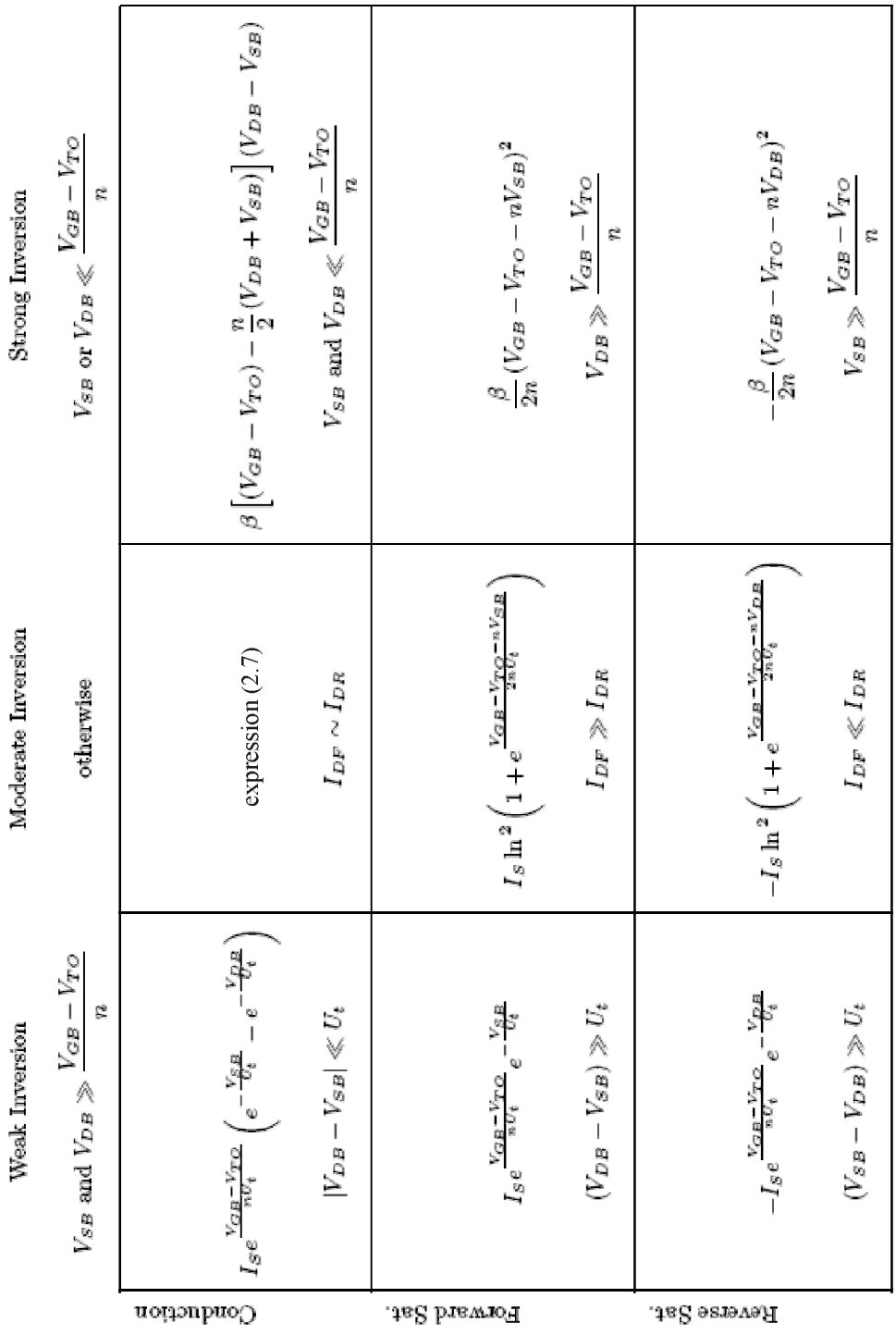


Table 2.2 Large signal DC equations of EKV model

The major advantage of F function remains on continuity between strong and weak inversion regimes, along the moderate inversion region. It can be seen in Figure 2.13 that the latter coincides with the non-dominant asymptote zone. In this sense, the inversion coefficient (i.e. IC) is defined as:

$$IC = \frac{I_D}{I_S} \tag{2.8}$$

IC is an easy way to locate the MOS operation region without the necessity of any terminal voltage reference. Figure 2.13 fixes a moderate inversion region of about one decade around 0 dB or, in other words:

IC	Region
> 10	Strong Inversion
~ 1	Moderate Inversion
< 0.1	Weak Inversion

Table 2.3 IC versus inversion region

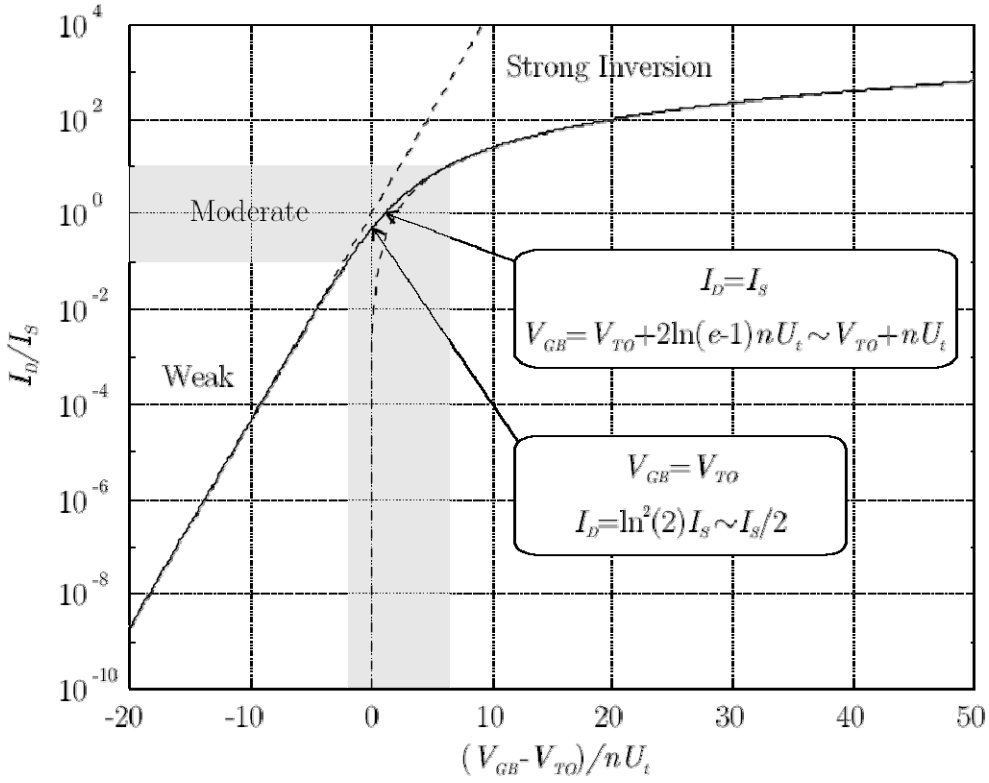


Figure 2.13 Normalized drain current versus V_p in forward saturation and V_{SB}=0V. Dashed lines indicate the asymptotic approximations of Table 2.2

Quasi-Static Capacitances

The static I/V description presented until now does not consider MOSFET dynamics. The capacitive model appears as a way to predict the transitory behavior of the device, and is shown in Figure 2.14 where transcapacitances are defined as follows:

$$C_{GS} \doteq \left.\frac{\partial Q_G}{\partial V_{SB}}\right|_{V_{GB0},V_{DB0}} \quad C_{GD} \doteq \left.\frac{\partial Q_G}{\partial V_{DB}}\right|_{V_{GB0},V_{SB0}} \quad C_{GB} \doteq \left.\frac{\partial Q_G}{\partial V_{GB}}\right|_{V_{GS0},V_{GD0}} \tag{2.9}$$

$$C_{BS} \doteq \left.\frac{\partial Q_B}{\partial V_{SB}}\right|_{V_{GB0},V_{DB0}} \quad C_{DB} \doteq \left.\frac{\partial Q_B}{\partial V_{DB}}\right|_{V_{GB0},V_{SB0}} \tag{2.10}$$

where Q stands for charge.

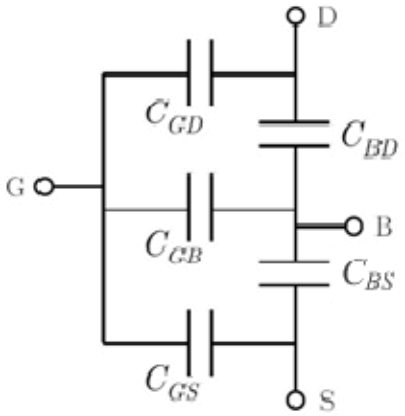


Figure 2.14 Simplified capacitive model of MOS

In general, all above elements are not reciprocal due to MOS device asymmetries. It is possible to establish, anyway, some inter-capacitance relation:

$$C_{BD} \equiv (n-1)C_{GD}C_{BS} \equiv (n-1)C_{GS} \tag{2.11}$$

Hence, only three transcapacitances are needed to predict charge evolution over the time. Expressions for all regions of operation are depicted below from the EKV model:

$$C_{GD} = C_{ox}\left[\frac{1}{\frac{2}{3}\left(1-\frac{IC_F}{\left(\sqrt{IC_F}+\sqrt{IC_R}\right)^2}\right)}+\frac{1}{\sqrt{IC_R}\left(1-e^{-\sqrt{IC_R}}\right)}\right]^{-1} \tag{2.12}$$

$$C_{GB} = C_{ox}\frac{n-1}{n}\left[1-\left[\frac{1}{\frac{2}{3}\left(1+2\frac{\sqrt{IC_F IC_R}}{\left(\sqrt{IC_F}+\sqrt{IC_R}\right)^2}\right)}+\frac{1}{\sqrt{IC_F}\left(1-e^{-\sqrt{IC_F}}\right)+\sqrt{IC_R}\left(1-e^{-\sqrt{IC_R}}\right)}\right]^{-1}\right] \quad \textbf{(2.13)}$$

$$C_{GS} = C_{ox}\left[\frac{1}{\frac{2}{3}\left(1-\frac{IC_R}{\left(\sqrt{IC_F}+\sqrt{IC_R}\right)^2}\right)}+\frac{1}{\sqrt{IC_F}\left(1-e^{-\sqrt{IC_F}}\right)}\right]^{-1} \quad \textbf{(2.14)}$$

where C_{ox} is the oxide gate capacitance and IC_F, IC_R are the forward and reverse inversion coefficients, respectively

$$IC_F = \frac{I_F}{I_S} \quad IC_R = \frac{I_R}{I_S} \quad \textbf{(2.15)}$$

Figure 2.15 illustrates normalized transcapacitance dependence on the pinch-off voltage.

2.2.2. Small Signal Parameters

The small signal model consists of the main set of transconductances shown in Figure 2.15. The definition comes from the linear incremental model:

$$g_{mg} \doteq \left.\frac{\partial I_D}{\partial V_{GB}}\right|_{V_{SB0},V_{DB0}} \quad g_{ms} \doteq \left.\frac{\partial I_D}{\partial V_{SB}}\right|_{V_{GB0},V_{DB0}} \quad g_{md} \doteq \left.\frac{\partial I_D}{\partial V_{DB}}\right|_{V_{GB0},V_{SB0}} \quad \textbf{(2.16)}$$

where transconductances are referred to the bulk terminal instead of to the source. The equivalences with the classical common source models can be easily obtained:

$$\begin{aligned} g_m &= \left.\frac{\partial I_D}{\partial V_{GS}}\right|_{V_{BS0},V_{DS0}} \equiv g_{mg} \\ g_{mb} &= \left.\frac{\partial I_D}{\partial V_{BS}}\right|_{V_{GS0},V_{DS0}} \equiv g_{ms} - g_{mg} - g_{md} \\ g_{ds} &= \left.\frac{\partial I_D}{\partial V_{DB}}\right|_{V_{GS0},V_{BS0}} \equiv g_{md} \end{aligned} \quad \textbf{(2.17)}$$

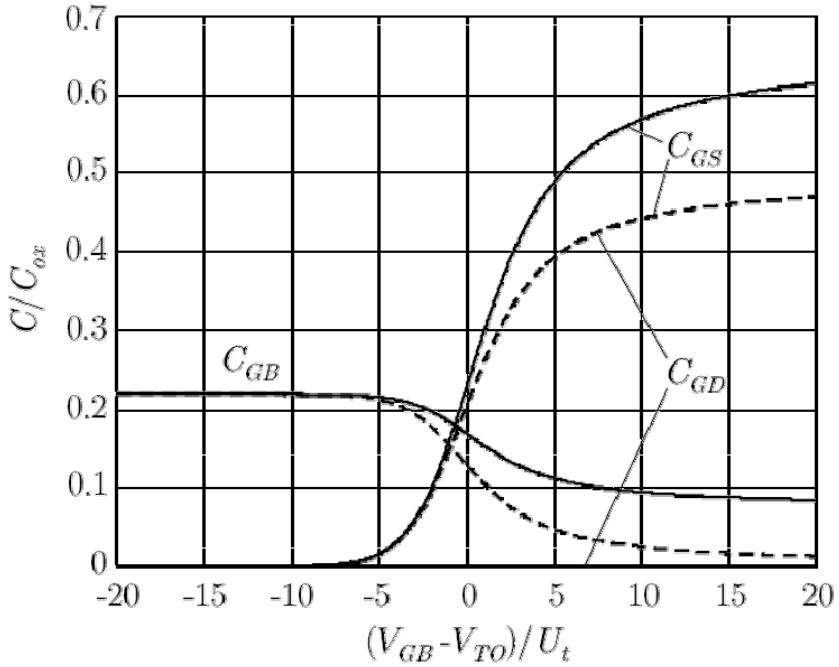


Figure 2.15 Normalized MOS transcapacitances in conduction (dashed) and forward saturation (solid) for n=1.3

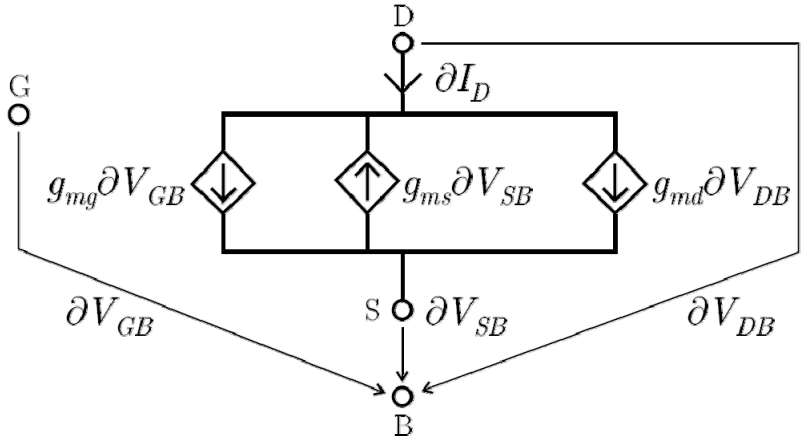


Figure 2.16 MOS small-signal equivalent circuit

Table 2.4 contains expressions for all parameters of each operation region, obtained from the general formula (2.7).

g_{mg}	Weak I.	Moderate I.	Strong I.
Conduction	$\frac{I_D}{nU_t}$	$\sqrt{\frac{2\beta}{n}}\left[\sqrt{I_{DF}}\left(1-e^{-\sqrt{IC_F}}\right)-\sqrt{I_{DR}}\left(1-e^{-\sqrt{IC_R}}\right)\right]$	$\beta\left(V_{DB}-V_{SB}\right)$
Direct sat	$\frac{I_D}{nU_t}$	$\sqrt{\frac{2\beta I_D}{n}}\left(1-e^{-\sqrt{IC}}\right)$	$\sqrt{\frac{2\beta I_D}{n}}$
Reverse sat	$\frac{I_D}{nU_t}$	$-\sqrt{\frac{2\beta\lvert I_D\rvert}{n}}\left(1-e^{-\sqrt{IC}}\right)$	$-\sqrt{\frac{2\beta\lvert I_D\rvert}{n}}$

g_{ms}	Weak I.	Moderate I.	Strong I.
Conduction	$\frac{I_{DF}}{U_t}$	$\sqrt{2n\beta I_{DF}}\left(1-e^{-\sqrt{IC_F}}\right)$	$\sqrt{2n\beta I_{DF}}$
Direct sat	$\frac{I_D}{U_t}$	$\sqrt{2n\beta I_D}\left(1-e^{-\sqrt{IC}}\right)$	$\sqrt{2n\beta I_D}$
Reverse sat	$\simeq 0$ (λI_D)	$\simeq 0\ (\lambda I_D)$	$\simeq 0\ (\lambda I_D)$

g_{md}	Weak I.	Moderate I.	Strong I.
Conduction	$\frac{I_{DR}}{U_t}$	$\sqrt{2n\beta I_{DF}}\left(1-e^{-\sqrt{IC_F}}\right)$	$\sqrt{2n\beta I_{DF}}$
Direct sat	$\simeq 0\ (\lambda I_D)$	$\simeq 0\ (\lambda I_D)$	$\simeq 0\ (\lambda I_D)$
Reverse sat	$-\frac{I_D}{U_t}$	$-\sqrt{2n\beta\lvert I_D\rvert}\left(1-e^{-\sqrt{IC}}\right)$	$-\sqrt{2n\beta\lvert I_D\rvert}$

Table 2.4 Transconductances versus MOSFET operational region boundaries. I. stands for inversion

From the given results, continuity of all these parameters along the different regions is ensured by the asymptotic equation in (2.6). For g_{mg} the valid expression for all regions is, for example:

$$\frac{g_{mg}}{I_D}=\frac{1}{nU_t}\left(\frac{1-e^{-\sqrt{IC}}}{\sqrt{IC}}\right) \qquad \textbf{(2.18)}$$

as seen in Figure 2.17.

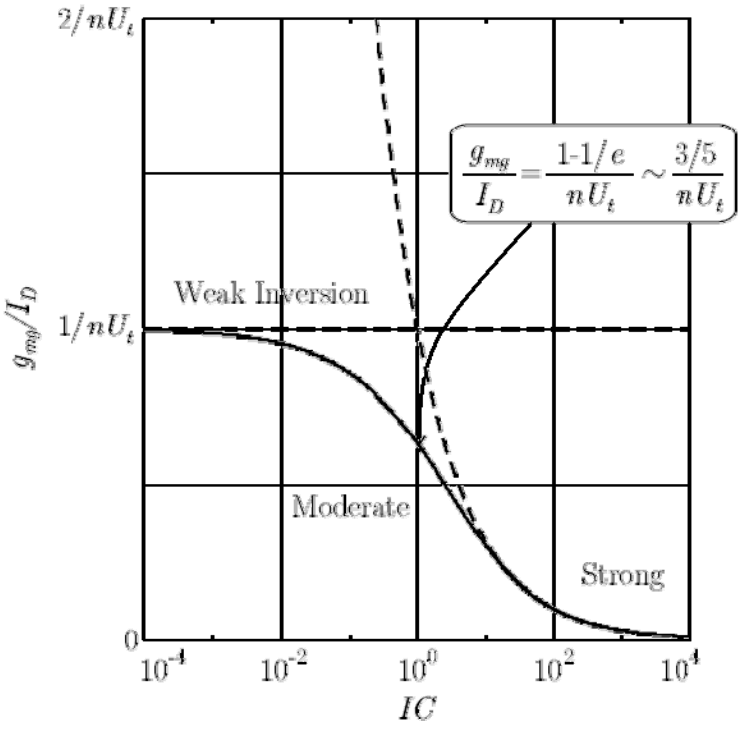


Figure 2.17 Normalized g_{mg} parameter versus the Inversion Coefficient in forward saturation. Dashed lines indicate the asymptotic approximations of Table 2.2

2.2.3. Noise Equations

A small signal and spectral model is chosen for the intrinsic noisy phenomena of the MOS transistor. Due to their random nature, the equivalent noise sources are described in terms of power spectral densities (PSD). The main expressions are again derived from the EKV model, although they have been rewritten here as equivalent parallel current sources between drain and source terminals. This nomenclature facilitates dynamic range and signal-to-noise studies in the current domain.

Two different types of noise are considered for the MOS device: Thermal, caused by the random motion of electrons across the conductor, and flicker, originated by fluctuations in the conductivity of imperfect junctions, i.e. the interface between the gate oxide and the silicon substrate in a MOSFET.

The thermal component exhibits a flat or white PSD proportional to the total charge stored in the channel:

$$\frac{\mathrm{d}I_{DNth}^{\ 2}}{\mathrm{d}f} = 4KTg_{ms}K_{th} \qquad \textbf{(2.19)}$$

where:

$$K_{th} \doteq \frac{1}{1+IC_F}\left(\frac{1+\frac{IC_R}{IC_F}}{2}+\frac{2}{3}IC_F\frac{1+\sqrt{\frac{IC_R}{IC_F}}+\frac{IC_R}{IC_F}}{1+\sqrt{\frac{IC_R}{IC_F}}}\right) \qquad \textbf{(2.20)}$$

is the thermal factor, while I_{CF} and I_{CR} stand for the forward and reverse Inversion Coefficients respectively. The equivalent noise transconductance is interpolated through the different regions of operation via K_{th} as listed in Table 2.5. Reverse saturation has been omitted due to its full duality to the forward case.

K_{th}	Weak I.	Moderate I.	Strong I.
Conduction	1	1	1
Forward sat.	$\frac{1}{2}$	$\frac{3+4IC}{6+6IC}$	$\frac{2}{3}$

Table 2.5 Thermal factor (Kth) versus region of operation

On the other hand, flicker noise exhibits a 1/f or pink PSD in terms of equivalent gate voltage.

$$\frac{\mathrm{d}V_{GBNfk}^{\ 2}}{\mathrm{d}f}=\frac{K_{fk}}{WL}\frac{1}{f} \qquad \textbf{(2.21)}$$

where K_{fk} stands for the flicker factor, with a strong technological dependence (up to 2 orders of magnitude between complementary devices $K_{fkNMOS} \sim 10^2 K_{fkPMOS}$, but very little sensitivity respect to the drain current. Finally, the total noise drain current can be computed as the root-sum-square of the thermal and flicker components, provided these two phenomena are not correlated:

$$\frac{\mathrm{d}I_{DN}^{\ 2}}{\mathrm{d}f}=\frac{\mathrm{d}I_{DNth}^{\ 2}}{\mathrm{d}f}+\frac{\mathrm{d}I_{DNfk}^{\ 2}}{\mathrm{d}f}=4KTg_{ms}K_{th}+g_{mg}^{\ 2}\frac{K_{fk}}{WL}\frac{1}{f} \qquad \textbf{(2.22)}$$

The dominant range for each noise component is of particular interest when compared to the signal bandwidth, since it can help to select between different circuit strategies. In this sense, the noise corner frequency (f_{CN}) is defined here as the boundary between thermal and flicker spectral regions (i.e. $dI_{DNth}^{\ 2}/df \equiv I_{DNfk}^{\ 2}/df$):

$$f_{CN} \doteq \frac{g_{mg}^{\ 2}}{g_{ms}} \frac{K_{fk}}{K_{th}} \frac{1}{4KTWL} \qquad \textbf{(2.23)}$$

2.2.4. Technology Mismatch Model

Physical implementation of real integrated MOSFET devices manifest non deterministic variations of their electrical properties that are not usually considered in standard simulation models. These time-invariant dispersions are caused by mismatching originated mainly during the manufacturing process. While these effects may not be critical in digital designs, they play an important role in the practical dimensioning of MOS devices for analog circuit techniques based on matching ratios, like the case of this work As a result, an stochastic model needs to be added to reflect the statistic behavior.

Only transistor-level technology mismatching is covered here, that is differences between two identically sized MOS transistors of the same integrated circuit. Process spread at batch and run levels are usually covered by the corner.

For a general parameter (P), two types of variations (ΔP) are observed:

- ✓ **Local** variations with correlation distances comparable to device dimensions. Commonly caused by non-uniform distributions of implanted, diffused or substrate ions, local mobility fluctuations, granular oxide and trapped charges in oxide. They can be fitted to a spatial zero mean distribution.

- ✓ **Global** variations when correlation distances are larger than practical device geometries. In this case, the origin can be found in the wafer fabrication and oxidation process. Normal probabilistic distributions are also used to model this type of variations.

Under the assumption of non-correlation, the total deviation of ΔP is the root-sum-square of all contributions. A well accepted model for CMOS technologies is formulated as:

$$\sigma^2(\Delta P) = \frac{A_P^{\ 2}}{WL} + B_P^{\ 2} D \simeq \frac{A_P^{\ 2}}{WL} \qquad \textbf{(2.24)}$$

where A_P and B_P stand for the mismatching parameters of local and global variations respectively. While the first component depends only on the device area (WL), the latter is related to the distance (D) between the two matched MOS transistors. The above equation does not take into account other important aspects of the layout such as device parameters, substrate orientation, surrounding layers and thermal gradients. Hence, in order to avoid further geometrical variables, the practical recommendations compiled in Table 2.6 are supposed to be used in the physical design.

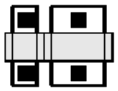
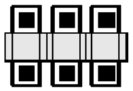
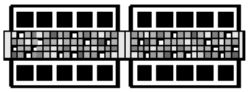
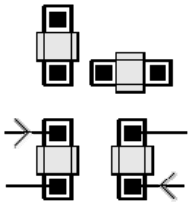
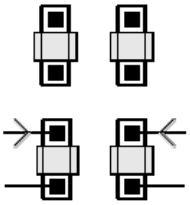
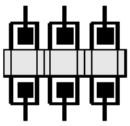
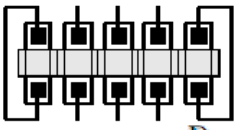
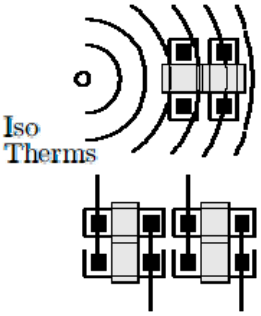
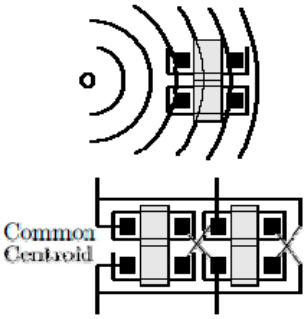
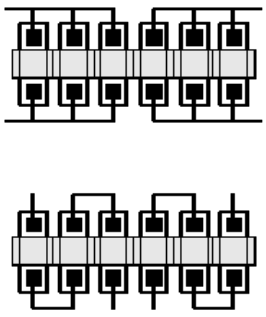
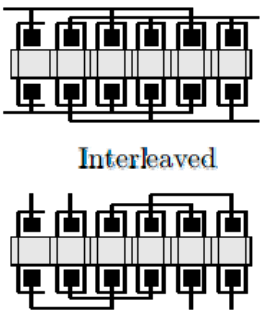
Layout Rule	Bad	Good
Unitary Elements		
Large Area	 Process Resolution	
Same Orientation		
Minimum Distance		
Same Surround		 Dummy Dummy
Same Symmetry	 Iso Therms	 Common Centroid
$(W/L)\gg 1$ Examples $(W/L)\ll 1$		 Interleaved

Table 2.6 General layout recommendations for CMOS device matching

of the analog circuit. In fact, the contributions of global variations can be strongly reduced by minimizing the distance D down to the lithography limits specified in the design rules of the CMOS process. As a result, the total deviation of ΔP can be simplified according to (2.24).

The electrical parameters usually modeled are β and V_{TO}. Also in the context of this work, the mismatch of the drain current is of particular importance when designing the final dimensioning of the MOS devices. The total ΔI_D deviation can be obtained supposing non-correlation between these two electrical parameters:

$$\sigma^2(\Delta I_D) = \sigma^2(\Delta\beta) + g_{mg}{}^2\sigma^2(\Delta V_{TO}) \qquad \textbf{(2.25)}$$

When speaking in terms of resolution in the current domain, a more useful figure is the relative mismatching $\Delta I_D/I_D$ rather than the absolute values. Furthermore, this type of study is commonly interesting when the MOSFET is operating is saturation with high output impedance, hence behaving as a controlled current source. In this case, (2.25) can be rewritten as:

$$\left(\frac{\sigma(\Delta I_D)}{I_D}\right)^2 = \frac{1}{WL}\left[\left(\frac{A_\beta}{\beta}\right)^2 + \left(\frac{1-e^{-\sqrt{IC}}}{\sqrt{IC}}\right)^2\left(\frac{AV_{TO}}{nU_t}\right)^2\right] \qquad \textbf{(2.26)}$$

Due to the non-linear law of the drain current versus the threshold voltage, such current mismatching changes along the saturation regions of operation. Practical values of β and V_{TO} deviations are collected in Figure 2.18 and Figure 2.19 from literature. Based on these data, a comparison between both terms of (2.26) returns a V_{TO} dominance extending from deep weak inversion to medium strong inversion regions.

In this way, a knee Inversion Coefficient (IC_{knee}) is defined as the boundary between V_{TO} and β dominant mismatching regions in strong inversion:

$$IC_{knee} \simeq \left(\frac{\frac{A_{VTO}}{nU_t}}{\frac{A_\beta}{\beta}}\right)^2 \qquad \textbf{(2.27)}$$

An example of a typical behavior is plotted in Figure 2.19. For a typical 1μm CMOS technology, with A_β/β=2.5%μm and A_{VTO}=15mVμm, the resulting $IC_{knee} \simeq 256$ is located at more than two decades over I_s.

Hence, considering only V_{TO} deviations, the asymptotic expressions for each region of saturated inversion are as follows:

$$\frac{\sigma(\Delta I_D)}{I_D} \simeq \begin{cases} \dfrac{1}{\sqrt{WL}}\dfrac{A_{VTO}}{nU_t} & IC << 1 \\ \dfrac{1}{L}\dfrac{A_{VTO}}{\sqrt{nI_D/2\beta}} & 1 << IC << IC_{knee} \end{cases} \qquad \textbf{(2.28)}$$

The maximum and relative deviation is reached at weak inversion due to the factor $e^{\frac{\Delta V_{TO}}{nU_t}}$ in Table 2.2. On the other hand, the sensitivity versus V_{TO} tends to decrease for large voltage overdrives. Also, once strong inversion is reached, W sensitivity tends to vanish. Such effect is a cancellation between the $1/\sqrt{W}$ -law decrease of $\sigma(\Delta V_{TO})$ and the $\sqrt{W}$ -law increase of the gate sensitivity to V_{TO} according again to Table 2.2.

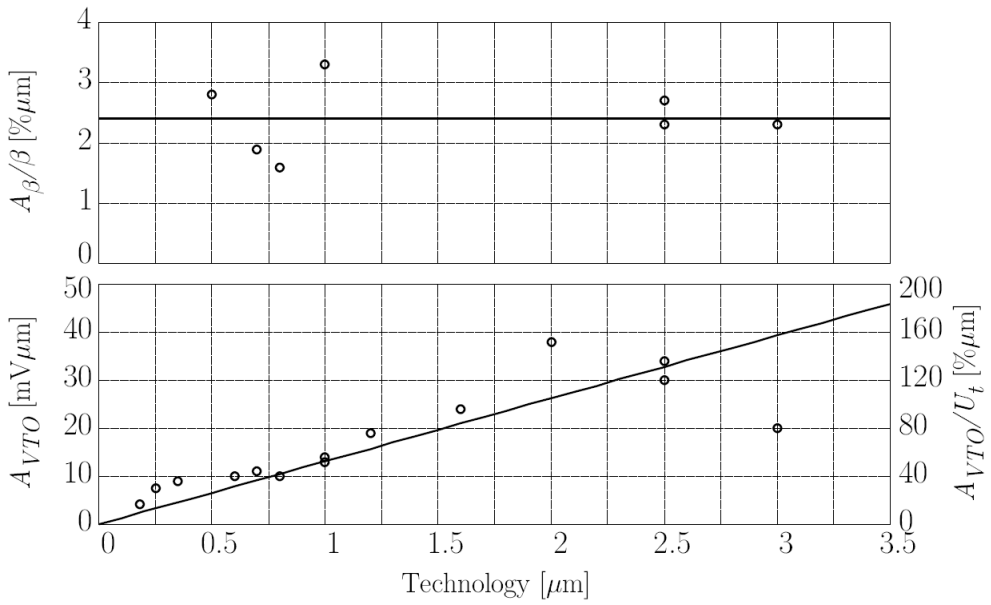


Figure 2.18 NMOSFET β and V_{TO} deviations versus technology generation at room temperature

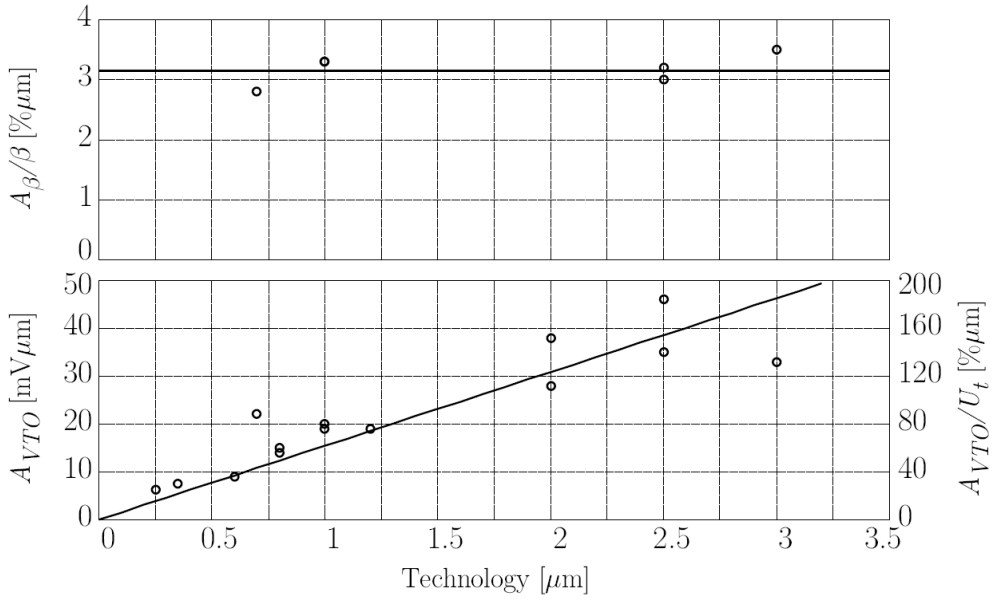


Figure 2.19 PMOSFET β and V_{TO} deviations versus technology generation at room temperature

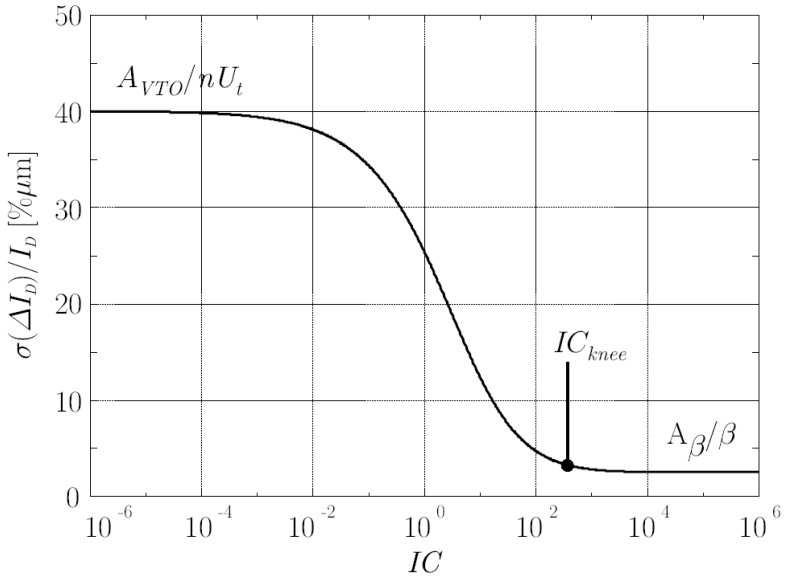


Figure 2.20 Relative drain current deviations versus inversion coefficient for a typical 1µm CMOS process of Figure 2.17 and n=1.5 at room temperature

Chapter 3

IR System Design Overview

Imager design sets out with an overall first sight of the system. In this way, the state-of-the-art of both focal plane array structures and read-out circuit implementations is presented. An overall design strategy is also discussed, defining a general work methodology, and fixing some technology and general system characteristics for the desired objectives.

3.1. IR FPAs: Structures & Op. Requirements

Throughout last thirty years, major advances in infrared detectors and microelectronics have lead in the obtaining of infrared focal plane arrays composed by two-dimensional arrays of detectors with a multiplexed read-out. In general, the IR FPA can be divided into two major parts, the detector array and read-out electronics. Recent IR FPA technology improvements make the design of high-sensitivity, high-density, large-format, and high-spectral-resolution IR image systems quite feasible. The application of recently developed architectures on the design of IR FPAs has resulted in the advantages of simplified electrical interconnection, reduced number of leads through the dewar, higher performance reliability, and easier packaging.

The key FPA figures of merit are fill factor and quantum efficiency. Unfortunately, not all the FPA detector surface is sensitive to IR energy. There is an inactive area surrounding individual IR detector rows/columns which is commonly used as electronic-signal pathways. The ratio of active IR sensing material to inactive row and column borders is called the fill factor. An ideal detector would have a very high fill factor because it is desired that a large percentage of its area will be dedicated to collecting IR photons and a very small area to detector segregation. Today's best infrared FPA detectors offer fill factors as high as ninety percent.

Effects of high fill factor are better sensitivity and overall image quality. Quantum efficiency refers stands for the relative efficiency at which IR photons are collected and converted into electrical charges. High quantum efficiency makes signal processing easier, and usually offer better sensitivity and performance at low

temperatures. A wide variety of architectures have been used in the development of FPAs, being the structures of the three major classes of IR focal plane arrays described below.

3.1.1. Hybrid Arrays

The most commonly used IR FPA structures for hybrid arrays are flip-chip and Z-plane technologies (Figure 3.1(a) and (b), respectively). In flip-chip implementations, the IR detector array chip and the ROIC are joined by the indium bump grown on the aligned pixels of both chips. This is the most used structure in the hybrid array technology. On the other hand, the Z-plane technology is compounded of several read-out chip stacked one on top of another and a detector array mounted to the third-dimensional plate on the edge. In Z-plane structure, one ROIC is used by one channel of detectors so that many circuit techniques like complex input circuit, gain offset correction, A/D converter, smart filtering, and neural computation, as well as image signal processing can be implemented in the read-out chip. However, image resolution is limited by the read-out chip thickness. Uniformity of indium bumps, chip alignment, thermal expansion effects and mechanical damage on the detectors should be considered during the array hybridization process.

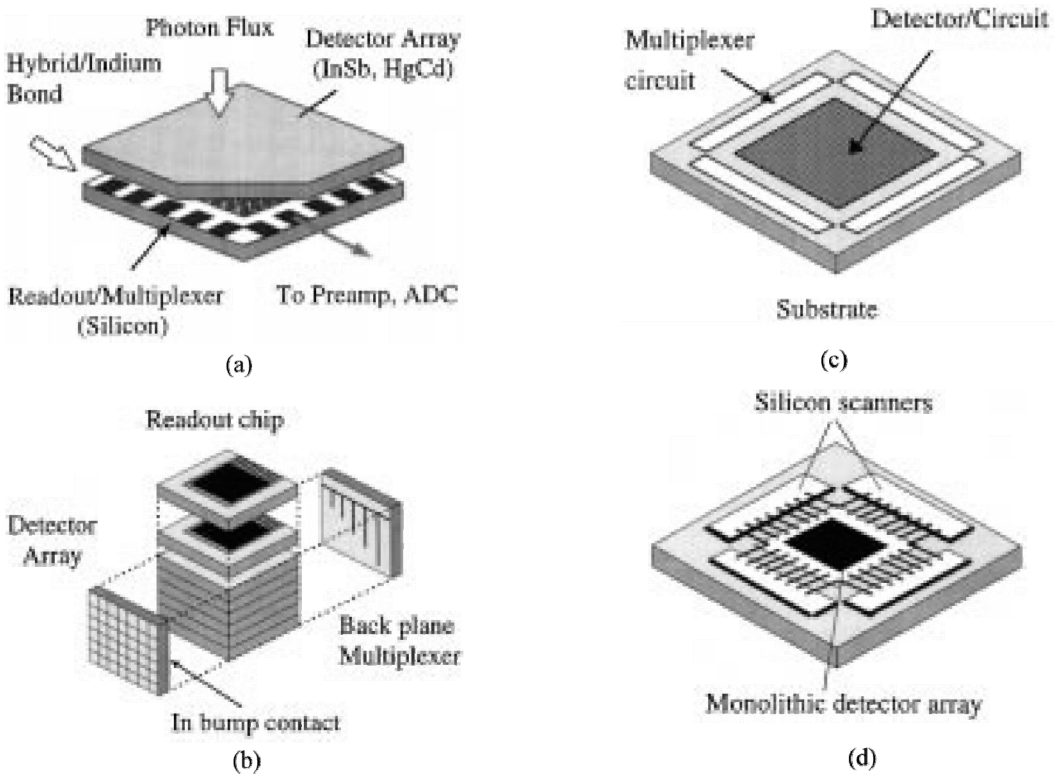


Figure 3.1 The structure of flip-chip hybrid array technology (a), Z-plane hybrid array technology (b), monolithic array technology (c), and pseudo-monolithic array technology (d) [HSI97]

3.1.2. Monolithic arrays

Monolithic array technology is being currently developed to overcome hybrid process drawbacks by building IR detectors like PtSi Schottky barriers, micromachining bolometers, or extrinsic detectors on the silicon substrate. Thus, both IR detectors and read-out circuits can be fabricated in a monolithic chip as shown in Figure 3.1(c). Both production and reliability of IR FPAs can be improved under monolithic design. However, the detector types and materials must be compatible with the silicon process, and reliable, large FPA arrays are really hard to obtain, which limit the applications of the monolithic arrays in IR image systems.

Comparison between hybrid and monolithic arrays is bound to be made. Monolithic FPAs are easier and less expensive to manufacture than their hybrid counterpart because fewer manufacture steps are required. Conversely, monolithic FPAs generally behave with lower performance than their hybrid counterparts because disposing the detector material and signal pathways on the same level results in a significantly lower fill factor (~55%), which reflects in poor image quality, specially for low temperature or small temperature gradient scenes. Even though hybrid process requires more steps and can be more expensive for medium-resolution arrays, it results in FPAs with a noticeably higher fill factor (~75%-90%), leading to high thermal sensitivity.

3.1.3. Pseudo-Monolithic Arrays

As an alternative method to the indium-bumping hybrid array and monolithic array technologies, the ROIC and the detector can be compounded using the via-hole technique, in the so-called pseudo-monolithic array as shown in Figure 3.1(d). Both read-out chip and detector chip surfaces must be polished to achieve a precise flatness and parallelism before combining a single chip. Then some detectors fabrication processes and routing metallization processes are applied to the combined single chip. The pseudo-monolithic technology retains some advantages of silicon-like processing, but its reliability still needs to be optimized.

3.1.4. Operational Requirements

In different applications of IR image systems, there exist certain specific requirements for the design of IR FPAs. In general, the requirements involve a broad range of electrical circuit detector array parameters that are summarized in the next paragraphs [HSI97].

Detector Bias Control

Detector bias reflects on dark current, injection efficiency, flicker noise and responsivity besides it has a direct influence on the operation ability and linearity of spectral response. This parameter should be controlled for a proper operation of the FPA.

Injection Efficiency and Bandwidth

Injection efficiency is defined as the read-out circuit input current over the IR detector photogenerated current. High injection efficiency and wide bandwidth lead to good responsivity and read-out performance. An input impedance smaller than shunt detector resistance is required in order to accomplish such conditions.

Charge Storage Capacity

In most read-out structures of IR FPAs, the photon excited carriers are accumulated on the integrating capacitor and transferred to voltage outputs. The charge storage is determined by both bias and dark currents of IR detectors as well as the value of the integrating capacitor. and can be improved through low offset and I_{dark} values and by using a large integrating capacitor. However, the capacitance value is limited by pixel size and chip area of the read-out circuit.

Noise

Random FPA noise sources are mainly the photonic and electric sensor noises, and noise from read-out electronics. The random and time-invariant noise source associated with the fabrication process of detectors and read-out circuits is the fixed-pattern-noise (FPN). Those noise sources contributed by read-out electronics such as transistor white noise and reset noise (KTC or clocking noise) must be minimized so that their levels will be below the background photon noise (i.e. achieve the BLIP). Generally, an accurate layout and the use of specific circuit techniques are employed to correct these effects.

Dynamic Range

The dynamic range is defined as the ratio of maximum capacity to noise floor. The required dynamic range of IR FPAs is determined by the ratio of the brightest signal level to the weakest. Larger dynamic ranges are desirable but limited by storage capacitance, linearity and background noise.

Read-out Rate

The read-out rate is chosen depending on specific system requirements, and is limited by the maximum allowed chip power dissipation. Usually, a higher read-out rate is required for video application on real-time image analysis.

Integration Time

Like the read-out rate, the integration time is selected according to application. In most cases, integration capacitance saturation frequency and detector sensitivity determine the proper length of integration time.

Array size and Pitch

The array size and pitch are usually set by the IR FPA technology. Higher image resolution requires larger array size and smaller pixel pitch. However, larger integrator capacitances can be implemented in bigger pixels, and a higher dynamic range can be achieved. Thus, the optimal design trade-off should is somewhere between application flexibility and resolution performance.

Power Dissipation

This is a typical requirement in applications using photonic IR FPAs. Such detectors must be operated under low temperature condition in order to avoid carrier generation effects.

Operating Temperature

The operating temperature is determined by the detected wavelength range and the material of IR detectors. For each detector, there is a unique operating temperature.

As explained before, electronic and FPN are the predominant noises in infrared systems. Temporal noise includes shot, thermal, flicker, generation-recombination, KTC and photonic sources, and are generated in both the detector and the read-out circuitry. The pattern noise is caused by the process dependent variations which produce offset drifts among detector channels. Usually, the temporal noise can be reduced by detector technology, operational condition, circuit techniques, and system arrangement, whereas the fixed pattern noise can be reduced by calibration techniques.

The two-point and multipoint calibrations are commonly used to reduce the FPN. The required number of calibration points is dependent on the infrared radiation determined by the range of object temperature variations. A larger radiation means a larger output voltage swing and more non-uniformity of response. For the same range of temperature variations, the infrared radiation of the MWIR detector is larger than that of the LWIR detector. Thus, the number of calibration points of MWIR read-out is usually more than that of LWIR read-out. The noise sources contributed by ROICs should be carefully reduced to achieve a BLIP. Some general strategies of noise reduction for read-out circuits are correlated double sampling (CDS) [KAN80], modified CDS [HAN06], multiple correlated sample read (MCS) [YOU92], and chopper-stabilized input circuit (CSI) [LOC87].

3.2. Classical Read-out Circuit Topologies

One of the key points in IR FPA development is the design of fine read-out circuits, which must provide good interface between the detector and the following processing stage. In this sense, some of the most popular CMOS topologies are discussed [HSI97] [TAN04]. Circuits like source-follower per detector (SFD), direct injection (DI), and gate-modulation input (GMI) are still commonly used in large

staring FPAs because of the small pixel area and low power consumption. In addition, more complex circuit structures like buffered direct injection (BDI) and capacitive trans-impedance amplifier (CTIA) have been developed to provide excellent bias control, high injection efficiency, linearity and noise performance. Recently, some new read-out structures like share-buffered direct injection (SBDI), switch current integration (SCI) and buffered gate modulation input (BGMI) have arised to overcome the traditional area-performance trade-off. In the following some of these state-of-the-art structures will be presented.

3.2.1. Source-Follower per Detector (SFD)

The circuit of Figure 3.2, namely Source-Follower per Detector, is compounded by the NMOS source-follower MNI-MNL, the PMOS reset gate M-Rst and the NMOS multiplexer M-Sel used in each cell. The capacitive integrator is obtained as a sum of the detector capacitance $C_{detector}$ and the input capacitance of the SFD. The integrator capacitance is reset to high and then discharged by the photocurrent $I_{detector}$. After one integration period, the cell voltage signal is sampled to the output stage serially through the multiplexer controlled by the clock select.

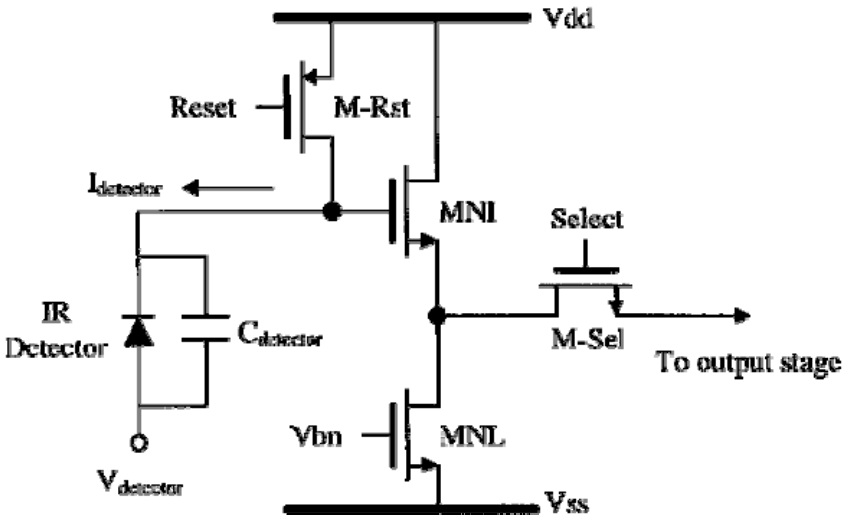


Figure 3.2 Source Follower per Detector [HSI97]

The simplicity of such a structure makes it suitable for high density, large format and low power applications. However, since the photocurrent is directly integrated to $C_{detector}$, the detector bias changes through integration. It can result in variations of detector characteristics and non-linearity of read-out current, which limit the usable range of this topology. Moreover, SFD is quite sensible to the KTC noise induced by the integration-and-reset function and to the FPN caused by process-dependent threshold voltage variations. KTC noise is normally reduced by applying CDS, which measures an effective signal level over an initial integration noise offset.

3.2.2. Direct Injection (DI)

Another compact read-out topology is the direct injection circuit of Figure 3.3. In DI, the common-gate PMOS device M_{DI} is used to bias the IR detector and sense $I_{detector}$. The latter charges integration capacitance (C_{int}) through M_{DI}, and this capacitance is reset to GND by NMOS M-Rst. The output integrated voltage is finally read through the follower M_{PI} and the multiplexer M-Sel.

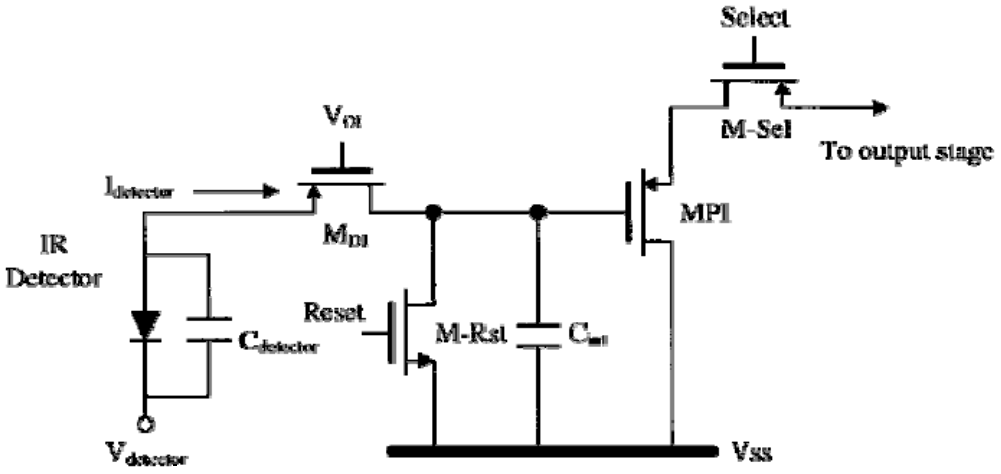


Figure 3.3 Direct Injection circuit [HSI97]

The common-gate MDI provides better bias to DI circuit. Like in the previous Section, this circuit has a simple structure and no active power dissipation. Injection efficiency is determined by the ratio of detector shunt resistance to input resistance of M_{DI}. Thus, lower input resistance needs higher injection efficiency and better detectivity since the input resistance of the PMOS device M_{DI} is proportional to its overall current including the background current level. Hence, the DI is not suitable for the applications of low background IR current read-out. Moreover, a stable and low noise dc bias V_{DI} is needed in the DI circuit. Both threshold voltage non-uniformity and KTC noise are still problems of the DI read-out circuit.

3.2.3. Gate-Modulation Input (GMI)

The circuit Gate Modulation Input is made of a gain-controlled current mirror by a tunable source bias V_{source} as shown in Figure 3.4. The injection current flowing into the master device M_{input} is integrated in C_{int}, whereas the reset is performed by M-Rst. The current gain of the current mirror M_{load} and M_{input} is tunable by the adjustable bias V_{source}. Similarly to DI circuit, the injection efficiency of GMI depends on the ratio of internal detector resistance to the M_{load} input. However, the inherent current gain of the GMI leads to higher detection sensitivity and reduced input referred noise as compared to the DI. Moreover, the adaptive current gain in the GMI can be controlled by the background level and thus the realizable background suppression leads to a higher dynamic range. On the other hand, both injection efficiency and current gain of the GMI are sensitive to the variations of V_{source} and threshold voltages. To obtain a large total

dynamic range in the GMI circuit, the current gain should be kept high and uniform, by means of strict requirements on MOSFET threshold voltage and dc bias stability of V_{source}.

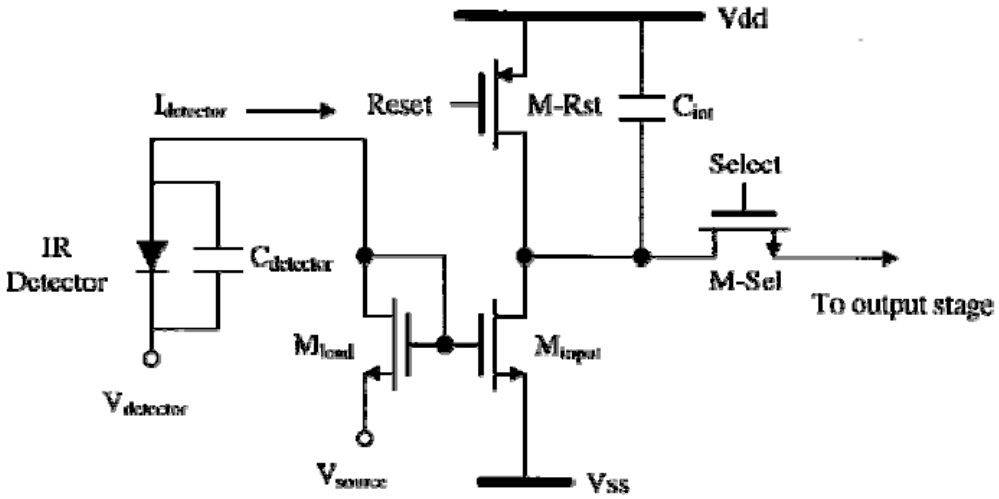


Figure 3.4 Gate-Modulation Input circuit [HSI97]

3.2.4. Buffered Direct Injection (BDI)

A more complex version of the previous direct injection topology is the Buffered Direct Injection circuit of Figure 3.5, where an additional inverted stage (-A) is added between the gate of the input device M_{BDI} and the input node. The negative feedback gain arises to an input impedance reduction of a factor A, increasing, at the same time, the circuit injection efficiency to values close to unity. The gain stage is usually implemented through a differential pair.

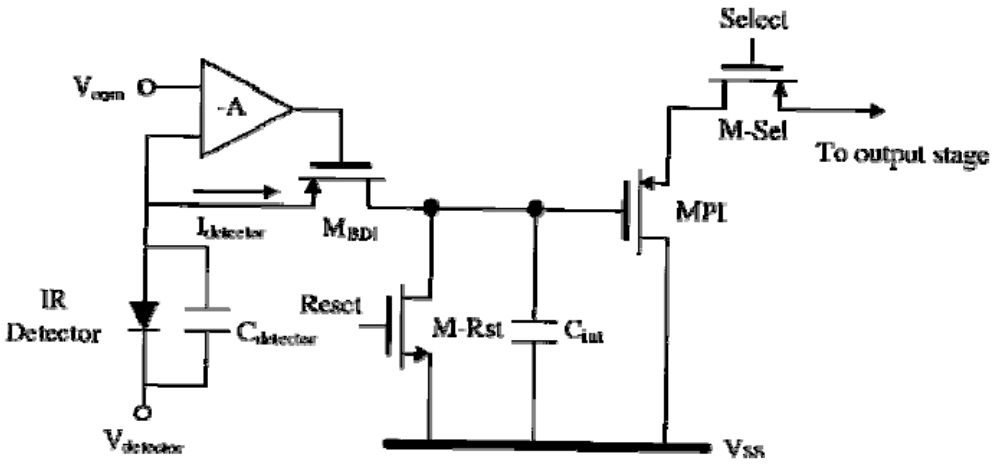


Figure 3.5 Buffered Direct Injection circuit [HSI97]

The detector bias control is in this case more stable that in SFD or DI due to the amplifier virtual short-circuit, and both input noise and bandwidth are even better than

in conventional DI. Detector bias is controlled over the input voltage V_{com} of the differential pair, instead of the preceding V_{DI}. This feature immunizes the circuit from possible threshold voltage variations and input noise sources. The price to pay is active power consumption during the integration, which can be reduced applying low-power techniques to the gain stage. Generally, BDI is used in applications that require high read-out performance and can afford additional circuit complexity, area, and power restrictions.

3.2.5. Capacitive Trans-Impedance Amplifier (CTIA)

Figure 3.6 shows the schematic of the Capacitive Trans-Impedance Amplifier (CTIA) circuit, where the integration capacitance C_{int} is placed in the feedback loop, in parallel with the M-Rst transistor, which discharges the referred capacitance and resets the output voltage to the V_{com} value. The detector current bias is now managed by the latter though the amplifier virtual short-circuit hence it is possible to obtain good controllability as in BDI.

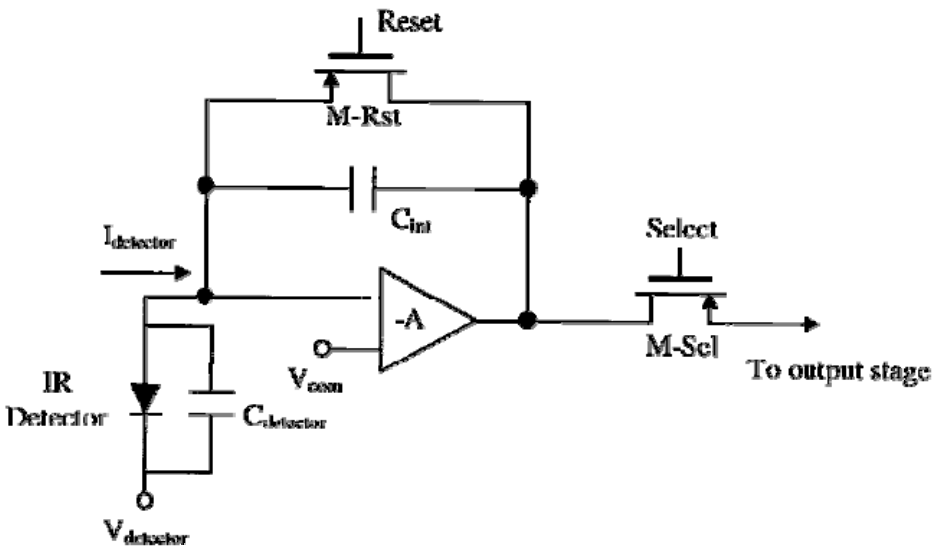


Figure 3.6 Capacitive Trans-Impedance Amplifier circuit [HSI97]

Due to Miller effects on the integration capacitor, its capacitance can be made extremely small to obtain low-noise and high-sensitivity performance. Unlike DI and BDI, the input impedance of CTIA is independent of detector current. However, the feedthrough effect of the reset clock can be coupled to the detector node and affect the stability of both detector bias and amplifier DC point. Moreover, additional area and power consumption are needed in the CTIA inverted gain stage. Usually, this inverted gain stage is implemented by a differential amplifier to provide low detector bias offset and a CDS stage is used to eliminate the KTC noise.

3.2.6. Share-Buffered Direct Injection (SBDI)

An improved release of the implementation seen in Figure 3.5, known as Share-Buffered Direct Injection, has been recently proposed. In SBDI, the gain stage is also a differential amplifier with the shared half circuit techniques as shown in Figure 3.7.

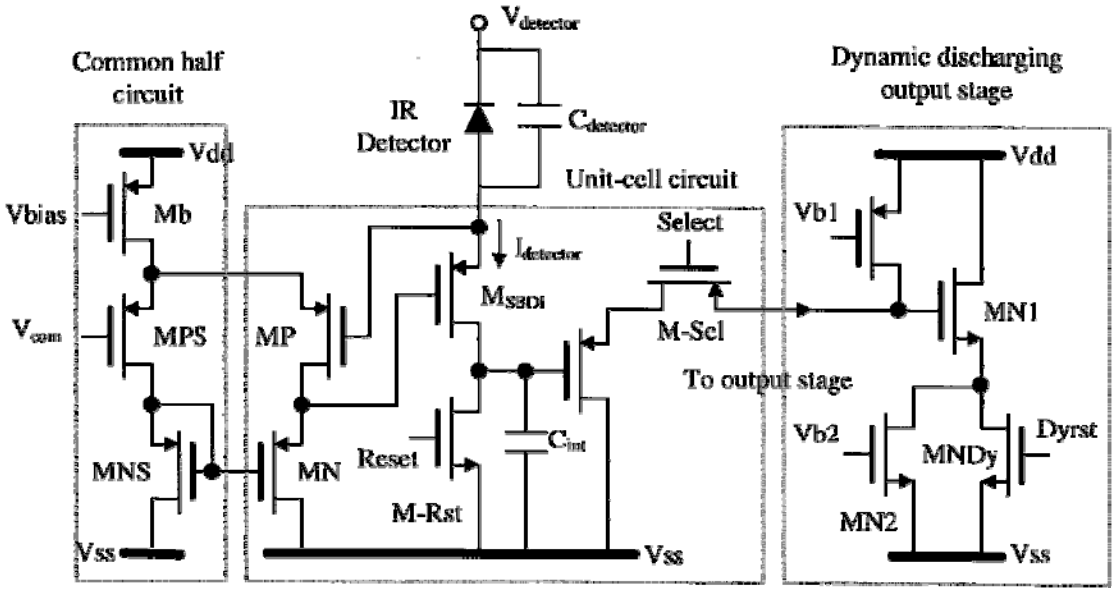


Figure 3.7 Share-Buffered Direct Injection circuit [HSI97]

The differential pair consists of the common left-half circuit Mb, MNS, and MPS which is shared by all the cells in the same row and the two MOS devices MP and MN which are implemented in each cell circuit. The source node of MP and the gate node of MN are biased by the shared half circuit though two global lines. Under this arrangement, both chip area and power dissipation of the amplifier in the SBDI can be reduced to nearly the 50% of those in BDI or CTIA circuits. However, high injection efficiency, good detector bias control, threshold voltage variation immunity, and low noise performance of the BDI circuit can be maintained using the SBDI topology. In the SBDI circuit of Figure 3.7, a dynamic discharging output stage is also introduced to save the static power dissipation and improve read-out speed by applying a dynamic discharging gate MNDy and clock Dyrst. The discharging gate MNDy is controlled by clock Dyrst and dynamically turned on to overcome the speed bottleneck of output stage at discharging phase consuming only dynamic power.

Generally, the SBDI can offer good behavior by means of circuit area, power consumption, and circuit performance. This makes it more suitable for high density, large-array, and high-performance applications in IR FPAs.

3.2.7. Switch Current Integration (SCI)

A new structure called the SCI is shown in Figure 3.8 where the integration capacitors are put outside the FPA and shared by the cells in the same column. The

detector current $I_{detector}$ is selected row by row, switched to the share integrator through the row select switch MR-Sel, and integrated. Thus, the structure performs the current switching and integration as its name implies.

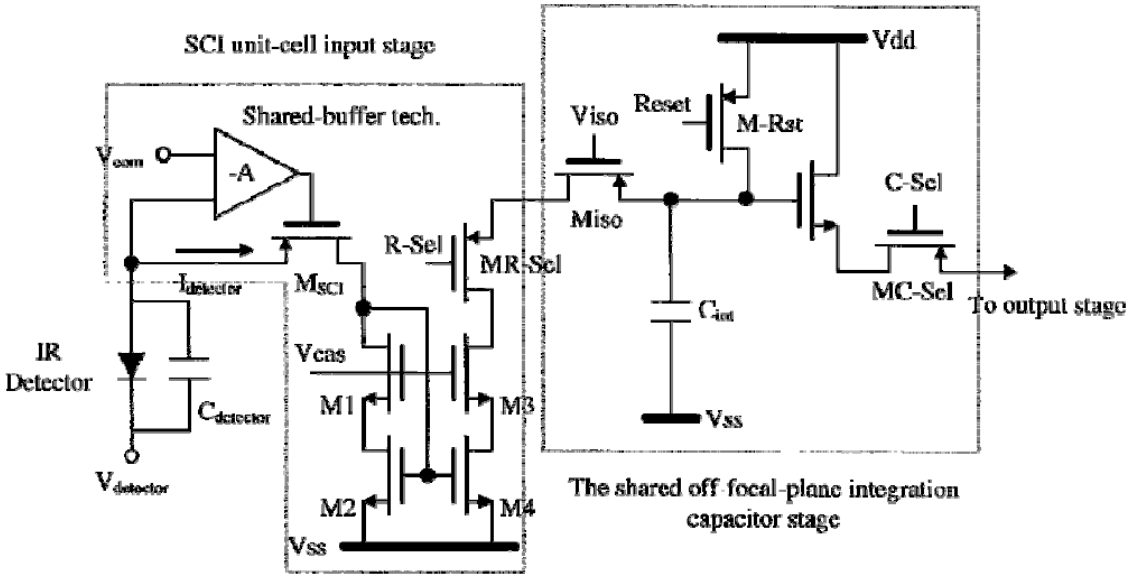


Figure 3.8 Switch Current Integration circuit [HSI97]

As shown in Figure 3.8, the shared buffer technique is used in the gain stage of the SCI. Therefore, good performance of both SBDI and BSI can be retained in the SCI read-out structure. The cascade current mirror M1-M4 acts as the current buffer previously to switch selection and offers a current mode gain given by the dimension ratio of M2 and M4. This current gain is able to improve the detection sensitivity and reduce the input referred noise. When the row-selection signal R-Sel is low, each cell in the same row is selected through MR-Sel and connected to the shared integration capacitor stage. The switched current is integrated on the shared capacitor and then sampled to the output stage through MC-Sel controlled by the column-selection signal C-Sel.

Since the integration capacitor is moved out of both the cell circuit and the focal plane, pixel size limitations related to the read-out circuit can be released. Moreover, both dynamic range and charge capacity can be increased by introducing a large integration capacitor along the column direction in the shared off-focal-plane integration capacitor stage. The integration time of the SCI read-out structure is limited by one row processing time. This effect could lead to reduced detection sensitivity, which can be compensated by increasing the current gain of the current mirror.

3.2.8. Buffered Gate Modulation Input (BGMI)

In the GMI circuit of Figure 3.4 the amplified background current is directly integrated, and thus a large amount of charges must be stored within a unit cell. Under this situation, a large capacitor is required to avoid saturation, a notorious drawback when designing large, high-density IR FPA systems. In order to solve this problem, a

FPAGMI enhancement called BGMI is proposed and shown in Figure 3.9 where a current mode background suppression circuit is added to the SCI circuit to achieve higher dynamic range and better read-out performance. This technique results in a larger equivalent integration capacitance.

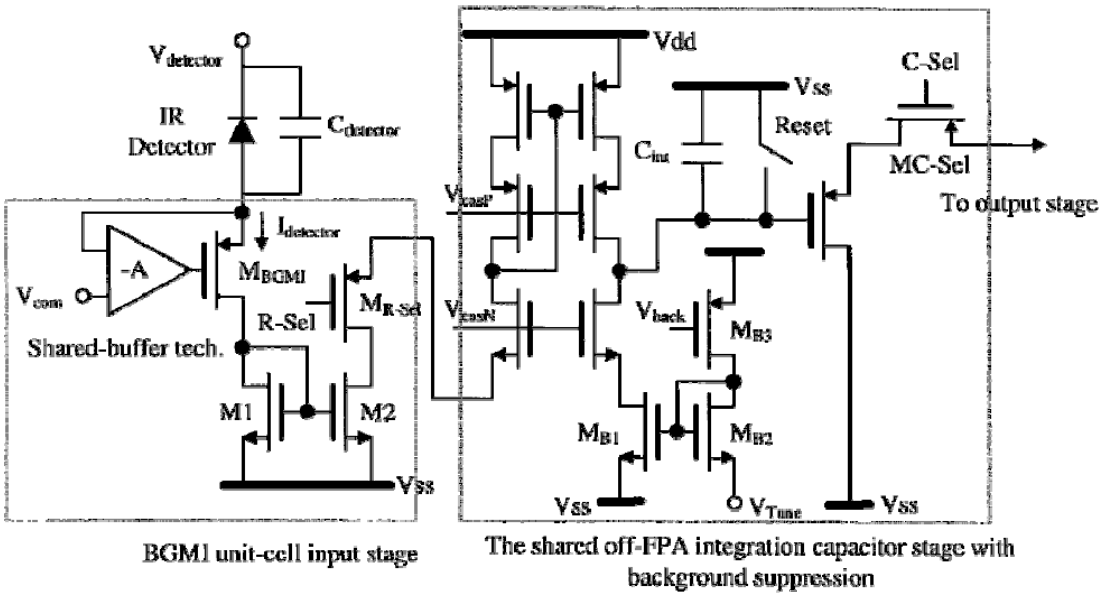


Figure 3.9 Buffered Gate Modulation Input circuit [HSI97]

As shown in Figure 3.9, the unit cell circuit of the BGMI consists of a shared buffer input stage, the unbalance current mirror M1 and M2, and the row selection switch MR-Sel. The shared-buffer technique provides a good bias control for the IR detector, whereas the unbalance current mirror has a large current gain due to the threshold voltage difference between M1 and M2 caused by the intentional device channel-length unbalance. Through the use of the threshold voltage difference, the strict requirement of low-noise tunable dc source bias V_{source} in the GMI and the inevitable FPN due to threshold voltage process dependence can be avoided.

The detector current is switched from the BGMI unit-cell input stage to the shared off-FPA integration capacitor. In the shared input capacitor stage the current is replicated through a cascade current mirror and subtracted by a dc tunable current before its integration in C_{int}. The current-mode background suppression is achieved. To generate de DC tunable current, the threshold voltage compensated current source M_{B1}, M_{B2} and M_{B3} is used with an adjustable voltage V_{tune} added to the source node of M_{B2}. This current source can generate a DC current quite independent on MOS threshold voltages. Thus, background is removed from the IR FPA read-out and good immunity to threshold voltage variations is achieved. The suppression current is also adjustable through the voltage V_{tune}. After the background suppression, the current signal is integrated in the integration capacitor, and alternatively sampled to the common output stage through the P-type source-follower.

Since the only row of the integration capacitor stage is needed in the whole chip and the infrared background current is low, the additional power dissipation of

background suppression circuits is still tolerable. The good read-out performance and adaptive gain control make BGMI suitable for the IR FPA read-out applications with large background level range.

Recently, design techniques for APS circuits are recently evolving from the previous analog topologies [SHI04] [FIS06], which output the amplitude integrated for a given fixed time, to mixed A/D solutions, which digitally quantify the integrated magnitude in terms of time for a given fixed reference amplitude. This second approach is generally implemented using asynchronous A/D converters inside the DPS (Digital Pixel Sensor) to compute either the time-to-first-spike [YUN05] or spike counting [ILR01] [CUL04]. In some cases, the digital read-out is also event-driven according to an arbitrated access protocol [CUL03a] [CHI07] [COS07] [LIC08]. However, none of these reported digital realizations supply any built-in FPN cancellation method, and they are not suitable for uncooled IR sensors, as no dark current nor input capacitance cancellation are considered. Furthermore, the required V/I references for their analog blocks are globally generated and distributed, so the DPS cell tends to be sensitive to pixel crosstalk.

3.3. New Design Proposal

This work is related to the design of new IR FPA structures based on the MWIR PbSe detector of Chapter 2. The overall FPA structure is made by two main development strategies:

- **Compact Monolithic (CM):** The detector is directly attached by post-processing to the ROIC CMOS substrate. The last metal is used here as the polarization and contact detector mask.

- **Modular Hybrid (MH):** The FPA is composed by a continuous PbSe detector matrix indirectly joined to a second matrix of ROIC modules through an intermediate substrate fabricated using a specific CNM Multi-Chip Module (MCM) through-via-hole technology that will be explained in Chapter 4. Since this technology is used for interconnection, all the CMOS process metals can be employed for ROIC internal routing.

The use of hybridization technologies is especially attractive for the construction of very large FPAs due to the next reasons:

- ✓ It makes ROIC CMOS technology independent to the detector technology, as far as its biasing potentials.

- ✓ Lowers the total system cost.

- ✓ Improves design flexibility and easy-reuse.

- ✓ Increases fill factor.

3.3.1. Design Basic Features & Specifications

The read-out circuit is designed for 3.3 V, standard, moderate-scale sub-micron CMOS technology (0.35µm from AMS). For the PbSe detector characteristics presented in Chapter 2, the following APS specifications are fixed:

- ✓ Dark current (I_{dark}) cancellation (µA).
- ✓ Input parasitic capacitance (C_{par}) compensation, as a result of each detector, hybridization technology and ROIC contribution (pF).
- ✓ Detector effective current integration (nA)

A digital interface is also convenient in order to reduce crosstalk effects, improve signal integrity, and simplify the signal post-processing. Moreover, such interface can be also used in order to provide external FPN compensation, I_{dark} calibration, etc. Hence, the read-out circuits are desired to include the additional features:

- ✓ Internal A/D conversion (at the highest available resolution)
- ✓ Purely digital I/O interface, pixel level programming
- ✓ FPN compensation and AGC capabilities
- ✓ Self-biasing
- ✓ Very low static power consumption (as low as possible)
- ✓ Reduced pixel size (below the up-to-date IR detector technology dimensions)

Several APS novel topologies are developed during this work. The designed basic building blocks have been integrated as APS libraries, to be finally applied in a resulting industrial application.

3.3.2. Design Methodology

The project follows, basically, the top-down design flow of Figure 3.10. General ROIC architecture assays are achieved using Matlab, while the electric design is performed under the Cadence environment. Thus, a complete design becomes a parallel and inter-dependent high-level/low-level research where several iterations are needed. Consequently, a first high-level of abstraction Matlab simulation is performed to select a global read-out architecture. After optimum strategy selection, a circuit level DPS architecture study is performed in order to satisfy the technological specifications of previous Section, and completed by a more accurate, transistor level, design. Is in this point where the design parameters (e. g. W, L) and their related MOS effects (e.g. aspect ratio, capacitance, bias currents, channel modulation) are tuned, using the simplified set of equations presented in Chapter 2. If everything is ok, next step is

All the design is conceived in a hierarchical and modular way-of-work. In other words, every single architecture element has been splitter into subcircuits depending on its functionality, and the latter are, at the same time, subdivided to simpler structures until basic, transistor-number limited blocks are obtained. Hence, both design and simulation are simplified, shortening the localization of possible system degradation issues. The main design software tools used in this work are explained downwards:

MATLAB: A powerful integrated numerical computing environment. It includes mathematical, graphical processing, and advanced visualization libraries by its own programming language based on standard C. Their powerful toolboxes make it the most employed engineering environment. Initial ROIC architecture research and evaluation are done using this software tool.

CADENCE IC FRONT-BACKEND: Professional CAD environment, oriented to integrated circuits design that mainly includes schematic, layout editors, numerical simulation by electrical and functional modeling, and physical verification. The following specific software has been used:

Diva/Assura: Verification utilities: used to perform automatic electric and design rule check (i.e. ERC, DRC), parasitic netlist extraction and layout-versus-schematic verification (LVS).

Virtuoso Analog Environment: Specific environment for analog and mixed circuit simulation. Compatible with some different simulators (e.g. HSPICE, Spectre), it allows the use of its own script language (OCEAN) and provide tools for waveform visualization and electrical characteristics calculus.

Virtuoso Editor: Schematic and layout editor, focused on physical and electrical system description.

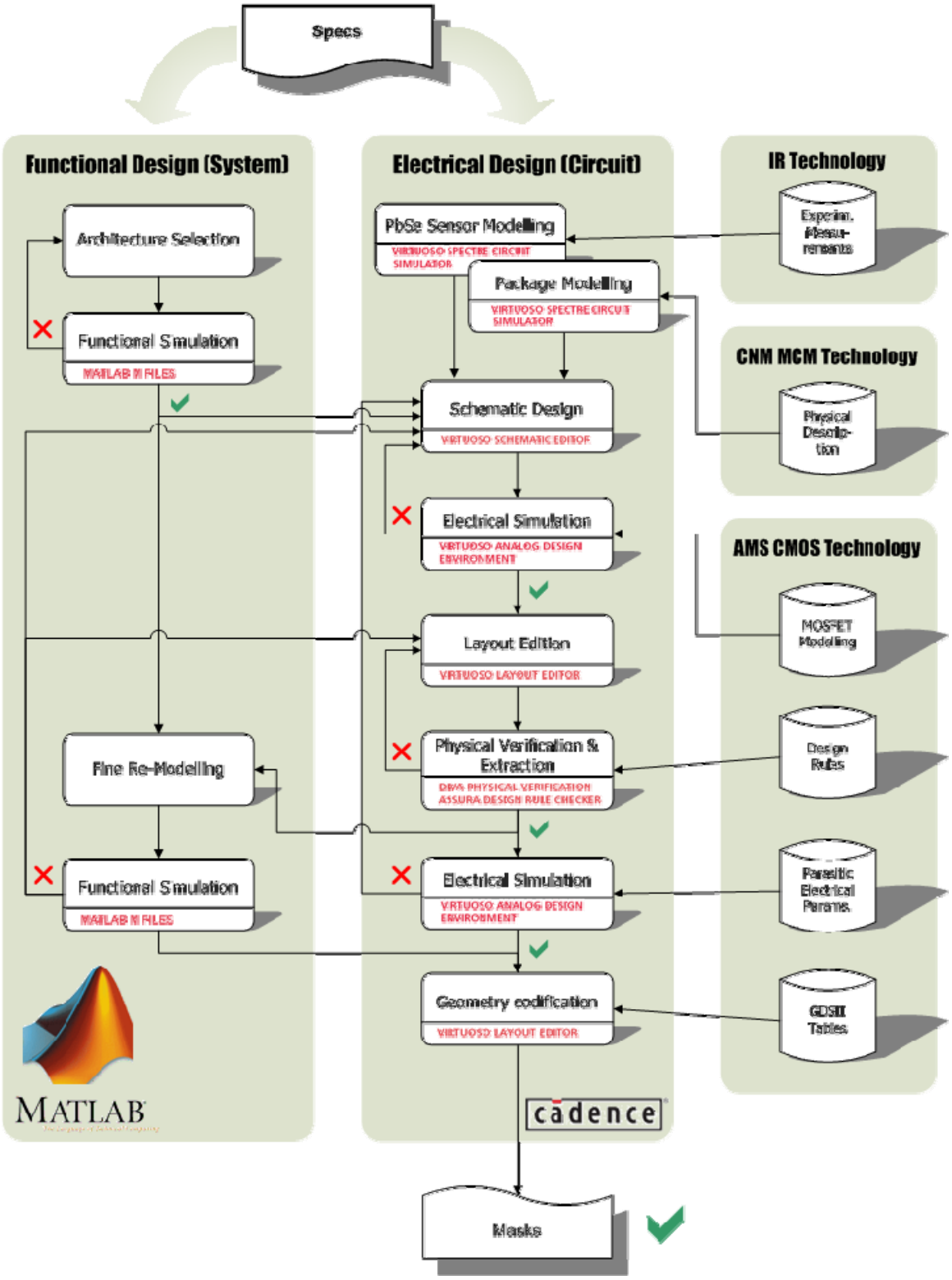


Figure 3.10 Design flow

Chapter 4

FPA Architecture

As cited in the previous chapter, the FPA design introduced here is based on a top-down research, where one of the primal steps is the architecture selection itself. In the following Sections, the FPA system is studied, including not only functional features (e.g. I/O interface, internal data mapping, ...), but also considering architectural details (e.g. scalability, modularity, ...) resulting on a focal plane implementation methodology.

4.1. FPA Construction

The complete FPA integration can be achieved in two different ways: the Compact Monolithic and the Modular Hybrid. Even though the monolithic approach is a trustworthy and commonly used technique to join both detector and ROIC materials, the hybridization alternative, currently under development, will lead to more compact APS designs, to a larger focal plane area and to the possibility of highly modular imagers. Since ROIC circuit functional design can be considered independent of the particular FPA physical implementation, both methods will be considered, being the former the present alternative for global system construction and evaluation, and the latter the future FPA work-line.

4.1.1. The Compact Monolithic (CM) Approach

This is the current available technology for this work. The focal plane of Figure 4.1 consists in a unitary, indivisible array structure where each APS is directly connected to its IR sensor using the last metal of the CMOS technology. In the Compact Monolithic approach, both the whole APS matrix and its corresponding access I/O pads are integrated in a single Silicon dice (i.e. the ROIC), to be post-processed a posteriori to build the PbSe detector layer on top of the CMOS die. It is interesting to remark at this point that detector post-processing is highly dependent on the particular CMOS technology compatibility, and cannot be used with all IR detectors.

This reliable, low complexity post-processing procedure reduces risks on system construction, which in terms of cost has always a positive meaning. Therefore, if large

FPA sizes are not required, monolithic structures are cheap, interesting alternatives to consider. Furthermore, the existing direct path between the detector and the APS reduces undesired parasitic capacitance and resistance effects in the input reading node.

On the other hand, large monolithic FPA designs are hard to integrate due to the limited yield of CMOS technologies, which tends to increase production costs. Hence, scaling up vision systems require modular strategies in order to overcome CMOS technology limitations.

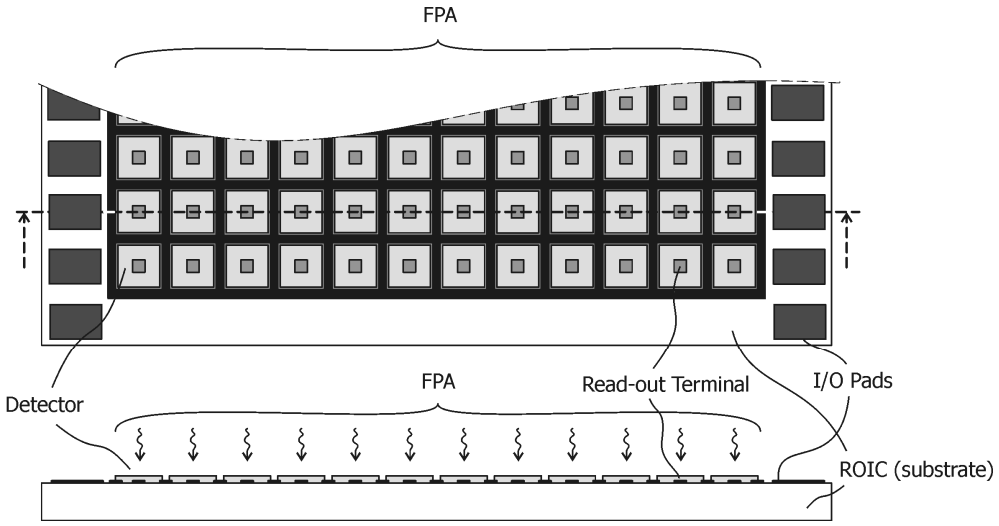


Figure 4.1 Compact Monolithic FPA structure scheme

4.1.2. The Modular Hybrid (MH) Approach

The future hybrid system [PAT05] makes use of in-house MCM packaging technologies in order to obtain a composite FPA without image loss. Three main elements compound the system of Figure 4.2:

- ✓ A continuous plane of PbSe detectors that delimits the effective FPA and share one of the two biasing terminals.
- ✓ A modular mosaic of identical CMOS ROICs, each one also made of several indistinguishable APS for detector signal processing.
- ✓ An intermediate substrate, using specific CNM Multi-Chip Module (MCM) technology, which acts as an interface between each detector and APS, through vertical metal vias. The ROIC modules are internally and externally connected using a deposited metal layer over the substrate and the hybridization AgSn bump contacts.

As the read-out and the detector layer only share the intermediate substrate, both technologies can be strongly independent. The modular placement of Figure 4.2 overcomes the fabrication limits of other technologies, where the total CMOS integration area would be at least as large as the focal plane. Using identical and

interchangeable ROIC modules the production performance of the overall system can be increased, and the last metal released can now be used to obtain smaller pixel sizes. Moreover, the IR detector can be produced at wafer level and it is allowed to employ non-standard FPA shapes depending on final application.

However, the hybrid structure also has many weaknesses as a larger parasitic input capacitance, or the lack of a reliable technology model, as a consequence of its early development state. In this sense, Table 4.1 compares the advantages and disadvantages of both Compact Monolithic and Modular Hybrid technologies.

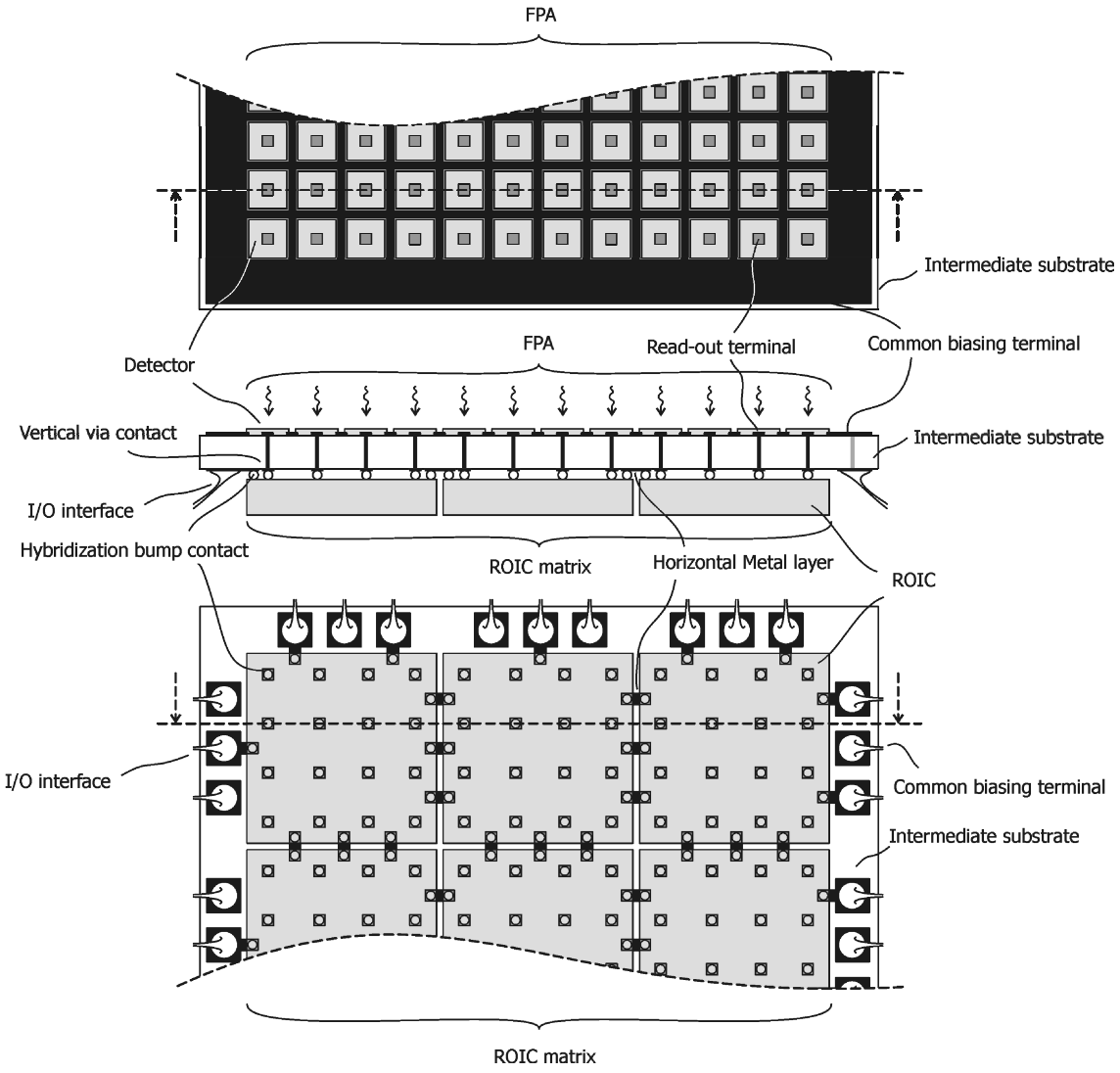


Figure 4.2 Modular Hybrid FPA structure scheme

Parameter	Compact Monolithic	Modular Hybrid
Production cost	Good, for low-medium resolutions; High, for high resolutions	High, for low-medium resolutions; Good, for high resolutions
Detector technology independence	Low	High
Flexibility	Low	High
Parasitic input effects	Low	Medium
Technology background	High	Low

Table 4.1 Compact Monolithic versus Modular Hybrid technology comparison chart

4.2. FPA Architecture

The design of mixed analog-digital systems is currently an extensive practice as considerably reduces the complexity of signal acquisition. Thus, the use of an internal A/D converter is a desired feature, and its implementation and location is a challenge. Every possible ADC location yields to one global system design strategy, all of which not only include the essential detector signal pre-amplification, but an output signal multiplexer in order to reduce the total amount of ROIC outputs.

4.2.1. Architecture Analysis

The most classical strategy directly integrates the detector current through an internal APS amplifier; the resulting voltage is then binarized through a high-speed, usually direct, A/D conversion previously to ROIC read-out. Temporal noise sources and induced multiplexing-stage crosstalk are relevant disturbances with noticeable effects on the obtained analog value (V_{mux}) of Figure 4.3.

An alternative is shown in Figure 4.4, where coupling is reduced by means of performing the A/D conversion previously to multiplexing. Integrating the ADC in the DPS considerably reduces the total available internal area of the pixel, revealing the necessity of compact and low-power CMOS design techniques. This last restriction leads to the use of the depicted predictive ADC topology instead of other direct (e.g. parallel conversion) or algorithmic (e.g. successive approximation) techniques, as the former simplifies the converter analog design. In the resulting processing chain, the employed ADC is composed by two cascaded stages: a pulse modulator and a digital

filter. The modulator is intended to sample amplitude to 1-bit, resulting on the pulse-train V_{pdm} (i.e. event generation). The main parts of this modulator are the low-frequency amplifier/integrator, a quantifier (i.e. comparator) and a DAC (i.e. a simple switch) to provide the necessary predictive feedback. The resulting quantification power error is focused in the V_{pdm} high-frequency band, so a low-pass digital noise filter is finally added, completing also time sampling. As a result, the digital code b_{out} is obtained.

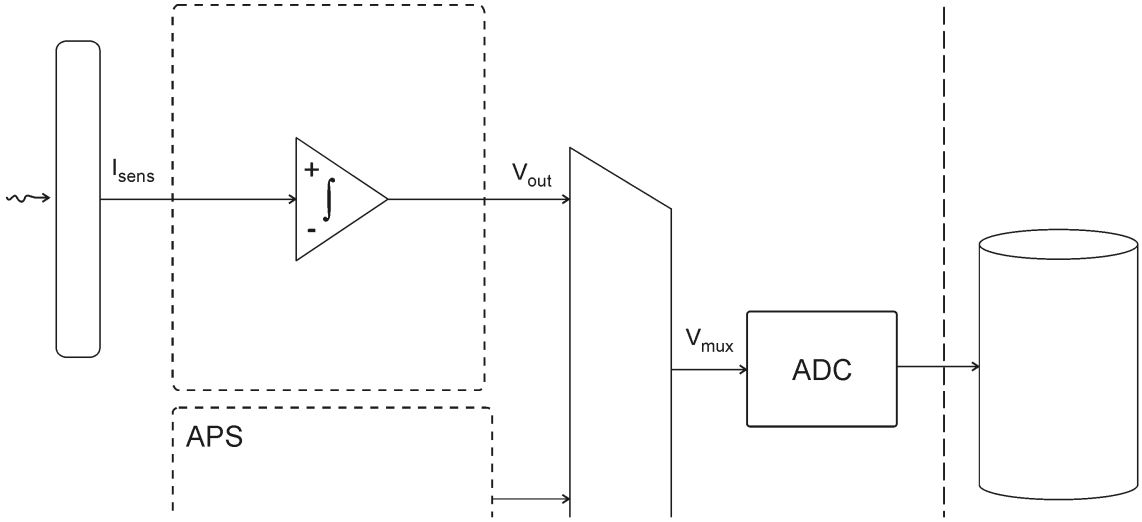


Figure 4.3 Mixed strategy num. 1: purely analog internal signal APS processing, external ADC

In order to reduce pixel power consumption, the modulator is commonly implemented by means of asynchronous design methods, either by time-to-first-spike (equivalent to PWM) [LUO06] [SHO06] or spike counting (equivalent to PDM) [MCI01] [CUL04] [LIC08]. The second approach provides a lower digital-switching activity during A/D conversion, so electronic noise decreases.

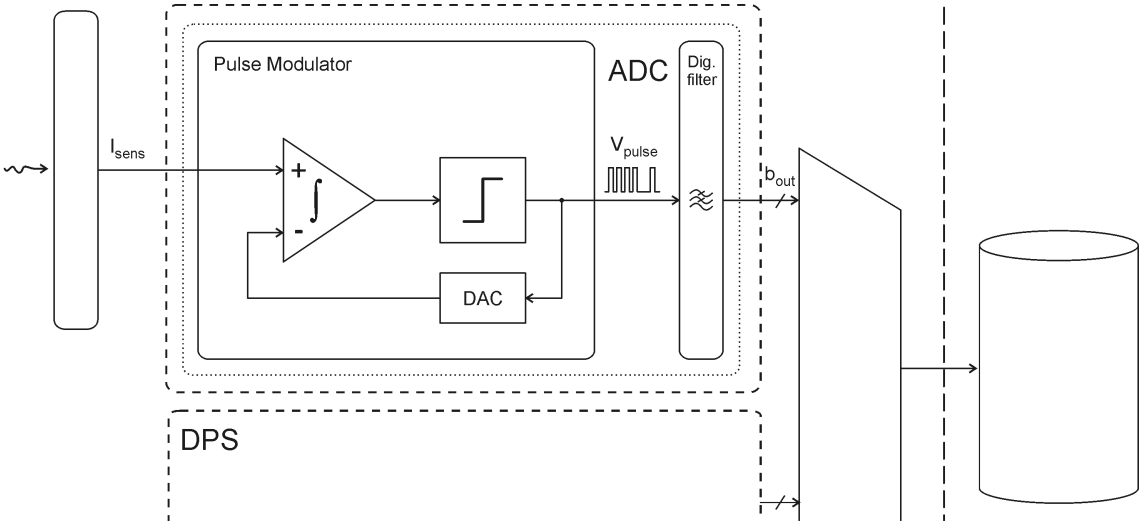


Figure 4.4 Mixed strategy num. 2: predictive ADC integrated in the DPS.

A method to reduce the total amount of required area per pixel is to remotely address and filter the pulses/events internally modulated in the DPS as in Figure 4.5; this solution usually introduce reading-out losses due to addressing speed restrictions.

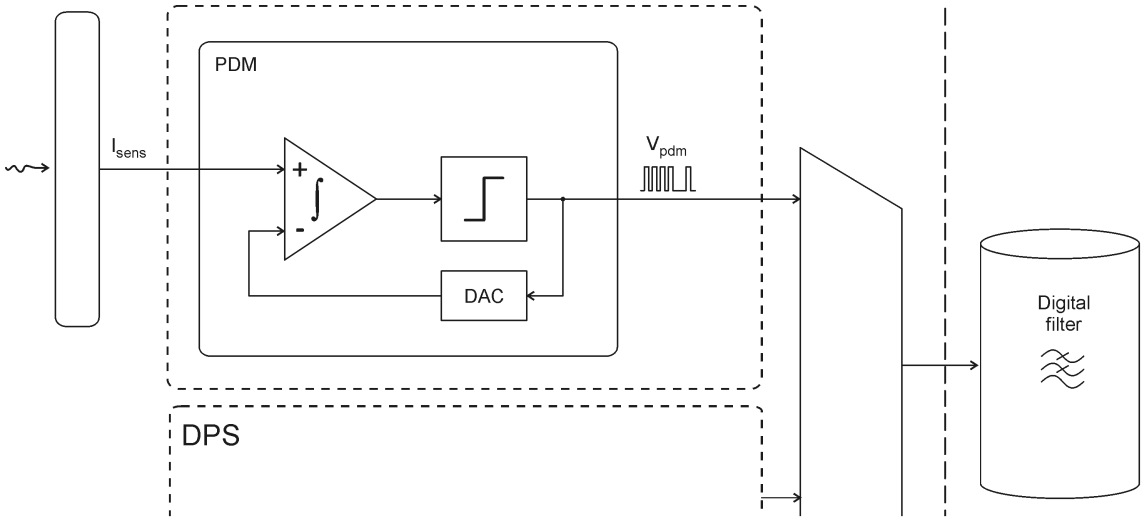


Figure 4.5 Mixed strategy num. 3: pulse-density-modulation integrated in the DPS, remote digital integration.

After discussing the four preceding strategies, logic brings onto consider the last two alternatives. Nonetheless, the choice is not clear. The most optimum area architecture (mixed strategy num. 3) will be first studied.

4.2.2. Addressed-Event Representation

Looking onto Figure 4.5, it is noticeable that the applied digital multiplexing is an asynchronous process. Moreover, the external addressing method has to be carefully evaluated to avoid final image reconstruction losses.

With this purpose a parallel row/column read-out strategy is chosen [CUL03b] [CUL04]. Some different arbitration rules are also selected to perform the row/column selection in case of event collision detection, as depicted in Figure 4.6. The operation is inspired in human retina, where every photoreceptor acquires and transmits the light in parallel, but addressed in a single dimension so as to relax area and bandwidth requirements.

Events are generated inside each pixel in direct proportion to the incident light level, and remain active until their external attendance. Every row/column reading access is achieved at a fixed scanning time, during which on-demanding rows are detected and selected by the arbitration circuit depending on a particular criterion. The selected set of pixels is binary read and recorded in order to compose the image; the figure is reconstructed dynamically in time, so a gradually increasing luminance map is obtained.

Even though conventional image generation procedures integrate signal over a constant time period, in this case the method is reverted: every single DPS integrates the input signal until a threshold value is reached, generating an event pulse. Hence, the incident luminance per pixel can be expressed as an event per time ratio (i.e. spike counting). This technique takes better profit on the total bus bandwidth, as the information is only acquired when necessary, reducing access to the darkest pixels.

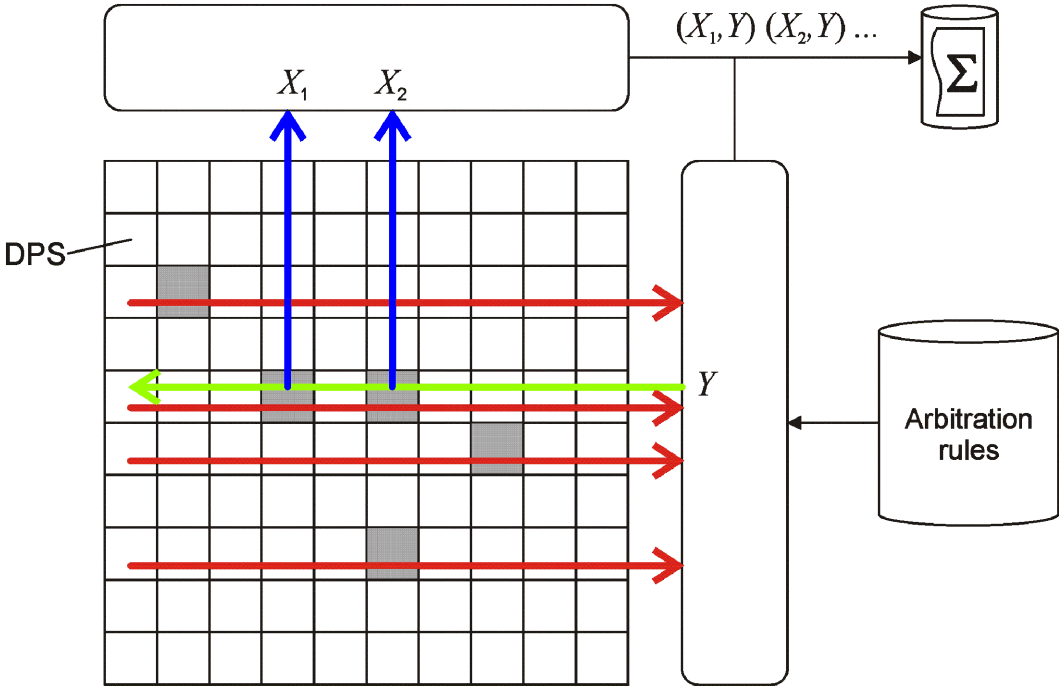


Figure 4.6 AER global scheme

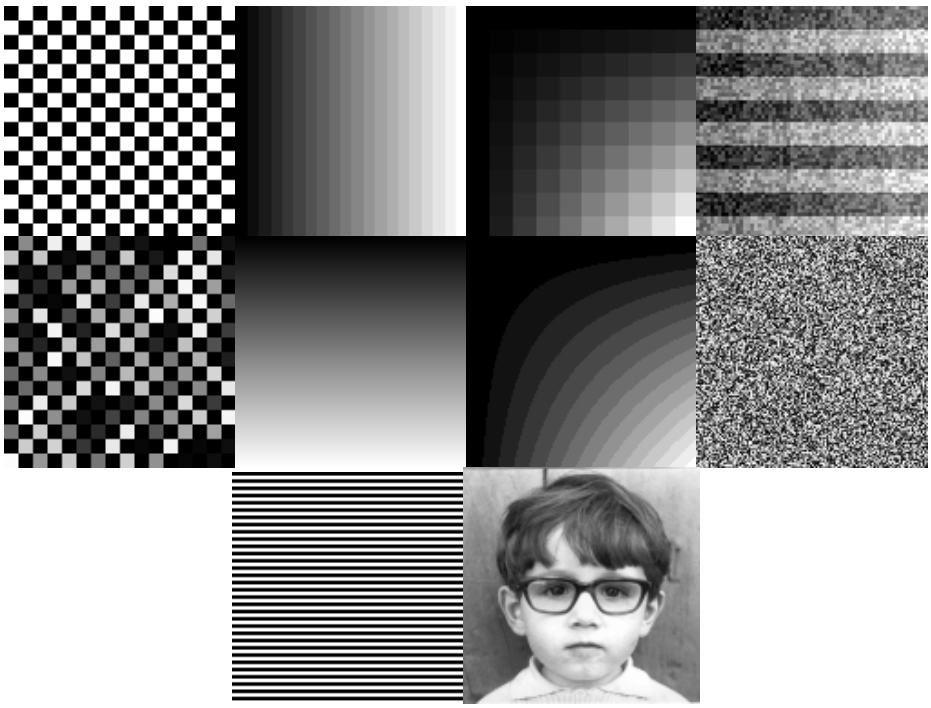


Figure 4.7 High-level simulation samples

The Address-Event Representation (AER) communication protocol [CUL03a] [CHI07] [COS07] [LIC08] used is a particular appliance of the referred PDM scheme, providing system of good noise immunity. The resulting signal can be rebuilt, low-pass filtered by the use of an event counter windowed in time, which considerably simplifies the ROIC structure.

The previous system architecture can be functionally evaluated. The following global variables are used in the study:

- ✓ Row/column pixel grouping in the matrix
- ✓ Arbitration rules. If a collision is detected, pixel selection following the criterion:
  - Position (PO) taken inside the row/column sequence: first (FPO) or last (LPO) position.
  - Number of events (NE) generated per row/column: highest (HNE) or lowest (LNE) number of events.
  - Total number of events requested (NR): highest (HNR) or lowest (LNR) number of requests on standby.
  - Number of iterations (NI) waiting for attendance: highest (HNI) or lowest number of iterations.
  - Random selection (RS).
  - Criterion mix: alternative (-) or with priority (+) selection, following a specification order. For example:
    - FPO: First row/column selection.
    - HNE+RS: Selection of the highest event-generated row/column, random selection if draw.
    - HNE+LNR+RS: Selection of the highest event-generated row/column. If draw, selection of the highest number of standby-events row/column. If second draw, random selection.
    - HNE-HNR+RS: Alternative selection of the highest event-generated row/column and the highest standby-event row-column. If draw, random selection.
  - Event attendance speed.

- Image patterns. 128 x 128 pixel resolution and 8-bit grey palette, with different luminance gradients and distributions.

The software routine consider a maximum luminance level of 2^N (in practice 2^8=256), where N stands for the number of grey-palette bit. The process starts with an initial zero-event matrix (E) and generation is produced for a value at least equal to unity. Every element of the original image matrix is incremented by 1 at a reading speed proportional to the inversely relation existing between the event generation time and the luminance, as described in (4.1).

$$G(x,y) = \frac{1}{\frac{256}{I(x,y)}}$$
$$E(x,y) = trunc(G(x,y)) \qquad \textbf{(4.1)}$$

Where I(x,y) stands for the (x,y) position luminance value of the image matrix (256 – white / 0 – black), and G(x,y), E(x,y) are, respectively, the actual event-generation matrix value and the standby event matrix value for the same position. The G elements saturate at '1' and the attended event row/columns of G and E are reset to '0'.

The reading speed parameter is delimited using the same relation: for a fixed total image scanning time (T_{scan}), the event-reading time (T_{read}) is resolved depending on the adimensional maximum reading iteration number (N_{read}), establishing the expression:

$$T_{read} = \frac{T_{scan}}{N_{read}} \qquad \textbf{(4.2)}$$

which normalizes to:

$$T_{read} = \frac{1}{N_{read}} \qquad \textbf{(4.3)}$$

and where N_{read} are power of 2 values. Thus, the final image (H) can be expressed as:

$$H(x,y) = N_{read} E(x,y) \qquad \textbf{(4.4)}$$

As (4.4) suggests, an iteration number of 2^8 yields, a priori, to the appearance of the maximum white level in H, as an absolute white in I(x,y) will generate an event for every test program iteration. Considering a total iteration number of 256:

$$H(x,y) = 256 \cdot 1 = \boxed{256} \quad \textbf{(4.5)}$$

But, in practice, a maximum number of events is hardly ever attended due to the appearance of event collision effects.

Additional image handling and analysis functions are also included in the main simulator, and in order to evaluate the different event arbitration rules. As a result, the majority of available reading strategies are checked: alternative row/column selection for all the criteria explained, in diverse order and priority, and random selection if draw.

Since row/column selection is equivalent, simulation is decided to group pixels in rows. After image pattern generation, a first iteration is done for each arbitration method and event scanning speed. After that, best image quality settings are selected and processed again with refined mixed algorithms. Figure 4.8 shows the result of applying mixed techniques to one of the image patterns. Conclusions are presented below:

- ✓ The best algorithm in terms of image sharpness per reading speed is the HNE. This method enhances high luminance image regions, and correct results are obtained above 256 readings per frame.
- ✓ The RS algorithm is reasonably efficient in shape detection, as it detects gradually higher luminance levels depending on the iteration run number.
- ✓ HNI arbitration performs a grey-level filtering, which will be interesting in contour detection.
- ✓ LNR criterion results are slightly worse than random selection.
- ✓ Double or mix criteria don't offer evident improvement over simpler methods.
- ✓ The remaining algorithms are rejected in first tests accordingly to their low efficiency.

Generally, a high dependency on the reading speed is noticed, a requirement difficult to manage when using global buses, decreasing the overall system performance. DPS design will finally forgo area restrictions in pro to speed and power consumption reduction. Hence, the FPA architecture will be focused on the in-pixel predictive A/D conversion scheme (Figure 4.4).

Figure 4.8 Resulting acquired 128 x 128 pixel, 8-bit grey level images depending on arbitration rules and reading speed

4.2.3. In-Pixel ADC

The adopted strategy of Figure 4. 9 extends the prior event-generation to full in-pixel predictive ADC by means of a simple event integration (i.e. counter) as the digital filtering block inside the DPS. PDM feedback is provided by resetting the analog integrator, and output filter losses can be controlled by a frame initialization signal (`init`). Because all active pixels are accessed sequentially and synchronized at the end of the frame acquisition time, the drawback of event-read collisions is avoided, and a high-level, functional verification is not necessary.

As depicted in Figure 4.10, image composition is performed locally in each pixel, though three main steps: charge integration, comparator quantification and digital counting. Every frame is decoded at T_{scan} and all rows are accessed simultaneously in the ROIC matrix, serially after integration. Control signals are the same for all the DPS in which the counter-binary shift functions can be integrated as a single, programmable internal register.

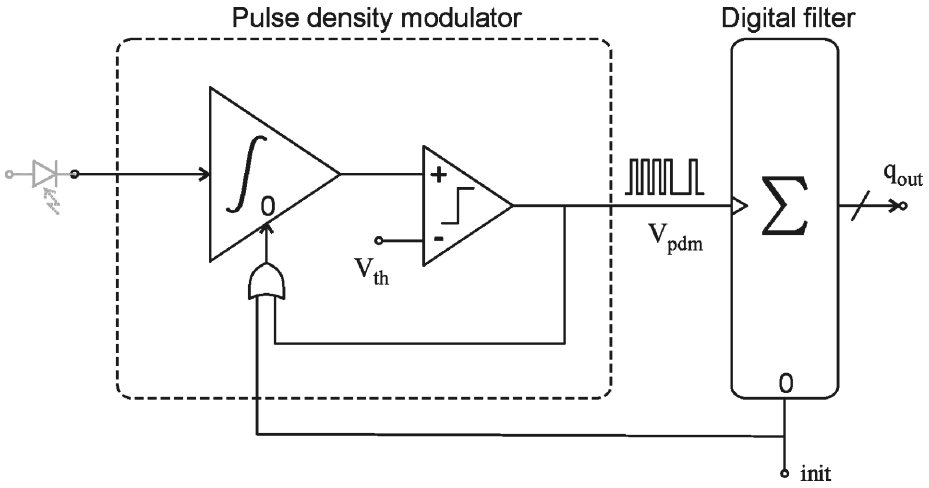


Figure 4. 9 Proposed in-pixel predictive ADC

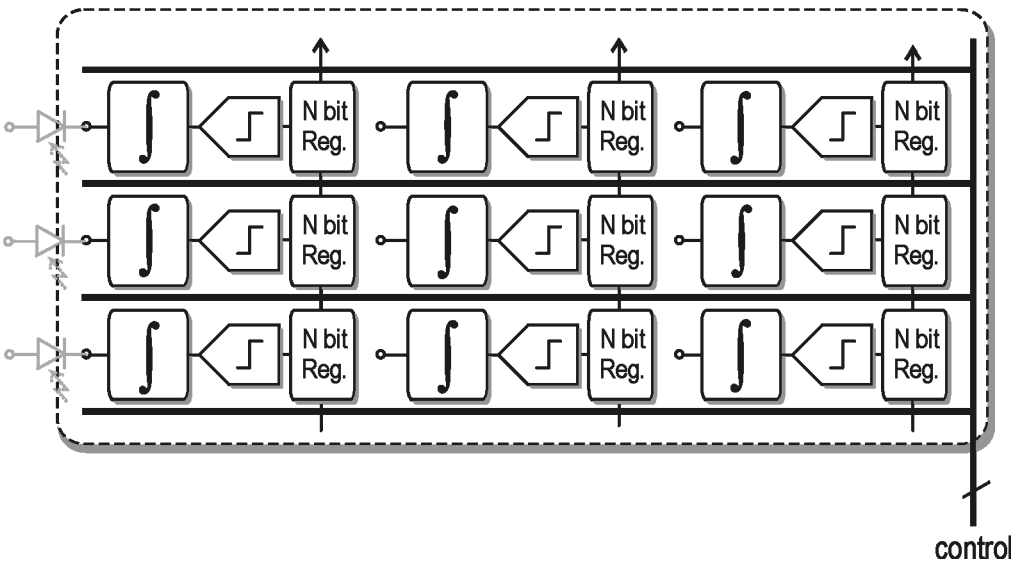


Figure 4.10 In-pixel ADC global scheme

Chapter 5

DPS Design

The DPS is the basic unitary active element of the FPA. This chapter presents all the new CMOS circuit techniques developed for the design of the in-pixel functional blocks. Every topology is widely explained and optimum strategies are chosen in terms of low-power consumption, compact design and integrability. A complete set of active stages are finally designed and ready to be integrated in full DPS cells.

5.1. DPS Block Architecture

Section 3.3. specifications lead to low-power, reduced area DPS CMOS circuits' research, in which an only-digital I/O interface is a must. From the analog point of view, the former requirements will be complemented with the next circuit strategies:

- ✓ Topologies which take maximum profit of each single MOS transistor in order to minimize the total number of per-pixel devices.
- ✓ MOSFET operation in weak inversion (subthreshold region) in order to obtain high a gain-consumption ratio.
- ✓ Self-biasing topologies for the internal generation of low-noise voltage and current references.
- ✓ Not only area-saving but also technology-mismatching and noise-reduction layout techniques usage.

On the other hand, the design of the digital block is oriented to:

- ✓ Local modularity with low interconnection
- ✓ Multi-functional logical blocks to be reused in time.

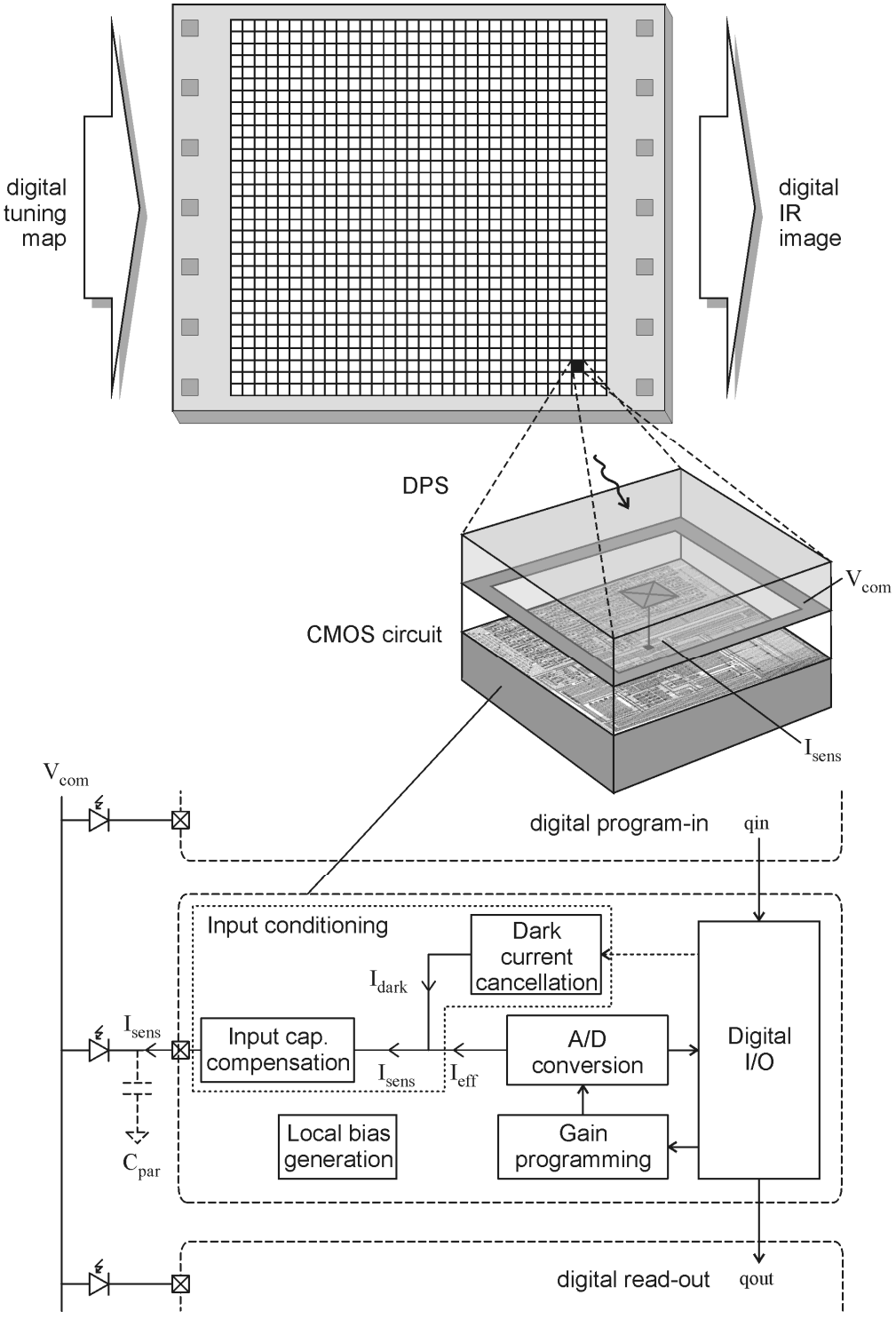


Figure 5.1 Simplified DPS architecture

Based on the above remarks, the selected ADC scheme and the considerations stated at the beginning of the documentation, the architectural model of the proposed system is shown in Figure 5.1. As a result, a fully digital imager is obtained, where a digital input map is supplied to the FPA for individual offset and gain tuning of each pixel, and the FPN compensated IR image is obtained as a digital output map. The DPS functional scheme is also depicted in the bottom part of the same figure, where V_{com} and I_{sens} are the common voltage and the individual output current of the IR sensor, respectively, while C_{par} stands for the total input parasitic capacitance contributed by the sensor, the interconnection technology (either monolithic or hybrid) and the CMOS circuit itself.

The DPS can be operated in two different modes: acquisition or communication. In the first case, the input blocks compensates C_{par} and the DC dark current (I_{dark}), so the effective signal I_{eff}, ideally proportional to the incoming IR power, can be codified by the spike-counting ADC and stored in the digital I/O block. During the communication phase, the digital block is reconfigured to allow at the same time both, the serial read-out of the IR sample through `qout`, and the programming-in through `qin` at each frame. It is already important to note at this level that no external analog references are supplied on the DPS. In fact, by the proper serial connectivity of these cells inside the FPA, the individual programmability of I_{dark} and the gain of the ADC can be managed at alternate frames. Dynamic offset cancellation (I_{dark}) can be then achieved either by auto-calibration methods or direct current programming through the DAC, whereas FPN correction and spatial contrast improvement of the IR image are encoded in the programming ADC gain sequence.

Next Sections present different circuit topologies for the design of each one of the functional blocks depicted in Figure 5.1. Every technique is conceived to accomplish the mentioned requirements and is strictly verified by the use of extensive Cadence simulations.

5.2. Input Signal Conditioning

The main specifications for this input stage are a low enough input impedance, combined with a high-resolution subtraction of I_{dark}. In this sense, the functional concept explained below is adopted.

5.2.1. Operation Principle

As any current-mode input circuit, the input capacitance limits the total system bandwidth. As a result, if current integration was performed in the self DPS input node, C_{par} would impose a minimum value for the I_{eff} integrator capacitance ($C_{int.}$) Even if such capacitance was smaller than C_{int}, voltage variations in the image detector, together with its finite output resistance, would distort the integration. Thus, voltage in bumping pad should be kept invariable so as to operate C_{par} at a constant charge and to be compatible with the broader range of detector output impedance. In this sense, the input

node regulator of Figure 5.2 is proposed, where zero voltage is fixed through the negative feedback loop so as to bias the IR sensor differentially to $-V_{com}$.

The input stage is also in charge of implementing the high-resolution subtraction of I_{dark}. It is important to remind, at this point, that the $I_{dark}(\mu A)/I_{eff}(nA)$ current ratio is 1000:1 (i.e. 60 dB, 10b) This restrictive specification automatically discards any technology mismatching sensitive topology, forcing the I_{dark} subtraction to be achieved in the transistor output node, as depicted by the current source of the referred figure.

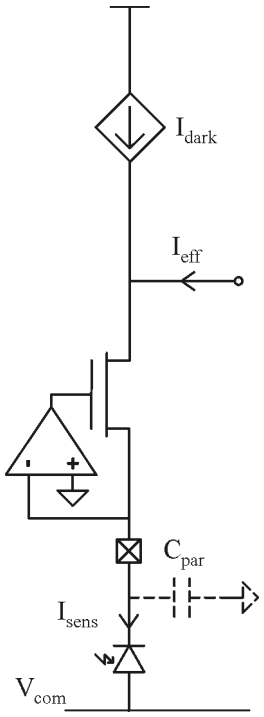


Figure 5.2 General scheme of the DPS input stage proposal

5.2.2. Compact CMOS Realization

The CMOS input capacitance compensation circuit is implemented through M1-M5 devices in Figure 5.3 and Figure 5.4. According to the general input resistance expression:

$$r_{in} = \frac{V_{in}}{I_{in}} \tag{5.1}$$

And the differential amplifier M1-M4 stage transfer function, according to the EKV [EKV95] small signal model is:

$$V_{oamp} = V_{in} g_{mg1,2} \left(r_{o1,2} \,||\, r_{o3,4} \right) = V_{in} \frac{g_{mg1,2}}{g_{md1,2} + g_{md3,4}} \tag{5.2}$$

I_{in} can be expressed as:

$$I_{in} = g_{mg5}\left(nV_{in} + V_{oamp}\right) = V_{in}g_{mg5}\left(n + \frac{g_{mg1,2}}{g_{md1,2} + g_{md3,4}}\right) \quad \textbf{(5.3)}$$

Thus, the resulting resistance is found to be:

$$r_{in} = \frac{V_{in}}{V_{in}g_{mg5}\left(n + \frac{g_{mg1,2}}{g_{md1,2} + g_{md3,4}}\right)} = \frac{1}{g_{mg5}}\frac{1}{\left(n + \frac{g_{mg1,2}}{g_{md1,2} + g_{md3,4}}\right)} \quad \textbf{(5.4)}$$

Simplifying:

$$r_{in} \simeq \frac{g_{md1,2} + g_{md3,4}}{g_{mg5}g_{mg1,2}} = \frac{n_N n_P U_t^{\,2}}{I_{sense}}\left(\lambda_N + \lambda_P\right) \quad \textbf{(5.5)}$$

Where n, U_t and λ stand for the subthreshold slope, the thermal potential and the channel length modulation factor, respectively. In practice, resistance values below kΩ can be easily obtained, increasing the upper limit of C_{par} above several pF.

The upper part of the proposed circuits performs input offset subtraction in three different ways. The left side topology of Figure 5.3 uses the Switched Current (SC) copier implemented by M6: during calibration phase (`cal`=1 and no incident radiation) I_{dark} is sampled and dynamically stored in the M6 non-linear gate capacitance (C_{dark}); just before acquisition time (`cal`=0) the latter current value is directly subtracted to I_{sens}. This structure presents the advantage to be completely insensitive to technology mismatching, since the same M6 device is in charge of both I_{dark} memorization and cancellation tasks. In order to improve the output impedance of the SC copier, the cascode M7-M9 is added.

The right side of Figure 5.3 presents a wider dynamic range variant implementation of the same concept. Removing the M9 device, and disposing the M7-M8 interconnections as depicted in the figure, a regulated cascode is obtained. The operation procedure is easily understood referring to Figure 5.3 and Figure 5.10. The low I_{bias} value force M8 (Figure 5.3), M1 (Figure 5.10) transistors to operate in the weak inversion, forward saturation region. Therefore, the M7 D-S voltage can be related:

$$V_{DS7} = \cancel{V_{DD}} - nU_t \ln\left(\frac{I_{bias}}{I_{S8}}\right) - \left[\cancel{V_{DD}} - nU_t \ln\left(\frac{I_{bias}}{I_{S1}}\right)\right] \quad \textbf{(5.6)}$$

Or simply:

$$V_{DS7} = nU_t \ln\left(\frac{I_{S8}}{I_{S1}}\right) = nU_t \ln\left(\frac{\left(\frac{W}{L}\right)_8}{\left(\frac{W}{L}\right)_1}\right) \quad \textbf{(5.7)}$$

Considering that M7 operates closely to weak inversion, saturation is achieved if (5.8) is accomplished:

$$V_{DS7} > 3(5)U_t \quad \textbf{(5.8)}$$

so:

$$\left(\frac{W}{L}\right)_8 > e^{\frac{3(5)}{n}}\left(\frac{W}{L}\right)_1 \underset{n=1.3}{\simeq} 10(50)\left(\frac{W}{L}\right)_1 \quad \textbf{(5.9)}$$

In practice, M8/M1 devices can be scaled to:

$$\left.\begin{aligned}\left(\frac{W}{L}\right)_1 &= \frac{15\mu m}{3\mu m} = 5 \\ \left(\frac{W}{L}\right)_8 &= 2\times\frac{30\mu m}{1.5\mu m} = 40\end{aligned}\right\} V_{DS7} = nU_t \ln 8 \simeq 2.7U_t \sim 68mV \quad \textbf{(5.10)}$$

as effective regulation is also extended to V_{DS7} values near saturation. This circuit is able to compensate I_{dark} values in the 0,2–5µA range, with nA resolution, at the cost of higher switched noise sensitivity.

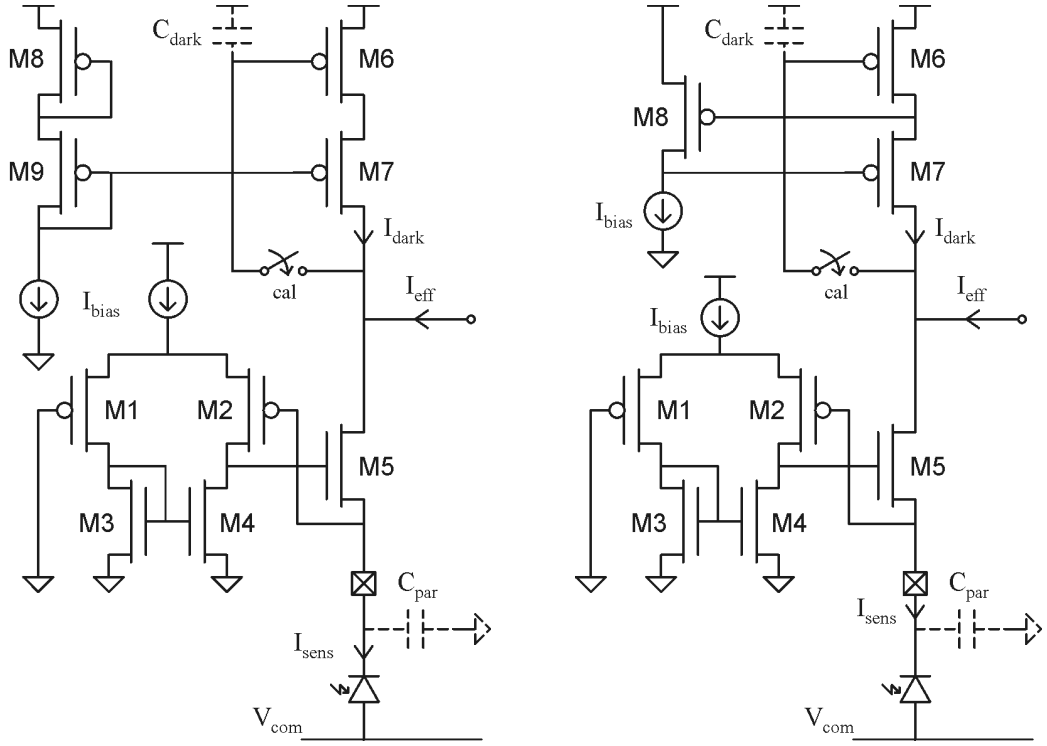


Figure 5.3 DPS CMOS input stage proposals for parasitic capacitance and offset self-compensation

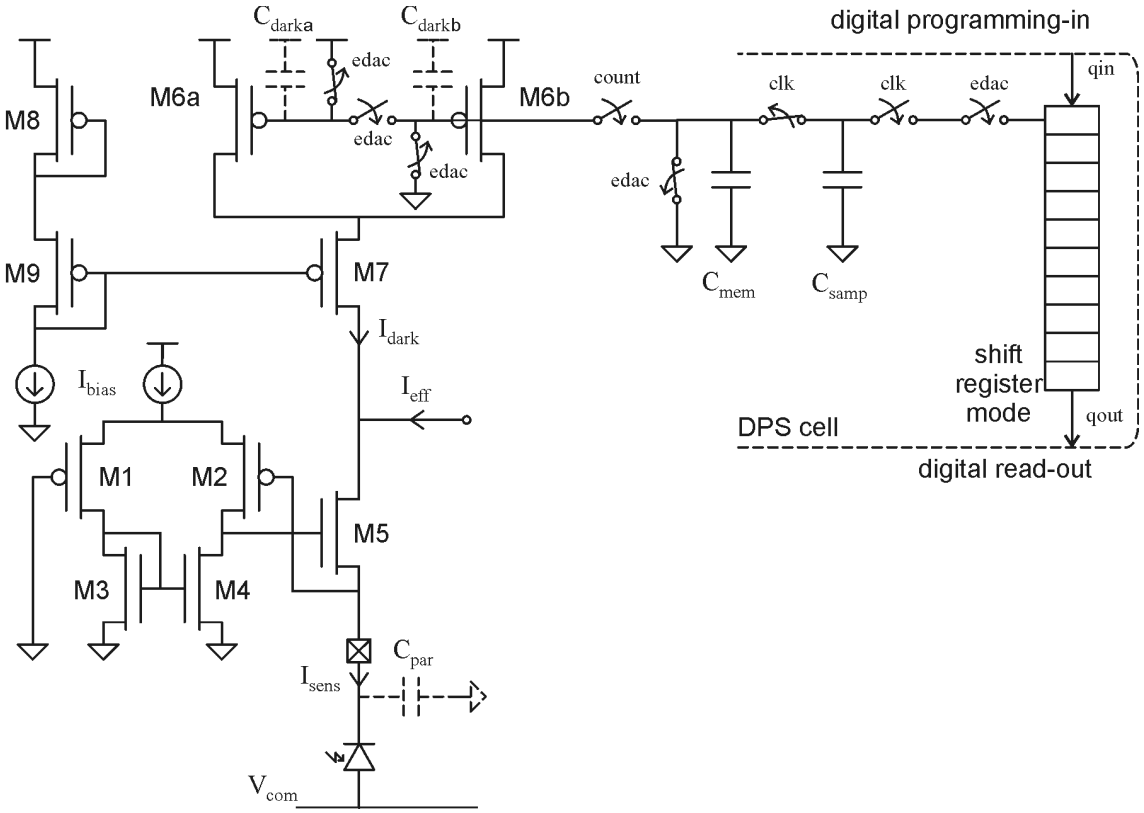


Figure 5.4 DPS CMOS input stage proposal for parasitic capacitance compensation and offset external tuning

However, input offset self-compensation requires the DPS to be periodically calibrated under zero-radiation conditions which are, in practice, really hard to grant. In order to provide I_{dark} external programming, the circuit of Figure 5.4 is conceived, where the cascoded current source located in the left-side Figure 5.3 is adapted so as the analog memory M6 will be comprised into a switched D/A converter to generate an individual DPS I_{dark} around a pre-established center value. The operation principle can be qualitatively described in three phases: during the first one (`edac`=0 and `count`=0) all capacitances are reset; in the communication phase (`edac`=1 and `count`=0) the entering code `qin` together with `clk` generate by charge redistribution a programmable voltage level in C_{mem}; finally, in the acquisition stage (`edac`=1, `count`=1 and `clk`=0) this program is combined with the pre-charge in M6a and M6b to generate a final I_{dark} control voltage that will be stored in the analog memory $C_{darka}+C_{darkb}+C_{mem}+C_{samp}$. If M6 is pre-charged to $V_{DD}/2$, charge redistribution results in:

$$V_{GB6} = V_{DD}\left[\frac{C_{dark}}{C_{dark}+C_{DAC}}\left(\frac{1}{2}+\frac{C_{DAC}}{C_{dark}}\sum_{i=1}^{N}\frac{p_{N-i}}{2^{i}}\right)-1\right] \qquad \textbf{(5.11)}$$

where V_{DD}, p and N are the supply voltage, the programming-in digital code and its bit length. DAC operation will be explained in detail in chapter 5.5.

5.3. Pulse Density Modulation

As explained in Section 4.2. , a PDM predictive ADC approach is preferred for its relaxed analog requirements and digital low-noise performance. The converter high-gain and band-limited input stage is synthesized as a first order integrator, which amplifies the low-frequency components of I_{eff} into a voltage (V_{int}) value, to be quantified at a given threshold (V_{th}) by a comparator.

5.3.1. Operation Principle

In order to achieve a fast frame rate, low values must be selected for the front analog integrator integration capacitance. In practice, intrinsic circuit capacitances can easily exceed the required resolution values compared to the chosen integrating capacitance, so the use of a capacitive trans-impedance amplifier (CTIA) is usually mandatory.

Normally, the pre-amplification and CDS low frequency noise filtering functions [HAN06] are implemented in two cascaded stages, as shown in Figure 5.5, where C_{par} and C_{int} stand for the input parasitic and integration capacitances, respectively. If CTIA noise and offset are not taken into account, the obtained V_{int} is:

$$V_{int} = V_{ref} + \frac{1}{C_{int}}\int_{0}^{T_{int}} I_{eff}\,dt \simeq V_{ref} + \frac{T_{int}}{C_{int}} I_{eff} \qquad BW_{eff}T_{int} << 1 \qquad \textbf{(5.12)}$$

where BW_{eff} refers to the I_{eff} bandwidth. Then, for a fixed threshold value of $V_{int}=V_{th}$, the resulting V_{pdm} pulse frequency is ideally determined by the expression:

$$f_{pulse\_ideal} = \frac{1}{C_{int}\left(V_{th} - V_{ref}\right)} I_{eff} \tag{5.13}$$

However, this standard topology requires the use of two capacitors, C_{int} and C_{CDS}, reducing the available pixel cell area for other tasks. In order to improve Si area-saving, the novel one-capacitor integration/CDS scheme of Figure 5.6 is proposed. Its principle of operation is the following: during frame initialization (`init`=1), the analog integrator based on $C_{int/CDS}$ is not discharged at all, but samples the offset and the low frequency noise of the first stage by the virtual short-circuit of the amplifier; once in acquisition (`init`=0), the detector quasi-static effective current I_{eff} is integrated in C_{int}, with the equivalent noise voltage compensated in the previous phase. Finally, when the integrated signal V_{int} reaches the fixed threshold V_{th}, the comparator generates a PDM signal (V_{pdm}), which is sent to a digital counter and also fed back to the first stage as the reset signal; the ideal waveforms of this operation cycle are illustrated in Figure 5.7. At the end of the frame time T_{frame}, the asynchronous A/D conversion is completed and the state of the digital counter according to this ideal operation will be:

$$w_{out\_ideal} = \frac{f_{pulse}}{f_{frame}} = \frac{T_{frame}}{C_{int}(V_{th} - V_{ref})} I_{eff} \tag{5.14}$$

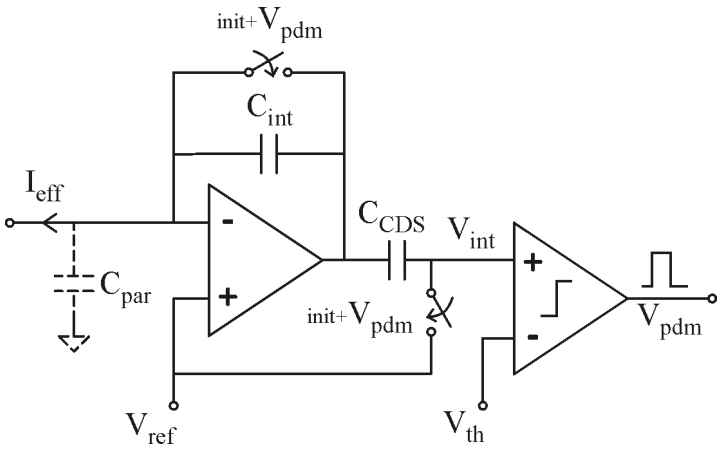


Figure 5.5 DPS classical integrator scheme for fast spike counting

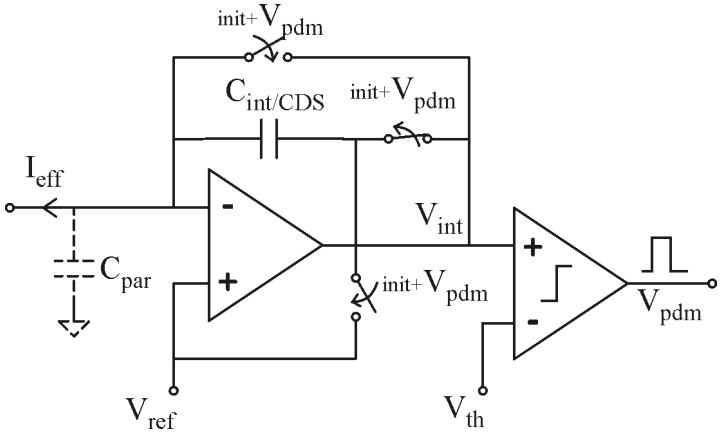


Figure 5.6 DPS one-capacitor integrator scheme for fast spike counting

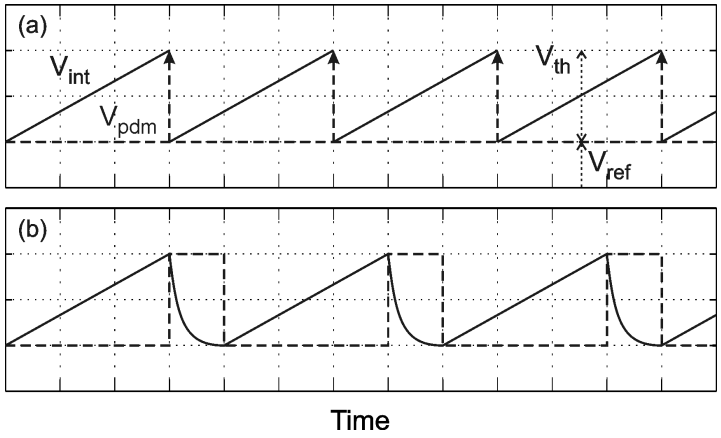


Figure 5.7 Integrator operation according to ideal (a) and one-capacitor (b) integrator schemes. Reset times not in scale

Unfortunately, due to low-current biasing levels in the analog integrator and the comparator blocks, or due to the low-voltage supply operation of switching devices, the V_{pdm} pulse duration in Figure 5.7(a) cannot be null in practice. Hence, some time is lost at each spike generation in order to reset the analog integrator, as depicted in Figure 5.7(b). According to Figure 5.6, no integration in C_{int} is possible during this event time, so the resulting spike frequency in Figure 5.7(b) is decreased compared to Figure 5.7(a). This effect is especially noticeable at full-scale of I_{eff}, where the pulse period is comparable to the reset time causing saturation of the ADC curve. Furthermore, in case of non-quasi static I_{eff} levels (e.g. particle detection applications), charge loss during reset is no longer predictable (i.e. non-compensable by digital processing) and it may be already dominant at the lower range of the ADC curve. Anyway, the reset time normally forces to waste more power in the analog blocks of the DPS in order to achieve the desired fast frame rate performance. The spike frequency also depends on T_{reset} (pulse or reset time) as described in (5.15).

$$f_{pulse\_real} = \frac{1}{T_{reset} + C_{int}\left(V_{th} - V_{ref}\right) I_{eff}} \qquad \textbf{(5.15)}$$

so, according to **(5.16)** the digital counter final value will be:

$$w_{out\_real} = \frac{f_{pulse\_real}}{f_{frame}} = \frac{T_{frame}}{T_{reset} + T_{pulse\_ideal}} = \frac{w_{out\_ideal}}{1 + \frac{T_{reset}}{T_{pulse\_ideal}}} \qquad \textbf{(5.16)}$$

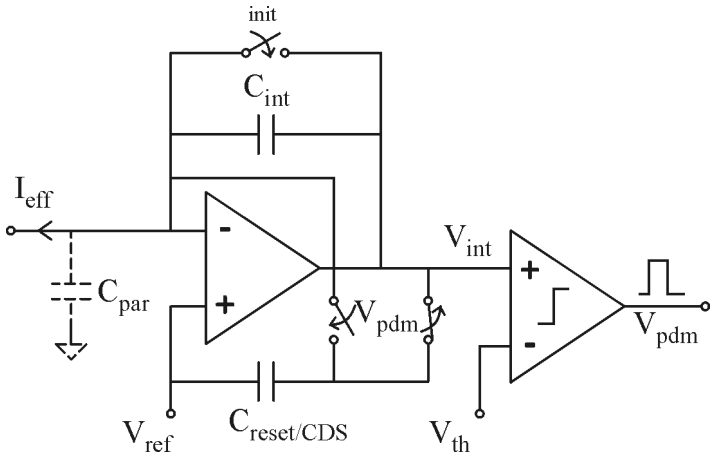


Figure 5.8 DPS reset-insensitive integrator scheme for fast spike counting

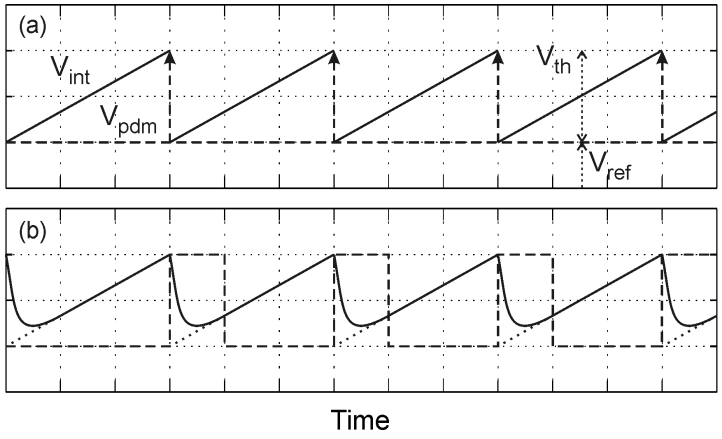


Figure 5.9 Integrator operation according to ideal (a) and reset-insensitive (b) integrator schemes. Reset times not in scale

In order to overcome reset time issues, the alternative approach of Figure 5.8 is also proposed, which does not use a hard short circuit but a novel switched-capacitor technique to reset C_{int} [MAR08b] [PAT08]. The principle of operation is as follows: during frame initialization (`init`=1), the analog integrator is reset , while $C_{reset/CDS}$ remains connected to V_{int}; once in acquisition (`init`=0), the effective sensor quasi-static current I_{eff} is integrated in C_{int} while $C_{reset/CDS}$ is tracking the offset, the low frequency noise itself of the first stage; finally, when the fixed threshold V_{th} is reached, the comparator generates a pulse, which is sent to the digital counter and cause $C_{reset/CDS}$ to be connected to the input of the analog integrator. As a result, the charge stored in C_{int} is compensated by $C_{reset/CDS}$ and the reset is performed.

However, and unlike the one-capacitor topology of Figure 5.6, this novel strategy does not block the integration in C_{int} during the event time. In fact, the proposed scheme behaves like an analog APS design from this viewpoint, as the integrator is operating in continuous time during the full frame. Thus, integration of both the charge coming from I_{eff} and from $C_{reset/CDS}$ is linearly combined in C_{int} during the reset phase, as illustrated in Figure 5.9(b). In consequence, the spike frequency is no longer dependent on the reset time and matches the ideal target of Figure 5.9(a), leading to the ideal final count expression (5.14).

Even in case of technology mismatching between C_{int} and $C_{reset/CDS}$, its effect is equivalent to small offset in V_{th}, so causing negligible gain errors compared to the process deviations of the C_{int} absolute values. In practice, just a minimum reset time is required to ensure complete charge redistribution between $C_{reset/CDS}$ and C_{int}, but its particular value is not relevant. Furthermore, since $C_{reset/CDS}$ is continuously sampling the offset and the low frequency noise of the analog integrator, it already implements the CDS function. Hence, the C_{CDS} element in Figure 5.5 can be avoided, and not more than two capacitors are finally needed.

5.3.2. Compact CMOS Realization

The reset-insensitive strategy is a completely novel topology which needs further study previously to pixel integration, so is considered to be a strong alternative for future pixel architectures. Nevertheless, a CMOS compact circuit has been designed for the second spike-counting one-capacitor integrator of Figure 5.6. Considering I_{eff} as the input generated signal, the Pulse Density Modulation CMOS circuit of Figure 5.10 is proposed, based on the one-transistor capacitive trans-impedance amplifier (CTIA) built around M9.

The main advantages of such a topology can be summarized as follows:

- ✓ Larger resolution in the offset cancellation described in Section 5.2. , since voltage variations are minimized in the input block terminal.
- ✓ Better I_{dark} analog memory retention due to the same effect, as the calibration switch is not affected by V_{int}.
- ✓ Less static power consumption due to the class-AB M9 configuration: the low I_{bias} levels (typically nA), that yield to a good resolution for small I_{eff} values, are made compatible with high full-scale values $I_{eff} \gg I_{bias}$.
- ✓ Better control on the physical design of the floating integration capacitor C_{int}, independently to parasitic capacitances present in other nodes (e.g. ground), specially for sub-pF C_{int} values.
- ✓ Larger V_{int} dynamic range and simpler implementation since ground is used as V_{ref}.

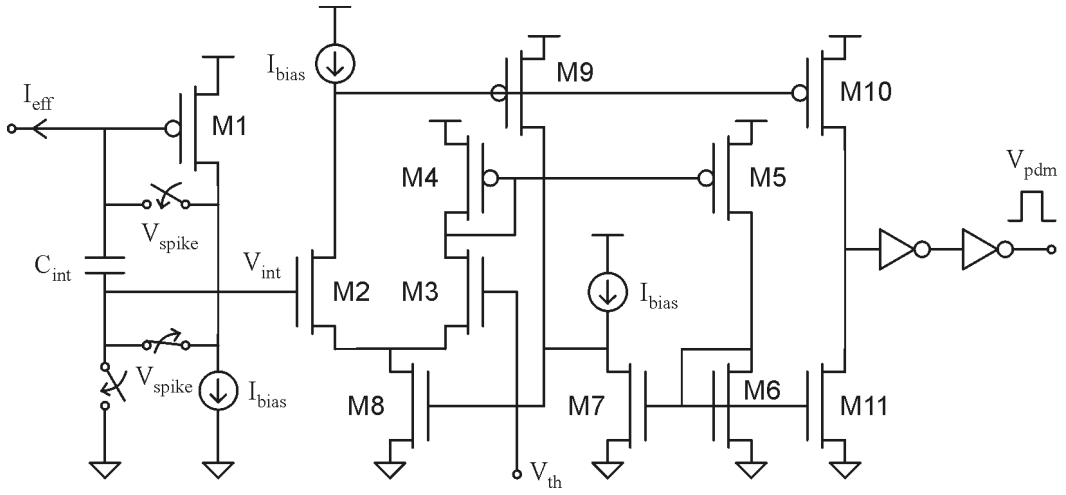


Figure 5.10 DPS CMOS analog integrator (left) and 1-bit A/D converter (right)

A novel 3-switch reset scheme is proposed for this CTIA to ensure fast reset times under low-power operation, implementing CDS by copying the output noise of M1 in C_{int} during the reset phase. The pre-amplified signal V_{int} is then quantified at 1-bit by comparator M2-M11 according to the given threshold V_{th}, as shown in Figure 5.10(right). Due to the individual tuning of V_{th}, discussed in Section 5.5. , the topology of this comparator is optimized for high input and output ranges. Furthermore, the proposed comparator combines a very low static I_{bias} with the dynamic current biasing supplied by M8 during pulse transitions. As a result, low-power operation and fast reset times are obtained. Once the spike is generated, the feedback of V_{pdm} to the CTIA causes the comparator to return to its previous state. Thus, under constant I_{eff} and zero-potential V_{ref}, and supposing depreciable reset times, the closed loop operation of Figure 5.10 leads the f_{pulse} expression (5.16) to:

$$f_{pulse} = \frac{1}{\underbrace{T_{reset}}_{\ll T_{int}} + C_{int}\left(V_{th} - \underbrace{V_{ref}}_{=0}\right) I_{eff}} = \frac{1}{C_{int} V_{th}} I_{eff} = f_{pulse\_ideal} \qquad \textbf{(5.17)}$$

5.4. Digital Filtering and Read-Out

As discussed in Section 5.1. , the PDM low-pass filtering of predictive A/D conversion is performed in the digital domain. The following requirements have been added to basic functional specs:

- ✓ Reuse as an I/O communication interface, in order to reduce the total amount of Si area employed.
- ✓ Digital integration saturation or binary overflow management

- ✓ High modularity in order to fit different dynamic range applications (i.e. selecting the number of bits N).

5.4.1. Operation Principle

Since acquisition integration is non overlapped in time with I/O communication, the reusable circuit implementation is presented in Figure 5.11, where `count` and `init` stand, respectively, for the acquisition enabling and initialization. Basically, two operation modes are configured: during acquisition (`count`=1), the binary spikes V_{spike} are digitally integrated by a ripple counter made of T-type flip-flops; during I/O communication (`count`=0), a scanning path is implemented using a shift register of D-type flip-flops, which in turn connects all the DPS cells along the row/column of the FPA. For a given frame frequency and using the PDM circuit of Figure 5.10, the ideal value of the digital word in the register at the end of each frame corresponds to the expression:

$$w_{out\_ideal} = \frac{f_{pulse\_ideal}}{f_{frame}} = \frac{T_{frame}}{C_{int}V_{th}} I_{eff} \qquad \textbf{(5.18)}$$

The double filtering nature of I_{eff} is reflected, for the same dynamic range, on the existing direct dependence between C_{int} and the counter bit resolution (N): $C_{int} \propto 2^{-N}$. Hence, 1-bit resolution increase of the latter is equivalent to reduce the integration capacitance by two. From another point of view, even though reducing C_{int} will add noise to analog integration, the digital filtering performed afterwards will compensate such effect, acting as a coarse+fine double-stage.

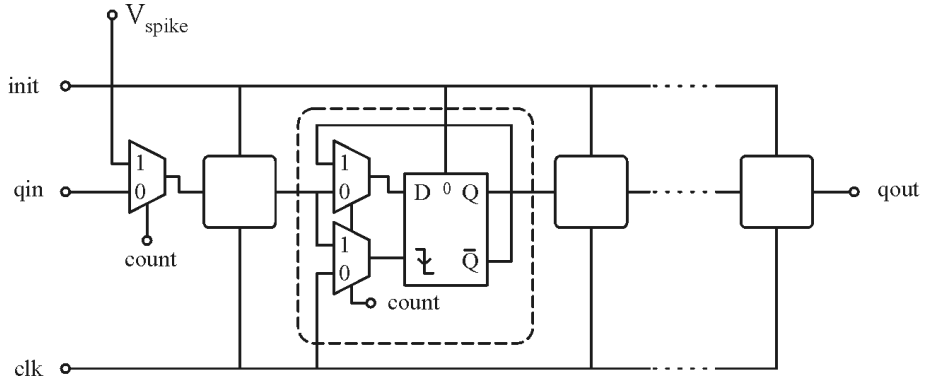


Figure 5.11 DPS shared digital integrator (as ripple counter for count=1) and I/O interface (as shift register for count=0)

5.4.2. Compact CMOS Realization

The CMOS unitary cell of the referred digital block is shown on top of Figure 5.12; the equivalent counting-mode (centre) and serial-communication (bottom) circuits are also included. During digital integration, the biestable operates as an asynchronous T-type flip-flop controlled by the falling edge of the input signal V_{pdm}, in case to be

placed as the first bit, or by the output bit of the previous flip-flop. On the other hand, serial-communication is performed through the D-type flip-flop configuration synchronized with the falling edge of the clock signal. In order to avoid invalid edge detections, clock signal rests low after the last communication period and return to high immediately before the next scan.

Both configurations use the basic static master-slave or sample & hold structure together with an additional AND initialization gate. Clock synchronism is not required in acquisition phase since the counter operates as an isolated module during this time. In fact, the T-type flip-flop is significantly simplified using direct feedback from the negative output to the master input, and the external input as the loop switch control signal.

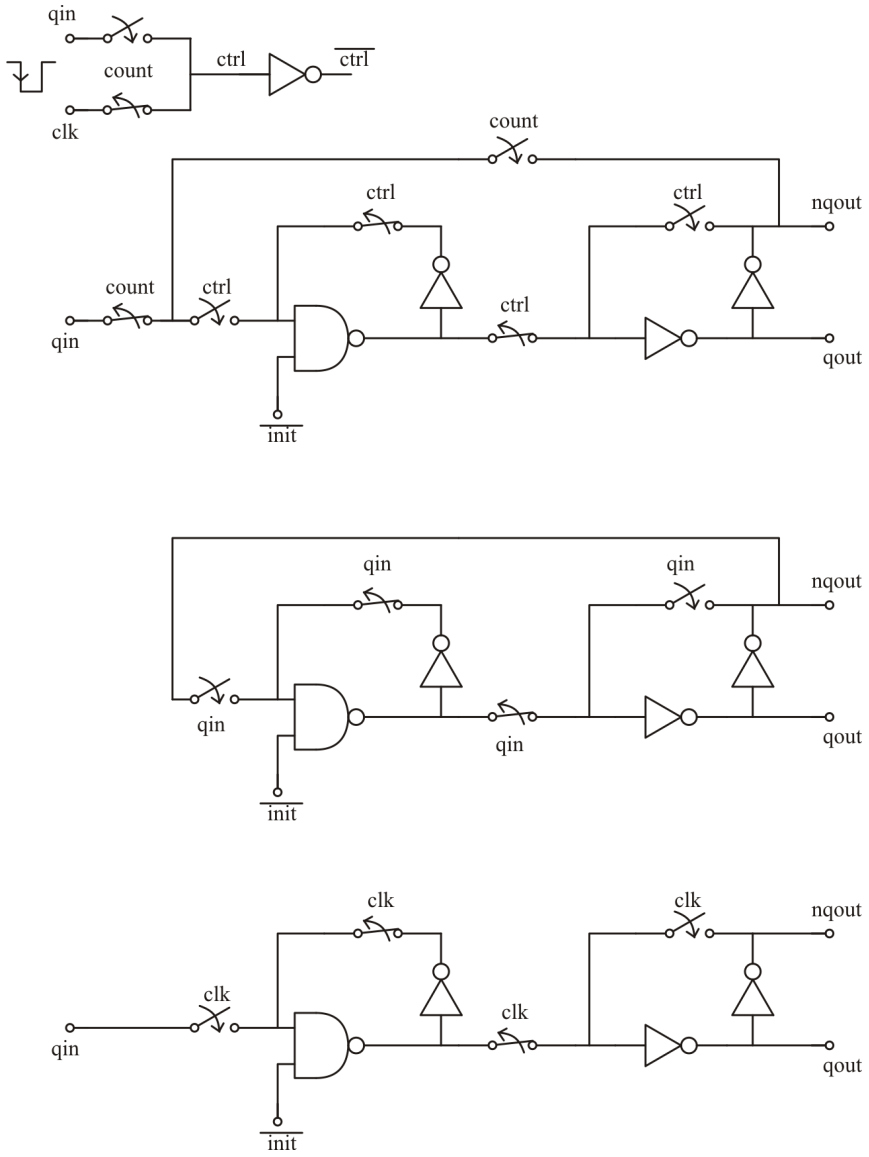


Figure 5.12 DPS CMOS basic multi-functional digital module scheme

The reset block is designed for good counter-mode compatibility, as the register initialization is only necessary when acquiring. Moreover, the shift register doesn't need any additional control signal for resetting; a serial programming of the '0' value would be enough. Initialization is finally achieved at sample time by a standard NAND, in which first master inverter is included. This topology forces a high output value to the first latch, independently to the flip-flop output state, for $\overline{init}=1$. Thus, if the slave output is '1' when reset is activated, this value will be isolated from the circuit by the NMOS block of the NAND and the second latch will be updated to '0'. In other case, the flip-flop will remain as before.

The entire block but the output inverter is implemented with minimum W-L. The aspect ratio of this single gate will be high enough to permit scanning speeds such as 10 Mbit/s, in other words, it will be able to generate enough current to charge and discharge an associated 2pF packaging capacitance in less than 100 ns.

One of the main disadvantages of the ripple counter relies on its cyclic behavior, which is open to any possible saturation or overflow of the digital integration. This effect can be avoided by the inclusion of an overflow detector (qout(i)=1 for i=1..N). Two options were considered, at first, for the detector synthesis. For a selected resolution of N bit:

- ✓ To use the classical static logic AND, together with a switch in the counter input. A non-modular proposal, with high area requirements:

$$\underbrace{N \cdot 2}_{AND} + \underbrace{2}_{switch} \text{ transistors} \qquad \textbf{(5.19)}$$

- ✓ Local overflow detection allows a distributed internal implementation for each flip-flop. This implementation can be simplified to:

$$\underbrace{N}_{\text{PMOS AND}} \text{ transistors} \qquad \textbf{(5.20)}$$

The latest technique is finally adopted as depicted in Figure 5.13. The V_{enable} signal directly disables acquisition if full-scale is reached.

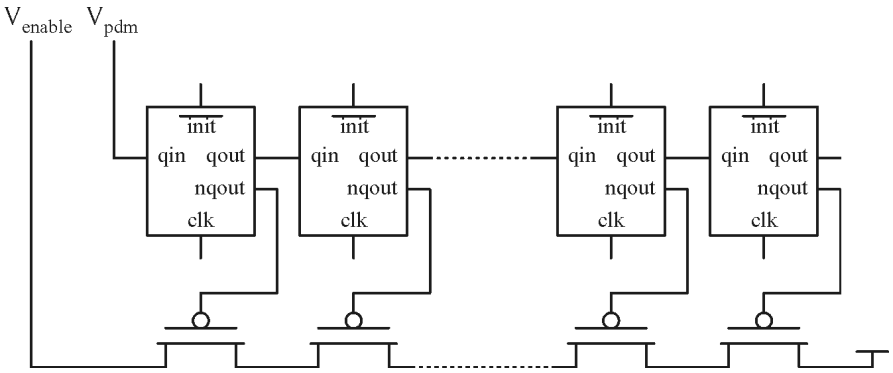


Figure 5.13 DPS digital counter overflow control scheme

5.5. Individual Gain Tuning

It is convenient to provide some individual gain programming mechanism at pixel level in order to:

- ✓ **Perform FPN cancellation:** As explained in Section 3.1.4. , geometrical, electrical and thermal mismatching between both detectors and read-out circuits origin asymmetries in transfer functions of the FPA pixels, even under uniform radiation. An external and individual sensitivity control would compensate this undesired effect.

- ✓ **Implement AGC techniques:** Even though FPN noise will not manifest, it is usually interesting to perform an Automatic Gain Control at pixel level to provide better contrast in FPA regions where the average incident radiation considerably differs (e.g. the typical problem of a dark tunnel seen from the bright outside).

5.5.1. Operation Principle

Individual gain tuning is achieved through the switched-capacitance DAC scheme of Figure 5.14. Its principle of operation is the same as in Figure 5.4, in order to obtain a programmable analog V_{th} value for increasing/decreasing pulse generation frequency.

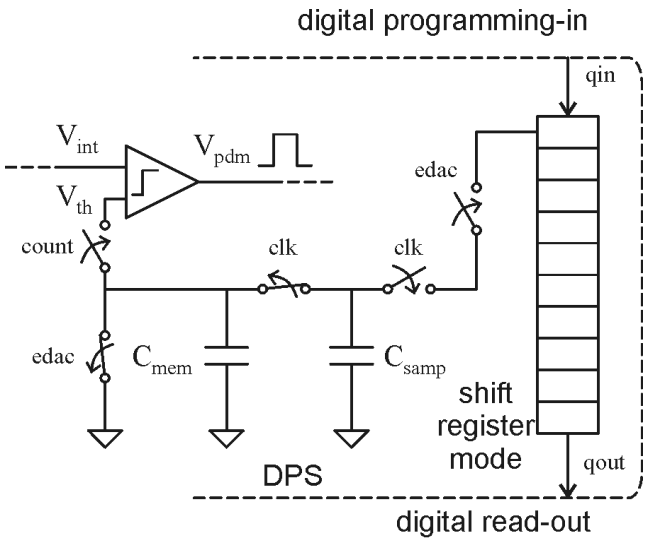


Figure 5.14 DPS individual gain tuning scheme

Circuit can be considered as a charge redistribution D/A converter. The circuit is based on the equivalence:

$$Q = CV \tag{5.21}$$

DAC operation is disabled mostly the communication phase (`edac`=0) and the V_{th} value is reset to zero. In the last N cycles of the referred phase the conversion is performed (`edac`=1): C_{samp} capacitance is sequentially pre-charged depending on the programming code bits (b_i), according to the expression:

$$V_{samp} = b_i V_{DD} \tag{5.22}$$

Being the charge cyclically redistributed with C_{mem}, so the first cycle pre-charge value is:

$$Q = C_{mem} V_{DD} \tag{5.23}$$

From now on, the output voltage will depend on the previous Q value:

$$V_{th} = \frac{Q}{C_{samp} + C_{mem}} \tag{5.24}$$

Applying (5.23) in (5.24), an instantaneous voltage value is obtained as:

$$V_{th(i)} = \frac{C_{mem} V_{DD} + V_{th(i-1)}}{C_{samp} + C_{mem}} \tag{5.25}$$

Once both capacitances are designed to have the same value:

$$V_{th(i)} = \frac{\not{C} V_{DD} + V_{th(i-1)}}{2\not{C}} = \frac{V_{DD} + V_{th(i-1)}}{2} \tag{5.26}$$

V_{th} instantaneous value is stored throughout the conversion, following the expression:

$$V_{th} = \frac{\dfrac{\dfrac{b_0 V_{DD} + V_{init}}{2} + b_1 V_{DD}}{2} + \ddots + b_{N-2} V_{DD}}{2} + b_{N-1} V_{DD}}{2} \tag{5.27}$$

Finally, during acquisition phase (`clk`=0), the V_{th} final value is saved in the equivalent C_{samp}+C_{hold} capacitance. Supposing an initial reset to zero (i.e. V_{init}=0), the DAC generates a resulting ideal threshold reference:

$$V_{th} = V_{DD} \sum_{i=1}^{N} \frac{b_{N-i}}{2^i} \quad \textbf{(5.28)}$$

The scheme of Figure 5.14 presents the next advantages:

- ✓ No extra time is required for the program-in.
- ✓ In case not to require gain tuning, it can be effortlessly disabled by fixing to '1' all the incoming `qin` (i.e. physically connecting the corresponding input pin to V_{DD}) whereas the `edac` pulse duration is limited to the last programming clock cycle, so the centered reference threshold $V_{th} = \frac{V_{DD}}{2}$ is obtained.

5.5.2. Compact CMOS Realization

The CMOS circuit of Figure 5.15 implements the switched DAC function of Figure 5.14. The employed compact charge redistribution topology is especially sensible to any current injection in both sample and hold stages. Three basic points have to be considered when designing this circuit:

- ✓ Sample and hold clock signals must not to be overlapped in order to avoid any undesired capacitance charge redistribution.
- ✓ Signal paths to sample/hold capacitors must be as clean as possible (i.e. minimum number of devices in the way).
- ✓ Charge injection and capacitive coupling phenomena of MOS switches must be compensated by the addition of dummy switches [EIC89].

As depicted in Figure 5.15, the sample input path is implemented rail-to-rail through MP and MN. Both devices are controlled by sample control logic, two (PMOS and NMOS) combinational functions with three inputs: `edac`, `qin` and `clks` (or its complementary), which stands for the DAC enable signal, the input bit signal and the non-overlapped sample clock signal. The logic circuit of Figure 5.15(top) is used in order to avoid such overlapping. The topology is based on the well-known R-S latch, where the input inverter delays the negative clock path in order to synthesize separate-in-time Q and $\overline{Q}$ transitions; a second inverter is added afterwards for the complementary gate control of switches.

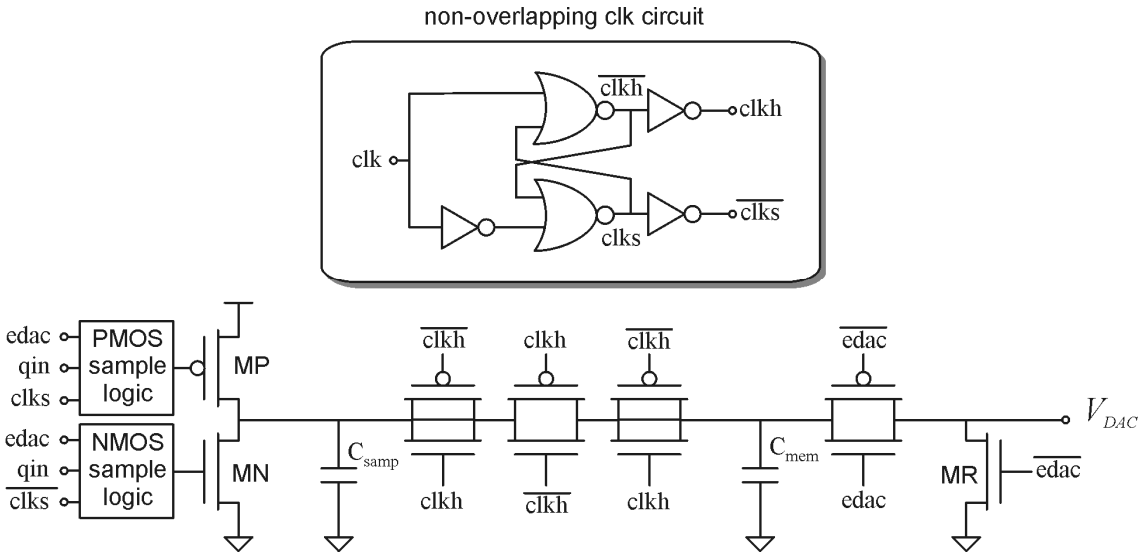


Figure 5.15 DPS DAC compact CMOS realization

All the resting switches of the main path are made using the double PMOS-NMOS topology with their corresponding half-width dummies. Minimum length is used and multiple minimum-width fingers are implemented to ensure proper matching conditions. Once previous requirements are achieved in the schematic, the physical implementation of the DAC circuit presents further challenges due to its high dependence of parasitic capacitances, which straightly unbalance the capacitance unity ratio. Hence, a fine routing capacitance adjust is necessary to accomplish with the required resolution specs. Figure 5.16 exemplifies DAC conversion results before and after parasitic adjustment, for a supply voltage of 3.3V and a 10-bit code resolution. The existing direct lineal proportionality between absolute error and charge-discharge-cycle sequence can also be appreciated.

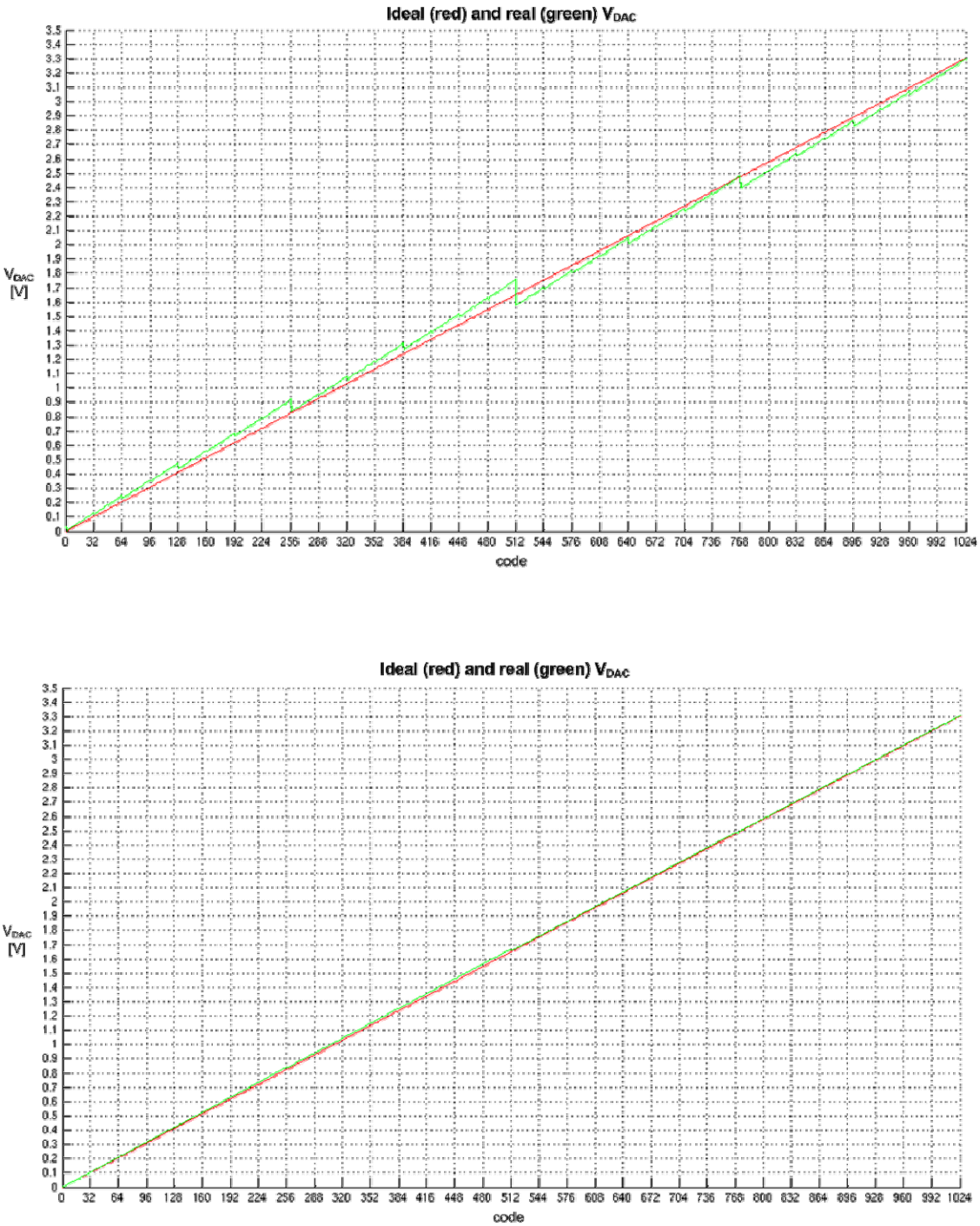


Figure 5.16 DAC linearity simulation before (top) and after (bottom) parasitic adjustment

5.6. Self-Biasing

As stated in the third chapter, mostly of the mixed DPS realizations reported in the literature generate the required I/V references at system level. The developed DPS system locally generates all biasing references. Advantages are clear:

- ✓ Common bias crosstalk avoidance between DPS cells.
- ✓ FPA technological connectivity (i.e. number of metal layers) simplification.
- ✓ Reduction of technology mismatching effects.
- ✓ Simplification of the external discrete ROIC acquisition system.

On the other hand, local bias also present new design challenges:

- ✓ Low-power locally-generated references are not easy to be generated.
- ✓ Technological dependence of the bias circuit.
- ✓ Extra pixel area required for block synthesis.

5.6.1. Operation Principle

A new Log-Companding design approach is used to allow strong supply scaling for the PTAT generator. Both I and V variables can be represented by the general signals y and x:

$$y \propto \frac{I_k}{I_S} \quad x \propto \frac{V_{ij}}{U_t} \tag{5.29}$$

where I_k stands for the physical terminal current (e.g. anode or collector), I_s corresponds to some specific current including technological, geometrical and thermal parameters. In an equivalent way, V_{ij} symbolizes the differential voltage between device terminals (e.g. anode-catode or base-emitter) normalized to the thermal potential (U_t). In fact, the specific constants of proportionality in (5.29) depend on each particular semiconductor device.

From the general device-independent y/x nomenclature described above, $x \propto V_{ij}/U_t$, so obtaining a PTAT reference is equivalent to synthesize a constant value in the compressed domain. The basic idea consists on describing the PTAT voltage generator as a Log amplifier (G) within a fixed attenuation feedback (1/P) as depicted in Figure 5.17. Due to the feedback loop, the controllable amplifier operates at forced input and output and the control port (x_{ref}) becomes the effective result.

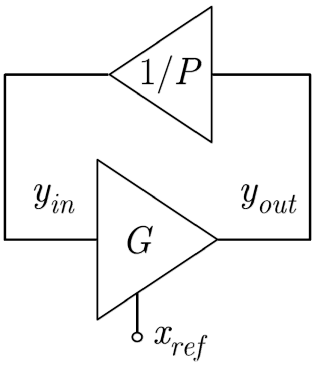


Figure 5.17 Log companding proposal for the PTAT generator

The controllable Log Amplifier is designed to exhibit the following gain:

$$G = \frac{y_{out}}{y_{in}} \doteq e^{x_{ref}} \qquad \textbf{(5.30)}$$

Moreover, feedback in Figure 5.17 sets $GP \equiv 1$, causing the control terminals of the amplifier to exhibit:

$$x_{ref} = \ln P \qquad \textbf{(5.31)}$$

so the desired PTAT reference V_{ref} is obtained due to the normalizing factor U_t in (5.29), while low voltage operation is achieved by its log compression respect to circuit currents. The corresponding current reference (I_{ref}) can be easily synthesized through an attached impedance at the control port V_{ref}. Linearity of this load element is only necessary in case of additional PTAT specifications for I_{ref}.

An important design parameter of any reference is its accuracy. In this case, the main source of uncertainty in equation (5.31) comes from the resolution of P factor. Hence, it is convenient to express the relative accuracy on x_{ref} in terms of:

$$\left(\frac{\Delta x_{ref}}{x_{ref}}\right) = \frac{\ln(1+\frac{\Delta P}{P})}{\ln P} \simeq \frac{1}{\ln P}\left(\frac{\Delta P}{P}\right) \qquad \Delta P << P \qquad \textbf{(5.32)}$$

Due to the log dependence on P, maximum x_{ref} sensitivity occurs at $P \to 1^+$, whereas x_{ref} robustness increases for $P \to \infty$. Thus, high sensitivity should be avoided in favor of maximum P ratios, so larger x_{ref} vales. In implementations of Figure 5.17, ΔP is typically associated to technology mismatching at transistor level, and must be taken into account during the design process as described downwards.

5.6.2. Compact CMOS Realization

From a circuit viewpoint, fixed feedback 1/P can be obtained through simple geometry scaling (i.e. current mirrors), while the logarithmic gain G will be synthesized through Gate Driven – Source Controlled (GD-SC) topologies. The compact CMOS circuit of Figure 5.18 takes profit on the subthreshold MOS operation principle in order to bias low-power static consumption devices [SER03]. The core of this circuit is the proportional to temperature (PTAT) voltage generator M1-M4, where the M3-M4 current mirror topology force equal current values in the branches:

$$I_{M1} = I_{M2} = I_{M3} = I_{M4} = I_{ref} \tag{5.33}$$

Supposing weak inversion, direct saturation operation of M1 and M2 (GD-SC cell), and applying Table 2.2 expressions:

$$\begin{aligned} I_{M1} &= PI_S e^{\left(\frac{V_{node}-V_{TO}}{nU_t}\right)} e^{-\left(\frac{V_{ref}}{U_t}\right)} \\ I_{M2} &= I_S e^{\left(\frac{V_{node}-V_{TO}}{nU_t}\right)} \end{aligned} \tag{5.34}$$

Thus:

$$P\,\cancel{I_S e^{\left(\frac{V_{node}-V_{TO}}{nU_t}\right)}}\, e^{-\left(\frac{V_{ref}}{U_t}\right)} = \cancel{I_S e^{\left(\frac{V_{node}-V_{TO}}{nU_t}\right)}} \tag{5.35}$$

So the resulting gain expression from (5.30) is:

$$G = \frac{Iout}{Iin} \doteq e^{\frac{V_{ref}}{U_t}} \tag{5.36}$$

Operating, (5.37) expression is obtained:

$$V_{ref} = U_t \ln P \tag{5.37}$$

It can be appreciated that the generated reference voltage is directly proportional to the absolute temperature through U_t, with a typical <100mV value for P~10.

As:

$$V_{ref} \ll V_{DD} - V_{TO} \tag{5.38}$$

For the employed technology it results:

$$I_{bias} \simeq \underbrace{\beta n}_{150\frac{\mu A}{V^2}} \underbrace{\left(\frac{W}{L}\right)_5}_{\frac{1}{3}\frac{0.4}{45}} \left(\underbrace{V_{DD}}_{3.3V} - \underbrace{V_{TO}}_{0.5V}\right) \underbrace{V_{ref}}_{\approx 60mV} < 100nA \qquad \textbf{(5.39)}$$

It is proven to be possible to obtain low voltage (mV) and low current (nA) bias values in order to reach the desired power saving.

Circuit start-up is depicted in Figure 5.19 for different power supply rise-time octaves. The minimum time is about 6µs, while there is no appreciable delay over the 16 µs input power rise-time.

5.6.3. Mismatch Study

Thanks to the high overdrive of M5, the absolute process variations of I_{bias} are reduced to β, while technology mismatching is mainly caused by P through V_{ref}. For the latter, sensitivity basically depends on the M1-M2 PTAT core threshold voltage mismatching. Since:

$$\Delta I_{ref} \propto \Delta V_{ref} \qquad \textbf{(5.40)}$$

With equations:

$$\begin{aligned} V_{ref} &= U_t \ln P \\ \Delta P &\ll P \end{aligned} \qquad \textbf{(5.41)}$$

It can be written:

$$\begin{aligned} \Delta V_{ref} &= U_t \left[\ln\left(P+\Delta P\right) - \ln P\right] = U_t \ln\left(1+\frac{\Delta P}{P}\right) \\ \Delta V_{ref} &\simeq U_t \frac{\Delta P}{P} \end{aligned} \qquad \textbf{(5.42)}$$

Otherwise, Pelgrom's law states:

$$\sigma\left(\frac{\Delta P}{P}\right) \simeq \frac{\sigma(V_{TO})}{nU_t} = \frac{1}{\sqrt{(WL)_{1,2}}} \frac{A_{V_{TO}}}{nV_{ref}} \qquad \textbf{(5.43)}$$

where W, L are, in that order, the transistor width and length, and A_{VTO} stands for the threshold voltage mismatching constant. Therefore, absolute and relative voltage variance can be expressed as:

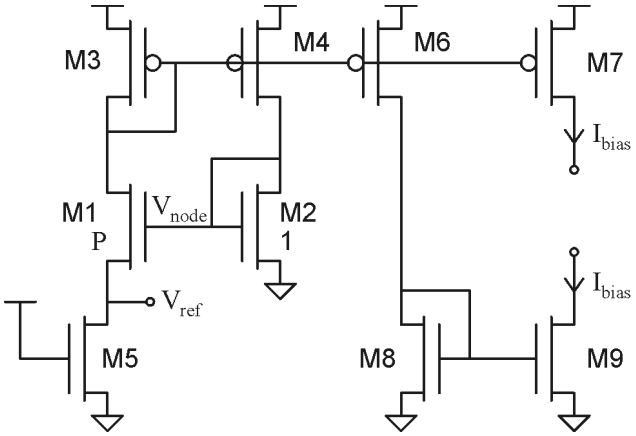


Figure 5.18 DPS CMOS built-in generator

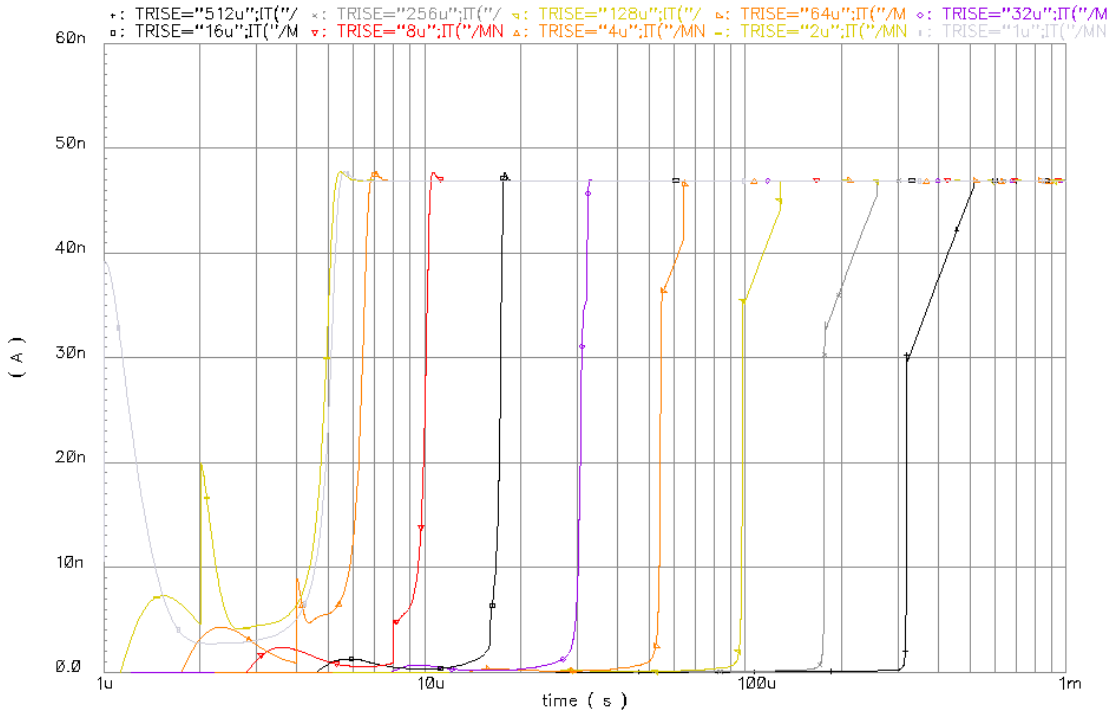


Figure 5.19 PTAT start-up parametrical simulation for a variable power supply rise-time

$$\sigma\left(\Delta V_{ref}\right)=\frac{1}{\sqrt{(WL)_{1,2}}}\frac{A_{V_{TO}}}{n} \tag{5.44}$$

$$\sigma\left(\frac{\Delta V_{ref}}{V_{ref}}\right)=\frac{1}{\sqrt{(WL)_{1,2}}}\frac{A_{V_{TO}}}{nV_{ref}} \tag{5.45}$$

So absolute variance only depends on the device area (WL), whereas relative is inversely proportional on P. It is obvious that such sensitivity can be improved if both higher V_{ref} values ($P \gg 1$) and larger M1, M2 devices are chosen.

$A_{V_{TO}}$ values for the AMS C35 CMOS process [AMS03] are:

$$A_{V_{TO}}\begin{cases} PMOS \rightarrow 16mV\,\mu m \\ NMOS \rightarrow 9.6mV\,\mu m \end{cases} \tag{5.46}$$

so device contributions can be balanced as follows:

$$\frac{WL_{PMOS}}{WL_{NMOS}}=\left(\frac{16}{9.6}\right)^2=2.78\sim\boxed{3} \tag{5.47}$$

Hence:

$$\left(\frac{W}{L}\right)_{NMOS}=\frac{1\mu m}{1\mu m}\;\Leftrightarrow\;\left(\frac{W}{L}\right)_{PMOS}=\frac{1\mu m}{3\mu m} \tag{5.48}$$

where the 3:1 ratio is established lengthen the transistor channel to optimize the PSRR.

Figure 5.20 contains the PSRR characterization of V_{ref} and I_{bias}. V_{ref} is the most sensible variable leading to values slightly over the 50 dB for a cut-off frequency of 50 kHz, while I_{bias} is almost independent to supply variations.

Figure 5.21 shows the result of a 1000-samples V_{ref}, I_{bias} Montecarlo technology mismatching analysis of the PTAT, for P=10, and T=27ºC. Both variables have a Gaussian behavior and, as previously explained, V_{ref} is affected by major dispersion. Process deviation analysis results for same conditions are depicted in Figure 5.22, whereas mixed simulation results in Figure 5.23 statistics. As expected, process variations have more influence over I_{bias}, due to β divergences, and distributions are close to being uniform. Yellow boxes stands for sample grouping, while orange is used to plot the approximate probability density function.

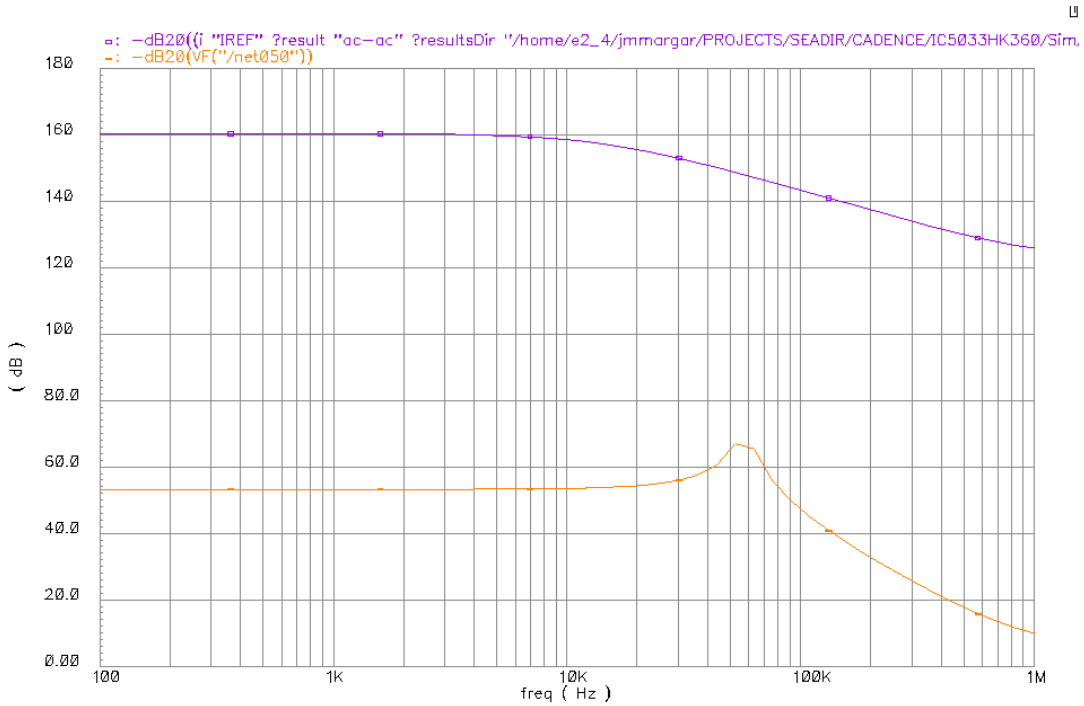


Figure 5.20 PSRR characterization of V_{ref} (lilac) and I_{bias} (orange)

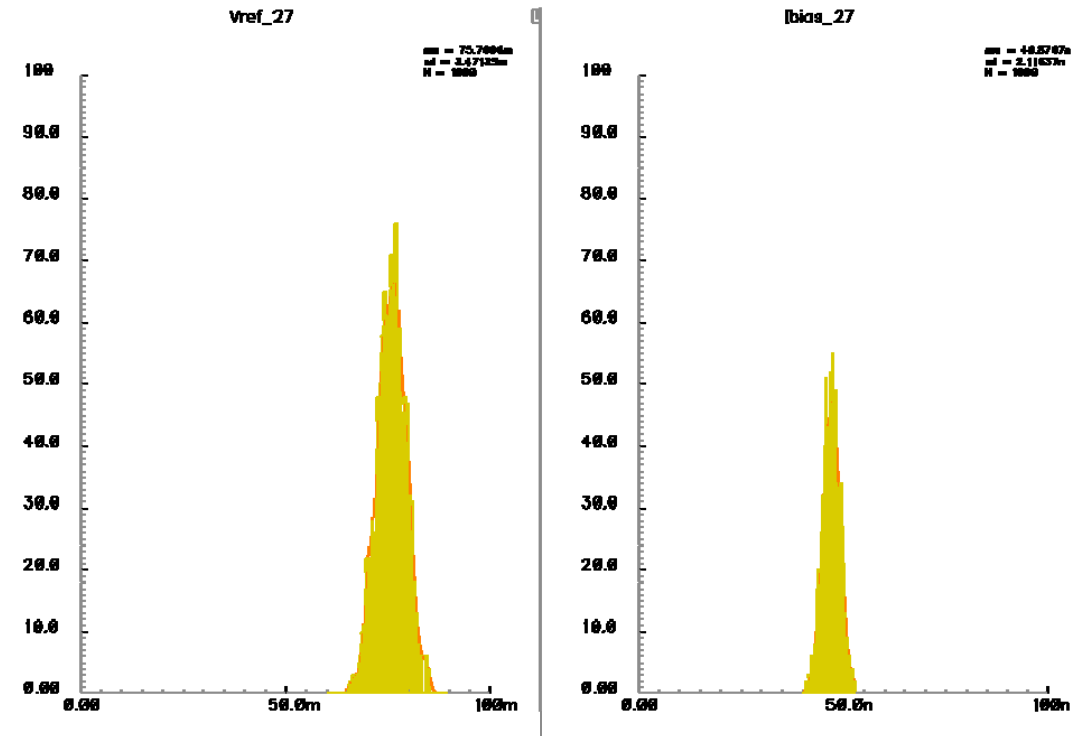


Figure 5.21 Montecarlo histogram of the V_{ref} and I_{bias} technology mismatching analysis

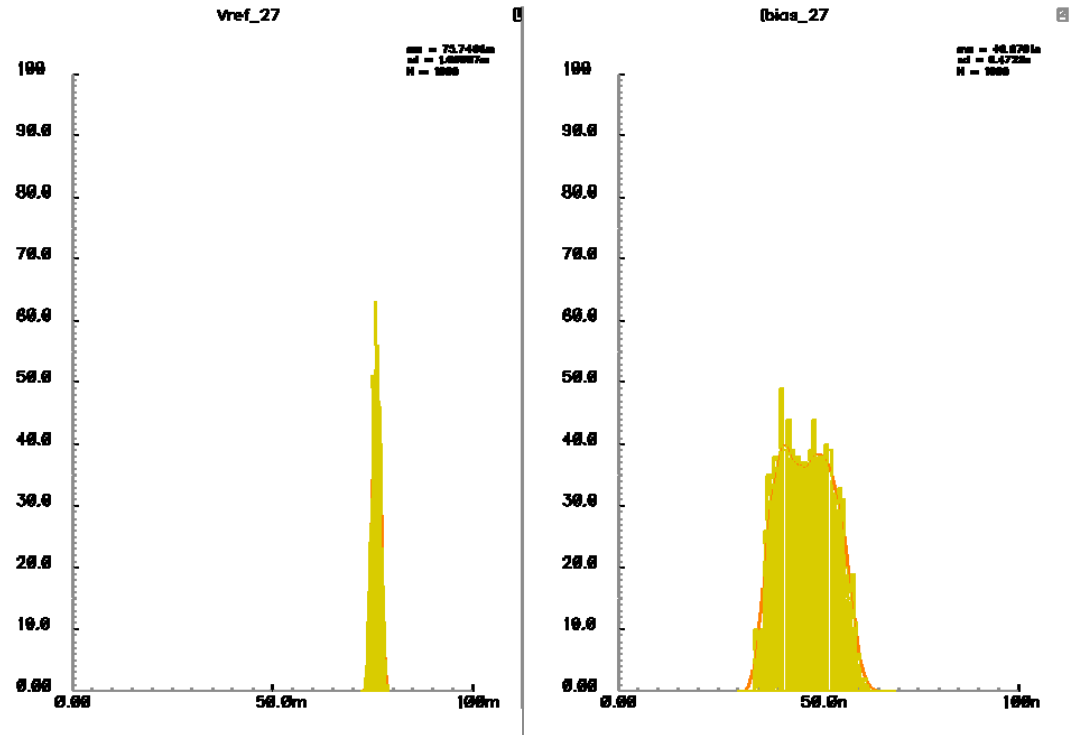


Figure 5.22 Montecarlo histogram of the V_{ref} and I_{bias} process deviation analysis

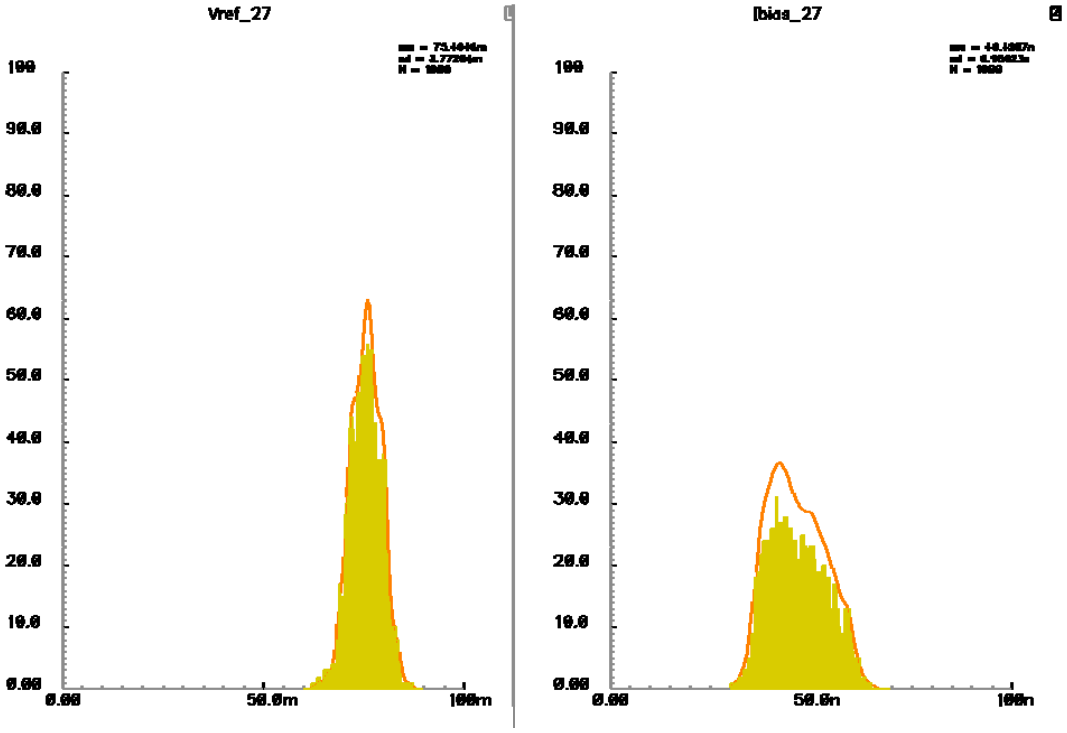


Figure 5.23 Montecarlo histogram of the V_{ref} and I_{bias}, for a mixed technology mismatching - process deviation analysis

Chapter 6

Industrial Application: A Low-Power and Fully Tunable Digital Imager for Uncooled IR Fast Cameras

This chapter presents industrial FPA designs in which all the new circuit techniques proposed in this work are applied. The novel CMOS topologies for self-biasing, input conditioning, mixed A/D integration and I/O communication are used here to implement different pixel, matrix size monolithic and hybrid FPAs for strategic customers. Overall specifications for the ROIC are described as long as the experimental results for the full-custom synthesis. Both test vehicle design and procedure are also explained.

6.1. Concept and Specifications

This Section describes in brief the development of SEADIR, a camera processing core for uncooled IR fast imaging, as a complete application example for all the proposed FPA construction strategies and the basic building blocks presented, respectively, along Chapter 4 and Chapter 5. This project is a join venture between NIT, the industrial customer exploiting the IR PbSe based detector technology developed at CIDA, and cnm (Centre Nacional de Microelectrònica – CSIC), as the design center.

The customer request consists on the development of a fully-digital, low-power ROIC and its associated modular hybrid FPA interface. As described in the design proposal of Chapter 3, the required pixel will operate at supply voltages of 3.3 V under a very low-current consumption. Moreover, electrical performance and programmable capabilities of the resulting ASIC must fit operational requirements, all using a 0.35µm,

- ✓ Local bias
- ✓ Input conditioning (Offset cancellation and parasitic capacitance compensation)
- ✓ A/D Conversion Digital-only
- ✓ I/O interface
- ✓ Individual gain tuning

And must accomplish with the overall specs detailed in Table 6.1:

Description	Value	Units
Dark current range	0.5-2	µA
Maximum input capacitance	>10	pF
Signal range	1-1000	nA
Integration time	1	ms
Program-in/read-out speed	10	Mbps
Supply voltage	3.3	V
Power consumption	<10	µW
Size	<200x200	µm
Read-out resolution	>8	bit

Table 6.1 Operational specs for the industrial DPS design

At present, three main layout realizations of the DPS have been developed for the selected application [MAR07] [MAR08a]. A test vehicle is created for each version, and experimental characterization is performed as a physical validation stage. Matricial ROIC structures are also integrated for the two (CM and MH) lines of work, and sent to the detector supplier in order to verify full system performance. The current goal is to confirm the feasibility of such a design in order to obtain even more compact and reliable future generations.

6.2. Full-Custom FPA Implementation

Once the specifications for each stage are set, all the novel CMOS circuit techniques proposed in the previous chapter are used in the synthesis of each DPS block. Accurate layout procedure is applied on physical implementation, as it has a strong influence on analog circuits. Special emphasis is dispensed to the mismatching reduction of parameter V_{TO} in order to reduce the total FPN, with even a harder influence in the MOS weak inversion region of operation. Device perimeter, substrate orientation, surrounding layers and assembly gradients are also effects which must not be overlooked, as they can considerably vary the desired system behavior. Another relevant error source is switching-noise coupling from digital to analog circuits, especially in low-voltage designs.

Hence, full-custom design work focuses on reduction of the previous phenomena; device mismatching is prevented using the general techniques of Table 2.6, whereas the latter is minimized through the following rules:

- ✓ Use of guard rings to isolate analog and digital circuits; these stacked contacts perform their function by collecting the leakage currents.
- ✓ Avoidance of analog-digital crosstalk, in order to reduce capacitive coupling. Therefore, maximum inter-path distance is desired, with special accent to high impedance nodes and high-frequency switching signals.
- ✓ Independent supply of analog and digital circuits from power pad. In this way, perturbations related to transient current consumption peaks are reduced since both power paths don't share their equivalent series resistance.

All the existing pixel generations adopted prior recommendations; their features are explained in the next lines.

6.2.1. Generation 0: The First Prototype

Conceived as a first dummy prototype, the zero-generation DPS was designed as an overall synchronous strategy concept demonstrator. Based on the structure of Figure 6.1(top), this initial version includes the dark current self-cancellation schemes described in Section 5.2.2. , together with preliminary, simple CMOS circuit implementations in order to validate the conceived general architecture. The simplified CMOS topology used for pulse density modulation is depicted in Figure 6.1(bottom). Note how a simple double-switch scheme is employed, whereas pulse generation is achieved through the regenerative comparator M14-M17.

The DPS cells of this library share the basic design parameters of Table 6.2, the I/O diagram of Table 6.3, as well as the same digital protocol shown in the chronogram of Figure 6.2, where X, p and w stand for the number of serially-connected DPSs, typically the width or height of the FPA, the length of the programming word and of the reading word, respectively.

The layout of the cascoded offset self-compensation DPS cell is shown in Figure 6.3. This early scheme was oriented to hybridization, which permitted to use the last metal not only for detector inter-connection but for internal routing. The entire design is then integrated to obtain the minimum operative pixel-size layout in order to get a first impression about both area-size limits and performance of the conceived global architecture. Thus, a reduced number of elements are employed in the synthesis, yielding to final dimensions slightly smaller than 100x100µm.

Based on the initial design experience, the FPA-oriented Compact-Monolithic (1st-generation) and Modular-Hybrid (2^{nd}-generation) versions of the active pixel were released. Both designs correct the weak points observed in 0-generation zero tests (see Section 6.3.) and adapt their pitch to updated detector dimensions.

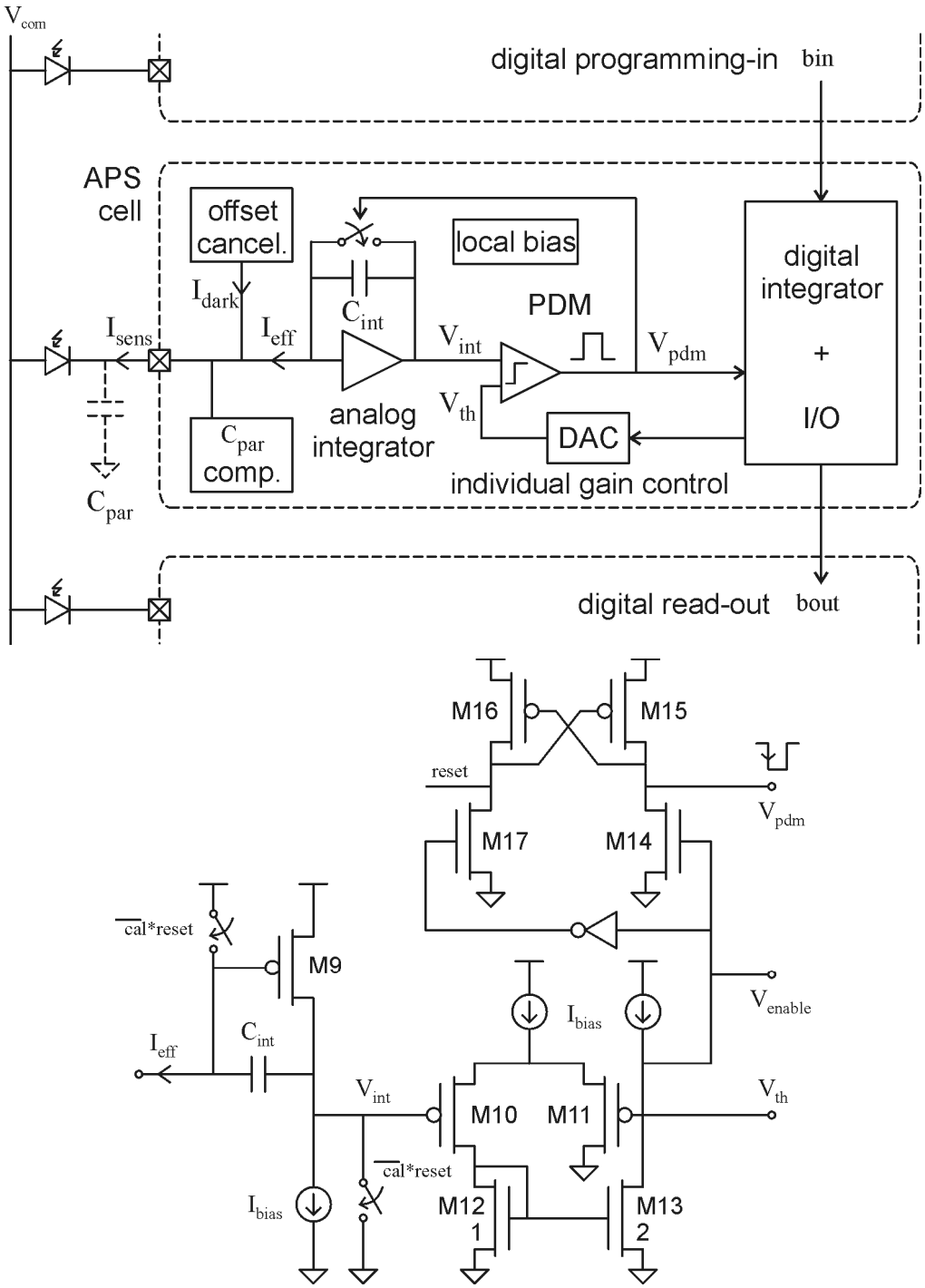


Figure 6.1 Generation 0 DPS global scheme (top) & pulse density modulation CMOS topology (bottom).

Variable	Value	Units
I_{bias}	60	nA
C_{int}	0.5	pF
$C_{mem,samp}$	100	fF
N	10	bit
P	12	-

Table 6.2 Zero-generation DPSs design parameters

Name	Type	Direction	Comments
vdda/d	P	-	Analog/digital power
gnda/d	P	-	Analog/digital power
cal	D	I	I_{dark} calibration enable
clk	D	I	Read-out clock (at falling edge)
count	D	I	Acquisition/$\overline{\text{reading}}$ selector and analog integration initialization
edac	D	I	V_{th} programming enable
ninit	D	I	Digital integration initialization (active at low)
qin	D	I	Serial communications input
qout	D	O	Serial communications output

Table 6.3 Zero-generation DPSs I/O (P-Power, D-Digital, I-Input, O-Output)

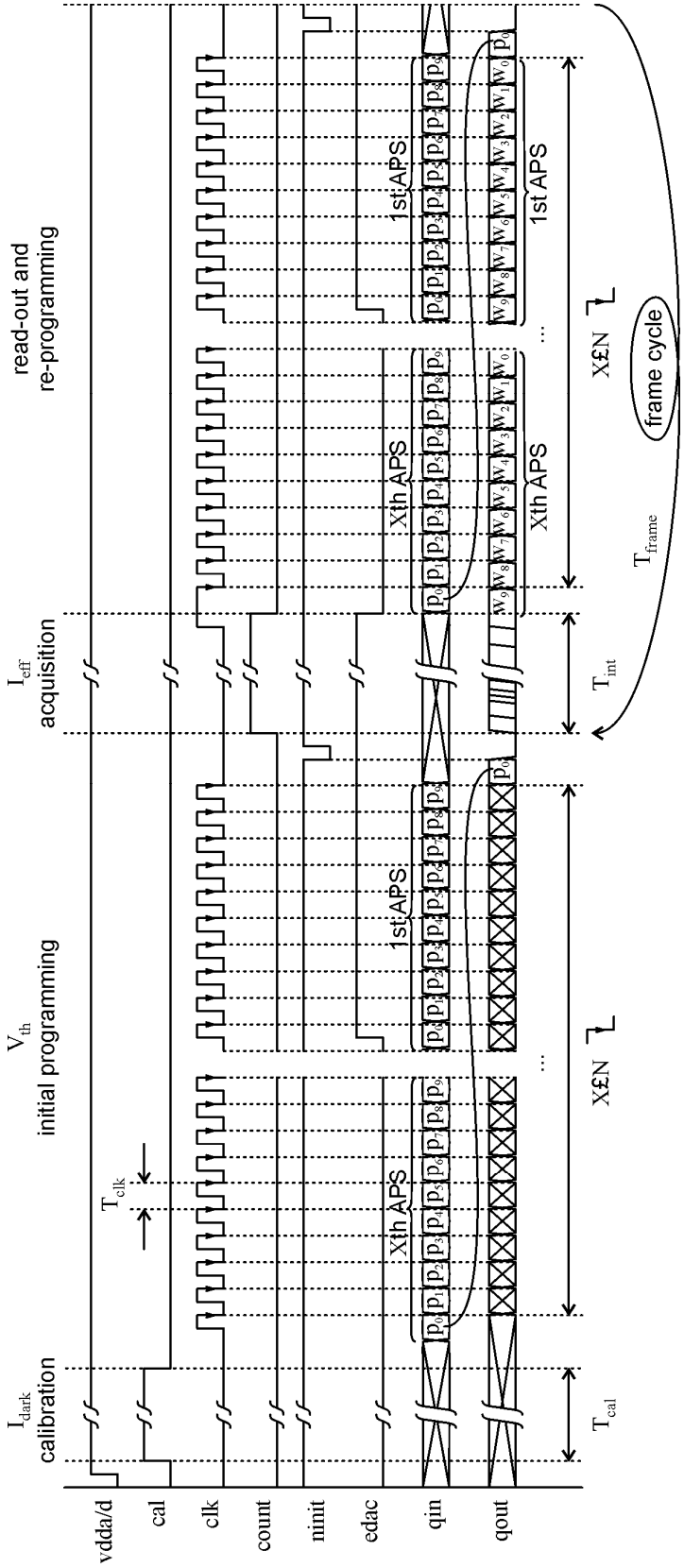


Figure 6.2 Zero-generation DPSs common control chronogram (example for N=10, typically $T_{cal} \simeq 1\text{ms}$, $T_{int} \simeq 1\text{ms}$ and $T_{clk} \simeq 100\text{ns}$)

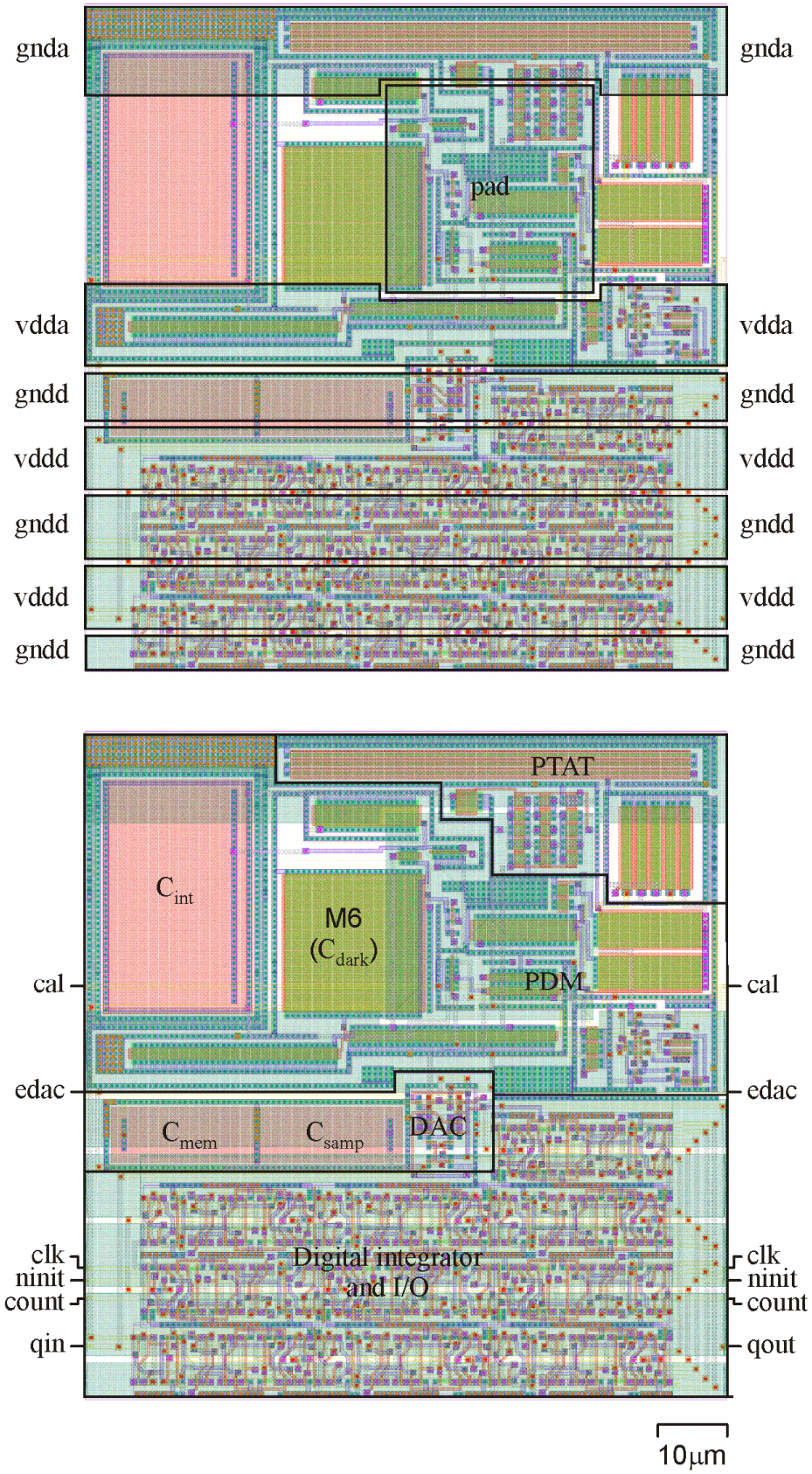


Figure 6.3 Physical layout of a zero-generation DPS cell. Metal-4 power lines (top) and metal-3 digital I/O, basic blocks (bottom)

6.2.2. Generation 1: The Compact Monolithic FPA

The first-generation DPS (Figure 6.4) is intended for post-processing the PbSe sensor on top of the CMOS circuit in order to obtain a monolithic IR imager. For such a purpose, the top metal layer of the CMOS technology is entirely devoted to define the two terminals of the PbSe detector (Figure 6.7): the grille common bias V_{com} and the inverted U-shape individual terminal collecting I_{sens}; the bonding aperture has a width of 20µm, whereas the resulting metal shape is a little wider as pointed in the design rules. In this case, pixel pitch is limited by the loss of the fourth metal level for the CMOS layout design, and by the lithography of the sensor post-processing itself (200x200µm).

In this generation, DPS integrates the dark current external compensation topology of Figure 5.4, through the inclusion of an additional switched-DAC, and all the remaining ultimate compact CMOS block realizations described in Chapter 5. The larger pixel pitch is used to include the dual DAC approach and to improve DACs reliability (i.e. increasing by three its capacitance values and improving matching between C_{samp} and C_{mem}), as well as to introduce some layout adjustments (i.e. providing better isolation between analog and digital circuits, and reducing biasing noise coupling by the inclusion of additional current mirror stages). Both 1st and 2nd generations share Table 6.4 parameters, as well as the I/O diagram of Table 6.5.

Every pixel of this library can be operated as explained in Figure 6.6. The procedure consists of two main phases: an initial I_{dark} tuning, which performs a dichotomic search of the offset compensation value for a given mid-scale V_{th}, and the basic dual-frame routine, that alternatively programs the two variables for every standard acquisition cycle (Figure 6.5). The preliminary tuning only requires N iterations, where N stands for the number of I_{dark} programming bits. In case further compensation will be required, offset variations would only affect the LSB and so even less iterations would be needed.

The layout of the 200x200µm DPS cell is depicted in Figure 6.8, including both detector bias terminals. The double-DAC scheme can also be noticed, in which common-centroid techniques and dummy capacitances are used for the physical implementation. The first FPA system is constructed as the 16x16 1st-generation DPS matrix of Figure 6.9, with a pitch of 200µm, and approximate total dimensions of 3.4mm x 4.8mm. Since inter-DPS communication is performed at row level, the I/O wire-bonding pads are distributed at both matrix sides (see Figure 6.10), where the rows can be interlaced depending on final application specifications. The I/O diagram is almost the same as detailed in Table 6.5, with exception of the multiple sixteen communication lines (as many as the integrated matrix rows) and the inclusion of the V_{com} signal in order to bias the PbSe sensor.

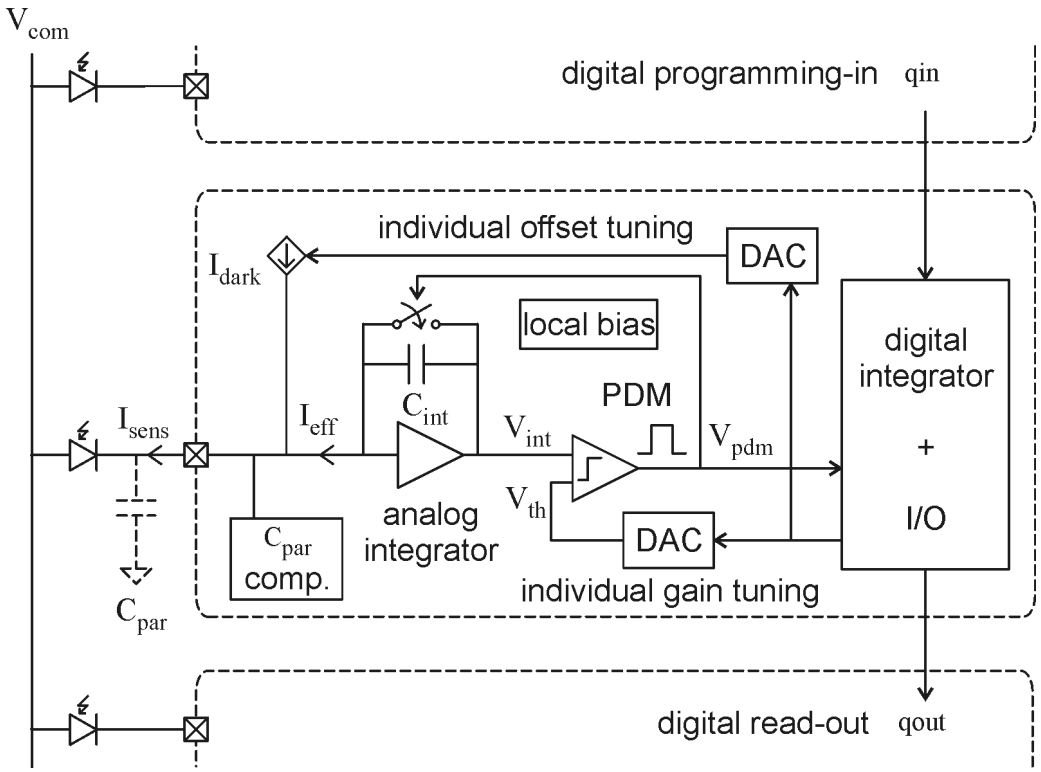


Figure 6.4 1st generation DPS global scheme

Variable	Value	Units
$\mathbf{I_{bias}}$	60	nA
$\mathbf{C_{int}}$	0.5	pF
$\mathbf{C_{mem,samp}}$	300	fF
N	10	bit
P	12	-

Table 6.4 1st/2nd -generation DPSs design parameters

Name	Type	Direction	Comments
vdda/d	P	-	Analog/digital power
gnda/d	P	-	Analog/digital power
cal	D	I	$I_{dark}/\overline{V_{th}}$ programming selector
clk	D	I	Read-out clock (at falling edge)
count	D	I	Acquisition/$\overline{\text{reading}}$ selector and analog integration initialization
edac	D	I	I_{dark}, V_{th} programming enable
ninit	D	I	Digital integration initialization (active at low)
qin	D	I	Serial communications input
qout	D	O	Serial communications output

Table 6.5 1st/2nd-generation DPSs I/O (P-Power, D-Digital, I-Input, O-Output)

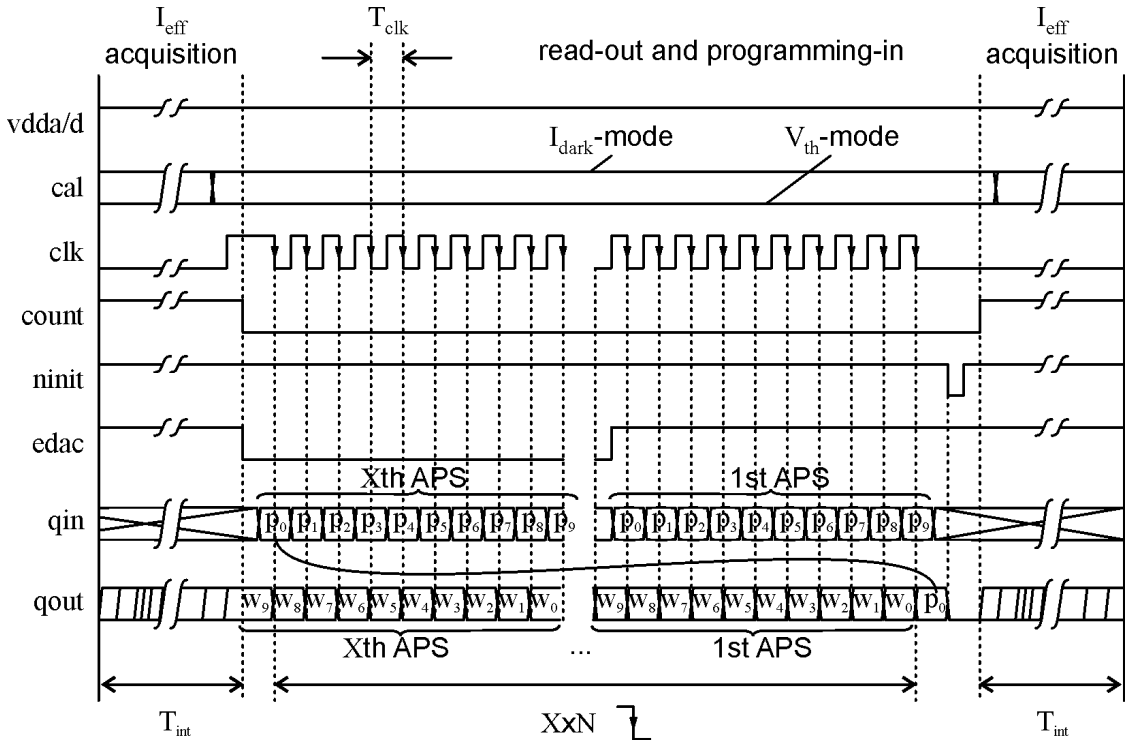


Figure 6.5 1st/2nd-generation DPSs control chronogram (example for N=10, typically $T_{int} \simeq 1\text{ms}$ and $T_{clk} \simeq 100\text{ns}$)

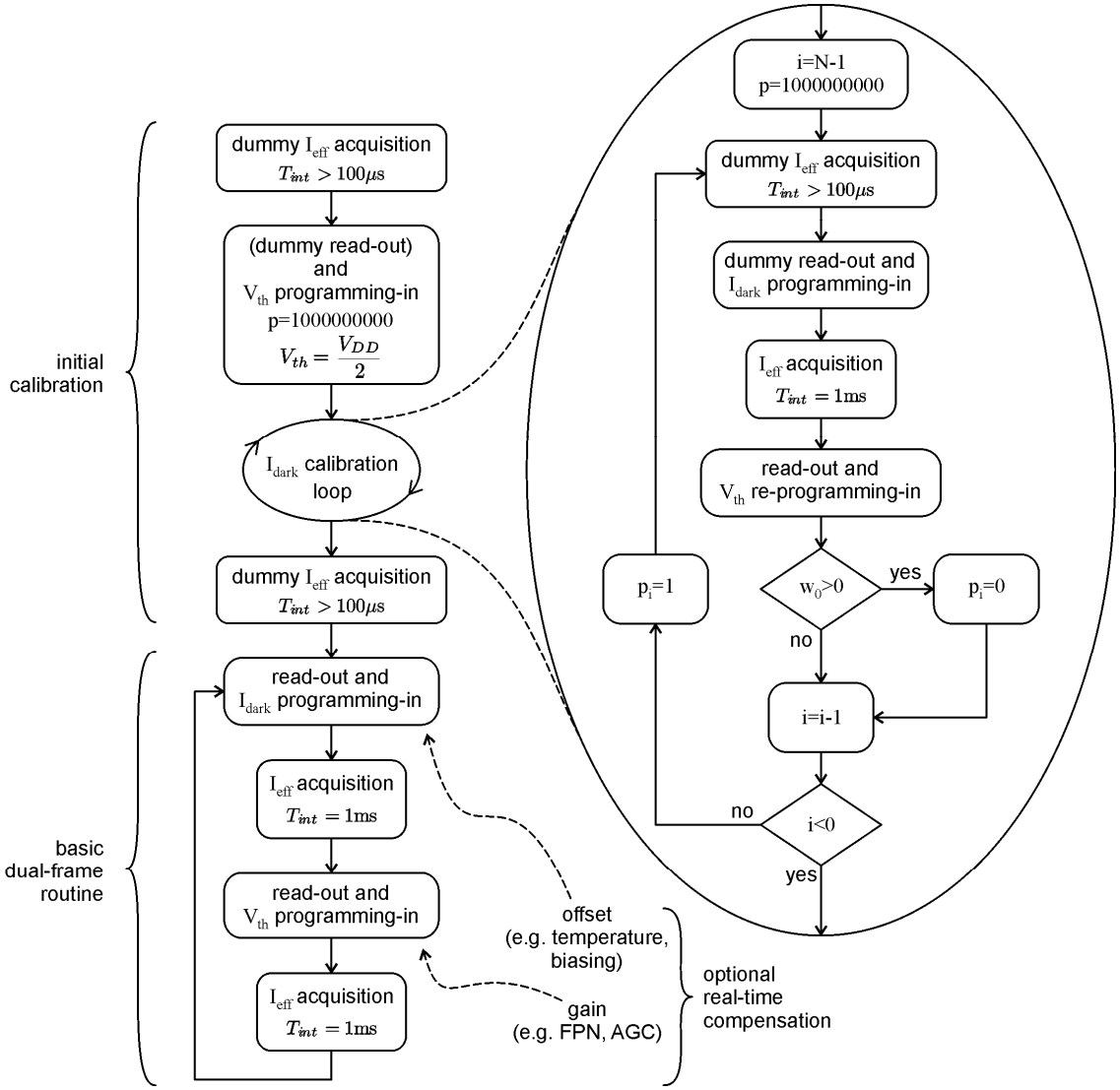


Figure 6.6 General 1st/2nd-generation DPS operation routine proposal

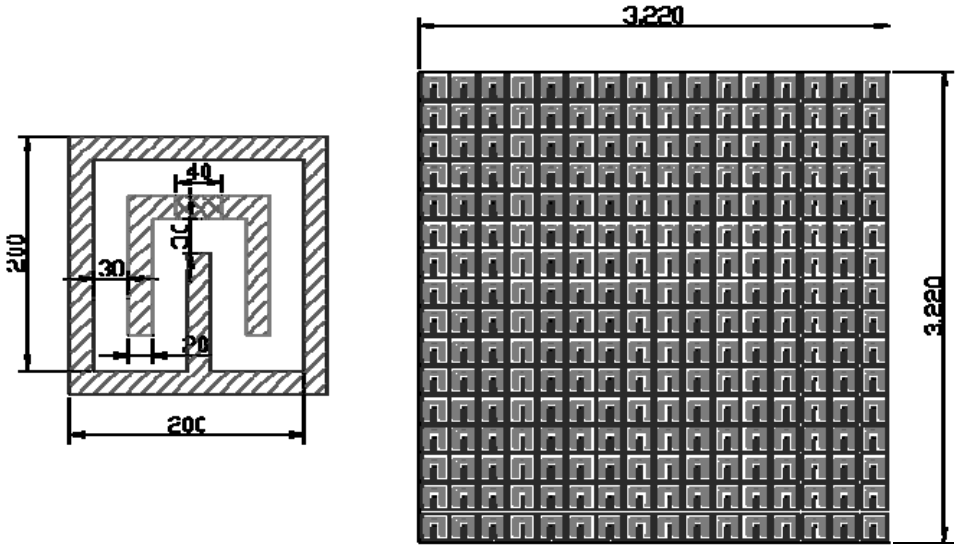


Figure 6.7 1st -generation DPS top metal apertures layout required to contact the PbSe detector

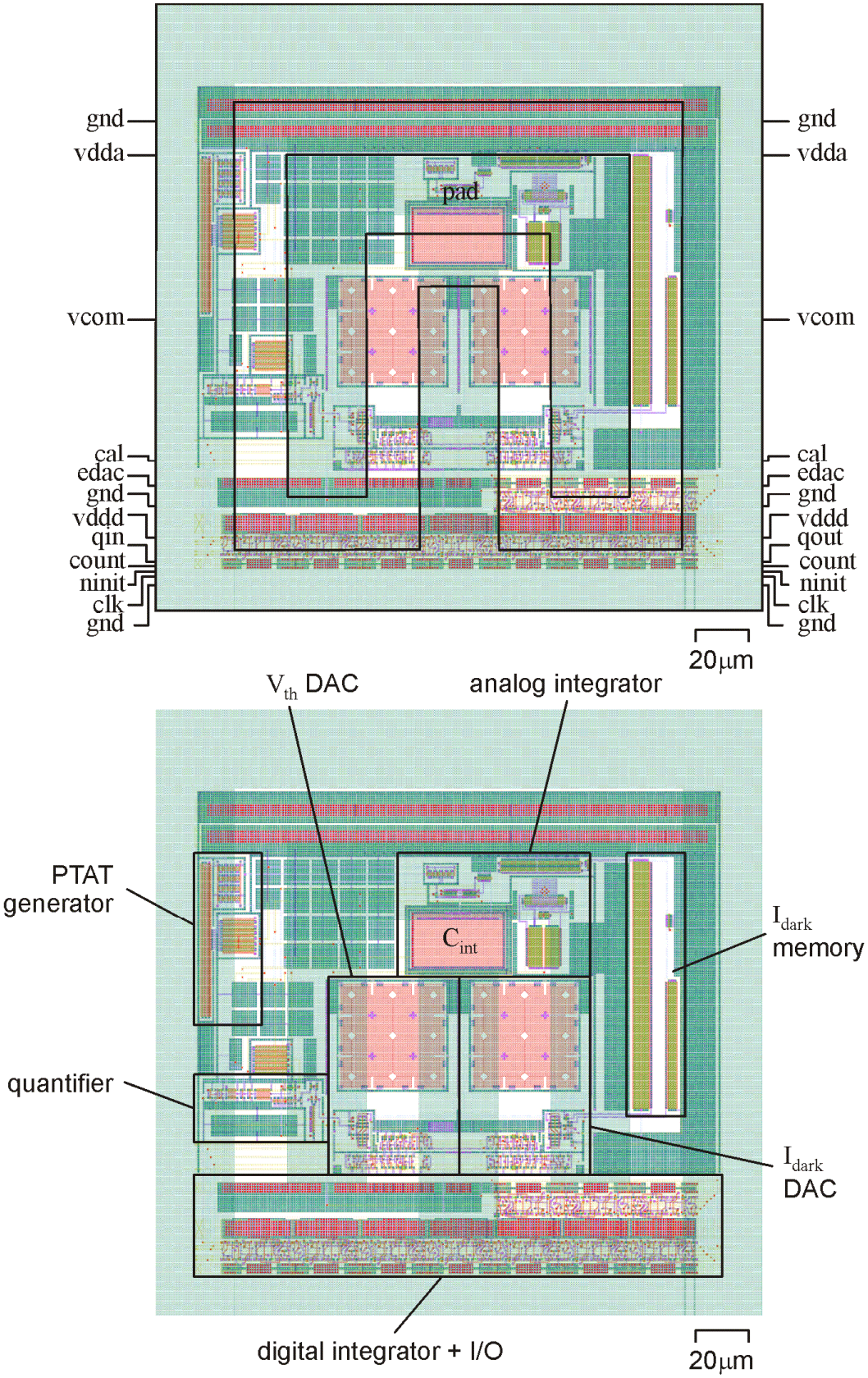


Figure 6.8 Physical layout of a first-generation DPS cell, showing connections (top) and basic blocks (bottom)

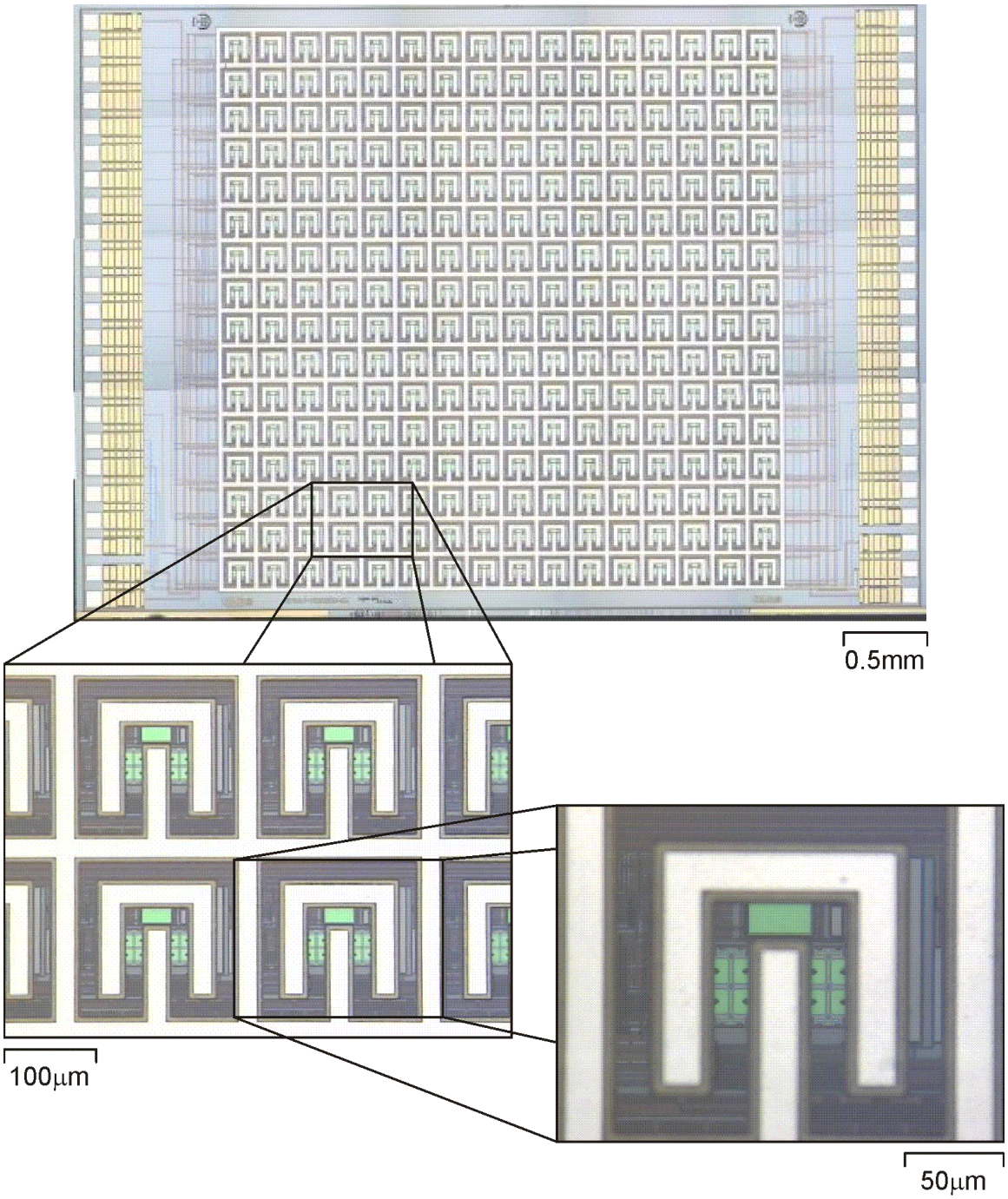


Figure 6.9 Microscope photography and detail of the 16x16 DPS FPA for post-processing

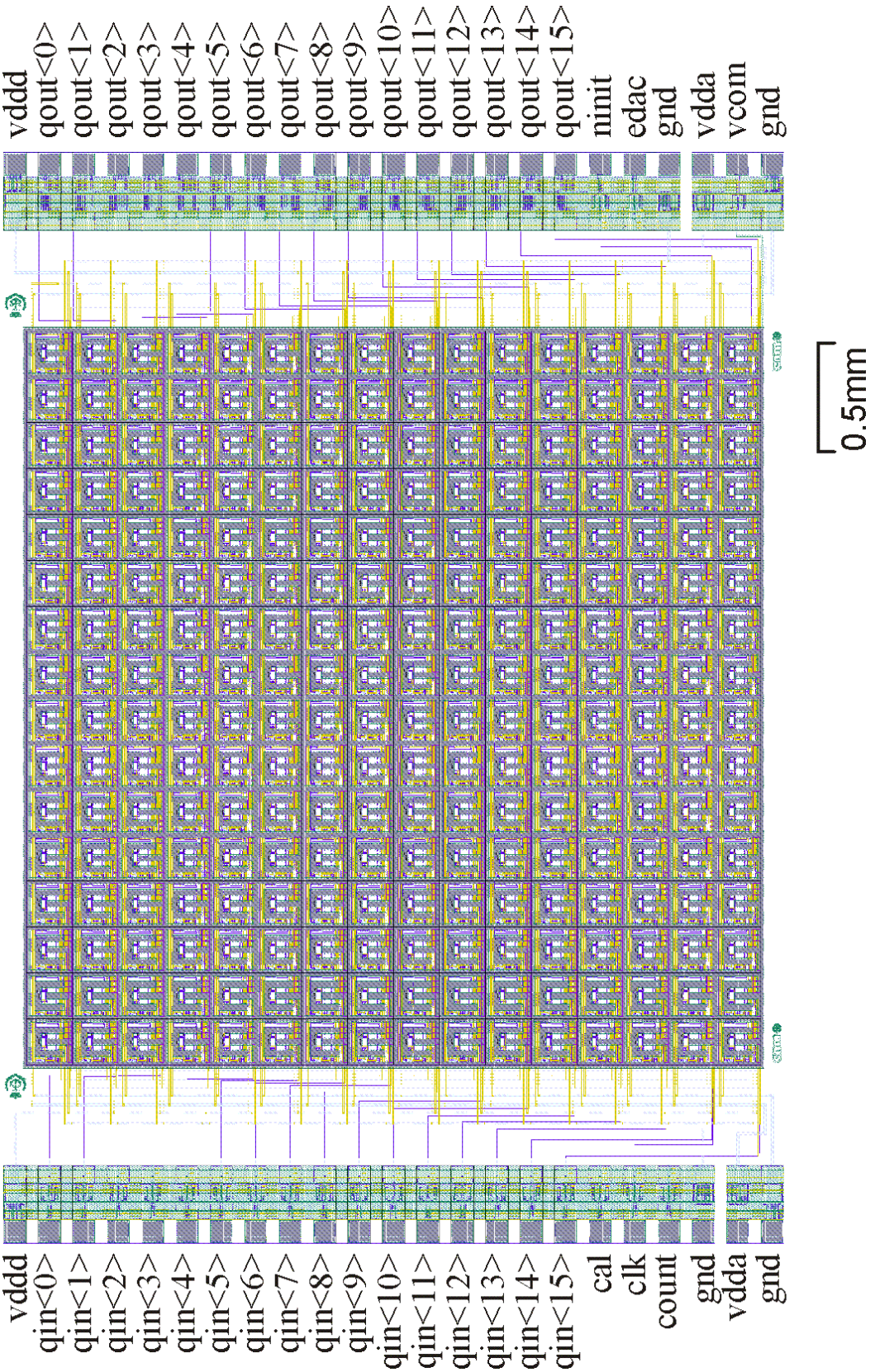


Figure 6.10 1st-generation DPS FPA layout and pin-out

6.2.3. Generation 2: Towards the Modular Hybrid Approach

The second generation is the last DPS version integrated up to now. This novel pixel approach is conceived to construct the Modular Hybrid FPA described in Section 4.1.2. In this sense, all the design rules related to both CMOS module, MCM packaging technologies has been compiled as summarized in Figure 6.14(top). Considering a dice saw tolerance of about 35µm, combined with a minimum pick-and-place inter-module space of 50µm, a resulting 2x70µm spatial loss in the CMOS layer is obtained for two adjacent module edges.

In view of the desired lossless image-acquisition FPA, the estimated 140µm must be recovered through MCM rerouting and a non-uniform DPS CMOS cells distribution, with an equivalent pitch slightly minor to the IR detector boundaries of Figure 6.13. This solution is depicted in Figure 6.14(bottom).

The active pixel has been redesigned in order to reduce Si size on the new cell. The CMOS circuits have not suffered functional changes (see Figure 6.11), and can also be operated using the same procedure as first generation (Figure 6.5, Figure 6.6). Main changes have been devoted to redistribute the elements of the previous generation, in order to save unnecessary area. The D/A converter layout has also been compacted, and is multiplexed for both I_{dark} and V_{th} programming, with the aim of control, respectively, the offset and the gain of every DPS cell. As a result, the pixel is scaled from 200µmx200µm to the final 130µmx130µm area of Figure 6.12.

The first ROIC MH-FPA samples have been already assembled. Pitch is selected to be 135µmx135µm, with a margin of 5µm per pixel, according to Figure 6.12, so as to dispose the loosen 140µm inter-ROIC-module gap (see Figure 6.14). Every module has, as well, 32x32 pixels, with a resulting matrix dimensions close to the 16x16 pixels of first generation. However, the rows are now alternatively oriented to the left-right and right-left ways to provide simpler serial external connection. An additional 20µm bumping pad has also been included, in each pixel, to provide connectivity from the external MCM substrate to the ROIC. The resulting module is shown in Figure 6.15.

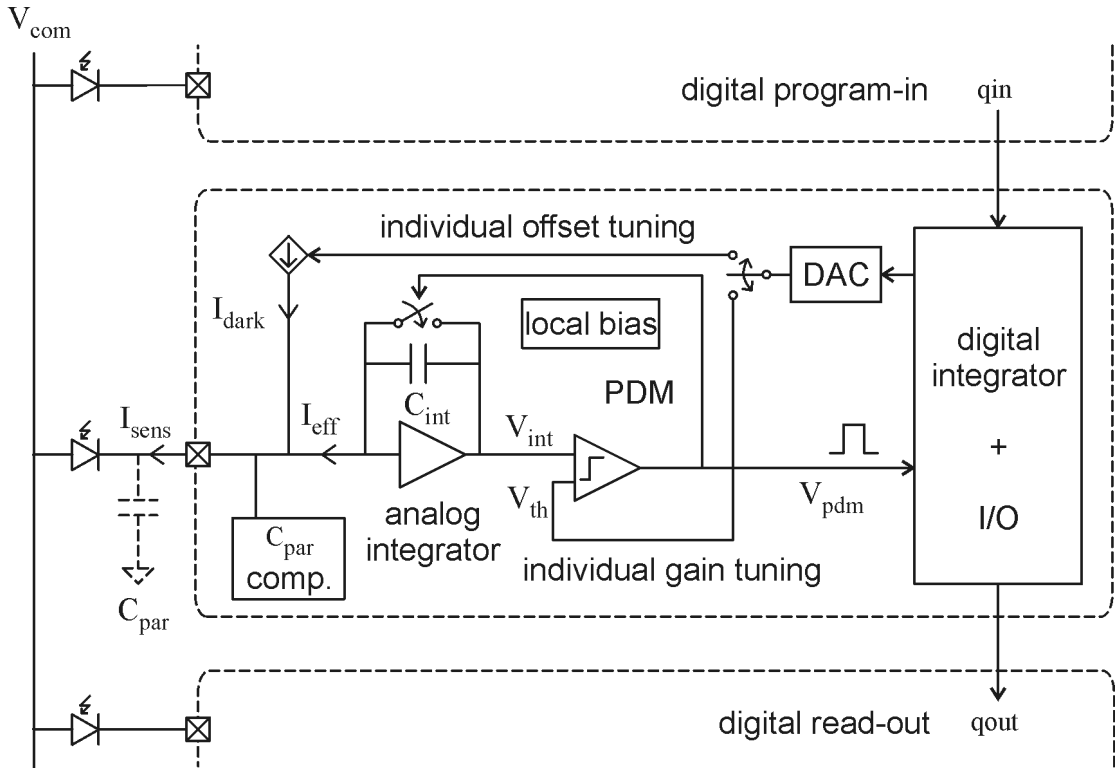


Figure 6.11 2nd generation DPS global scheme

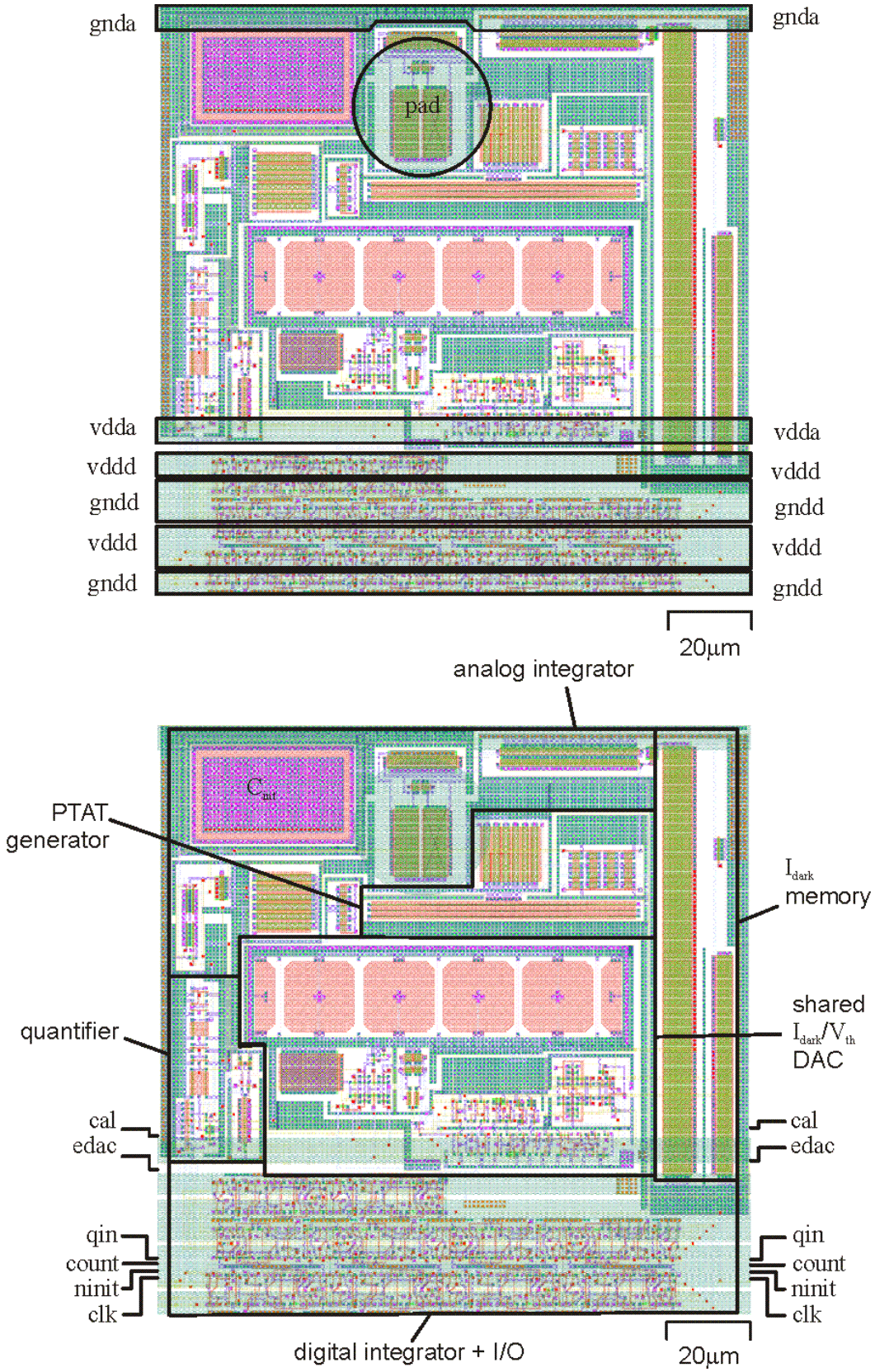


Figure 6.12 Physical layout of a 2nd-generation DPS cell. Metal-4 power lines (top) and metal-3 digital I/O, basic blocks (bottom)

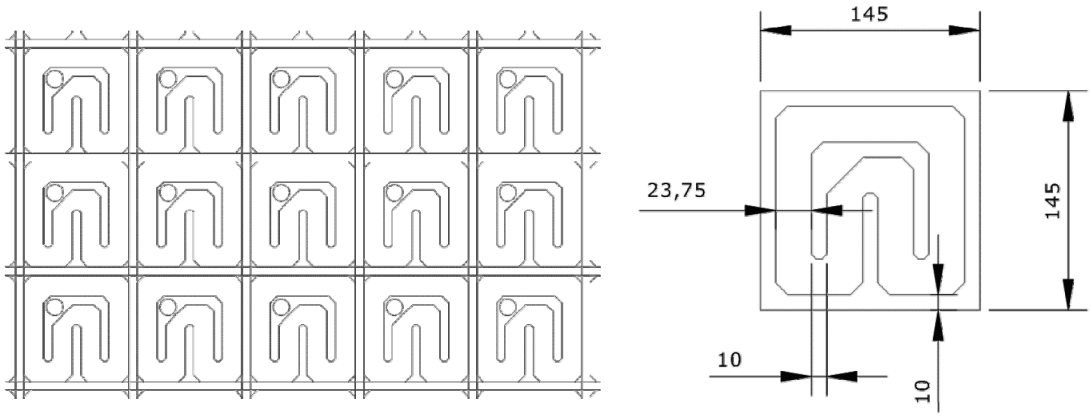


Figure 6.13 Au layer layout for the 135µm x 135µm IR sensor boundaries and Al via (∅20µm) for 2nd-generation DPS. All dimensions are in µm.

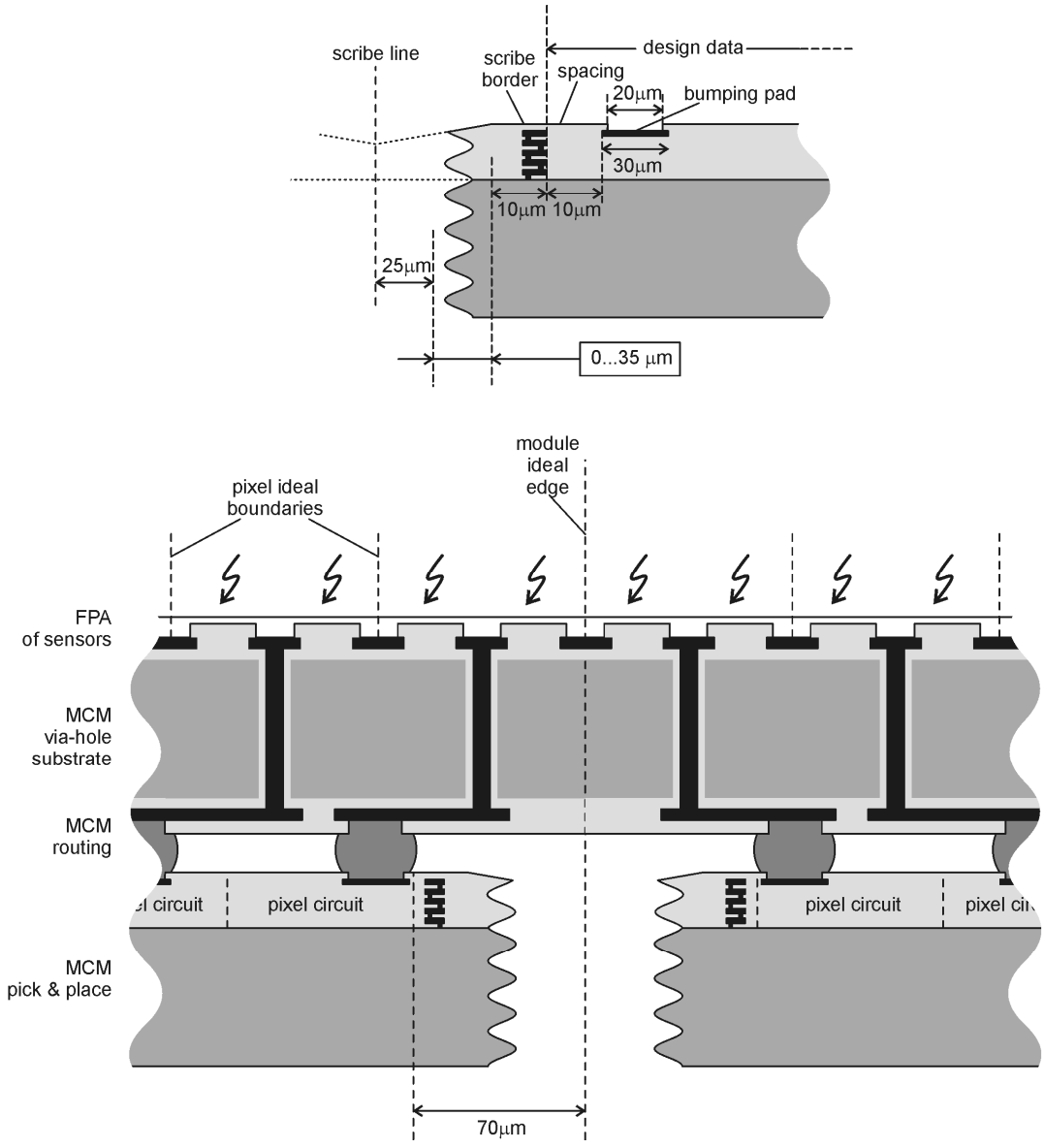


Figure 6.14 2nd-generation DPS design rules (top) and FPA packaging specs (bottom)

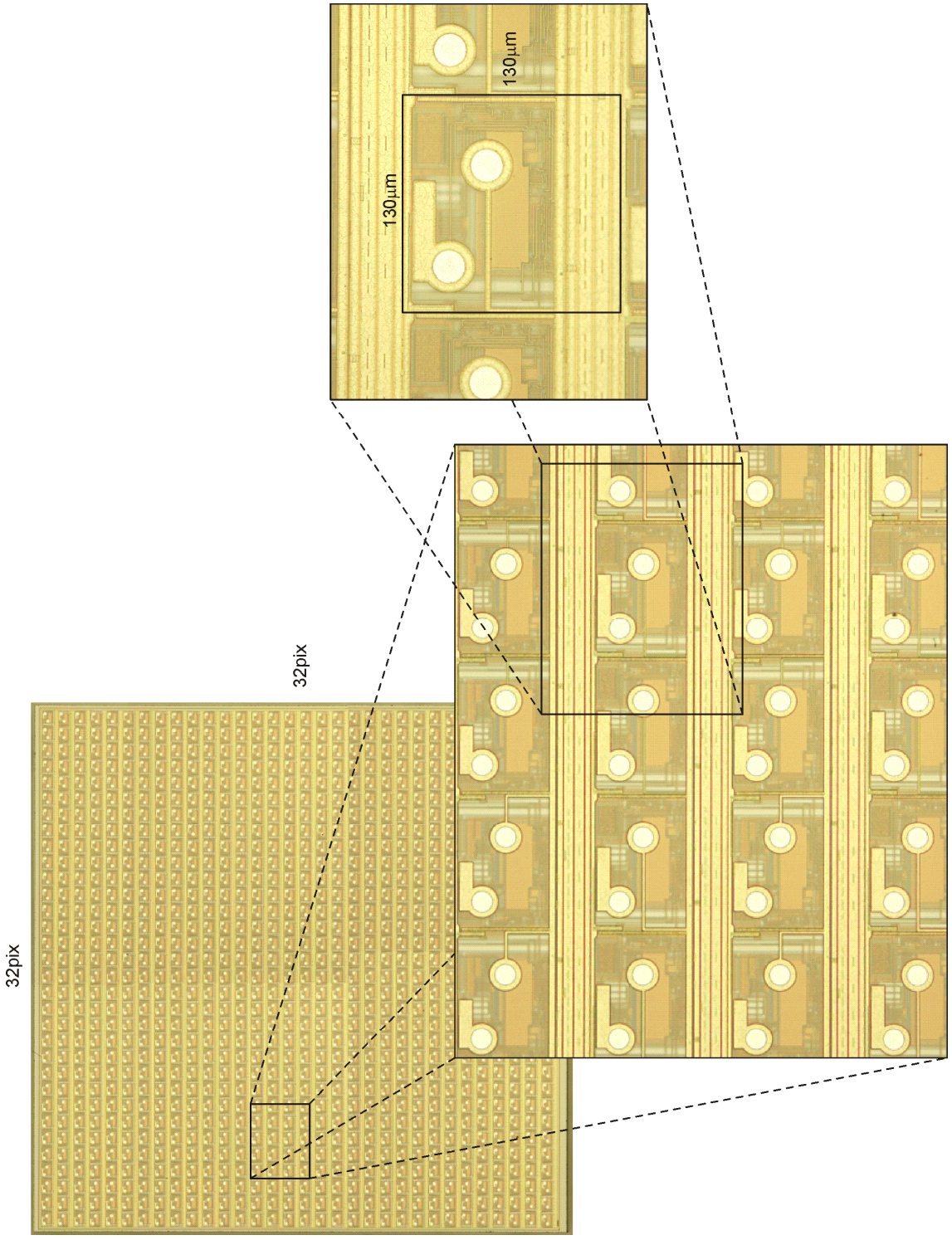


Figure 6.15 Microscope photography and detail of the modular 32x32 DPS matrix for hybridization

6.3. Electrical Characterization

Once physical design of every single DPS generation is done, it is necessary to perform electrical and optical characterization in order to obtain experimental results as a reliability check. Future work will depend on the real statistics acquired from the tests especially conceived for this purpose.

6.3.1. Test Vehicle IC

With the objective to characterize all the existing generations, the integrated test vehicle circuit scheme includes IR detector current internal emulation and single/matricial DPS testing. The PbSe sensor current (I_{sens}) is generated through integrated NMOSFETs. Designed with a long aspect ratio, these devices drain in the strong inversion, conduction region of operation. Specifically:

$$\left.\begin{array}{l} W = 10\mu m \\ l = 100\mu m \end{array}\right\} \left(\frac{W}{L}\right) = 0.1 \qquad \textbf{(6.1)}$$

The assigned dimensions yield to good linearity in the µA region, and transconductance corner values among 1-2 nA/mV. All the sources are polarized to an external voltage $V_{com} = -100mV$ according to Figure 6.16(top), so both leakage current and latch-up effects will be depreciable. Moreover, avoiding external connections to the DPS input, the issue of wire-bonding parasitic capacitance is prevented. The gate control (V_{ctrl}) of each NMOS device generate a wide range of equivalent IR radiation levels, as depicted in the experimental results of Figure 6.17.

Using the emulation strategy described above, every generation test vehicle is made including an isolated DPS cell and a small matrix of pixels. In order to minimize the amount of output pads, IR emulation control is joined in two possible values (V_{ctrlA}, V_{ctrlB}), of which copy of each one of both values is generated (I_{refA}, I_{refB}) for external characterization. Since both I_{sens} values are distributed alternatively, it is possible to obtain a high-contrast, chess-board luminance pattern for adjacent crosstalk test purposes.

6.3.2. Test Methodology

The experimental test bench (Figure 6.18) is mainly composed of the logic analyzer Tektronix TLA720, which is in charge to generate any DPS I/O communication protocol. The Keithley 6487 picoammeter/voltage source controls and senses the emulated input current, while the HP 8904A multifunction synthesizer fixes any other required stable analog reference. All the instrumentation is automatically controlled through a laptop computer powered by LabView software.

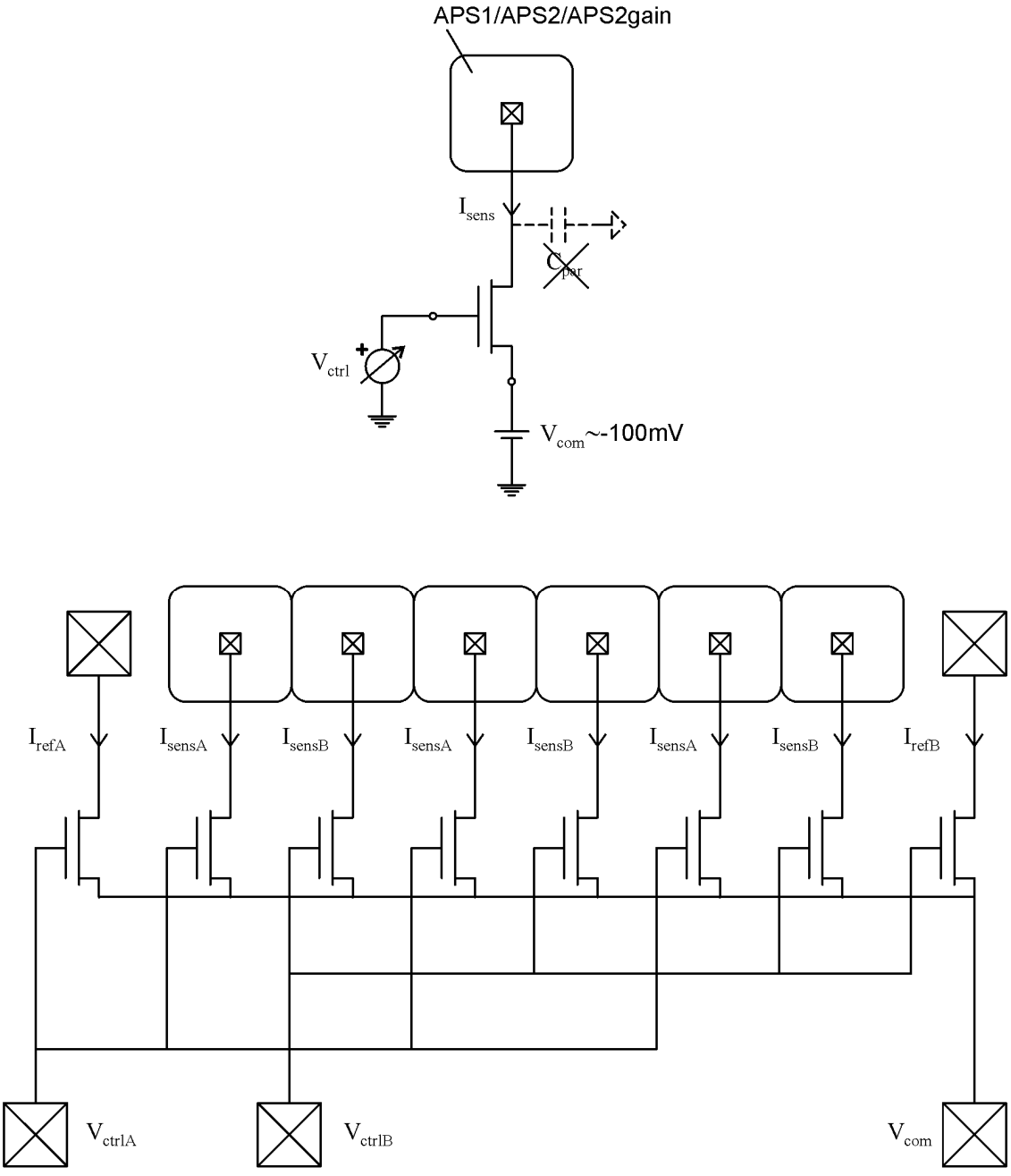


Figure 6.16 IR sensor emulator basic scheme (top) and matrix distribution (bottom)

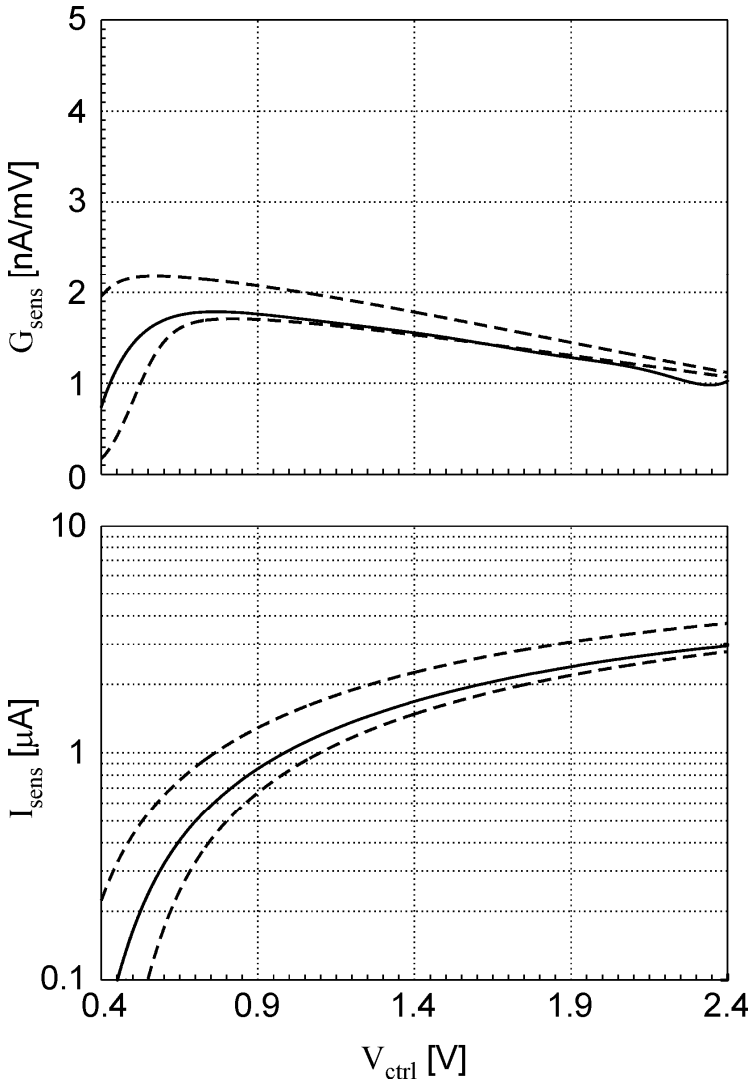


Figure 6.17 NMOS IR detector emulator sensitivity (top) and absolute levels (bottom) obtained from experimental data (dashed lines stand for the simulated technological window).

With the described instrumentation, and applying the protocols described in Figure 6.2 (zero-generation) and Figure 6.5 (1st/2nd-generations), a general test pattern is proposed:

1. Characterization of the IR detector emulation devices.
2. Effective current – digital output code transfer function measure of each DPS.
3. Analog memory retention study
4. Individual gain/offset programmability analysis.
5. Crosstalk test inside the matrix.

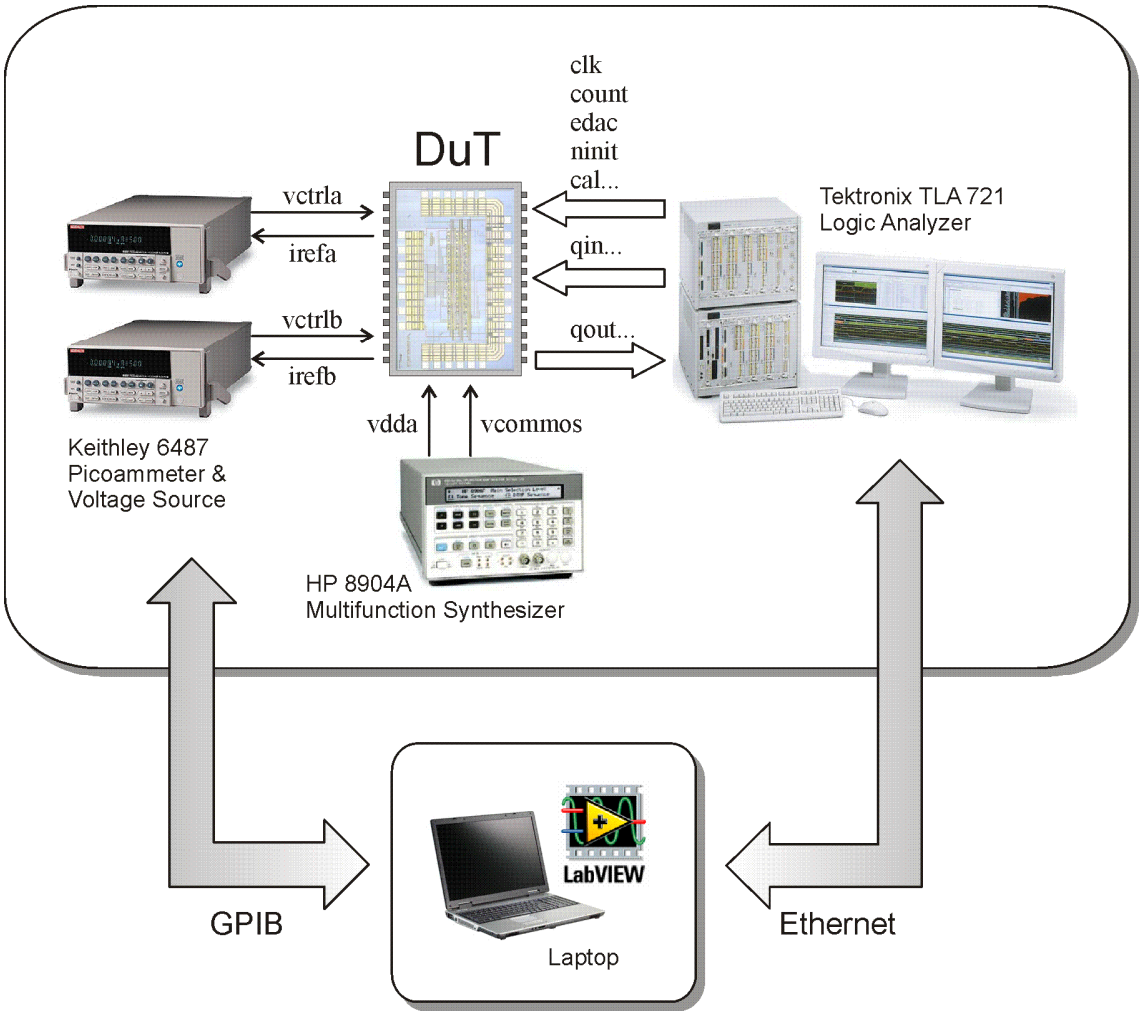


Figure 6.18 Simplified scheme of the DuT electrical testbench

IR Detector Emulation

In order to control in-pixel IR equivalent excitation the detector emulation devices must be characterized. For this purpose, I/V device functions are obtained previously to any other analysis. As shown in Figure 6.17, both tuning margin and control sensitivity are close to the expected results obtained by electrical simulation, and do not depend on DPS generation. The acquired data is used in look-up tables for automatic adjustment of both dark current (I_{dark}) and effective current (I_{eff}) during the test.

Transfer Curve

This is the core basic test, as it characterizes the main function of the internal DPS processing. Using the related IR detector emulators, an equivalent input current sweep is executed for a fixed I_{dark} and V_{th} levels. Considering V_{ctrl} as the superposition of an AC over a DC, offset component, and fixing the alternate component during acquisition, it is possible to cyclically generate a large variety of I_{sens} values in order to perform the required analysis. Figure 6.19(top) exemplifies a transfer curve data characterization, where the initial calibration cycle is followed by a succession of N acquisition cycles, depending on the desired extracted curve resolution (normally N=100). The output code is read and post-processed using Matlab software.

Analog Memory Retention

This test is intended to evaluate internal DPS analog memory degradation, for a particular I_{dark} calibration value and a programmed V_{th} level. An indirect measure of this effect is performed if digital read-out variations are acquired for a fixed I_{sens}.(i.e. static programming of the IR emulation device). Under the referred conditions:

$$\Delta b_{out} \propto \begin{cases} -\Delta I_{dark} \equiv I_{eff} \\ -\Delta V_{th} \end{cases} \qquad \textbf{(6.2)}$$

Taking into account that analog integration is only valid for positive I_{eff} values, it is necessary to set up a high enough initial I_{sens} value in order detect positive variations of I_{dark}. Based on this idea, the test procedure of Figure 6.19(bottom) consists of an initial calibration phase, executed with I_{sens}=I_{dark}, and continued by several standard acquisition cycles for a known IR emulator current I_{sens}=I_{dark}+I_{eff} during an undefined time.

Individual Programmability

This test stage is devoted to digital, individual offset and/or gain programming. In this sense, the transfer curve characterization sweep is repeated for every desired code. A larger V_{th} will lead to higher function slope, whereas the larger the programmed I_{dark} code, the less dark current will flow through the PMOS devices of Figure 5.4(top), so the higher the necessary I_{sens} to start integration event counting.

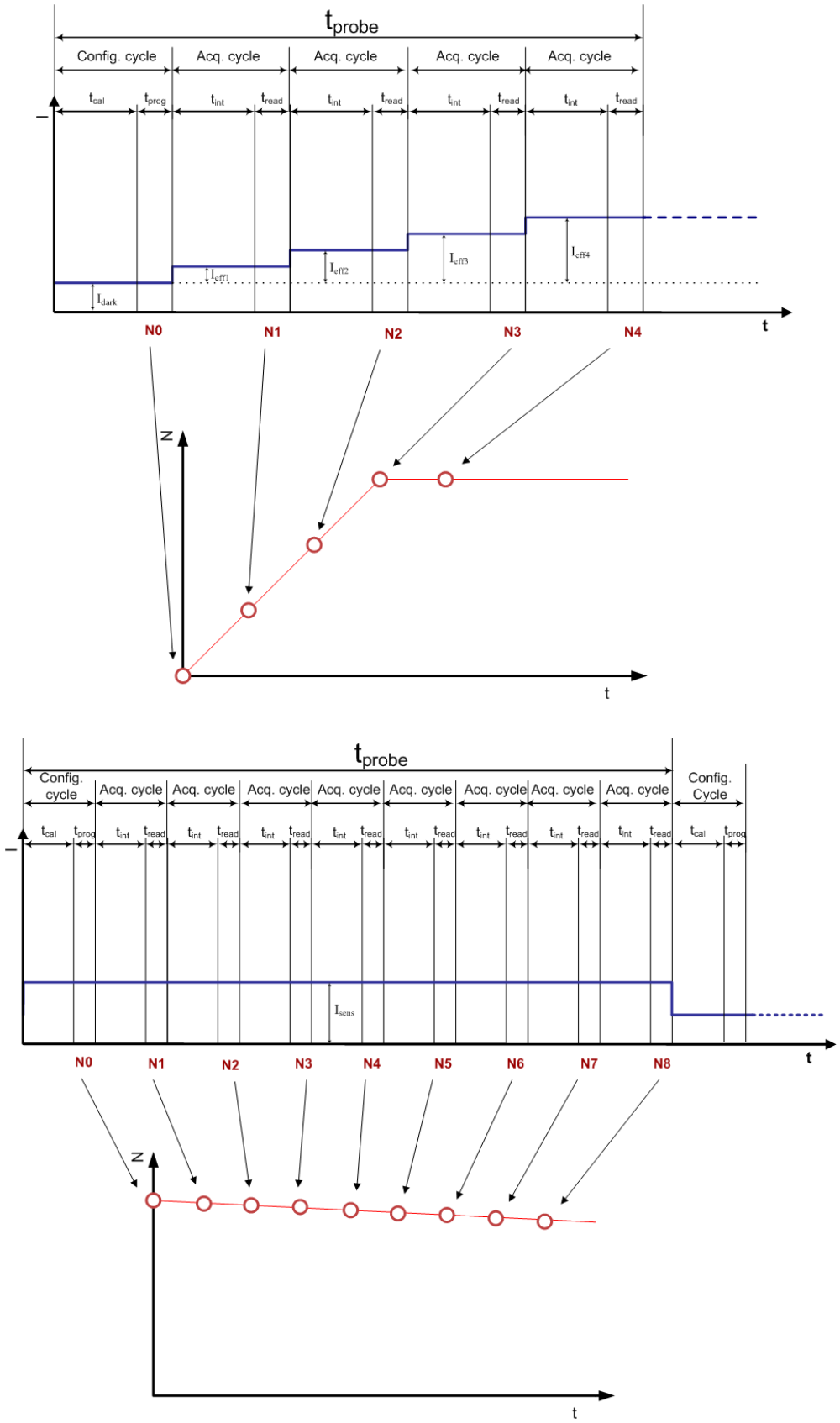


Figure 6.19 Transfer function (top) and analog memory (bottom) characterization scheme

Crosstalk

The remaining test aims to measure coupling effects between adjacent pixels. For such a purpose, one of the IR emulation V_{ctrl} is set to full-scale, while he rest of the DPSs receive null excitation. The latter are monitored to detect any induced event, either due to spatial proximity or temporal immediacy in the I/O protocol.

6.3.3. Generation O: Opening Results

Once first prototype samples were produced, the received samples were submitted to test. Results proved general architectural feasibility, as well as some weak points susceptible to be improved. An example is I_{dark} auto-calibration, which behaves with a retention time of about 1 second (Figure 6.20(top)) mostly produced by the discharge of M6 (i.e. C_{dark}) through subthreshold conduction or parasitic PN junctions due to switching coupling produced on successive ADC integrator resets, as shown in Figure 6.20(bottom).

Referring to transfer function and gain programming, effective programming is confirmed but a curve compression phenomenon is also observed, as depicted in Figure 6.21. Exhaustive electrical simulations point to parasitic coupling from comparator to V_{th} analog memory, which results in progressive increase of the threshold voltage, and so a reduction of the generated density of pulses counted by the digital integrator. The regenerative comparator of Figure 6.1(bottom), suffer also of unexpected meta-states which reduce spike width below the minimum noticeable duration for digital integration. Crosstalk is revealed to be inappreciable.

Experimentation results are summarized in Table 6.6. Conclusions are the following:

- ✓ IR detector emulation is proved to be feasible.
- ✓ Functional architecture seemed to be optimum in order to integrate a fully digital APS with inner FPN compensation.
- ✓ Cells library needs further revision at CMOS level in order to overcome the drawbacks described in Table 6.6.

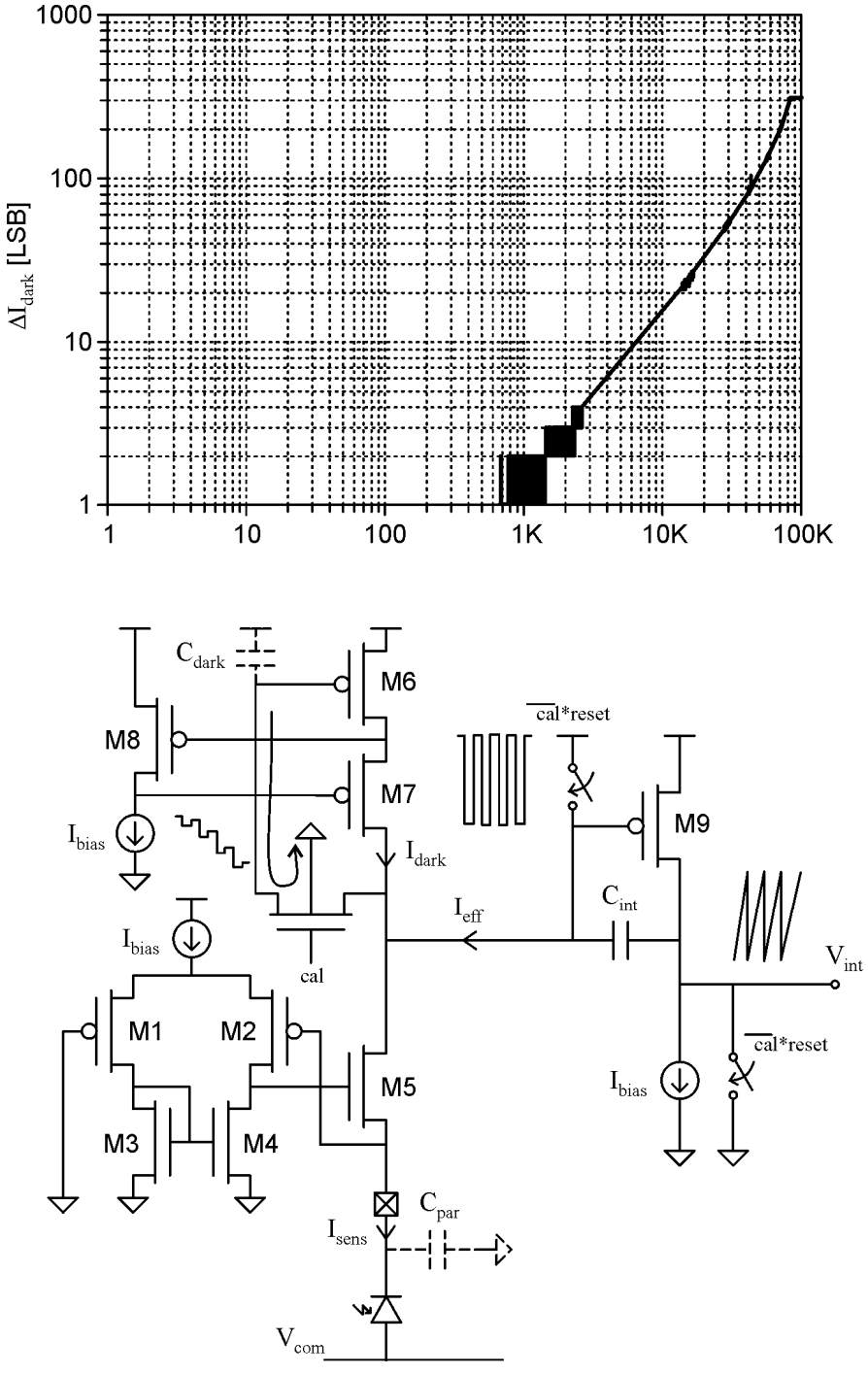


Figure 6.20 Experimental measures of I_{dark} memory retention (top) and possible sources illustration (bottom), for I_{dark}=1uA and I_{eff}=0.5uA.

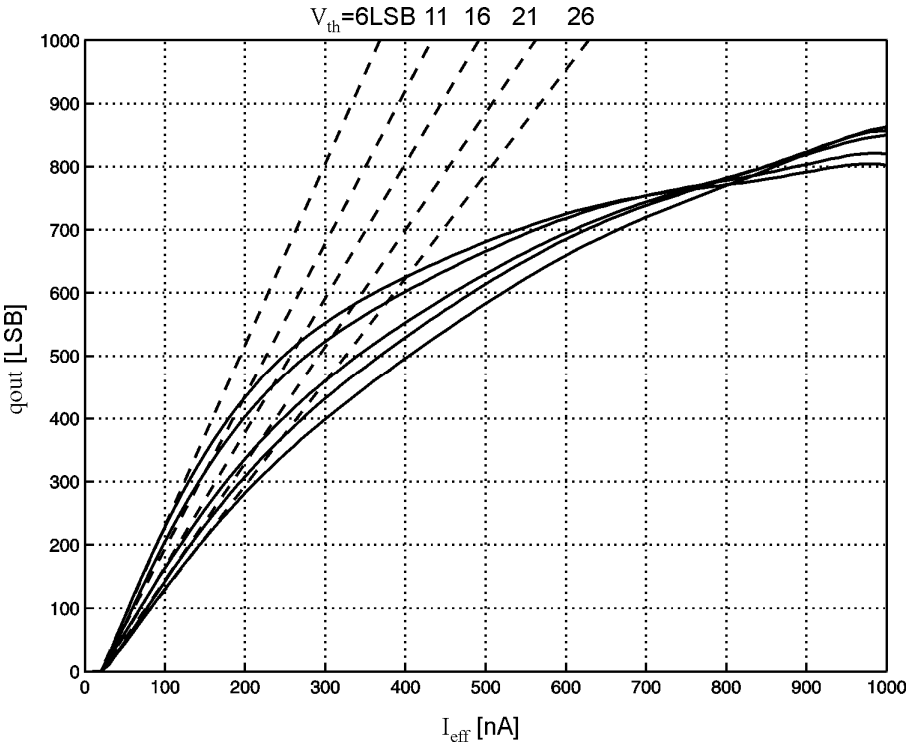


Figure 6.21 Example of transfer function and individual gain control over a zero-generation cell, with I_{dark}=1μA and multiple V_{th} values

DPS function	Comments
Self-biasing generation	✓ Correct.
Input capacitance compensation	✓ Correct.
Offset cancellation	✓ Appropriate resolution (~1nA). × Low retention time (~1000ms/LSB): Frequent calibration is needed.
Analog integration	✓ CTIA function performs correctly. × Slow reset: switching scheme must be redesigned.
Pulse generation	✓ Threshold comparison is correct. × Coupling to the DAC: Larger DAC capacitances, minimum comparator dimensions must be used. × Slow transitions, event loosing: Spike generation circuit must be redefined.
Digital integration	✓ Correct.
Individual gain programming	✓ Correct.
Digital communication interface	✓ Correct.

Table 6.6 Zero-generation test results summary

6.3.4. Generation 1 & 2: Electrical Performance

An exhaustive characterization is applied to 7 1st-generation and 10 2nd-generation tiny 3x16 FPA test samples (i.e. Figure 6.22). A total amount of roughly 800 DPS have been tested, yielding to an extensive statistical results study. Considering that both generations share general architecture, it is understandable that experimental results look quite similar. Therefore, a unique test report has been generated for the enhanced, fully tunable, current DPS design.

The transfer curve current sweep is repeated for different I_{dark} and V_{th} programming codes in order to get comparative results. A qualitative pattern of the obtained results is shown in Figure 6.24. A closer look to the large number of obtained graphs reveals that not only linearity, but also the offset control and its related equivalent gain are satisfactory for the desired FPA final applications. If desired, wider I_{dark} programming range would be achieved in cons of lower compensation resolution (e.g. 0.1μA-5μA).

Belonging analog memory degradation, this effect is evaluated for dark current and event threshold internal charge storing. In this sense, repetitive read-outs are performed for both variables. Figure 6.25 shows experimental data, with a retention time higher than the required acquisition period, reflecting the validity of the alternate programming scheme.

Based on the huge number of acquired transfer curves (>8000!), a statistical analysis is done considering offset (I_{off}) and gain (G) as the equivalent characteristic parameters. Thus, all the obtained DPS transfer curves have been compared for a fixed I_{dark} and V_{th}. The obtained results are depicted in Figure 6.27 and Figure 6.26, respectively. It must be considered in this point that I_{off} and G variations are not caused by DAC I_{dark} and V_{th} programming, but by the existing inter-pixel mismatching present all over the DPS cell.

Input offset scattering is probably caused by threshold voltage (V_{TOP}) and current factor ($\Delta\beta_P$) variations in the PMOSFETs employed for I_{dark} generation. Applying Pelgrom's law to technological mismatching:

$$\sigma\left(\Delta V_{TOP}\right) = \frac{A_{V_{TOP}}}{\sqrt{WL}} = \frac{14.5mV\mu m}{\sqrt{717\mu m^2}} \simeq 0.54mV \qquad \textbf{(6.3)}$$

$$\sigma\left(\frac{\Delta\beta_P}{\beta_P}\right) = \frac{\Delta\beta_P/\beta_P}{\sqrt{WL}} = \frac{1.0\%\mu m}{\sqrt{717\mu m^2}} \simeq 0.04\% \qquad \textbf{(6.4)}$$

Depending on saturation region:

$$\text{strong inversion} : \sigma\left(\frac{\Delta\beta_P}{\beta_P}\right) < \sigma\left(\frac{\Delta I_{off}}{I_{off}}\right) < \frac{\sigma\left(\Delta V_{TOP}\right)}{nU_t} : \text{weak inversion} \qquad \textbf{(6.5)}$$

Hence, it is expected:

$$0.04\% < \sigma\left(\frac{\Delta I_{off}}{I_{off}}\right) < 1.66\% \qquad \textbf{(6.6)}$$

Unfortunately, this estimation is only valid for adjacent device pairs, so too optimistic for a pitch higher than 100µm.

Gain differences may be probably produced by local mismatching in the differential pair of the NMOS (V_{TON}) comparator depicted in Figure 5.10 and, in lesser extent, by divergences between pixel integration capacitances. Applying the mismatch model used above:

$$\sigma\left(\Delta V_{TON}\right) = \frac{A_{V_{TON}}}{\sqrt{WL}} = \frac{9.5mV\mu m}{\sqrt{0.14\mu m^2}} \simeq 25.4mV \qquad \textbf{(6.7)}$$

$$\sigma\left(\frac{\Delta C_{int}}{C_{int}}\right) = \frac{A_C / C}{\sqrt{WL}} = \frac{0.45\%\mu m}{\sqrt{576\mu m^2}} \simeq 0.02\% \qquad \textbf{(6.8)}$$

And:

$$\sigma\left(\frac{\Delta G}{G}\right) = \sqrt{\sigma^2\left(\frac{\Delta V_{TON}}{V_{th}}\right) + \sigma^2\left(\frac{\Delta C_{int}}{C_{int}}\right)} \simeq \sigma\left(\frac{\Delta V_{TON}}{V_{th}}\right) \equiv \frac{25.4mV}{3.3V/2} = 1.54\% \qquad \textbf{(6.9)}$$

Results of both Figure 6.26 and Figure 6.27 reflect expected larger I_{off} and G distribution apertures, of which effects can be fully compensated by means of the corresponding I_{dark} and V_{th} external calibration. Are just these last measures that reveal the necessity of both dark current and event threshold digital FPN tuning.

Finally, as observed in previous generation, crosstalk tests don't detect coupling disturbances in anyone of the numerous characterized pixels, so DPS is confirmed to be the proper design strategy in front of the traditional, analog APS. New DPS architectures exhibit satisfactory performance.

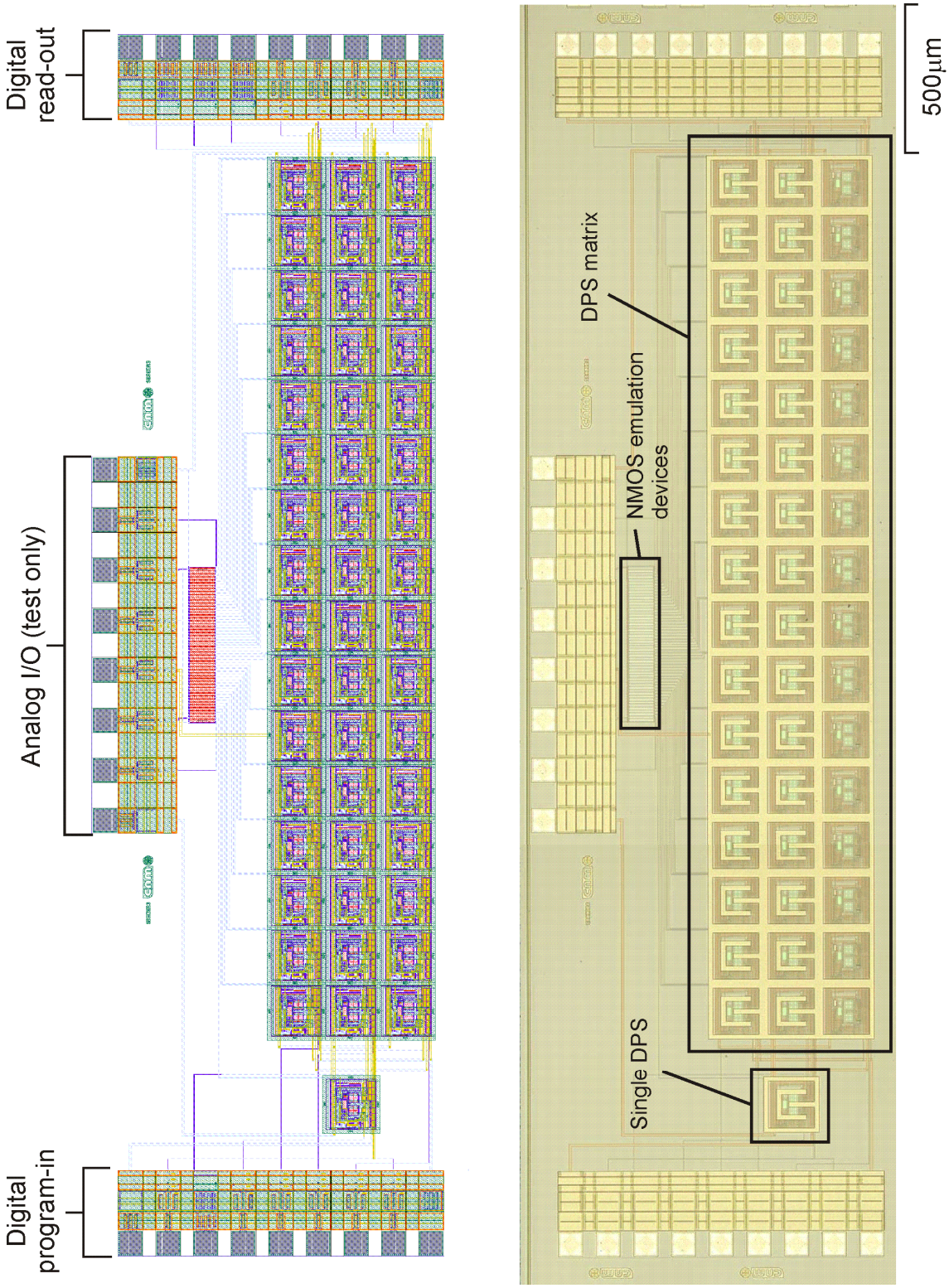


Figure 6.22 Layout and microscope photography of the 1st-generation test vehicle

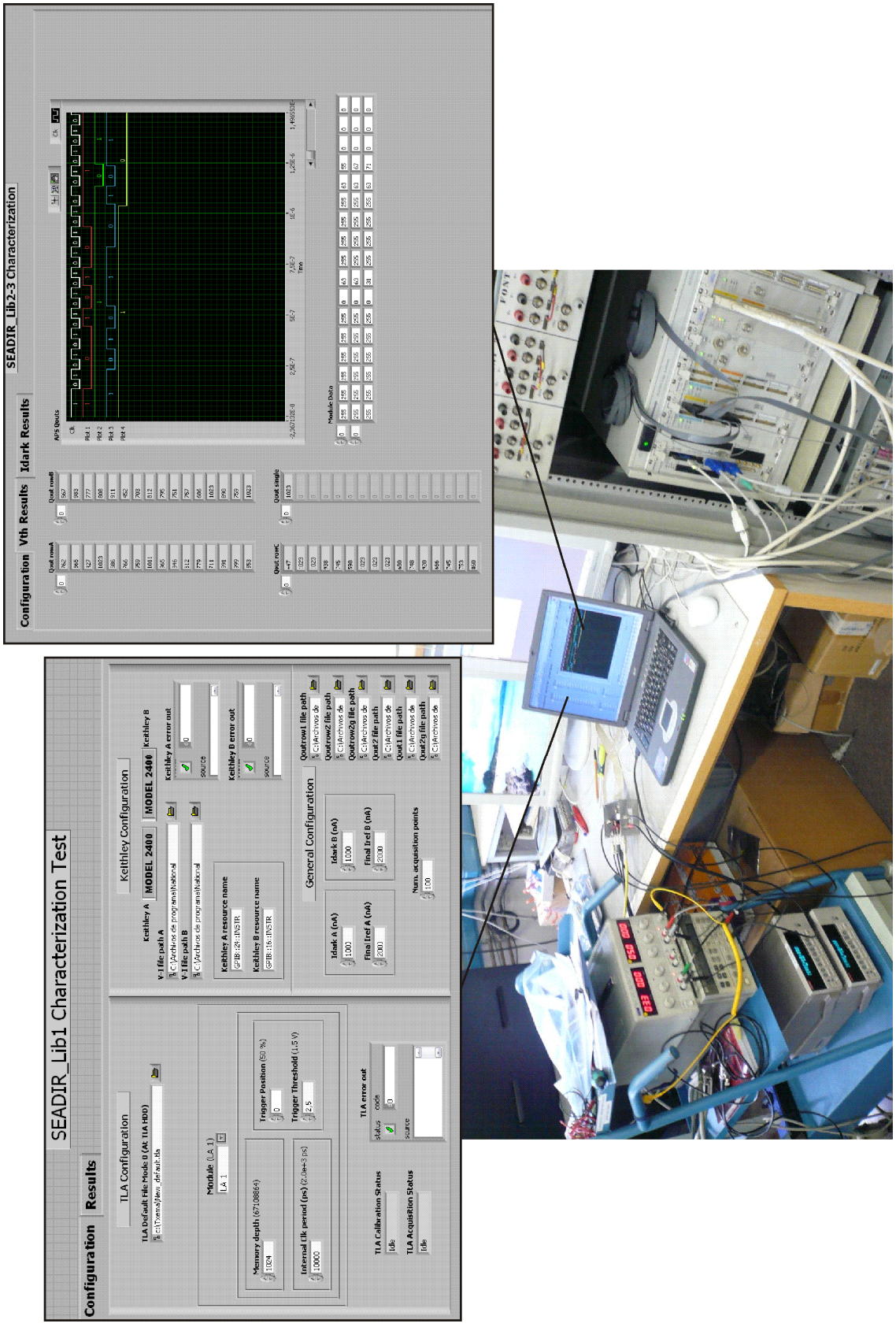


Figure 6.23 FPA electrical testbench (bottom). LabView interface front panel for zero-generation characterization (top-left) and 1st/2nd-generation read-out (top-right) captures.

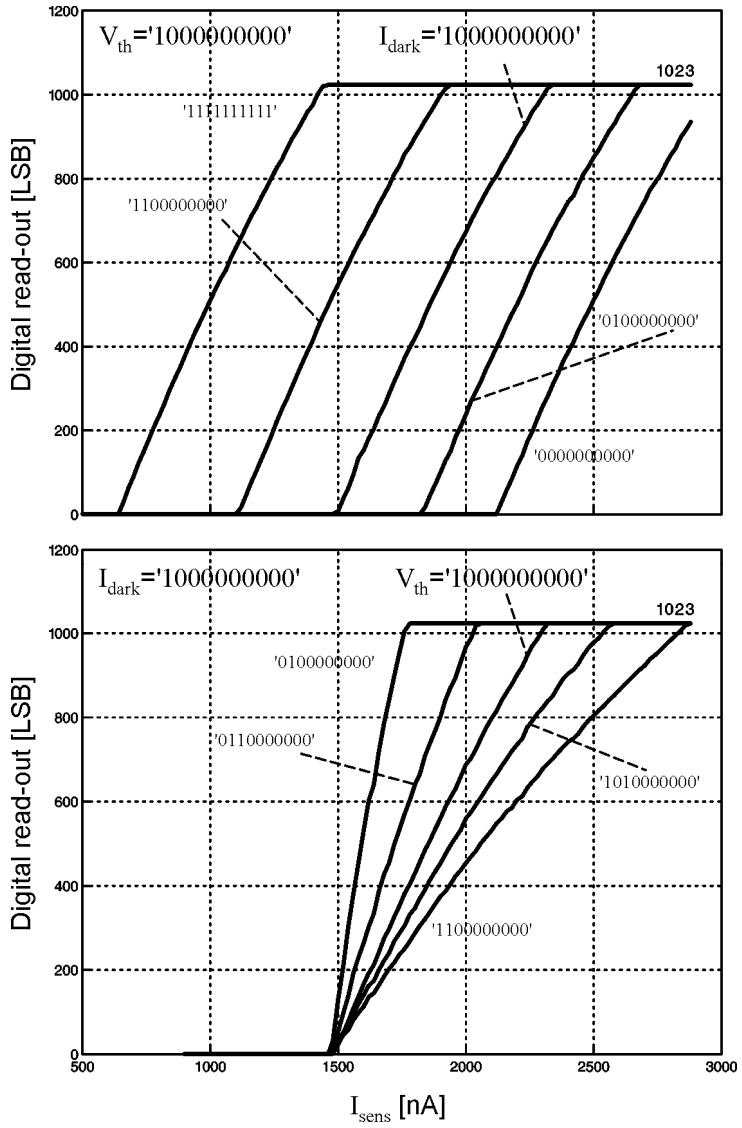


Figure 6.24 Experimental DPS transfer curve for different individual offset (top) and gain (bottom) digital tuning codes.

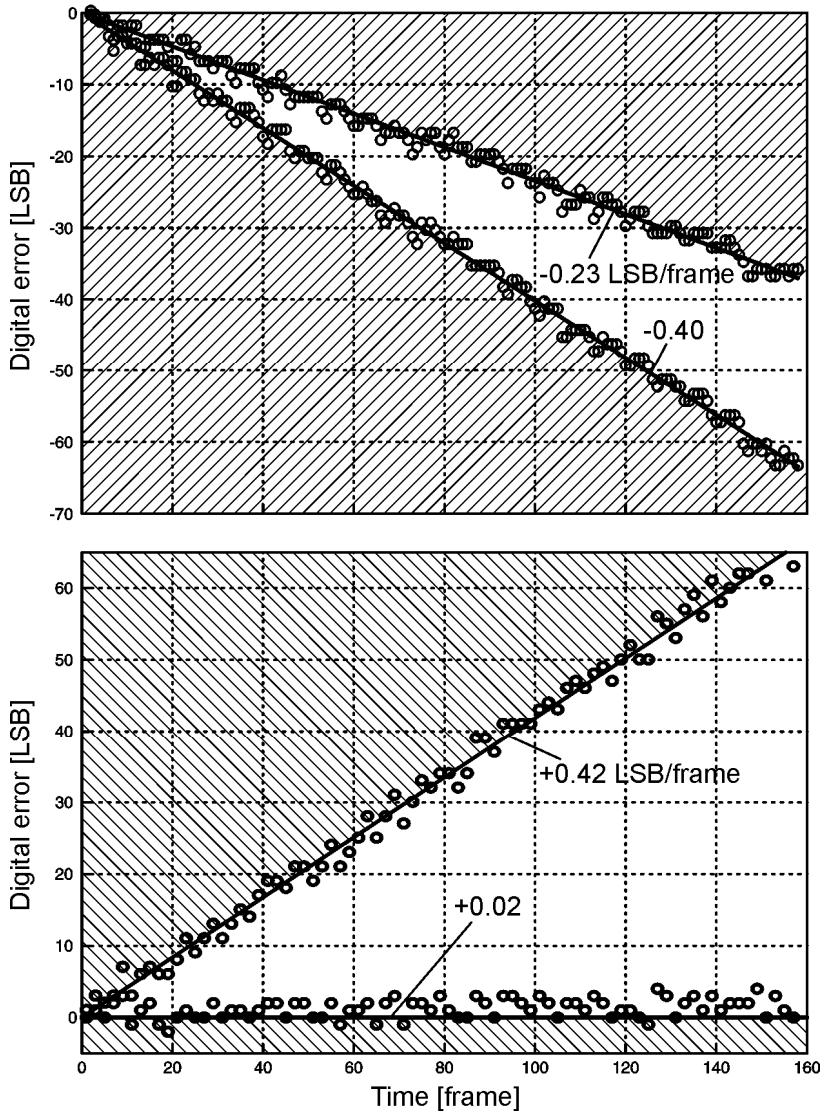


Figure 6.25 Experimental results of I_{dark} (top) and V_{th} (bottom) memory leakage rates inside the DPS.

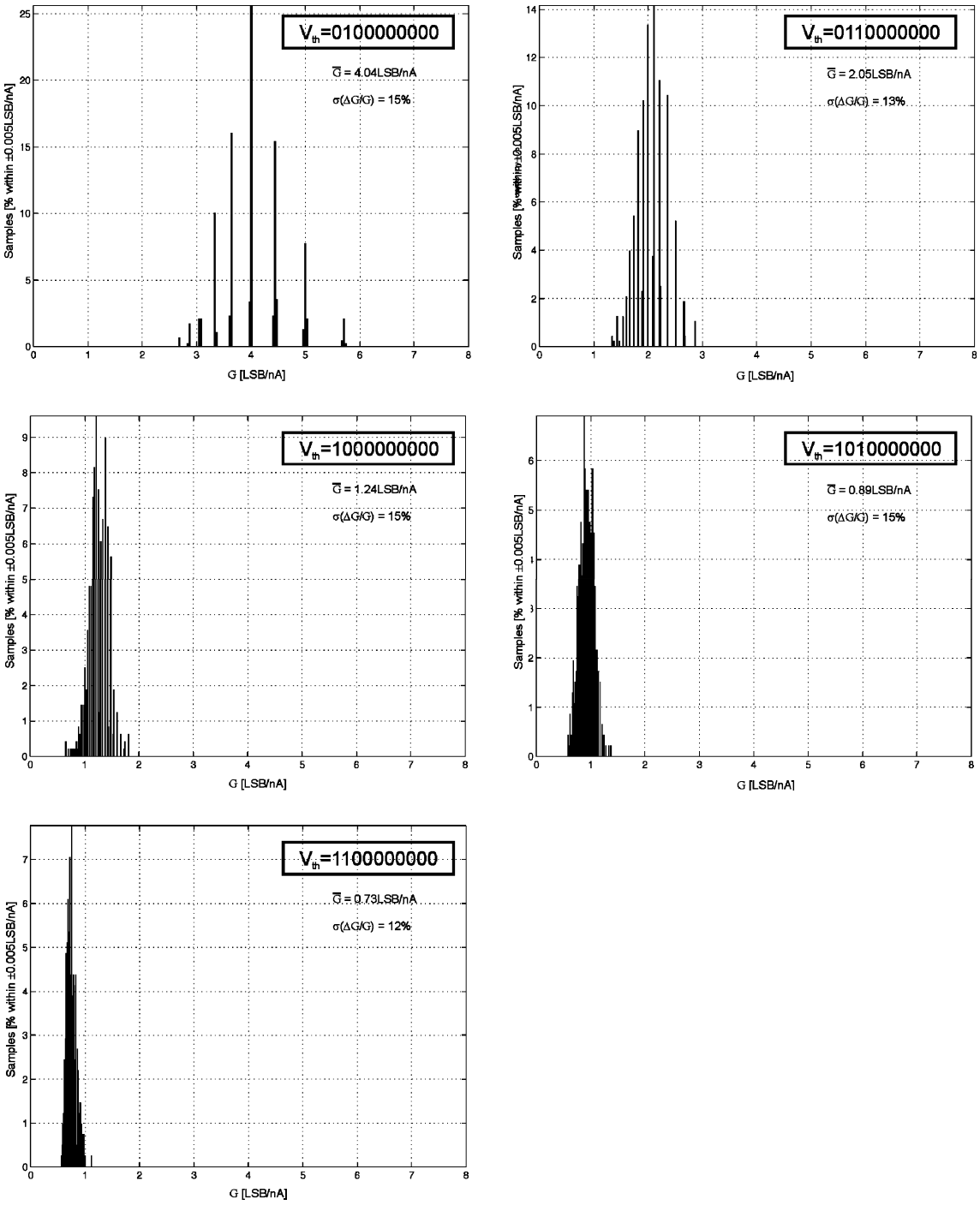


Figure 6.26 Experimental gain deviations for I_{dark}='1000000000', and a six V_{th} tuning-code sweep.

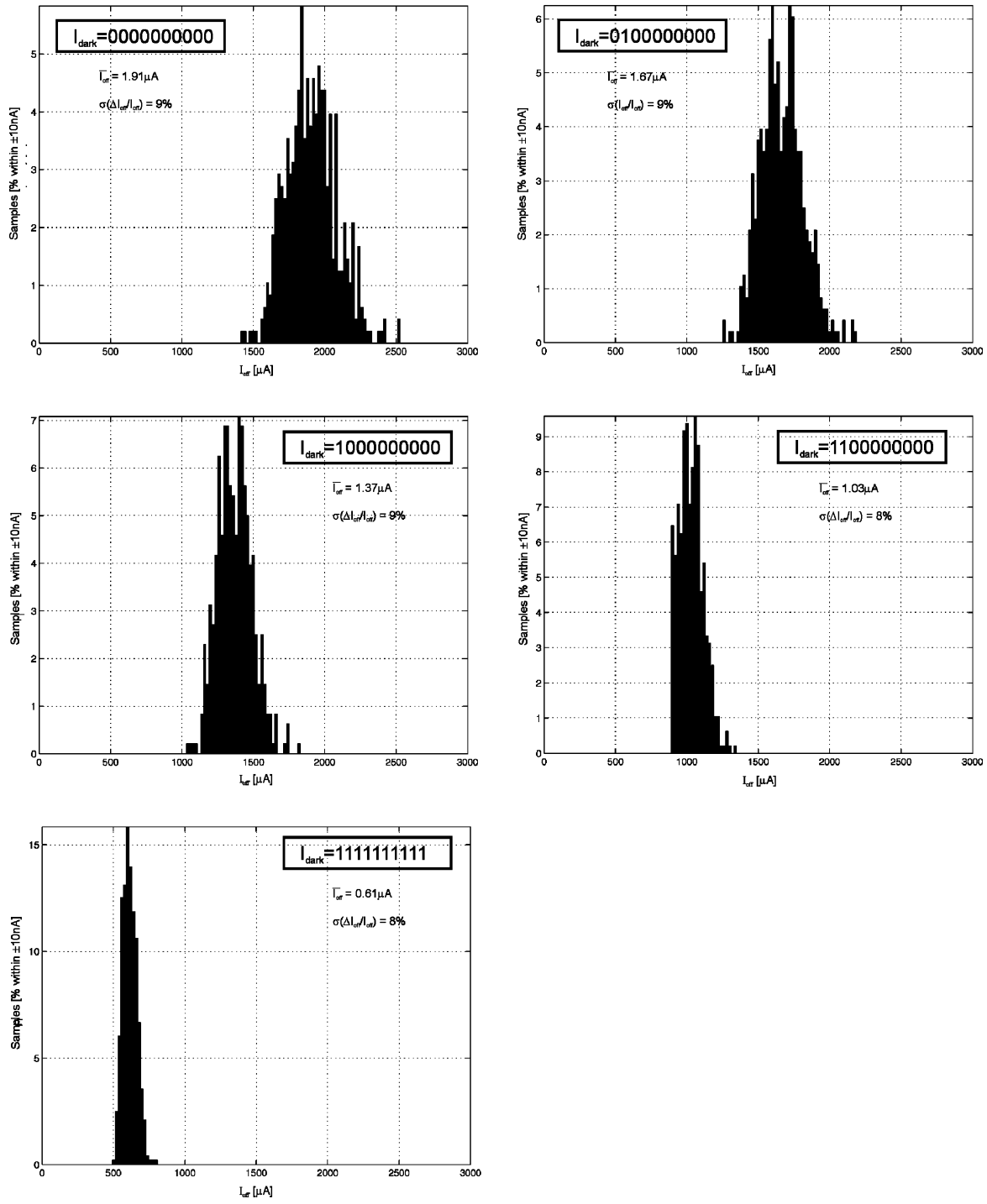


Figure 6.27 Experimental I_{off} deviations for V_{th} ='1000000000', and a six I_{dark} tuning-code sweep.

6.4. Optical Characterization

Not only electrical but also IR optical characterization will be applied to FPAs. In this sense, some 1st-generation samples have been sent to the customer for PbSe post-processing and experimental validation. As shown in Figure 6.28, the optical test system is mainly composed by a chopped IR emitter of which infrared radiation is focalized directly to the ROIC. Digital communication is established through a probe-station and controlled by an external FPGA, whereas read-out is finally processed by way of LabView software.

Preliminary results depicted in Figure 6.29 confirm technological compatibility between the detector and the CMOS technologies, and a flat, quick response beyond the 2000 fps, in front of the hardly 100 fps that bolometers are able to manage.

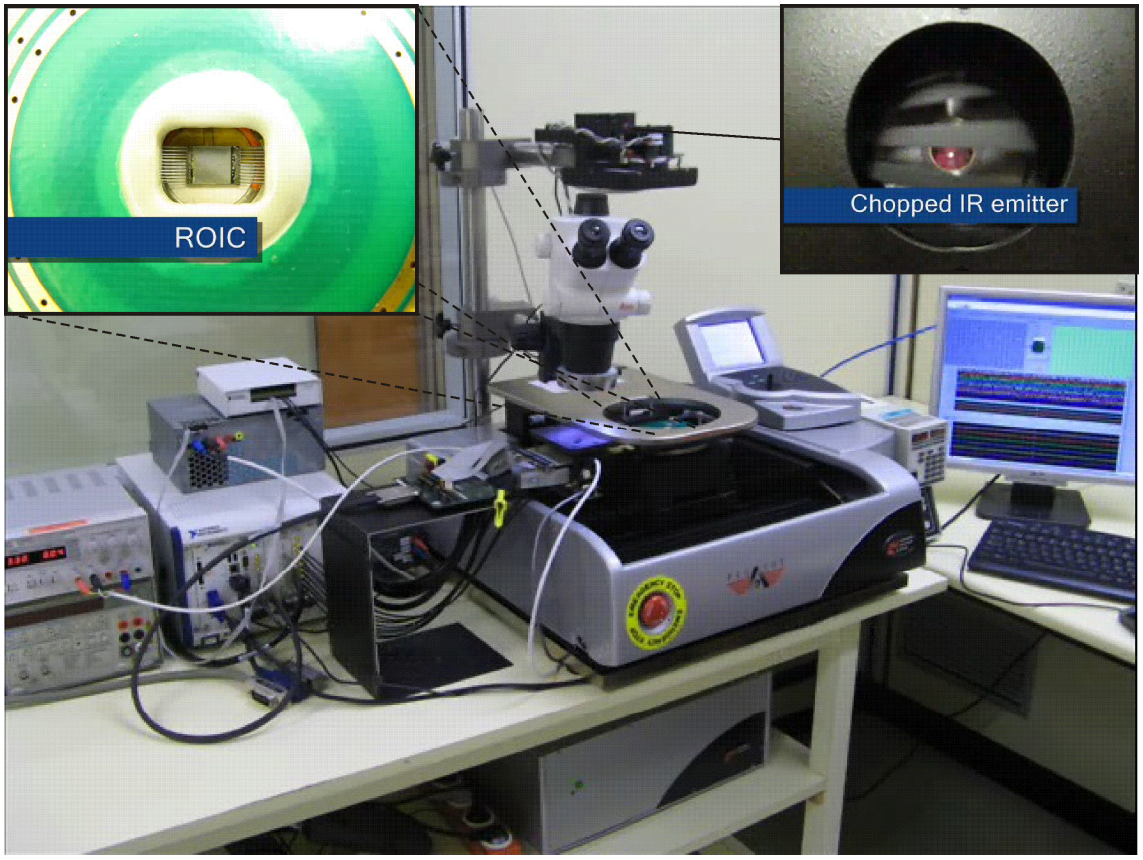


Figure 6.28 IR FPA optical measurement system

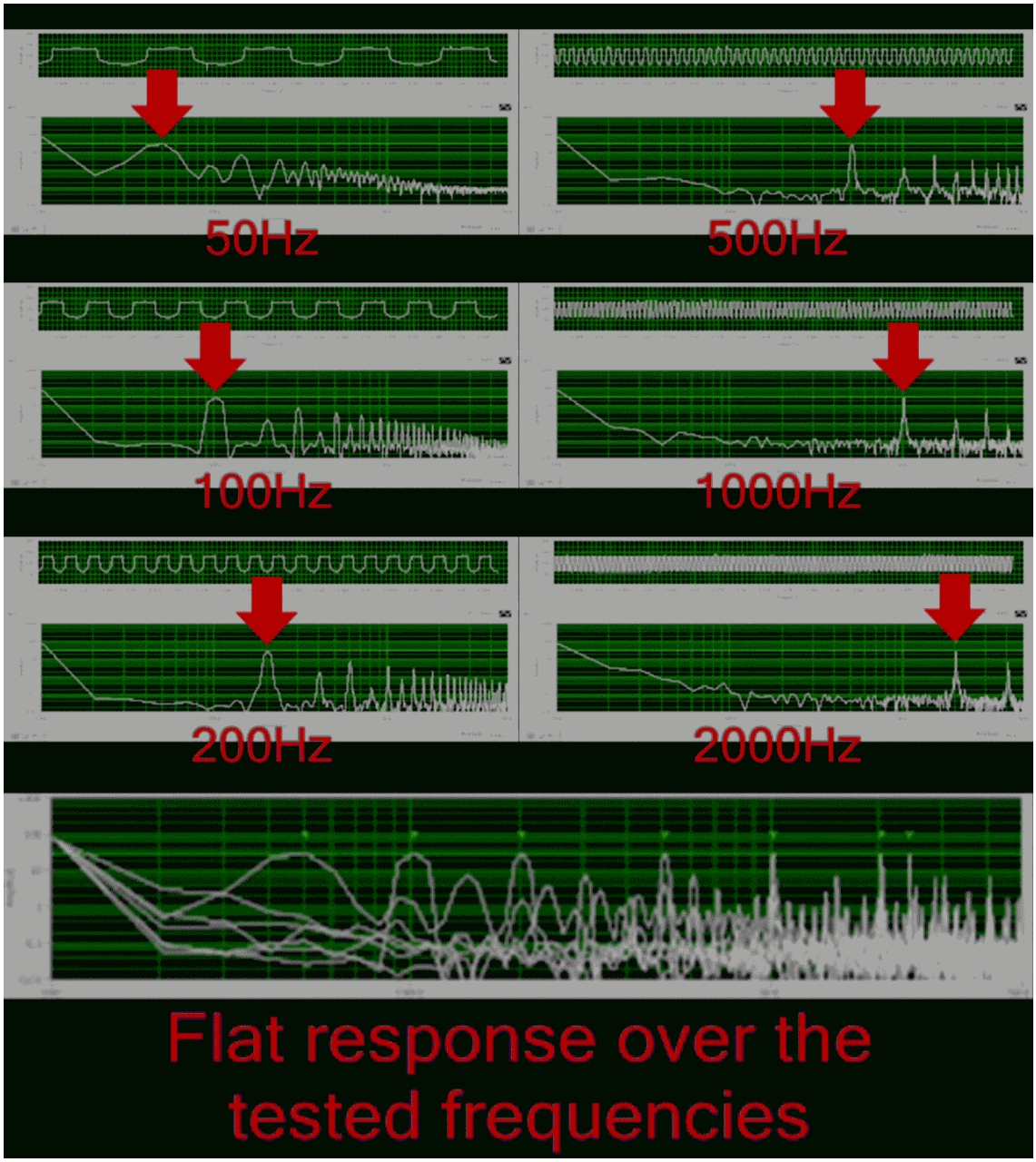


Figure 6.29 Preliminary IR optical characterization results

Chapter 7
Conclusions

This last chapter can be understood as a summary of all the new experience acquired by this work, where the generated know-how and design results are briefly exposed from the academic and applied points of view. Furthermore, future work tasks are also proposed in order to expand this research area in terms of general architecture development, circuit design improvement and hybridization processing and evaluation.

7.1. Results

The semiconductor market is on increasing demand for fast IR imaging in key application fields like automotive, medical, scientific and strategic equipments. This master thesis addresses IR system design issues obtaining specific results in three main fields: IR sensor modeling, FPA module technology, architecture definition, and full-custom DPS cell design.

Since the research activity started, an SPICE electrical PbSe detector model has been created which includes both all main characteristics and non-idealities of the sensor. The equivalent circuit is proposed for general system simulation, and contains direct-tuning detector variables according to supplier physical characterization.

The overall FPA structure is chosen to be implemented using both compact-monolithic and new in-house modular-hybrid technologies. Whereas the modular approach was initially presented in [PFC05] as the selected FPA construction methodology, monolithic focal planes are here introduced as an interesting alternative in order to obtain in-progress results previously to MCM technology availability. On the other hand, ROIC architecture strategies have been carefully evaluated and functionally tested through Matlab software routines; as a result, a fully-digital interface, synchronous, pulse density modulation scheme with in-pixel A/D conversion is applied.

Referring to the APS, a novel low-power and completely programmable CMOS digital active pixel sensor has been developed for uncooled IR fast imaging, using MOSFET sub-threshold design techniques. The circuit proposals include several CMOS topologies for all the basic building blocks: input capacitance and dark current

compensation, integrating A/D conversion, digital I/O interface and self-biasing, all inside the DPS cell. Furthermore, full FPN compensation is supplied in this design by adding independent digital tuning of both offset and gain for each individual DPS circuit without any reduction in the read-out speed.

In [PFC05] a general ROIC, DPS architecture and concept feasibility through a dummy DPS prototype was introduced; the long-term post-PFC design activity is centered on the development of effective CMOS realizations, yielding to new topologies, like the lossless PDM scheme exposed in Section 5.3. or the novel external tuning mechanism for dark current compensation, and extensive CMOS improvement of the functional blocks. As a result, three compact physical DPS generations are presented for IR PbSe detector post-processing and bump-bonding, in order to obtain practical results, at system level and for real applications. Both designs have been integrated in standard 0.35um 2-PoliSi 4-metal CMOS technology, and exhaustive experimental data has been acquired from electrical measurements applied to specific test vehicles, proving the validity of the proposed DPS design. The obtained DPS design performance is summarized in Table 7.1.

Description	Value	Units
Maximum input capacitance	15	pF
Crosstalk	<0.5	LSB
Dark current retention time	>2	s
Dark current deviation	10-15	%
Gain retention time	>2	s
Gain deviation	5-10	%
Static power consumption	<1	µW
Biasing deviations (±σ)	±15	%
Read-out resolution	10	bit

Table 7.1 DPS circuit performance

Complementary research has been performed in order to integrate monolithic, 16x16 pixel and hybrid, 32x32 pixel ROICs. Several samples have been already received, being prepared for PbSe post-processing or hybrid packaging. Preliminary optical characterization results from the compact-monolithic imager show a fast response of the system, which is able to operate at speeds as high as 2kfps.

7.2. Dissemination

Along the work reported in this document several publications and patents have been presented, which are summarized in the next points.

7.2.1. Work Related Papers

Already Published

G. Vergara et al.
Monolithic Uncooled IR Detectors of Polycrystalline PbSe: a Real Alternative.
Proceedings of SPIE, Infrared Technology and Applications XXXIII, vol. 6542, 2007.

In this work, the first monolithic device Vapor Phase Deposition PbSe is presented, which uses the 1st DPS generation in order to integrate a 16x16 monolithic 200µm-pitch FPA. As a result, detector suitability for low-cost, fast MWIR imaging is confirmed, leading to frame rates higher than 1000 fps.

F. Serra-Graells, J.M. Margarit, Ll. Terés.
A Self-Biased and FPN-Compensated Digital APS for Hybrid CMOS Imagers.
Proceedings of IEEE International Symposium on Circuits and Systems, pp. 2850-2853, 2007.

This paper presents a new low-power and compact (100µm × 100µm) DPS prototype for hybrid CMOS imagers, including built-in dark current and input capacitance compensation, A/D conversion and a purely digital I/O interface, all at pixel level. Furthermore, full FPN compensation and AGC capabilities are also supplied by digitally pre-programming the individual sensitivity of each pixel during the read-out phase without any speed reduction.

J.M. Margarit, J. Sabadell, Ll. Terés, F. Serra-Graells.
A Novel DPS Integrator for Fast CMOS Imagers.
Proceedings of IEEE International Symposium on Circuits and Systems, pp. 1632-1635, 2008.

A novel DPS integrator scheme for fast CMOS imagers is presented, which combines the advantages of analog APS and DPS circuits. The reset-insensitive integrator proposal improves the linearity of the ADC curve, while it allows both low-power consumption for the active blocks and low-voltage operation for the switching devices even at high frame rates. In this sense, a comparative study is presented in 0.18µm 1-poly 6-metal 1.8V CMOS technology to demonstrate the advantages of this novel solution.

J.M. Margarit, Ll. Terés, F. Serra-Graells.

A Sub-µW Fully Programmable CMOS DPS for Uncooled Infrared Fast Imaging.
Proceedings of IEEE International Symposium on Circuits and Systems, pp. 1424-1427, 2008.
IEEE CAS Sensory Systems Technical Committee's 2008 Best Paper Award.

This paper presents a new low-power and fully programmable digital CMOS active pixel sensor for uncooled and fast IR imagers. In fact, this work is an important design improvement over the previous paper "A Self-Biased and FPN-Compensated Digital APS for Hybrid CMOS Imagers", reporting in this case exhaustive experimental results for two circuit implementations in 0.35µm 2polySi 4-metal technology from AMS: the monolithic, 1st generation realization for PbSe post-processing, and the hybrid, 2nd generation DPS for bump bonding.

Already Submitted

J.M. Margarit, Ll. Terés, F. Serra-Graells.
A Sub-1µW Fully Programmable CMOS DPS for Uncooled Infrared Fast Imaging.
Conference on Design of Circuits and Integrated Systems 2008.

J.M. Margarit, Ll. Terés, F. Serra-Graells.
A Sub-µW Fully Tunable CMOS DPS for Uncooled Infrared Fast Imaging.
IEEE Transactions on Circuits and Systems I.

7.2.2. Work Related Patents

Pending

ES2289878 M. Bigas, E. Cabruja, M. Lozano, F. Serra-Graells, Ll. Terés.
Dispositivo Híbrido Modular para la Lectura de Matrices de Sensores de Imagen.
Oficina Española de Patentes y Marcas, July 2005.

This invention is referred to FPA ROICs, introducing a new hybrid packaging strategy, which consists on a read-out array implementation, through identical and interchangeable ICs, with a total dimension identical to which of the equivalent FPA. The invention also presents a hybrid connection scheme in order to provide fully independence between the physical sensor and the ROIC technology. As a result, this patent proposal introduces a novel cost reduction, performance enhancement alternative for the read-out array, improving technology compatibility between both sensor and circuits and increasing flexibility when scaling the FPA.

P200801428 F. Serra-Graells, J.M. Margarit, Ll. Terés.
Circuito Integrado para la Lectura Digital de Sensores de Imagen de Alta Velocidad.
Oficina Española de Patentes y Marcas, May 2008.

This patent proposal is referred to ROIC imager arrays, introducing a new Pulse Density Modulation topology, as part of the DPS A/D converter, which attenuates signal losses when resetting the analog integrator. Furthermore, CDS noise cancellation is supplied in this invention through the same mechanism. In front of actual state-of-the-art schemes, this proposal presents the advantage of reducing power consumption with no resolution costs.

7.3. Future Work

The further short-term research activities are focused on the layout mask and physical implementation of the modular hybrid approach. In this sense, the global ROIC interconnection scheme is being created, which will distribute both power and control lines along the FPA. Once this layer will be ready, first bumping essays will start in order to adjust the focal plane hybridization process. As a result, a first complete MH (Modular-Hybrid) prototype will be available for characterization, leading to preliminary monolithic-hybrid comparative results.

On the other hand, mid-, long-term design efforts will be especially centered on the third DPS generation: a new compact cell architecture based on asynchronous Addressed-Event Representation (AER) as introduced in Section 4.2.2. in order to scale down the pixel pitch. This new design strategy is also intended to include the lossless integration scheme presented in Figure 5.8 so to improve image acquisition linearity. All the advances will come with further electrical and optical characterization to validate the expected performance, and will be compiled in a future PhD dissertation.

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Annex: Schematics

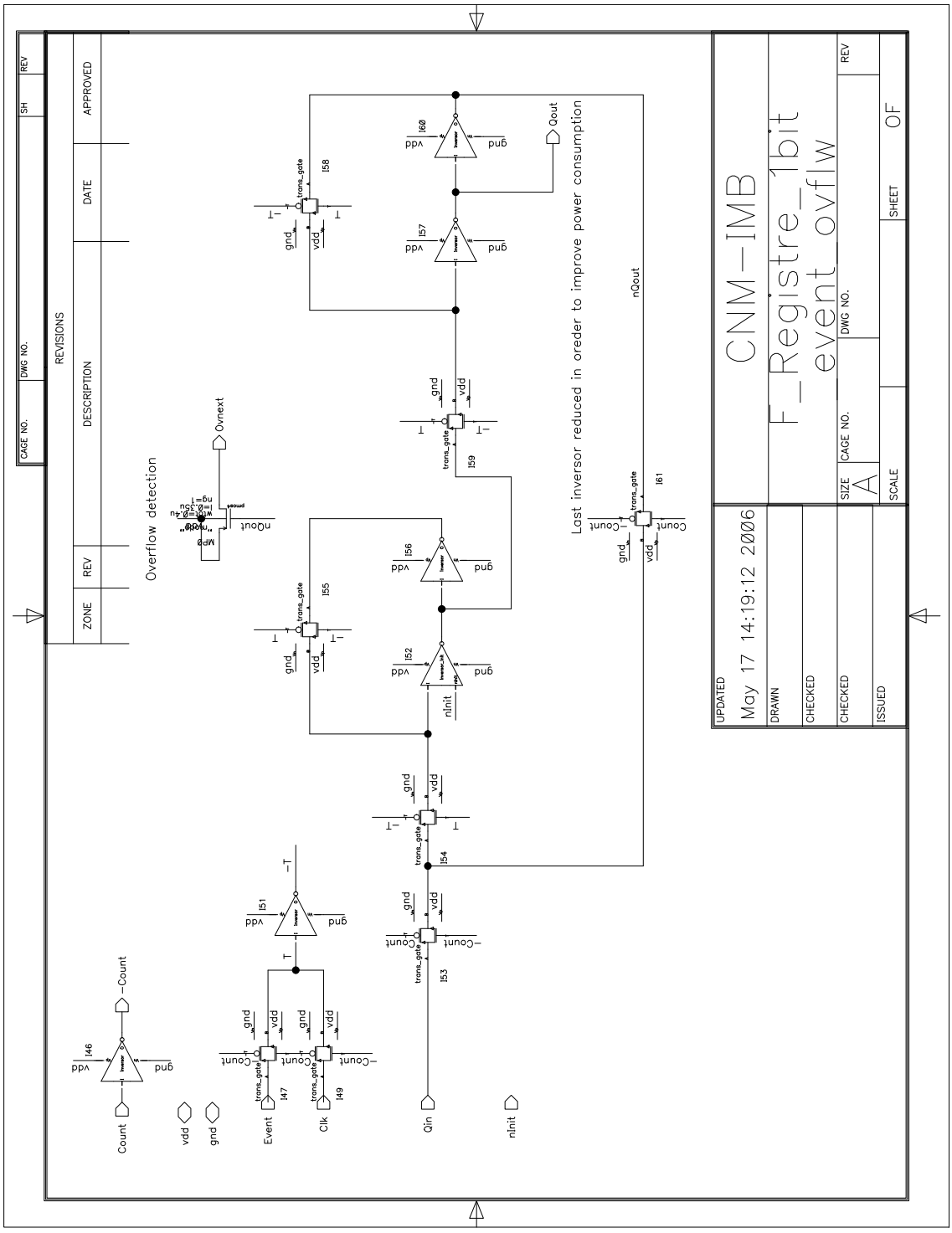

Figure B.1 Common 0, 1st, 2nd generation DPS 10th bit configurable register schematic.

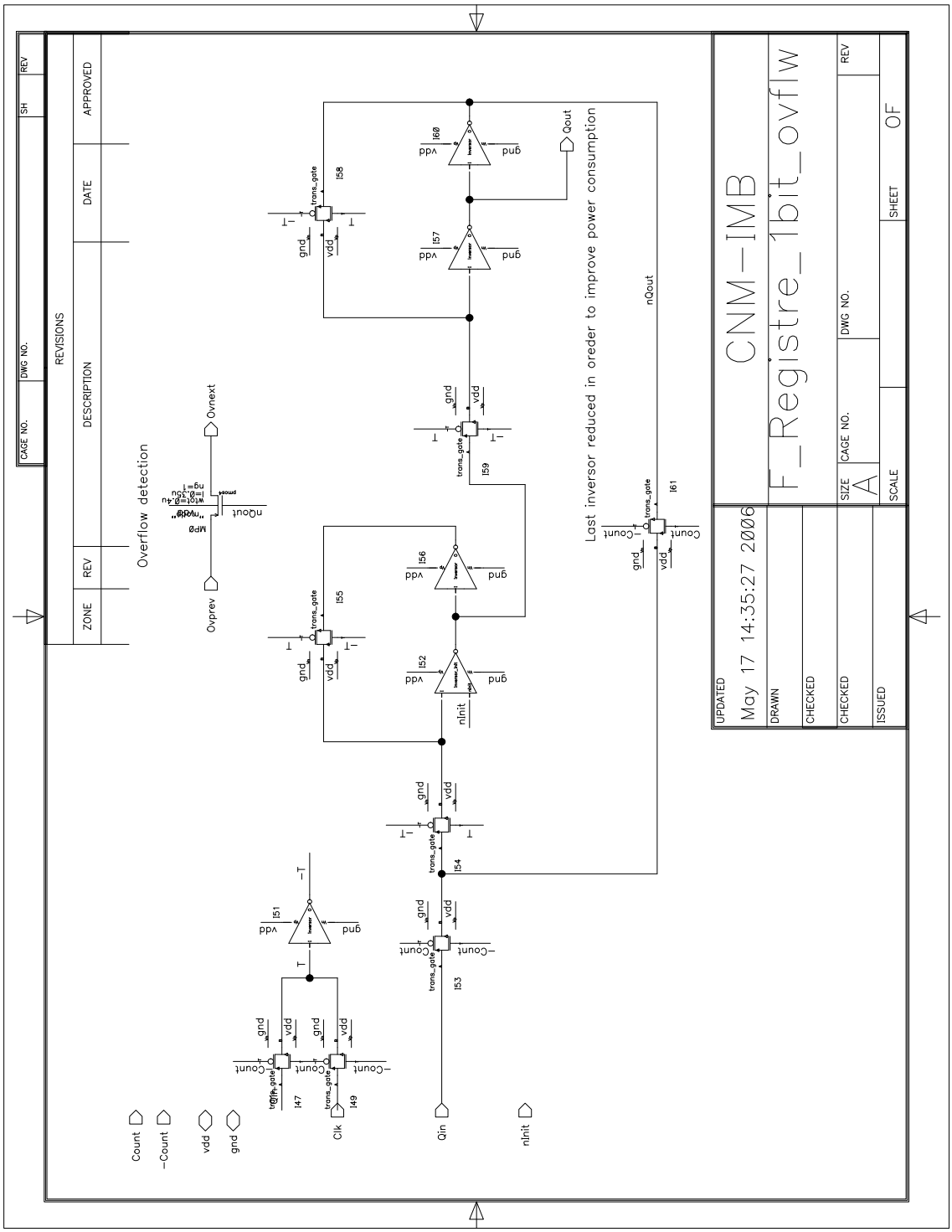

Figure B.2 Common 0, 1st, 2nd generation DPS standard 1-bit configurable register schematic.

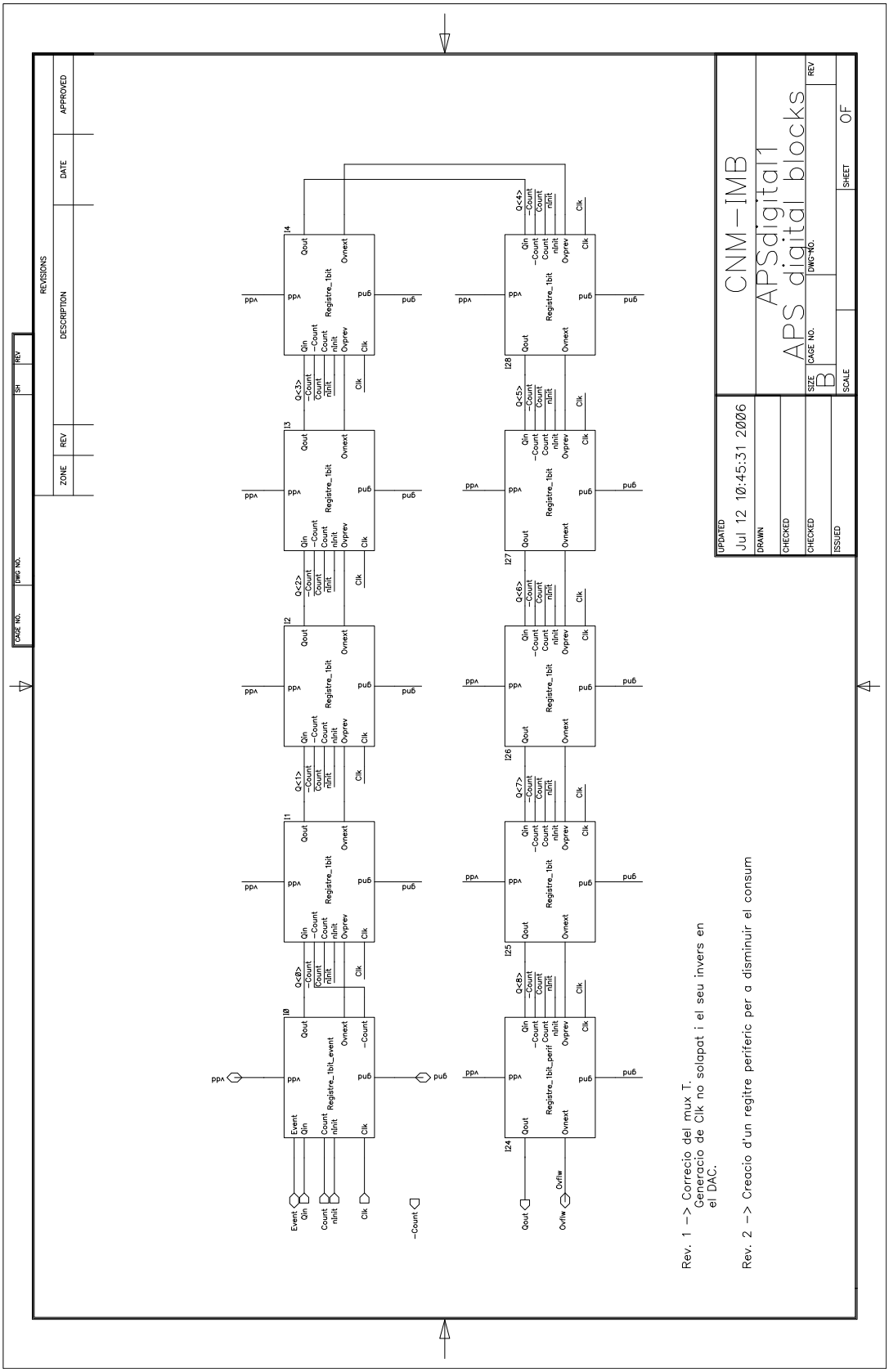

Figure B.3 Common 0, 1st, 2nd generation 10-bit configurable register schematic.

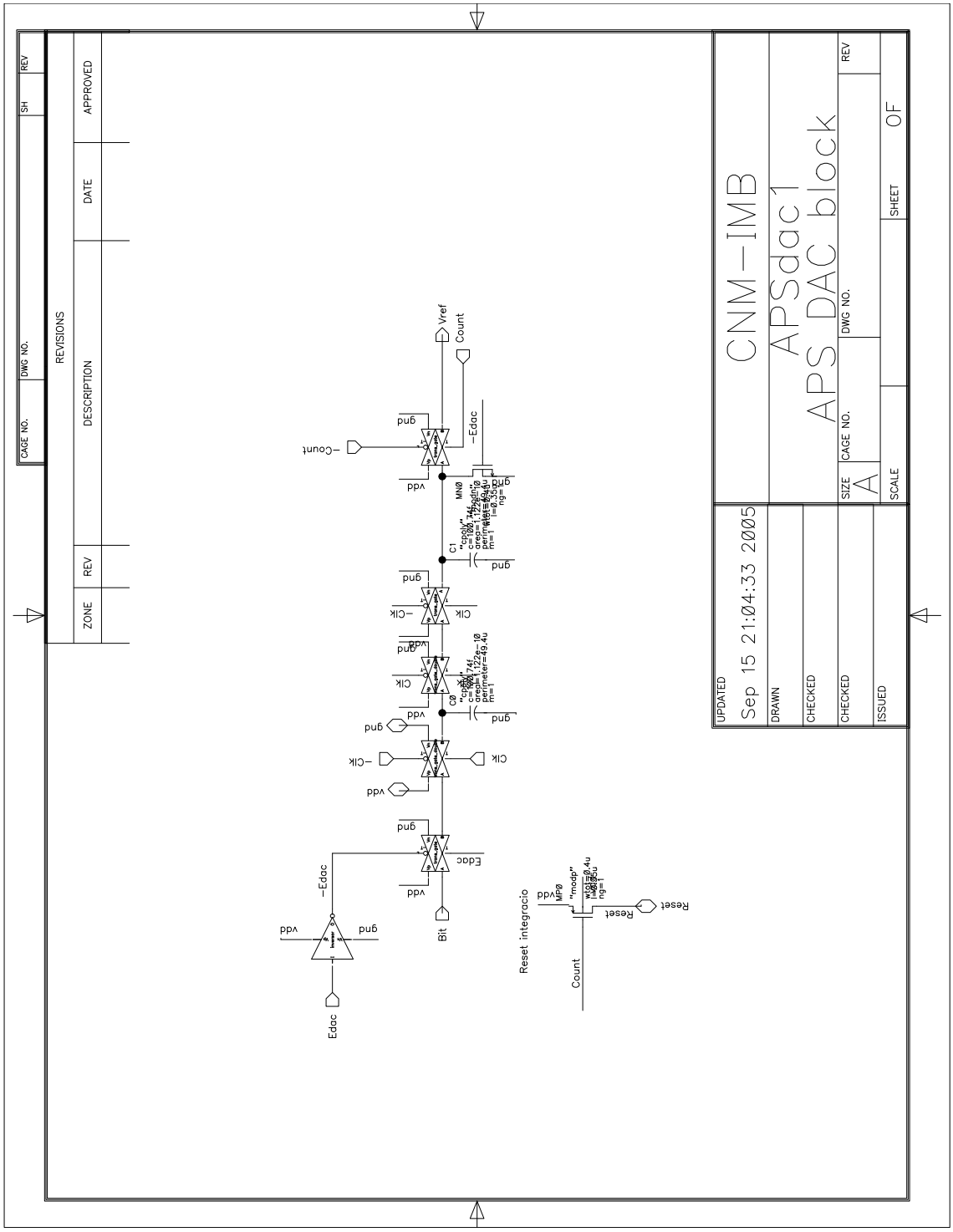

Figure B.4 0 generation switched-capacitance D/A converter schematic.

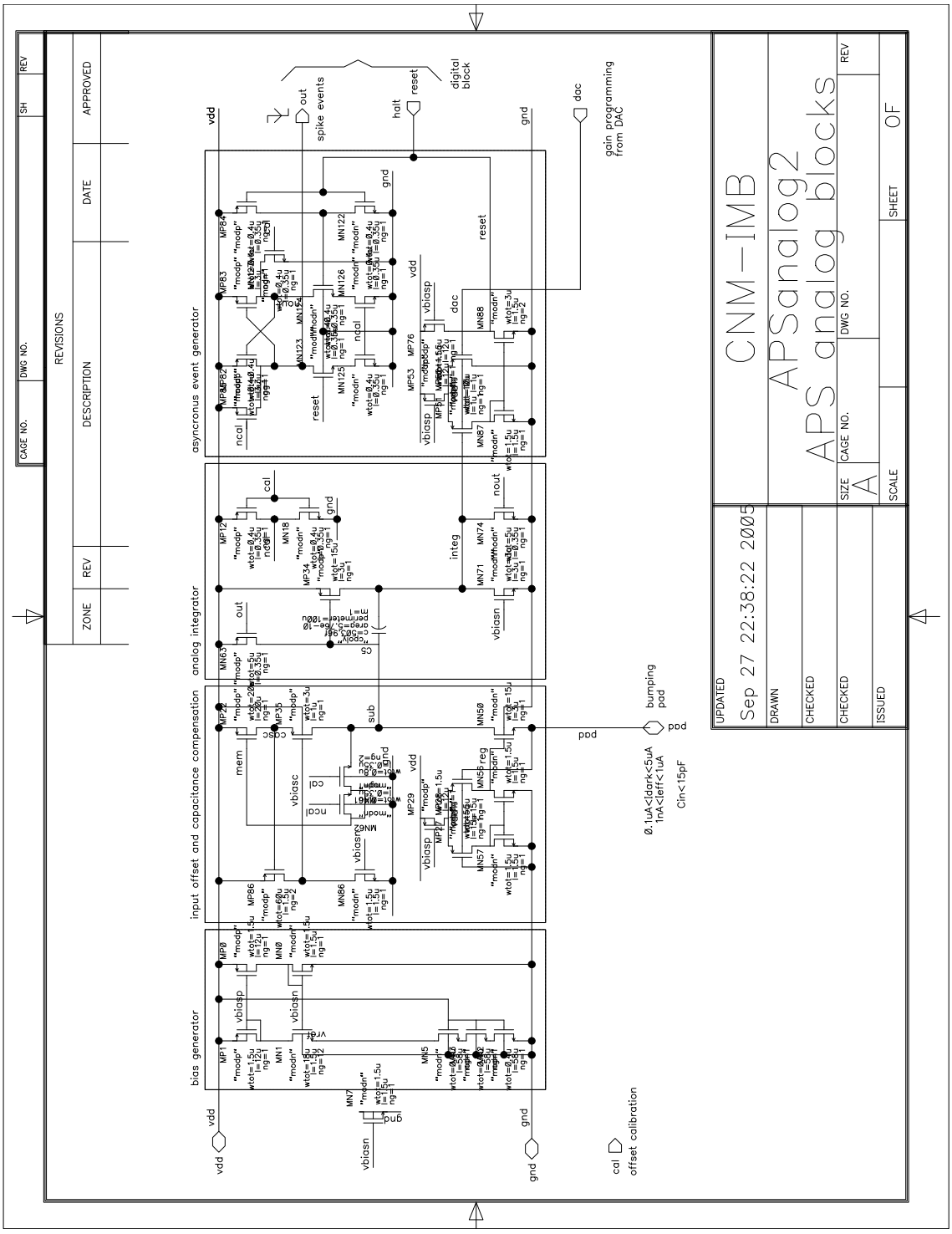

Figure B.5 0 generation DPS analog block schematic.

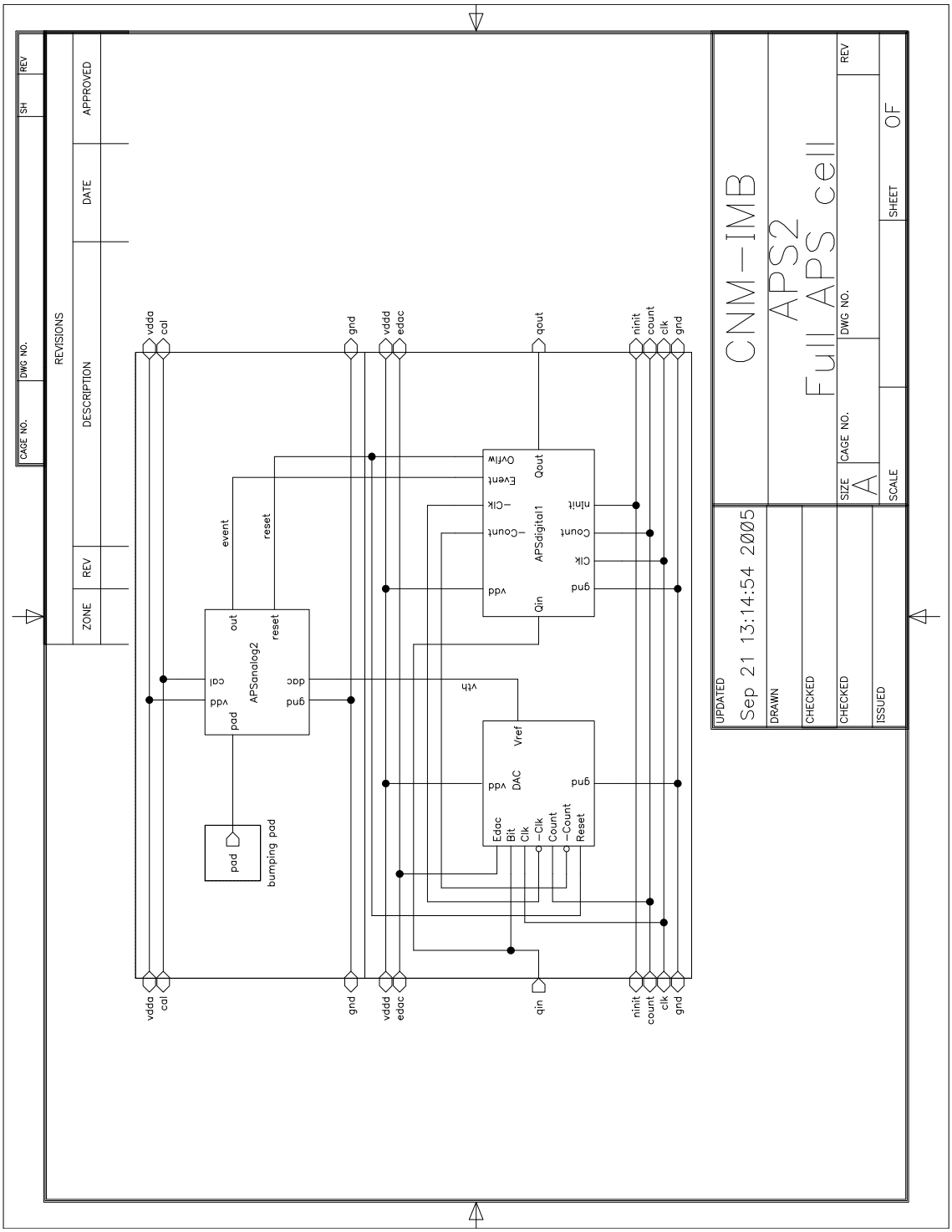

Figure B.6 0 generation DPS full schematic.

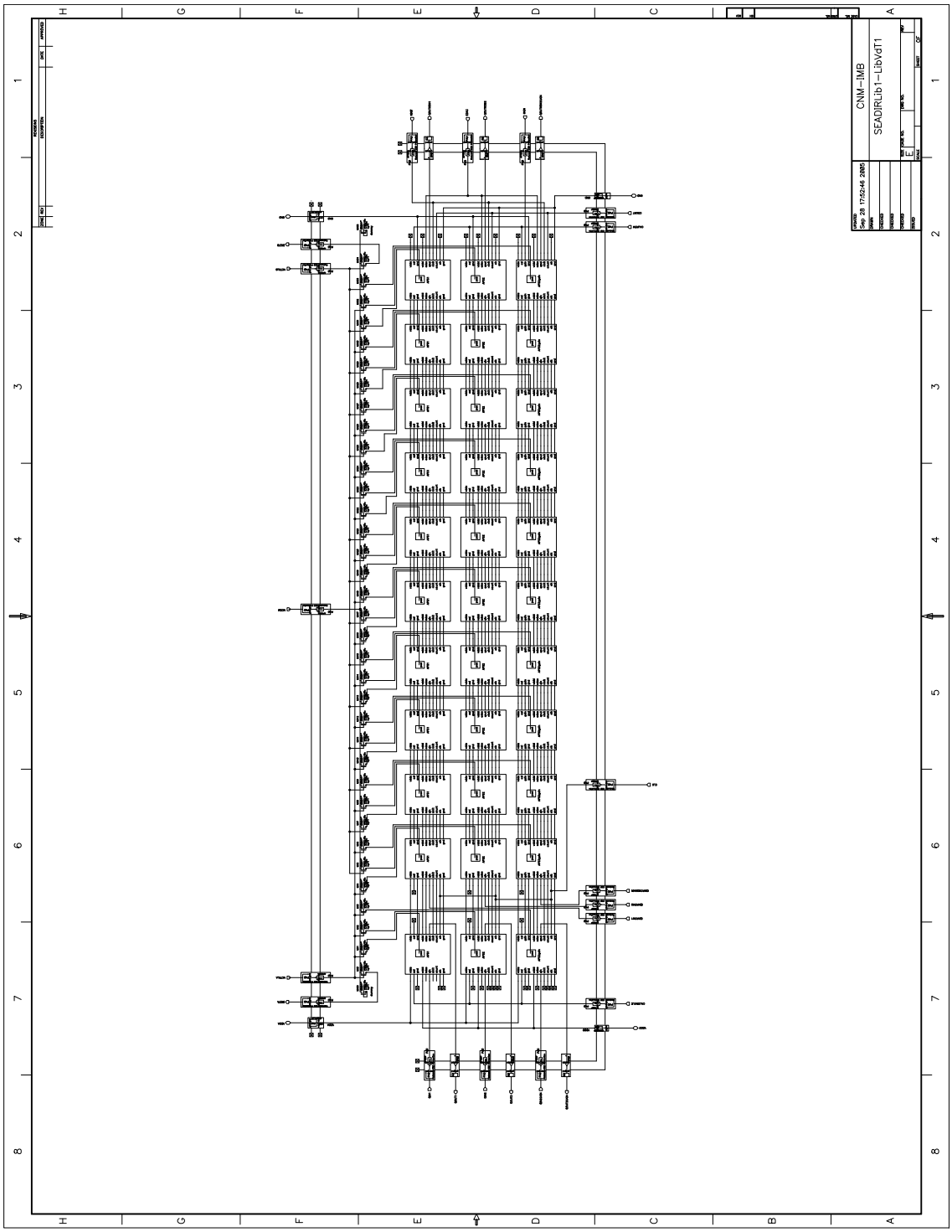

Figure B.7 0 generation test vehicle schematic.

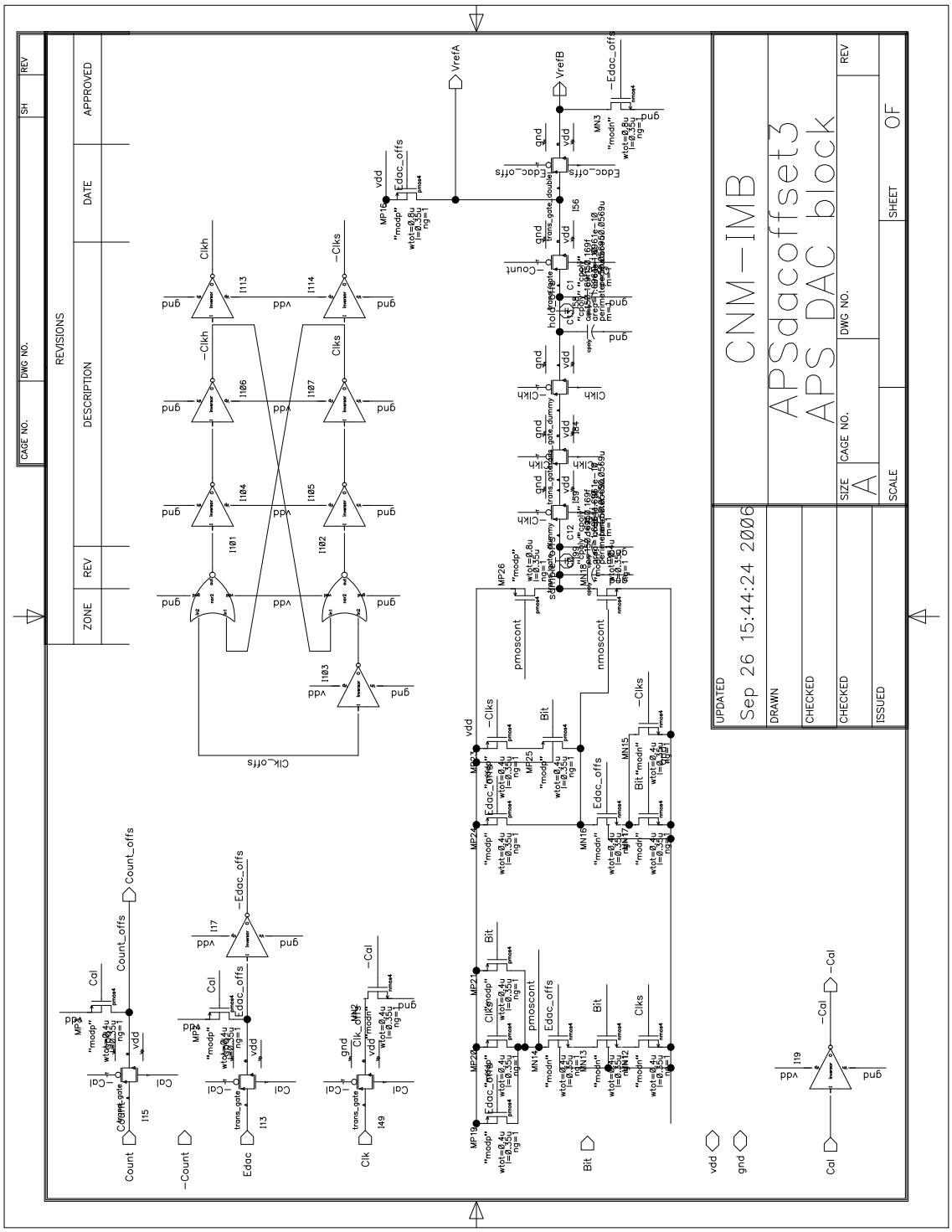

Figure B.8 1st generation DPS switched-capacitance D/A converter schematic for I_{dark} programming.

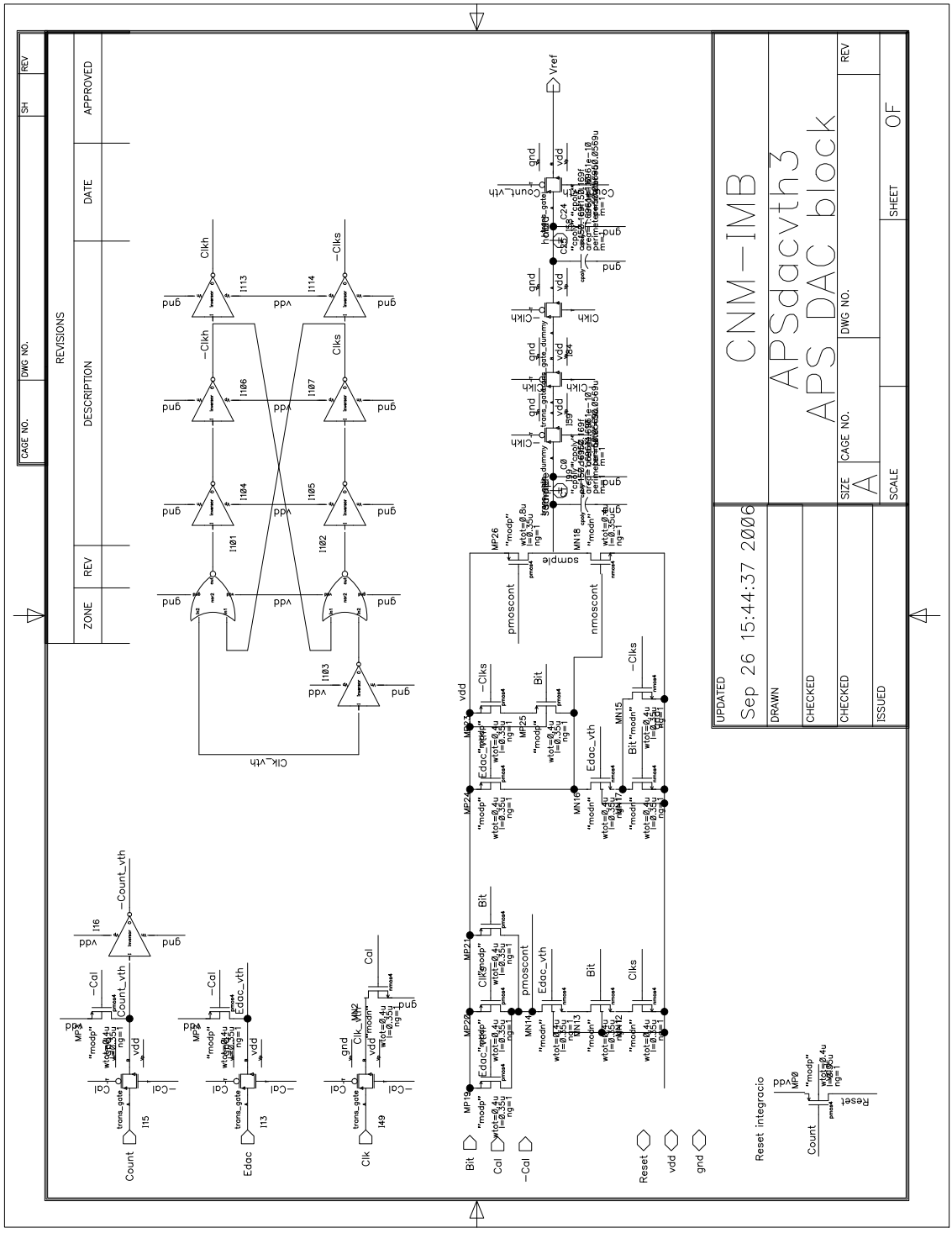

Figure B.9 1st generation DPS switched-capacitance D/A converter schematic for V_{th} programming.

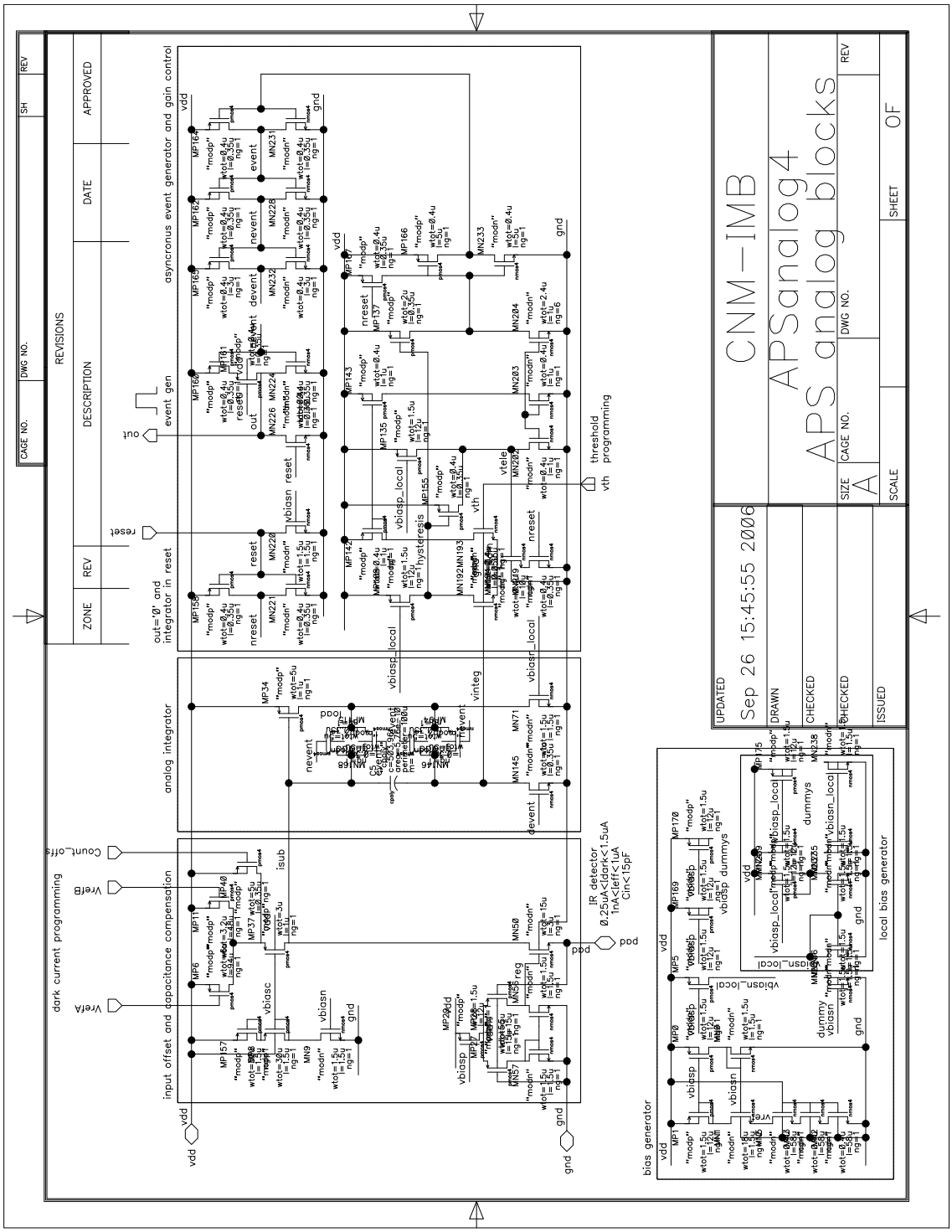

Figure B. 10 1st generation DPS analog block schematic.

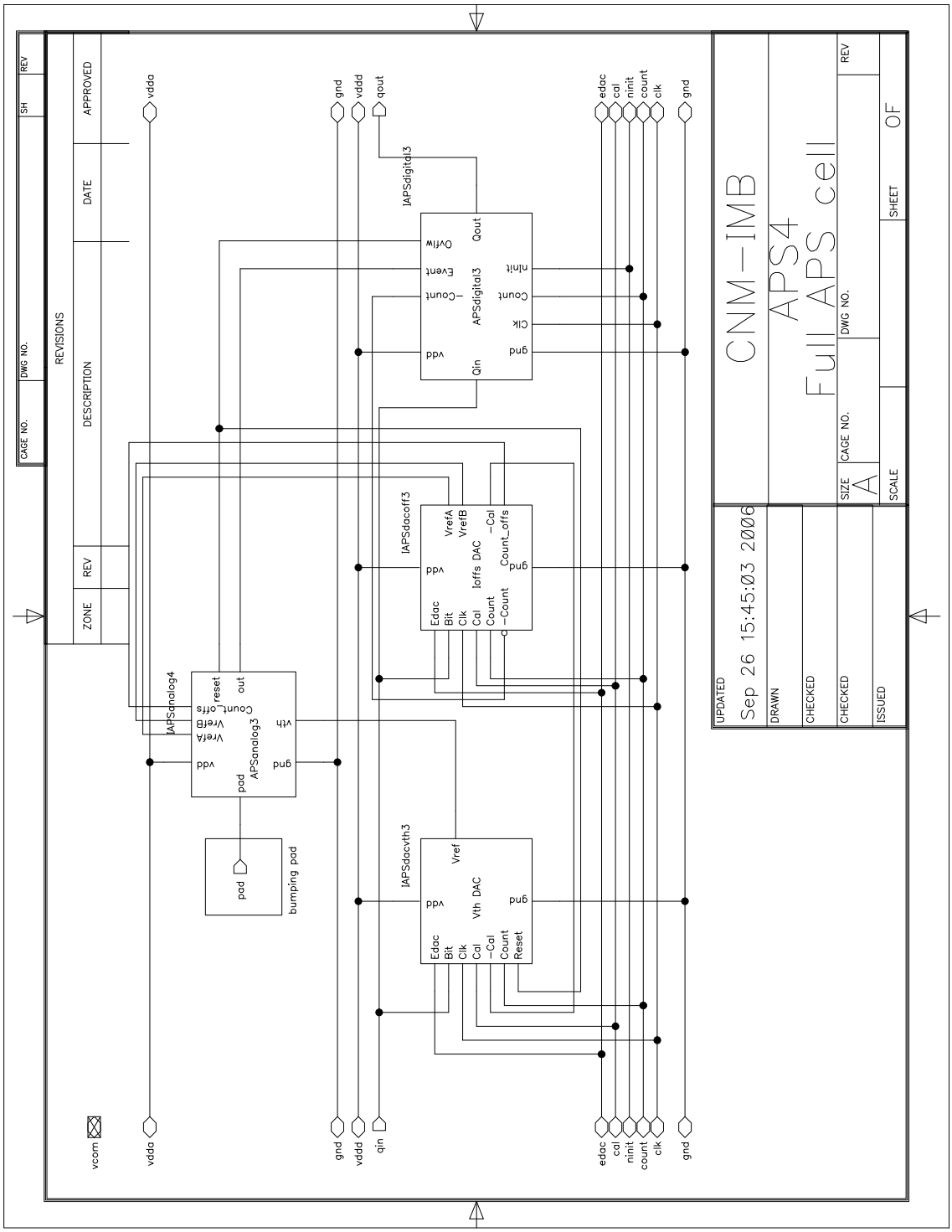

Figure B.11 1st generation DPS full schematic.

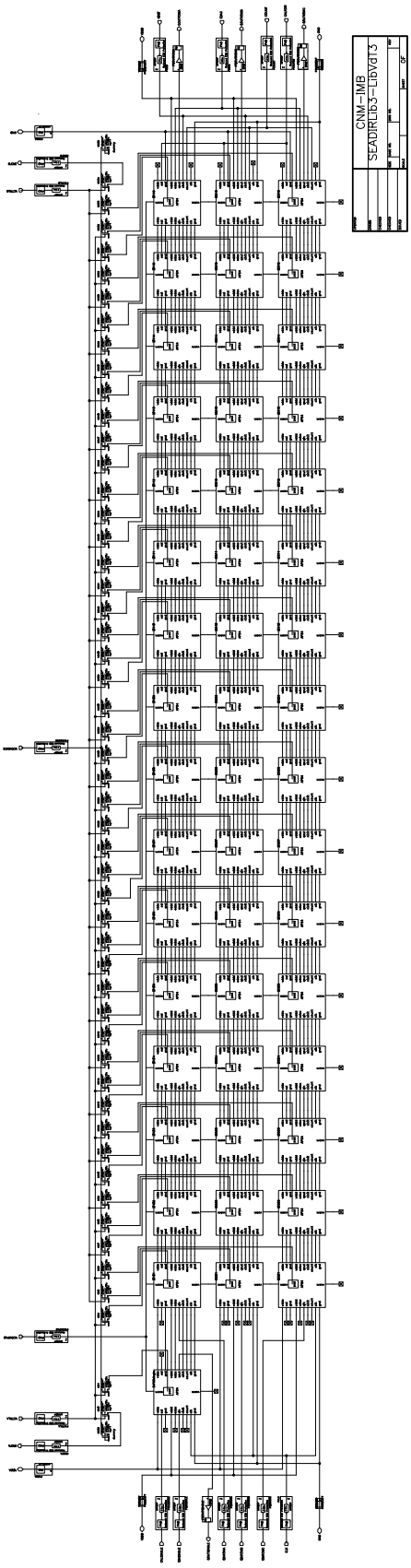

Figure B.12 1st generation DPS test vehicle schematic.

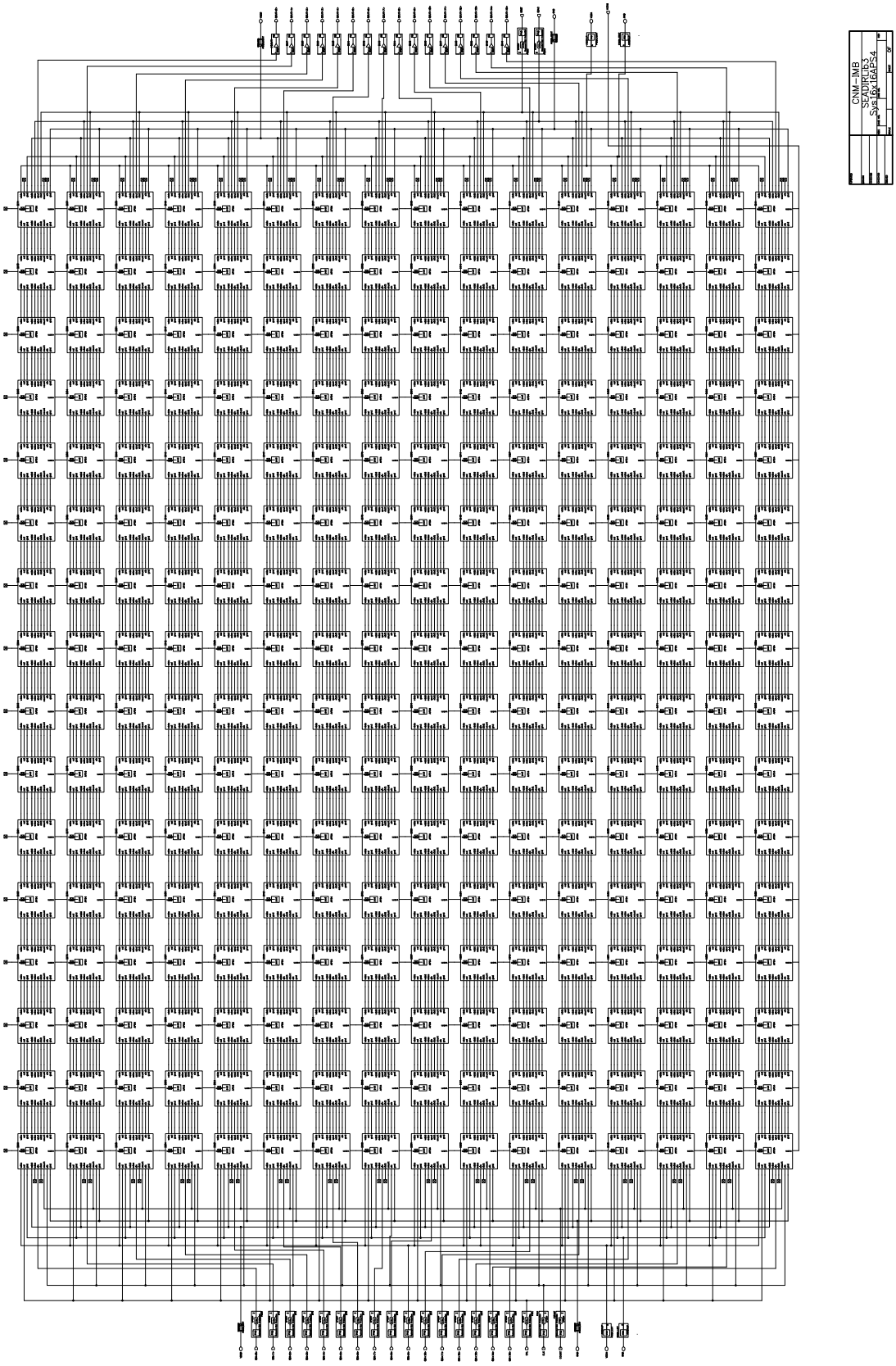

Figure B.13 1st generation DPS 16x16 pix. CM FPA schenatic.

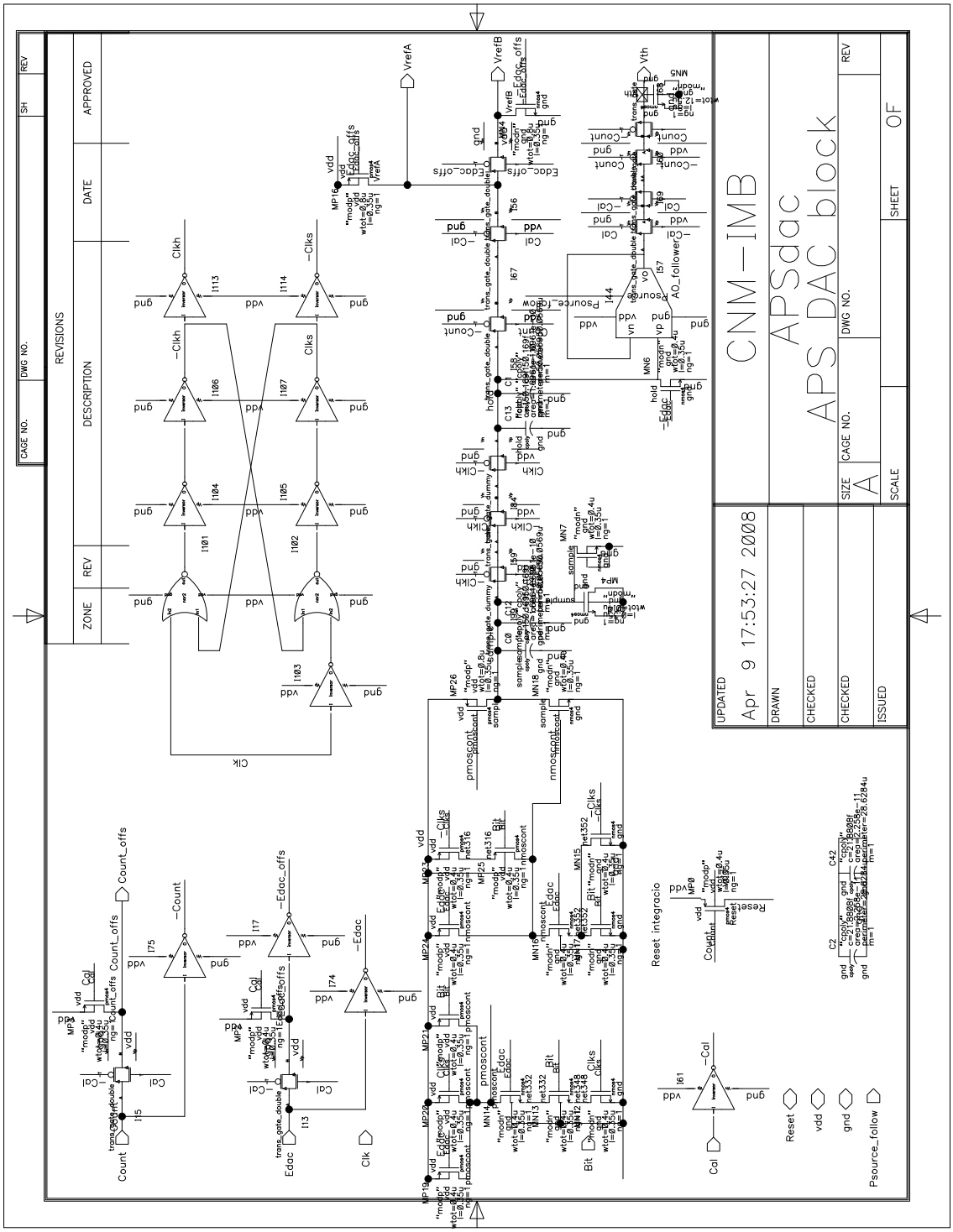

Figure B.14 2nd generation DPS multiplexed D/A converter schematic.

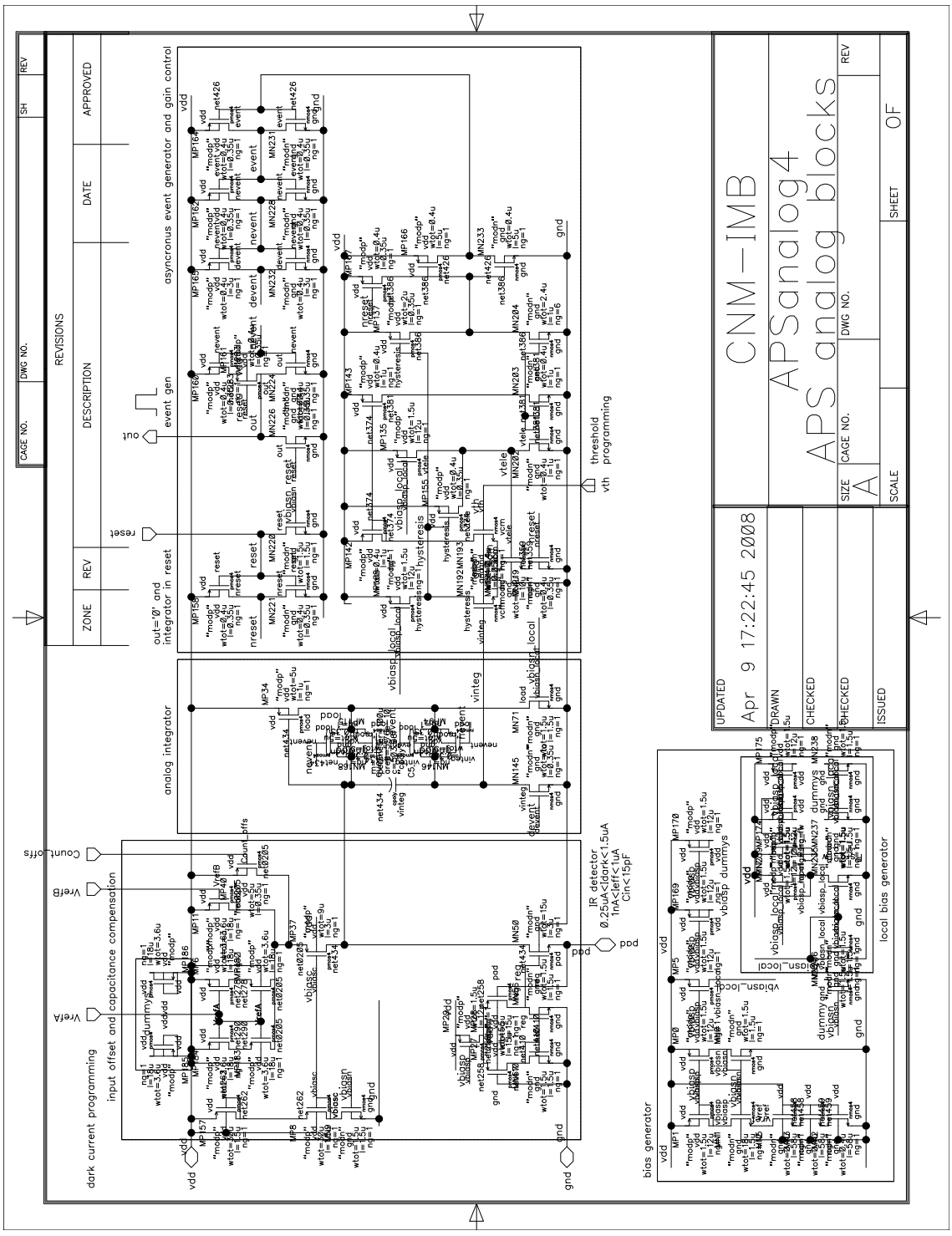

Figure B.15 2nd generation DPS analog block schematic.

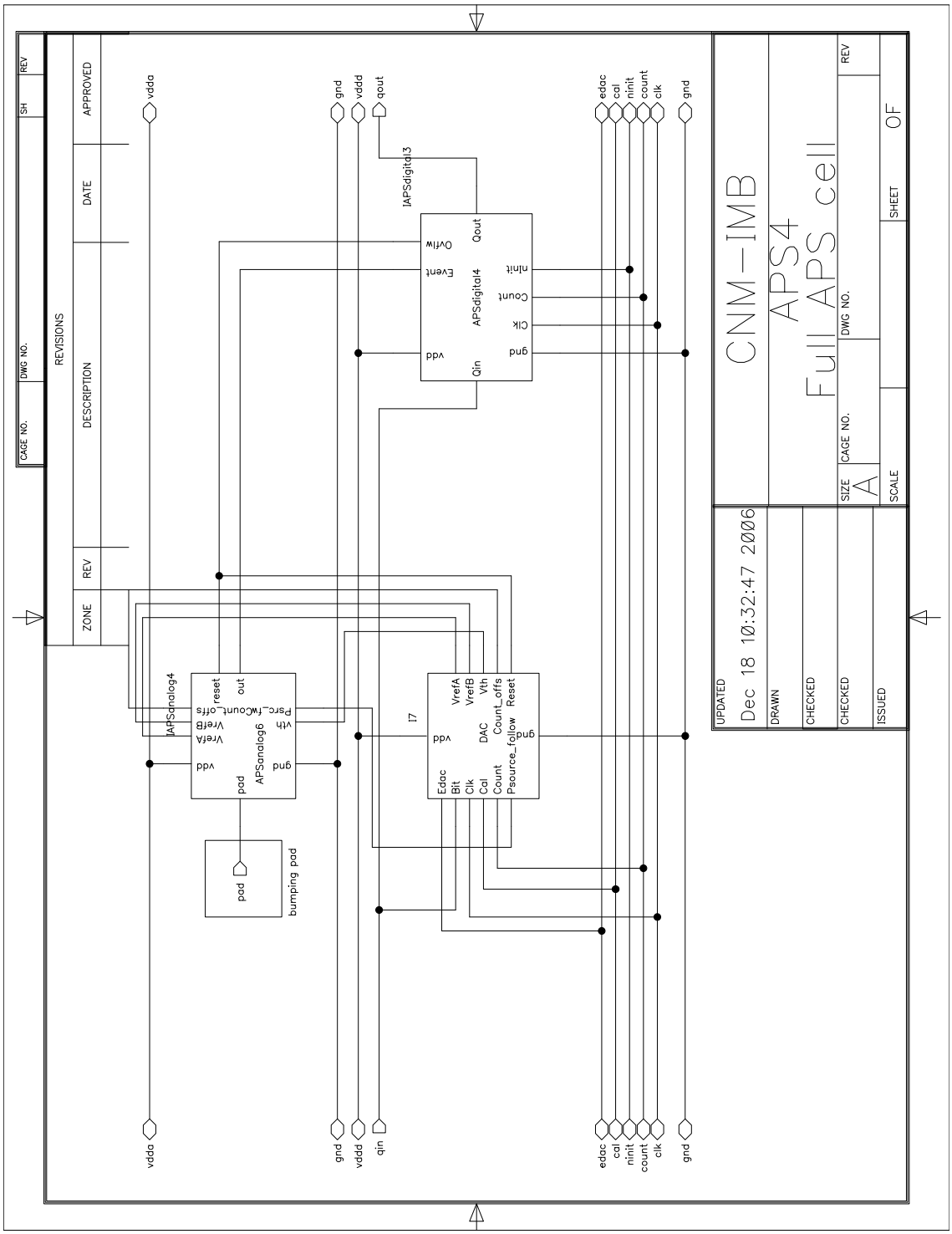

Figure B.16 2nd generation DPS full schematic.

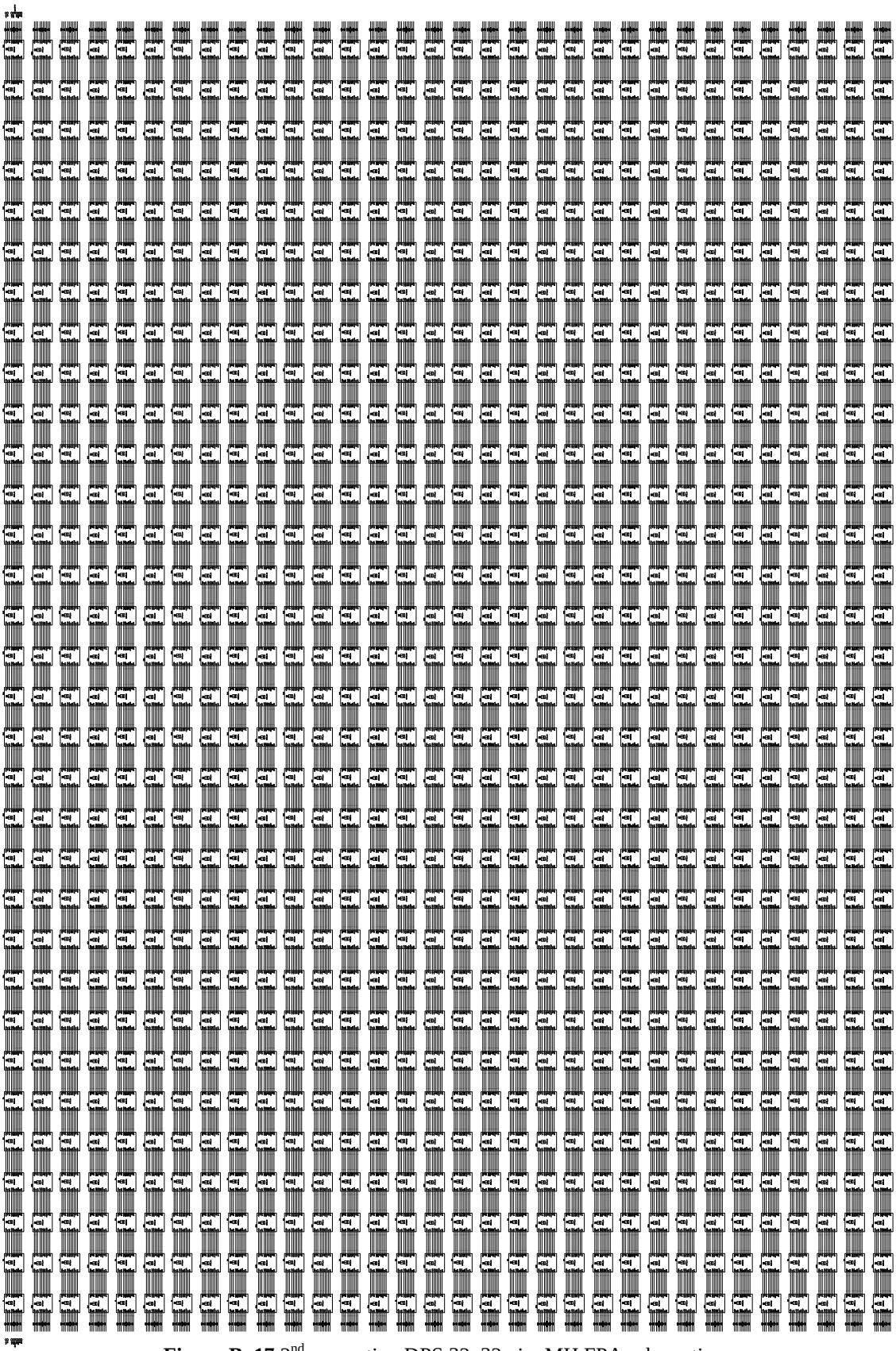

Figure B. 17 2nd generation DPS 32x32 pix. MH FPA schematic.