Polytechnic Institute of New York University

Master Thesis

Symmetric ±270V DC Power Supply of a Universal Power Converter for Airborne Applications

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August 16, 2010

Abstract

The trend of the last years in the aeronautic industry is to reduce the weight of the commercial aircrafts. This weight reduction implies the need for more electrical power on board, since the heavy hydraulic drive system is replaced by and an electromechanical system. In order to supply this amount of extra electrical power, a Symmetric ±270V DC Power Supply as a part of a Universal Power Converter is presented in this thesis. The Universal Power Converter generates the different airborne voltages - 32VDC, ±270V DC and 230V AC- using as Fuel Cell Stack as raw energy supply.

The thesis focus on the the power conditioning system includes three DC-DC converters, generating regulated ±270V DC output. The first stage, a 3-phase interleaved full-bridge soft-switching converter, so called *V6*, boosts the Fuel cell voltages to a non regulated DC-Link bus with a voltage between the 320 and 580 Volts. The following stage, composed of a SEPIC converter and Cúk converter parallel connected and in interleaving operation provide the regulated output. The three converters of the proposed conditioning system has been studied obtaining the design equations, sized the components and then verified with computer simulations using Matlab Simulink. The simulation results show regulation in the entire range of load with and excellent result within the Continuous Conduction Mode of the converter, a high performance of 93% at full load and a small current ripple at the Fuel Cell input, less than 17% peak-to-peak of the drawn current at full load.

Furthermore, this thesis presents the Universal Power Converter at system level, to place the reader in context. The system supplied with a 16kW Proton Membrane Fuel Cell is designed to generate different outputs: 32Vdc at 5kW, ±270Vdc at 16kW and 230Vac at 16kW; supplying at a time three, two or one voltage. Furthermore, the selected Fuel Cell is introduced and a Simulink model is build to perform simulations of th econverters.

To my parents for their unconditional support whenever I need and wherever I am.

Contents

List of Figures

List of Tables

Preface

This thesis arouse from my internship in the Power Group of the Polytechnic Institute of New York University, with the Associate Professor Dariuz Czarkowsi as a internship supervisor. During the internship Boeing Corporation requested for a design of a Universal Power Converter (UPC) for airborne applications. In order to work and develop this project a work group formed with different MS and PhD students was created, which I got involved as a internship student. The thesis is the product of the work done during my internship in the PolyNYU.
The opportunity to work with the Universal Power Converter, give me the chance to improve my knowledge on the subject of the Power Electronics and the Switched-Mode Power Supply. Moreover, since the project was a technological challenge, it boosted my interest on this subject of the Electrical Engineering. During the time I dedicated to this thesis I had the chance to discover a large number of concepts and technologies around the world of the Power Electronics, which where merely or completely unknown for me, such as: Fuel Cell technology, interleaved techniques for SMPS, current model control, current sharing, planar magnetics technology. The resulting experience in the PolyNYU was successfully for my professional career and a better personal experience from my personal sight.

Thesis Organization

This thesis has been organized into two parts:

- Part I: Introduction to the UPC System
- Part II: UPC Power Converters Design

Part I, as its name indicates, introduces the concepts at the system level of the Universal Power Converter and the related technologies that this system involves; without entering into the design aspects of the Power Converters. Part II, focuses on the design process of the different Switched Power Units

that composes the system; developing the design equations for each converter, sizing the components and finally validating the design with the simulation tool Matlab Simulink.

This organization separates the thesis in a two parts, on more descriptive which will help to place the reader in context, and the second part completely technical where the reader will figure out the design process of the converters.

Part I

Introduction to the Universal Power Converter System

Chapter 1

Universal Power Converter

The current tendency in the aeronautics industry is to reduce weight of new commercial aircraft models. Lighter airplanes reduce fuel consumption, consequently the costs of the airborne transportation and the polluting emissions decrease. The benefits of weight reduction are an important issue for the flight companies and also a compromise with the sustainable development, hence it is an interesting research topic for the aeronautics industry.

One way to go in the weight reduction of the aircraft is replacing the old steering system -based on a hydromechanics system- with an electrical steering system. Furthermore, the heavy cables, pipes and rods that bind the cabin with the moving parts of the plane (actuators) are substituted for electrical lines which transmit the steering information to the actuators. As a consequence, the amount of electrical power needed in the aircraft increases -to feed the electrical steering system.

The idea of the Universal Power Converter (UPC) comes form the need of more electrical power in the new aircrafts. So the goal of the UPC is to supply this extra power using a Fuel Cells stack (FC) as a raw electrical source and generate the different voltages needed in the aircraft.

The goal of this chapter is to present the requirements of the Universal Power Converter, and discuss at system level the way to generate the different voltages. However power converter names and other power electronics concepts will appear, they will not be explained or clarified in this chapters.

1.1 System Description

The goal of the Universal Power Converter is to supply different voltages levels current used in aircrafts with a fuel cell as raw electrical energy source. The unit shall be designed to meet aerospace standards for power quality and Electro-Magnetic Interference (EMI) as specified by the RTCA Standard DO-160 Environmental Conditions and Test Procedures for Airborne Equipment or as provided by Boeing.

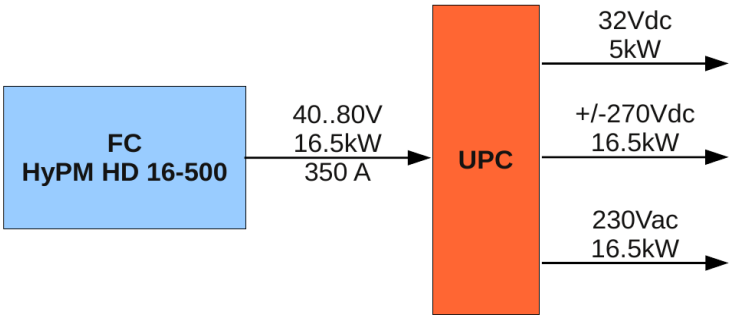


Figure 1.1: Voltages and powers of the UPC system

The power electronic converter has to provide the following regulated aircraft voltages 32V DC , ±270V DC and 230V AC within the frequency range from 400Hz to 800Hz. The power requirements for the outputs are 5kW for the 32V DC output and 16.5kW -maximum FC power- for the other outputs, as figure 1.1 shows.

The fuel cell candidate is the HyPM® HD 16-500 of Hydrogenics, since it has the highest power density of the series HyPM which is suitable for transportation systems. The main characteristics are: nominal power 16.5kW, output voltage range between 40-80 VDC and weight 114kg. Some restrictions of the fuel cells that will compromise the design are the no inverse current drawn capability, low input current ripple and slow dynamics. The chapter 3 is dedicated exclusively to the Fuel Cell technology, where we will dig into this technology more deeply.

1.2 System Topology

The topology of the UPC is determined by the output voltage range of the fuel cell -we can see the most relevant characteristics in the Table 1.1. Another important factor for the topology is the availability of all, two of them, or just one voltage output at a time. Figure 1.2 shows the solution proposed that fullfills the UPC requirements and overcomes the restrictions of the fuel cell.

The system is composed by two subsystems, power delivery and power backup. The first one encompass all the converters dedicated to generate the regulated output levels of the UPC -part of it is the focus of this thesis. The second one, connected to the FC with dashed wires, could be added to backup the FC and improve its slow dynamics, f.e. in case of a load step the super-capacitor will supply the extra power need until the FC delivers the required power.

The power delivery system is composed of four statics converters. A buck converter steps-down the fuel cell voltage to generate the regulated 32Vdc output. A boost converter steps-up the FC voltage above 320Vdc, providing an unregulated DC Bus for the *symmetric buck* converter and the inverter. The *symmetric buck* steps-down the bus voltage generating the regulated ±270V output and the inverter generates the 230Vac output between 400-800Hz. The presented topology allows all type of outputs available in any combination. Notice that the total drawn power extract from the FC can not exceed 16.5kW, so the outputs should split the power or in case of one of the 16.5kW output is supplying the maximum power the other outputs should be disconnected, otherwise the FC could be damaged.

The power backup system is composed of a super capacitor and a bi-directional

Table 1.1: FC specifications UPC requirements

Name	**Value**
FC Model	FC HyPM® 16-500
FC Nominal Power	16.5 kW
FC Voltage Bounds	40 - 80 Vdc
FC Max. Current	350 A
UPC Out Voltages	32 Vdc ±270 Vdc 230 Vac
UPC Nominal Power	5 kW 16.5 kW [max FC pwr.]

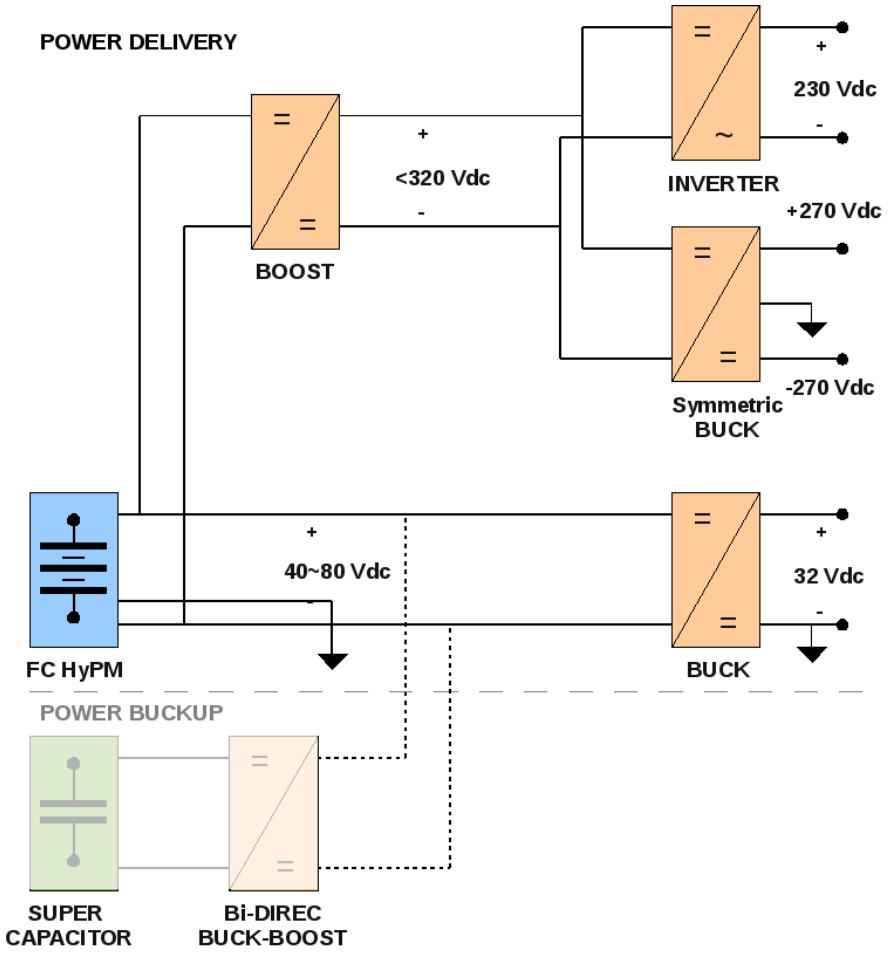


Figure 1.2: System topology

power converter. The super capacitor stores some energy to deliver at any time in case of strong load changes, the bi-directional buck-boost converter controls the charge and discharge of the super-capacitor. As you could see in the Figure 1.2 the power backup is optional, hence this two blocs are represented with thin colors and connected with dotted wires to the FC. We will not go in further explanations about the power backup subsystem, however we would like to introduce this concept here due to the fact that FC based systems usually adds power backup systems.

1.3 Converters Topologies

Once the system topology has been defined, a hard work have been done to decide the topology of each converter. The selection criteria is given by two facts: the first in terms of performance to make the UPC suitable for airborne application; the second in terms of electrical characteristics to accomplish the FC and UPC power quality specifications.

The performance factors of the UPC set by Boeing are (order by relevance): weight, volume and efficiency ; so the goal is to achieve a unit with the highest power density (W/kg) possible, even against the efficiency loss. With this idea in mind, we adopt some restrictions in our design space. First, reduction the size of the magnetics (inductors and transformers), since the major contribution in weight and volume is due to this components. And second, the use of fast switching semiconductors, such as Power MOSFETs, IGBTs and Ultra-Fast or SiC Diodes.

In the other hand, the use of a FC as energy source is a challenge for the overall system. Due to its I-V characteristic the voltage decreases as the load increases, so the system is not set to a constant operating point; instead it must operate in a dynamic operating point because changes in the load will also affect the FC voltage. In addition, the FC has some other limitations, it can not accept power, so it does not allow inverse current; as well drawn current must to be continuous and current ripple not too large, hence both have a negative effect on the efficiency and lifespan of the FC unit.

The diagram of the figure 1.3 could help to better understanding the dependence of the system on the FC stack, it shows the system topology with the power, current and voltage that each converter have to manage. Actually, the most critical power stages are the ones that connect directly with the fuel cell -the buck and the boost converters - because they have to deal with high currents, in the order of hundreds of amperes. Also, the out voltage range of the FC, 40 to 80 volts, determine the conversion nature of those converters, so for the 32V output a buck converter is needed and for the DC link bus at 320V a boost converter. Finally, all the converter stages should have continuous input current, beside small input current ripple amplitude.

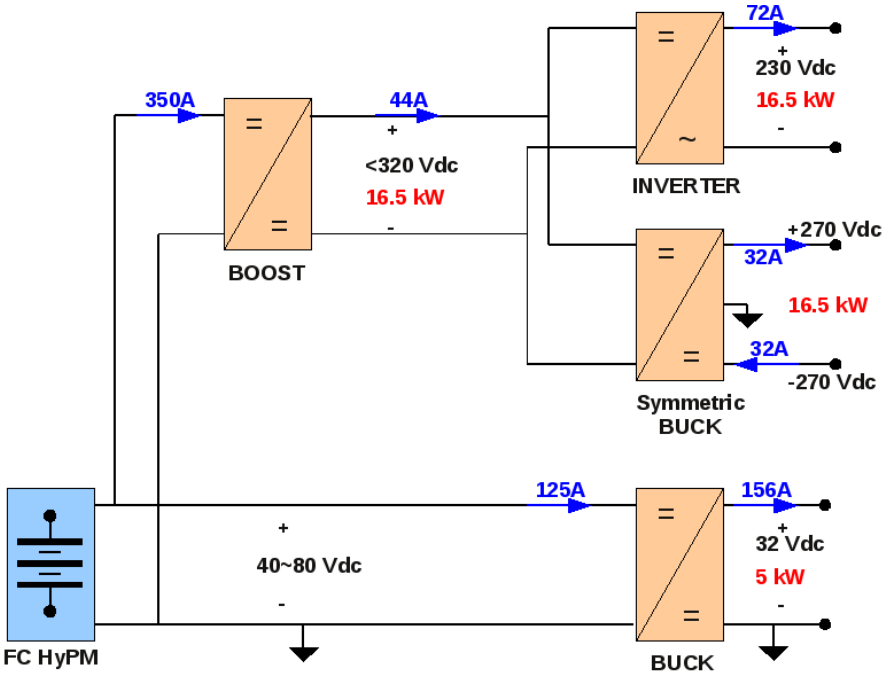


Figure 1.3: Power, voltages and maximum currents values of each converter

Based on the previous considerations the final topology candidates are:

For the 32Vdc output: A 4-phase interleaved buck converter.

For the DC link: A 3-phase interleaved full-bridge isolated converter, called *V6*.

For the 270Vdc output: A SEPIC converter generates the positive output and the Cuk generates the negative. The converters operate 180 degrees out of phase, like a 2-phase interleaved buck converter, and the composition of them operate as a single converter that we named *Symmetric converter*.

For the 240Vac output: A 3-phase inverter.

Three of the candidates are interleaved converters, actually the buck and the boost stages are pure interleaved converters, the SEPIC and the Cuk only take some advantages of this concept. In this way, the converters can deal with this high currents at high frequencies, hence the energy storage elements (magnetics) keep small in size, so do the volume of the converters. Also, interleaved converters mitigate the current ripple amplitude and current discontinuities by harmonic cancellation fact that allow the reduction of the filtering components

(capacitors). The next chapters focus on the study analysis of the *V6* converter and the *Symmetric* converter. The other aforementioned topologies has been presented to place the reader in context and have a better understanding of the UPC.

Chapter 2

Fuel Cell Technology

A fuel cell is a system that produces electrical and thermal energy from an electrochemical reaction, like a battery. Unlike a battery it does not run down of charge or it does not need to be recharged, it will produce energy as long as fuel is supplied.
A fuel cell consist of two electrodes sandwiched around a electrolyte. In an hydrogen fuel cell, hydrogen is feed on the anode side and and oxidant (oxygen or air) is feed on the cathode side. Encouraged by a catalyst the hydrogen atom splits into a proton and an electron, which take different paths. The protons go through the electrolyte. The spare electrons generate a current that can be used before they return to the cathode, and then reunited to the hydrogen proton and the oxygen into a molecule of water as exhaust product.

Since a fuel cell operation relies on chemistry reaction and not combustion, the emissions are much smaller than the cleanest fuel combustion engine.

2.1 Selected Model

Proton Exchange Membrane (PEM) is the suitable fuel cell technology type for mobile applications. PEM fuel cells operate in a relatively low temperature range, 80° C (175° F), have a high power density and can vary their output quickly to meet shifts in power demand.

A series of Hydrogenics 4.5, 8.5, 12, and 16.5 kW HyPM® fuel cells provide 20-40, 20-40, 30-60, and 40-80 Vdc at the output, respectively. These fuel cells differ only slightly in volume and mass. Hence, the 16.5-kW fuel cell is selected as a model cell for aircraft applications. As sold by Hydrogenics, this fuel cell

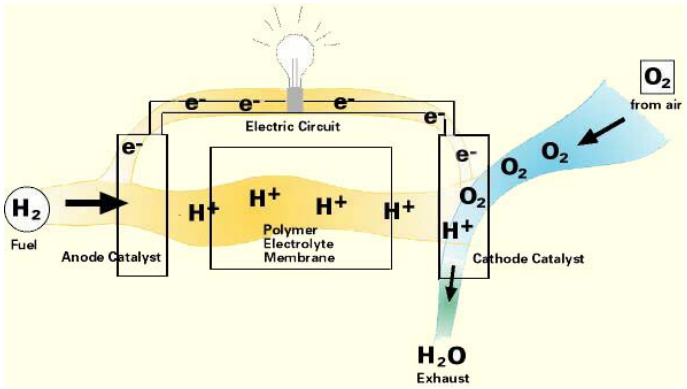


Figure 2.1: Hydrogen fuel cell diagram

dimensions are 910 x 448 x 312 mm and its weight is 114 kg. These size-weight parameters could be further decreased by removal of covers and some monitoring circuitry. NYU-Poly is in possession of full specifications of Hydrogenics fuel cells under a confidentiality agreement.

2.1.1 System Specifications

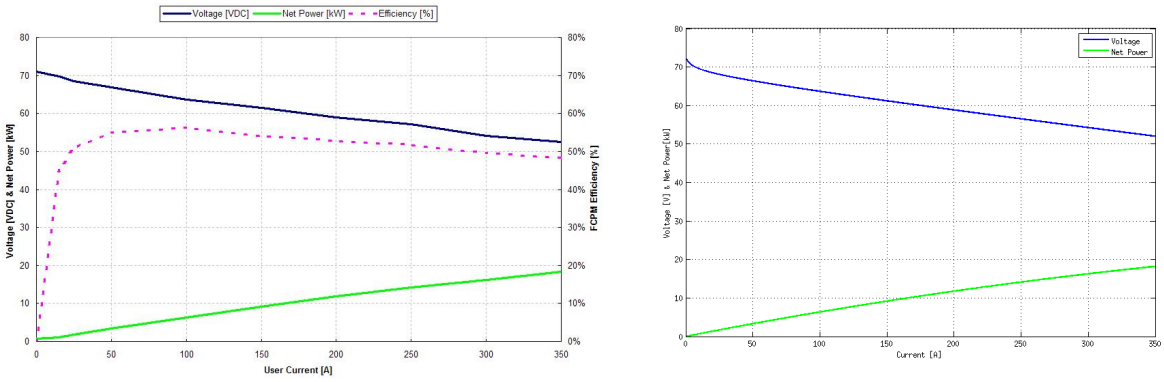
The full technical specification document of the *Hy-PM 16-500* could be found in the annex 1, however the most relevant values are in the table 2.1.

Table 2.1: Main specification of the HyPM-HD-16-500

Property	**Unit**	**Value**
Performance		
Net Electrical Power	kW	16.5
Operating Current Range	A_{DC}	0 to 350
Operating Voltage Range	V_{DC}	40 to 80
Peak Efficiency (@100A)	%	56
Physical		
Dimensions (L x W x H)	mm	910 x 448 x 312
Total Mass	kg	114
Volume	L	127
Emissions		
Water Collected (Anode + Cathode)	mL/min	< 56
Noise (@350A, 1m distance)	dBA	< 70

In the figure 2.2 *a*, we could appreciate the typical I-V characteristic (blue

line). Here the output voltage, varies between 72V in open circuit, to 56V at full load. This I-V characteristic will change during the lifetime of FC, however the out voltages will keep within the range given in the technical specifications (40V to 80V).



(a) HyPM-HD 16-500

(b) Simulink model

Figure 2.2: Typical performance

Other relevant aspects are:

- The PMFC has a CAN interface to query and control the system
- An overall system controller capable of communicating via the CAN interface to control the PMFC is required
- The user (or the system controller) must avoid to exceed the maximum power rating
- The user (or the system controller) must avoid to exceed the Current Draw Allowed (CDA) value, sent by the PMFC via CAN
- Provide reverse current protection for the PMFC
- The PMFC must not run below 10% of its rated power during more than 5 minutes
- Maximum peak to peak current ripple on the PMFC must not exceed 5% of the system current draw
- A fuel supply and a cooling system is required by the PMFC
- External power supply of 12V, 300W is required to start-up the PMFC

2.1.2 Power Converter Design Considerations

As we explained in the previous chapter, the UPC topology has a strong dependence on the fuel cell electrical characteristics. During the design process we needed to make some considerations about the output voltage and current of the FC system in order to dimension the converters components.

We adopted the I-V characteristic given in technical documentation, figure 2.2 *a*, as the standard output characteristic and build a Simulink model to run simulations, see in the figure 2.2 *b* the model I-V curve and in the figure 2.3 the Simulink model. From the build model, 3 pairs of values have been extrapolated to use as points of operation : at the maximum power rating, at half power and at about 10% [1] of the maximum power rating.

Table 2.2: Extrapolated values from the I-V model

Net power (kW)	**Voltage (V)**	**Current (A)**
16.50	54	305
8.25	62	133
2.14	68	31.5
14.00	40	350

The two first extrapolation points are chosen considering that all the converters operate in continuous conduction mode (CCM) from full load to half load; however we sized the components to handle the fuel cell voltage in minimum load conditions- this is the third point. Since the I-V characteristic will change during the lifetime of the fuel cell, we added another pair of values extracted from the specifications sheet, we considered in the worst case the fuel cell will give 40V at 350A.

Figure 2.3 shows the Simulink model build to model the behavior of the FC. The system is composed by a controlled voltage source, *PMFC* block, where the output current is measured, *Iin* block, and used as a feed back signal. The measured current is limited between the 0-350 amperes, to do not exceed the I-V curve boundaries, and low-pass filtered, *FC Dynamics* block, to emulate the slow dynamics of the fuel cell. Then LPF output value is the input for a look-up table, *I-V Char* block, with the I-V characteristic of the fuel cell, and the output signal of this block closes the loop connection to the input of the

[1] Is the minimum power rating that the FC must provide.

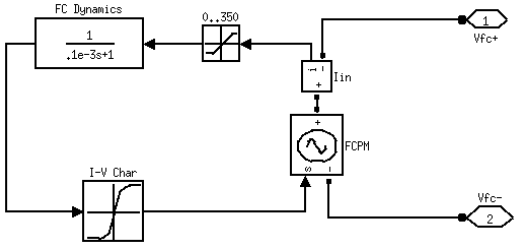


Figure 2.3: Fuel Cell Simulink model

voltage controlled source, *PMFC* block.

Since we did not have any information yet about the dynamics of the fuel cell, we set an arbitrary vale of $\tau = 100\mu s$ to give some dynamics to the fuel cell, but without aggravate the simulation time. The *FC Dynamics* block should be enhanced when we get the fuel cell dynamics specifications.

Part II

UPC Power Converters Design

Chapter 3

V6 converter

The *V6* converter steps-up the Fuel Cell voltage generating the DC bus link for the PWM inverter and the *Symmetric converter*. The DC link voltage must be at least 320V to guarantee a good power quality at the inverter output; and deliver 16.5 kW -the maximum FC power.
This topology has been chosen among other candidates [1–4], for the following reasons:

- High step-up conversion ratio
- High power capability
- Isolation
- Reduced transformer turns ratio
- High Efficiency
- No filtering components
- Soft switching

Besides this reasons, this topology has a relevant disadvantage: it has no regulation; so its conversion ratio is constant and can not be regulated in anyway. However, the regulation in the outputs is a achieve through the converters connected to the DC-Link bus.

This chapter is entirely dedicated to the *V6* converter divided in four sections. The first section introduces the converter at circuit level and how works the converter . The second section develops the model and extracts the design equations of the converter. The third section puts values to the converter and

sizes the components using the equations of the previous section. The fourth section does a rough estimation of the losses and the efficiency of the converter, and the last section presents the results from the simulations.

3.1 Topology Description

This topology is extracted from the work of [5]. The converter is composed by three full-bridge DC-DC converter, each one connected to an independent transformer. The secondary windings of the transformers are connected in a wye configuration to the bridge rectifier. You could see the circuit in the figure 3.1.

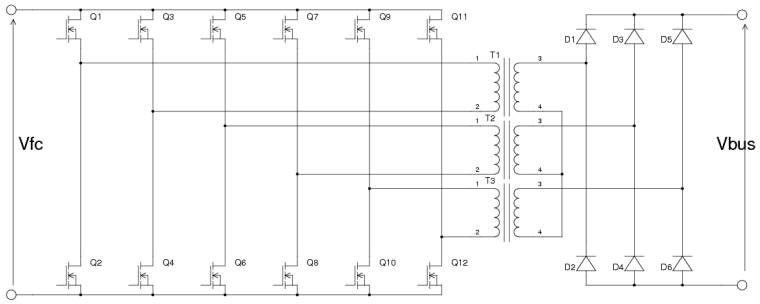


Figure 3.1: Circuit of the V6 converter

The resulting circuit is an interleaved full-bridge converter with 3-phases, where each phase is operated synchronously, but shifted 120°. The circuit may be controlled either with the classical pulse width modulation (PWM) control or with phase shifted modulation (PSM) control. Operating the circuit in PSM and setting the angle shift (α) as control variable, the converter has two modes of operation, divided in the following cases: when $0° < \alpha < 120°$ and when $120° < \alpha < 180°$. For a more accurate analysis of the converter operation you could read [6].

In the first case, the averaged output voltage is:

$$V_{OUT} = \frac{\alpha}{60°} n V_{FC} \tag{3.1}$$

in the second case, the averaged output voltage is:

$$V_{OUT} = 2nVFC \tag{3.2}$$

where n is the transformers turns ratio.

The second case, is the operation mode used for the *V6* converter of the UPC, so no more details of the first operation mode will be given in the thesis.
The following section does a detailed analysis of the operation of the second operating mode, extracting the equivalent model and the equations of the circuit.

3.2 Steady State Circuit Model

When the converter operates with a phase angle above 120° at least two and at most three phases transfer power to the output, see circuits of the figure 3.3. Since the secondary windings of the transformers are conected in wye configuration the voltage at the output terminals of the converter is always proportional to the input by the factor $2n$, therefore there is no regulation. Owing to the fact that the conversion ratio is a constant we could say that the converter behaves like a DC-DC transformer. The *V6* does not modify the waveform of the current and the voltage, besides the small ripple noise cause of the commutation. Hence, the converter does not requires the output filter stage.

The figure 3.2 shows the most relevant signals of the converter, operating the circuit with a phase shift angle of 150°. We could see that the voltage waveform of three phases is shifted 120° from each other, marked with the dashed orange lines. Considering the transistors ideal switches , the voltage amplitude at left winding of the transformer is fuel cell voltage, V_{FC}, and its applied during during $\alpha = 150°$ in this example, marked with the orange line. u,in green, is the equivalent duty cycle, it is value between 0 and 1 that represents the phase shift angle within the boundaries of 120° and 180°; this variable is created to simplify the equation derivation.

From this graph, when the three transformers are conducting, two of them are connected in parallel with the fuel cell terminals and the other in anti-parallel, as the circuit in the figure 3.3 *a*. In the other case, when just two of them are conducting (figure 3.3 *b*) , the two primaries are connected in ant-parallel (with the fuel cell terminals reversed). Due to the wye connection of the secondaries, the windings with opposite voltages result in a series connection, and the windings with same voltage in a parallel connection. Due to the fact that there is always two primaries with opposite voltages, there is all the time two secondaries connected in series, so the output voltage is always the sum of them.

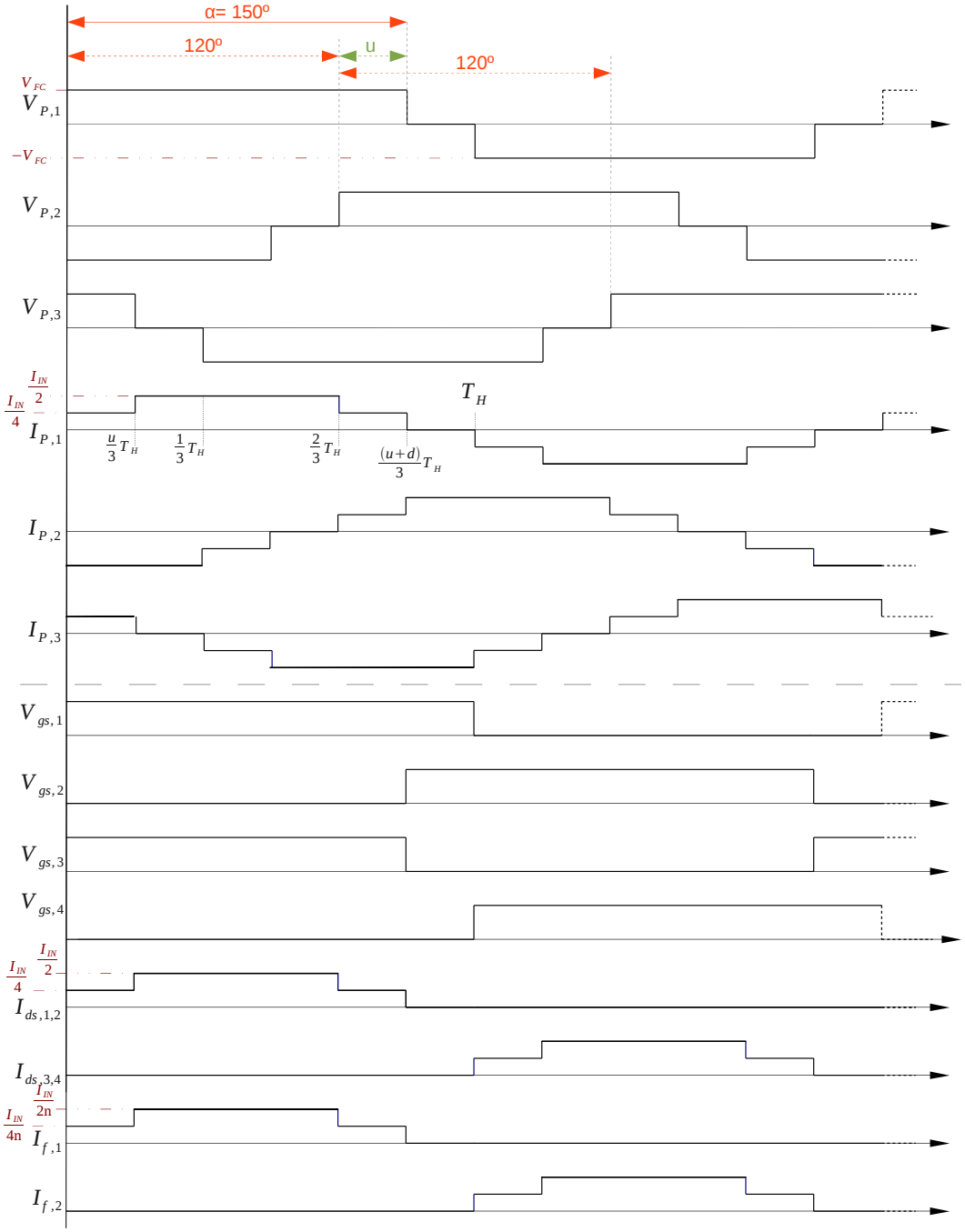
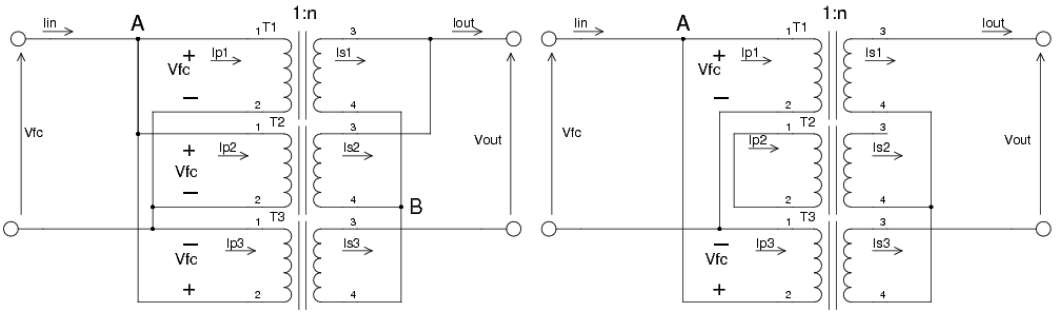


Figure 3.2: Operating the converter with a phase angle of 150°:
$V_{P,x} \rightarrow x$-phase transformer primary winding voltage
$I_{P,x} \rightarrow x$-phase transformer primary winding current
$V_{gs,x} \rightarrow x$ transistor gate voltage
$I_{ds,x} \rightarrow x$ transistor channel current
$I_{f,x} \rightarrow x$ diode forward current



(a) Three phases conduct (b) Two phases conduct

Figure 3.3: Generic states of the converter

In case of two transformers conducting, the voltages in the primaries are

$$V_{P1} = V_{FC} \quad V_{P2} = 0 \quad V_{P3} = -V_{FC} \tag{3.3}$$

and the secondaries voltages are

$$V_{S1} = nV_{FC} \quad V_{S2} = 0 \quad V_{S3} = -nV_{FC} \tag{3.4}$$

hence, the out voltage is:

$$V_{OUT} = V_{S1} - V_{S3} = nV_{FC} - (-nV_{FC}) = 2nV_{FC} \tag{3.5}$$

So the converter conversion ratio is:

$$\frac{V_{OUT}}{V_{FC}} = 2n \tag{3.6}$$

The resulting circuit model of the converter is shown in the figure 3.4, it is as simple as an ideal transformer with a conversion ratio of $2n$. Since, the converter operates in open-loop there is no need for the small signal analysis.

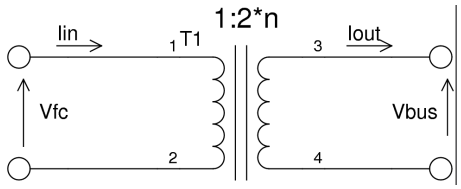


Figure 3.4: Circuit model of the converter

As we explained before, there is at least two and at most three phases conducting. In the first case, the converter input current (I_{IN}) is divided equally

in each phase, so the primaries of each converter conduct the half of the input current. The currents in the A node of circuit b figure 3.3 are,

$$I_{IN} = I_{P1} - I_{P3} \tag{3.7}$$

in the output there is only one net, so the currents are,

$$I_{OUT} = I_{S1} = -I_{S2} \tag{3.8}$$

hence, the currents in the primary keep this relation,

$$I_{P1} = -I_{P2} \tag{3.9}$$

substituting in 3.7 we obtain

$$I_{IN} = I_{P1} - (-I_{P1}) \Rightarrow I_{P1} = \frac{I_{IN}}{2} \tag{3.10}$$

The second case is not that evident, there is two of the primaries connected in parallel -with the fuel cell terminals at V_{FC} voltage, so their secondaries are as well connected in parallel. The remaining winding is connected in anti-parallel -with its terminals upside-down with the FC terminals at $-V_{FC}$ voltage, so its secondary winding is connected in series with the other two windings, thus conducting the sum of the current of the other windings. As a result, the two phases in parallel conduct the half of the current, and the remaining phase conducts the other half of the total current amount.
The currents in the node A in circuit of the figure 3.3 a are

$$I_{IN} = I_{P1} + I_{P2} - I_{P3} \tag{3.11}$$

and the currents in the node B are,

$$-I_{S3} = I_{S1} + I_{S2} \tag{3.12}$$

hence, the currents in the primaries keep this relation

$$-I_{P3} = I_{P1} + I_{P2} \tag{3.13}$$

and assuming the transformers are identical, T1 and T2 conduct the same amount of current, so

$$-I_{P3} = 2I_{P1} \tag{3.14}$$

substituting in 3.11 we solve the equation for I_{P1} and I_{P3}

$$\begin{aligned} I_{IN} = 2I_{P1} + 2I_{P1} \quad &\Rightarrow \quad I_{P1} = I_{P2} = \frac{I_{IN}}{4} \\ I_{IN} = I_{P3} + I_{P3} \quad &\Rightarrow \quad I_{P3} = \frac{I_{IN}}{2} \end{aligned} \tag{3.15}$$

The figure 3.2 shows the current waveform in the primary winding of the first transformer. We can obtain the RMS value for the current, since the signal is symmetric the calculation is done for one half-period, thus

$$I_{P,rms} = \sqrt{\frac{1}{T_H}\int_0^{T_H} i_p(t)^2\,dt} =$$

$$\sqrt{\frac{1}{T_H}\left[\int_0^{\frac{u}{3}T_H}\left(\frac{I_{IN}}{4}\right)^2 dt + \int_{\frac{u}{3}T_H}^{\frac{2}{3}T_H}\left(\frac{I_{IN}}{2}\right)^2 dt + \int_{\frac{2}{3}T_H}^{\frac{u+2}{3}T_H}\left(\frac{I_{IN}}{4}\right)^2 dt\right]} \tag{3.16}$$

solving the integrals, we have

$$\sqrt{\frac{1}{T_H}\left[\frac{I_{IN}^2}{16}\frac{u}{3}T_H + \frac{I_{IN}^2}{4}\left(\frac{2}{3}-\frac{u}{3}\right)T_H + \frac{I_{IN}^2}{16}\left(\frac{u+2}{3}-\frac{2}{3}\right)T_H\right]} \tag{3.17}$$

simplifying

$$I_{P,rms} = \sqrt{\frac{I_{IN}^2}{4}\left[\frac{1}{4}\frac{u}{3}+\frac{2}{3}-\frac{u}{3}+\frac{1}{4}\frac{u}{3}\right]} = \frac{I_{IN}}{2}\sqrt{\frac{2}{3}-\frac{u}{6}} \tag{3.18}$$

As well, we can derive the expression of the RMS and the mean current in the transistors from the waveform of the figure 3.2. In this case the period of integration is $2T_H$. Hence the RMS current is

$$I_{ds,rms} = \sqrt{\frac{1}{2T_H}\int_0^{2T_H} i_p(t)^2\,dt} \tag{3.19}$$

since the current between T_H and $2T_H$ is zero, we can reformulate the equation as

$$I_{ds,rms} = \frac{1}{\sqrt{2}}\sqrt{\frac{1}{T_H}\int_0^{T_H} i_p(t)^2\,dt} = \frac{I_{P,rms}}{\sqrt{2}} \tag{3.20}$$

substituting 3.18

$$I_{ds,rms} = \frac{I_{IN}}{2}\sqrt{\frac{1}{3}-\frac{u}{12}} \tag{3.21}$$

and the mean current is

$$\widehat{I_{ds}} = \frac{1}{2T_H}\int_0^{2T_H} i_p(t)^2\,dt =$$

$$\frac{1}{2T_H}\left[\int_0^{\frac{u}{3}T_H}\frac{I_{IN}}{4}\,dt + \int_{\frac{u}{3}T_H}^{\frac{2}{3}T_H}\frac{I_{IN}}{2}\,dt + \int_{\frac{2}{3}T_H}^{\frac{u+2}{3}T_H}\frac{I_{IN}}{4}\,dt\right] \tag{3.22}$$

solving the integrals, we have

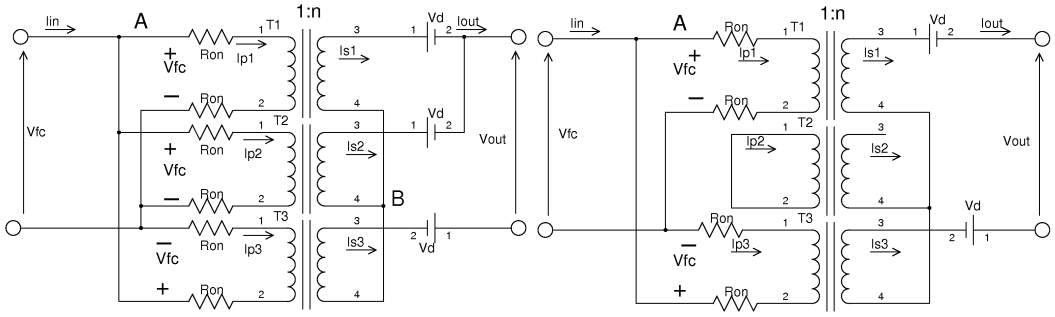
$$\frac{1}{2T_H}\left[\frac{I_{IN}}{4}\left(\frac{u}{3}T_H\right)+\frac{I_{IN}}{2}\left(\frac{2}{3}-\frac{u}{3}T_H\right)+\frac{I_{IN}}{4}\left(\frac{u+2}{3}-\frac{2}{3}T_H\right)\right] \tag{3.23}$$

simplifying

$$\widehat{I_{ds}}=\frac{I_{IN}}{6} \tag{3.24}$$

The figure 3.2 shows equal waveform of the currents in the diodes and in the transistors, but with a factor of transformer turns ratio, the equations of the RMS and mean current in the diodes keep also this relation.

In order to derive an expression to dimension the transformer turns ratio, we added the non idealities of the switches to the circuit, as you could see in the figure 3.5. Thus, ON resistances are added for the transistors ,R_{ON}, and DC sources for the diodes, V_D.



(a) Three phases conduct

(b) Two phases conduct

Figure 3.5: The two states of the converter with the conduction losses

The derivation of the equations in the case of having three phases conducting. The voltages in the primaries are,

$$V_{P,1}=V_{FC}-\frac{R_{ON}I_{IN}}{2}\quad V_{P,3}=-V_{FC}+R_{ON}I_{IN} \tag{3.25}$$

and applying KVL in the output net, we have

$$V_{OUT}+2V_D=V_{S,1}-V_{S,3} \tag{3.26}$$

applying the turns ration relation between the secondary and the primary and substituting in 3.25

$$V_{OUT}+2V_D=n\left(2V_{FC}-\frac{3}{2}R_{ON}I_{IN}\right) \tag{3.27}$$

so the transformer turns ratio expression is n

$$n = \frac{V_{OUT} + 2V_D}{2V_{FC} - \frac{3}{2}R_{ON}I_{IN}} \tag{3.28}$$

The derivation of the equations in the case of having two phases conducting. The voltages in the primaries are,

$$V_{P,1} = V_{FC} - R_{ON}I_{IN} \quad V_{P,3} = -V_{FC} + R_{ON}I_{IN} \tag{3.29}$$

applying the turns ration between the secondary and the primary and substituting 3.29 in 3.27

$$V_{OUT} + 2V_D = n\left(2V_{FC} - 2R_{ON}I_{IN}\right) \tag{3.30}$$

so the transformer turns ratio expression is n

$$n = \frac{V_{OUT} + 2V_D}{2V_{FC} - 2R_{ON}I_{IN}} \tag{3.31}$$

The worst of the two cases is when only two phases conducting, so 3.31 is the equation used to dimension the converter.All the equations used to dimension the components of the converter are in the table 3.1

Table 3.1

Transformer	V_{max}	I_{max}	I_{rms}	n
Primary Winding	V_{FC}	$\frac{I_{IN}}{2}$	$\frac{I_{IN}}{2}\sqrt{\frac{2}{3} - \frac{u}{6}}$	$\frac{V_{OUT}+2V_D}{2V_{FC}-2R_{ON}I_{IN}}$
Secondary Winding	nV_{FC}	$\frac{I_{IN}}{2n}$	$\frac{I_{IN}}{2n}\sqrt{\frac{2}{3} - \frac{u}{6}}$	-
Switches	$V_{GD,max}$	$I_{D,max}$	$I_{D,rms}$	$I_{D,mean}$
Transistor	V_{FC}	$\frac{I_{IN}}{2}$	$\frac{I_{IN}}{2}\sqrt{\frac{1}{3} - \frac{u}{12}}$	$\frac{I_{IN}}{6}$
Diode	$2nV_{FC}$	$\frac{I_{IN}}{2n}$	$\frac{I_{IN}}{2n}\sqrt{\frac{1}{3} - \frac{u}{12}}$	$\frac{I_{IN}}{n6}$

3.3 Component Sizing

The *V6* shall boost at least the fuel cell voltage to $320V_{DC}$. The design is dimension to handle the voltages and the currents for the test points defined in the chapter 2 section 2.1.2. The switching frequency of the converter is fixed to 100kHz, because the transformers are optimized to achieve the maximum efficiency at this frequency.

The technology chosen to implement the switches of the H-bridges is MOSFET, because MOSFET switches achieve better performance at this frequency range

than IGBTs. Since we need a large number of devices (12), the bridges are implemented using two Power Modules (PM) with part number **GMM 3x120-0075x2** by *IXYS*. This PM integrates 6 MOS transistors and their reverse diodes placed in a 3-legs full bridge layout and it is suitable for high power density applications. Find the relevant characteristics in table 3.2 and the datasheet in the appendix A.

Table 3.2: 3-phase MOSFET PM parameters

Model	**Company**	V_{DS}	I_D	R_{ON}	t_r	t_f
GMM 3x120-0075x2	IXYS	75V	110A	4 $m\Omega$	100 ns	100 ns

The required transformers turns ratio is computed with the equation 3.31 . It is solved for the defined operating point: minimum voltage, (40V, 350A), converter output, (320V), MOS R_{ON} , $4m\Omega$ and we estimated a diode direct voltage drop of 1.2V. With these values the turns ratio relation to step-up from 40V to 320V is $n = 4.18$, thus is not an number with round relation we designed the transformer with the relation $3 : 13$ that give a turns ratio relation of $n = 4.33$. With this n we guarantee a DC bus voltage grater than 320V.

Since the application is critical in volume and mass, we decided to employ the planar transformers manufactured by *Payton Group*, hence they have a high power density and efficiency. The specifications given for the transformers are in the table 3.5, fora an operating frequency of 100kHz.

Table 3.3: Transformer main parameters

Model	T1000DC	-
Firm	Payton Group	-
P_{WR}	6	kW
f_{opt}	100	kHz
R_{DC}	0.25 2.5	$m\Omega$
L_{leak}	61 551	μH
Weight	1	kg
Dim. (WxLxH)	135x89x32	mm

With the turns ratio defined we can dimension the diodes for the rectifier bridge. The bridge is implemented with a 3-phase rectifier bridge module from *IXYS* with part number **VUO-220NO1**. Find the relevant characteristic in the table 3.5 and the datasheet in the appendix A.

Table 3.4: MOS main parameters

Model	**Company**	V_R	I_D	V_f	R_f
VUO-220NO1	IXYS	800V	22 A	1.2V	40 $m\Omega$

Table 3.5: Components sizing values

Parameters			**Unit**	**Values**				**Max.**
Fuel Cell		Pwr	kW	16.5	8.25	2.14	14	-
		V_{OUT}	V	54	62	68	40	-
		I_{OUT}	A	305	133	32	350	-
Transistors		V_{DS}	V	54	62	68	40	68
		I_{max}	A	152	67	16	175	175
		I_{avg}	A	51	23	5	58	58
Transformer		P_{WR}	kW	6				6
		n	-	4.33				3:13
		V_{S-P}[1]	V	180	206	226	133	226
	Primary	V_P	V	54	62	68	40	68
		$I_{P,max}$	A	152	67	16	175	175
		$I_{P,rms}$	A	116	54	13	143	143
	Secondary	V_S	V	251	268	294	173	294
		$I_{S,max}$	A	35	15	3.6	40	40
		$I_{S,rms}$	A	27	13	3	33	33
Diode		V_R	V	455	530	585	331	585
		I_{max}	A	35	15	3.6	40	40
		I_{avg}	A	12	5.1	1.2	13.5	13.5

3.4 Simulation

The *V6* converter is implemented in Matlab Simulink with the SimPowerSystems library. This simulation is a first approach of the system behaviour, to validate the calculations of the previous section and to have a rough estimation of the converter losses. The switches and the transformers include the parasitic resistances, in order to estimate the conducting losses. The switching losses are not considered in the simulation, indeed the converter is designed to operate in soft switching, thus switching losses should not be relevant. The operation conditions for the *V6* converter are: switching frequency 100 kHz, phase shift modulation angle of 150°.

[1]Voltage between primary to secondary windings

The first simulation runs the converter operating at full load, drawing the maximum power of the fuel cell, $16.5kW$. Then the converter is subjected to a load step at minimum load, drawing the minimum power from the FC, about $2kW$. The figure 3.6 shows the voltage and the current of the fuel cell and in the

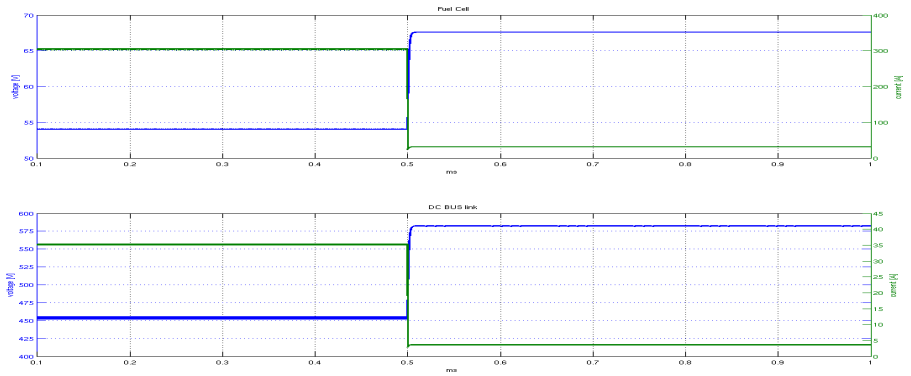


Figure 3.6: Simulation results: Load step transient voltage and current response, Top- Fuel Cell; Bottom- *V6* converter output

DC-link bus. At full load the DC-link voltage is 454V and the fuel cell voltage is 54V, so the conversion ratio of the converter is 8.4. At minimum load the DC-link voltage is 582V and the fuel cell voltage is 67.5V, so the conversion ratio of the converter is 8.62. The variation in the converter step-up ratio is cause of the parasitic resistances in the components.

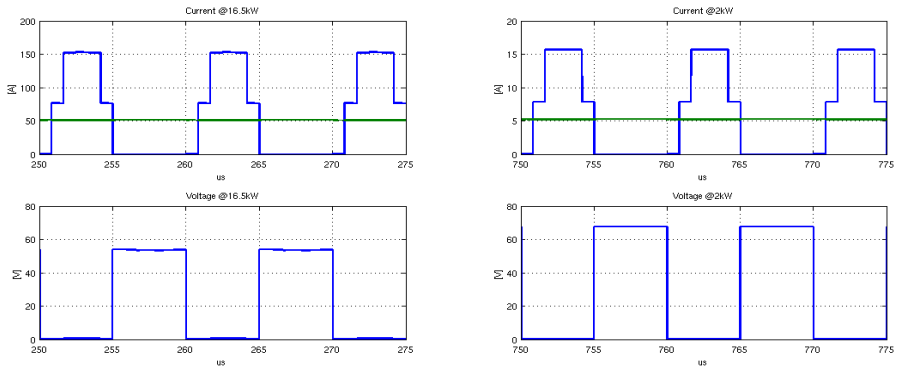


Figure 3.7: Simulation Results: MOSFETs voltage and current at maximum(left) and minimum (right) load, Top- Channel Current; Bottom- Drain-Source Voltage.
Blue-instantaneous value; *Green*- mean value

In the figures 3.7, 3.8 and 3.9 we can see the voltages and currents waveforms of one of the MOS-Transistors, one of the Diodes and the primary winding of one of the transformers, respectively. The simulation results match with the tensions and currents calculated for those devices in the previous section and presented in the table 3.5.

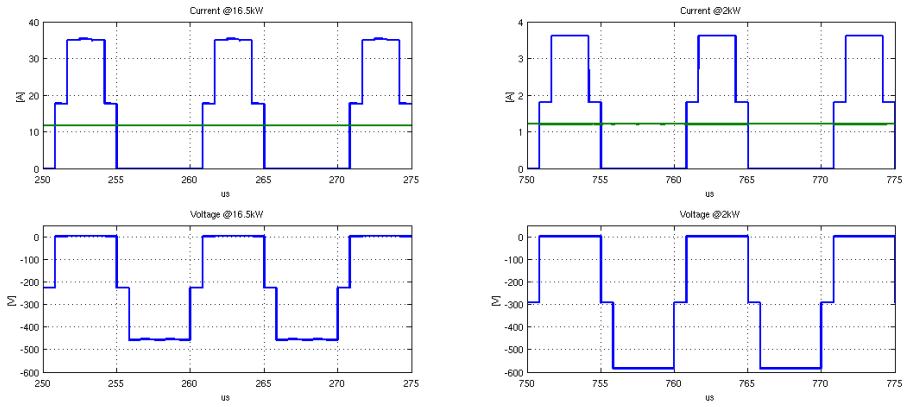


Figure 3.8: Simulation Results: Diodes current(top) and voltage(bottom) at maximum(left) and minimum (right) load.
Blue-instantaneous value; *Green*- mean value

The second simulation runs the converter under abnormal conditions when the fuel cell stack only provides 40V and 350A, emulating the FC end-of-life conditions. In this case the DC-link bus voltage is 330 V, so the step-up ratio is 8.25, it is large enough to guarantee a bus voltage of 320V. The figure 3.10 shows the voltages and currents of the MOSFET, Diode and Transformer primary, in the graphs we can appreciate that the components are dimensioned to handle the high currents that will this abnormal mode produce.

The last simulation is preformed to evaluate the efficiency of the converter. The simulation runs the model with the standard I-V FC characteristic with a load sweep from minimum to full power, the figure 3.11 shows the results. This is a rough first approach of the converter efficiency, that only takes into account the conduction losses. However wit the achieve results, 97% of efficiency at full power, we considered that is a good result for conducting losses.

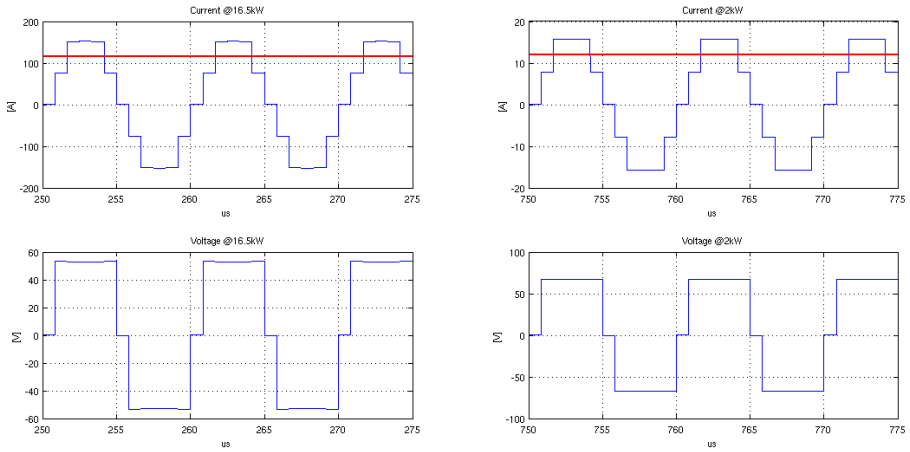


Figure 3.9: Simulation Results: Transformer primary winding current (top) and voltage(bottom at maximum(left) and minimum (right) load).
Blue- instantaneous value, *Red*- RMS value

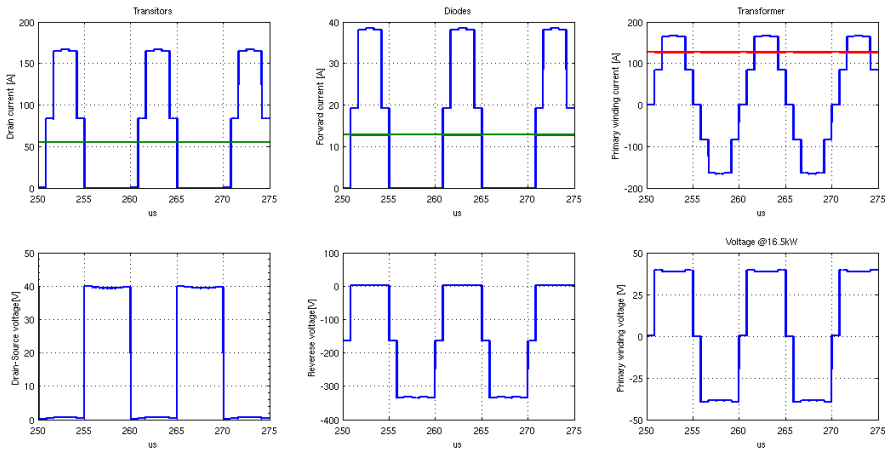


Figure 3.10: Simulation Results: Top- MOSFET channel current , Diode current and Transformer Primary Winding current; Bottom- MOSFET channel voltage, Diode voltage and Transformer Primary Winding voltage.
Blue- instantaneous value; *Green*- Mean value; *Red*- RMS value

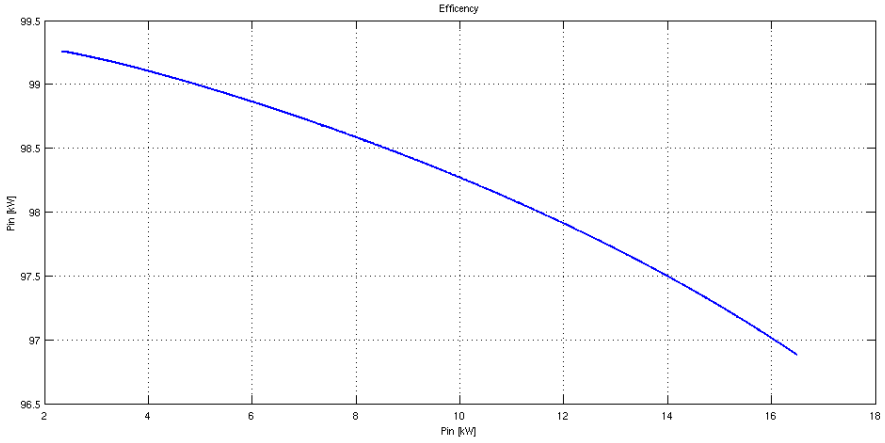


Figure 3.11: Simulation Results: *V6* converter efficiency versus input power

Chapter 4

Symmetric converter

The goal of this power stage is to supply a regulated output of - from the DC-link bus. Since the DC-link has no regulation and the voltage varies with the load, this stage should provide regulation for variations in the load and in the DC-link voltage in order to guarantee the ±270V in the outputs. Furthermore, since the *V6* converter behaves like a DC-DC transformer, this stage should fulfill FC electrical restrictions -continuous drawn current and low current ripple.

The stage is implemented using two converters with dual characteristics, a SEPIC converter and a Cúk converter. The SEPIC converter provides the +270V and the Cúk converter provides -270V. The selection of this topologies is cause of both converters have continuous input current, required by the FC. As well as they have continuous input current, the fact to use theses converters with dual characteristics, let us reduce the current ripple in the bus , up to 66%, through harmonic cancellation by operating them 180 ° out of phase.

This chapter is divided in five sections. In the first section describes the converters topology. In the second section the steady state models and equations are derived for each topology, the components are dimensioned and validated through open-loop simulations. In the third section the small signal model and the transfer functions are computed for each converter. In the fourth section is designed the close-loop control for the converters and the results are presented through simulations.

4.1 Topology Description

SEPIC and Cúk converter, respectively figures 4.1 and 4.2, are converter with dual characteristics, besides the voltage inversion of the Cúk converter. Both converters allow the voltage at its output to be grater than, less than or equal to that its input voltage, and the conversion ratio is controlled by the duty cycle of the switching transistor. Also, the converters have true shutdown mode: when the transistor is turned off, its output drops to 0V.

SEPIC and Cúk converter, respectively figures 4.1 and 4.2, have analogous characteristics, besides the voltage inversion of the Cúk converter. Both converters have a buck-boost transformation ration -that allow the voltage at its output to be grater than, less than or equal to that its input voltage- it is controlled by the duty cycle of the switching transistor Q_1. Both converters use a capacitor as storage element to transfer the energy from the input to the output, unlike most other types of converter which use an inductor. This capacitor (placed in series between input and output) provides isolation from input to output, and true shutdown mode: when the transistor is turned off, the output drops to 0V.

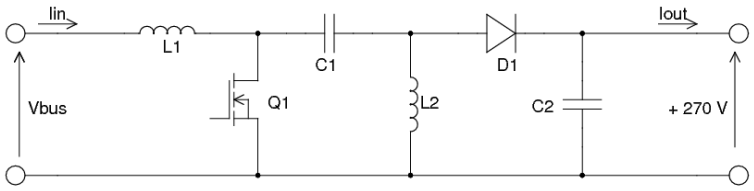


Figure 4.1: Schematic of SEPIC

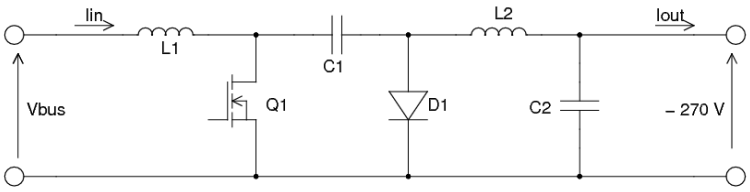


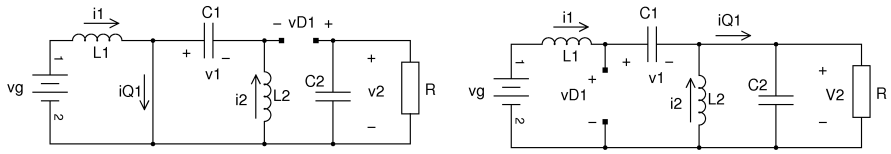
Figure 4.2: Schematic of Cúk

Besides the advantages of theses topologies, these converters have the disadvantage of having a large number of passive components, 2 coils and 2 capacitors. This increases the complexity in the implementation and in the circuit analysis.

4.2 Steady State Circuit Model

4.2.1 SEPIC converter

The figure 4.3 shows the two equivalent circuits during the two states of the SEPCI converter. When transistor Q_1 is turned on, on T_{ON}, the currents in the inductors increases, the voltage supply E transfers power to L_1 and the capacitor C_1 transfers energy to L_2; at same time C_2 feeds the load. When transistor Q_1 is turned off, on T_{OFF}, the current in the inductors decreases, the current of L_1 charges C_1 and i_2 adds to i_1 to supply current to the load and charge C_2.



(a) Circuit during T_{ON} (b) Circuit during T_{OFF}

Figure 4.3: Equivalent circuits during the two intervals of SEPIC converter

During the interval T_{ON}, circuit reduce to figure 4.3 *a*, the inductor voltages and capacitor currents are:

$$\begin{aligned} v_{L1} &= v_e \\ v_{L2} &= v_1 \\ i_{C1} &= -i_2 \\ i_{C2} &= -\tfrac{v_2}{R} \end{aligned} \tag{4.1}$$

We next assume the switching ripple magnitudes in $i_1(t)$, $i_2(t)$, $v_1(t)$ and $v_2(t)$ are small compared to their DC components I_1, I_2, V_1 and V_2. We can therefore make the small ripple approximation, and Eq.(4.1) becomes:

$$\begin{aligned} v_{L1} &= V_e \\ v_{L2} &= V_1 \\ i_{C1} &= -I_2 \\ i_{C2} &= -\frac{V_2}{R} \end{aligned} \tag{4.2}$$

During the interval T_{OFF}, circuit reduce to figure 4.3 *b*, the inductor voltages

and capacitor currents are:

$$\begin{aligned} v_{L1} &= v_e - v_1 - v_2 \\ v_{L2} &= -v_2 \\ i_{C1} &= i_1 \\ i_{C2} &= i_1 + i_2 - \frac{v_2}{R} \end{aligned} \tag{4.3}$$

We next make the small ripple approximation, and Eq.(4.3) becomes:

$$\begin{aligned} v_{L1} &= V_e - V_1 - V_2 \\ v_{L2} &= -V_2 \\ i_{C1} &= I_1 \\ i_{C2} &= I_1 + I_2 - \frac{V_2}{R} \end{aligned} \tag{4.4}$$

The next step is to equate the DC components, or averaged values, of the inductor currents and the capacitor voltages with Eq.(4.2, 4.4). We make the assumption that the mean values of the inductor voltages and capacitors currents are 0. The results are:

$$\begin{aligned} < v_{L1} > &= DV_e + D'(V_e - V_1 - V_2) \\ < v_{L2} > &= DV_1 + D'(-V_2) \\ < i_{C1} > &= D(-I_2) + D'I_1 \\ < i_{C2} > &= D\left(-\frac{V_2}{R}\right) + D'\left(I_1 + I_2 - \frac{V_2}{R}\right) \end{aligned} \tag{4.5}$$

where D and D' is the duty cycle of the switching signal that defines the times of the commutations intervals as $t_{ON} = DT$ and $t_{OFF} = D'T$.

Solution for this system of equations for the DC components of the capacitor voltages and the inductor currents leads to

$$\begin{aligned} V_1 &= V_e \\ V_2 &= V_e\frac{D}{D'} \\ I_1 &= I_2\frac{D}{D'} = \frac{V_e}{R}\left(\frac{D}{D'}\right)^2 \\ I_2 &= \frac{V_2}{R} = \frac{V_e}{R}\frac{D}{D'} \end{aligned} \tag{4.6}$$

Equations (4.2) ,(4.4) and (4.6) are used to sketch the inductor currents and capacitor voltages waveforms of in Fig. 4.4.

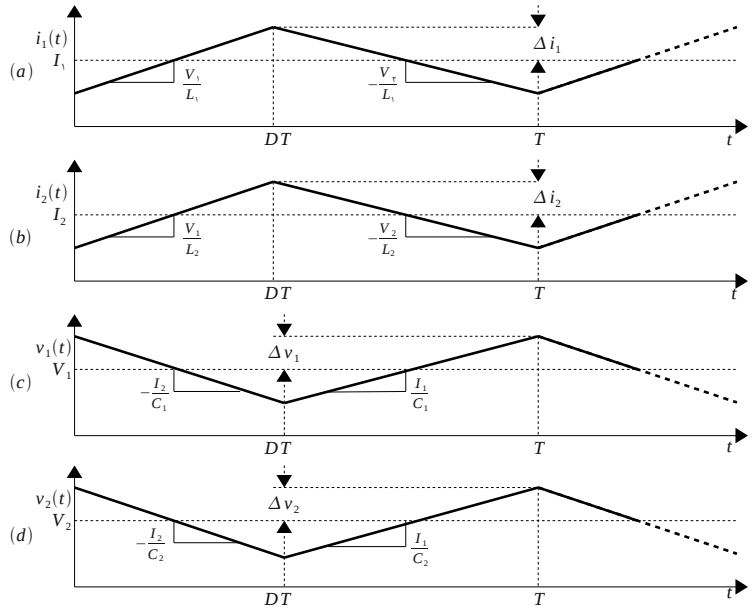


Figure 4.4: SEPIC converter waveforms: (a) inductor L_1 current; (b) inductor L_2 current; (c) capacitor C_1 voltage; (d) capacitor C_2 voltage

The next step is to equate the ripple amplitudes of the inductor currents and the capacitor voltages, we obtain them multiplying the slopes defined in Fig. 4.4 by the interval time DT and dividing by 2. Then, using DC relations of Eq. (4.6) we simplify to eliminate V_1, V_2, I_1 and I_2, and the results are:

$$\begin{aligned} \Delta v_1 &= \frac{V_e D^2 T}{2C_1 R D'} \\ \Delta v_2 &= \frac{V_e D^2 T}{2C_2 R D'} \\ \Delta i_1 &= \frac{V_e D T}{2L_1} \\ \Delta i_2 &= \frac{V_e D T}{2L_2} \end{aligned} \tag{4.7}$$

With the ripple amplitudes we can equate the maximum absolute values of the capacitor voltage and inductors currents adding the ripple amplitude to the DC component from Eq. (4.6) it yields to

$$\begin{aligned} v_{1,max} &= V_1 + \Delta v_1 \\ v_{2,max} &= V_2 + \Delta v_2 \\ i_{1,max} &= I_1 + \Delta i_1 \\ i_{1,max} &= I_2 + \Delta i_2 \end{aligned} \tag{4.8}$$

With these equations we now can compute the minimum vales for L_1, L_2 and C_1 which guarantee the continuous conduction mode (CCM) of the converter. The boundary between the CCM and the DCM (discontinuous conduction mode) is when the ripple amplitude of those components equals to their DC component, so we equal the DC magnitudes in Eq. (4.6) to the ripple amplitudes of Eq. (4.7), hence we have:

$$\begin{aligned} V_e &= \frac{V_e D^2 T}{2C_1 RD'} \\ V_e \frac{D}{D'} &= \frac{V_e D^2 T}{2C_2 RD'} \\ \frac{V_e}{R}\left(\frac{D}{D'}\right)^2 &= \frac{V_e DT}{2L_1} \end{aligned} \tag{4.9}$$

Solution for this system of equations leads to:

$$\begin{aligned} C_{1,min} &= \frac{D^2 T}{2RD'} \\ L_{1,min} &= \frac{D'^2 RT}{2D} \\ L_{2,min} &= \frac{D'RT}{2} \end{aligned} \tag{4.10}$$

The minimum value for capacitor C_2 is given by the output voltage ripple specification, so with the expressions of V_2 from Eq.(4.6) and Δv_2 from Eq.(4.7) and isolating for C_2 we obtain

$$C_{2,min} = \frac{V_2}{\Delta v_2}\frac{DT}{2RD'} = \frac{V_{out}}{\Delta v_{out}}\frac{DT}{2RD'} \tag{4.11}$$

The equations (4.10) and (4.11) will be used to dimension the passive components, next we need to find the equations to dimension the semiconductors. Therefore we need to know the maximum blocking voltage, maximum forward current and the averaged current for the transistor Q_1 and the diode D_1. We can write the voltage drop and the current as:

$$v_{Q1}(t) = \begin{cases} 0 & 0 < t < t_{on} \\ v_1(t) + v_2(t) & t_{on} < t < T \end{cases}$$

$$i_{Q1}(t) = \begin{cases} i_1(t) + i_2(t) & 0 < t < t_{on} \\ 0 & t_{on} < t < T \end{cases}$$

$$v_{D1}(t) = \begin{cases} v_1(t) + v_2(t) & 0 < t < t_{on} \\ 0 & t_{on} < t < T \end{cases}$$

$$i_{D1}(t) = \begin{cases} 0 & 0 < t < t_{on} \\ i_1(t) + i_2(t) & t_{on} < t < T \end{cases} \tag{4.12}$$

With these equations we sketch the currents and the voltages of the devices in Fig. 4.5

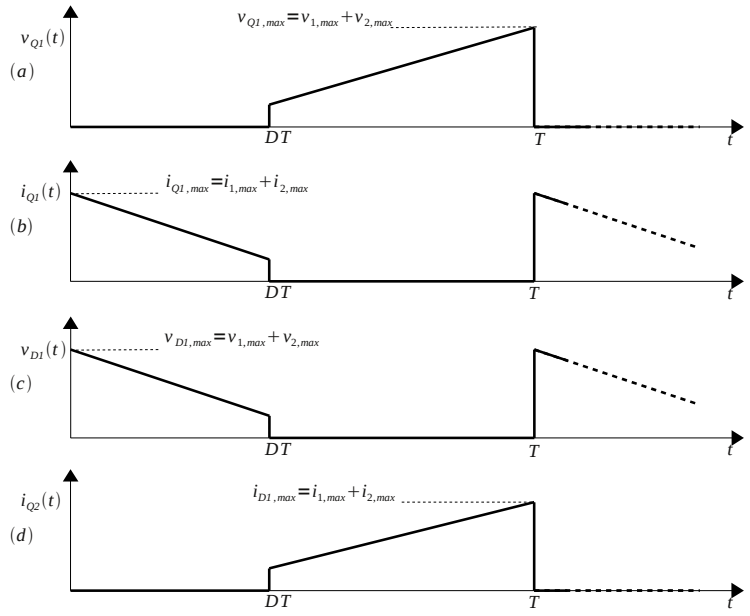


Figure 4.5: SEPIC converter waveforms: (a) transistor voltage; (b) transistor current; (c) diode voltage; (d) diode current

From the figure the maximum and minimum current and voltage can be written as

$$\begin{aligned} v_{Q1,max} = v_{D1,max} &= v_{1,max} + v_{2,max} \\ i_{Q1,max} = i_{D1,max} &= i_{1,max} + i_{2,max} \\ v_{Q1,min} = v_{D1,min} &= v_{1,min} + v_{2,min} \\ i_{Q1,min} = i_{D1,min} &= i_{1,min} + i_{2,min} \end{aligned} \tag{4.13}$$

next we can equate the mean value of the current in the transistor

$$I_{Q1} = \frac{1}{T}\int_0^T i_{Q1}(t)dt = \frac{DT}{T}\left[\frac{i_{Q1,max} - i_{Q1,min}}{2} + i_{Q1,min}\right] \tag{4.14}$$

using the expression in Eq.(4.14) the solution to the system leads

$$I_{Q1} = (I_1 + I_2)\, D \tag{4.15}$$

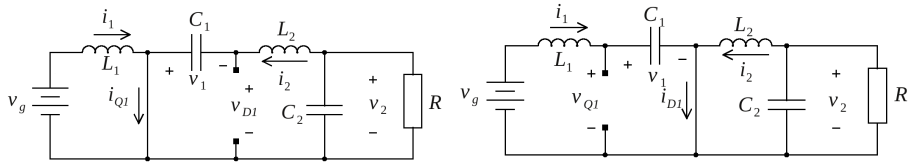
In the same way the mean current in the diode is

$$I_{D1} = \frac{1}{T}\int_0^T i_{D1}(t)dt = (I_1 + I_2)\, D' \tag{4.16}$$

The table 4.1 presents all the deign equations for the SEPIC converter.

4.2.2 Cúk converter

The figure 4.6 shows the two equivalent circuits during the two states of the Cúk converter. When transistor Q_1 is turned on, at T_{ON}, the currents in the inductors increases, the supply E transfers power to L_1 and the capacitor C_1 transfers energy to L_2; at same time C_2 feeds the load. When transistor Q_1 is turned off, at T_{OFF}, the current in the inductors decreases, the current of L_1 charges C_1 and i_2 supplies current to the load and charges C_2.



(a) Circuit during T_{ON} (b) Circuit during T_{OFF}

Figure 4.6: Equivalent circuits during the two intervals of Cúk converter

Applying the small ripple approximation, during the interval T_{ON}, the converter reduces to figure 4.6 *a*, the DC components in the inductor voltages and capacitor currents are:

$$\begin{aligned} v_{L1} &= V_e \\ v_{L2} &= (V_1 + V_2) \\ i_{C1} &= -I_2 \\ i_{C2} &= -I_2 - \frac{V_2}{R} \end{aligned} \tag{4.17}$$

And, during the interval T_{OFF}, the converter reduces to figure 4.6 *b*, the DC components in the inductor voltages and capacitor currents are:

$$\begin{aligned} v_{L1} &= V_e - V_1 \\ v_{L2} &= V_2 \\ i_{C1} &= I_1 \\ i_{C2} &= -I_2 - \frac{V_2}{R} \end{aligned} \tag{4.18}$$

The next step is to equate the DC components, or averaged values, of the inductor currents and the capacitor voltages with Eq.(4.17, 4.18). We make the assumption that the mean values of the inductor voltages and capacitors

currents are 0. The results are:

$$\begin{aligned} < v_{L1} > &= DV_e + D'(V_e - V_1) \\ < v_{L2} > &= D(V_1 + V_2) + D'(V_2) \\ < i_{C1} > &= D(-I_2) + D'I_1 \\ < i_{C2} > &= -I_2 - \frac{V_2}{R} \end{aligned} \tag{4.19}$$

where D and D' is the duty cycle of the switching signal that defines the times of the commutations intervals as $t_{ON} = DT$ and $t_{OFF} = D'T$.

Solution for this system of equations for the DC components of the capacitor voltages and the inductor currents leads to

$$\begin{aligned} V_1 &= \frac{V_e}{D'} \\ V_2 &= -V_e \frac{D}{D'} \\ I_1 &= I_2 \frac{D}{D'} = \frac{V_e}{R} \left(\frac{D}{D'} \right)^2 \\ I_2 &= \frac{V_2}{R} = \frac{V_e}{R} \frac{D}{D'} \end{aligned} \tag{4.20}$$

We can see that the resulting equations for the DC output voltage V_2 and the inductors current I_1 and I_2 are the same as the SEPIC converter, but the voltage sing in V_2.
Since the both converters are analogous their equations of the voltage ripple in V_1 and the current ripples in I_1 and I_2 are the same of the SEPIC converter; and the boundaries for the CCM are as well the same.
The most relevant difference in this converters is in the output capacitor.In the Cúk converter inductor L_2 and capacitor C_2 are always connected to the load. Hence the output capacitor only filter the AC component of the inductor current, but it does not supply the load. To compute the voltage ripple we will proceed as proposes Erickson, Rober .W in [**?**] with

$$\Delta v_2 = \frac{\Delta i_2 T}{8C_2} = \frac{V_e D T^2}{16 C_2 L_2} \tag{4.21}$$

The value of C_2 is determined by the specifications of the output voltage ripple, so we reformulate the expression to be the design equation of the out capacitor

$$C_2 = \frac{V_2}{\Delta v_2} \frac{D' T^2}{16 L_2} \tag{4.22}$$

Table 4.1: SEPIC and Cúk design equations

	SEPIC	**Cúk**
$\overline{V_1}$	V_e	$\frac{V_e}{D'}$
$\overline{V_2}$	$V_e \frac{D}{D'}$	$-V_e \frac{D}{D'}$
$\overline{I_1}$	$\frac{V_e}{R}\left(\frac{D}{D'}\right)^2$	
$\overline{I_2}$	$\frac{V_e}{R}\frac{D}{D'}$	
Δv_1	$V_e \frac{TD^2}{2C_1RD'}$	
Δv_2	$V_e \frac{TD^2}{2C_2RD'}$	$V_e \frac{TD^2}{16C_2L_2}$
Δi_1	$V_e \frac{TD}{2L_1}$	
Δi_2	$V_e \frac{TD}{2L_2}$	
$C_{1,min}$	$\frac{TD^2}{2D'^2R_{min}}$	
$C_{2,min}$	$\frac{V_{out}}{\Delta V_{out}} \frac{DT}{2D'R_{min}}$	$\frac{V_{out}}{\Delta V_{out}} \frac{DT^2}{16L_2}$
$I_{C_1,rms}$	$\sqrt{{I_1}^2 D' + {I_2}^2 D}$	
$I_{C_2,rms}$	$\sqrt{{I_1}^2 D' + {I_2}^2 D}$	$\frac{\Delta i_2}{\sqrt{3}}$
$L_{1,min}$	$\frac{TD'^2R_{max}}{2D}$	
$L_{2,min}$	$\frac{TD'R_{max}}{2}$	
$\overline{I_{trt}}$	$\overline{I_1}$	
$V_{trt,max}$	$\overline{V_1} + \overline{V_2} + \Delta v_1 + \Delta v_2$	$\overline{V_1} + \Delta v_1$
$\overline{I_{diode}}$	$\overline{I_2}$	
$V_{diode,max}$	$\overline{V_1} + \overline{V_2} + \Delta v_1 + \Delta v_2$	$\overline{V_1} + \Delta v_1$

4.2.3 Component Sizing

Since Boeing did not yet defined the specifications of the converter, the following assumptions have been done in order to to dimension the components of the converter:

- Absolute voltage at the outputs must be 270V
- Minimum load to operate in CCM is half of the FC power
- Maximum output ripple peak-to-peak is 5% of the rated output voltage
- Components should withstand the power and the currents for the 4 operating points defined in table 4.2

In the table 4.2 are the opertions points of the Fuel Cell defined in the chapter 2 The table has been extended with the values of the DC bus and load that the SEPIC and Cúk converter will supply. The value of the load is computed assuming that those converters has no losses.

Table 4.2: Power, current, voltages of the FC, DC link voltage for the four operating points

Fuel Cell				**DC link**			**Load**
P_{FC} [kW]	P_{FC} [%]	V_{FC} [V]	I_{FC} [A]	P_{bus} [kW]	V_{bus} [V]	I_{bus} [A]	R_o [Ω]
16.50	100	54	305	15.9	455	35.00	9.2
8.25	50	62	133	8.1	530	15.36	18.0
2.14	13	68	31.5	2.0	585	3.63	72.9
14.00	84	40	350	13.4	331	40.42	10.9

First we compute the values of the DC components of the currents in the inductors and in the transistors and of the voltages in the capacitors for the both converters. The table results are presented in the tables **??** and **??**. From the results, we can see that the semiconductors will conduct currents in the order of 30 amperes and the reverse voltage will be in the order of 700 volts, so the technology able to mange those voltages and currents for the controlled switches are the IGB devices. Due to the technology the switching frequency is fixed to operate at in 50kHz that is the limit for the IGB devices.

Table 4.3: DC components in the converters, subscript: S denotes SEPIC and C denotes Cúk

V_e [V]	D -	$V_{1,S}$ [V]	$V_{1,C}$ [V]	V_2 [V]	I_1 [A]	I_2 [A]	I_Q [A]	I_D [A]
455	0.373	455	725	270	17.6	29.7	17.6	29.7
530	0.338	530	780	270	7.7	15.1	7.7	15.1
585	0.316	585	855	270	1.8	3.9	1.8	3.9
332	0.449	332	602	270	20.2	24.8	20.2	24.8

Once the frequency is set we compute the values of the inductors and capacitors. The values of the inductors are the most critical, because their value will fix the limit between the CCM and DCM (discontinuous conduction mode). The inductors are dimensioned to fix the boundary between the two operation modes at half of the maximum FC power.

In the other hand, capacitor C_1 is not dimensioned using the assumption of CCM, because that will fix a huge ripple in the capacitor and the maximum

h

Table 4.4: Computed values of the passive components

	L_1 $[\mu H]$	L_2 $[\mu H]$	C_1 $[\mu F]$	C_2 $[\mu F]$
SEPIC	233	120	3	30
Cúk	233	120	3	3.7

voltage values in the semiconductors will be higher than a thousand of volts. Therefore, the assumption to dimension C_1 is to have 40V peak-to-peak of voltage ripple in the capacitor at full power. The assumption to dimension C_2 is to limit the output voltage ripple peak-to-peak to 5% of the output voltage, that is 13.5 volts peak-to-peak.

The values of the table 4.4 are all the same for both converters, but the output capacitor. Here we can see that the SEPIC converter needs a bigger capacitor C_2 to achieve the same output voltage ripple. That is due to the discontinuous output current of this topology. However, we decoded to use the same value of 3 μF for both capacitors, thus the dynamics of the converter is the equal for both converters, this will be further discusses in the next section.

With the values defined in the table 4.4, we compute all the AC components in the currents and voltages of the converters for the four points of operation defined in 4.2. The results are presented in table 4.5, there we can see that currents and the voltages are almost the same for all the components in both converters, but for capacitor C_1 which has a higher voltage stress in Cúk converter than in SEPIC converter.

The candidate for the active switches is the high speed IGBT **IRG4PF50WD** from IR, with the following characteristics:

- $V_{CES} = 900V$
- $V_{CE} = 2.25V$
- $I_{C,avg}(@100°C) = 28A$
- $I_{C,max} = 204A$
- $t_r = 50ns$, $t_f = 170ns$

The candidate for the passive switches is the high speed diodes *STTH9012TV* from ST semiconductors, with the following characteristics:

Table 4.5: Components sizing values

Parameters			**Unit**	**Values**				**Max.**
Fuel Cell		Pwr	kW	16.5	8.25	2.14	14	-
		V_{OUT}	V	54	62	68	40	-
		I_{OUT}	A	305	133	32	350	-
DC_{link}		V_{bus}	V	455	530	585	331	-
		I_{bus}	A	35.00	15.36	3.63	40.42	-
SEPIC	C_1	V_{max}	V	492	547	590	369	590
		I_{rms}	A	22.9	10.8	2.7	22.4	22.9
	C_2	V_{max}	V	273.7	271.7	270.4	273.7	273.7
		I_{rms}	A	4.1	4.3	4.5	3.6	4.5
	L_1	I_{max}	A	24.9	15.4	9.75	26.6	24.9
		V_{max}	V	492	547	590	369	590
	L_2	I_{max}	A	43.8	30	19.4	37.25	43.8
		V_{max}	V	492	547	590	369	590
	TRT	V_R	V	766	819	860	643	860
		I_{max}	A	58	34	17.4	54.4	58
		I_{avg}	A	17.6	7.7	1.8	20.2	20.2
	Diode	V_R	V	766	819	860	643	860
		I_{max}	A	58	34	17.4	54.4	58
		I_{avg}	A	29.7	15.1	3.9	24.8	29.7
Cúk	C_1	V_{max}	V	762	817	860	639	860
		I_{rms}	A	22.9	10.8	2.7	22.4	22.9
	C_2	V_{max}	V	271.2	271.2	271.3	271	271.2
		I_{rms}	A	4.1	4.3	4.5	3.45	4.5
	L_1	I_{max}	A	25	15.4	9.8	26.6	26.6
		V_{max}	V	492	547	590	369	590
	L_2 I_{max}		A	43.8	30	19.4	37.25	43.8
		V_{max}	V	492	547	590	369	590
	TRT	V_R	V	762	817	860	640	860
		I_{max}	A	58.0	34.0	17.4	54.4	54.4
		I_{avg}	A	17.6	7.7	1.8	20.2	20.2
	Diode	V_R	V	762	817	860	640	860
		I_{max}	A	58.0	34.0	17.4	54.4	54.4
		I_{avg}	A	29.7	15.1	4.0	24.9	29.7

- Tow diodes per packages
- $V_{RRM} = 1200V$
- $V_F = 1.2V$
- $I_{F,avg}(@75°C) = 45A$
- $I_{FRM} = 600A$
- $t_rr = 50ns$

Capacitor C_1 implementation will be 2 capacitors of $1.5\mu F$ connected in parallel; the candidate is a Round Polypropylene Film capacitors from Cornell Dubilier with part number *940C10W1P5K-F* and the following characteristics:

- $C = 1.5\mu F$
- $ESR(@100kHz) = 4m\Omega$
- $V_{max} = 1000V$
- $I_{rms}(@70°, 100kHz) = 17.9A$
- $Size(L \text{ x } D) = 46x35.5mm$

Capacitor C_2 implementation will be 2 capacitors of $15\mu F$ connected in parallel; the candidate is a Round Polypropylene Film capacitors from Cornell Dubilier with part number *932C4W15J–F* and the following characteristics:

- $C = 15\mu F$
- $ESR(@100kHz) = 3.1m\Omega$
- $V_{max} = 400V$
- $I_{rms}(@70°, 100kHz) = 11A$
- $Size(L \text{ x}D) = 55x30mm$

The sizing of the inductors is not a trivial task and goes further the scope of this thesis, so no candidates are proposed. The goal of having some candidates is to perform a more accurate simulations since the non-idealities can be extracted form the proposed components, for the inductors we will do the assumption of 95% efficiency. Once the design will be freezed, the inductors specifications should be sent to the magnetics suppliers that build an optimum solution for the magnetics.

4.3 AC Circuit Modeling

4.3.1 SEPIC small signal model and transfer functions

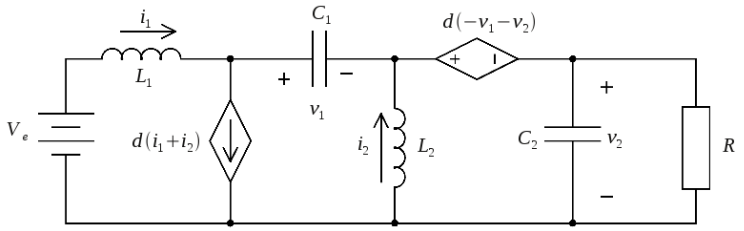


Figure 4.7: SEPIC small signal model

Figure 4.7 shows the small signal model for the SEPCI converter, from the model we write the equations for the four state variables:

$$\begin{array}{cc} L_1\frac{di_1}{dt} = v_e - (v_1+v_2)d' & C_1\frac{dv_1}{dt} = i_1 d' - i_2 d \\ L_2\frac{di_2}{dt} = v_1 d - v_2 d' & C_2\frac{dv_2}{dt} = (i_1+i_2)d' - \frac{v_2}{R} \end{array} \tag{4.23}$$

Applying the averaged model for the variables, where the variables are decomposed in the DC (X) component and the AC ($\hat{x}$) component and then eliminating the 2^{nd} Order terms, we can now write the equations in the S-Domain as:

$$\begin{aligned} s L_1 \hat{i_1} &= \hat{v_e} - \hat{v_1}D' - \hat{v_2}D' + \hat{d}V_e(1+\frac{D}{D'}) \\ s L_2 \hat{i_2} &= \hat{v_1}D - \hat{v_2}D' + \hat{d}V_e(1+\frac{D}{D'}) \\ s C_1 \hat{v_1} &= \hat{i_1}D' - \hat{i_2}D - \hat{d}\frac{V_e}{R}\frac{D}{D'^2} \\ s C_2 \hat{v_2} &= \hat{i_1}D' + \hat{i_2}D' - \frac{\hat{v_2}}{R} - \hat{d}\frac{V_e}{R}\frac{D}{D'^2} \end{aligned} \tag{4.24}$$

Due to the complexity of the system with the four equations, we solved the transfer function using the symbolic library of Matlab, the program is the appendix B. The transfer function of the plant leads to,

$$H(s) = \frac{\hat{v_2}}{\hat{d}} = H_o \frac{s^3 A_3 + s^2 A_2 + s A_1 + A_0}{s^4 B_4 + s^3 B_3 + s^2 B_2 + s B_1 + B_0} \tag{4.25}$$

where the coefficients are

$$\begin{array}{rclrcl} H_o &=& \frac{E}{D'^2} & B_4 &=& C_1C_2L_1L_2R \\ A_3 &=& -C_1L_1L_2D & B_3 &=& C_1L_1L_2 \\ A_2 &=& C_1(L_1+L_2)RD' & B_2 &=& R\left[C_1D'^2(L_1+L_2)+C_2(L_1D^2+L_2D'^2)\right] \\ A_1 &=& -L_1D^2 & B_1 &=& L_1D^2+L_2D'^2 \\ A_0 &=& D'^2R & B_0 &=& D'^2R \end{array} \tag{4.26}$$

Since the SEPIC converter has four storage elements, the control-to-output transfer function is a 4^{th} order system. Figure 4.8 shows the bode plot of the transfer function when the converter is at full load (8.25kW) and at half load(4.12kW); within this boundaries is where the converter operates in CCM, hence the transfer function is true.

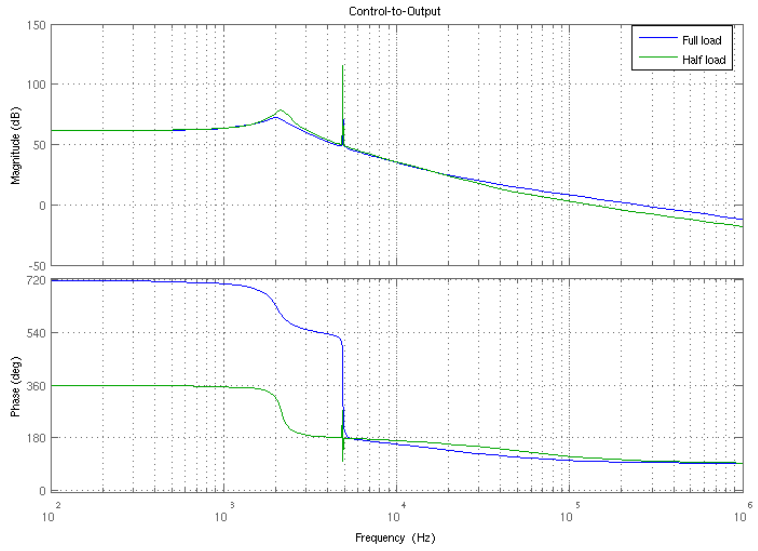


Figure 4.8: Bode diagram of the transfer function for SEPIC converter

With the s-plane plot 4.9 and the bode plot 4.8, we can identify the zeros and the poles of the transfer function. The first complex pole is around 2 kHz, at this point the phase drops 180° ant the magnitude takes an slope of 40 dB/dec. The next resonance peak in the bode plot is close to 5kHz, at this point there are a superimposed complex zero and complex pole, so they cancel each other, we can see in the bode plot the phase has a discontinuity of 360°, after this point the magnitude still decreases with the same slope of 40 dB/dec. More deep in frequency around 47kHz their is a real zero which is in the right half-plane of the

S-plane, so it drops 90° the phase and after this point the magnitude decrease with a slope of 20 dB/dec.

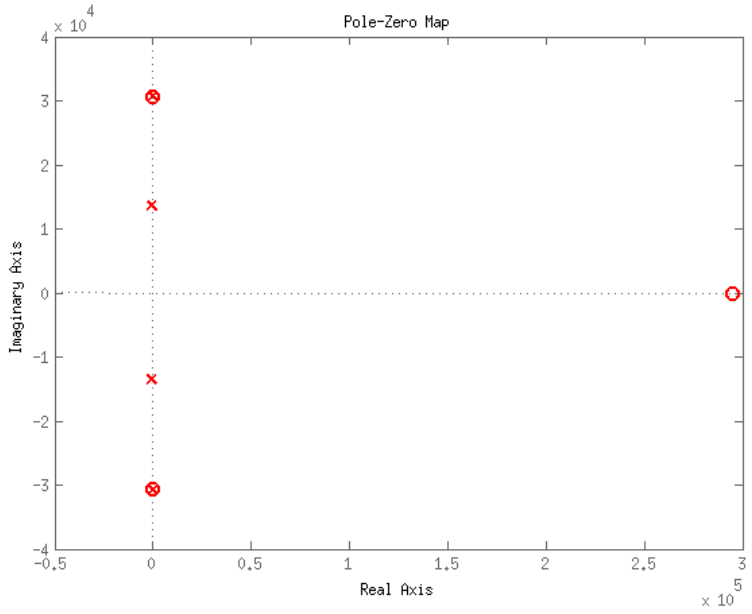


Figure 4.9: Location of the zeros and poles in the s-plane for the output-to-control transfer function of the SEPIC converter

In the bode plot we can see that in both cases the open-loop phase margin is around -90 degrees so the system needs to be regulated with a close-loop compensator. In addition, when the load increases the Q of the systems increases too, so the peaks at the resonance frequency are higher, since the system has less losses. Having this in mind, we will design the close loop compensator using the output-to-control transfer function with the values of half-load operation.

4.3.2 Cúk small signal model and transfer functions

Figure 4.10 shows the small signal model for the Cúk converter, from the model we write the equations for the four state variables:

$$\begin{aligned} L_1 \frac{di_1}{dt} &= v_e - v_1 d' \qquad & C_1 \frac{dv_1}{dt} &= i_1 d' - i_2 d \\ L_2 \frac{di_2}{dt} &= v_1 d + v_2 \qquad & C_2 \frac{dv_2}{dt} &= -i_2 - \frac{v_2}{R} \end{aligned} \tag{4.27}$$

Applying the averaged model for the variables, where the variables are decomposed in the DC (X) component and the AC ($\hat{x}$) component and then eliminating the 2^{nd} Order terms, we can now write the equations in the S-Domain

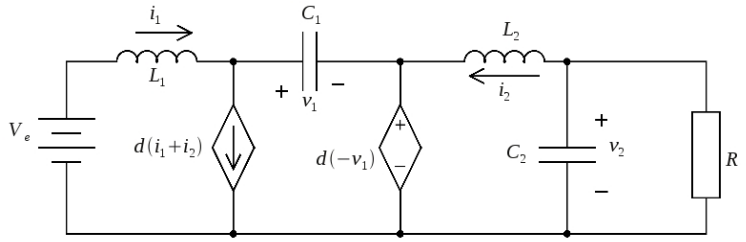


Figure 4.10: Cúk small signal model

as:

$$\begin{aligned} sL_1\hat{i_1} &= \hat{v_e} - \hat{v_1}D' + \hat{d}\frac{V_e}{D'} \\ sL_2\hat{i_2} &= \hat{v_1}D + \hat{v_2} + \hat{d}\frac{V_e}{D'} \\ sC_1\hat{v_1} &= \hat{i_1}D' - \hat{i_2}D - \hat{d}\frac{V_e}{R}\frac{D}{D'^2} \\ sC_2\hat{v_2} &= -\hat{i_2} - \frac{\hat{v_2}}{R} \end{aligned} \tag{4.28}$$

Due to the complexity of the system with the four equations, we solved the transfer function using the symbolic library of Matlab, the program is the appendix B. The transfer function of the plant leads to,

$$H(s) = \frac{\hat{v}_o}{\hat{d}} = H_o\frac{s^2A_2 + sA_1 + A_0}{s^4B_4 + s^3B_3 + s^2B_2 + sB_1 + B_0} \tag{4.29}$$

where the coefficients are

$$\begin{array}{rclrcl} H_o &=& -\frac{E}{D'^2} & B_4 &=& C_1C_2L_1L_2R \\ A_2 &=& C_1L_1L_2D' & B_3 &=& C_1L_1L_2 \\ A_1 &=& -L_1D^2 & B_2 &=& R(L_1C_1 + C_2(L_1D^2 + L_2D'^2)) \\ A_0 &=& RD'^2 & B_1 &=& L_1D^2 + L_2D'^2 \\ & & & B_0 &=& D'^2R \end{array} \tag{4.30}$$

The study did for the SEPIC converter is done for the Cúk converter. Cúk converter has also four storage elements, so its control-to-output transfer function is a 4^{th} order system, however the transfer function has one zero less than the SEPIC converter. The figure 4.11 shows the bode plot of the transfer function when the Cúk converter is at full load(8.25kW) and at half-load(4.12kW).

With the s-plane plot 4.12 and the bode plot 4.11, we can identify the zeros and the poles of the transfer function. The first complex pole is close to 2

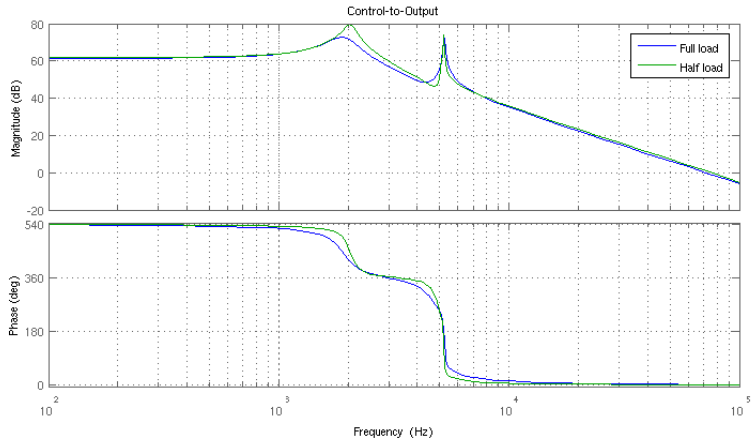


Figure 4.11: Bode diagram of the transfer function for Cúk converter

kHz, at this point the phase drops 180° and after this point the magnitude start decreasing with a slope of 40 dB/dec. The next resonance peak in the bode plot is close to 5kHz, at this point there are a complex zero and complex pole very close to each other, their natural frequency is at 5.17kHz for the complex pole and at 4.9 kHz for the complex zero. Since their are so close, they cancel each other in the magnitude plot, where it appears a resonance peak in between them, an for this point the magnitude keeps still decreasing whit 40 dB/dec. In the phase plot a drop of 360° appears, due to the fact that the complex zero is in the right half-plane of the S-plan so it adds - 180° to the phase plus the -180° of the complex pole the total drop is 360°.

As it happened in the SEPIC converter, the phase margin of the open-loop output-to-control does not guarantee the stability of the system, so a close-loop compensator will be added to regulate the output voltage. Also, the variation of the load modifies the transfer function of the converter, improving the Q of the system when the load decreases (the output resistance increases), hence the peaks at the natural frequencies are higher. As we did for the SEPIC converter, the close-loop controller is designed with the values when converter is at half-load.

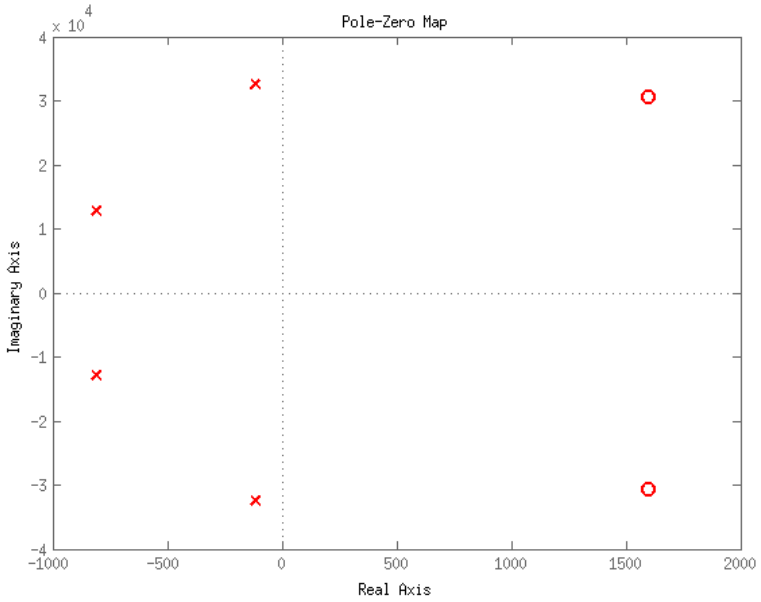


Figure 4.12: Location of the zeros and poles in the s-plane for the output-to-control transfer function of the Cúk converter

4.4 Close-Loop Controller Design

During the previous sections SEPIC and Cúk convert have been studied separately, but in the practice form the point of view of the load they will be a single converter with a symmetric voltage of +- 270 V DC. The way to achieve this single converter behaviour is through the close-loop controller, where the design of the compensator has the goal of give identical dynamic response to the converters.

The figure 4.13 is the block diagram of the Symmetric converter including the feed back loop. The diagram shows in the middle the Symmetric converter composed by the SEPIC and the Cúk converter, where they respectively supply +270V and -270V. The output voltage of each plant is sensed and attenuated by the sensor gain $H(s)$ then its compared to the reference voltage V_{ref}. The error signal is amplified by the compensator network $G_c(s)$ and after modulated with the Pulse Width Modulator, PWM, (PWM of each converter are 180^o out-of-phase to introduce the interleaving concept to the Symmetric, which reduces the current ripple in the DC-link bus). Then the PWM signal is amplified with the

IGBT driver to have enough current to charge fast the IGBT gate capacitors, and assure the IGBT commutation.

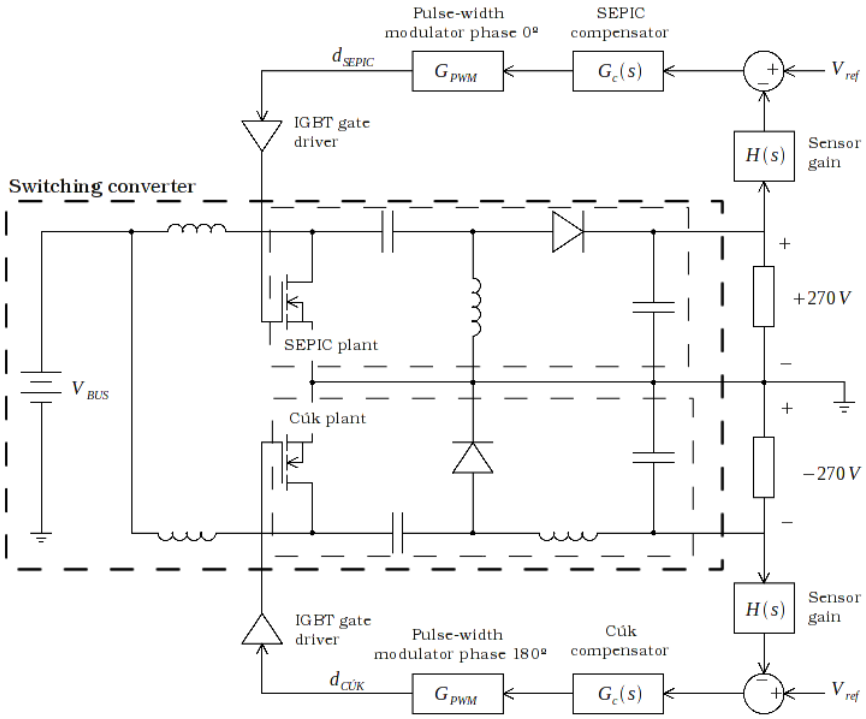


Figure 4.13: Block diagram of the feedback for the Symmetric converter

4.4.1 Compensation Network Design

In the previous sections, we identified the poles and zeros of the output-to-control transfer function for both converters. In fact both converters have almost identically transfer function, as as figure 4.14 shows. A complex-pole is located around 2kHz, and a complex zero and a complex pole are around 5kHz in both converters; in addition SEPIC converter has one more real zero at 47kHz. Therefore the same compensator network will be valid for both converters.

First we compute the feedback gain $H(s)$, the value chosen for the voltage reference, V_{ref}, is 3V, so the sensor gain for the SEPIC converter is,

$$H(s) = \frac{V_{ref}}{V_o} = \frac{3}{270} = \frac{1}{90} \tag{4.31}$$

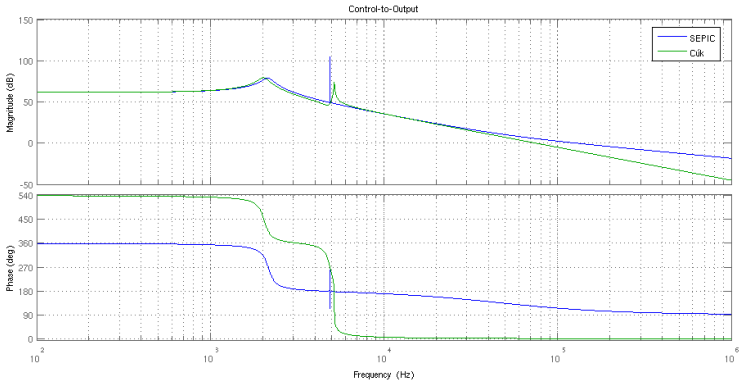


Figure 4.14: Bode diagram of the transfer function for SEPIC and Cúk

and for the Cúk converter

$$H(s) = \frac{V_{ref}}{V_o} = \frac{3}{-270} = -\frac{1}{90} \tag{4.32}$$

The amplitude of the sawtooth generator is fixed to 1, this leads the loop-gain transfer function

$$T(s) = H(s)G_c(s)G_{plant}(s) \tag{4.33}$$

The transfer function chosen for the compensation networks is:

$$G_c(s) = K * \frac{1}{s^2} \frac{\frac{s}{\omega_1} + 1}{(\frac{s}{\omega_o})^2 + 2\xi\frac{s}{\omega_o} + 1} \tag{4.34}$$

Where,

- The double pole at the origin improves the gain at the origin, cancelling the steady state error.
- The zero at $\omega_1 = 6Hz$ increases the band-with of the magnitude and advances the phase close the cut-off frequency to achieve a positive phase margin PM.
- The complex pole at $\omega_o = 400Hz$ and $\xi = 1$ attenuates the resonance frequency of the converter, which can cause instability and also it improves the filtering of the switching frequency of the converter. It also help to decrease the phase to achieve the goal PM.
- The gain is adjusted to $K = 1000$, to give the desired dynamics to the system.

The proposed compensation network, aims to attenuate the two resonance peaks of the open loop converter and meanwhile attenuate the switching noises of the converter. This forces to have the cut-off frequency f_c of the Loop-Gain $T(s)$ far enough to achieve enough attenuation to avoid the second resonance peak cross the 0 dB magnitude. As a result f_c is small, which implies a slow dynamics response of the Symmetric converter. Figure 4.15 shows the Loop-Gain of both

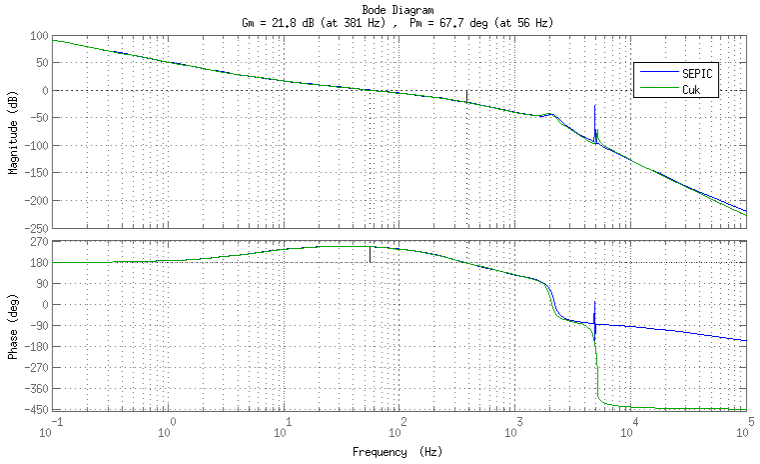


Figure 4.15: Bode diagram of the Gain-Loop for both converters

converters, you can see that is practically identical in both converters. The Gain Band With GMB of the converter is 56Hz and the Phase Margin is 67.7°. The achieved step response is represented in the figure 4.16, from the plot we see that the converter reaches its steady state after $120ms$, and the output voltage has overshoot that do not overpass the 300V, so the components of the converter will not be stressed for high voltages.

4.5 Simulation

4.5.1 Symmetric Converter Stand-Alone

The first simulation runs the model of the Symmetric Converter in the three operation points defined in the table 2.2 of the section *Components Sizing* 4.2.3. Therefore the simulation is divided in three steps: first at full load, drawing 8.25 kW each converter; second at half load, 4.12kW, and third at minimum load, 1kW. The model used for this simulation has the converter in close-loop and without including the losses of any component.

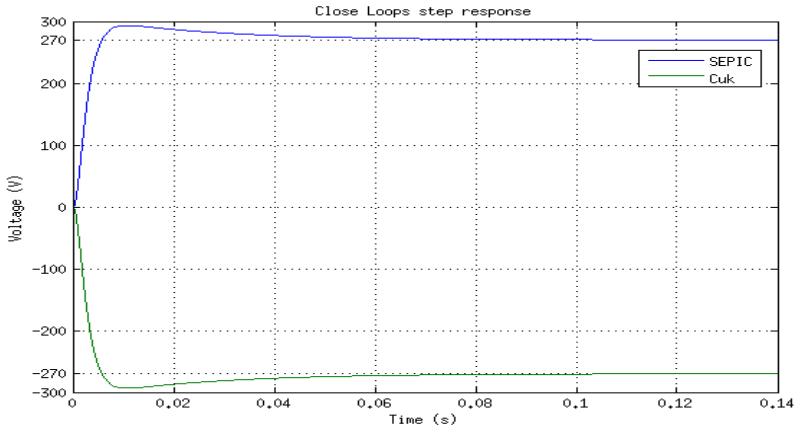


Figure 4.16: Close-Loop step response of the Symmetric Converter

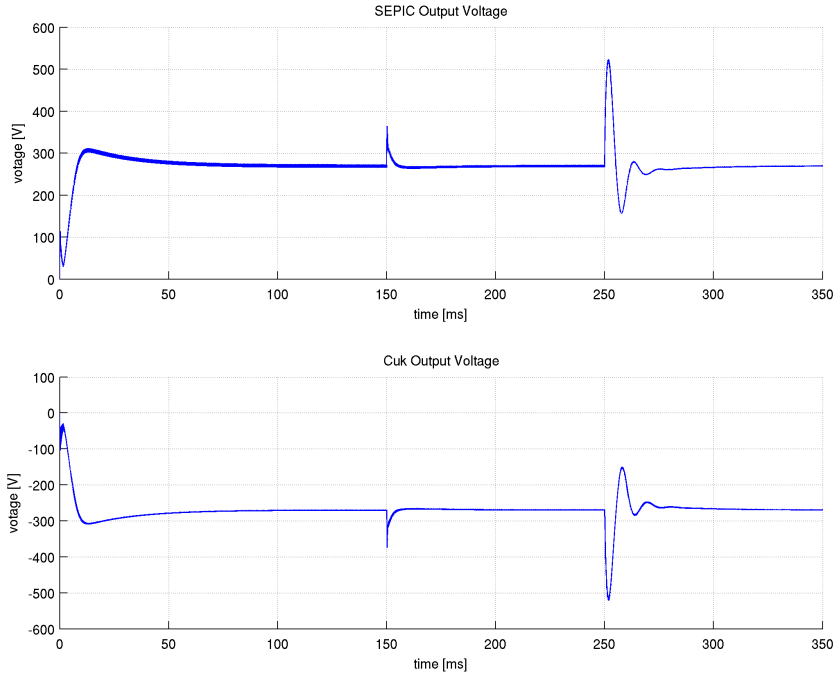
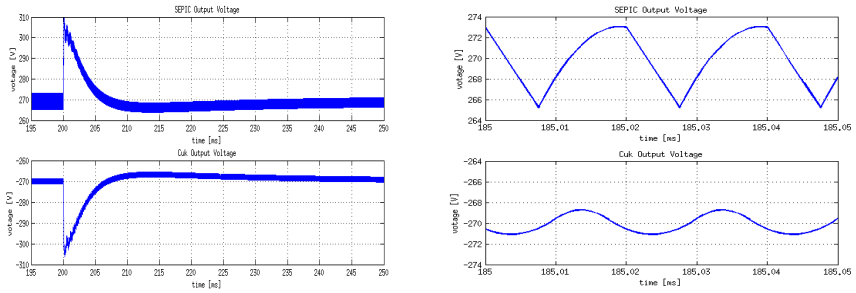


Figure 4.17: Simulation results: Output voltage of the Symmetric converter

The plot 4.17 shows the voltage at the two outputs regulated to the ±270V DC. We can see the close loop achieves regulation in both outputs in any of the three points of operation, also when the converter operates in DCM. The time to reach the steady state regime last about $50ms$ in the three cases, with

a dramatic voltage overshoot in the transition between CCM to DCM, beside this aspect the dynamic response of the system is correct, and identically for both outputs.



(a) Transient response of step load

(b) Output voltage ripple

Figure 4.18: Simulation: Transient of load step; Detail of output voltage ripple

The voltage ripple at the outputs, figure 4.19, is $7.8V$ peak-to-peak in the positive, 2.8% of the output voltage, and is $2.4V$ peak-to-peak n the negative, 0.89% of the output voltage; the values are much small than the given specifications. The difference in the ripple amplitude between the outputs is because the Cúk converter has continuous output current, as we can see in the current plot; the maximum *RMS* current in the capacitor is about $24.5A$ in the SEPIC, and $10A$ in the Cúk.

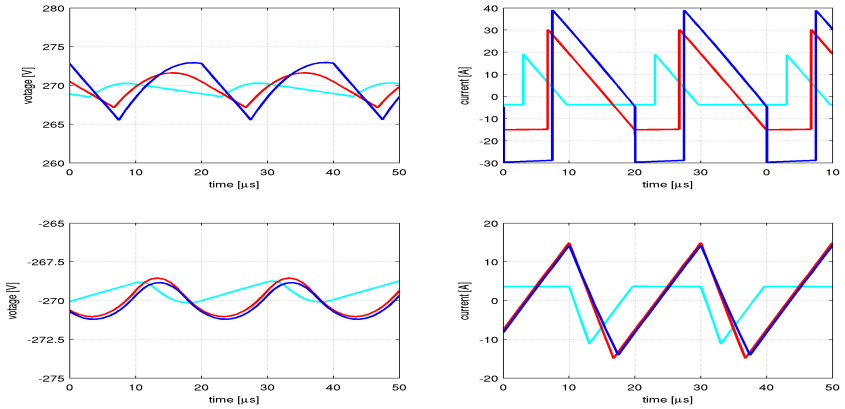


Figure 4.19: Simulation results: Output Capacitor voltage and current. Top- SEPIC; Bottom- Cúk. Legend: Blue- Full Load; Red- Half Load; Cyan- Minimum Load

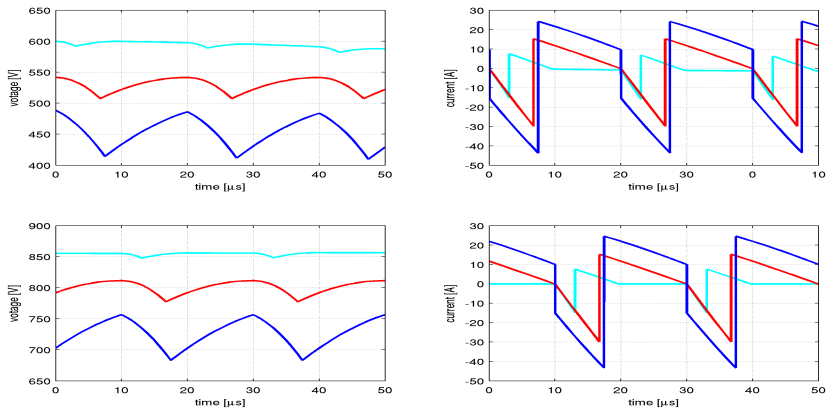


Figure 4.20: Simulation results: Transfer Energy Capacitor voltage and current. Top- SEPIC; Bottom- Cúk. Legend: Blue- Full Load; Red- Half Load; Cyan- Minimum Load

The voltage and the current of the energy transfer capacitor is plotted in figure 4.20. In the voltage graph we can see the mean voltage increases when the load decreases due to the I-V characteristics of the FC, achieving the maximum when the converter is supplying the minimum load. In opposite the ripple amplitude decreases when the load increases. The maximum voltage at the capacitors is $600V$ in the SEPIC and $860V$ in the Cúk, the maximum ripple voltage is about $50V$. The current through the capacitors average is 0A, verifying the capacitor amp-seconds balance principe, the maximum *RMS* current is measured when the converter is supplying full load, with a value about $23.5A$ in both converters. The ripple of the current decreases when the load decreases, since there is less energy to transfer to the output.

The figure 4.21 plots the current values on the inductors, we measure a maximum ripple $15A$ in the input inductor and $30A$ in the output inductor. Observing the red line we see that the inductors value is correct to guarantee the critical conduction mode at half load, further this point the converter enters to the DCM where the inductors currents is zero during a certain time for each switching period, cyan line.

The figure 4.22 and 4.23 show the reverse voltage and the direct current in the IGBTs and in the diodes; we see that, the voltages and the currents are the same in both converters. The maximum reverse voltage is about $860V$, and

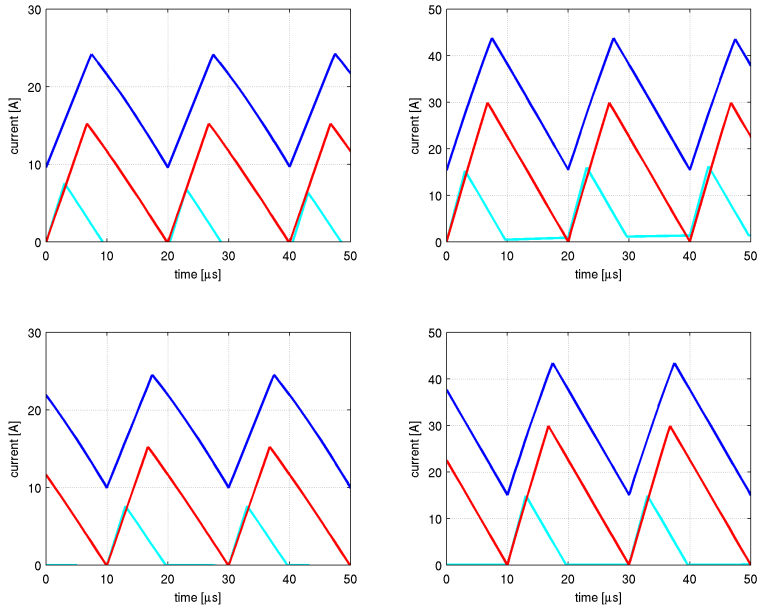


Figure 4.21: Simulation results: Current in the input inductor (left) and output inductor(right) , Top- SEPIC; Bottom- Cúk. Legend: Blue- Full Load; Red- Half Load; Cyan- Minimum Load

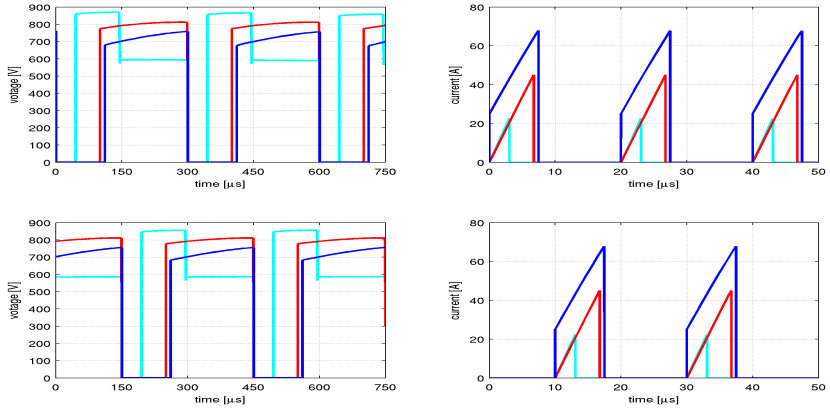


Figure 4.22: Simulation results: IGBT reverse voltage and direct current, Top- SEPIC ; Bottom- Cúk. Legend: Blue- Full Load; Red- Half Load; Cyan- Minimum Load

the maximum peak current is around $70A$. When the converter is operating in

the DCM, cyan line, the voltage stress on the switches achieves the maximum absolute value, but it last during less time, once the inductors have extinguished their current the reverse voltages drops to the DC-link value in the IGBTs and to the output value in the Diodes.

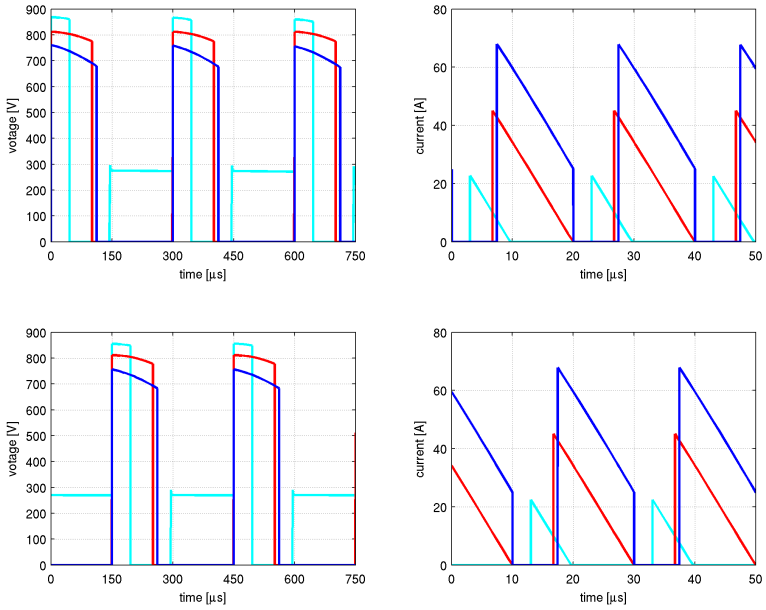


Figure 4.23: Simulation results: Diode reverse voltage and direct current, Top- SEPIC ; Bottom- Cúk. Legend: Blue- Full Load; Red- Half Load; Cyan- Minimum Load

The input current of the Symmetric converter drawn from the DC-link bus is plotted in the figure 4.24. The graphs with the input current of SEPIC and Cúk converter, show the interleaved operation of the Symmetric converter. Hence the interleaving operation of the converter the current ripple in the DC bus is dramatically reduced, achieving a ripple amplitude at full load about $5A$ compared to the $15A$ measured in the input of each converter. In addition the frequency of the ripple is twice the switching frequency of the converter, hence it will be advantageous in case of introduce a input filter.

4.5.2 Cascaded V6 and Symmetric converters

This simulation runs a Simulink model with the two converters cascaded connecting the load to the FC through the DC-Link, thus representing the

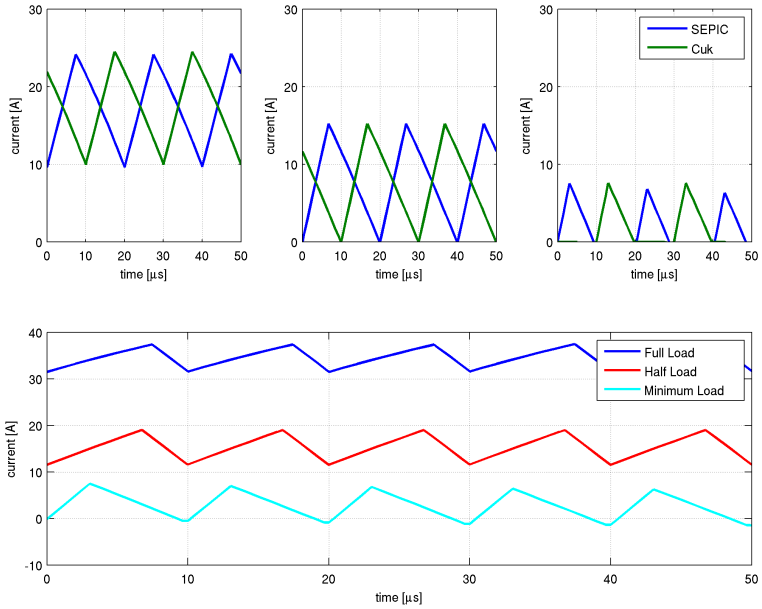


Figure 4.24: Simulation results: Top (left to right)- Input current of SEPIC an Cúk converter at full, half and minimum load; Bottom- Current drawn from the DC-link Bus.

complete system. The models used for this simulation includes the conducting losses produced by the non-idealities of the converters components, such as the R_{DS} of the MOSFETs, the voltage drops of the Diodes and IGBTs and the parasitic resistances of the transformers, capacitors and inductors. The values used in the components are extracted from the datasheet of the component candidates described in the previous sections.

The simulation varies the load from full power about 16.5kW to minimum power about 1.5kW. The graph of the figure 4.25 plots the efficiency of the converters as function of the load, the achieved results are not representative to the real system, however it led us to have a rough approach of the system efficiency and the trends of the efficiency whit the load variations. In this simulation the cascaded converters achieve the best performance with higher loads with a efficiency of 92% at full load, and the worst performance with at the minimum load with an efficiency of 83%.

The figure 4.26 plots the voltage variation in the FC, DC-Link bus and the

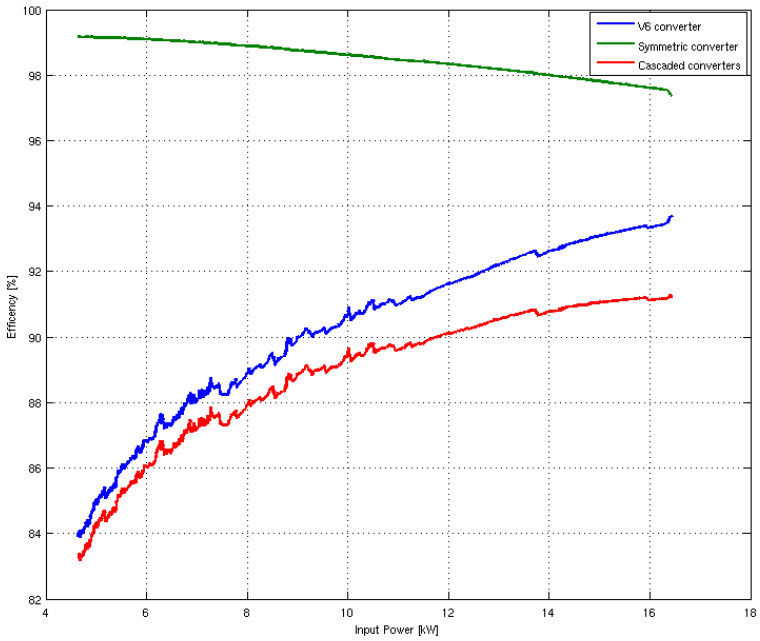


Figure 4.25: Simulation results: Efficiency of the converters as function of the output load.

Regulated Output. As it is logical the voltage in the FC and DC-Link bus keep an almost linear relation decreasing when the load increases, due to of the I-V characteristic of the FC; the two voltages keep a constant transformation ratio of the V6 converter. The regulated 270V Output, suffer a slight variations around the regulated voltage in function of the load charge with a maximum variation of 1.25V when the converter operates close to the boundary between the CCM and DCM, and a variation of 0.75 volts when the converter is at full load.

The figure **??** show the current ripple in the Fuel Cell, the DC-Link bus and the input of the SEPIC and Cúk converter at full load. The measure ripple in the output converters is 15A peak-to-peak in each converter. Since the current waveforms are 180° out-of-phase, due to the interleaved operation of the converters, they cancel each other by harmonic cancellation leading a current ripple in the bus of 6A peak-to-peak, with a DC component of 35A. The *V6* converter multiplies the current at the Fuel Cell input where a current ripple of 50A peak-to-peak is measured with a DC component of 305A; which express

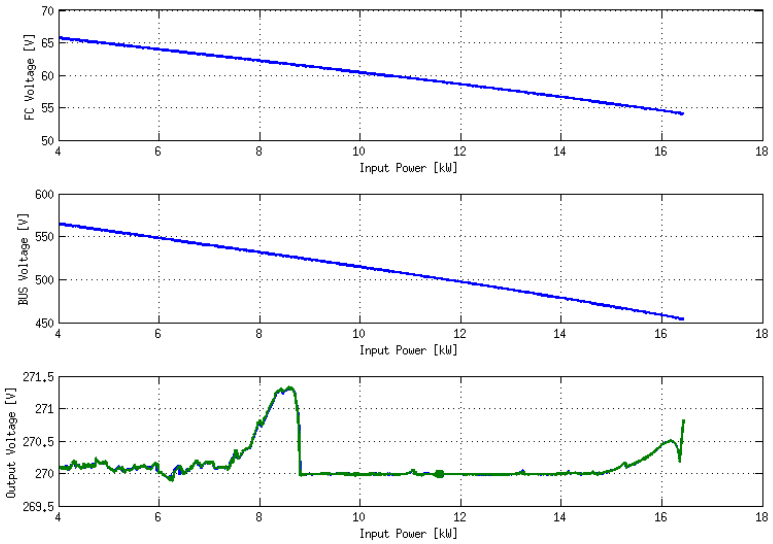


Figure 4.26: Simuation results: Votages of the FC, DC-Link, Output Votage as function of the output load.

in relative terms represents 16.5% of the current drawn. This value exceeds the 5% given in the FC specifications, however the current ripple could be decreased with a capacitor in the DC-Link Bus.

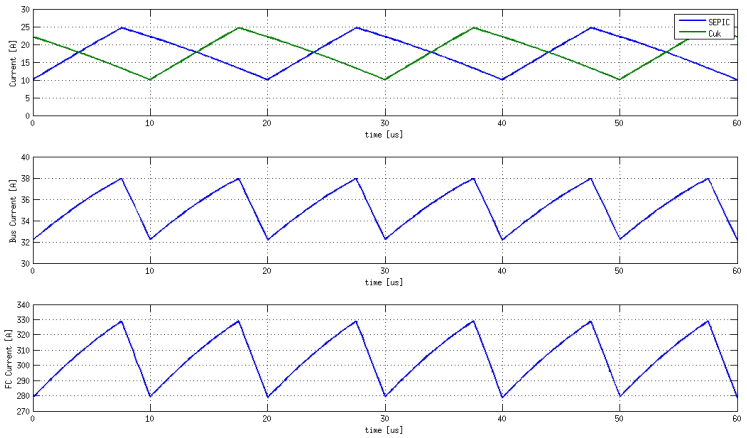


Figure 4.27: Simulation results: Current ripple at (top to bottom) SEPIC and Cúk input current , DC-Link bus and Fuel Cell

Chapter 5

Conclusions and Further Actions

The proposed topologie with the V6 and Symmetric converter for the UPC is suitable to boost the FC voltage and provide the regulated ±270V DC ouput and a high voltage DC-link for the Inverter; the achieved results demonstrate the feasability of both converters.

However in this first approach of the system important aspects of the converters desing were obviated such as enveriomental conditons, phisical and mechanical desing of the UPC and switching losses of the semiconductors. So to continue the desing and provide a real solution of the system and build the prototipe further actions should be done:

- Airbus should define the enviromental conditons for the convertar
- Airbus should define test conditions of the system (EMIs, mechanical and enviromental)
- Airbus could define the target volume of the system
- Design a refregeration system for the semiconductors, transforemrs and inductors. With the efficency achieved in the simulations, the system at least will dissipate $1.5kW$, so in order to dissipate this amount of power a water or forced air system will be necessary.
- Desing the electronics and PCBs for the converters wich has to provide at least drivers for the MOSFETs and the IGBTs, current, voltage and

temperature measurements, overcurrent protections for the switches and the control system (digital or analogic).

- Reduce the current ripple in the Fuel Cell with a filter in the DC-Link

Appendices

Appendix A

Datasheets

HYDROGENICS

5985 McLaughlin Road
Mississauga, Ontario
Canada L5R 1B8
Phone: 905.361.3660
Fax: 905.361.3626

HyPM® HD 16-500-01
FUEL CELL POWER MODULE

SPECIFICATION SHEET

October 16, 2008

Part Number: 1035785

HYDROGENICS

5985 McLaughlin Road
Mississauga, Ontario
Canada L5R 1B8
Phone: 905.361.3660
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The following are technical specifications for the HyPM HD 16-500-01 Fuel Cell Power Module (FCPM). The following supporting documents are enclosed:

1. Photographs
2. Dimensions
3. Technical Data
4. Performance
5. Mechanical Interface Diagram
6. Electrical System Signal & Power Interface Diagram

5985 McLaughlin Road
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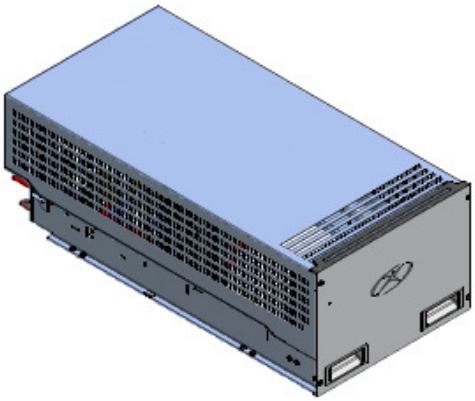
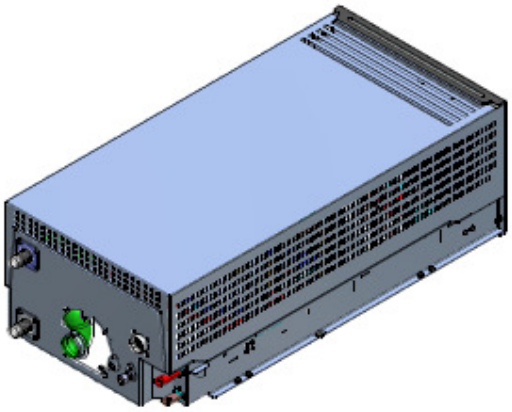
1. Photographs

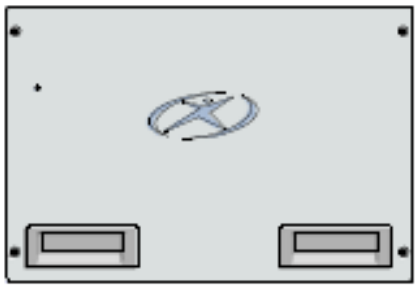
RIGHT



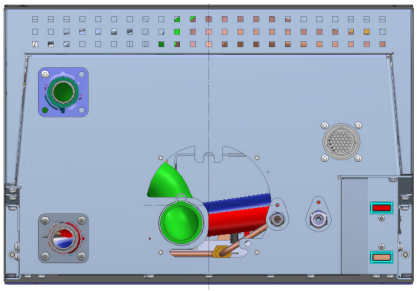
LEFT



FRONT



REAR



5985 McLaughlin Road
Mississauga, Ontario
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Phone: 905.361.3660
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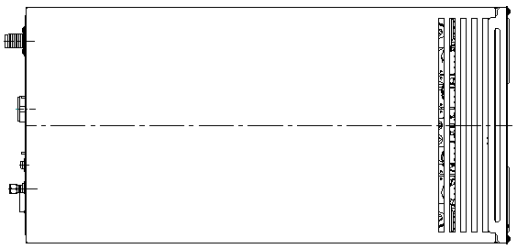
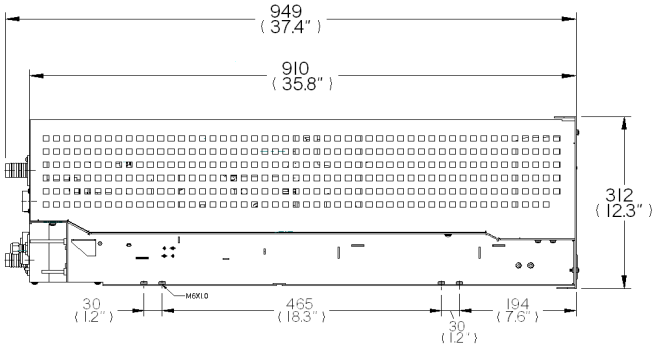
2. Dimensions

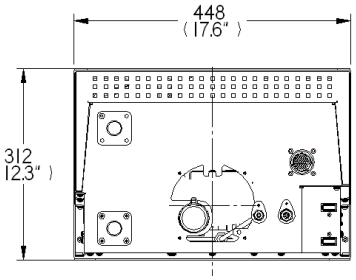
TOP



SIDE



REAR



Units: mm (±3 mm)

CONFIDENTIAL: SSN: 1035791-05

HYDROGENICS

5985 McLaughlin Road
Mississauga, Ontario
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Phone: 905.361.3660
Fax: 905.361.3626

3. Technical Data

PROPERTY	UNIT	VALUE
PRODUCT INFORMATION		
Model Number		HyPM HD 16-500-01
Part Number		1035785
PHYSICAL		
Dimensions of FCPM (L x W x H)(1)	mm	910 x 448 x 312
Total Mass	kg	114
Volume of FCPM	L	127
PERFORMANCE		
Net Electrical Power(2)	kW	16.5
Operating Current Range(3)	A_{dc}	0 to 350
Operating Voltage Range	V_{dc}	40 to 80
Peak Efficiency(4)	%	56
Time from Off Mode to Idle(5)	s	< 25
Time from Idle to 16.5 kW(6)	s	< 5
FUEL SYSTEM		
Gaseous Hydrogen(7)	%	≥ 99.99
CO	ppm	≤ 0.2
Sulfur (total, ex. H_2S, COS)	ppb	≤ 4
Total Hydrocarbons	ppm	≤ 2
Supply Pressure(8)	kPa	515 to 584
Stack Operating Pressure	kPa	< 120
Consumption(9)	lpm	< 230
Hydrogen Temperature	℃	2 to 35
AIR DELIVERY SYSTEM		
Flow Rate(9)	lpm	< 1100
Air Filtration	-	Particulate & Chemical Filter
Composition		Ambient Air
Sulfur	ppb	< 4

HYDROGENICS

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PROPERTY	UNIT	VALUE
OPERATING ENVIRONMENT		
Storage Air Temperature[10]	℃	-20 to 40
Operating Air Temperature	℃	2 to 35
Orientation	°	± 15
EMISSIONS		
Allowable Pressure Drop of Customer Cathode Exhaust	kPa	< 3
Water Collected[11]		
Anode	mL/min	< 24
Cathode	mL/min	< 32
Noise[12]	dBA	< 70
COOLING SYSTEM REQUIREMENTS		
Heat Rejection	kW	< 20
FCPM Coolant Outlet Temperature[13]	℃	40 to 60
Coolant Type		
De-ionized Water (DI H_2O)	%	100
Ethylene glycol (EG) / de-ionized water (DI H_2O)	%	40 / 60
Resistivity	kΩ·cm	> 200
Coolant Flow Rate[11] [14]	lpm	> 40
Maximum Pressure Drop of Customer Coolant System	kPa	< 20
ELECTRICAL INPUT		
Signal Voltage (FCPM Enable & E-stop)	V_{dc}	12 to 13.8
Start-up	-	12 to 13.8 V_{dc}, 300 W ≤ 25 s
MAIN SAFETIES		
Cathode Outlet High Temperature		
Communication Loss		
Coolant High Temperature		
Coolant Low Flow Rate		
FCPM Internal Over-Pressure		
FCPM Internal Under-Voltage		
Fuel Under Pressure		
Over-Current		
COMMUNICATION INTERFACES		
CAN v2.0A (standard 11 bit)		
Baud Rate 250 kbit/s		

HYDROGENICS

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Footnotes:

(1) All dimensions are ±3 mm.
(2) User must not exceed rated electrical power.
(3) Current is to be limited by the user and must not exceed the Current Draw Allowed (CDA) value, sent by the FCPM via CAN.
(4) Operating at 100 A_{dc} (lower heating value of hydrogen, 25°C, 101.3 kPa)
(5) During off mode, the FCPM does not require start-up or signal power
(6) Based on use of Current Draw Request (CDR) mode.
(7) Hydrogen supplied should conform to the *Hydrogen Fuel Quality Specification Guideline*, published in SAE J2719, November 2005.
(8) All reported pressures are absolute pressures.
(9) At 350 A_{dc} in RUN MODE-Closed Loop. Referenced to 0°C and 101.3 kPa.
(10) For storage temperature below 2°C, the module must undergo freeze storage procedure as described in the user manual.
(11) Referenced to 25°C and 101.3 kPa.
(12) At 350 A_{dc}, measured at a 1 m distance from the FCPM.
(13) Temperature set point changes within range based on load.
(14) Flow rate is based on use of de-ionized water only.

System Integration Notes

- Warranty will be voided if the system integrator operates outside of the reported technical specifications.
- An overall system controller or a computer capable of communicating via the CAN interface to the control the FCPM is required.
- Ensure there is no air flow through the cathode inlet or outlet of the FCPM when not operational.
- Fuel storage medium is to be supplied by the system integrator.
- Install a hydrogen supply valve and a safety relief device between the hydrogen delivery system and the FCPM.
- A varying number of hydrogen sensors and leak detectors may be required, depending on the specific requirements and conditions at the installation site.
- Limit the 12 V_{dc} power source with a 35 A_{dc} fuse.
- For diagnostic mode operation, provide 12 to 13.8 V_{dc}, 300 W ≤ 6.5 min.
- Provide load disconnect hardware (contactor). Rating must not exceed 5 A_{dc} and 28 V_{dc} (resistive).
- Provide reverse current protection for the FCPM (ex. diode).
- Maximum peak to peak current ripple on the FCPM must not exceed 5% of the system current draw.

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- Electrical and mechanical interface connectors to the FCPM are not supplied with the module. These connectors may be purchased from Hydrogenics or directly from the manufacturer. Part numbers are provided in the installation manual.

- A de-ionized water polisher is required to be installed on user's cooling system. (This may be purchased from Hydrogenics).

- A coolant filter rated to strain particles > 381 µm is required on the coolant inlet port of the FCPM.

- A cooling loop pressure relief device is required and must be rated to a maximum of 170 kPa (ex. radiator cap).

- Three temperature control options are available:
    1. Cooling set-point is communicated via a low powered (maximum 1 A, 12 Vdc nominal) PWM signal to a radiator fan motor or cooling valve.
    2. A PWM output drives a fan motor. The maximum current of the radiator fan(s) is not to exceed 20 A at 12 Vdc.
    3. The coolant outlet temperature set-point is broadcasted on CAN.

- For freeze tolerance of the FCPM, the customer must provide:
    1. Control Power:
        - 12 to 13.8 V_{dc}, 225 W ≤ 5 min, 275 W peak
    2. Blower Power:
        - 80 V_{dc}, 2400 W ≤ 5 min, 3000 W peak

- The FCPM does not require the customer to transmit the hydrogen supply pressure to the FCPM via CAN.

- The FCPM must not run below 10% of rated power for greater than 5 minutes.

- Specifications are subject to change without notice.

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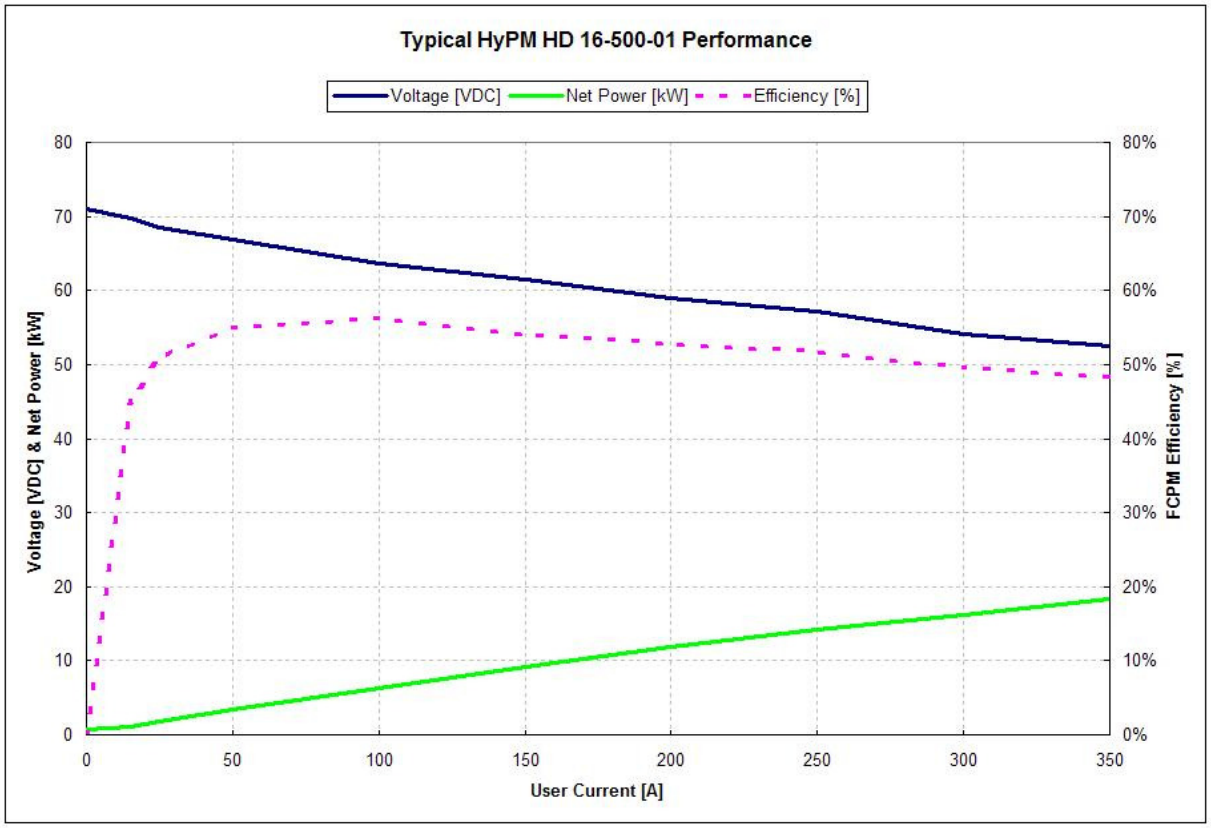
4. Typical Performance

- Below is a graph which illustrates typical HyPM HD 16-500-01 performance.



Note:

The FCPM efficiency reported in the graph above is calculated based on the lower heating value of hydrogen, at 25℃, 101.3 kPa, and takes into account all on-board parasitic loads.

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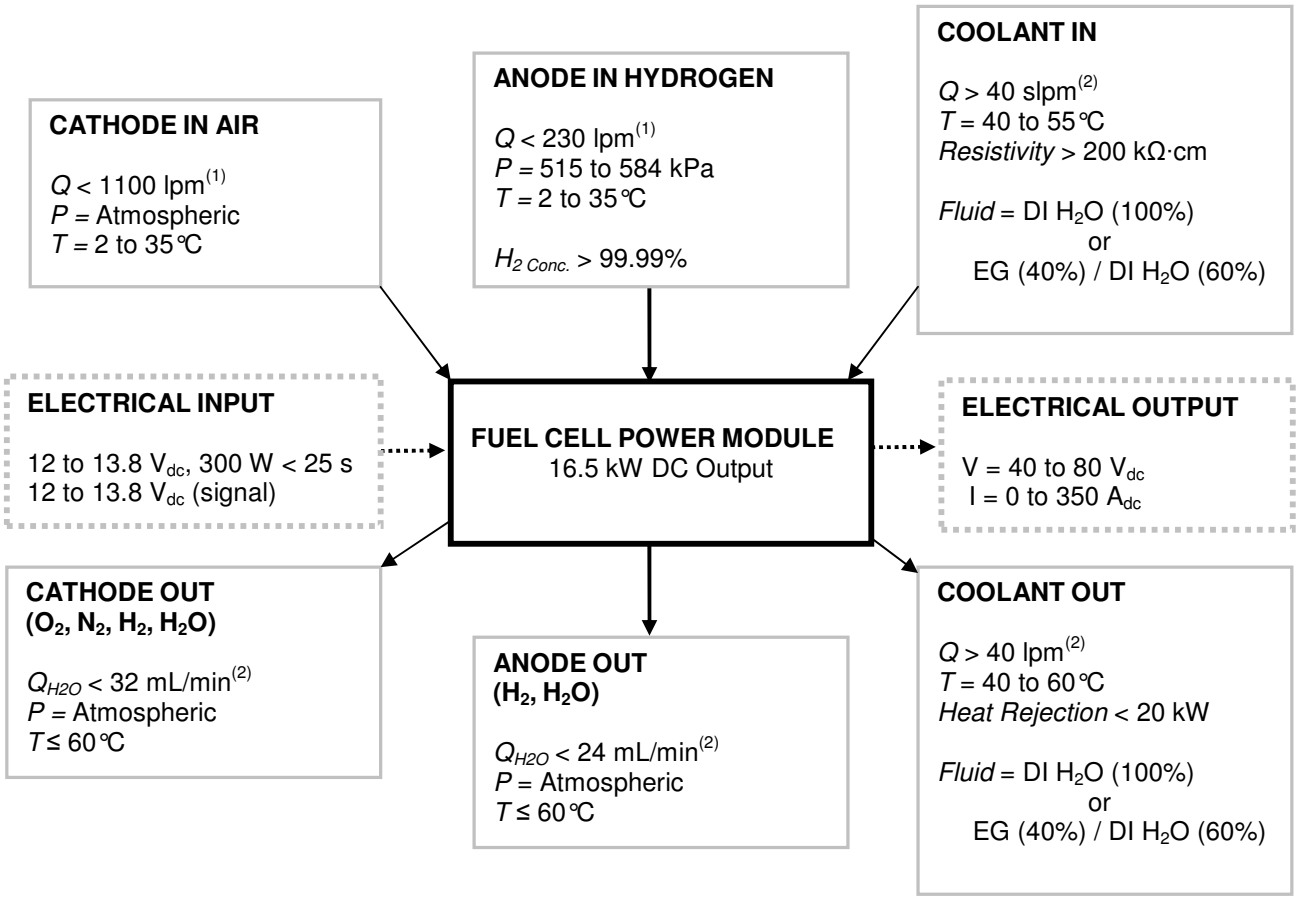
5. Mechanical Interface Diagram



(1) Referenced to 0°C and 101.3 kPa.
(2) Referenced to 25°C and 101.3 kPa.

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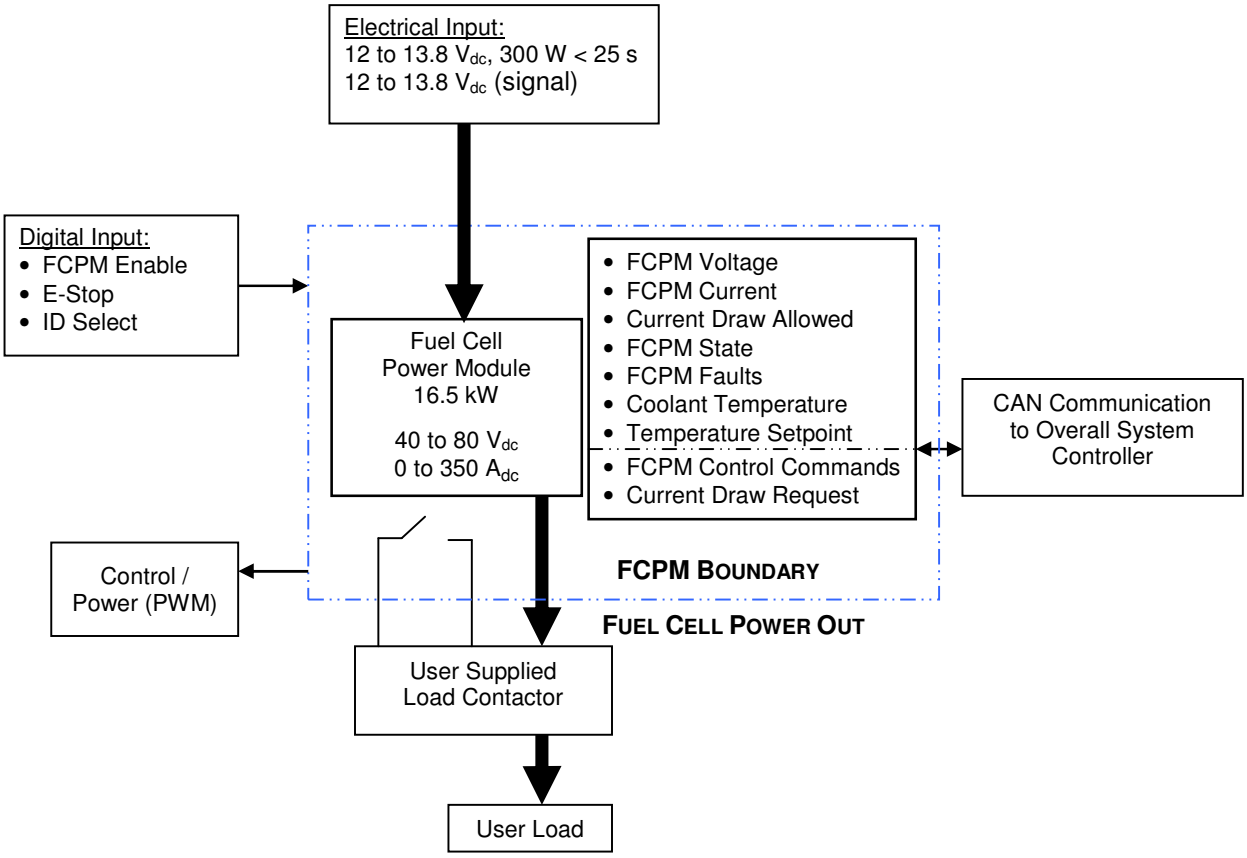
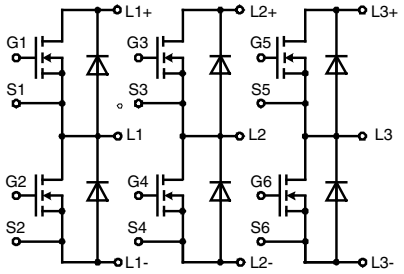
6. Electrical System Signal & Power Interface Diagram

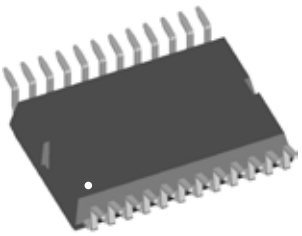


Three phase full Bridge

with Trench MOSFETs
in DCB isolated high current package

V_{DSS} = 75 V
I_{D25} = 110 A
$R_{DSon\ typ.}$ = 4.0 mΩ





MOSFETs

Symbol	Conditions	Maximum Ratings	
V_{DSS}	T_{VJ} = 25°C to 150°C	75	V
V_{GS}		± 20	V
I_{D25}	T_C = 25°C	110	A
I_{D90}	T_C = 90°C	85	A
I_{F25}	T_C = 25°C (diode)	110	A
I_{F90}	T_C = 90°C (diode)	80	A

Symbol	Conditions		Characteristic Values (T_{VJ} = 25°C, unless otherwise specified) min.	typ.	max.	
R_{DSon} [1]	on chip level at V_{GS} = 10 V	T_{VJ} = 25°C		4.0	4.9	mΩ
		T_{VJ} = 125°C		7.2	8.4	mΩ
$V_{GS(th)}$	V_{DS} = 20 V; I_D = 1 mA		2.0		4.0	V
I_{DSS}	V_{DS} = V_{DSS}; V_{GS} = 0 V	T_{VJ} = 25°C			1	µA
		T_{VJ} = 125°C		50		µA
I_{GSS}	V_{GS} = ± 20 V; V_{DS} = 0 V				0.2	µA
Q_g	V_{GS} = 10 V; V_{DS} = 36 V; I_D = 25 A			115		nC
Q_{gs}				30		nC
Q_{gd}				30		nC
$t_{d(on)}$	inductive load V_{GS} = 10 V; V_{DS} = 30 V I_D = 80 A; R_G = 39 Ω; T_J = 125°C			130		ns
t_r				100		ns
$t_{d(off)}$				500		ns
t_f				100		ns
E_{on}				0.20		mJ
E_{off}				0.50		mJ
E_{recoff}				0.01		mJ
R_{thJC}					1.0	K/W
R_{thJH}	with heat transfer paste (IXYS test setup)			1.3	1.6	K/W

[1] $V_{DS} = I_D \cdot (R_{DS(on)} + 2R_{Pin\ to\ Chip})$

Applications

AC drives
- in automobiles
  - electric power steering
  - starter generator
- in industrial vehicles
  - propulsion drives
  - fork lift drives
- in battery supplied equipment

Features

- MOSFETs in trench technology:
  - low R_{DSon}
  - optimized intrinsic reverse diode
- package:
  - high level of integration
  - high current capability
  - aux. terminals for MOSFET control
  - terminals for soldering or welding connections
  - isolated DCB ceramic base plate with optimized heat transfer
- Space and weight savings

Source-Drain Diode

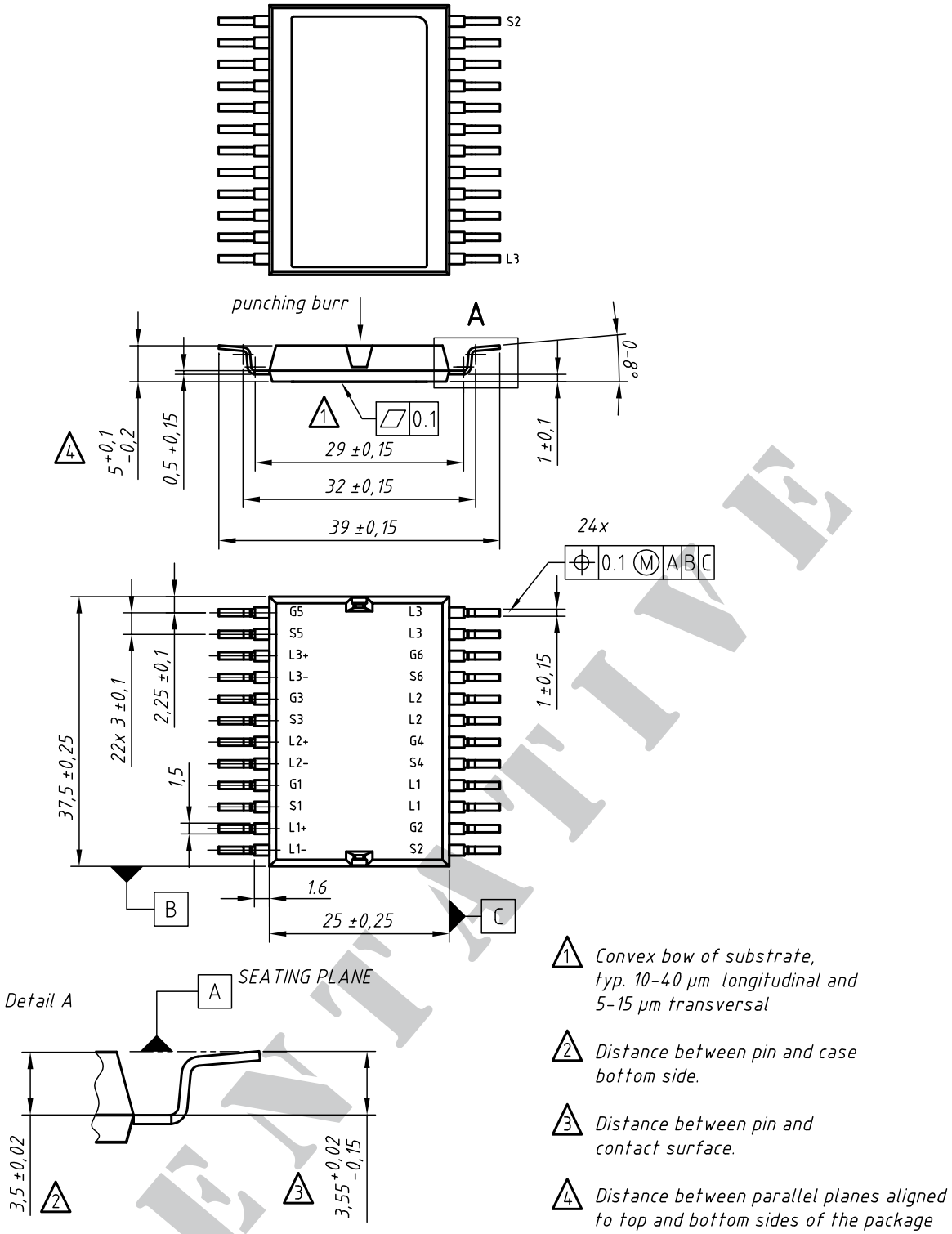
Symbol	Conditions	Characteristic Values (T_J = 25°C, unless otherwise specified) min.	typ.	max.	
V_{SD}	(diode) I_F = 80 A; V_{GS} = 0 V		0.9	1.2	V
t_{rr}	I_F = 80 A; -di_F/dt = 800 A/µs; V_R = 30 V		55		ns
Q_{RM}			0.9		µC
I_{RM}			30		A

Component

Symbol	Conditions	Maximum Ratings	
I_{RMS}	per pin in main current paths (P+, N-, L1, L2, L3) may be additionally limited by external connections 2 pins for output L1, L2, L3	75	A
T_J		-55...+175	°C
T_{stg}		-55...+125	°C
V_{ISOL}	$I_{ISOL} \leq$ 1 mA, 50/60 Hz, f = 1 minute	1000	V~
F_C	mounting force with clip	50 - 250	N

Symbol	Conditions	Characteristic Values min.	typ.	max.	
$R_{pin\ to\ chip}$ [1)]			tbd		mΩ
C_P	coupling capacity between shorted pins and back side metallization		160		pF
Weight			25		g

[1)] $V_{DS} = I_D \cdot (R_{DS(on)} + 2R_{Pin\ to\ Chip})$



1. Convex bow of substrate, typ. 10-40 µm longitudinal and 5-15 µm transversal
2. Distance between pin and case bottom side.
3. Distance between pin and contact surface.
4. Distance between parallel planes aligned to top and bottom sides of the package

contact pin:
- galv. tin plating, per pin side: Sn 10...25 µm, undercoating Ni 0,2...1 µm
- stamping edges may be free of tin
- puching burr: ≤ 0,05mm

Leads	Ordering	Part Name & Packing Unit Marking	Part Marking	Delivering Mode	Base Qty.	Ordering Code
SMD	Standard	GMM 3x120-0075X2 - SMD	GMM 3x120-0075X2	Blister	36	507 508

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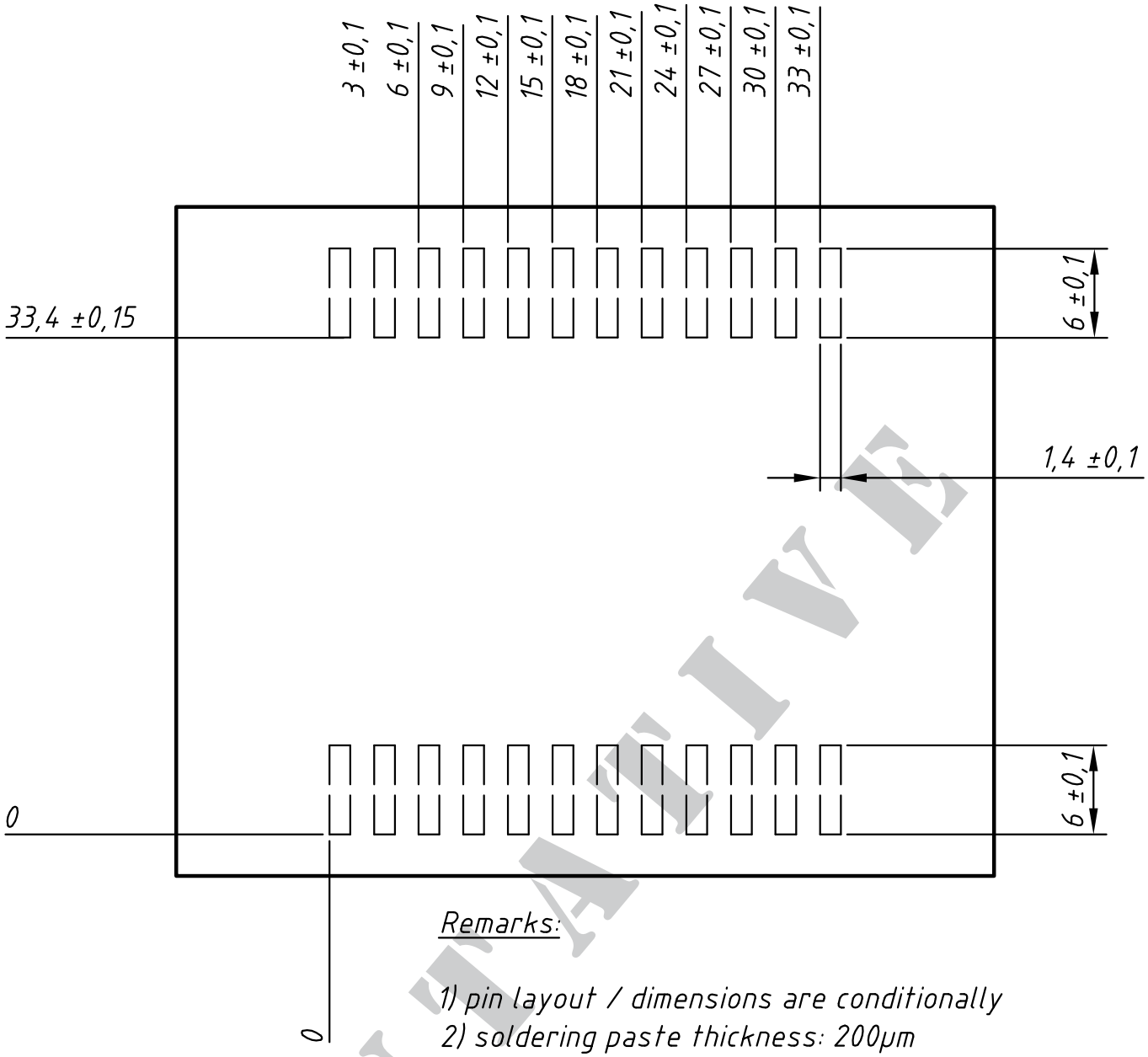
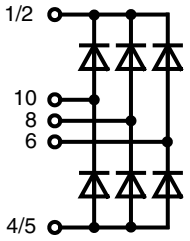
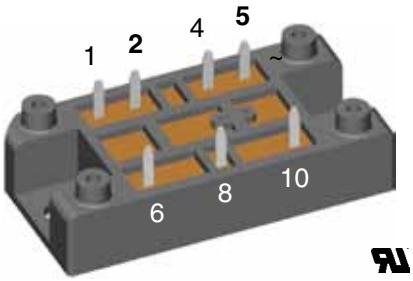


Three Phase Rectifier Bridge

I_{dAV} = 25 A
V_{RRM} = 800-1800 V

$V_{RSM/DSM}$ V	$V_{RRM/DRM}$ V	Type
900	800	VUO 22-08NO1
1300	1200	VUO 22-12NO1
1500	1400	VUO 22-14NO1
1700	1600	VUO 22-16NO1
1900	1800	VUO 22-18NO1





Symbol	Conditions			Maximum Ratings	
I_{dAV}	T_C = 90°C, module			22	A
I_{dAV}	T_A = 45°C (R_{thKA} = 0.5 K/W), module			25	A
I_{dAVM}	module			25	A
I_{FSM}	T_{VJ} = 45°C;	t = 10 ms	(50 Hz)	100	A
	V_R = 0	t = 8.3 ms	(60 Hz)	106	A
	T_{VJ} = T_{VJM};	t = 10 ms	(50 Hz)	85	A
	V_R = 0	t = 8.3 ms	(60 Hz)	90	A
I^2t	T_{VJ} = 45°C;	t = 10 ms	(50 Hz)	50	A^2s
	V_R = 0	t = 8.3 ms	(60 Hz)	47	A^2s
	T_{VJ} = T_{VJM};	t = 10 ms	(50 Hz)	36	A^2s
	V_R = 0	t = 8.3 ms	(60 Hz)	33	A^2s
T_{VJ}				-40...+130	°C
T_{VJM}				130	°C
T_{stg}				-40...+125	°C
V_{ISOL}	50/60 Hz, RMS	t = 1 min		3000	V~
	$I_{ISOL} \leq$ 1 mA	t = 1 s		3600	V~
M_d	Mounting torque	(M5)		2 - 2.5	Nm
		(10-32 UNF)		18 - 22	lb.in.
Weight	Typ.			35	g

Symbol	Conditions		Characteristic Values	
I_R	V_R = V_{RRM}	T_{VJ} = 25°C	0.3	mA
		T_{VJ} = T_{VJM}	5.0	mA
V_F	I_F = 7 A	T_{VJ} = 25°C	1.12	V
V_{T0}	For power-loss calculations only		0.8	V
r_t			40	mΩ
R_{thJH}	per diode,	120° rect.	3.1	K/W
	per module,	120° rect.	0.516	K/W
d_S	Creeping distance on surface		12.7	mm
d_A	Creepage distance in air		9.4	mm
a	Max. allowable acceleration		50	m/s^2

Data according to IEC 60747 and refer to a single diode unless otherwise stated.

Features

- Package with DCB ceramic base plate
- Isolation voltage 3600 V~
- Planar passivated chips
- Blocking voltage up to 1800 V
- Low forward voltage drop
- UL registered E 72873

Applications

- Supplies for DC power equipment
- Input rectifiers for PWM inverter
- Battery DC power supplies
- Field supply for DC motors

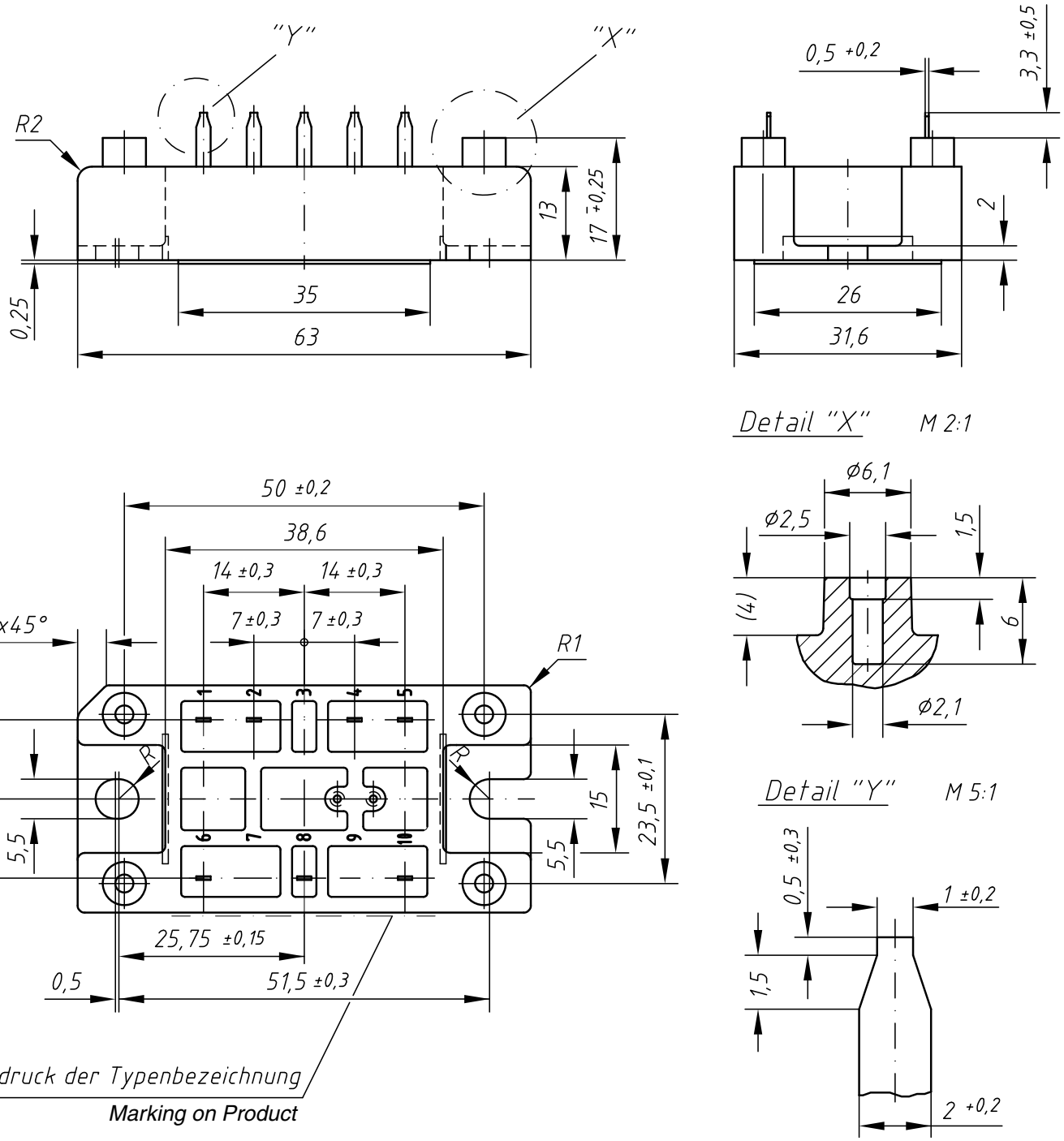
Advantages

- Easy to mount with one screw
- Space and weight savings
- Improved temperature & power cycling

IXYS reserves the right to change limits, test conditions and dimensions.

20100503a

Dimensions in mm (1 mm = 0.0394“)



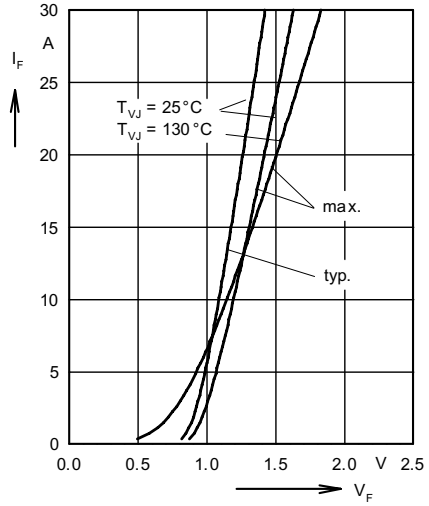


Fig. 1 Forward current versus voltage drop per diode

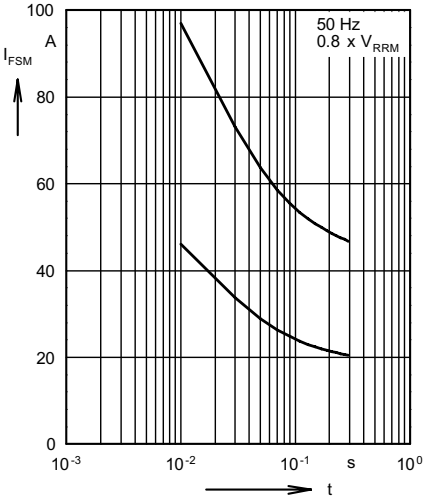


Fig. 2 Surge overload current per diode
I_{FSM}: Crest value. t: duration

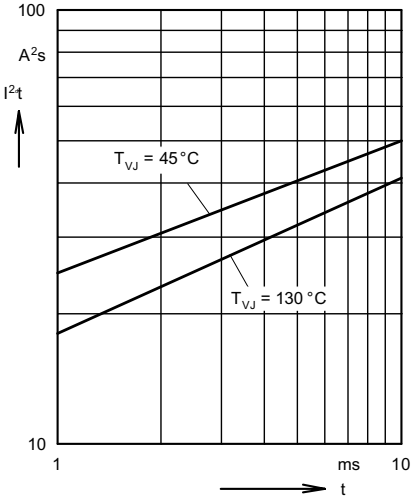


Fig. 3 I^2t versus time (1-10 ms) per diode

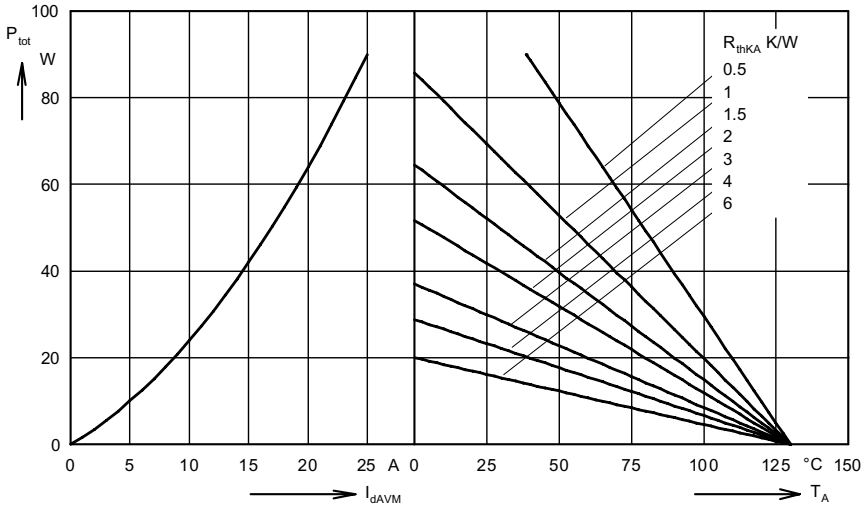


Fig. 4 Power dissipation versus direct output current and ambient temperature

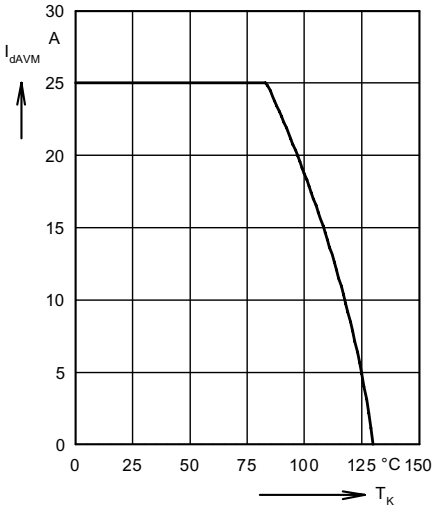


Fig. 5 Maximum forward current at case temperature

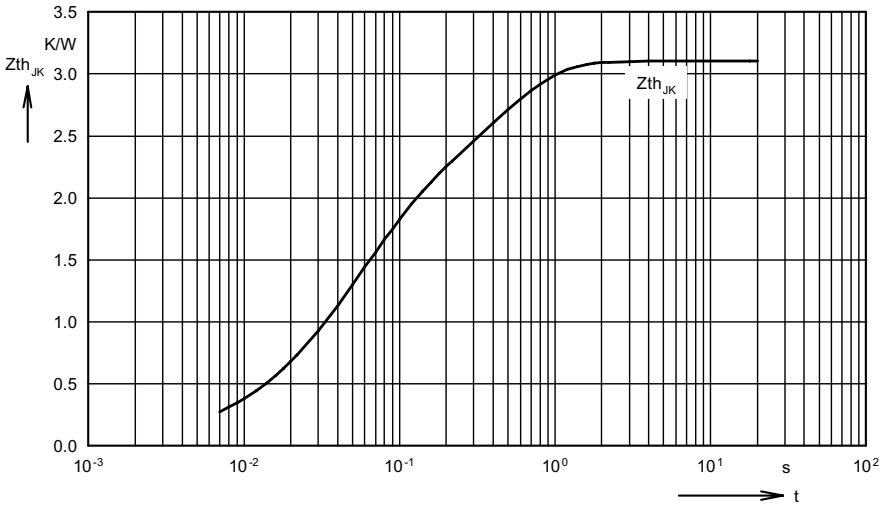


Fig. 6 Transient thermal impedance per diode

Constants for Z_{thJC} calculation:

i	R_{thi} (K/W)	t_i (s)
1	0.005	0.008
2	0.1	0.02
3	1.635	0.05
4	1.35	0.4

Three Phase Rectifier Bridge

I_{dAV} = 25 A
V_{RRM} = 800-1800 V

$V_{RSM/DSM}$ V	$V_{RRM/DRM}$ V	Type
900	800	VUO 22-08NO1
1300	1200	VUO 22-12NO1
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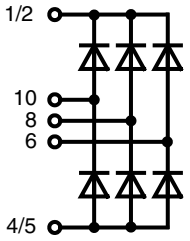

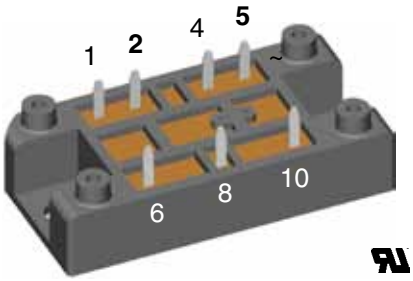

Symbol	Conditions			Maximum Ratings	
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I_{dAV}	T_A = 45°C (R_{thKA} = 0.5 K/W), module			25	A
I_{dAVM}	module			25	A
I_{FSM}	T_{VJ} = 45°C;	t = 10 ms	(50 Hz)	100	A
	V_R = 0	t = 8.3 ms	(60 Hz)	106	A
	T_{VJ} = T_{VJM};	t = 10 ms	(50 Hz)	85	A
	V_R = 0	t = 8.3 ms	(60 Hz)	90	A
I^2t	T_{VJ} = 45°C;	t = 10 ms	(50 Hz)	50	A^2s
	V_R = 0	t = 8.3 ms	(60 Hz)	47	A^2s
	T_{VJ} = T_{VJM};	t = 10 ms	(50 Hz)	36	A^2s
	V_R = 0	t = 8.3 ms	(60 Hz)	33	A^2s
T_{VJ}				-40...+130	°C
T_{VJM}				130	°C
T_{stg}				-40...+125	°C
V_{ISOL}	50/60 Hz, RMS	t = 1 min		3000	V~
	$I_{ISOL} \leq$ 1 mA	t = 1 s		3600	V~
M_d	Mounting torque	(M5)		2 - 2.5	Nm
		(10-32 UNF)		18 - 22	lb.in.
Weight	Typ.			35	g

Symbol	Conditions		Characteristic Values	
I_R	V_R = V_{RRM}	T_{VJ} = 25°C	0.3	mA
		T_{VJ} = T_{VJM}	5.0	mA
V_F	I_F = 7 A	T_{VJ} = 25°C	1.12	V
V_{T0}	For power-loss calculations only		0.8	V
r_t			40	mΩ
R_{thJH}	per diode,	120° rect.	3.1	K/W
	per module,	120° rect.	0.516	K/W
d_S	Creeping distance on surface		12.7	mm
d_A	Creepage distance in air		9.4	mm
a	Max. allowable acceleration		50	m/s^2

Data according to IEC 60747 and refer to a single diode unless otherwise stated.

Features

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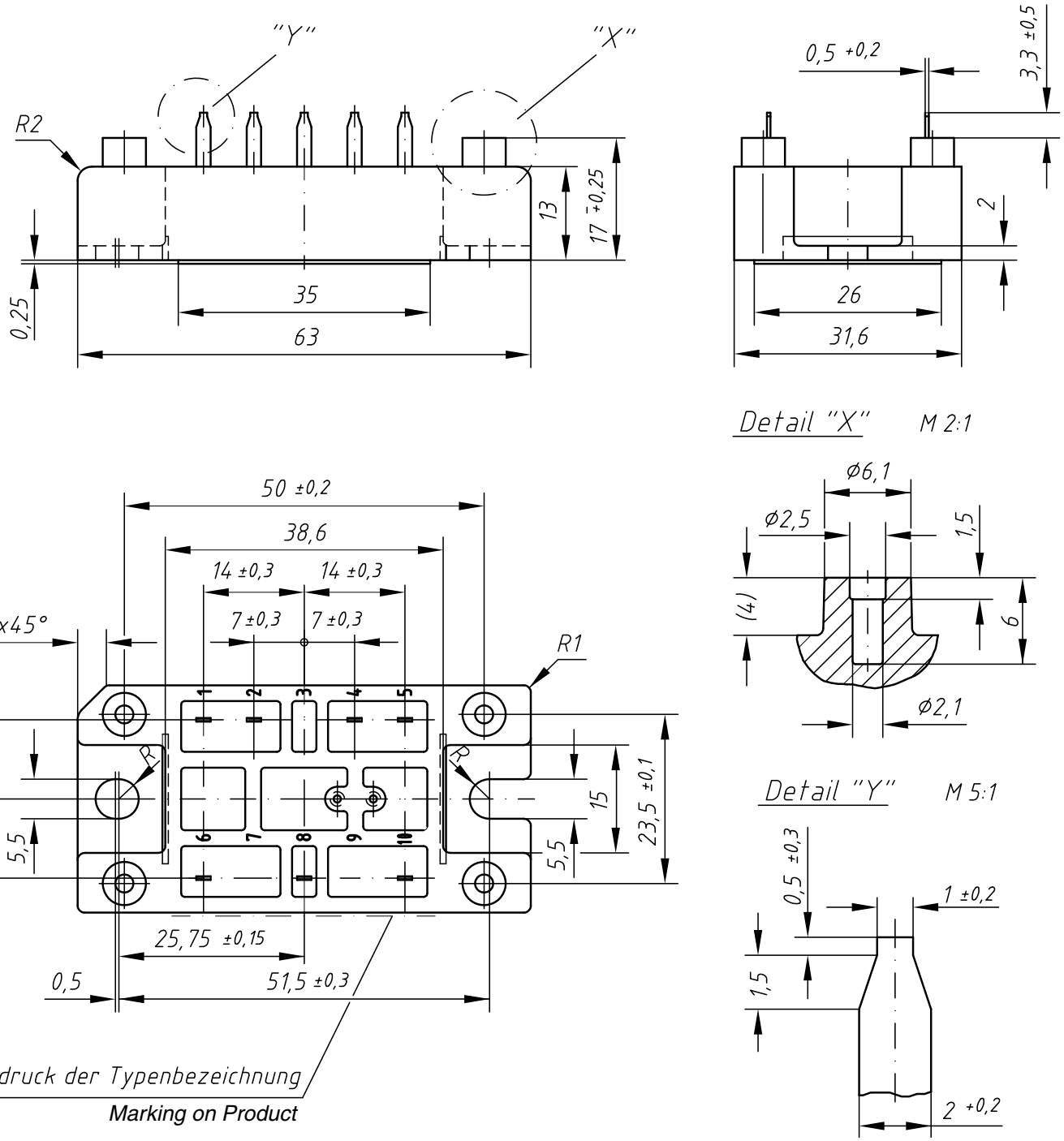


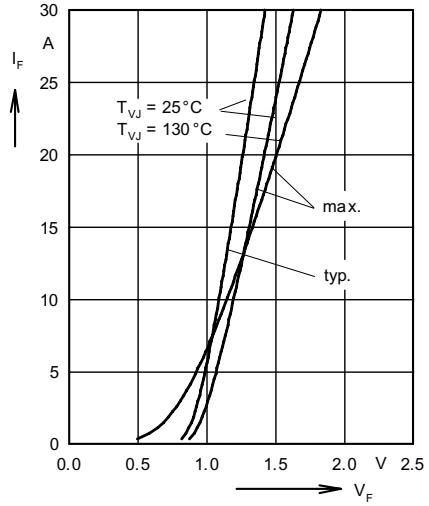


Fig. 1 Forward current versus voltage drop per diode

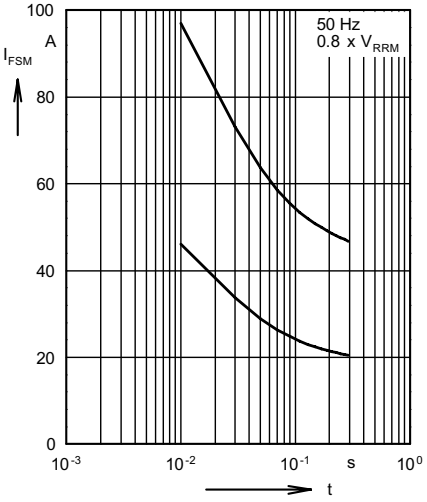


Fig. 2 Surge overload current per diode
I_{FSM}: Crest value. t: duration

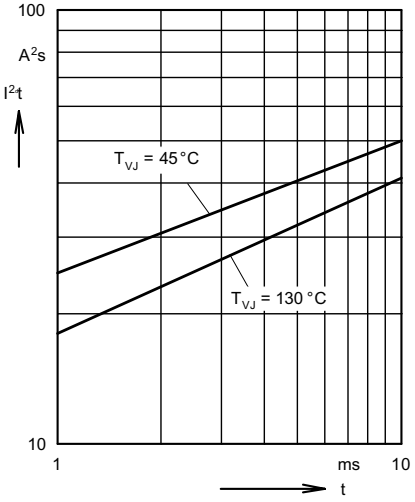


Fig. 3 I^2t versus time (1-10 ms) per diode

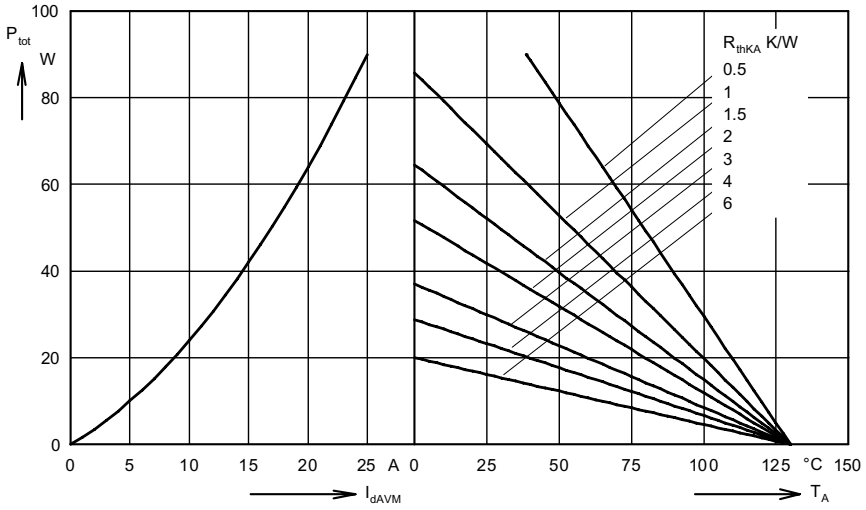


Fig. 4 Power dissipation versus direct output current and ambient temperature

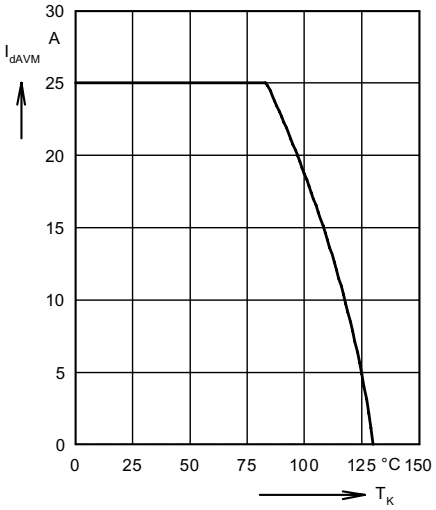


Fig. 5 Maximum forward current at case temperature

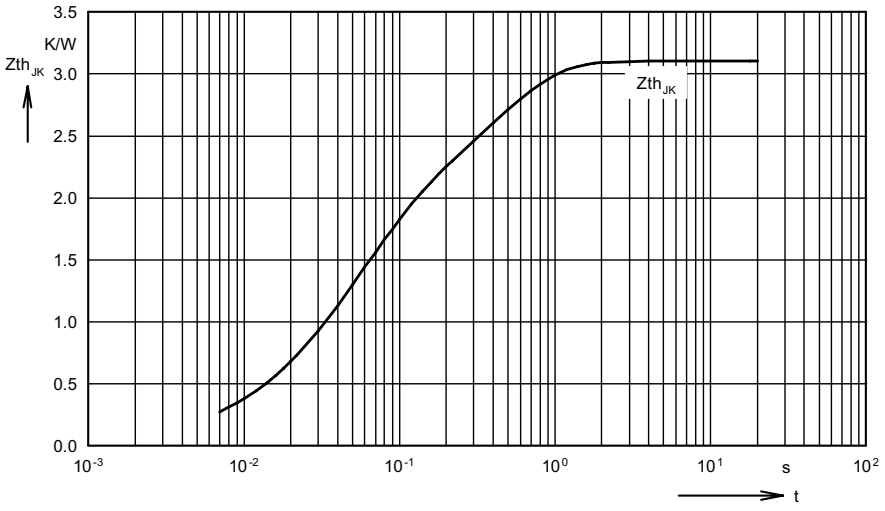


Fig. 6 Transient thermal impedance per diode

Constants for Z_{thJC} calculation:

i	R_{thi} (K/W)	t_i (s)
1	0.005	0.008
2	0.1	0.02
3	1.635	0.05
4	1.35	0.4

PAYTON GROUP

P.O.B 4068 RISHON LE ZION 75140 ISRAEL TEL.972 3 9616601, 9611164 ◆ FAX. 972 3 9616677

PAYTON 7872 W SMPS TRANSFORMER.
Functional specs.

Date : 15/11/09

1.	Generic Type	:	T1000DC-2-6.
2.	Output power	:	7872 W (164 Vdc/48 Adc).
3.	Operating frequency of trafo	:	100 kHz.
4.	Output ripple frequency	:	200 kHz.
5.	Input voltage of power stage	:	57 - 72 Vdc link.
6.	Input voltage of transformer	:	55 - 70 Vpeak.
7.	Topology	:	Full bridge, 4 diodes rectifier.
8.	Operating Duty Cycle	:	2x0.5.
9.	Operating Volt-Sec product	:	2x275 V-usec, max.
10.	Pri. to Sec. turns ratio (Sec. current - 48 Arms)	:	1 : 3.
11.	Pri. current, max. (for 90% power supply effic.)	:	159 Arms.
12.	Dielectric strength (Sec. to Pri.+ Core) (Pri. to Core)	: :	500 Vdc. 500 Vdc.
13.	Ambient temperature range	:	0 ÷ 50°C.
14.	Estimated total losses **(With 55°C heat sink)**	:	60 W.
15.	Estimated HOT SPOT temperature **(With 55°C heat sink)**	:	110°C.
16.	Mechanical dimensions. (for reference only)	:	Length - 135mm. Width - 89mm. Height - 32mm.

PAYTON GROUP

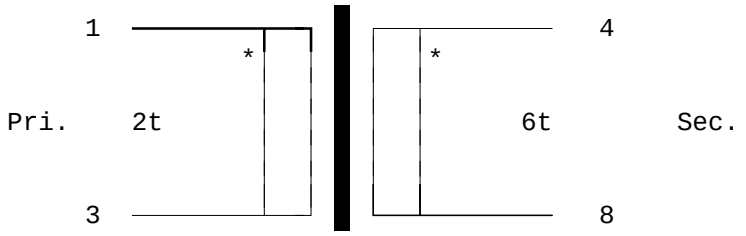
P.O.B 4068 RISHON LE ZION 75140 ISRAEL TEL.972 3 9616601, 9611164 ◆ FAX. 972 3 9616677

PAYTON 7872 W SMPS TRANSFORMER.

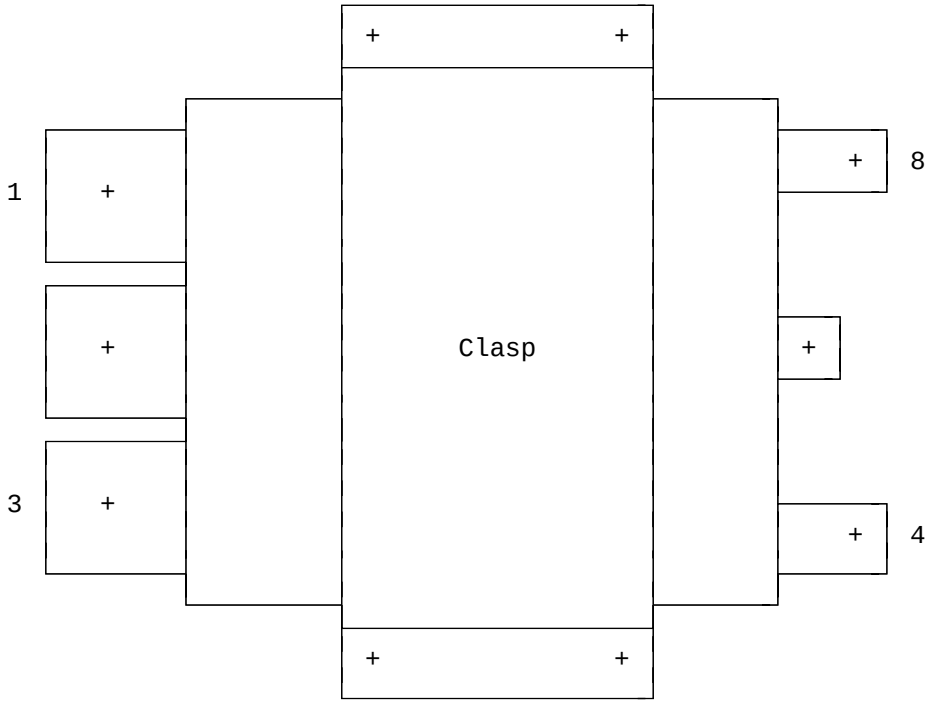
Functional specs.

Date : 15/11/09

Electrical diagram.



Terminations and fixations holes location sketch (top view; not in scale).



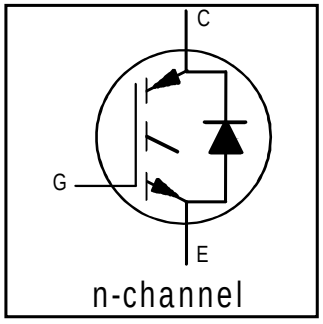
Note: All terminations made of copper strips suitable for screw connections of cable shoes.

International
IOR Rectifier

PD- 91788

IRG4PF50WD

INSULATED GATE BIPOLAR TRANSISTOR WITH ULTRAFAST SOFT RECOVERY DIODE



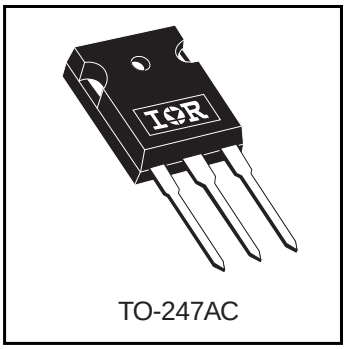
V_{CES} = 900V

$V_{CE(on)\ typ.}$ = 2.25V

@V_{GE} = 15V, I_C = 28A

Features

- Optimized for use in Welding and Switch-Mode Power Supply applications
- Industry benchmark switching losses improve efficiency of all power supply topologies
- 50% reduction of Eoff parameter
- Low IGBT conduction losses
- Latest technology IGBT design offers tighter parameter distribution coupled with exceptional reliability
- IGBT co-packaged with HEXFRED™ ultrafast, ultra-soft-recovery anti-parallel diodes for use in bridge configurations
- Industry standard TO-247AC package



TO-247AC

Benefits

- Lower switching losses allow more cost-effective operation and hence efficient replacement of larger-die MOSFETs up to 100kHz
- HEXFRED™ diodes optimized for performance with IGBTs. Minimized recovery characteristics reduce noise, EMI and switching losses

Absolute Maximum Ratings

	Parameter	Max.	Units
V_{CES}	Collector-to-Emitter Breakdown Voltage	900	V
I_C @ T_C = 25°C	Continuous Collector Current	51	A
I_C @ T_C = 100°C	Continuous Collector Current	28	
I_{CM}	Pulsed Collector Current ①	204	
I_{LM}	Clamped Inductive Load Current ②	204	
I_F @ T_C = 100°C	Diode Continuous Forward Current	16	
I_{FM}	Diode Maximum Forward Current	204	
V_{GE}	Gate-to-Emitter Voltage	± 20	V
P_D @ T_C = 25°C	Maximum Power Dissipation	200	W
P_D @ T_C = 100°C	Maximum Power Dissipation	78	
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to + 150	°C
	Soldering Temperature, for 10 seconds	300 (0.063 in. (1.6mm) from case)	
	Mounting torque, 6-32 or M3 screw.	10 lbf•in (1.1N•m)	

Thermal Resistance

	Parameter	Min.	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case - IGBT	—	—	0.64	°C/W
$R_{\theta JC}$	Junction-to-Case - Diode	—	—	0.83	
$R_{\theta CS}$	Case-to-Sink, flat, greased surface	—	0.24	—	
$R_{\theta JA}$	Junction-to-Ambient, typical socket mount	—	—	40	
Wt	Weight	—	6 (0.21)	—	g (oz)

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)CES}$	Collector-to-Emitter Breakdown Voltage③	900	—	—	V	V_{GE} = 0V, I_C = 250µA
$\Delta V_{(BR)CES}/\Delta T_J$	Temperature Coeff. of Breakdown Voltage	—	0.295	—	V/°C	V_{GE} = 0V, I_C = 3.5mA
$V_{CE(on)}$	Collector-to-Emitter Saturation Voltage	—	2.25	2.7	V	I_C = 28A V_{GE} = 15V
		—	2.74	—		I_C = 60A See Fig. 2, 5
		—	2.12	—		I_C = 28A, T_J = 150°C
$V_{GE(th)}$	Gate Threshold Voltage	3.0	—	6.0		V_{CE} = V_{GE}, I_C = 250µA
$\Delta V_{GE(th)}/\Delta T_J$	Temperature Coeff. of Threshold Voltage	—	-13	—	mV/°C	V_{CE} = V_{GE}, I_C = 250µA
g_{fe}	Forward Transconductance ④	26	39	—	S	V_{CE} = 50V, I_C = 28A
I_{CES}	Zero Gate Voltage Collector Current	—	—	500	µA	V_{GE} = 0V, V_{CE} = 900V
		—	—	2.0		V_{GE} = 0V, V_{CE} = 10V, T_J = 25°C
		—	—	6.5	mA	V_{GE} = 0V, V_{CE} = 900V, T_J = 150°C
V_{FM}	Diode Forward Voltage Drop	—	2.5	3.5	V	I_C = 16A See Fig. 13
		—	2.1	3.0		I_C = 16A, T_J = 150°C
I_{GES}	Gate-to-Emitter Leakage Current	—	—	±100	nA	V_{GE} = ±20V

Switching Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
Q_g	Total Gate Charge (turn-on)	—	160	240		I_C = 28A
Qge	Gate - Emitter Charge (turn-on)	—	19	29	nC	V_{CC} = 400V See Fig. 8
Q_{gc}	Gate - Collector Charge (turn-on)	—	53	80		V_{GE} = 15V
$t_{d(on)}$	Turn-On Delay Time	—	71	—		T_J = 25°C
t_r	Rise Time	—	50	—	ns	I_C = 28A, V_{CC} = 720V
$t_{d(off)}$	Turn-Off Delay Time	—	150	220		V_{GE} = 15V, R_G = 5.0Ω
t_f	Fall Time	—	110	170		Energy losses include "tail" and
E_{on}	Turn-On Switching Loss	—	2.63	—		diode reverse recovery.
E_{off}	Turn-Off Switching Loss	—	1.34	—	mJ	See Fig. 9, 10, 18
E_{ts}	Total Switching Loss	—	3.97	5.3		
$t_{d(on)}$	Turn-On Delay Time	—	69	—		T_J = 150°C, See Fig. 11, 18
t_r	Rise Time	—	52	—	ns	I_C = 28A, V_{CC} = 720V
$t_{d(off)}$	Turn-Off Delay Time	—	270	—		V_{GE} = 15V, R_G = 5.0Ω
t_f	Fall Time	—	190	—		Energy losses include "tail" and
E_{ts}	Total Switching Loss	—	6.0	—	mJ	diode reverse recovery.
L_E	Internal Emitter Inductance	—	13	—	nH	Measured 5mm from package
C_{ies}	Input Capacitance	—	3300	—		V_{GE} = 0V
C_{oes}	Output Capacitance	—	200	—	pF	V_{CC} = 30V See Fig. 7
C_{res}	Reverse Transfer Capacitance	—	45	—		f = 1.0MHz
t_{rr}	Diode Reverse Recovery Time	—	90	135	ns	T_J = 25°C See Fig.
		—	164	245		T_J = 125°C 14 I_F = 16A
I_{rr}	Diode Peak Reverse Recovery Current	—	5.8	10	A	T_J = 25°C See Fig.
		—	8.3	15		T_J = 125°C 15 V_R = 200V
Q_{rr}	Diode Reverse Recovery Charge	—	260	675	nC	T_J = 25°C See Fig.
		—	680	1838		T_J = 125°C 16 di/dt = 200A/µs
$di_{(rec)M}/dt$	Diode Peak Rate of Fall of Recovery	—	120	—	A/µs	T_J = 25°C See Fig.
	During t_b	—	76	—		T_J = 125°C 17

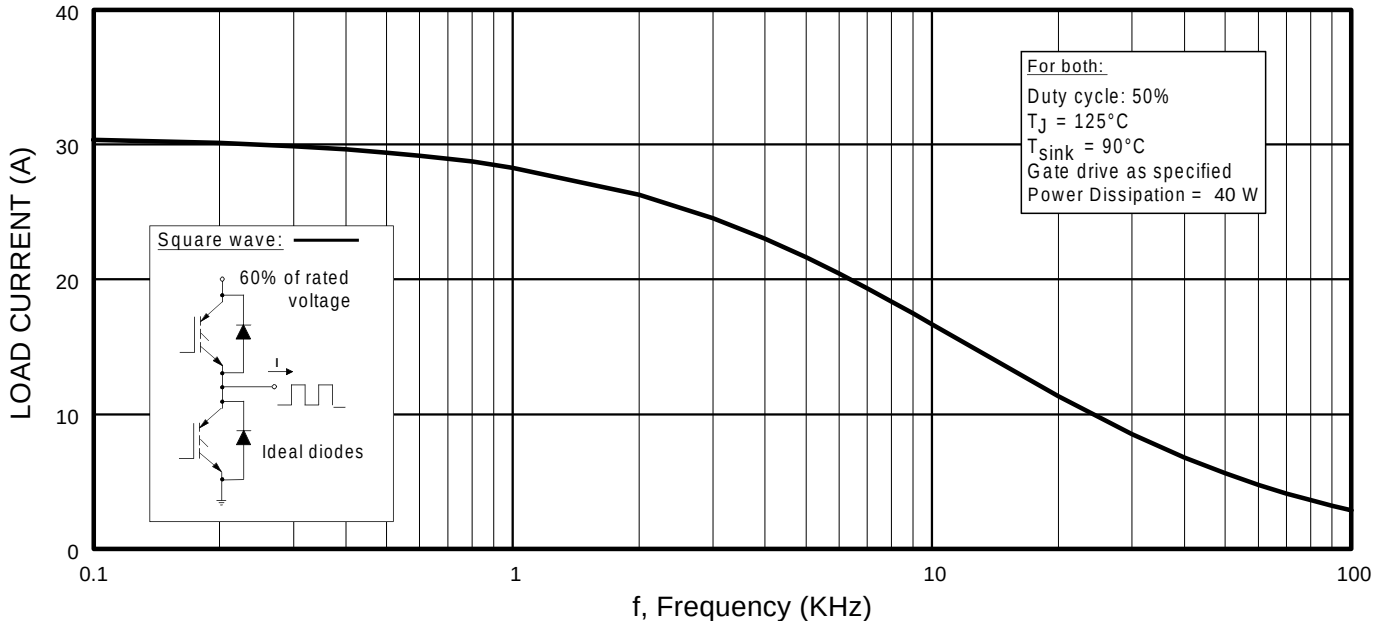


Fig. 1 - Typical Load Current vs. Frequency
(Load Current = I_{RMS} of fundamental)

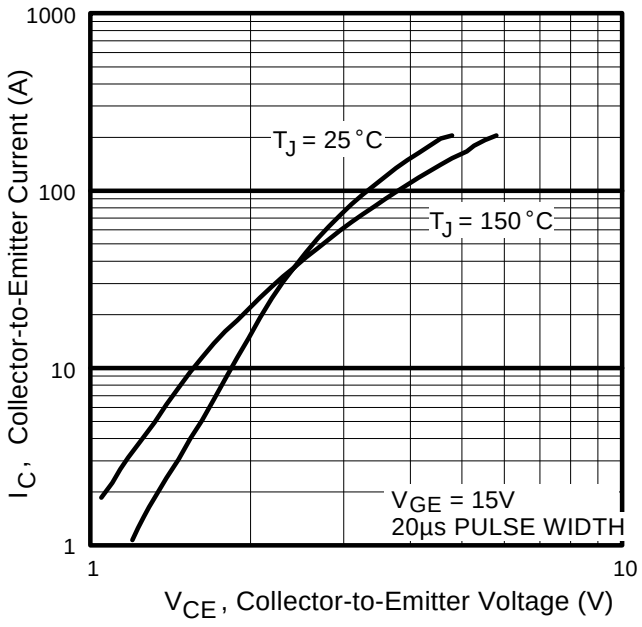


Fig. 2 - Typical Output Characteristics

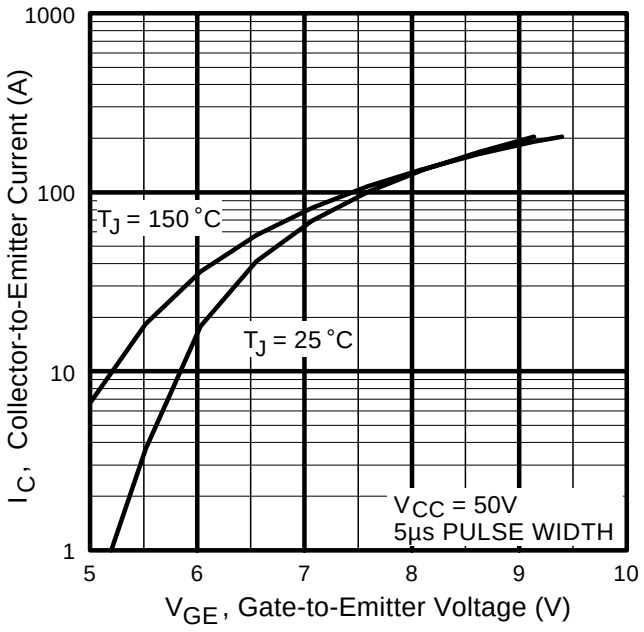


Fig. 3 - Typical Transfer Characteristics

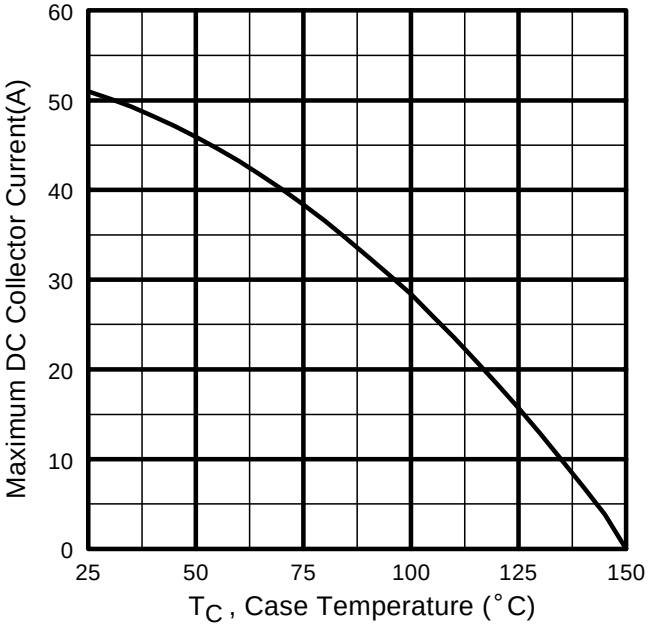


Fig. 4 - Maximum Collector Current vs. Case Temperature

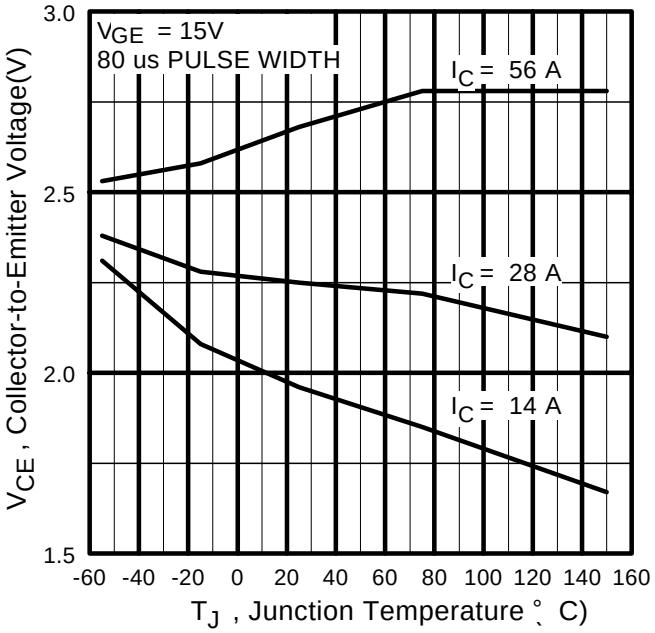


Fig. 5 - Collector-to-Emitter Voltage vs. Junction Temperature

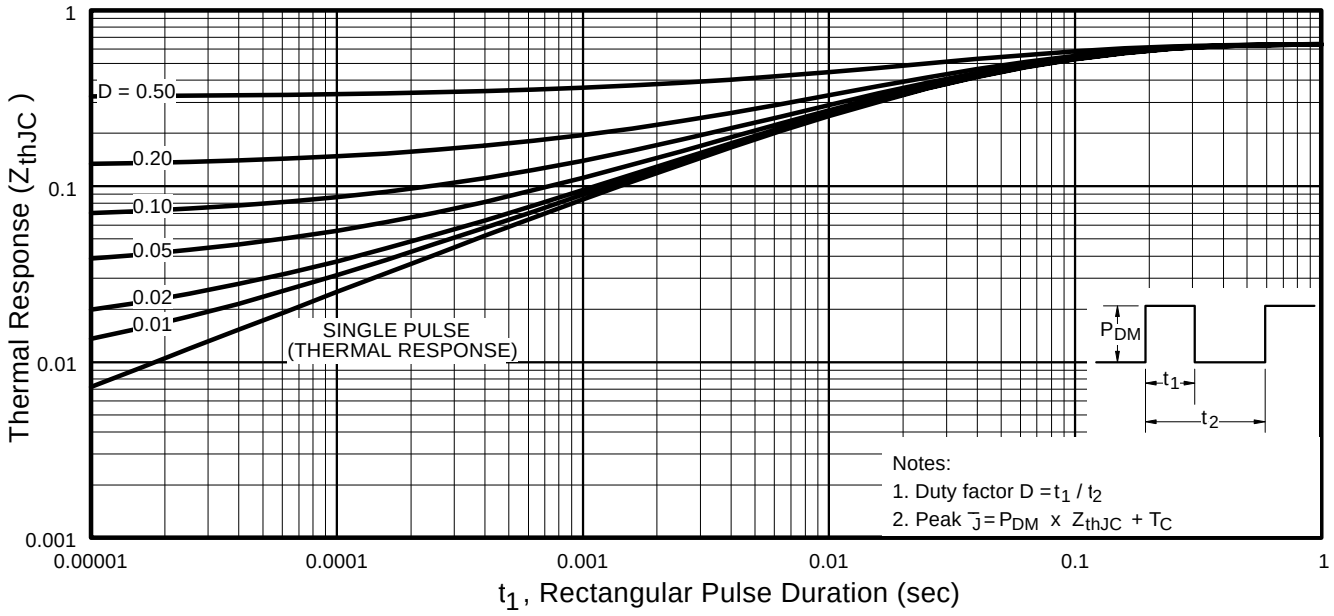


Fig. 6 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

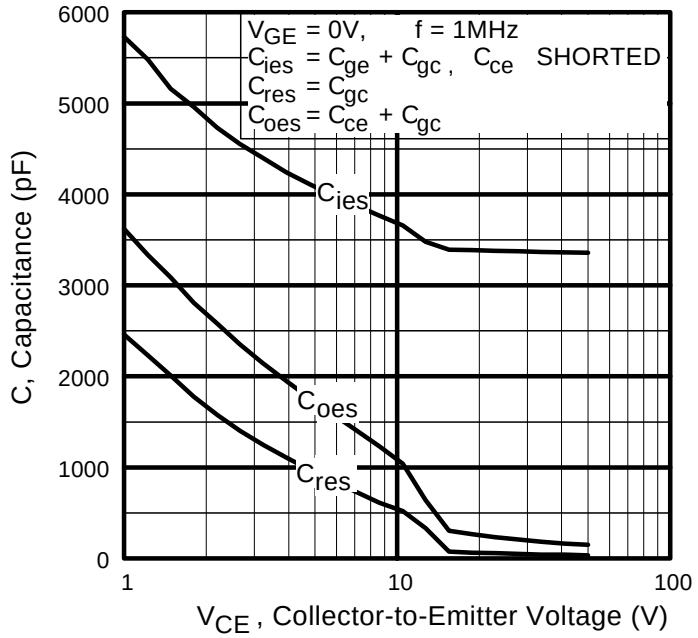


Fig. 7 - Typical Capacitance vs. Collector-to-Emitter Voltage

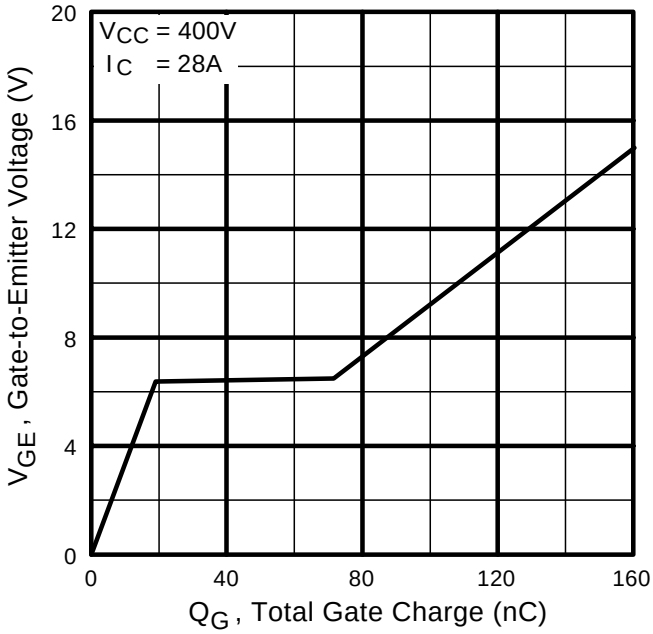


Fig. 8 - Typical Gate Charge vs. Gate-to-Emitter Voltage

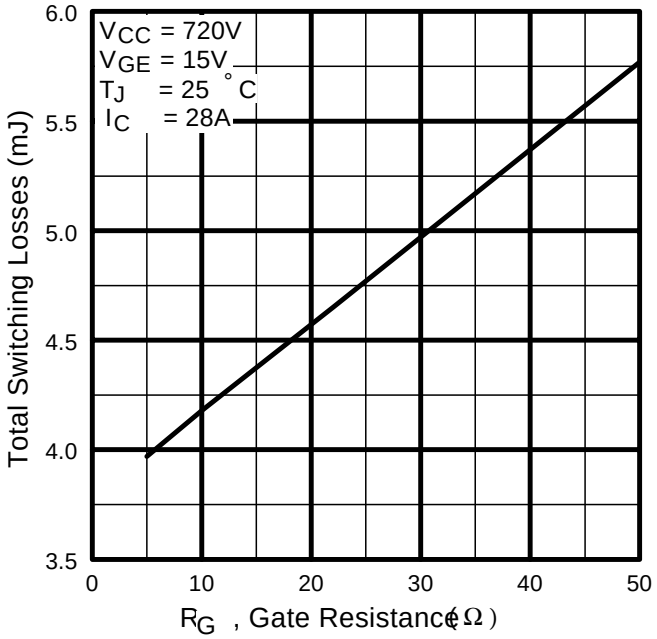


Fig. 9 - Typical Switching Losses vs. Gate Resistance

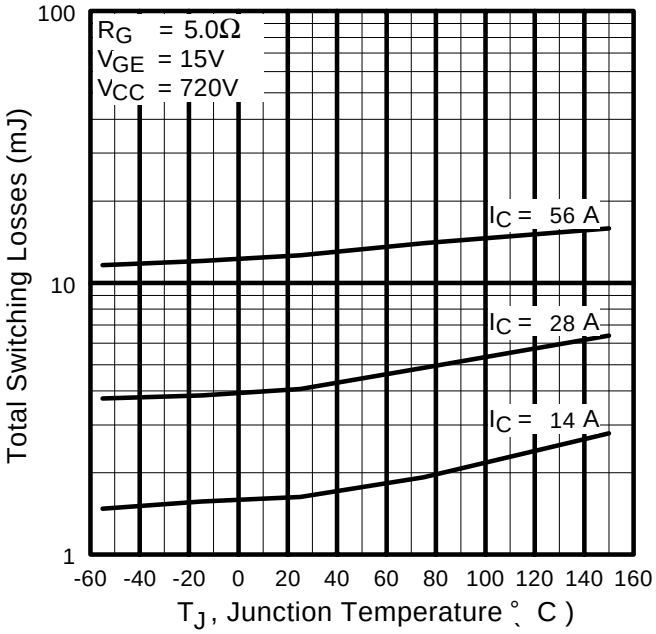


Fig. 10 - Typical Switching Losses vs. Junction Temperature

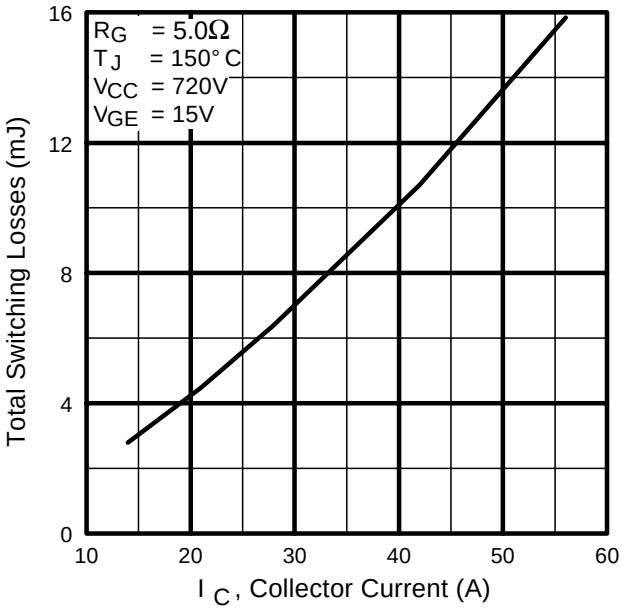


Fig. 11 - Typical Switching Losses vs. Collector-to-Emitter Current

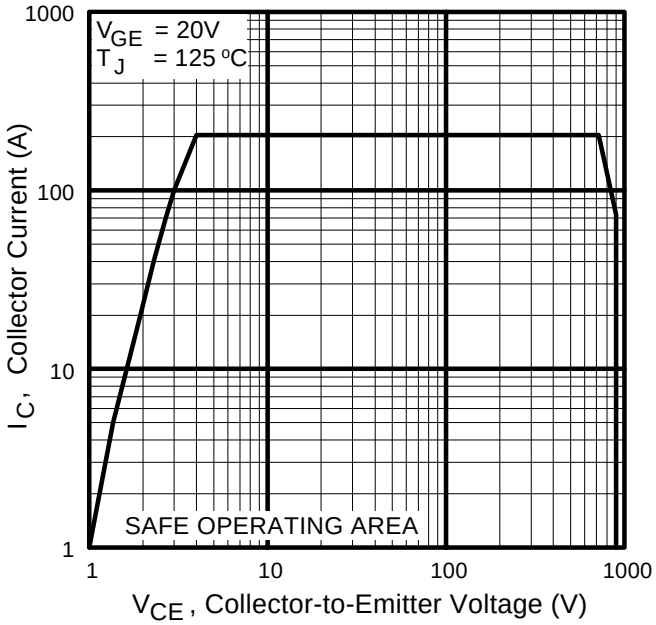


Fig. 12 - Turn-Off SOA

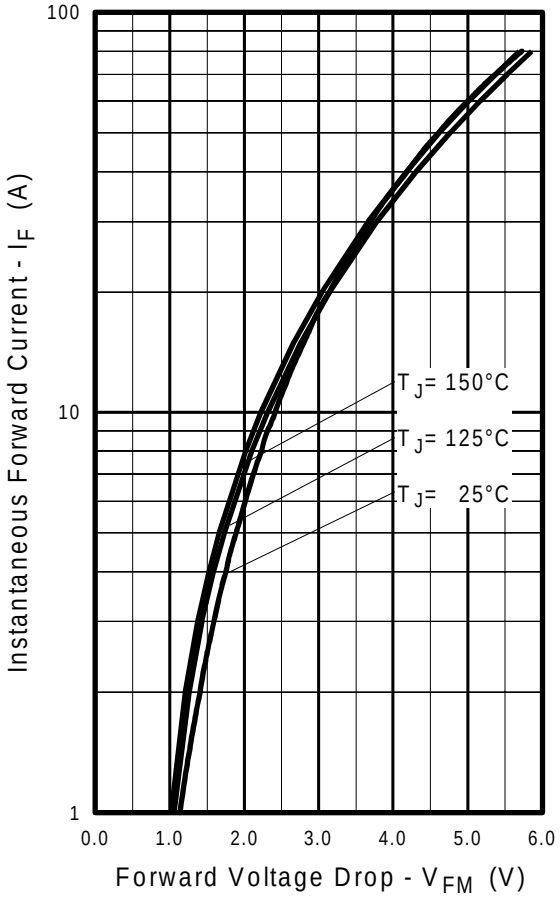


Fig. 13 - Typical Forward Voltage Drop vs. Instantaneous Forward Current

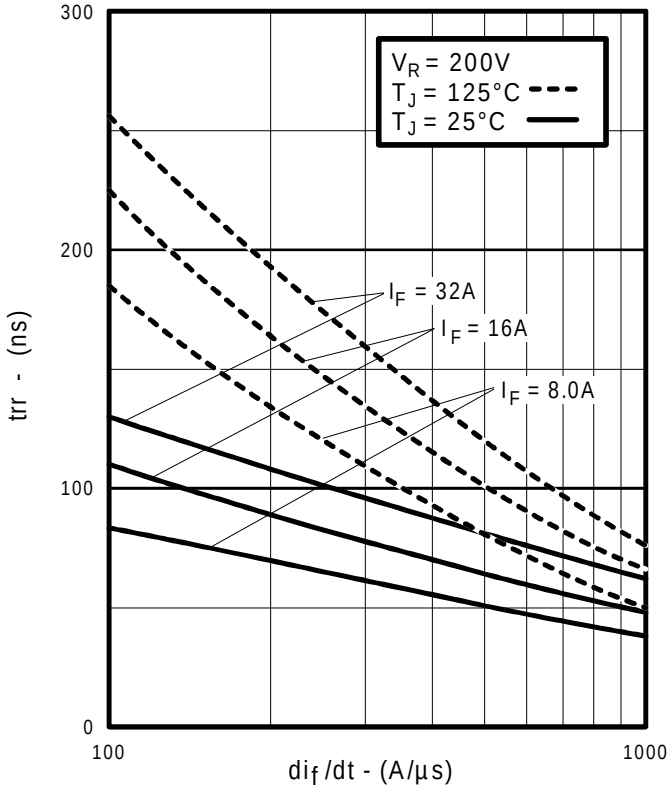


Fig. 14 - Typical Reverse Recovery vs. di_f/dt

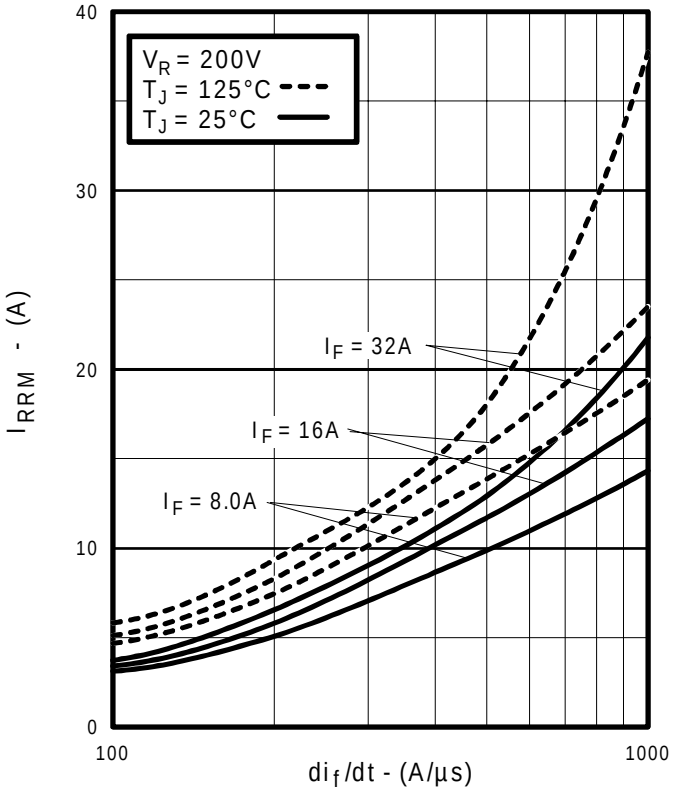


Fig. 15 - Typical Recovery Current vs. di_f/dt

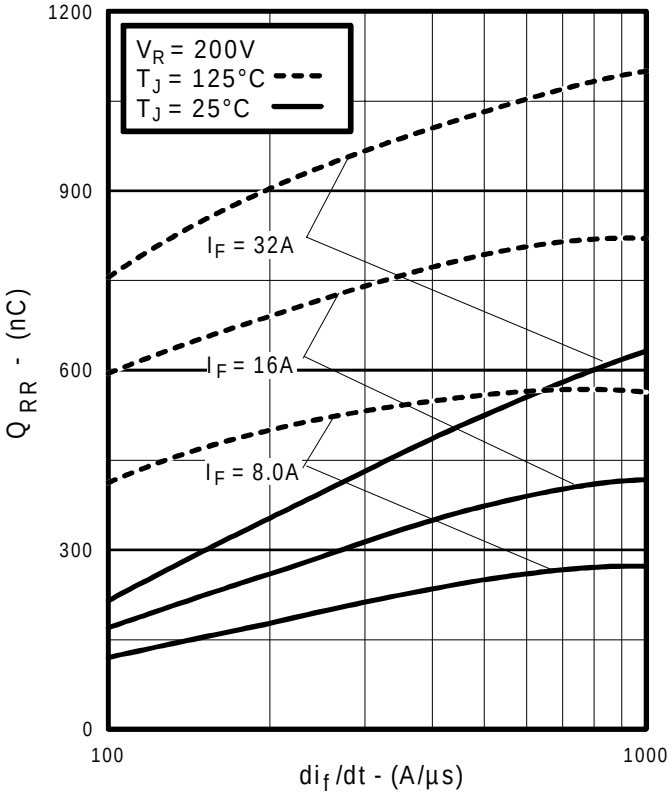


Fig. 16 - Typical Stored Charge vs. di_f/dt

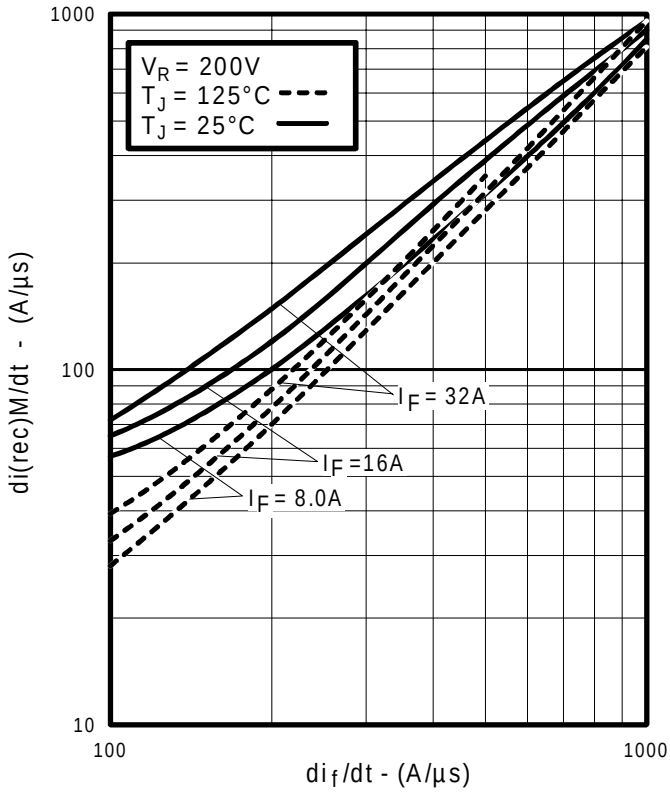


Fig. 17 - Typical $di_{(rec)M}/dt$ vs. di_f/dt

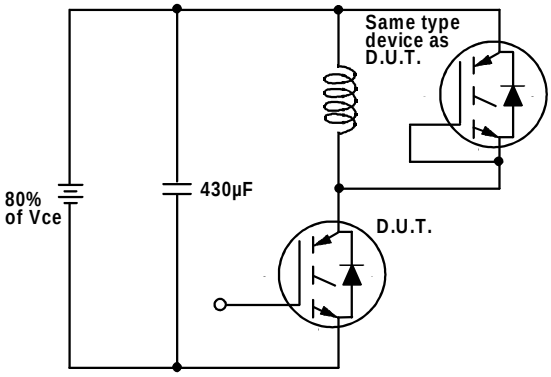


Fig. 18a - Test Circuit for Measurement of I_{LM}, E_{on}, $E_{off(diode)}$, t_{rr}, Q_{rr}, I_{rr}, $t_{d(on)}$, t_r, $t_{d(off)}$, t_f

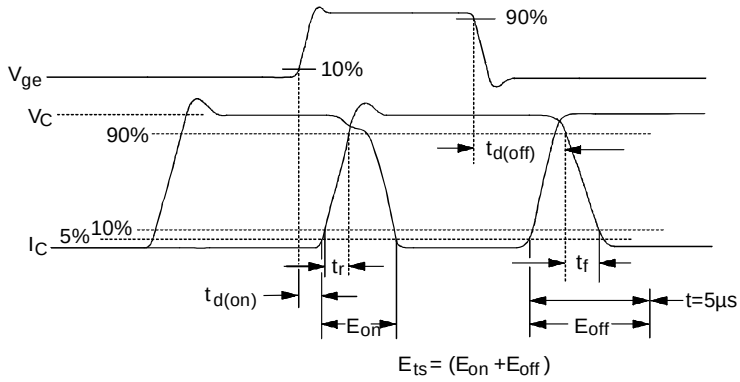


Fig. 18b - Test Waveforms for Circuit of Fig. 18a, Defining E_{off}, $t_{d(off)}$, t_f

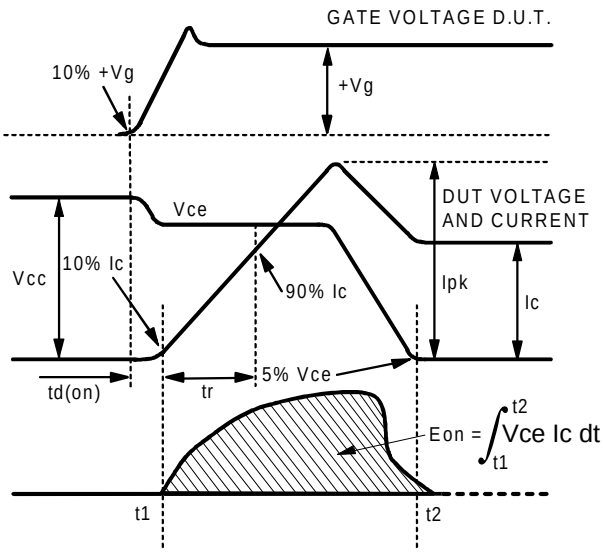


Fig. 18c - Test Waveforms for Circuit of Fig. 18a, Defining E_{on}, $t_{d(on)}$, t_r

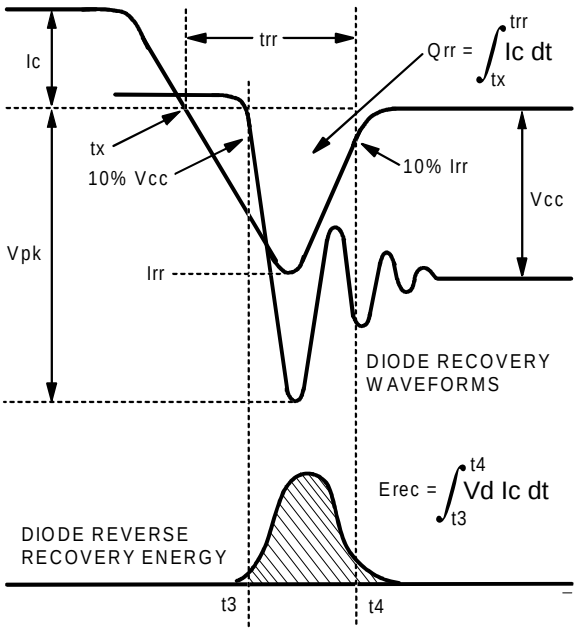


Fig. 18d - Test Waveforms for Circuit of Fig. 18a, Defining E_{rec}, t_{rr}, Q_{rr}, I_{rr}

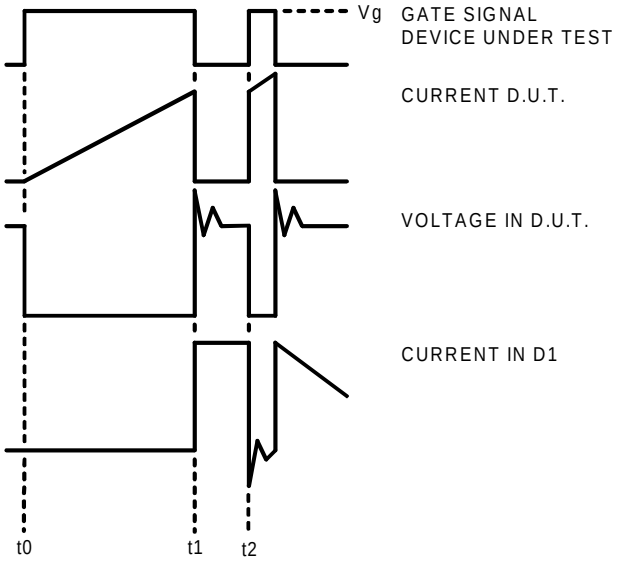


Figure 18e. Macro Waveforms for Figure 18a's Test Circuit

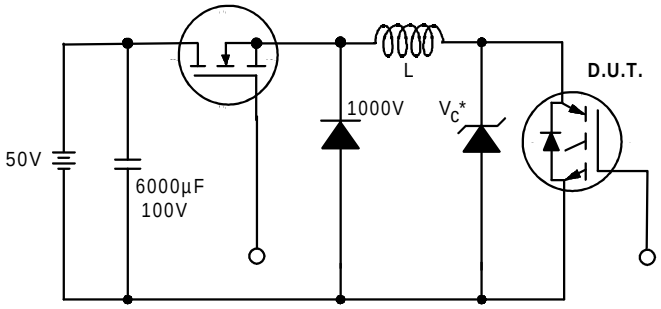


Figure 19. Clamped Inductive Load Test Circuit

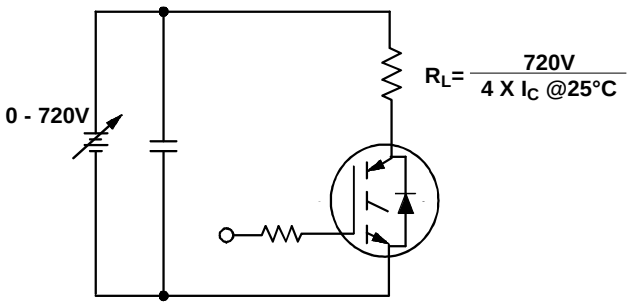


Figure 20. Pulsed Collector Current Test Circuit

Notes:

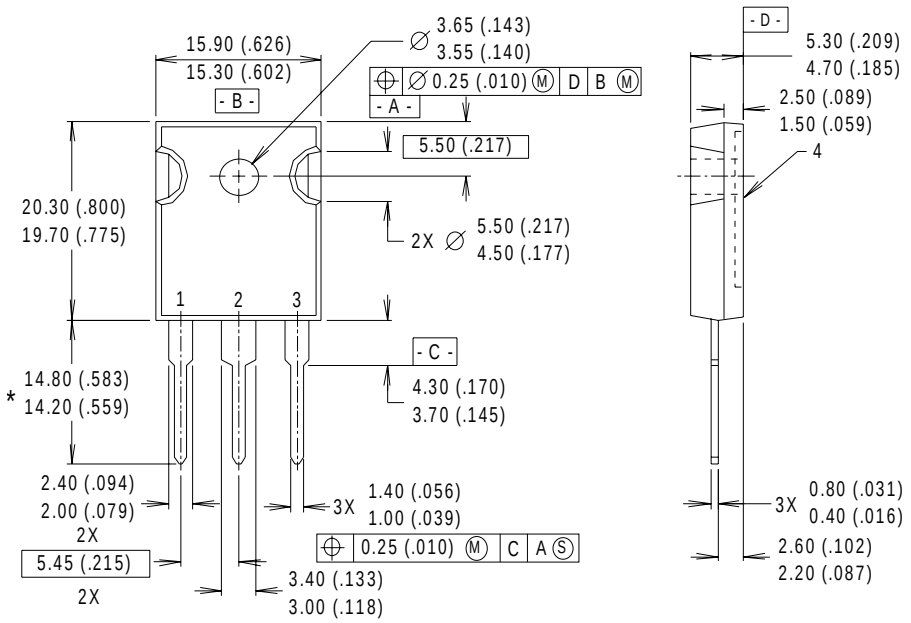
① Repetitive rating: V_{GE}=20V; pulse width limited by maximum junction temperature (figure 20)

② V_{CC}=80%(V_{CES}), V_{GE}=20V, L=10µH, R_G= 5.0Ω (figure 19)

③ Pulse width ≤ 80µs; duty factor ≤ 0.1%.

④ Pulse width 5.0µs, single shot.

Case Outline and Dimensions — TO-247AC



NOTES:
1 DIMENSIONS & TOLERANCING PER ANSI Y14.5M, 1982.
2 CONTROLLING DIMENSION : INCH.
3 DIMENSIONS ARE SHOWN MILLIMETERS (INCHES).
4 CONFORMS TO JEDEC OUTLINE TO-247AC.

LEAD ASSIGNMENTS
1 - GATE
2 - COLLECTOR
3 - EMITTER
4 - COLLECTOR

* LONGER LEADED (20mm) VERSION AVAILABLE (TO-247AD) TO ORDER ADD "-E" SUFFIX TO PART NUMBER

CONFORMS TO JEDEC OUTLINE TO-247AC (TO-3P)
Dimensions in Millimeters and (Inches)

International
IOR Rectifier

WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, Tel: (310) 322 3331
IR GREAT BRITAIN: Hurst Green, Oxted, Surrey RH8 9BB, UK Tel: ++ 44 1883 732020
IR CANADA: 15 Lincoln Court, Brampton, Ontario L6T3Z2, Tel: (905) 453 2200
IR GERMANY: Saalburgstrasse 157, 61350 Bad Homburg Tel: ++ 49 6172 96590
IR ITALY: Via Liguria 49, 10071 Borgaro, Torino Tel: ++ 39 11 451 0111
IR FAR EAST: K&H Bldg., 2F, 30-4 Nishi-Ikebukuro 3-Chome, Toshima-Ku, Tokyo Japan 171 Tel: 81 3 3983 0086
IR SOUTHEAST ASIA: 315 Outram Road, #10-02 Tan Boon Liat Building, Singapore 0316 Tel: 65 221 8371
IR TAIWAN:16 Fl. Suite D. 207, Sec. 2, Tun Haw South Road, Taipei, 10673, Taiwan Tel: 886-2-2377-9936
http://www.irf.com/ Data and specifications subject to change without notice. 7/98

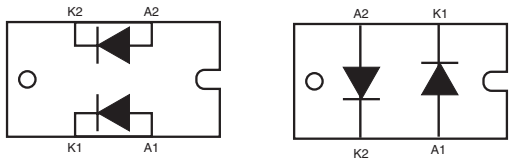
Note: For the most current drawings please refer to the IR website at:
http://www.irf.com/package/

STTH9012TV

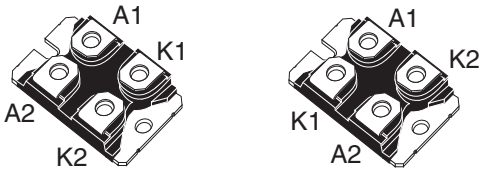
Ultrafast recovery - 1200 V diode

Main product characteristics

$I_{F(AV)}$	2 x 45 A
V_{RRM}	1200 V
T_j	150° C
V_F (typ)	1.20 V
t_{rr} (typ)	50 ns



STTH9012TV1 **STTH9012TV2**



ISOTOP

Features and benefits

- Ultrafast, soft recovery
- Very low conduction and switching losses
- High frequency and/or high pulsed current operation
- High reverse voltage capability
- High junction temperature
- Insulated package:
  Electrical insulation = 2500 V_{RMS}
  Capacitance = 45 pF

Order codes

Part Number	Marking
STTH9012TV1	STTH9012TV1
STTH9012TV2	STTH9012TV2

Description

The high quality design of this diode has produced a device with low leakage current, regularly reproducible characteristics and intrinsic ruggedness. These characteristics make it ideal for heavy duty applications that demand long term reliability.

Such demanding applications include industrial power supplies, motor control, and similar mission-critical systems that require rectification and freewheeling. These diodes also fit into auxiliary functions such as snubber, bootstrap, and demagnetization applications.

The improved performance in low leakage current, and therefore thermal runaway guard band, is an immediate competitive advantage for this device.

1 Characteristics

Table 1. Absolute ratings (limiting values per diode at 25° C, unless otherwise specified)

Symbol	Parameter			Value	Unit
V_{RRM}	Repetitive peak reverse voltage			1200	V
$I_{F(RMS)}$	RMS forward current			150	A
$I_{F(AV)}$	Average forward current, $\delta = 0.5$		T_c = 75° C per diode	45	A
I_{FRM}	Repetitive peak forward current	t_p = 5 µs, F = 5 kHz square		600	A
I_{FSM}	Surge non repetitive forward current	t_p = 10 ms Sinusoidal		420	A
T_{stg}	Storage temperature range			-65 to + 150	°C
T_j	Maximum operating junction temperature			150	°C

Table 2. Thermal parameters

Symbol	Parameter		Value	Unit
$R_{th(j-c)}$	Junction to case	Per diode	0.74	°C/W
		Total	0.42	
$R_{th(c)}$	Coupling thermal resistance		0.1	

When the diodes are used simultaneously:
$\Delta T_{j(diode1)} = P_{(diode1)} \times R_{th(j-c)}$ (per diode) + $P_{(diode2)} \times R_{th(c)}$

Table 3. Static electrical characteristics

Symbol	Parameter	Test conditions		Min.	Typ	Max.	Unit
I_R(1)	Reverse leakage current	T_j = 25° C	$V_R = V_{RRM}$			30	µA
		T_j = 125° C			30	300	
V_F(2)	Forward voltage drop	T_j = 25° C	I_F = 45 A			2.10	V
		T_j = 125° C			1.25	1.90	
		T_j = 150° C			1.20	1.80	

1. Pulse test: t_p = 5 ms, δ < 2 %
2. Pulse test: t_p = 380 µs, δ < 2 %

To evaluate the conduction losses use the following equation:
$P = 1.40 \times I_{F(AV)} + 0.0089\ I_F{}^2{}_{(RMS)}$

Table 4. Dynamic characteristics

Symbol	Parameter	Test conditions	Min.	Typ	Max.	Unit
t_{rr}	Reverse recovery time	I_F = 1 A, dI_F/dt = -50 A/µs, V_R = 30 V, T_j = 25° C			125	ns
		I_F = 1 A, dI_F/dt = -100 A/µs, V_R = 30 V, T_j = 25° C		63	85	
		I_F = 1 A, dI_F/dt = -200 A/µs, V_R = 30 V, T_j = 25° C		50	70	
I_{RM}	Reverse recovery current	I_F = 45 A, dI_F/dt = -200 A/µs, V_R = 600 V, T_j = 125° C		32	45	A
S	Softness factor	I_F = 45 A, dI_F/dt = -200 A/µs, V_R = 600 V, T_j = 125° C		1		
t_{fr}	Forward recovery time	I_F = 45 A dI_F/dt = 100 A/µs V_{FR} = 1.5 x V_{Fmax}, T_j = 25° C			700	ns
V_{FP}	Forward recovery voltage	I_F = 45 A, dI_F/dt = 100 A/µs, T_j = 25° C		4.5		V

Figure 1. Conduction losses versus average current

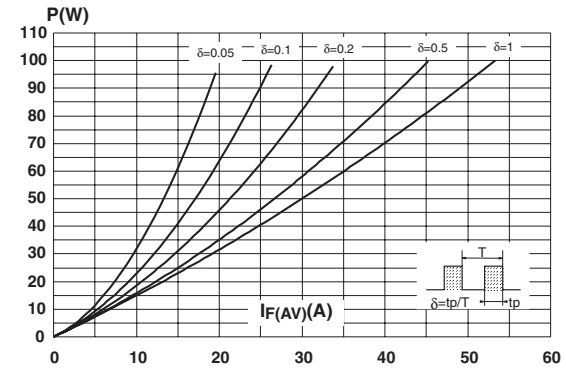


Figure 2. Forward voltage drop versus forward current

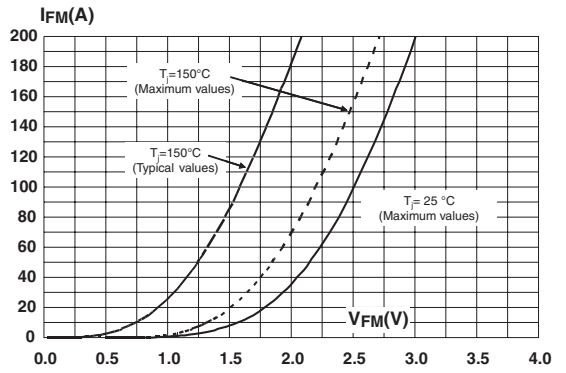


Figure 3. Relative variation of thermal impedance junction to case versus pulse duration

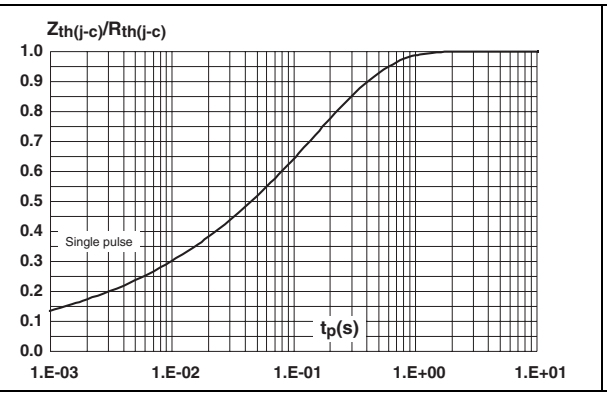


Figure 4. Peak reverse recovery current versus dI_F/dt (typical values)

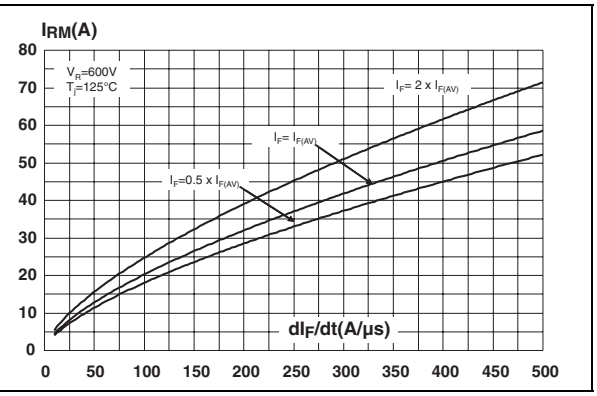


Figure 5. Reverse recovery time versus dI_F/dt (typical values)

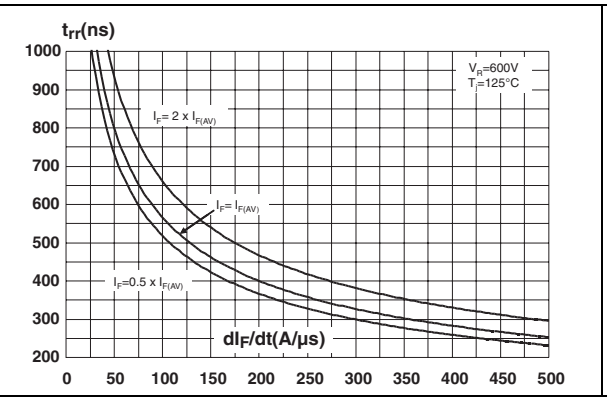


Figure 6. Reverse recovery charges versus dI_F/dt (typical values)

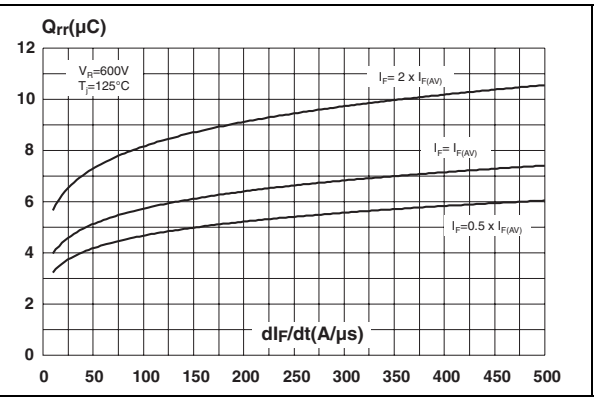


Figure 7. Softness factor versus dI_F/dt (typical values)

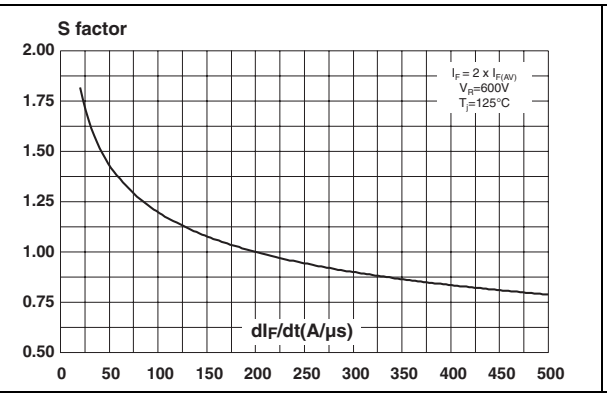


Figure 8. Relative variations of dynamic parameters versus junction temperature

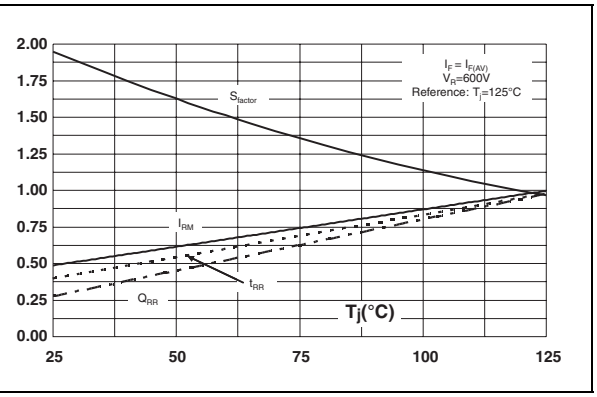


Figure 9. Transient peak forward voltage versus dI_F/dt (typical values)

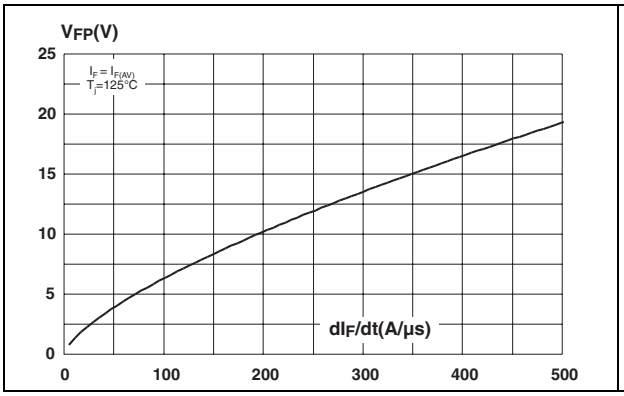


Figure 10. Forward recovery time versus dI_F/dt (typical values)

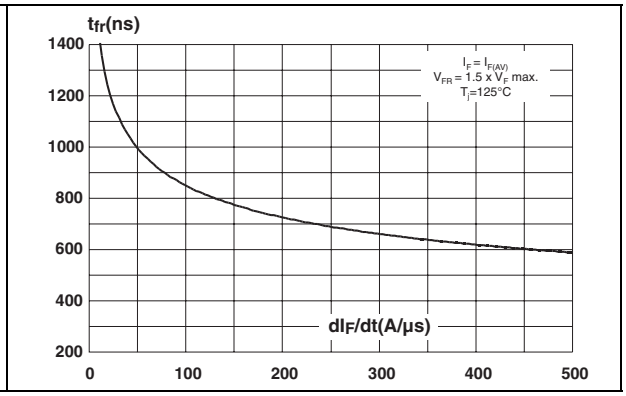
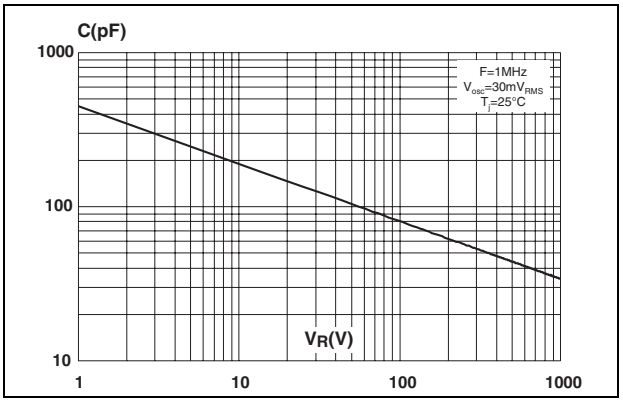


Figure 11. Junction capacitance versus reverse voltage applied (typical values)

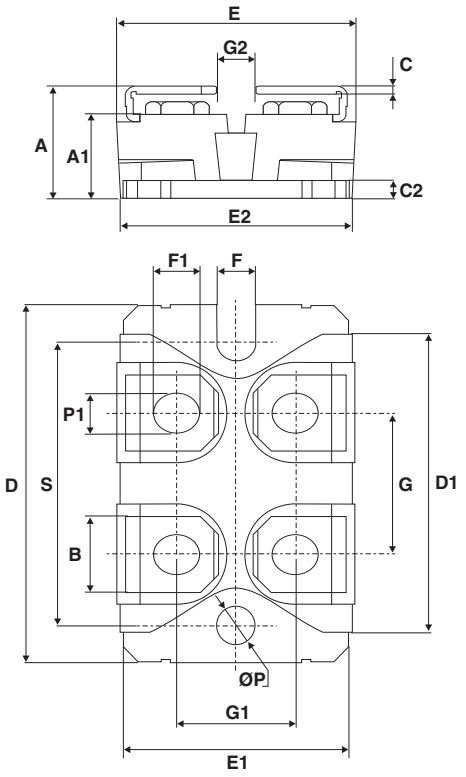


2 Package information

Epoxy meets UL94, V0

Cooling method: by conduction (C)

Table 5. ISOTOP dimensions



REF.	DIMENSIONS			
	Millimeters		Inches	
	Min.	Max	Min.	Max.
A	11.80	12.20	0.465	0.480
A1	8.90	9.10	0.350	0.358
B	7.8	8.20	0.307	0.323
C	0.75	0.85	0.030	0.033
C2	1.95	2.05	0.077	0.081
D	37.80	38.20	1.488	1.504
D1	31.50	31.70	1.240	1.248
E	25.15	25.50	0.990	1.004
E1	23.85	24.15	0.939	0.951
E2	24.80 typ.		0.976 typ.	
G	14.90	15.10	0.587	0.594
G1	12.60	12.80	0.496	0.504
G2	3.50	4.30	0.138	0.169
F	4.10	4.30	0.161	0.169
F1	4.60	5.00	0.181	0.197
P	4.00	4.30	0.157	0.69
P1	4.00	4.40	0.157	0.173
S	30.10	30.30	1.185	1.193

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com.

3 Ordering information

Part Number	Marking	Package	Weight	Base qty	Delivery mode
STTH9012TV1	STTH9012TV1	ISOTOP	27 g	10	Tube
STTH9012TV2	STTH9012TV2	ISOTOP	27 g	10	Tube

4 Revision history

Date	Revision	Description of Changes
02-Mar-2006	1	First issue.

Type 932 Polypropylene Film Capacitors

Metallized Axial Leads

High Voltage/High Frequency Switching Power Supplies

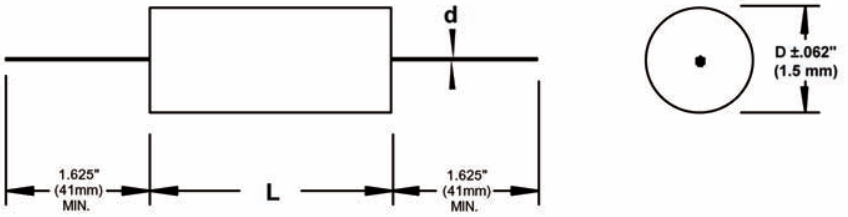
Type 932 axial-leaded, metallized polypropylene capacitors are available in a wide range of capacitance values in reduced sizes. Flame-retardant tape wrap and epoxy end seals provide moisture resistance. Used most frequently in high-voltage/high-frequency switching power supplies where superior stability and AC performance characteristics are important.

Specifications

Voltage Range:	250—700 Vdc (160-400 Vac, 60 Hz)
Capacitance Range:	1.0—30.0 µF
Capacitance Tolerance:	±5% (J) standard ±10% (K) optional
Operating Temperature Range:	–55 ºC to 105 ºC* *Full-rated voltage at 85 °C–Derate linearly to 50%-rated voltage at 105 °C
Dielectric Strength:	200% (1 minute)
Dissipation Factor:	.10% Max. (25 ºC, 1kHz)
Insulation Resistance:	200,000 M. x µF 400,000 M. Min.
Life Test:	1,000 Hours at 85 ºC at 125% Rated Voltage

RoHS Compliant

Complies with the EU Directive 2002/95/EC requirement restricting the use of Lead (Pb), Mercury (Hg), Cadmium (Cd), Hexavalent chromium (Cr(VI)), PolyBrominated Biphenyls (PBB) and PolyBrominated Diphenyl Ethers (PBDE).



Ratings

Cap. (µF)	Catalog Part Number	D ±.062(1.5) Inches(mm)		L +.062(1.5) Inches(mm)		d Inches(mm)		Typical ESR @100 KHz milliohms	dV/dt V/µs	I peak A	I_{RMS} 70 ºC 100 kHz (A)
250 Vdc(160 Vac)											
1	932C2W1J–F	0.433	11.0	0.748	19.0	.040	1.0	2.7	90	90	5
1.5	932C2W1P5J–F	0.394	10.0	1.220	31.0	.040	1.0	5.4	50	75	7
2.2	932C2W2P2J–F	0.453	11.5	1.220	31.0	.040	1.0	3.7	50	110	9
2.5	932C2W2P5J–F	0.472	12.0	1.220	31.0	.040	1.0	3.3	50	125	9
3	932C2W3J–F	0.531	13.5	1.220	31.0	.040	1.0	2.9	50	150	9
5	932C2W5J–F	0.669	17.0	1.220	31.0	.040	1.0	2.1	50	250	9
6.8	932C2W6P8J–F	0.787	20.0	1.220	31.0	.040	1.0	1.8	50	340	9
10	932C2W10J–F	0.787	20.0	1.654	42.0	.040	1.0	2.1	30	300	9
15	932C2W15J–F	0.965	24.5	1.654	42.0	.051	1.3	1.6	30	450	11
20	932C2W20J–F	1.102	28.0	1.654	42.0	.051	1.3	1.5	30	600	11
25	932C2W25J–F	1.240	31.5	1.654	42.0	.051	1.3	1.5	30	750	11
30	932C2W30J–F	1.161	29.5	2.165	55.0	.051	1.3	2.6	20	600	11
400 Vdc (250 Vac)											
0.68	932C4P68J–F	0.394	10.0	1.220	31.0	.040	1.0	7.4	70	48	6
1.00	932C4W1J–F	0.472	12.0	1.220	31.0	.040	1.0	5.1	70	70	8

Type 932 Polypropylene Film Capacitors

Cap. (µF)	Catalog Part Number	D ±.062(1.5) Inches(mm)		L +.062(1.5) Inches(mm)		d Inches(mm)		Typical ESR @100 KHz milliohms	dV/dt V/µs	I peak A	I_{RMS} 70 °C 100 kHz (A)
400 Vdc (250)											
1.50	932C4W1P5J–F	0.571	14.5	1.220	31	.040	1.0	3.6	70	105	9
2.00	932C4W2J–F	0.650	16.5	1.220	31	.040	1.0	2.9	70	140	9
2.20	932C4W2P2J–F	0.689	17.5	1.220	31	.040	1.0	2.8	70	155	9
2.50	932C4W2P5J–F	0.728	18.5	1.220	31	.040	1.0	2.5	70	175	9
3.00	932C4W3J–F	0.787	20.0	1.220	31	.040	1.0	2.3	70	210	9
4.00	932C4W4J–F	0.768	19.5	1.654	42	.040	1.0	3	50	200	9
4.70	932C4W4P7J–F	0.827	21.0	1.654	42	.040	1.0	2.7	50	235	9
5.00	932C4W5J–F	0.846	21.5	1.654	42	.040	1.0	2.6	50	250	9
6.80	932C4W6P8J–F	0.984	25.0	1.654	42	.051	1.0	2.1	50	340	11
10.00	932C4W10J–F	1.181	30.0	1.654	42	.051	1.3	1.8	50	500	11
15.00	932C4W15J–F	1.260	32.0	2.165	55	.051	1.3	3.1	30	450	11
600 Vdc (330 Vac)											
1.00	932C6W1J–F	0.61	15.5	1.220	31	.040	1.0	4.2	100	100	9
2.00	932C6W2J–F	0.728	18.5	1.654	42	.040	1.0	4.1	75	150	9
2.20	932C6W2P2J–F	0.768	19.5	1.654	42	.040	1.0	3.9	75	165	9
3.00	932C6W3J–F	0.886	22.5	1.654	42	.051	1.3	3.1	75	225	9
4.70	932C6W4P7J–F	1.083	27.5	1.654	42	.051	1.3	2.3	75	350	11
5.00	932C6W5J–F	1.122	28.5	1.654	42	.051	1.3	2.2	75	375	11
6.80	932C6W6P8J–F	1.122	28.5	2.165	55	.051	1.3	4.5	50	340	11
10.00	932C6W10J–F	1.358	34.5	2.165	55	.051	1.3	3.5	50	500	11
700 Vdc (400Vac)											
0.68	932C7P68J–F	0.669	17.0	1.220	31	.040	1.0	4.6	125	85	9
1.00	932C7W1J–F	0.807	20.5	1.220	31	.040	1.0	3.4	125	125	9
1.50	932C7W1P5J–F	0.807	20.5	1.654	42	.040	1.0	4.2	90	135	9
2.00	932C7W2J–F	0.925	23.5	1.654	42	.051	1.3	3.3	90	180	11
2.20	932C7W2P2J–F	0.965	24.5	1.654	42	.051	1.3	3.1	90	200	11
3.00	932C7W3J–F	1.122	28.5	1.654	42	.051	1.3	2.6	90	270	11
4.00	932C7W4J–F	1.299	33.0	1.654	42	.051	1.3	2.2	90	360	11
4.70	932C7W4P7J–F	1.181	30.0	2.165	55	.051	1.3	5.2	60	280	11
5.00	932C7W5J–F	1.201	30.5	2.165	55	.051	1.3	4.9	60	300	11

Type 940C through 943C Power Film Capacitors

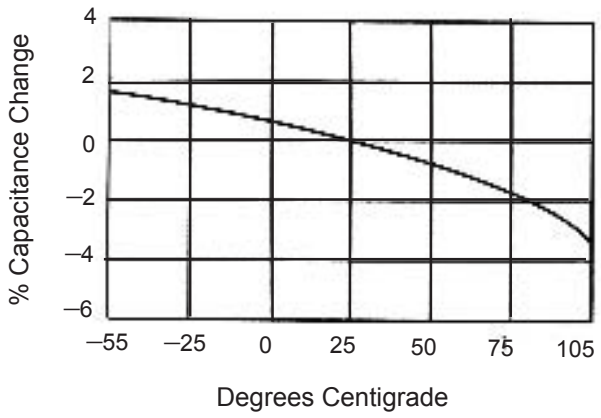
Electrical Characteristics

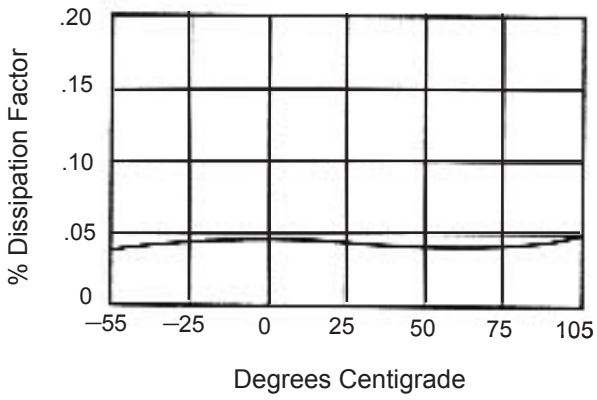
Operating Temperature	–55 ºC to +105 ºC *Full rated voltage at 85 ºC, derate linearly to 50% rated voltage at 105 ºC
Capacitance tolerance	±10% standard tolerance
Dissipation Factor	<0.1% at 1 kHz, 25 ºC
Dielectric Withstand	1.6 x rated voltage for 60 seconds
Insulation Resistance	>100,000 MΩ x µF at 100 Vdc measured after 2 minutes
Equivalent Series Resistance (ESR)	See rating tables for values
Equivalent Series Inductance (ESL)	See rating tables for values
dV/dt	See rating tables for values
Rated Current, I_{pk} and I_{rms} Maximum allowable current in amperes at 70 ºC	See rating tables for values
Capacitance Temperature Coefficient	–200 ppm/ºC ±100 ppm
Service Life	30,000 hours @ rated Vac, 70 ºC 60,000 hours @ rated Vdc, 70 ºC

Accelerated Tests

Accelerated Life	1.25 x rated DC voltage at 85 ºC for 2,000 hours
Performance	<3% capacitance change ESR <125% of initial reading IR >50% of initial limit
Accelerated Pulse Testing	per IEC-384
Performance	<3% in capacitance change <.003 increase in DF from initial value

Typical Characteristics

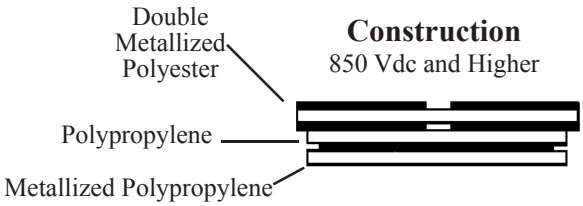




Type 940C High dV/dt, Round Polypropylene Film Capacitors

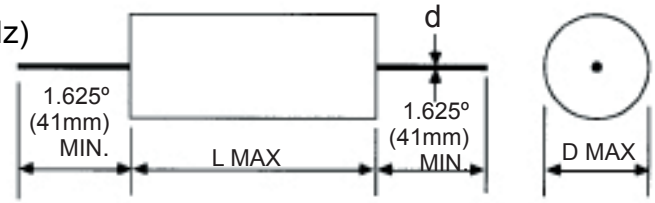
Double Metallized – Axial Leads

Type 940C round, axial leaded film capacitors have polypropylene film and dual metallized electrodes for both self healing properties and high peak current carrying capability (dV/dt). This series features low ESR characteristics, excellent high frequency and high voltage capabilities.



Specifications

Voltage Range: 600 – 3000 Vdc (275 - 750 Vac, 60 Hz)
Capacitance Range: 0.01 – 4.7 µF
Capacitance Tolerance: ±10%
Operating Temperature Range: –55 °C to 105 °C*
*Full-rated voltage at 85 °C–Derate linearly to 50%-rated voltage at 105 °C



NOTE: Refer to Application Guide for test conditions. Contact us for other capacitance values, sizes and performance specifications.

RoHS Compliant

Complies with the EU Directive 2002/95/EC requirement restricting the use of Lead (Pb), Mercury (Hg), Cadmium (Cd), Hexavalent chromium (Cr(VI)), PolyBrominated Biphenyls (PBB) and PolyBrominated Diphenyl Ethers (PBDE).

Ratings

Cap. (µF)	Catalog Part Number	D Inches	D (mm)	L Inches	L (mm)	d Inches	d (mm)	Typical ESR (mΩ)	Typical ESL (nH)	dV/dt V/µs	I peak (A)	I_{RMS} 70 °C 100 kHz (A)
600 Vdc (275 Vac)												
.10	940C6P1K-F	.354	(9.0)	1.339	(34.0)	.032	(.8)	28	19	196	20	2.5
.15	940C6P15K-F	.413	(10.5)	1.339	(34.0)	.032	(.8)	13	20	196	29	4.0
.22	940C6P22K-F	.453	(11.5)	1.339	(34.0)	.032	(.8)	12	20	196	43	4.4
.33	940C6P33K-F	.531	(13.5)	1.339	(34.0)	.032	(.8)	9	21	196	65	5.6
.47	940C6P47K-F	.610	(15.5)	1.339	(34.0)	.040	(1.0)	7	22	196	92	6.9
.68	940C6P68K-F	.709	(18.0)	1.339	(34.0)	.040	(1.0)	6	23	196	134	8.1
1.00	940C6W1K-F	.827	(21.0)	1.339	(34.0)	.040	(1.0)	6	24	196	196	8.9
1.50	940C6W1P5K-F	.984	(25.0)	1.339	(34.0)	.047	(1.2)	5	26	196	295	10.9
2.00	940C6W2K-F	.925	(23.5)	1.811	(46.0)	.047	(1.2)	5	31	128	255	11.8
3.30	940C6W3P3K-F	1.063	(27.0)	2.126	(54.0)	.047	(1.2)	4	36	105	346	15.3
4.70	940C6W4P7K-F	1.240	(31.5)	2.126	(54.0)	.047	(1.2)	4	38	105	492	16.8
850 Vdc (450 Vac)												
.15	940C8P15K-F	.512	(13.0)	1.339	(34.0)	.032	(.8)	8	21	713	107	5.8
.22	940C8P22K-F	.610	(15.5)	1.339	(34.0)	.040	(1.0)	8	22	713	157	6.4
.33	940C8P33K-F	.709	(18.0)	1.339	(34.0)	.040	(1.0)	7	23	713	235	7.5
.47	940C8P47K-F	.827	(21.0)	1.339	(34.0)	.040	(1.0)	5	24	713	335	9.8
.68	940C8P68K-F	.965	(24.5)	1.339	(34.0)	.047	(1.2)	4	26	713	485	12.0
1.00	940C8W1K-F	.886	(22.5)	1.811	(46.0)	.047	(1.2)	5	30	400	400	11.5
1.50	940C8W1P5K-F	1.063	(27.0)	1.811	(46.0)	.047	(1.2)	4	32	400	600	14.3
2.00	940C8W2K-F	1.201	(30.5)	1.811	(46.0)	.047	(1.2)	3	34	400	800	17.9
2.20	940C8W2P2K-F	1.260	(32.0)	1.811	(46.0)	.047	(1.2)	3	34	400	880	18.4
2.50	940C8W2P5K-F	1.339	(34.0)	1.811	(46.0)	.047	(1.2)	3	35	400	1000	19.1

Type 940C High dV/dt, Round Polypropylene Film Capacitors

Ratings

Cap. (µF)	Catalog Part Number	D Inches	(mm)	L Inches	(mm)	d Inches	(mm)	Typical ESR (mΩ)	Typical ESL (nH)	dV/dt V/µs	I peak (A)	I_{RMS} 70 ºC 100 kHz (A)
1000 Vdc (500 Vac)												
.15	940C10P15K-F	.591	(15.0)	1.339	(34.0)	.040	(1.0)	7	22	856	128	6.7
.22	940C10P22K-F	.689	(17.5)	1.339	(34.0)	.040	(1.0)	7	23	856	188	7.4
.33	940C10P33K-F	.807	(20.5)	1.339	(34.0)	.040	(1.0)	6	24	856	283	8.8
.47	940C10P47K-F	.945	(24.0)	1.339	(34.0)	.047	(1.2)	5	26	856	402	10.6
.68	940C10P68K-F	1.102	(28.0)	1.339	(34.0)	.047	(1.2)	5	27	856	582	11.7
1.00	940C10W1K-F	1.024	(26.0)	1.811	(46.0)	.047	(1.2)	5	32	480	480	12.5
1.50	940C10W1P5K-F	1.220	(31.0)	1.811	(46.0)	.047	(1.2)	4	34	480	720	15.6
2.00	940C10W2K-F	1.398	(35.5)	1.811	(46.0)	.047	(1.2)	3	36	480	960	19.6
1200 Vdc (500 Vac)												
.10	940C12P1K-F	.610	(15.5)	1.339	(34.0)	.040	(1.0)	9	22	1142	114	6.1
.15	940C12P15K-F	.728	(18.5)	1.339	(34.0)	.040	(1.0)	7	23	1142	171	7.6
.22	940C12P22K-F	.846	(21.5)	1.339	(34.0)	.040	(1.0)	7	24	1142	251	8.4
.33	940C12P33K-F	.787	(20.0)	1.811	(46.0)	.040	(1.0)	7	29	640	211	9.0
.47	940C12P47K-F	.906	(23.0)	1.811	(46.0)	.047	(1.2)	7	30	640	301	9.8
.68	940C12P68K-F	1.063	(27.0)	1.811	(46.0)	.047	(1.2)	6	32	640	435	11.7
1.00	940C12W1K-F	1.299	(33.0)	1.811	(46.0)	.047	(1.2)	5	35	640	640	14.5
1.50	940C12W1P5K-F	1.378	(35.0)	2.126	(54.0)	.047	(1.2)	4	39	502	754	17.9
1600 Vdc (630 Vac)												
.10	940C16P1K-F	.709	(18.0)	1.339	(34.0)	.040	(1.0)	7	23	1427	143	7.5
.15	940C16P15K-F	.846	(21.5)	1.339	(34.0)	.040	(1.0)	5	24	1427	214	9.9
.22	940C16P22K-F	1.004	(25.5)	1.339	(34.0)	.047	(1.2)	7	26	1427	314	9.3
.33	940C16P33K-F	.925	(23.5)	1.811	(46.0)	.047	(1.2)	7	31	800	264	10.0
.47	940C16P47K-F	1.083	(27.5)	1.811	(46.0)	.047	(1.2)	6	32	800	376	11.8
.68	940C16P68K-F	1.280	(32.5)	1.811	(46.0)	.047	(1.2)	6	35	800	544	13.1
1.00	940C16W1K-F	1.535	(39.0)	1.811	(46.0)	.047	(1.2)	5	37	800	800	16.2
1.50	940C16W1P5K-F	1.654	(42.0)	2.126	(54.0)	.047	(1.2)	4	42	628	942	20.1
2000 Vdc (630 Vac)												
.022	940C20S22K-F	.453	(11.5)	1.339	(34.0)	.032	(.8)	35	6	1712	38	2.6
.033	940C20S33K-F	.531	(13.5)	1.339	(34.0)	.032	(.8)	20	21	1712	57	3.8
.047	940C20S47K-F	.591	(15.0)	1.339	(34.0)	.040	(1.0)	12	22	1712	80	5.2
.068	940C20S68K-F	.689	(17.5)	1.339	(34.0)	.040	(1.0)	8	23	1712	116	6.9
.100	940C20P1K-F	.827	(21.0)	1.339	(34.0)	.040	(1.0)	7	24	1712	171	8.3
.150	940C20P15K-F	.768	(19.5)	1.811	(46.0)	.040	(1.0)	7	29	960	144	8.9
.220	940C20P22K-F	.866	(22.0)	1.811	(46.0)	.040	(1.0)	8	30	960	211	9.0
.330	940C20P33K-F	1.063	(27.0)	1.811	(46.0)	.047	(1.2)	8	32	960	317	10.1
.470	940C20P47K-F	1.260	(32.0)	1.811	(46.0)	.047	(1.2)	6	34	960	451	13.0
.560	940C20P56K-F	1.220	(31.0)	2.126	(54.0)	.047	(1.2)	7	37	754	422	12.6
.680	940C20P68K-F	1.339	(34.0)	2.126	(54.0)	.047	(1.2)	6	39	754	513	14.3
1.00	940C20W1K-F	1.614	(41.0)	2.126	(54.0)	.047	(1.2)	5	42	754	754	17.7
3000 Vdc (750 Vac)												
.010	940C30S1K-F	0.453	(11.5)	1.339	(34.0)	.032	(.8)	60	20	2568	26	2.0
.015	940C30S15K-F	0.531	(13.5)	1.339	(34.0)	.032	(.8)	40	21	2568	39	2.7
.022	940C30S22K-F	0.61	(15.5)	1.339	(34.0)	.040	(1.0)	25	22	2568	57	3.6
.033	940C30S33K-F	0.709	(18.0)	1.339	(34.0)	.040	(1.0)	14	23	2568	85	5.3
.047	940C30S47K-F	0.65	(16.5)	1.811	(46.0)	.040	(1.0)	14	28	1440	68	5.7
.068	940C30S68K-F	0.748	(19.0)	1.811	(46.0)	.040	(1.0)	12	29	1440	98	6.7
.100	940C30P1K-F	0.886	(22.5)	1.811	(46.0)	.047	(1.2)	10	30	1440	144	8.1
.150	940C30P15K-F	1.063	(27.0)	1.811	(46.0)	.047	(1.2)	8	32	1440	216	10.1

Appendix B

Matlab Files

Solve_SEPIC_TF_Symbolic.m

```
% Title: Solve_SEPIC_TF_Symbolic
% Description: Solve TF for the SEPIC converter with the symbolic math
% toolbox
%
% Autor: Julia Delos Ayllon
% Mail:  jdelos.etsetb@gmail.com
%



tic %Start timer
clear %Clear Workspace
syms v1 v2 i1 i2 C1 C2 L1 L2 D Dp E e d R s  %Define the Symbolic variables

%Symbolic variables definition:
  % Small Signla Variables:
    % v1 => C1 voltage
    % v2 => C2 voltage
    % i1 => L1 current
    % i2 => L2 current
    % e  => Vin
    % d  => duty cycle
  % Steady State Varaibles
    % D => duty cycle
    % E => input voltage
  % Parameters
    % C1, C2 => Capacitors
    % L1, L2 => Inductors
    % R => Load


%Matrix represetnation of the state equations
% 0 = A * x + B
% Where:
    % x => state variables vector
    % A => state variables constants
```

```
    % B => independent vaiables

x = [v1; v2; i1; i2];
A = [-s*C1 0 Dp -D;  0 -(s*C2+1/R) 0 -1; -Dp 0 -s*L1 0; D 1 0 -s*L2 ];
B = [-(E/R*D/Dp^2)*d;  0;  e + d*E/Dp; +d*E/Dp];

StateEq= A * x + B;

%Solve the system for the control transfer functions
%Hence we have H(s)= state_var/d ,when e=0
StateCtr = subs(StateEq,[e d],[0 1]);

Hcrt_cuk = solve(StateCtr,v1,v2,i1,i2); %Solve the system
Gcrt_cuk = collect(Hcrt_cuk.v2,'s'); %Isolate the TF control-to-output
pretty(Gcrt_cuk)

%Solve the system for the input to output transfer functions
%hence we have H(s)= state_var/e ,when d=0
StateOut = subs(StateEq,[e d],[1 0]);
Hout_cuk = solve(StateOut,v1,v2,i1,i2); %Solve the system
Gout_cuk = collect(Hout_cuk.v2,'s'); %Isolate the TF input-to-output
pretty(Gout_cuk)

toc
```

Solve_Cuk_TF_Symbolic.m

```
% Title: Solve_Cuk_TF_Symbolic
% Description: Solve TF for the Cúk converter with the symbolic math
% toolbox
%
% Autor: Julia Delos Ayllon
% Mail:  jdelos.etsetb@gmail.com
%
```

```
tic %Start timer
clear %Clear Workspace
syms v1 v2 i1 i2 C1 C2 L1 L2 D Dp E e d R s  %Define the Symbolic variables

%Symbolic variables definition:
  % Small Signla Variables:
    % v1 => C1 voltage
    % v2 => C2 voltage
    % i1 => L1 current
    % i2 => L2 current
    % e  => Vin
    % d  => duty cycle
  % Steady State Varaibles
    % D => duty cycle
    % E => input voltage
  % Parameters
    % C1, C2 => Capacitors
    % L1, L2 => Inductors
    % R => Load


%Matrix represetnation of the state equations
% 0 = A * x + B
% Where:
    % x => state variables vector
    % A => state variables constants
    % B => independent vaiables

x = [v1; v2; i1; i2];
A = [-s*C1 0 Dp -D;  0 -(s*C2+1/R) 0 -1; -Dp 0 -s*L1 0; D 1 0 -s*L2 ];
B = [-(E/R*D/Dp^2)*d;  0;  e + d*E/Dp; +d*E/Dp];

StateEq= A * x + B;

%Solve the system for the control transfer functions
%Hence we have H(s)= state_var/d ,when e=0
StateCtr = subs(StateEq,[e d],[0 1]);
```

```
Hcrt_cuk = solve(StateCtr,v1,v2,i1,i2); %Solve the system
Gcrt_cuk = collect(Hcrt_cuk.v2,'s'); %Isolate the TF control-to-output
pretty(Gcrt_cuk)

%Solve the system for the input to output transfer functions
%hence we have H(s)= state_var/e ,when d=0
StateOut = subs(StateEq,[e d],[1 0]);
Hout_cuk = solve(StateOut,v1,v2,i1,i2); %Solve the system
Gout_cuk = collect(Hout_cuk.v2,'s'); %Isolate the TF input-to-output
pretty(Gout_cuk)

toc
```

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