MASTER THESIS

TITLE OF THE THESIS : Development and Characterization of Subsystems for a 2.45 GHz RFID Research Environment

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Resumen

Actualmente, la tecnología de identificación por radio frecuencia (RFID del inglés Radio Frequency IDentification) es una tecnología emergente y en vías de desarrollo con un amplio rango de aplicaciones en diferentes campos. Debido al progreso tecnológico, el número de aplicaciones ha aumentado enormemente, llevando al desarrollo de una gran cantidad de estandares en diferentes bandas frecuenciales para soportar cada una de las aplicaciones.

La mayoría de estos estandares no son compatibles entre ellos y además, no existe un único estándar UHF alrededor de todo el mundo. Por esa razón una posible solución para alcanzar un sistema RFID compatible mundialmente es por medio de la banda de microondas ISM en la frecuencia de 2.45 GHz. Cada vez más, esta banda de RFID a 2.45 GHz está tomando más fuerza y actualmente ya hay sistemas funcionando en esa frecuencia.

Esta tesis describe el diseño e implementación de un frontend para un testbed RFID en la frecuencia de 2.45 GHz. En el documento, los fundamentos básicos más relevantes de RFID y las regulaciones asumidas son descritas. El concepto del sistema diseñado es explicado y algunos elementos importantes son seleccionados para comprobar su funcionamiento y optimizarlos. Se describe el desarrollo del transmisor y del receptor y finalmente para ambos dispositivos se muestran las medidas de su caracterización.

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Overview

Nowadays, the Radio Frequency IDentification (RFID) technology is a very fast emerging and developing technology with a wide range of applications in different fields. Due to the technological progress, the number of applications has increased enormously, leading to the creation of many different standards in several distinct frequency bands for supporting these applications.

The majority of this standards are not compatible with each other and moreover, there is not an unique UHF band standard worldwide. For this reason, a possible solution to achieve a compatible RFID system around the world is by means of the 2.45 GHz microwave ISM band. More and more this 2.45 GHz RFID band is considered and currently there are systems working at this frequency.

This thesis describes the design and the implementation of a frontend for a 2.45 GHz RFID testbed. Inside the document, relevant RFID basics and the assumed regulations are discussed. The system concept designed is explained and selected elements are tested and optimized. The development of the transmitter and receiver board is described and finally for both boards the characterization and the measurements results are shown.

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CHAPTER 1. INTRODUCTION

Throughout history, there has been a very important need to identify "things". Once identified, it is possible to sort, classify, arrange, order, transport, ship and find specific objects. It is executed for personal use or for commercial or governmental aim. But it was not until two decades ago, with the appearance of the bar code, the identification of objects was made from human eye in our society.

Currently, our society lives in a world in which communication between people and at businesses is very important. Communications can be carried out in many different ways and the amount of the available information in our society is immense.

Nowadays, the information accompanied by time is "the fuel" of our economy and it is possible to use it to enrich ourselves, to make us stronger compared to our competitors or to differentiate ourselves from them. In order to promote this "fuel", in recent years automatic identification procedures have become very popular and new technologies have been applied trying to make laborious task as sorting, ordering, transporting, searching, identifying items simple and to provide information about people, animals, goods and products in a easy and fast way.

RFID[1] is one of the fastest growing and most beneficial automatic identification technology which identifies items easily and fastly by means of radio frequency technology. Therefore, it is an alternative solution to current conventional automatic identification systems like bar codes or OCR[2].

By its very nature, RFID is a technology that began with the pioneers of radio and electromagnetic theory, James Clerk Maxwell, Michael Faraday and Guglielmo Marconi. In the applications fields, the idea of using reflected radio waves, was developed in 1922 with the RADAR[3]. However, it was in the World War II when a principle similar to RFID was used by the military to identify aircraft as friend or foe, IFF[4]. Therefore, it is possible to say that the RFID has existed since the 1960s for the military.
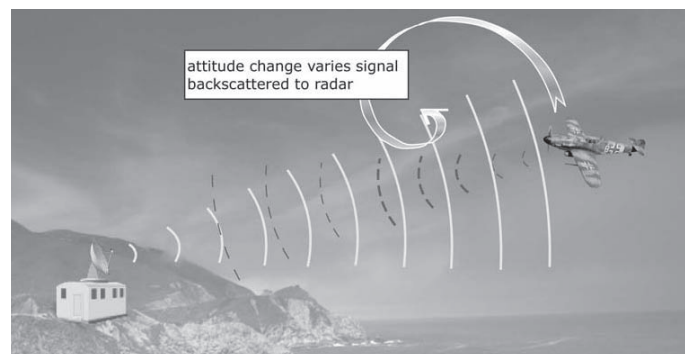
Figure 1.1: Use of backscattered radiation to identify friend or foe in the World War II. Source [1]

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[1]Radio Frequency IDentification
[2]Optical Character Recognition
[3]RAdio Detection And Ranging
[4]Identify Friend or Foe. This principle is illustrated in Figure 1.1

Nowadays, a great range of applications in which this technology is usable like medical, telemetry, low-cost sensors, remote switches, position location and tracking devices, and passive data exchange, to name just a few, makes RFID an interesting technology. There are already developed systems in low frequency, high frequency and ultra high frequency ISM[5] bands. Nevertheless, still there is a technological gap at the 2.45 GHz microwave band. For this reason, this thesis presents a systems for a 2.45 GHz RFID research environment developed at the Institute of Communications and Radio-Frequency Engineering at the Vienna University of Technology for experimental research in RFID at this frequency band.

1.1. RFID system

An RFID system is composed by two elements (see Figure 1.2):

- A transponder or tag, which is located on the object to be identified.

- A reader or interrogator, which main task is to communicate and read the identification number from one or more tags.
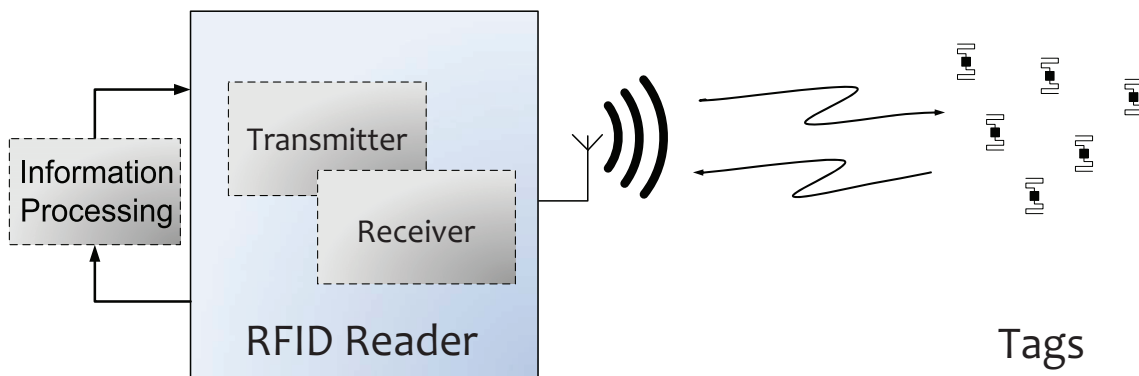
Figure 1.2: Structure of a common RFID system

The reader consist of: A control unit where the information is processed, a radio frequency module (transmitter and receiver) and an antenna [4]. The communication between reader and tag is performed wireless. The transmitted data is subject to the influences of the channel, the air interface and the internal reader components like, amplifiers, filters, mixers, etc. With that, the transmitted power in both the transmitter and the tag are the main distance limitation because the strength of this power is reduced respect to the distance (Inverse proportion to the square of the distance).

Depending on the nominal reader frequency, the protocol used to communicate between the tag and the reader, and the provided power to the tag, it is possible to distinguish different RFID systems. Table 1.1 summarizes some of the common frequencies used, their comunication ranges and some available standards.

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[5]Industrial, Scientific and Medical band

Table 1.1: Frequency characteristics of RFID systems [3]

Frequency range	135 kHz (LF[6])	13.56 MHz (HF[7])	860 MHz (UHF[8])	2.45 GHz (MW[9])
Typ.read range	$\leq$0.5 m	~1 m	~4 − 5 m	~1 m
Passive tag size	Larger	$\longrightarrow$	$\longrightarrow$	Smaller
Relevant standard	ISO 18000-2	ISO 18000-3	ISO 18000-6	ISO 18000-4

A different way to distinguish and classify the RFID system is by the tag. There are three types:

- Active tags

- Passive tags

- Semi-passive tags

Active tags are equipped with a battery unit which allows to have the longest communication range and the largest memory between the different kind of tags. As a disadvantage, the batteries make the tag bulky and limit the tag lifetime.

Passive tags do not have their own DC[10] power supply. However, the tiny electrical current induced in the antenna by the incoming RF signal provides enough power for the transponder to send a response. This kind of tags use the backscatter technology explained in Section 1.2. As disadvantage, these transponders do not support complex functions.

Semi-passive tags are a mix between the previous tags. This kind of tags use the backscatter technology to transmit the signal. However, the internal circuit is supplied by batteries. This combination allows active tag functionality as supporting complex functions and enhances the battery lifetime.

1.2.   Backscattering technology

The backscattering technique is applied in passive RFID systems like shown in Figure 1.3. This systems are composed by an RFID reader and a passive tag. The reader, on the left, is divided into the transmitter and the receiver. On the right, a passive tag consisting of an antenna and the RFIC[11] which require a minimum RF power to power up the internal circuits.

In these systems, the communication between the reader and the tag is half duplex. First, a modulated carrier is transmitted by the reader looking for tags. If the tag is inside the reader

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[6]Low Frequency
[7]High Frequency
[8]Ultra High Frequency
[9]Microwave
[10]Direct Current
[11]Radio Frequency Integrated Circuit

interrogation range, the tag responses to the reader receiver. While the reader is waiting for the tag response, at the reader's transmitter, an unmodulated carrier is transmitted continuously to provide the power supply for the internal circuit of the tag. Therefore, the reader transmits a carrier at the same frequency while receives data from the tags. This causes that some of the transmitted carrier also leaks into the receiver. This leaking carrier problem is also called crosstalk and possible solutions are explained further in Section 2.2.2.
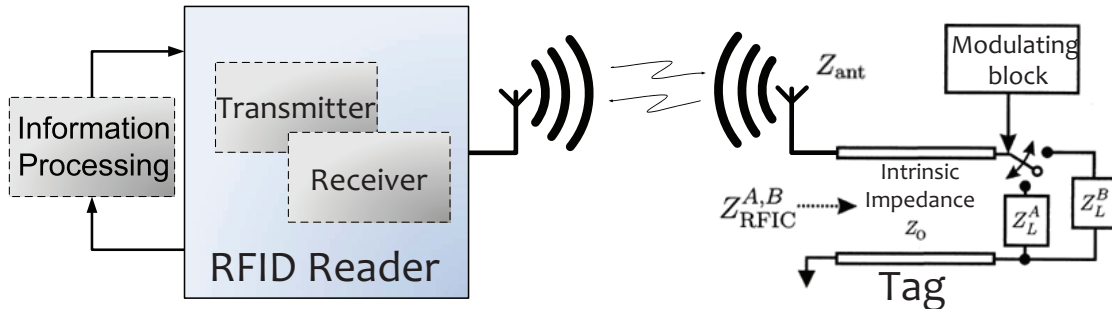
Figure 1.3: An overview of a typical passive RFID system

In these systems which one of the devices, the passive tag, has not a dedicated power supply available for the communication, the goal of the backscatter technique is to retrieve information from the tag by illuminating the device with power, and then decode the modulated portion of signal scattered back from the tag.

The RFIC inside the tag is responsible for the modulated backscattered signal which is generated switching the RFIC input impedance between two states Z_L^A and Z_L^B (see Figure 1.3) presenting a certain RCS[12] of the tag for each state.

The total backscattered power from the antenna is divided in two parts, the originated in the open-circuit antenna and the re-radiated field. Assuming an equivalent tag as in Figure 1.4, the re-radiated field is a variable part and can be obtained from the same figure. In the other side, an open circuit antenna, according with the same figure, re-radiates a continuous non interesting field for this thesis purpose. Therefore, assuming a minimum scattering antenna, antennas whose open-circuited backscattered part is zero, it is possible to calculate the radar cross section [2].
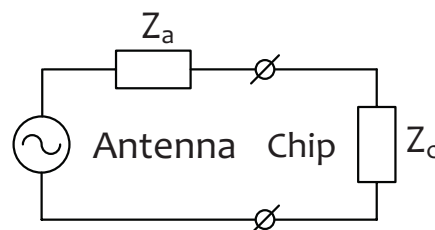
Figure 1.4: The equivalent circuit of an RFID tag [2]

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[12]Radar Cross Section

At an RFID tag, the power density of an electromagnetic wave S in free space is

$$S = \frac{P_{TX}G_{TX}}{4\pi r^2}.$$

(1.1)

Where: P_{TX} is the transmitted power

G_{TX} is the transmitter antenna gain

r is the distance to the tag

This power density at the tag's antenna is a power, P_a of

$$P_a = SA_e,$$

(1.2)

where A_e is the antenna effective area, given by

$$A_e = \frac{\lambda^2}{4\pi}G_{Tag}.$$

(1.3)

With: G_{Tag} the gain for the tag's antenna

λ the wavelength

Once the received power at the tag's antenna P_a is known by Equation 1.3, it is possible to calculate the reradiated power ,$P_{re-radiated}$, from the tag's antenna to the receiver in Equation 1.4.

$$P_{re-radiated} = KP_aG_{Tag},$$

(1.4)

K is a factor for different antenna load impedances given by [2]

$$K = \frac{4R_a^2}{|Z_a + Z_c|^2}.$$

(1.5)

Where: Z_a is the impedance of the antenna

Z_c is the impedance of the internal circuit of the tag

R_a is the real part of Z_a

Equation 1.5 gives the influence of the load-impedance mismatch on the amount of re-radiated power. Table 1.2 gives the values for some interesting results when the tag is short circuited, matched and open-circuited.

Table 1.2: The K factor for different antenna load impedances. [2]

Z_c	K	$P_{re-radiated}$
0	$\frac{4R_a^2}{R_a^2 + X_a^2}$	$4P_aG_{Tag}$
Z_a^*	1	P_aG_{Tag}
∞	0	0

For a minimum scattering antenna, the radar cross section of the RFID tag is given by Equation 1.6

$$\sigma = \frac{P_{re-radiated}}{S} = K\,A_e\,G_{Tag}.$$ (1.6)

By replacing A_e and K in Equation 1.6 by Equation 1.3 and Equation 1.5, Equation 1.7 for the radar cross section of the tag is obtained as

$$\sigma = \frac{\lambda^2 G_{Tag}^2 R_a^2}{\pi\,|Z_a + Z_c|^2}.$$ (1.7)

It is important to remember that this equation is valid for reader and tag antennas with matched polarizations and tag pointing toward the reader.

To finalize, Equation 1.7 which represents the different RFIC impedance states, gives a scalar difference value to detect the modulated backscattered signal. However, the power of the modulated backscattered signal received by the RFID reader depends not only on the scalar difference between radar cross-sections defined in Equation 1.7, but also on relative phases of the reflected field components. This relative phase is very useful to receive successfully the tag's message when two chip impedance states have the same scalar value, resulting nonzero modulated backscattered signal power [5] [2].

1.3.   Regulations

For a correct RFID system operation, readers and tags have to work using a compatible modulation, protocol, power and same frequency band. Otherwise it is impossible to achieve communication. For this reason RFID standards are required to achieve compatibility between RFID devices. There are many standards, nevertheless no standard is universally accepted for RFID at ultra high frequencies. In Figure 1.5 a map shows the different and incompatible frequency bands used in the main regions of the world.
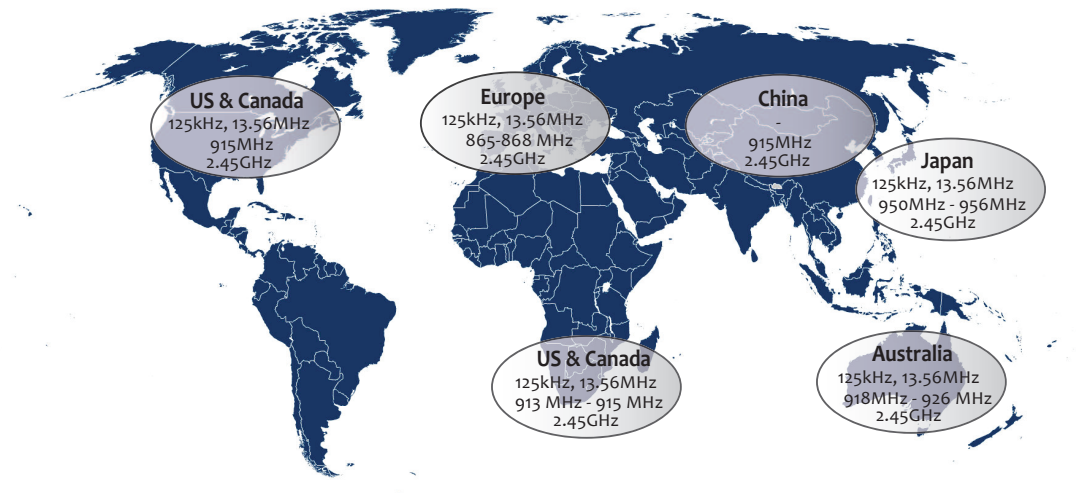
Figure 1.5: World wide frequency map. Data source: IBM business consulting service

Despite the different frequency bands employed in different parts of the world at the UHF band, there is a common frequency around the world which could be a solution for this frequency problem. The 2.45 GHz frequency at the microwave ISM band used in this thesis.

Therefore, the focus of this work is on European RFID systems operating in the 2.45 GHz ISM band, so only regulations regarding this band are discussed.

At this frequency band at 2.45 GHz, the ISO 18000 part 4[13] [6] defines the forward and return link parameters for technical attributes including, but not limited to, operating frequency, operating channel accuracy, occupied channel bandwidth, spurious emissions, modulation type, duty cycle, data coding, bit rate, etc. It further defines the communication protocol used in the air interface which is divided in two modes: Mode 1, passive backscatter RFID system, and mode 2, long range high data rate RFID system. In Table 1.3 the main difference between them are summarized.

Table 1.3: Mode 1 and mode 2 frequency band difference

	Mode 1	Mode 2
Channel bandwidth	0.5 MHz	819.2 kHz
Op. freq. channels	2446-2454 MHz	2400-2483.5 MHz
Number of channels	8	99

In terms of power, the local governments for each state defines their own regulation. However, many European countries have implemented the ERC RECOMMENDATION 70-03 [7]. At the frequency band of $2446 - 2454$ MHz defined for the mode 1, the maximum allowed EIRP[14] is 4 W for the indoor mode and 0.5 W for the outdoor mode.

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[13]For this thesis the used version of the ISO 18000-4 is the first edition of 2004-08-15.

[14]Equivalent Isotropically Radiated Power

CHAPTER 2. SYSTEM CONCEPT

This chapter presents an overview of the 2.45 GHz RFID system and describes the requirements for a possible integration with the already existing UHF system. The power level plan and the frequency plan are considered, in order to obtain a flexible system which allow to support current and future RFID regulations at this frequency band.

2.1. RFID testbed concept

Prior to this project, at the Institute of Communications and Radio-Frequency Engineering at the Vienna University of Technology, other RFID testbeds have already been developed [8] [9] [10]. These testbeds, in the HF and the UHF band, use as signal source a Rapid Prototyping Board.

As a platform for the Rapid Prototyping system it is used a Rapid Prototyping Board from the Austrian Research Centers [8] [10]. Figure 2.1 depicts the basic structure of the Rapid Prototyping Board [8]. The main reconfigurable components are a fixed-point DSP[1] from Texas Instruments (TMS320C6416) and a Xilinx Virtex II FPGA[2]. Additionally, it exhibits two digital to analog converters (16 bits) and two analog to digital converters (14 bits). The DSP is clocked with 600 MHz while the FPGA, DACs[3], and ADCs[4] are sourced by a single clock of 40 MHz. An Ethernet interface connects the DSP to a PC thus allowing for an external communication to an application running on a PC.
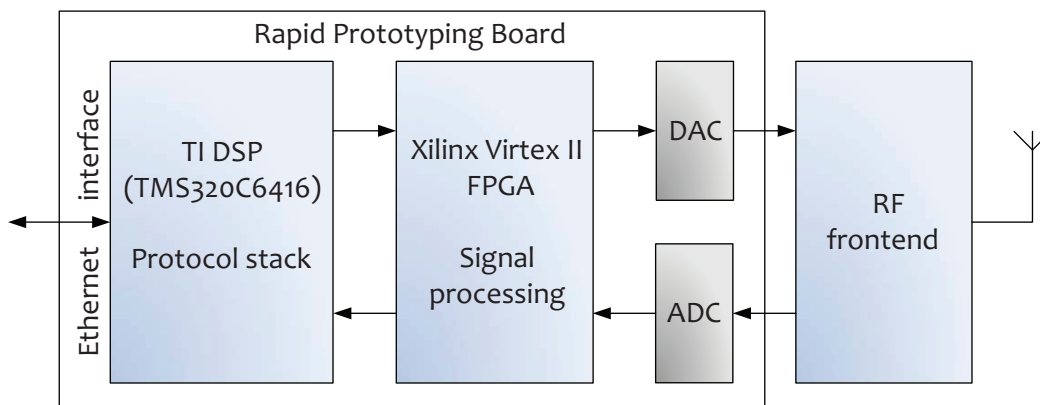
Figure 2.1: Block diagram of the Rapid Prototyping Board

The RF frontend is exchangeable and either supports the 13.56 MHz HF domain or the 868 MHz UHF domain already existing and this thesis presents the extension to the 2450 MHz ISM domain.

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[1]Digital Signal Procesors
[2]Field-Programmable Gate Array
[3]Digital to Analog Converter
[4]Analog to Digital Converter

2.1.1. The 2.45 GHz stage

The main idea of this project is to implement a new frontend for the 2.45 GHz band reusing parts of the UHF design, specially the IF[5] parts at the frequencies of 13.56 MHz and 140 MHz. This IF stage is then connected to the new 2.45 GHz stage through the "X2" interface, defined below. Figure 2.2 depicts the testbed concept employing the frontend at the frequency of 2.45 GHz.
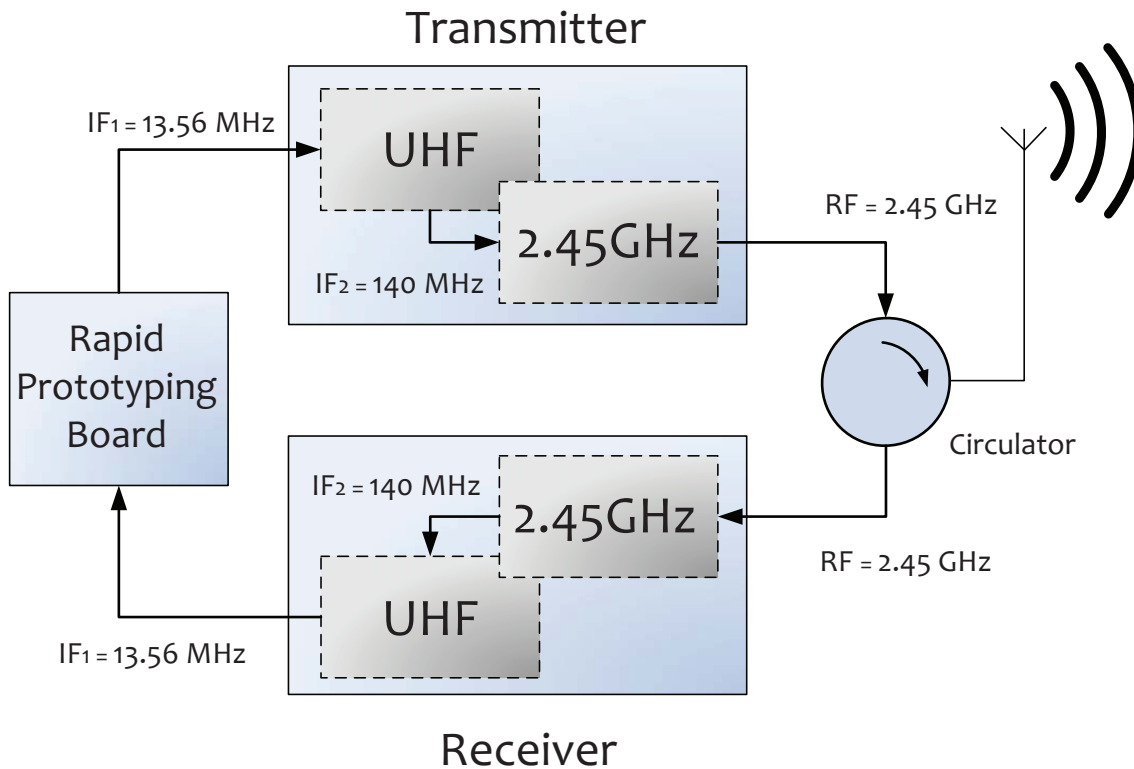
Figure 2.2: The 2.45 GHz testbed concept

The design criteria of the transmitter are shown on the upper part of Figure 2.2. The transmitter is fed by the Rapid Prototyping Board which generates a signal at the first IF, IF1[6]. This signal is directly synthesized at the 13.56 MHz carrier in the internal FPGA of the Rapid Prototyping Board. The modulated transmit sequence is transmitted to the DAC. Then, the signal is filtered, amplified and frequency upconverted using the double frequency conversion concept described in Section 2.3. Initially, the input signal at IF1, is amplified, filtered and upconverted to the IF2[7] reusing parts of the UHF design and then it is again amplified, filtered and upconverted to the desired frequency of 2.45 GHz.

The design criteria of the receiver are shown in the lower part of Figure 2.2. The input signal from the antenna is filtered, amplified and downconverted using the same double frequency conversion concept as at the transmitter. The receiver output is then directly connected to the ADC of the Rapid Prototyping Board.

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[5]Intermediate Frequency
[6]First Intermediate Frequency at the frequency of 13.56 MHz
[7]Second Intermediate Frequency at the frequency of 140 MHz

The frontend is divided into two blocks, transmitter and receiver, and it can be configured as a single antenna system as shown in Figure 2.2 or as dual antenna system. The selected scenario determines the transmitter to receiver isolation as described in Section 2.2.2. To increase the frontend flexibility, proper inputs and outputs are employed to add a CCU[8] module to improve the isolation between the two blocks. Others inputs and outputs are implemented allowing further extension to control and monitor the system externally and also to provide an external amplification by means of an external power amplifier. To achieve a flexible design which fits current regulations and possible future changes, this frontend is endowed with exchangeable band pass filters to adapt the frontend bandwidth and the frequency range since these are the only conceptual limitations for the frontends. In addition, to achieve a linear response while using at the same time different carriers, all filters are designed to obtain a flat frequency response and a linear phase response.

This thesis focus on the design of the final conversion stage from the IF2 to the RF in the transmitter and vice-versa in the receiver, keeping the compatibility with the already existing UHF testbed but also assuring flexibility in order to support future RFID regulations.

2.1.2. Common IF stage

The reuse of the IF part from the existing UHF board is possible because this design was created with an interface, called X2, that allows further extension. This interface is defined as:

- Input at the receiver board.

- Output at the transmitter board.

Figure 2.3 depicts the transmitter block diagram for the common IF stage and shows where the connection "X2" for further extension is located.
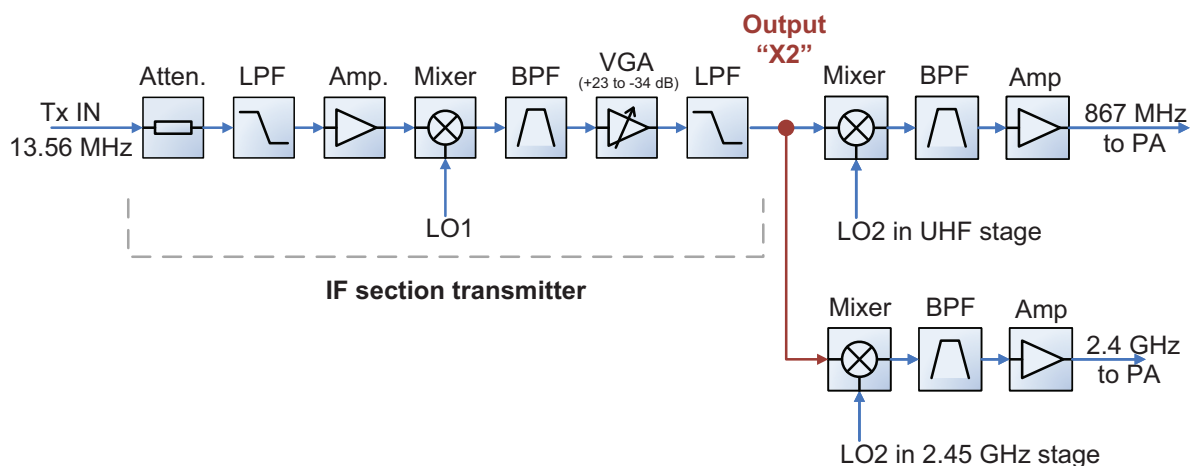
Figure 2.3: Transmitter extension to 2.45 GHz

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[8]Carrier Compensation Unit

The common IF section for the transmitter and the receiver is described in [9]. The 13.56 MHz, IF1 input signal from the Rapid Prototyping Board enters to the transmitter through a fixed attenuator. This provides some sort of enforced matching for the following low pass filter, and allows easy adaptation to higher signal level feeding. The low pass filter provides suppression of periodical spectrum produced by the DAC on the Rapid Prototyping Board. An amplifier compensates the losses in the previous stages and provides isolation between the low pass filter and the first mixer. This double balanced mixer, fed by the 153.56 MHz local oscillator, converts the first IF signal into the second IF at 140 MHz. At 140 MHz, the system overall bandwidth is fixed with a 5 MHz band pass filter and the upper sideband of the frequency conversion process is suppressed. This first frequency conversion and filtering up to here is further explained in Section 2.3. where the frequency plan continues with the 2.45 GHz stage. Then, the signal is fed into a variable gain amplifier that is used to set the desired transmit level of the transmitter. The output of this amplifier is low pass filtered and then fed into the 2.45 GHz stage by means of the "X2" output.

The receiver has a similar operation in which the signal is amplified and filtered with the only difference that in this case the RF input signal is downconverted and driven to the Rapid Prototyping Board.

Due to the processing of the signal along this section, it is necessary to know the power levels at the input and the output of each element in order to design the 2.45 GHz stage. For this reason, the input and output power level considerations and the frequency plan are described for this new stage.

2.2.   Power level considerations

To design the frontend it is necessary to know the required input power and the expected output power level of the Rapid Prototyping Board.
These power levels were measured and the results are available in [9, Sec. 2.2.1.]. In summary, the output of the Rapid Prototyping Board is:

- -3.1 dBm when operating as high frequency, HF testbed.

- 4 dBm when measuring the maximum output power.[9]

On the other hand, the maximum input power at the ADC of the Rapid Prototyping Board is 12.56 dBm.

Once the maximum output power of the Rapid Prototyping Board is known, it is possible to set the maximum input power of the frontend. Hence, the maximum input power allowed without using an external power amplifier[10] is:

- 2 dBm for linear operation of the transmitter.

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[9]Using a digital sawtooth signal of full height
[10]Further details about the power level plan in Section 5.2.

- 4 dBm for the absolute maximum input without damaging the transmitter.

Both, the power level of 2 dBm for linear operation and the power level of 4 dBm for the absolute maximum input are obtained from the power level plan described in Section 5.2. Therefore, as important as the frontend maximum input power and the maximum output power, are the maximum input power and the maximum output power for the 2.45 GHz stage. These levels are critical because they are conditioning the new stage design and also limiting the component selection to those that can withstand the design conditions.

Figure 2.4 indicates, using dots, the input and output power levels of interest for this new stage.
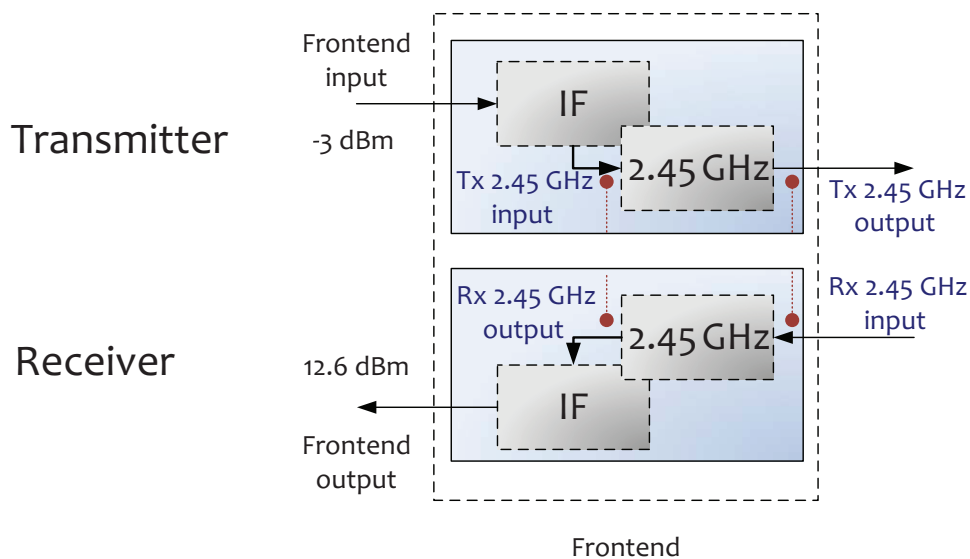
Figure 2.4: Inputs and outputs of the 2.45 GHz stage

For the 2.45 GHz transmitter module design, there are three main power considerations:

1. The input power level for the 2.45 GHz module is variable and depends on the first IF amplifier and the setting of the VGA[11], both placed in the IF section. See Figure 2.3.

2. Setting the previous devices to the maximum gain configuration, the maximum input power for the 2.45 GHz stage is 6.3 dBm when using the external power amplifier in linear mode. At higher input power than 6.3 dBm the external power amplifier is the first element to saturate in this maximum gain configuration. When the external power amplifier is omitted the maximum input power is 13.3 dBm.

3. The transmitter output level is defined by the local government regulation. Depending on the environment, the maximum allowed output power is 27 dBm (outdoor) or 36 dBm (indoor). This feature requires a flexible design which can get the maximum output power in both environments using the same maximum input power of 6.3 dBm generated when the IF stage works at the maximum gain settings.

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[11]Variable Gain Amplifier

For the 2.45 GHz receiver module design, there are two main power considerations:

1. The expected input power at the receiver is the tag's backscattered power, which is explained further in Section 2.2.1. However, there is a leaking carrier from the transmitter into the receiver. A description of this phenomenon is given in Section 2.2.2.

2. The output power, fed into the IF section, is variable and changes as function of the frontend gain configuration. Nevertheless, the aim of this frontend is to achieve always the maximum output power to drive the Rapid Prototyping Board without exceed the maximum power of 12.56 dBm. It is important not to exceed this value, otherwise the ADC of Rapid Prototyping Board could be damage. This fact requires a continuous monitoring and controlling of the system.

2.2.1. Backscattered signal

The expected backscattered input signal at the receiver is the most important input for the system due to the fact that, apart from containing the message of the tag, it defines the reader's sensitivity requirements. To calculate the required sensitivity, it is necessary to calculate previously the maximum distance range of the reader.

To determine the maximum distance range between the tag and the reader Equation 2.1 [4] is used.

$$P_{Tag} = G_{TX} P_{TX} G_{Tag} \left(\frac{\lambda}{4\pi r} \right)^2 \tag{2.1}$$

Where: P_{TX} is the transmitted power of the reader
   G_{TX} is the gain for the reader's transmitter antenna
   G_{Tag} is the gain for the tag's antenna
   λ is the wavelength
   r is the distance between reader and tag

Current passive tags require a minimum received power to feed the integrated circuit, P_{Tag}. In general, this minimum power is in the range of 5 μW to 50 μW [11]. For the calculations a minimum input power P_{Tag} of 5 μW is assumed. By definition, $G_{TX} P_{TX}$ is the EIRP. As presented in Section 1.3. the maximum EIRP is 4 W. Using this definition leads from Equation 2.1 to Equation 2.2.

$$P_{Tag} = EIRP \, G_{Tag} \left(\frac{\lambda}{4\pi r} \right)^2 \tag{2.2}$$

Hence, in order to calculate the maximum distance range of the reader having communication with the tag, G_{Tag} is the only parameter missing. Typically, this value is between 0 dBi[12] and -5 dBi [12]. Nevertheless, some 2.45 GHz RFID antennas can achieve slightly higher values as 0.766 dBi [13]. From Equation 2.2 the variable r is obtained as shown in Equation 2.3:

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[12]Here, the unit dBi indicates that this antenna gain is given with respect to an isotropic antenna

$$r = \sqrt{\frac{EIRP\, G_{Tag}\lambda^2}{(4\pi)^2 P_{Tag}}} \tag{2.3}$$

Then, assuming an antenna gain of 0 dBi, a required power of 5 μW at the tag, 4 W EIRP and a wavelength of 122 mm corresponding to a frequency of 2.45 GHz, in Equation 2.3, a maximum achievable read-distance range of 8.70 m is obtained for the reader.

With this maximum achievable read-distance range of the reader, it is possible to determine the strength of the backscattered signal at this distance. This value defines now the required sensitivity, and is given by Equation 2.4 [4]:

$$P_{RX} = \frac{P_{TX}G_{TX}G_{RX}\lambda^2\sigma}{(4\pi)^3 r^4} \tag{2.4}$$

The RCS[13], σ, can be calculated by Equation 2.5 obtained by Equation 1.7 (Section 1.2.) assuming that the internal impedance of the tag and the antenna tag are matched ($Z_c = Z_a^*$). Then, the result from Equation 2.5 is an RCS of 11.93 cm^2.

$$\sigma = \frac{\lambda^2 G_{Tag}^2}{4\pi} \tag{2.5}$$

Now, regarding all the assumptions made along the calculations, maximum distance range of the reader of 8.70 m, EIRP of 4 W and supposing the same antenna for both the transmitter and receiver and using Equation 2.4, the required sensitivity of the reader to achieve the distance of 8.70 m is 10.25 pW or -80 dBm.

With the receiver sensitivity calculated, it is possible to determine the maximum allowed direct coupled carrier to receive the tag's message successfully and the required transmitter-receiver isolation.

In order to develop a research environment where it is possible to work with an RFID 2.45 GHz reader until the limits, it means that $P_{backscattered}$ can be detected by the 14 bits ADC, an SNR[14] of 1 dB is assumed at the ADC for detection. It implies that in the worst case when $P_{backscattered}$ is -80 dBm and the leaking carrier is full modulating the ADC, this leaking carrier is not allowed to exceed a ratio of power of $20 \cdot \log(2^{14-1}) = 78.2$ dB from the $P_{backscattered}$ in order to achieve reader tag comunication with an SNR of 1 dB.

Therefore, with the minimum received input signal, the sensitivity of -80 dBm and the maximum ratio leaking carrier - $P_{backscattered}$ of 78.2 dB, the maximum possible direct coupled carrier at the input is -80 dBm $+ 78.2$ dB $= -1.6$ dBm. It means that assuming a transmit power of 36 dBm, it is necessary to achieve a transmitter-receiver isolation of 36 dBm $- (-1.6$ dBm$) = 37.6$ dB to communicate with the tag in the indoor mode.

To communicate with the tag in the outdoor mode, the same process described in this section is followed. Therefore, for the outdoor mode, it is calculated a maximum distance

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[13]Radar Cross Section

[14]Signal to Noise Ratio

range of 3.1 m for the reader and a required reader sensitivity of -70.1 dBm. Then, the maximum possible direct coupled carrier at the input is -70.1 dBm $+ 78.2$ dB $= 8.1$ dBm. It means that assuming a transmit power of 27 dBm, it is necessary to achieve a transmitter-receiver isolation of 27 dBm $- 8.1$ dBm $= 18.9$ dB.

Such high isolation values are only possible in dual antenna scenarios or with an additional carrier compensation module.

To calculate the admissible upper boundary of the reader's receiver noise figure, an SNR of 0 dB is supposed at the input of the ADC.

$$SNR = \frac{P_{Signal}}{P_{Ne}} \tag{2.6}$$

Then, the equivalent receiver output noise power P_{Ne} can be calculated with Equation 2.6. The result, for an SNR assumption of 0 dB, is that P_{Ne} must not exceed -80.0 dBm. On the other hand, at the input of the receiver there is a thermal noise. This thermal noise is -174 dBm/Hz by a bandwidth of 5 MHz[15] resulting a noise power P_N of -107 dBm at the input.

The noise figure, defined in Equation 2.7, can also be calculated in logarithmic scale as the difference of the equivalent receiver input noise power P_{Ne} and the noise power P_N.

$$F = \frac{P_{Ne}}{P_N} \tag{2.7}$$

The result of this calculation is a maximum noise figure F of 27 dB for the receiver, to detect the signal at the maximum distance range.

2.2.2. Crosstalk in RFID readers

Despite that the passive RFID system communication between the reader and the tag is half duplex, as explained in Section 1.2., one of the main properties of the passive RFID system is transmitting a carrier signal without any information to power up the integrated circuitry of the tag while receiving the tag message at the same frequency, at the same time. This property causes a carrier leakage from the transmitter to the receiver of the reader. This phenomenon is also known as crosstalk and it is produced by imperfect circulator isolation and the circulator - antenna mismatch when a single antenna scenario is implemented, see Figure 2.6, or when antenna to antenna coupling happens in a dual antenna scenario, see Figure 2.5.

In a dual antenna scenario, the quantity of signal directly coupled into the receiver, depends on the type of the antenna and the distance between each other. A way to reduce the direct coupling in this scenario is using high gain antennas. It is possible because this kind of antennas has a radiation pattern which allows to position the antenna beam in parallel. Also, moving the antennas more apart of each other increase the isolation, but it

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[15]The bandwidth of 5 MHz was assumed in the UHF design and corresponds to the testbed's nominal receiver bandwidth.
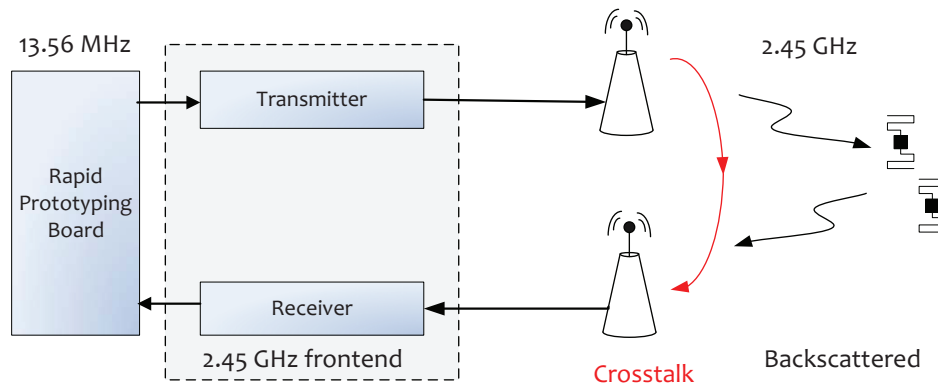
Figure 2.5: Crosstalk in a dual antenna scenario

is more difficult pointing to the tag. Typical transmitter-receiver isolation in a dual antenna scenario is in the range of $30 - 40$ dB.

In a single antenna scenario usually circulators are used to separate the receiver and the transmitter channels.
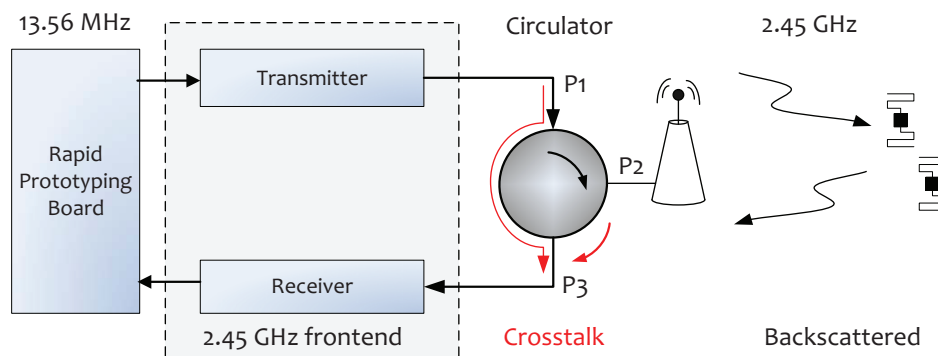
Figure 2.6: Crosstalk in a single antenna scenario

By definition, an ideal circulator isolates completely port 3 from port 1 if the port 2 is perfectly matched, in this case with the antenna. In practice, circulator's isolation is in the range of $20 - 25$ dB and this value further decreases if the antenna is not properly matched to the circulator. Therefore, single antenna readers are more challenging to build and often some sort of carrier compensation or direct coupling compensation has to be used.

Besides the leaking carrier produced in the scenarios shown in Figure 2.5 and in Figure 2.6, it is also possible to receive strong reflections from conducting objects near the RFID reader. The reflection level varies as function of the object size, conductivity and distance producing a carrier component at the receiver input.

These reflections occur and are critical in both scenarios reducing the expected isolation. Especially in dual antenna scenarios where the expected isolation is between 35 -40 dB, these reflections can result in damage of the receiver.

In a single antenna scenario, the critical situation happens when circulator and antenna mismatch occurs or even worst, when the antenna is not connected. Then, the transmitted

power is reflected back to the receiver board through the circulator port 3. For this reason it is necessary to withstand in both scenario high input power due to reflections, by means of using a shutdown system to avoid damages or using a carrier compensation enhancing the overall system quality.

2.3. Frequency plan

The transmitter and receiver discussed in this master thesis operates at three different frequencies:

IF1 Is the frontend input at the intermediate frequency f_{IF1} of 13.56 MHz.

IF2 Is the second intermediate frequency f_{IF2} at 140 MHz.

RF The nominal output frequency of 2.45 GHz

The reason of these three frequencies is the double frequency conversion concept used for the frontend. Figure 2.7 depicts the entire conversion process including all filter stages.

At the beginning of the frequency up conversion process, the IF1 input signal is filtered by a low pass filter with a cut-off frequency of 30 MHz. Then, it is upconverted to the IF2 by means of the first mixer which uses a local oscillator LO1 at 153.56 MHz. Both mixers employ high-side LO[16] injection, because this method favors to the upper sideband suppression using a band pass filter as image rejection filter and the harmonic suppression with a simple low pass filter. After this upconversion, the signal is again filtered with a SAW[17] filter. This filter has a 1 dB bandwidth of 5 MHz. Thus, the overall selectivity of the frontend is fixed to that bandwidth. However, as indicated in Chapter 1.3. the maximum occupied bandwidth per channel is 1 MHz for mode 2 so, this filter does not imply any critical limitation for the RFID system. The following step is the second and final upconversion to the nominal output frequency. For this second high-side LO injection a variable LO is used, centered at 2.59 GHz, providing a nominal output range between 2400 MHz and 2483 MHz. Finally, after the second upconversion, there are two more filters. The first, is a SAW band pass filter which is centered at 2.45 GHz and its function is to suppress the image frequency signal and the LO leakage from the second mixer. The second, is a low pass filter which is responsible for suppressing the harmonic frequencies.

This frequency plan could be used also to understand the receiver. The main difference is the upconversion direction which is downconversion at the receiver. Furthermore, all filters and mixers used at the transmitter design are the same in the receiver in order to simplify the design.

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[16]Local Oscillator
[17]Surface Acoustic Wave

Figure 2.7: Spectral overview of the 2.45 GHz frontend
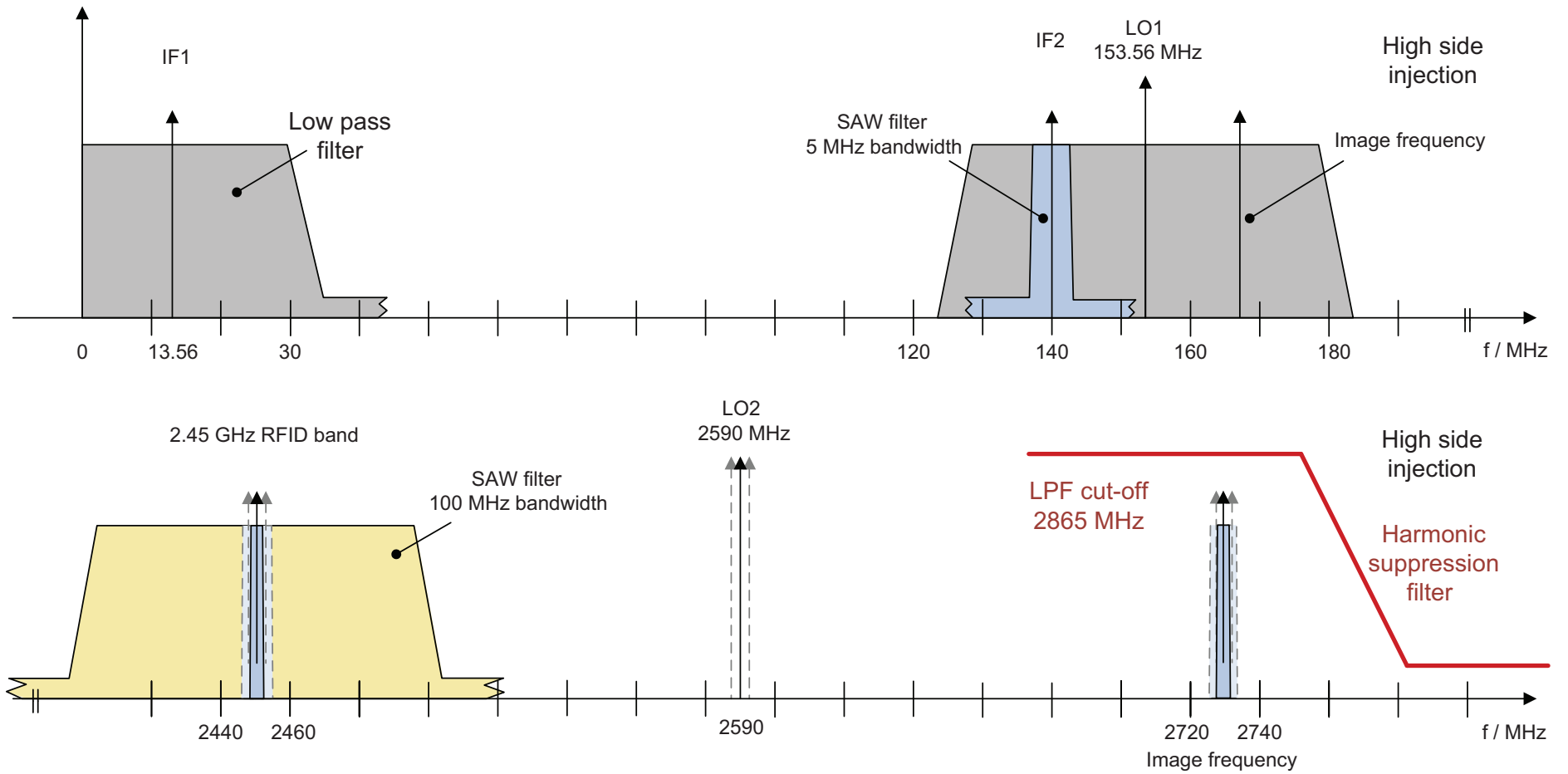
CHAPTER 3. TECHNICAL DESCRIPTION

This chapter gives an overview of the 2.45 GHz stage by means of block diagrams. Then, it discusses the layout considerations for the circuit implementation, which are required for a later integration with the existing parts of the IF stages. Finally, it describes in detail the circuit design of selected elements.

3.1. System block diagram

This section describes the block diagram for the system design and also describes the functions and requirements for each device. A more detailed description of them together with measurement results are given in the following Chapters 4 and 5.

The block diagram shown in Figure 3.1 gives an overview of the transmitter and the receiver for the 2.45 GHz frontend. The block diagram also shows all additional frontend parts which have to be taken into consideration for the design of the 2.45 GHz transmitter and the receiver. In the upper part of Figure 3.1 the transmitter, from the IF stage input connection on the left to the antenna output on the right, is shown. The CCU, a microcontroller and the LO source with its power splitter are placed in the middle of the figure.

The LO signal is provided by a signal generator at a frequency of 2590 MHz, and it is split up by a power divider which feds the transmitter's and receiver's LO ports.

The CCU allows to suppress a part of the carrier leakage by providing a well adjusted in amplitud and phase compensation signal. The microcontroller monitors the system power levels and controls the gain/attenuation settings of the testbed. Consequently, proper and adjusted inputs and outputs are required at the 2.45 GHz stage to be easily controlled and managed by external devices.

Finally, the lower part of the figure shows the receiver. The input of the receiver is at the antenna port, on the right, and its IF stage output to the UHF board is placed on the left of Figure 3.1.

3.1.1. Transmitter

The input of the 2.45 GHz transmitter module is connected to the UHF transmitter board using the X2 interface at the IF stage. This signal enters directly to the first element in the block diagram, the TX[1] Mixer, which performs the frequency upconversion of the IF2 input signal to the desired RF output range.

The RF output frequency range of 2446 -2454 MHz[2] is determined by a variable LO, shown as LO2 in Figure 3.1. Operating this LO2 at a frequency of 2.59 GHz, the 140 MHz IF2 input is upconverted to the center frequency of the microwave RFID band at 2.45 GHz.

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[1]Transmitter

[2]Mode 1 operation

Figure 3.1: Block diagram of the 2.45 GHz frontend
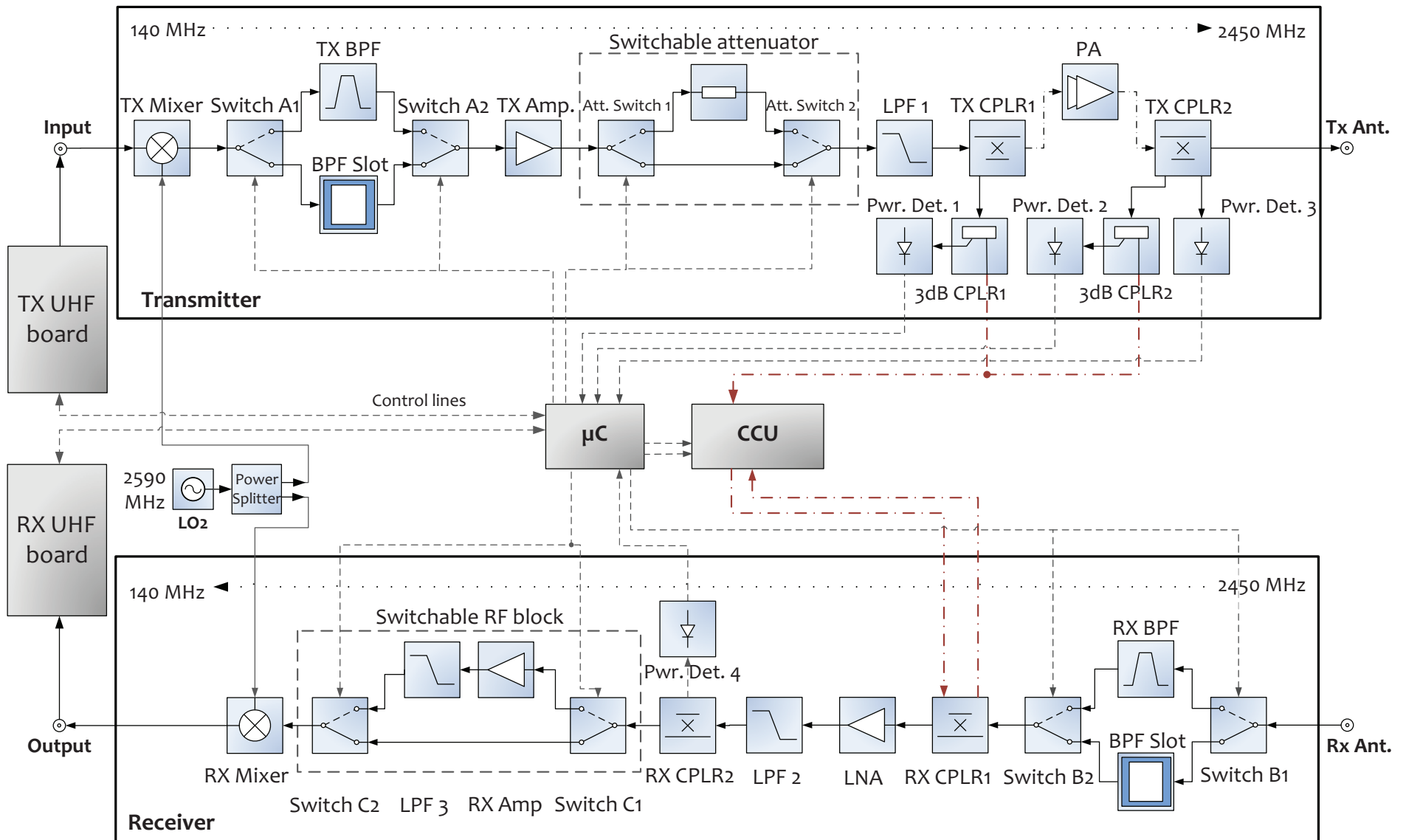
Nevertheless, the mixer also generates undesired spectral components, a frequency image at 2.73 GHz, LO leakage and harmonic frequencies. For these reasons one important parameter at the moment of selecting this mixer is the LO-RF isolation.

After the frequency upconversion, the signal enters a BPF[3]. This filter suppress the undesired image frequency signal and the LO leakage. Specially, the image frequency signal from the mixer is filtered at this element. Therefore, at time to select the BPF, a high attenuation at the image frequency band from 2726 MHz to 2734 MHz[4] is required. Furthermore, the maximum output frequency range is determined by the bandwidth of the BPF. In order to achieve a flexible design one can switch between a fixed onboard filter or a parallel signal path which allows to connect in a BPF slot new filters. This enhances the possibility of the system to adjust the overall frequency bandwidth to further RFID regulations. Then, it is possible to switch between the onboard BPF and the external BPF by means of the switches Switch A1 and Switch A2 shown in the Figure 3.1.

An amplifier, TX Amp, compensates for the losses in the previous stages and provides the necessary output power to the switchable attenuator. The purpose of this switchable attenuator is to allow for indoor and outdoor operation of the transmitter. As described in Section 1.3. the difference in terms of power between these two modes is 10 dB. Hence, the switchable attenuator for this design requires 10 dB attenuation. The next element that follows is a low pass filter, LPF[5] 1, responsible of the harmonic frequency suppression.

Finally, there are two directional couplers. One is placed prior the external power amplifier and the second after the external PA[6]. The first coupler of the transmitter, TX CPLR1 in Figure 3.1, extracts a signal sample of the non amplified forward path. A 3 dB coupler which acts as a power splitter, 3 dB CPLR1, divides the sample and provides a part to the CCU extension output port, and another to a power detector, Pwr. Det. 1. This power detector output allows to monitor the system RF power by a microcontroller. The second coupler of the transmitter, TX CPLR2 in Figure 3.1, is a high power coupler which performs the same as the first coupler. Additionally, it also provides a sample of the reverse power. This reverse power is originated at the transmitter antenna due to possibles mismatches or non properly connection between the board and the antenna. It is also measured by a power detector, Pwr. Det. 3, and monitored by the microcontroller in order to protect the external power amplifier from overloads by reducing the RF transmit power level.

3.1.2. Receiver

At the receiver, the input signal from the antenna is filtered by a BPF. The main function of this filter is to suppress any incoming signal located at the image frequency band because, at the downconvertion process the image frequency band, centered at the frequency of 2.73 GHz, is converted to the same IF2 frequency of 140 MHz as the 2.45 GHz RFID frequency of interest. Thus, this filter requires as much attenuation as possible on this image frequency band. Due to the possible regulation changes, a BPF slot allows further

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[3]Band Pass Filter
[4]For mode 1
[5]Low Pass Filter
[6]Power Amplifier

updates of this filter increasing, reducing or tuning the available receiver bandwidth. Here, it is possible to switch between the onboard BPF and the external BPF by means of the switches Switch B1 and Switch B2 shown in the Figure 3.1 at the receiver section.

Then, a directional coupler, RX[7] CPLR1 in Figure 3.1, serves as input port for the CCU extension, which suppress most of the leaking carrier when this circuit is used. The backscatter signal and the remaining leaking carrier are amplified by an LNA[8] and then filtered by the low pass filter LPF 2. At this point the same LPF design as at the transmitter is employed to suppress the harmonic frequencies.

The receiver design allows: gain adjusting and system shutdown. Both features avoid overloading the circuit from high input levels of direct coupled carrier or strong carrier reflections. Especially, the gain adjustment is done in different subsections to keep the minimum noise figure and do not overload the system itself.

For the gain adjustment and shutdown process, the input power level is measured at the second coupler of the receiver, RX CPLR2 in Figure 3.1. It extracts a sample which is provided to a power detector, Pwr. Det. 4. Here, the power level is measured and then, this result is fed into the microncontroller which takes the proper decisions for the reader performance. However, if the microcontroller is not connected to the system, the gain setting and the shutdown level can be set manually, further description in Section 4.1.4.

After the coupler follows an RF switchable gain block composed by an amplifier, RX Amp, and a low pass filter, LPF 3. This switchable subsection is used to amplify the power level when the leaked carrier is not so strong. For this purpose, the amplifier RX Amp and the low pass filter LPF 3 can be electronically bypassed by means of the electronic switches Switch C1 and Switch C2. Finally, the RX Mixer downconverts the RF signal to the 140 MHz IF2 frequency which is then received at the UHF board through the "X2" Interface.

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[7]Receiver
[8]Low Noise Amplifier

3.1.3. Devices selection

The device selection process is an important step in which every component has to be analyzed and selected to obtain the optimum performance, reasonable cost and availability. For this reason, it is a crucial step that requires time to study carefully the different manufacturer' solutions.

Table 3.1 gives a list of the devices I have selected for this thesis. This table indicates the model, manufacturer, distributor and the features for its selection.

Table 3.1: Devices selection list

Device	Model	Manufacturer	Features for selection
TX, RX Mixer	MAX2043	Maxim	Low LO leakage
TX Amp.	AD5542	Analog	18 dB gain, O1dBcomp[9]
RX Amp.	MGA-30216	Avago	11.8 dB gain, 2.8 dB F[10]
LNA	MGA-632P8	Avago	15.3 dB gain, 0.97 dB F
Attenuator	HMC541	Hittite	10 dB attenuation
Couplers	BDCA1-7-33+	Minicircuits	7 dB coupling
TX CPLR2	SYBD-16-272HP+	Minicircuits	16 dB coupling
3 dB CPLR1, 2	DB0805A	AVX RF	3 dB coupling
Pwr. Det.	ADL5513	Analog	80 dB dynamic range
Switches	SWMA-2-50	Minicircuits	TTL, absorptive
TX, RX BPF	B9430	Epcos	100 MHz passband
LPF 1,2,3	Butterworth	Selfmade	3 dB cutoff 2865 MHz

3.1.4. Specification of the 2.45 GHz stage

This subsection provides a summary of the input and the output parameters and the control pins for the receiver and the transmitter of the 2.45 GHz stage. Table 3.2 shows the power supply requirements, the maximum and the minimum input and output RF power levels, the gain and the noise figure for the transmitter and the receiver module. In this table, the values are given for indoor operation, unless otherwise is described. Furthermore, the transmitter's values are given without the external PA which provides a gain of 35 dB.

For the power supply and the external control lines a 25 pin Sub-D connector is provided. The pinning of this connector, the X1 main connector, is listed in Table 3.3 and Table 3.4[11].

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[9]Output 1 dB compression point of 16.6 dBm

[10]Noise Figure

[11]IF stage and 2.45 GHz stage are merged, some of the pins listed are ports for the UHF design which are explained in detail in [9].

Table 3.2: Specifications of the 2.45 GHz stage

Parameter	Conditions	Min	Typ	Max	Unit
Power supply					
TX/RX positive supply voltage		9.5	10	10.5	V
TX/RX negative supply voltage		-10.5	-10	-9.5	V
TX/RX positive supply current				0.65	A
TX/RX negative supply current				50	mA
Transmitter					
Abs. maximum IF2 input power	Full gain			13.5	dBm
Maximum IF2 input power	Lin. op.			11	dBm
Maximum RF output power	Lin. op.			11.9	dBm
Maximum RF output power	Compr. op.			14.4	dBm
Gain	Indoor		-0.1		dB
Gain	Outdoor		-9.5		dB
CCU before PA output attenuation			9.5		dB
CCU after PA output attenuation			39.4		dB
Receiver					
Abs. maximum RF input power	Lowest gain			15	dBm
Abs. maximum CCU input power				28.4	dBm
Maximum RF input power	Lin. op.		8		dBm
Maximum CCU input power			28.4		dBm
Maximum IF1 output power	Full frontend		12.4		dBm
Gain		-3.9		7.1	dB
Frontend noise figure	Full gain		7.7		dB
2.45 GHz stage noise figure	Full gain		5.5		dB

Table 3.3: Transmitter connector X1 pin definition

Pins	Use	Stage to control
1-3, 14-16	Ground	Both stages
4	External gain control	IF stage
5	External gain control ground	IF stage
6	Power detector before PA	2.45 GHz stage
7	Operation mode control	2.45 GHz stage
8	BPF selector	2.45 GHz stage
9	Enable line 2	IF stage
10	Enable line 1	2.45 GHz stage
11-13, 23-25	Positive power supply	Both stages
17	VGA reference voltage output	IF stage
18	VGA reference voltage output ground	IF stage
19	Antenna reverse power detector	2.45 GHz stage
20	Antenna reverse power detector ground	2.45 GHz stage
21	Antenna forward power detector	2.45 GHz stage
22	Antenna forward power detector ground	2.45 GHz stage

Table 3.4: Receiver connector X1 pin definition

Pins	Use	Stage to control
1-2, 14-16	Ground	Both stages
3	BPF selector	2.45 GHz stage
4	IF1 detector DC output	IF stage
5	Second RF amplifier control line	2.45 GHz stage
6	VGA 16 dB attenuator control line	IF stage
7	VGA 8 dB attenuator control line	IF stage
8	VGA 4 dB attenuator control line	IF stage
9	VGA 2 dB attenuator control line	IF stage
10	VGA 1 dB attenuator control line	IF stage
11	Auxiliary line 1	IF stage
12-13, 24-25	Positive power supply	Both stages
17	IF2 10 dB attenuator control line	IF stage
18, 22	Negative power supply	Both stages
19	IF2 power detector	IF stage
20	Measurement ground	IF stage
21	RF power detector	2.45 GHz stage
23	Auxiliary line 2	IF stage

3.2.   Layout considerations

The system concept described is functionally compatible with the previous designed UHF frontend. In order to increase this compatibility even more, this section establishes the layout considerations which makes it easier to fully integrate this project with the already existing external circuits.

Figure 3.2 and Figure 3.3 show the delimitation areas to implement the circuit for the different frequency stages. The boards are divided into three parts, the IF stage, the 2.45 GHz stage and the power supply and control stage. Each stage is delimited in area and located in a suitable place in order to avoid RF coupling, to realize the interconnection and the merging of the UHF design and the 2.45 GHz design as simple as possible. Furthermore, to achieve an homogeneous system the connection positions are kept from the previous designs.

The RF, control and supply voltage ports of the frontend circuits are also depicted in Figure 3.2 and Figure 3.3. Both, the transmitter and the receiver PCB[12] have the Eurocard format $160\text{mm} \times 100\text{mm} \times 1\text{mm}$. This format is compatible with vertical mounting in a standard 19 '' housing or as the UHF frontend allows to enclose the circuit in a standardized steel frame housing.

Table 3.5: Properties of the employed FR4 PCB material

Parameter		Value	Unit
Relative permittivity	ε_r	4.7	-
Dielectric loss	$\tan\delta$	0.014	-
Height	h	1	mm
Copper plating thickness	d	35	μm
50 Ω microstrip line width for 2450 MHz	w	1.418	mm

The material for the printed circuit board is a low cost epoxy, the FR4[13], which properties are summarized in Table 3.5. All RF ports use SMA[14] connectors except the BPF slot connectors that are MMBX[15]. Using a steel frame housing which measures $160\text{mm} \times 100\text{mm} \times 35\text{mm}$), MMBX connectors and in series adapters allow to achieve a suitable board to board connection of 12 mm not exceeding the 35 mm height available.

The receiver shown in Figure 3.2 has the 2.45 GHz RF input ports located at the top right corner. The CCU input port is for a possible leaking carrier suppression and below this connector the antenna input is placed. The input signal of the antenna port is downconverted to a frequency of 140 MHz using a LO at the frequency of 2590 MHz connected to the LO2 port. Then, this downconverted signal is driven through the 2.45 GHz stage to the IF stage at the top left side. Therefore, all components working at the 2.45 GHz stage are inside the green area. The grey area is the IF stage of the UHF design. In this

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[12]Printed Circuit Board

[13]FR4 is the grade designation of the National Electrical Manufacturers Association for glass reinforced epoxy.

[14]SubMiniature version A

[15]Micro Miniature Board Connectors
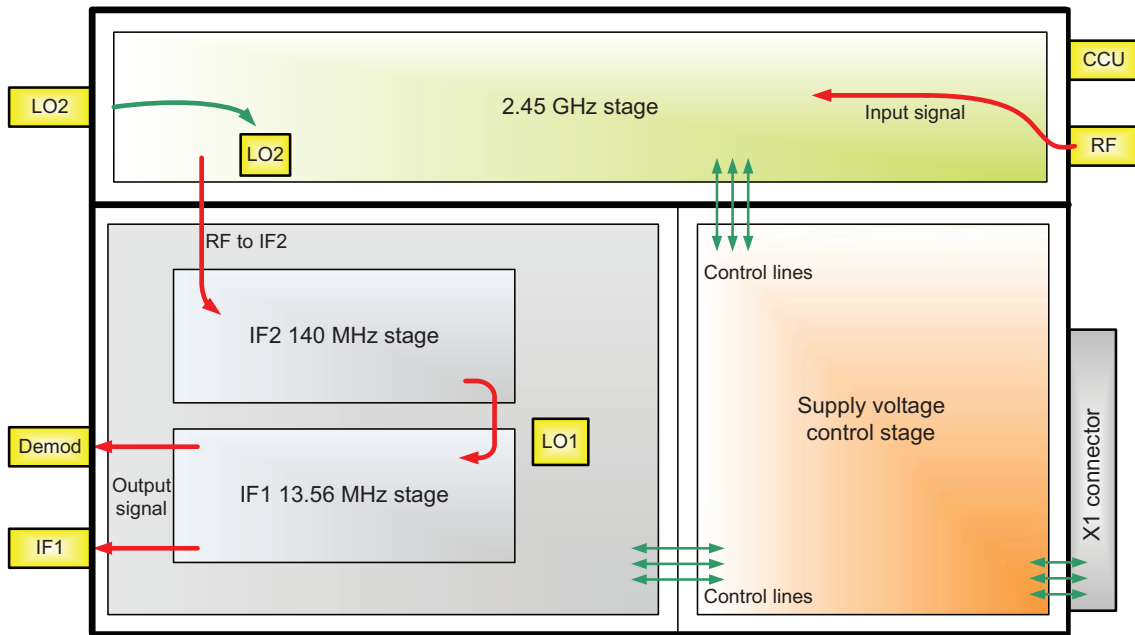
Figure 3.2: Receiver overview

zone, the incoming signal at 140 MHz is downconverted to 13.56 MHz employing a LO at the frequency of 153.56 MHz connected to the port LO1. Finally, this stage provides the output to the Rapid Prototyping Board through the port IF1, and also a demodulated signal through the port Demod.

The last area is the orange area which represents the power supply and control stage. This stage is endowed with jumpers and a trimmer resistor for a manual board configuration. Furthermore, for the supply voltage and the remote control, the X1 connector (see Table 3.3 and Table 3.4) is used. To indicate the status of the supply voltage and the configuration, four LEDs[16] are installed close to the control lines.

The transmitter shown in Figure 3.3 receives the 13.56 MHz input signal from the Rapid Prototyping Board on the bottom left corner. This signal is amplified and filtered in this grey area and also upconverted to the second IF frequency of 140 MHz. Therefore a LO signal with a frequency of 153.56 MHz is provided at the port LO1. The next stage, delimited to the green area, is the 2.45 GHz stage. This sector upconverts the input signal to the desired frequency of 2.45 GHz using the LO of 2590 MHZ frequency provided at the port LO2. Moreover, this sector amplifies and filters the signal to the proper power level which is fed into the external PA by the output port PA1. Additionally, the actual RF power level is measured to control the overall system gain and also a signal sample is provided to the CCU via the CCU1 port (without the external power amplifier amplification).

After the external amplification, the signal is supplied back to the circuit through the port PA2. The signal is sampled and measured in the top right corner of the board, and then, it is fed into the CCU by the right side CCU2 port. The last section, the orange area, is the power supply and control section. As at the receiver board, the settings can be remotely controlled with the external microcontroller or manually controlled via internal jumpers. The status is indicated with LEDs.

---

[16]Light Emitting Diode

Figure 3.3: Transmitter overview

3.3. Selected elements

The devices selected in the Table 3.1 operate at a frequency of 2.45 GHz. However, some of these devices as the LNA require impedance matching and optimization in order to achieve the best performance at the desired frequency band.

This subsection describes how I have realized the different devices optimizations, which in some cases requires to design new input and output matching networks. The simulation environment of AWR[17], Microwave Office, is used. Nevertheless, the results obtained from this software are simulation results. Hence, to corroborate the new devices performance and the manufacturer's circuit application, individual test PCBs have been implemented.

3.3.1. Mixer

The mixer is the first element of the 2.45 GHz transmitter module and the last element in the 2.45 GHz receiver module. The chosen mixer is a MAX2043 from Maxim as indicated in Table 3.1. The reasons for this choice are:

- Upconverter and downconverter operation

- Integrated baluns in RF and LO ports

- -3 to 6 dBm LO input power

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[17]Provider of electronic design automation software solutions

- Low LO leakage at the RF port (isolation of 38 dB)

- High input compression point of 23 dBm for high side injection[18]

Mixers are devices which translates signals from one frequency to another frequency. Functionally, this operation is a multiplication. The output for the mixer can be calculated as described from Equation 3.1 to Equation 3.3.

$$\alpha_{out}(t) = \alpha_{IF}(t) \cdot \alpha_{LO}(t).$$

$$\text{With } \alpha_{LO}(t) = \cos(\omega_{LO}t) = \cos(2\pi f_{LO}t)$$
$$\text{and } \alpha_{IF}(t) = \cos(\omega_{IF}t) = \cos(2\pi f_{IF}t)$$

(3.1)

For the frequency translation, the mixer multiplies the IF input signal with the LO input signal as Equation 3.1 shows. The result is the sum and the difference of IF and LO frequencies. When α_{IF} and α_{LO} have a sinusoidal form then, Equation 3.1 can be written as Equation 3.2.

$$\alpha_{out}(t) = \frac{1}{2}\left[\cos(2\pi(f_{LO} + f_{IF})t) + \cos(2\pi(f_{LO} - f_{IF})t)\right].$$

(3.2)

Hence, the expected output for our system using high side injection of the LO is given in Equation 3.3.

$$f_{RF} = f_{LO} - f_{IF2} = 2.45 \text{ GHz} \quad \text{and} \quad f_{Image} = f_{LO} + f_{IF2} = 2.73 \text{ GHz}$$

(3.3)

Both frequencies, at f_{RF} and f_{Image}, have the same power level. Then, the expected mixer output are two identical signals separated 140 MHz from the local oscillator signal which also is leaked into the RF port but, attenuated 38 dB as the datasheet [14] indicates. To analyze the device behavior and corroborate the values provided by the manufacturer's datasheet, a test PCB which can be operated as upconverter and as downconverter is implemented. In Figure 3.4a and Figure 3.4b the layout and the test board, respectively, are depicted.

As a result of this analysis, shown in Figure 3.5, the expected values are achieved. With an input signal of -15 dBm at the frequency f_{IF2} and 0 dBm at the frequency f_{LO}, the mixer's output is a 2.45 GHz RF signal with a power level of -23.8 dBm. This value fulfills with the expected mixer insertion loss of 8.8 dB given at the datasheet [14].

Besides the RF signal, the image signal presence at 2.73 GHz, the LO leakage attenuated 38 dB due to the non absolute port isolation and the harmonic at $2 \times f_{RF}$ are observed.

Consequently, to suppress the image signal at f_{Image}, the LO leakage and the harmonic frequencies it is necessary to filter the mixer output. This filtering process is done by an image rejection filter and a harmonic suppression filter which are described in Section 3.3.2. and Section 3.3.3.

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[18]When the LO frequency is greater than the RF frequency

(a) Mixer layout
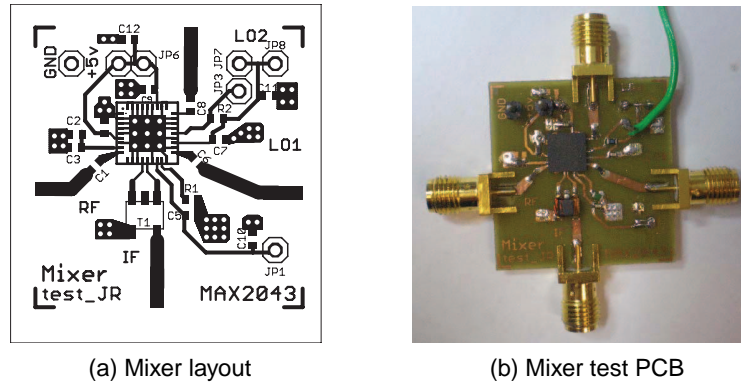
(b) Mixer test PCB

Figure 3.4: Mixer layout and implemented test PCB
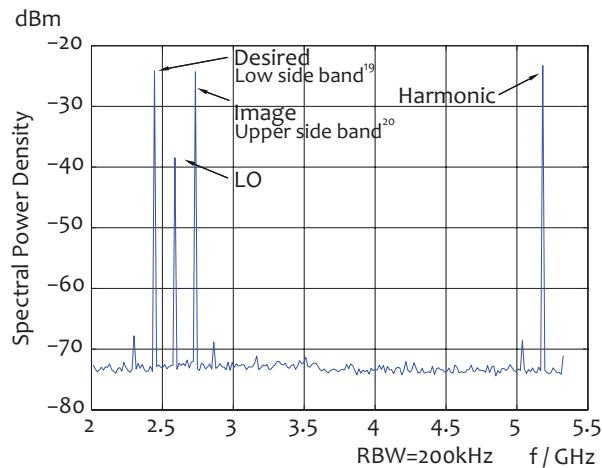
Figure 3.5: Measured result for an input signal at f_{IF2} with a power level of $P_{IF2} = -15$ dBm

3.3.2. Image rejection filter

The image rejection filter has as main goal to suppress the image signal at f_{Image} located in the upper side band, exactly at the frequency $f_{Image} = 2.73$ GHz. Nevertheless, this filter also attenuates the LO leakage and undesired harmonic frequencies.

For this purpose, a bandpass filter, the B9430 [15] SAW filter from EPCOS is used. The reasons for its choice are:

- Low insertion loss of 2.2 dB

- Constant amplitude ripple of 0.7 dB

- Attenuation of 15 dB at $f_{Image} = 2.73$ GHz

- Notch at $f_{LO} = 2.59$ GHz

- Usable passband of 100 MHz

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[19]Lower than the LO2 frequency
[20]Higher than the LO2 frequency

New input and output matching impedance networks are designed to improve the BPF performance to an insertion loss of 1.8 dB.
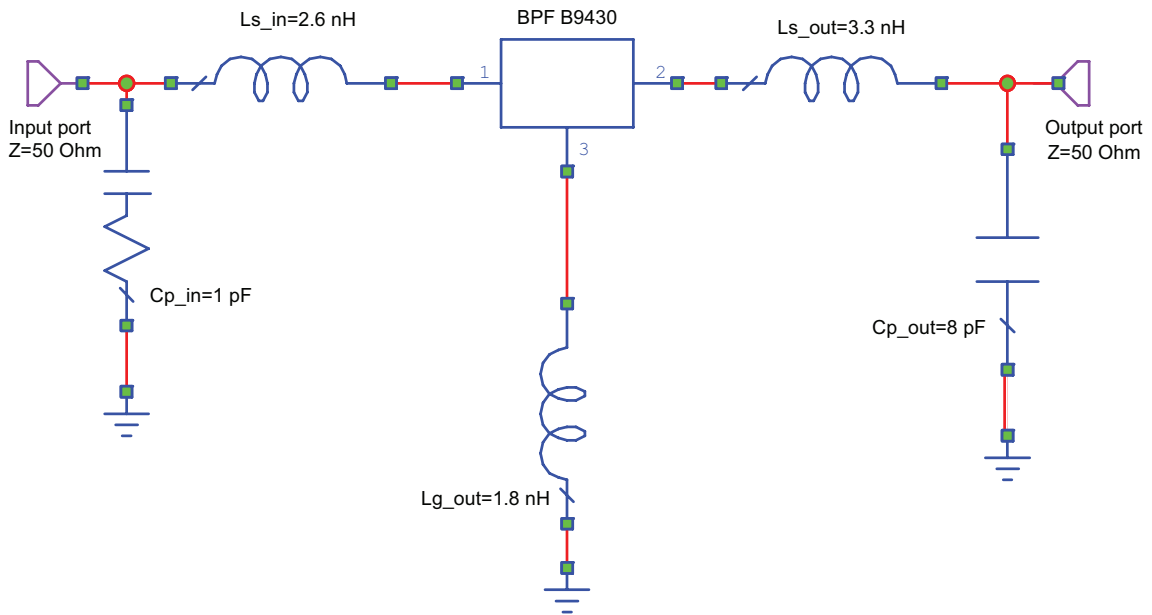
Figure 3.6: Epcos BPF schematic with input and output impedance network for simulation

Figure 3.6 shows the input and the output matching impedance networks schematic for the simulation. Furthermore, Figure 3.7a shows the simulated frequency response of the filter overlayed with the measured output of the mixer. Figure 3.7b shows the resulting filtered output signals of the implemented test PCB.

(a) BPF input and filter frequency response

(b) High side band and LO leakage suppression
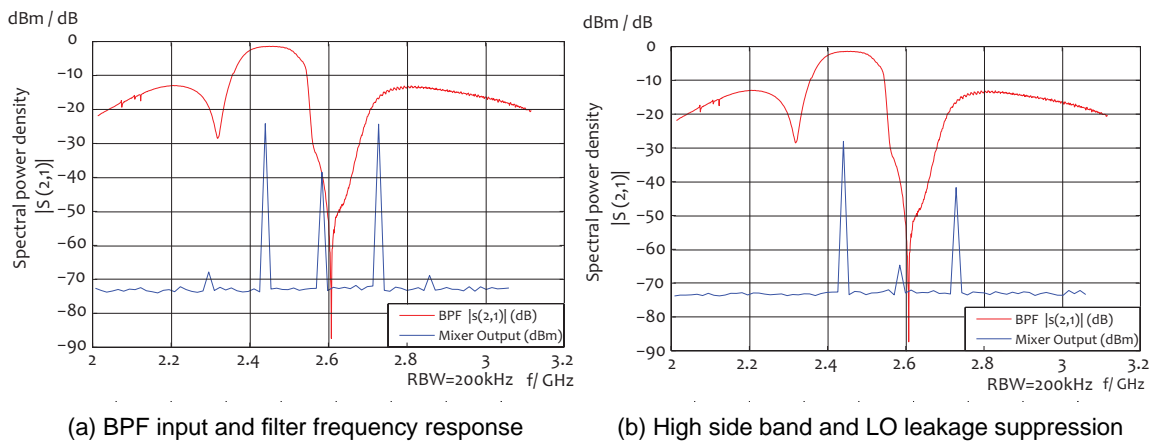
Figure 3.7: Filter performance

In these last figures (Figure 3.7) it is possible to see how the filter acts perfectly over the input signals, achieving: an insertion loss of 1.8 dB at the RFID band (2400 MHz - 2483 MHz) an additional LO leakage attenuation of 26 dB and the upper side band suppression better than 17 dB.

3.3.3.   Low pass filter

Because its maximally flat frequency response and linear phase response, a Butterworth lowpass filter fits very well with the reader requirements. However, its smooth frequency response implies to design a high order filter to achieve a sharply frequency response comparable with a Chebyshev lowpass filter.

Then, an 11th order Butterworth lowpass filter with a cutoff frequency of 2865 MHz is designed to give a sharply and maximally flat response using the insertion loss method explained in [16].

Table 3.6: Components values of the lowpass filter

Inductors		Capacitors	
L_1, L_6	1.8 nH	C_1, C_5	0.8 pF
L_2, L_5	3.3 nH	C_2, C_4	1.2 pF
L_3, L_4	4.3 nH	C_3	1.5 pF

Nevertheless, despite using this method, the component values of the filter are for ideal lumped elements. This needs to be readjusted and optimized changing then this ideal lumpeds elements to real lumped elements in the simulation of Microwave Office. With these new real values listed in Table 3.6 the filter is implemented as shown in Figure 3.8.
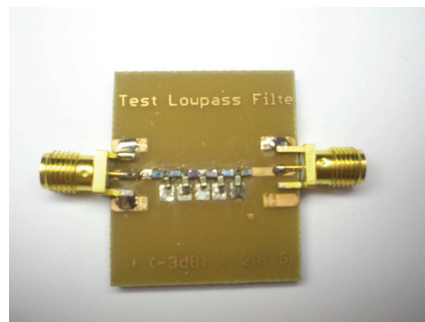
Figure 3.8: Implemented test PCB of a 11th order Butterworth LPF

In Figure 3.9 the implemented filter performance is shown and is compared with the simulated performance.

As it is shown in Figure 3.9, the implemented test PCB performance is very close to the simulated performance. The small difference between them is produced by the electronic components tolerance. Nevertheless, the insertion loss for the 2400 MHz - 2483 MHz passband is 0.8 dB and flat, and the harmonic signal at $2 \times f_{RF}$ is 55 dB attenuated.
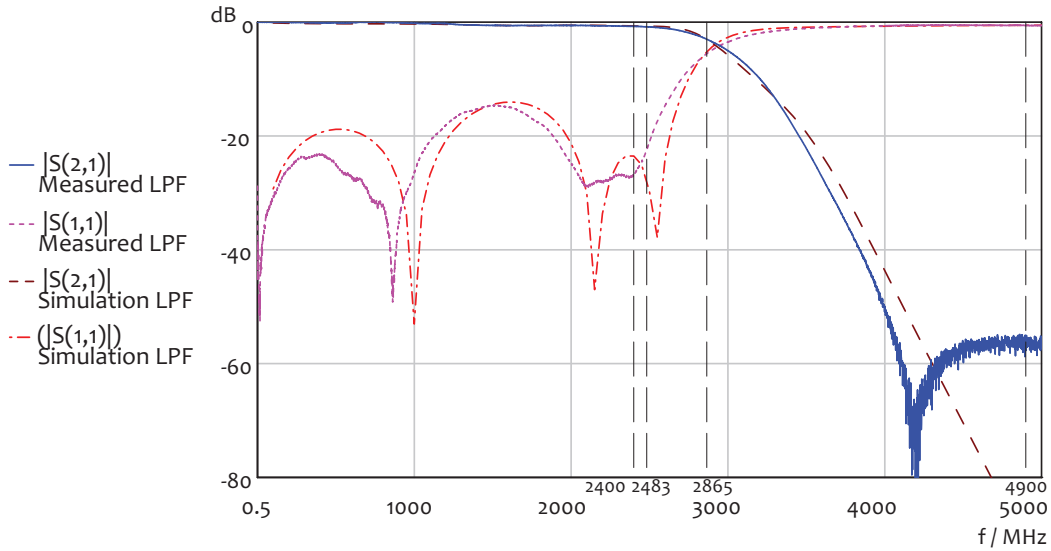
Figure 3.9: Comparison of measured filter and simulated filter performance

3.3.4. Low noise amplifier

As shown in Table 3.1 of this chapter, the selected LNA is the MGA-632P8 from AVAGO. The purpose of this amplifier is to amplify the input forward power from the antenna adding minimum noise. The main parameters of this LNA are:

- Noise figure of 0.97 dB.

- Gain at 2.6 GHz of 15.3 dB.

- Output 1 dB compression point at 18.5 dBm.

- Maximum input power for CW[21] of 20 dBm.

The maximum input power for a CW of 20 dBm and the output 1 dB compression point at 18.5 dBm allow supporting input signals for low transmitter – receiver isolation at the receiver. Nevertheless, despite this device can support lower isolation values as calculated in Section 2.2. it does not imply that the reader can operate safety without any device impairment at lower isolations as described in Section 2.2.

The parameters listed above, are taken from the manufacturer's datasheet [17] which are obtained at the frequency of 2.6 GHz using a demo board from Avago. This demo board uses a 10 mils Rogers RO4350 PCB material which has different properties than FR4. For these reasons, I have designed and implemented a test PCB that allows the evaluation of the LNA performance at 2.45 GHz using the FR4 PCB material and electronics components from different manufacturers.

Then, to implement a test PCB optimized at 2.45 GHz it is necessary to design the input and the output matching network starting from the device S-parameters, shown in Table 3.7.

Table 3.7: MGA632P8 S-parameters

Frequency	S(1,1)		S(2,1)		S(1,2)		S(2,2)	
GHz	Mag	Phase	Mag	Phase	Mag	Phase	Mag	Phase
2.5	0.360	-62.3°	4.930	113.3°	0.006	97.2°	0.49	-117.3°

To develop the input and the output matching networks, the input and the output impedance of the LNA, Z_{IN} and Z_{OUT}, are calculated. Thus, with these two values the starting points, in the following, the process for the input matching network design is described.

From the S(1,1) parameter indicated in Table 3.7, the normalized[22] Z_{IN} as shown in Equation 3.4 is calculated.

$$\frac{Z_{IN}}{Z_0} = \frac{1 + r + jx}{1 - r - jx} = 1.0955 - j0.8 \tag{3.4}$$

---

[21]Continuous Wave

[22]Normalized to $Z_0 = 50\,\Omega$

Now, using the Smith Chart in Figure 3.11, it is possible to create the input matching network for matching Z_{IN} to the characteristic impedance of the system $Z_0 = 50\,\Omega$. Although it is known that there are infinite available matching networks designs, for this LNA it is interesting to design a highpass matching network which allows AC[23] coupling as shown in Figure 3.10 avoiding a DC[24] bias voltage from previous and following circuits.
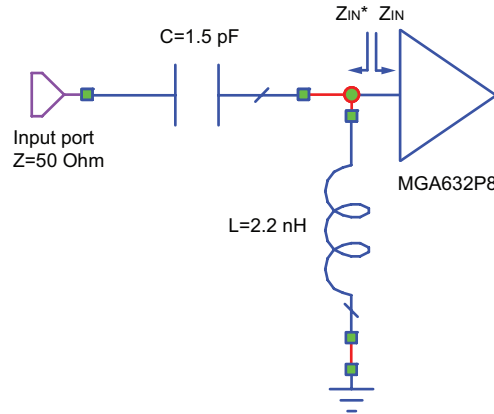
Figure 3.10: AC coupling input matching network

Therefore, starting from the Z_{IN} point in the Smith Chart, and going on the circle with constant conductance, changing only the susceptance until the circle of constant impedance of $50\,\Omega$, a shunt inductor L_{IN} of 2.2 nH is added. From this point, going on the circle of constant impedance of $50\,\Omega$ until $Z_0 = 50\,\Omega$ is possible adding a serial capacitor $C_{IN} = 1.5$ pF.
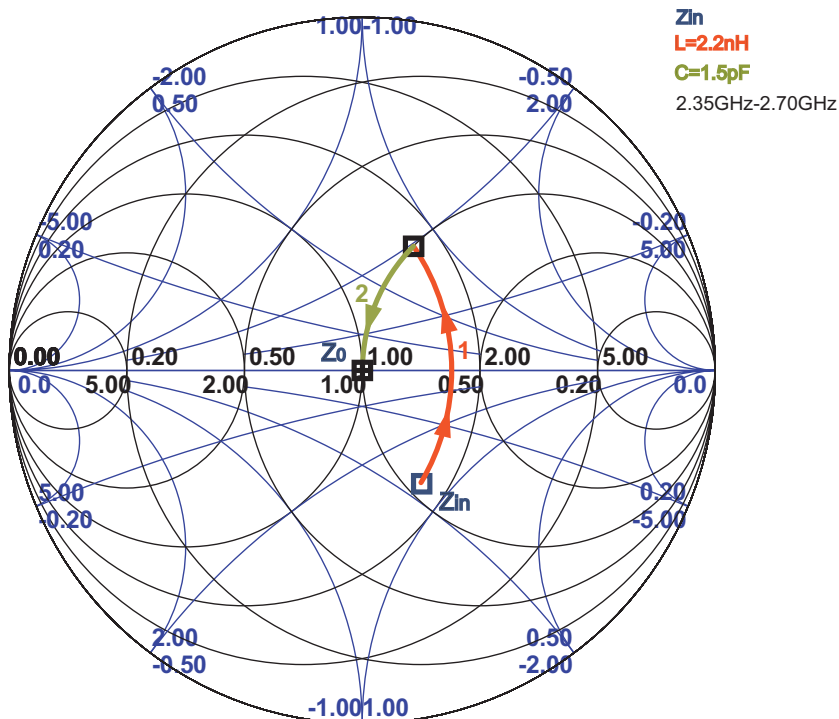
Figure 3.11: Matching Zin with the Smith Chart

[23]Alternating Current
[24]Direct Current

To achieve properly matching at the output the same process is done. For this matching network a shunt inductance, $L_{OUT} = 2.2\text{nH}$, and a serial capacitor, $C_{OUT} = 22\text{pF}$, are added.

With the input and the output properly matched, the LNA only needs a biasing circuit. For this purpose, the same application circuit from the datasheet is used as reference [17, Figure 33]. This biasing circuit consist of a bias resistor, RBIAS of 620 Ω, to set the current at the input and an RF choke, L3 = 47nH, combined with different shunt capacitors, C5 = 22 pF, C6 = 1 nF, C24 = 0.1 uF for high, medium and low frequency filtering.
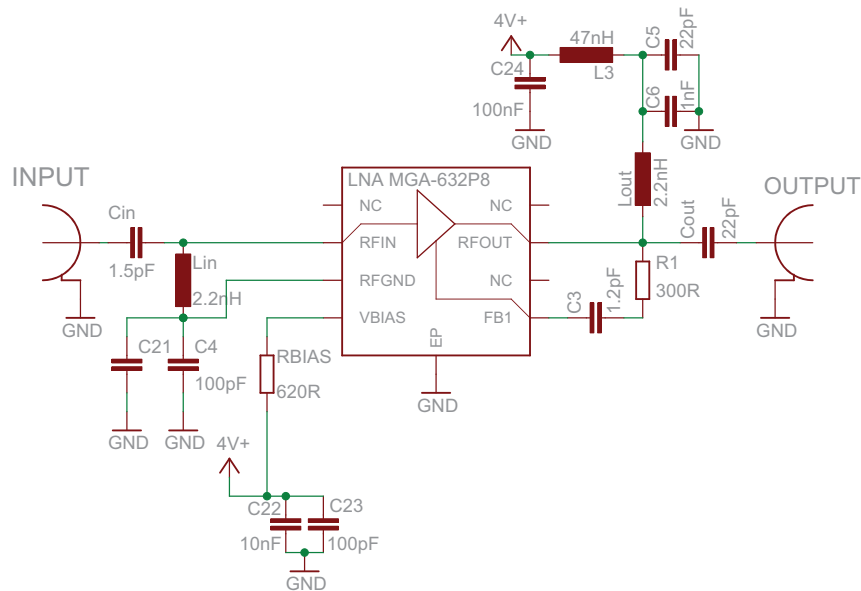
Figure 3.12: Schematic of the LNA PCB

Once the circuit is designed, the test PCB is implemented following the schematic of Figure 3.12 to analyze the LNA performance. Figure 3.13 compares the simulated LNA behavior with the measured LNA behavior obtained using a vector network analyzer. The obtained S(1,1) and S(2,2) results shown in Table 3.8 fits quite well with the expected results achieving input and output reflection coefficients lower than -16 dB.

Table 3.8: Expected and measured values

	Simulation	Measured
S(1,1)	R = 1.01 X = 0.04	R = 0.98 X = 0.24
S(2,2)	R = 0.89 X = 0.08	R = 0.83 X = 0.001
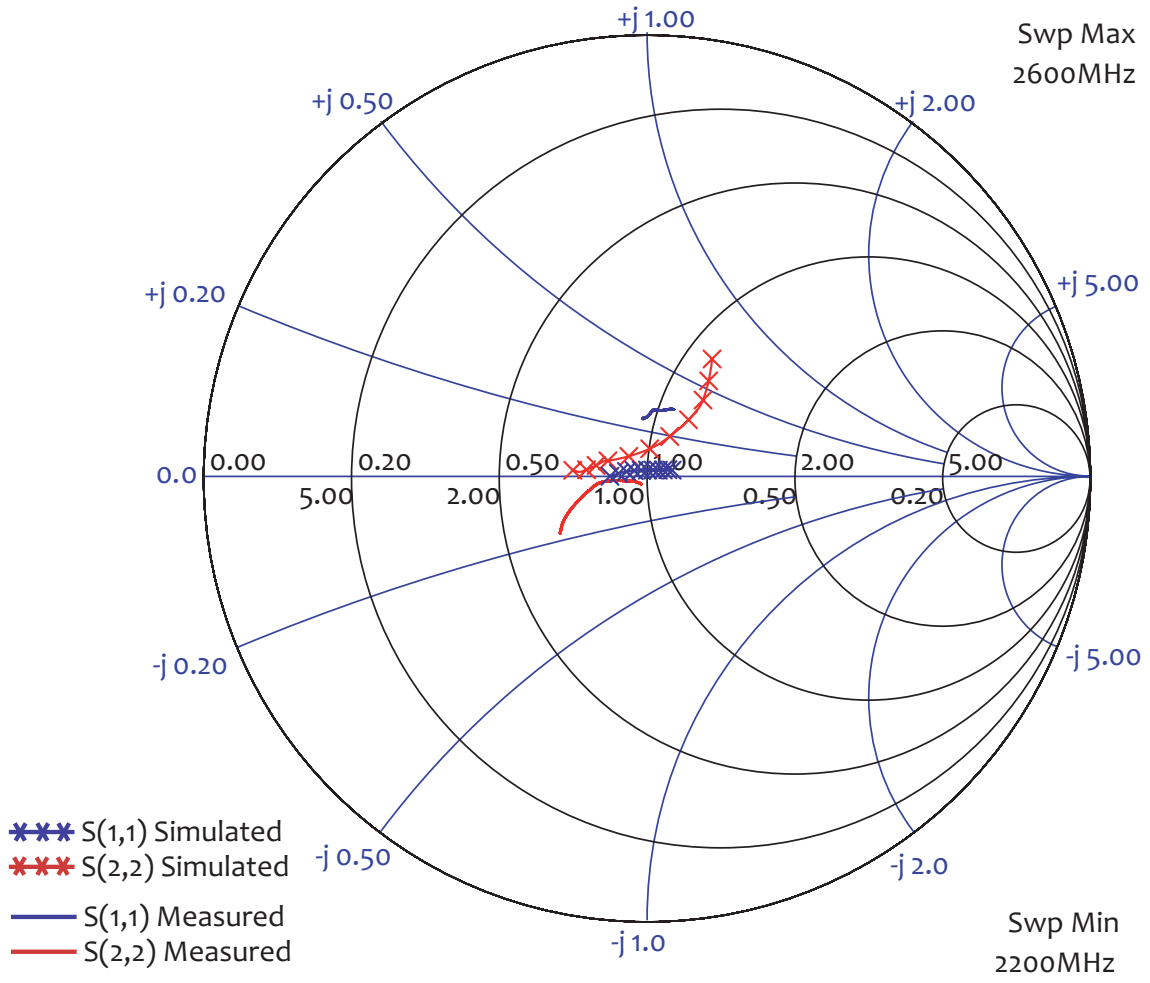
Figure 3.13: LNA comparison Simulation - Real

CHAPTER 4. RECEIVER

This chapter describes the 2.45 GHz receiver circuit designed and built during this master thesis. This circuit supplies the IF stage explained in detail in [9, pag. 54-57]. Furthermore, the power level plan for this board and the measurements results of the tested receiver prototype are described.

4.1. The 2.45 GHz receiver circuit

4.1.1. Switchable BPF and LNA stage

The incoming RF signal from the antenna, first is filtered by a BPF. This band pass filter attenuates out of band signals especially the image frequency band from 2680 MHz to 2763 MHz. As explained in Section 3.1.2. there is the possibility to operate the frontend either with an internal band pass filter, the Epcos B9430 or with an external filter. The selection between these filters is done by means of the switches shown in Figure 4.1, SWITCH_B1 and SWITCH_B2, which are controlled by the lines TTL_CTRL_INV_A and its inverted TTL_CTRL_A, respectively. Figure 4.1 shows the BPF and the values of the components CP_OUT and LS_OUT for the input matching network and LS_IN and CP_IN for the output matching network. After the filtering, the onboard BPF and the external BPF slot paths merge together at the switch SWITCH_B2. At this switch the RF ports RF1 and RF2 are exchanged compared to the switch SWITCH_B1 due to layout considerations.
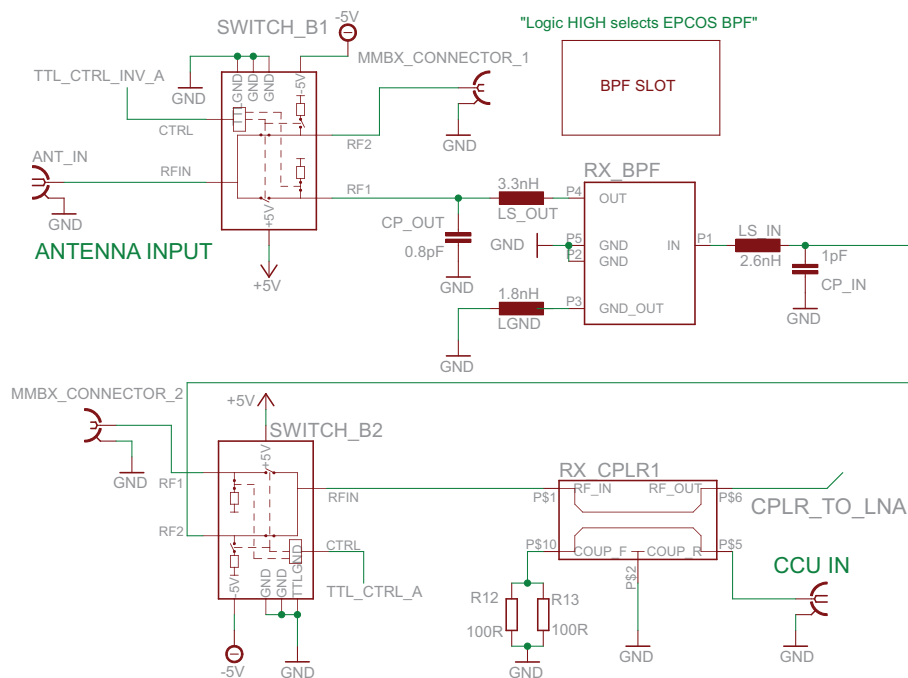
Figure 4.1: Switchable BPF and CCU coupler schematic of the receiver

After this filtering stage, the signal is fed in the directional coupler, RX_CPLR1. This coupler is a BDCA1-7-33+ from Minicircuits with a typical coupling loss of 6.4 dB and a mainline

loss of 1.4 dB. This coupler allows to inject a leaking carrier component with the polarity inverted, from an external carrier compensation unit, via the reverse coupled port to the main receiver path for carrier suppression. In order to avoid reflections back to the antenna, the forward coupled port is terminated by means of two parallel 100 Ω resistors, R12 and R13, in 1206 style. This 1206 style resistor withstand high power levels up to 0.25 W per resistor that allows to inject up to 28.4 dBm of carrier compensation signal to the receiver, 27 dBm of the resistors plus 1.4 dB of the coupler mainline loss.

The output RF_OUT of the coupler RX_CPLR1 is then amplified by the LNA MGA-632P8 from Avago Technologies. As described in Section 3.3.4. this LNA is chosen based on its power handling capability for a CW input power of 20 dBm and its output 1 dB compression point at 18.5 dBm. Figure 4.2 shows the optimized input matching network composed by C14 and L42, and the output matching network composed by L7 and C135. The capacitors C135 and C14 are also AC coupling capacitors in order to prevent DC biasing to the following and to the previous devices. This DC biasing at the LNA's output port is produced by a 4 V biasing voltage. In order to prevent external RF signals coupling or coupling between the RF output and the RF input over the supply circuit, the shunt capacitors C133 and C134 and the choke inductor L34 build a filter network to decouple AC signals. For the same purpose, at the VBIAS pin a similar AC filter network is composed by L52, C154, C155 and a high precision resistor which determines the biasing input current.
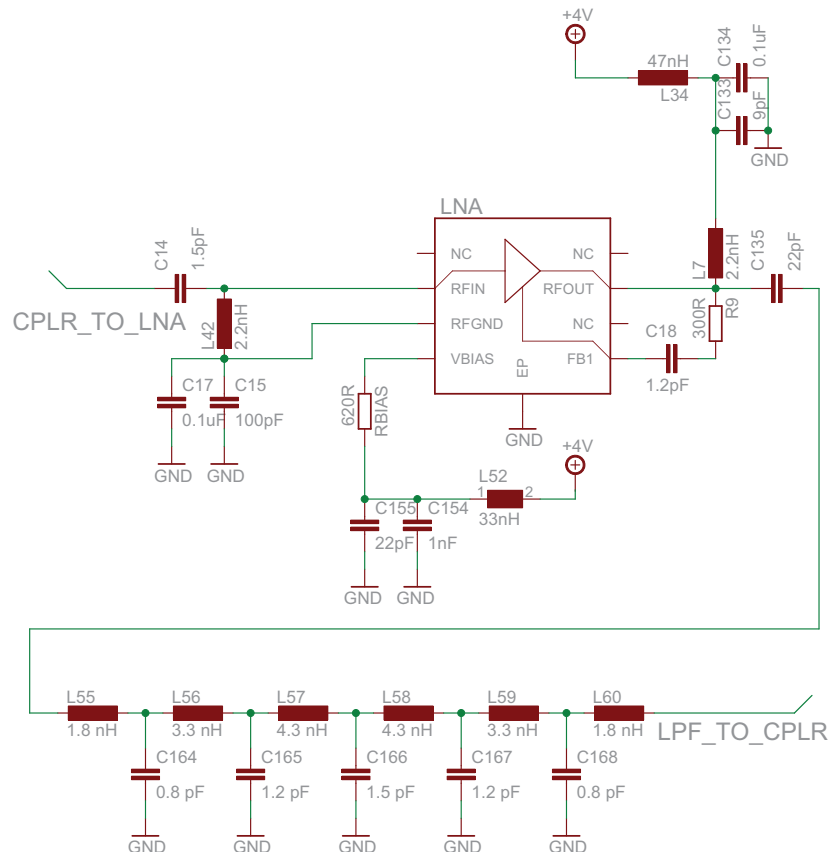
Figure 4.2: Low noise amplifier and 11th order low pass filter schematic of the receiver

After the LNA the signal is filtered by the designed low pass filter, LPF 2, described in Section 3.3.3. This filter shown in Figure 4.2 is composed by the inductors L55 to L60 and the capacitors C164 to C168. At the output of this filter, the power of the signal is

measured. Depending on the power level of the received signal, the receiver then, can be configured to a certain overall gain.

To measure the power level at this point of the receiver chain a power detector circuit as shown in Figure 4.3 is implemented. Again the coupler from Minicircuits, the BDCA1-7-33+ called RX_CPLR2 is used to extract a sample of the RF signal which is further split up by a 3 dB coupler also drawn in Figure 4.3. At both couplers the reverse coupled outputs are terminated to 50 Ω by two paralell 100 Ω resistors (R28 and R53 at RX_CPLR2 and R10 and R11 at the 3 dB coupler). The 3 dB coupler output, the output pin OUT2, is connected to the PWR_DET_4 power detector. Here, the power is measured and the power detector output is used by the microncontroller to adjust externally the overall receiver gain[1] and used in the protection circuit to shutdown the system when the input power level reaches a critical value. Furthermore, the output pin OUT1 of the 3 dB coupler can be used as test point.
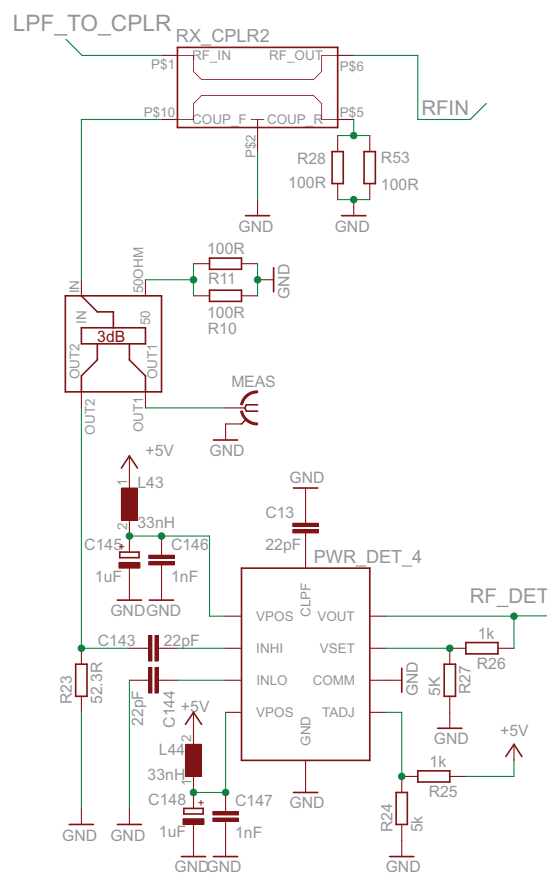
Figure 4.3: Power detector schematic of the receiver

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[1]If the microcontroller is not used, then the receiver overall gain is manually adjusted by the onboard jumpers in the control circuit.

The power detector employed is an ADL5513 from Analog Devices specified for operation up to 4 GHz. The input is AC coupled by means of the capacitor C143 and an external 52.3 Ω shunt resistor gives an adequate broadband 50 Ω match at this pin. A voltage of 5 V is supplied to the two VPOS pins of the IC drawn in Figure 4.3. Furthermore, at these pins are connected two shunt capacitors (C148 and C147 for one pin and C145 and C146 for the other pin) and a choke inductor at each pin to avoid RF leakage into the power supply circuit. Finally, the CPLF pin is unconnected and free of any stray capacitance obtaining a 10 MHz output video bandwidth. Nevertheless, in order to be able to reduce this value a capacitor, C13, can be placed for this purpose.

4.1.2.   Switchable RF block gain and low pass filter stage

After the coupler RX_CPLR2 the signal is amplified and filtered. A switchable RF gain block, shown in Figure 4.4, allows to select between an amplified path and a non amplified path and is controlled by the switches SWITCH_C1 and SWITCH_C2. The amplified path is composed by an MGA-30216 amplifier from Avago Technologies, the RX_AMP, and a 11th order low pass filter, LPF 3, as the described in Section 3.3.3.
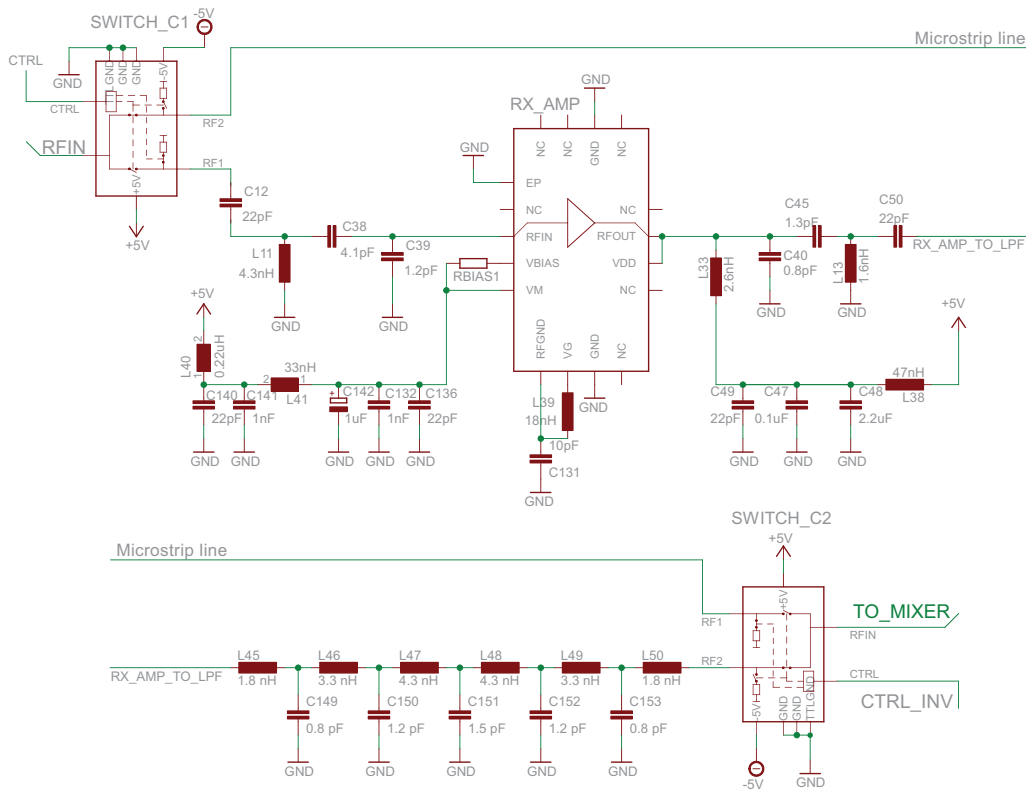
Figure 4.4: Schematic of the receiver switchable RF gain block

At the amplifier, L11, C38 and C39 form the input matching network and C50, L13, C45, C40 and L33 the output matching network to optimize the amplifier performance. This device is supplied by two 5 V biasing lines. At the output pin RFOUT, the inductance L38 provides high impedance at high frequencies decoupling the 5 V biasing line from RF signals. Furthermore, the capacitor C48 filters low frequencies, C47 medium frequencies

and C49 high frequencies. The second 5 V biasing line is connected to the pin VBIAS. Here, a similar bias filtering network filters low, medium and high frequencies by means of C132, C136, C142 and the inductor L41. Nevertheless, at this filtering network, there is an additional AC decoupling stage composed by C141, C140 and L40 which enhances the RF decoupling from the supply circuit. The amplifier is followed by an LPF, the LPF 3, and then the amplified and then non amplified paths merge together at the second switch SWITCH_C1. Both switches are of the same type as used for the switchable BPF. Again the RF1 and RF2 are interchanged for layout considerations and controlled by a similar circuit as used at the switchable BPF.

4.1.3.   Downconversion and output stage

To downconvert the received signal from the frequency of 2.45 GHz to the IF1 frequency of 140 MHz a mixer from Maxim, the MAX2043 is used. This device, called RX_MIXER in the Figure 4.5, is a passive double balanced mixer which integrate BALUNS[2] at the RF and LO ports, a selectable dual LO input, composed by the LO1 pin and the LO2 pin, and an LO buffer amplifier. The onchip integrated BALUN's and matching circuitry of the mixer allow for 50 Ω single ended LO inputs and a 50 Ω single ended RF input for downconversion (or RF output for upconversion) requiring no external matching components. Only, the AC coupling capacitors C19, C20 and C21 are required to filter possible DC currents from the previous and the next elements in the chain because the mixer's input is internally DC shorted to ground through the onchip BALUN [14].

At the differential IF port IF+ and IF- of the mixer, an external BALUN is connected to transform the differential mixer output to single ended. For this purpose the 1:1 transformer ETC1-1T-5 from M/A-COM in Figure 4.5 called T1, is employed. The capacitor C37 is placed for AC coupling the transformer's output.

Due to the positioning of the LO inputs of the mixer, the SMA connector "LO2" which provides from an external generator the second LO signal, LO2 of 2.59 GHz, is connected to the LO1 pin of the mixer to avoid lines intersections. The LO2 pin of the mixer is not employed. For this reason, this pin is terminated into a 50 Ω resistor, R8. This device is supplied with a voltage of 5 V through a similar bias filtering network as the RX_AMP to decouple the supply circuit from the RF path. However, due to the pin positions of the IC[3] the mixer's supply filtering network is divided into two parts: The M_VCCUP filtering network, which supplies the right and the top VCC pins, and the M_VCCDWN filtering network which supplies the left and the bottom VCC pins.

With the 2.45 GHz RF signal converted to the IF1 frequency, the mixer output is connected by means of the connector "X2" to the IF stage where the signal is further processed and then provided to the ADC of the Rapid Prototyping Board.

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[2]BALanced UNbalanced lines transformer
[3]Integrated Circuit
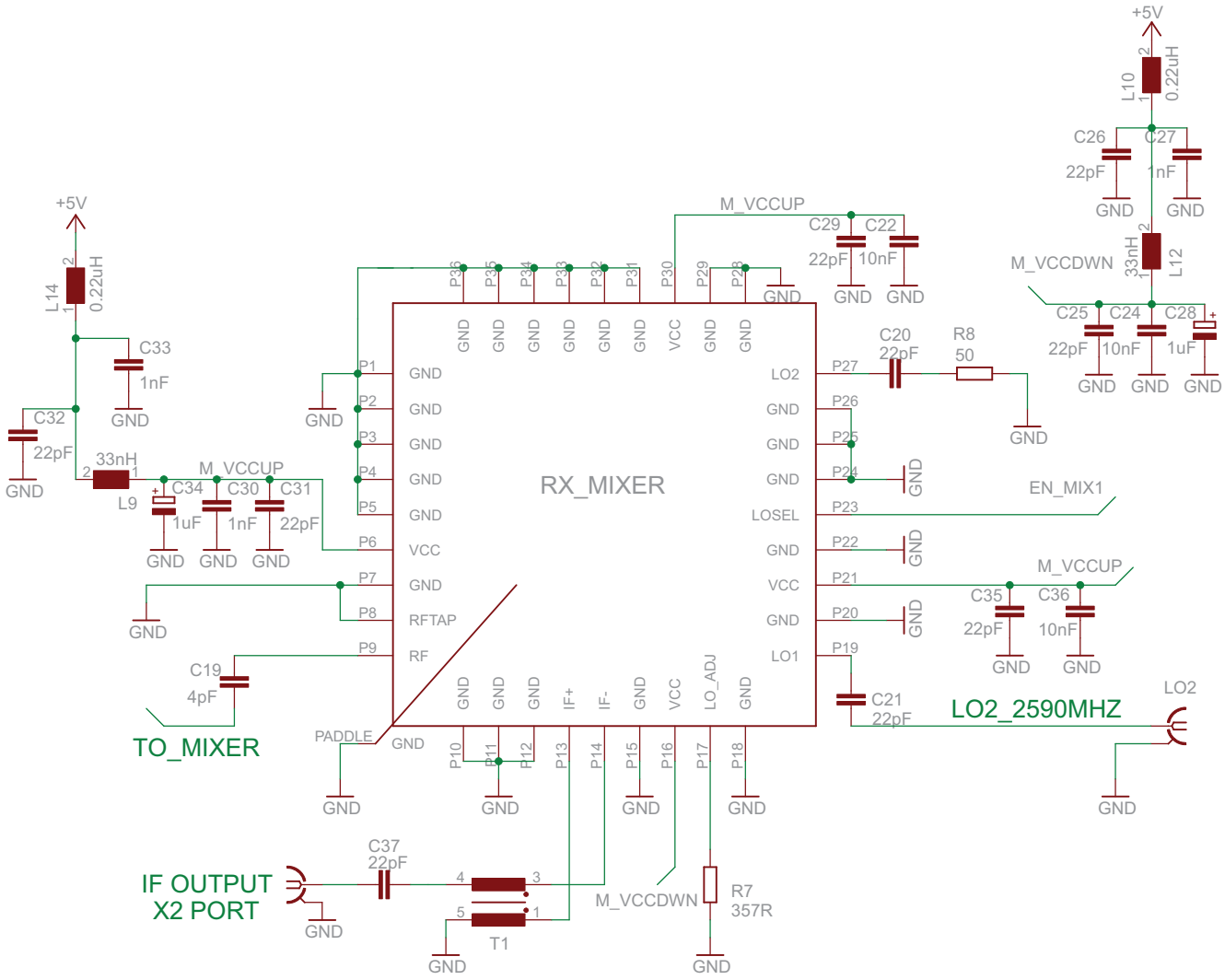
Figure 4.5: Schematic of the receiver mixer in downconversion mode

4.1.4. Power supply and control circuits

The receiver board is designed for a dual supply voltage of $\pm10\,V$ that is connected to the unit through a male 25 pin Sub-D connector, the "X1" connector, which also provides control and monitoring lines. The connector and the power supply input circuit is drawn in Figure 4.6.
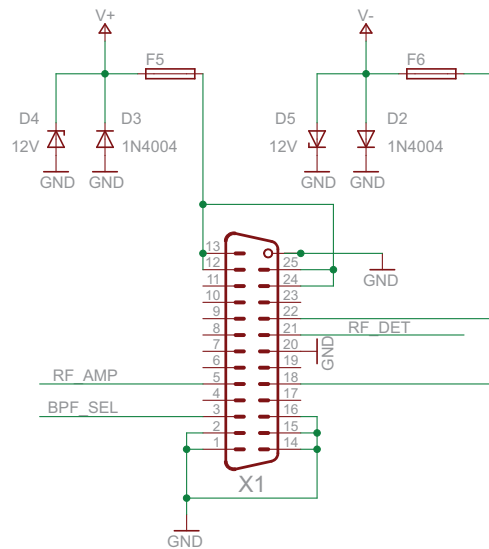
Figure 4.6: Control and voltage supply main connector of the receiver

The pins 11-13, 24 and 25 are connected to the internal positive supply lines through an 1 A fuse, F5. The pins 18 and 22 are connected to the internal negative supply lines through an 1 A fuse, F6. The circuit is further protected by the diodes D3 and D4 in the positive line and by the diodes D2 and D5 in the negative line. All diodes conduct if the polarity of the supply voltage is reversed. The Zener diodes D4 and D5 also starts conducting when the supply voltage reaches levels above $\pm12\,V$. In both cases F5 and F6 blow and prevent further damage in the receiver board.

The majority of the components used for the receiver require a supply voltage of 5 V which is obtained by the linear voltage regulator MC7805ABD2T shown in Figure 4.7a. This linear regulator is implemented following the datasheet application note [18]. In order to decrease the IC heat dissipation the input voltage of the voltage regulator is reduced to 9 V by the resistors R48, R49, R50 and R52. The supply voltage of $-5\,V$ for the RF switches is obtained by a MC79M05 linear regulator and the supply voltage of 4 V for the LNA is obtained by the LM317MSTT3 linear regulator shown in Figure 4.7b.

In Figure 4.8 the control circuit which controls the switches SWITCH_B1 and SWITCH_B2 for the BPF selection is shown. Due to the switches layout, to achieve the same selected path at both switches one of them is inverted. It means that the pin RF1 at the SWITCH_B1 is connected to the pin RF2 at the SWITCH_B2, so also it is necessary to invert the control lines. Therefore, two control lines are required, one line for each switch realized by the transistors T2 and T5 as drawn in Figure 4.8. Nevertheless, to control both switches remotely by means of a microcontroller the BPF_SEL line is used. However, also it is possible to control manually by means of the jumper JP1.

(a) 5V linear regulator

(b) 4V linear regulator
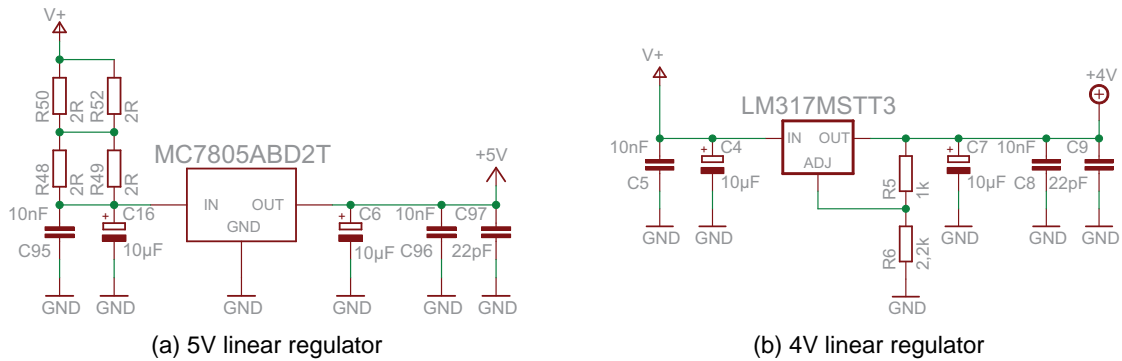
Figure 4.7: Voltage supply of the receiver

When the control line BPF_SEL is set to 5 V, logical "high", the NPN transistor, T2, is switched on and provides GND, logical "low", to the TTL_CTRL_INV_A line and the PNP transistor, T5. This second transistor T5 is also switched on and provides 5 V to the TTL_CTRL_A line. Then, the onboard BPF is selected and the LED1 indicates the selection of the onboard filter. In the same Figure 4.8 the LED4 indicates the presence of the 5 V supply voltage.
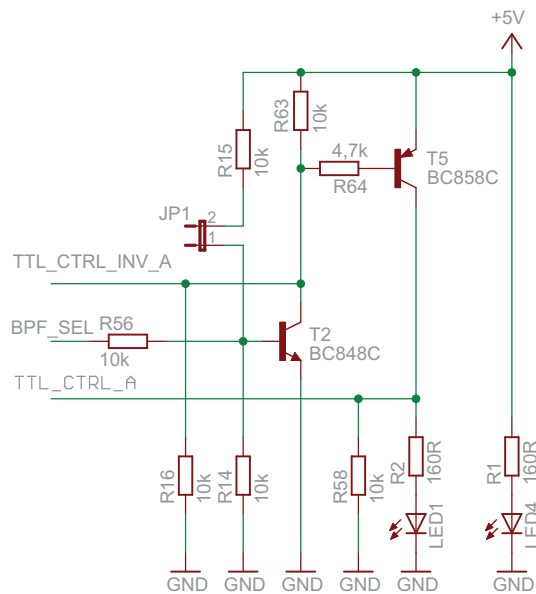
Figure 4.8: Receiver band pass filter control schematic

Keeping the compatibility with the previous designs [8] [9], to manually configure the receiver gain, as in the UHF board, the same 16 pin connector SV1 is used. Also, as already explained, the board has the pin JP1 to control the BPF selection. Table 4.1 gives a summary of the control lines, their function, logical activation level and the controlled stage.

Table 4.1: Receiver control lines

Pin SV1	Pin X1	Element/Function	Active on	Controlled stage
-	-	JP1, BPF selection	H	2.45 GHz stage
1	-	Shutdown	L	Both stages
3	17	10 dB attenuator	H	IF stage
5	5	RF gain block	L	2.45 GHz stage
7	6	VGA 16 dB att.[4]	H	IF stage
9	7	VGA 8 dB att.	H	IF stage
11	8	VGA 4 dB att.	H	IF stage
13	9	VGA 2 dB att.	H	IF stage
15	10	VGA 1 dB att.	H	IF stage

Figure 4.9 shows the control circuit for the switchable RF gain block. This circuit can be controlled by an external microcontroller by means of the input RF_GAIN_BLOCK or manually controlled with the pin 3 of the SV1 connector by the line RF_GAIN_BLOCK_JP. As occurs in the switches for the BPF selection, one of the switches is inverted so it is necessary also to invert one of the output control lines of this control circuit.
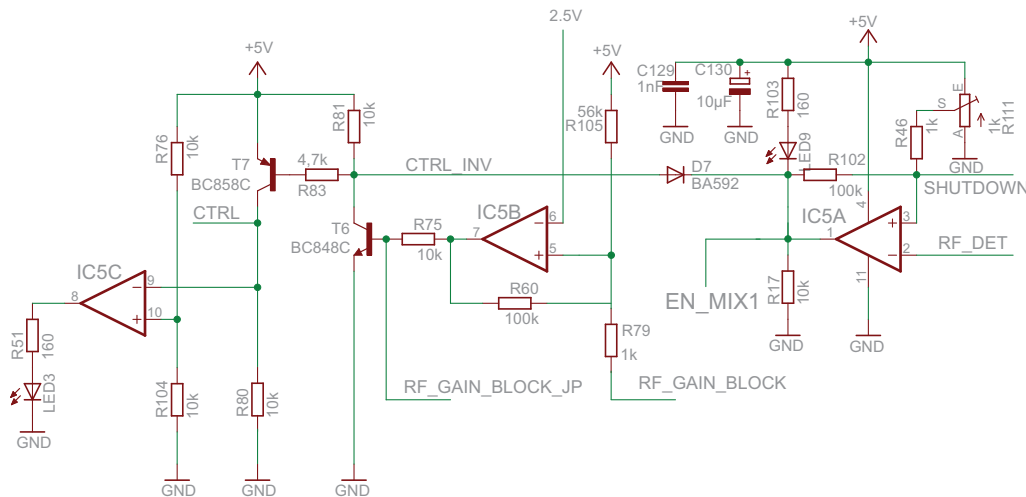
Figure 4.9: Shutdown and switchable RF gain block control schematic of the receiver

The IC5B, drawn in Figure 4.9, acts as a buffer amplifier and adds a small switching hysteresis. The output of this buffer amplifier is controlled by the line RF_GAIN_BLOCK. This output is then fed in a switch which is implemented by a transistor, T6, and then, to an inverter switch implemented by the transistor T7. IC5C monitors the CTRL input line and drives a LED when the switchable RF gain block is inserted in the signal path by the RF switches.

A protection circuit is implemented using IC5A. The output voltage of the RF power detector RF_DET is compared with an adjustable voltage derived from R111 or the SHUTDOWN line. When the input power reaches the level set by R111 or the SHUTDOWN line is low, IC5A pulls the mixer enable lines low, D7 starts to conduct and turns off the switchable RF

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[4]The use of the VGA 16 dB attenuator disables the VGA 8 dB attenuator automatically

gain block which contains the RX_AMP. The red LED, LED9 indicates the overload status.

Although when the protection circuit is tripped and the shutdown circuit gives an optical alarm, and shuts down some elements for protection, it can not prevent the destruction of the LNA, the RF switches and the BPF when the RF input power is further increased above the maximum ratings.

4.2. Power level plan

As described in Section 2.2.2. besides the backscattered signals, there is a strong carrier crosstalk from the transmitter module at the receiver input. Due to this strong carrier crosstalk, the receiver input power at the antenna connector depends on the carrier suppression if the CCU is used, and on the transmitter to receiver isolation.

Linear operation in the receiver's devices is possible up to an input power of 8 dBm. To do not exceed this input power level if the carrier compensation unit is omitted, a minimum TX–RX isolation of 28 dB is required when the transmitter operates with a power of 36 dBm. However, the absolute maximum input power without damaging any component is 15 dBm. For this input power a minimum TX–RX isolation of 21 dB and the lowest gain configuration of the receiver is required. Table 4.2 specifies for each receiver gain configuration the minimum isolation required to do not overload the ADC of the Rapid Prototyping Board. Nevertheless, if the minimum TX–RX isolation is not achieved, the shutdown system prevents from system overloads when the input power exceeds the maximum input power.

To calculate these values, a detailed power level plan which registers the power level at each receiver device has been created. In Figure 4.10 for low gain and in Figure 4.12 for high gain, the power level plan gives the gain, the noise figure, the output 1 dB compression point, and the absolute maximum output power for every receiver stage.

In both figures, the input signal is decomposed into two parts: The leaking carrier component and the modulated signal component. While the carrier component depends on the transmit power and the transmitter–receiver isolation, the modulated signal component depends on the transmit power, the tag antenna size, orientation and reader–tag distance. The signal and noise level at every stage were calculated with an effective bandwidth of 5 MHz. This bandwidth corresponds to the 140 MHz IF SAW filter at the IF stage which delimits the overall selectivity of the frontend. To illustrate the effect of the carrier leakage a weak data signal of −80 dBm was assumed in both power level plans and a transmit power level of 36 dBm.

Figure 4.10a and Figure 4.10b show the power level plan of the receiver in the linear operation boundary. In this situation the input power at the receiver is 8 dBm which corresponds to a minimum TX–RX isolation of 28 dB. In this configuration, the lower gain configuration for linear operation, the switchable RF gain block is switched off, the 10 dB attenuator is switched on and the VGA's attenuator is set to −15 dB, achieving at the output of the frontend a power level of 12 dBm which fully modulates the ADC and do not exceed the 12.6 dBm limit.

	Start	Switch B1	RX BPF	Switch B2	RX CPLR1	LNA	LPF 2	RX CPLR2	Switch C1	RX Amp	LPF 3	Switch C2	RX Mixer	Filter	ATT Sw.	10dB ATT	IF Amp1	Filter	var ATT2	IF Amp2	Coupler	2nd Mixer	LPF	Amplifier
		2.45 GHz Board												140 MHz								13.56 MHz		
Gain / dB		-1,4	-1,8	-1,4	-1,6	15,3	-0,8	-1,6	-1,4	0	0	-1,4	-7,8	-0,5	-0,8	-10	20	-13	-15	15,5	-0,5	2	-0,5	11
F / dB		1	1,8	1	1,6	0,95	0,8	1,6	1	0	0	1	8,3	0,5	0,8	10	2,7	13	15	4,7	0,5	10,3	0,5	1,23
Signal / dBm	-80,00	-81,40	-83,20	-84,60	-86,20	-70,90	-71,70	-73,30	-74,70	-74,70	-74,70	-76,10	-83,90	-84,40	-85,20	-95,20	-75,20	-88,20	-103,20	-87,70	-88,20	-86,20	-86,70	-75,70
Carrier / dBm	8,00	6,60	4,80	3,40	1,80	17,10	16,30	14,70	13,30	13,30	13,30	11,90	4,10	3,60	2,80	-7,20	12,80	-0,20	-15,20	0,30	-0,20	1,80	1,30	12,30
S/I / dB	-88,00	-88,00	-88,00	-88,00	-88,00	-88,00	-88,00	-88,00	-88,00	-88,00	-88,00	-88,00	-88,00	-88,00	-88,00	-88,00	-88,00	-88,00	-88,00	-88,00	-88,00	-88,00	-88,00	-88,00
Noise / dBm	-106,99	-107,39	-107,25	-107,59	-107,40	-91,06	-91,84	-93,38	-94,73	-94,73	-94,73	-96,07	-102,21	-102,53	-103,03	-106,39	-83,95	-96,56	-105,79	-86,34	-86,84	-84,45	-84,95	-73,94
SNR / dB	26,99																							
NF	1,00	1,26	1,97	2,51	3,79	4,81	4,84	4,90	4,96	4,96	4,96	5,04	7,38	7,68	8,24	38,04	66,59	72,86	275,19	682,85	683,57	747,76	748,27	749,80
NF / dB	0,00	1,00	2,94	3,99	5,79	6,82	6,85	6,91	6,95	6,95	6,95	7,02	8,68	8,85	9,16	15,80	18,23	18,63	24,40	28,34	28,35	28,74	28,74	28,75
SNR / dB	26,99	25,99	24,05	22,99	21,20	20,16	20,14	20,08	20,03	20,03	20,03	19,97	18,31	18,13	17,83	11,19	8,75	8,36	2,59	-1,36	-1,36	-1,75	-1,75	-1,76
1dB out comp. / dBm	47	23,60	24,20	23,30	30,00	18,50	25,00	30,00	23,30	30,00	25,00	23,30	14,20	25,00	17,00	30,00	19,60	23,00	5,10	20,60	25,00	12,50	25,00	17,50
Abs. max. output /d B	39	24,00	25,20	24,00	45,00	35,00	30,00	45,00	24,00	36,00	30,00	24,00	20,00	25,00	18,00	30,00	38,00	25,00	5,10	30,00	47,00	13,00	25,00	12,60
Cumulative Gain / dB	0	-1,4	-3,2	-4,6	-6,2	9,1	8,3	6,7	5,3	5,3	5,3	3,9	-3,90	-4,40	-5,20	-15,20	4,80	-8,20	-23,20	-7,70	-8,20	-6,20	-6,70	4,30
Manufacturer		Mini-Circuits	Epcos	Mini-Circuits	MiniCircuits	Avago	LPF	MiniCircuits	Mini-Circuits	AVAGO	LPF	Mini-Circuits	Maxim	LPF			AD	Telefilter	MAXIM		MiniCircuits	Linear Tech.	LPF	AD8045
Device		SWMA-2-50DR+	B9430	SWMA-2-50DR+	BDCA1-7-33+	MGA-632P8	Selfmade	BDCA1-7-33+	SWMA-2-50DR+	MGA-30216	Selfmade	SWMA-2-50DR+	MAX2043	Selfmade		HMC541LP3	ADL5542	TFS140AV	MAX2027		ADC-10-1R	LT5512	Selfmade	OPV

Bandwidth / Hz	5,00E+06
Tr / K	2,90E+02
TX-RX Isolation	28
NO CCU	

Figure 4.10: Receiver power level plan low gain configuration

(a)

(b)

Legend:
- Output 1dB compression point / dBm.
- Signal / dBm
- Carrier / dBm
- Abs. max. output / dBm

In this configuration, the calculated noise figure at the end of the frontend is 28.75 dB. This value exceeds the maximum noise figure F of 27 dB calculated in Section 2.2.1. corresponding to the maximum distance range of the reader. However, this low gain configuration is useful to receive the backscattered signal when the tag is not at the maximum distance range of 8.70 m and there is a high crosstalk component at the antenna connector which requires the lowest gain configuration to attenuate the RF input power.

Figure 4.11 shows how the noise figure increases through the receiver chain. The devices which influence the noise figure most are easily identified in Figure 4.11. These elements are the 10 dB switchable attenuator and the VGA set to -15 dB gain, both in the IF stage. But also the absence of amplification at the RF stage favors this high noise figure result. However, in this configuration, it is not possible to turn on the RF amplifier or decrease the attenuation value at the VGA, otherwise the following receiver stages would be overloaded.
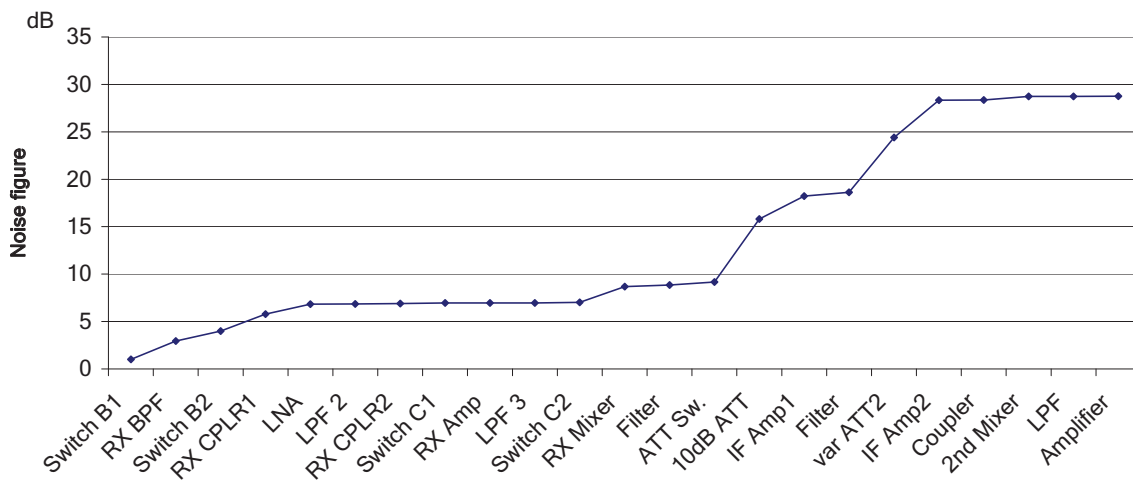
Figure 4.11: Noise figure plan of the receiver at the lowest gain configuration

In the opposite situation, when the receiver is working at the maximum gain configuration, the use of the CCU is necessary in order to suppress the leaking carrier. Otherwise, a really high transmitter to receiver isolation of 64 dB is required. In Figure 4.12a and in Figure 4.12b the power level plan is shown at the high gain configuration assuming a TX–RX isolation of 64 dB which provides an equivalent input power of -28 dBm at the receiver's input. In this configuration, the switchable RF gain block is switched on, the 10 dB attenuator is switched off and the VGA's attenuator is set to 0 dB, achieving the maximum receiver gain with a calculated noise figure of $F = 7.7$ dB. The RF amplifier of the switchable RF gain block, placed at the beginning of the receiver chain, improves considerately this noise figure result. Figure 4.13 shows the influence of the components in terms of noise for this high gain configuration. Now, the devices that contribute mostly to increase the noise figure are the switches to exchange the BPF, the BPF itself, the first coupler and the LNA. Therefore, to improve this value it is only possible by substituting this devices by lower loss types.

	Start	Switch B1	RX BPF	Switch B2	RX CPLR1	LNA	LPF 2	RX CPLR2	Switch C1	RX Amp	LPF 3	Switch C2	RX Mixer	Filter	ATT Sw.	10dB ATT	IF Amp1	Filter	var ATT2	IF Amp2	Coupler	2nd Mixer	LPF	Amplifier
														140 MHz								**13.56 MHz**		
Gain / dB		-1,4	-1,8	-1,4	-1,6	15,3	-0,8	-1,6	-1,4	11,8	-0,8	-1,4	-7,8	-0,5	-0,8	0	20	-13	0	15,5	-0,5	2	-0,5	11
F / dB		1	1,8	1	1,6	0,95	0,8	1,6	1	2,8	-0,8	1	8,3	0,5	0,8	0	2,7	13	0	4,7	0,5	10,3	0,5	1,23
Signal / dBm	-80,00	-81,40	-83,20	-84,60	-86,20	-70,90	-71,70	-73,30	-74,70	-62,90	-63,70	-65,10	-72,90	-73,40	-74,20	-74,20	-54,20	-67,20	-67,20	-51,70	-52,20	-50,20	-50,70	-39,70
Carrier / dBm	-28,00	-29,40	-31,20	-32,60	-34,20	-18,90	-19,70	-21,30	-22,70	-10,90	-11,70	-13,10	-20,90	-21,40	-22,20	-22,20	-2,20	-15,20	-15,20	0,30	-0,20	1,80	1,30	12,30
S/I / dB	-52,00	-52,00	-52,00	-52,00	-52,00	-52,00	-52,00	-52,00	-52,00	-52,00	-52,00	-52,00	-52,00	-52,00	-52,00	-52,00	-52,00	-52,00	-52,00	-52,00	-52,00	-52,00	-52,00	-52,00
Noise / dBm	-106,99	-107,39	-107,25	-107,59	-107,40	-91,06	-91,84	-93,38	-94,73	-82,71	-83,51	-84,90	-92,55	-93,03	-93,80	-93,80	-73,62	-86,58	-86,58	-71,01	-71,51	-69,49	-69,99	-58,99
SNR / dB	26,99																							
NF	1,00	1,26	1,97	2,51	3,79	4,81	4,84	4,90	4,96	5,23	5,22	5,23	5,42	5,44	5,48	5,48	5,71	5,76	5,76	5,86	5,86	5,88	5,88	5,88
NF / dB	0,00	1,00	2,94	3,99	5,79	6,82	6,85	6,91	6,95	7,18	7,18	7,18	7,34	7,36	7,39	7,39	7,57	7,60	7,60	7,68	7,68	7,69	7,69	7,69
SNR / dB	26,99	25,99	24,05	22,99	21,20	20,16	20,14	20,08	20,03	19,81	19,81	19,80	19,65	19,63	19,60	19,60	19,42	19,38	19,38	19,31	19,31	19,29	19,29	19,29
1dB out comp. / dBm	47	23,60	24,20	23,30	30,00	18,50	25,00	30,00	23,30	30,00	25,00	23,30	14,20	25,00	17,00	30,00	19,60	23,00	5,10	20,60	25,00	12,50	25,00	17,50
Abs. max. output /d B	39	24,00	25,20	24,00	45,00	35,00	30,00	45,00	24,00	36,00	30,00	24,00	20,00	25,00	18,00	30,00	38,00	25,00	5,10	30,00	47,00	13,00	25,00	12,60
Cumulative Gain / dB	0	-1,4	-3,2	-4,6	-6,2	9,1	8,3	6,7	5,3	17,1	16,3	14,9	7,10	6,60	5,80	5,80	25,80	12,80	12,80	28,30	27,80	29,80	29,30	40,30
Manufacturer		Mini-Circuits	Epcos	Mini-Circuits	MiniCircuits	Avago	LPF	MiniCircuits	Mini-Circuits	AVAGO	LPF	Mini-Circuits	Maxim	LPF			AD	Telefilter	MAXIM		MiniCircuits	Linear Tech.	LPF	AD8045
Device		SWMA-2-50DR+	B9430	SWMA-2-50DR+	BDCA1-7-33+	MGA-632P8	Selfmade	BDCA1-7-33+	SWMA-2-50DR+	MGA-30216	Selfmade	SWMA-2-50DR+	MAX2043	Selfmade		HMC541LP3	ADL5542	TFS140AV	MAX2027		ADC-10-1R	LT5512	Selfmade	OPV

*Columns Start through RX Mixer belong to the **2.45 GHz Board**; Filter through IF Amp2 to **140 MHz**; 2nd Mixer through Amplifier to **13.56 MHz**.*

Bandwidth / Hz 5,00E+06
Tr / K 2,90E+02
TX-RX Isolation 64
NO CCU

Figure 4.12: Receiver power level plan high gain configuration

(a)

(b)

Figure 4.13: Noise figure plan of the receiver at the highest gain configuration

In Table 4.2 different receiver configurations are listed for different transmitter to receiver isolations values without using a carrier compensation unit. The first column of the Table 4.2 lists the TX–RX isolation, the second column lists the leaking carrier or equivalent input power at the receiver input. With this input power, the receiver is set to an optimum gain configuration that achieves the maximum frontend output in order to fully modulate the ADC without exceeding the limitation of 12.6 dBm. Next columns show the status for the switchable RF gain block, the switchable 10 dB attenuator and the VGA's settings. Finally, the last column of Table 4.2 shows for each receiver configuration the obtained noise figure. It is important to remark that this values are obtained without using a carrier compensation unit. Using a carrier compensation unit allows to obtain a lower noise figure and a lower TX–RX isolations requirements.

Table 4.2: Gain settings and noise figures (F) of the receiver and the corresponding necessary minimum TX – RX isolation without carrier suppression at a TX power of 36 dBm.

TX–RX isolation /dB	Equiv. input power /dBm	RX Amp.	10 dB-Att.	VGA Att. Setting /dB	F /dB
21	15	off	on	-22	35.4
23	13	off	on	-20	33.5
25	11	off	on	-18	31.6
27	9	off	on	-16	29.7
29	7	off	on	-14	27.9
31	5	on	on	-23	25.5
33	3	on	on	-21	23.6
35	1	on	on	-19	21.6
37	-1	on	on	-17	19.8
39	-3	on	on	-15	18.1
41	-5	on	off	-23	16.0
44	-8	on	off	-20	13.6
49	-13	on	off	-15	10.5
54	-18	on	off	-10	8.7
59	-23	on	off	-5	8.0
64	-28	on	off	0	7.7

4.3. Measurements

Based on the already implemented test circuits a receiver prototype was implemented. This prototype receiver contains all relevant parts configured at the maximum gain without the switching possibilities of the receiver. Figure 4.14 shows the blockdiagram of this receiver prototype. To characterize this receiver the frequency response and linearity are measured.

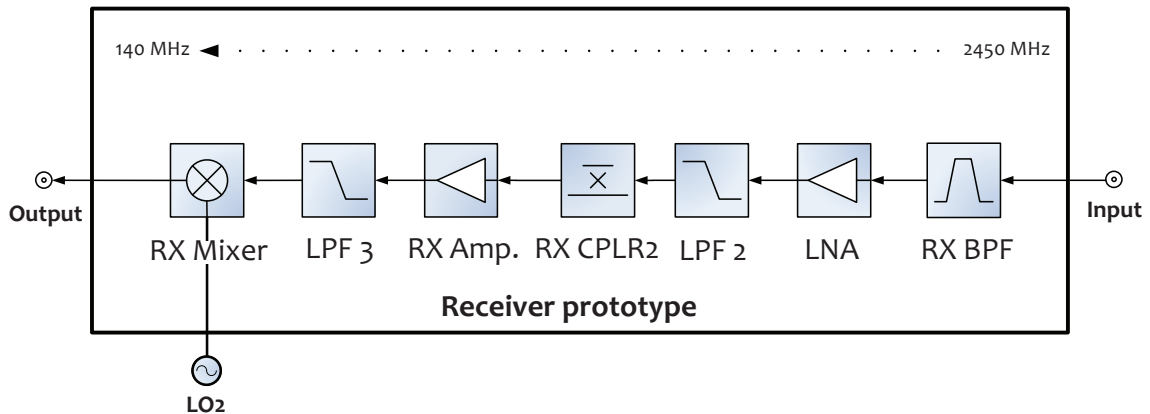Figure 4.14: Receiver prototype for measurements

4.3.1. Frequency response

The measured frequency response provides the gain, the bandwidth and flatness of the receiver bandpass frequency. As shown in Figure 4.15 a 4 ports vector network analyzer[5] was employed to obtain this measurement.
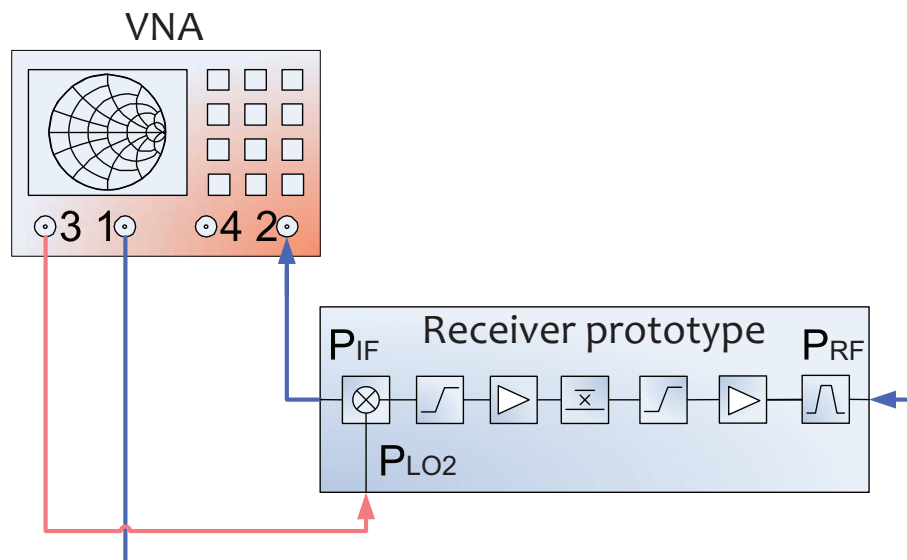

Figure 4.15: Measurement setup for the frequency response of the receiver

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[5]ZVA8 from Rhode & Schwarz

This VNA[6] provides two individual signal generators at port 1 and port 3. As shown in Figure 4.15 one generator can be used as the RF input signal for the prototype and the other one as the second LO at the frequency of 2590 MHz.

Table 4.3 summarizes the frequency sweep for the different VNA ports and indicates the frequency bands of interest for the measurement. In order to obtain a broadband measurement at the low side band[7], port 1 sweeps from 300 kHz[8] to 2589.7 MHz[9]. Due to the importance of suppressing the image frequency, the upper side band frequency response is also measured. For this measurement, the port 1 sweep is reconfigured to the image frequency band from 2590.3 MHz to 5 GHz .

Table 4.3: Port and frequency definition for the measurements

Port	Use	Value	Measured band	Unit
ZVA8 port 1	LSB[11] RF output	0.3- 2589.7	2400- 2483	MHz
ZVA8 port 1	USB[12] image output	2590.3 - 5000	2697- 2780	MHz
ZVA8 port 2	IF input	0.3- 2589.7	107 - 190	MHz
ZVA8 port 3	LO2 output	2590	-	MHz

The LSB frequency response shown in Figure 4.16 gives the conversion gain of the receiver prototype at the IF frequency band, 107 MHz-190 MHz, which corresponds to the downconverted 2400 MHz-2483 MHz RF frequency band.

The expected gain of the prototype at this frequency band is 13.2 dB. This value is calculated using for each component of the prototype the same value of gain as in the power level plan in Section 4.2. Finally, as shown in Figure 4.16 the measured gain of 12.9 dB fits very well with the expected value of 13.2 dB and furthermore a small flatness deviation of 0.8 dB is achieved at the measured band.

The frequency response shown in Figure 4.17 gives the conversion gain of the receiver prototype for the USB. Here the measured conversion gain of -12.5 dB at the 107 MHz-190 MHz frequency band corresponds to the image frequency band of 2697 MHz-2780 MHz.

Now, the difference between the conversion gain of 12.9 dB in the LSB, and the conversion gain of -12.5 dB in the USB at the desire IF band, is the total image frequency suppression in this band. This suppression is 25.5 dB.

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[6]Vector Network Analyzer
[7]Lower than the LO2 frequency
[8]The minimum possible frequency generated by the VNA
[9]The closest possible frequency to the LO2 frequency
[11]Lower Side Band
[12]Upper Side Band
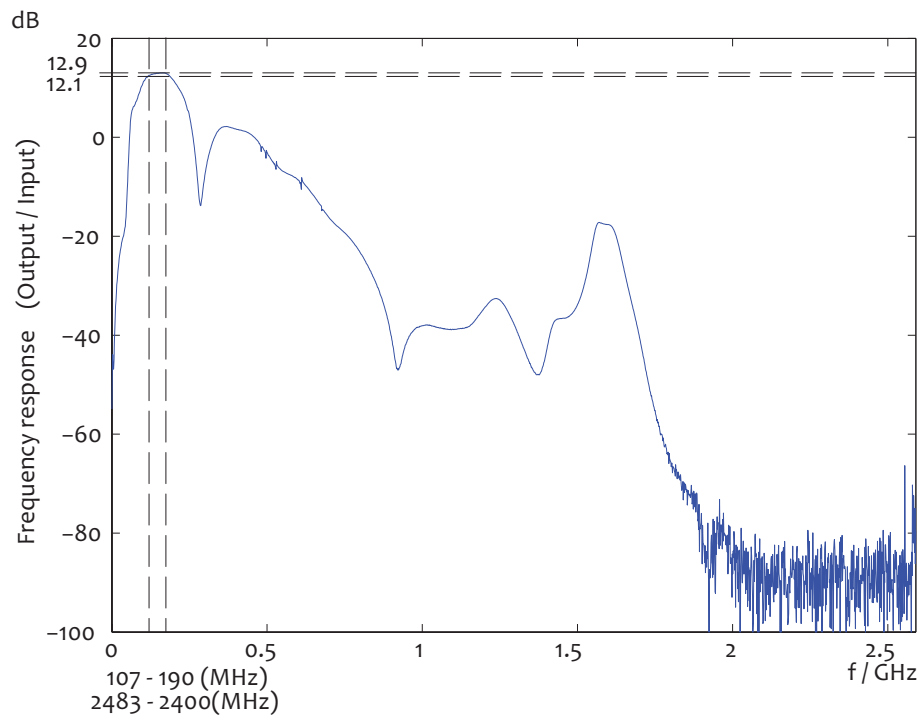
Figure 4.16: Measured LSB frequency response
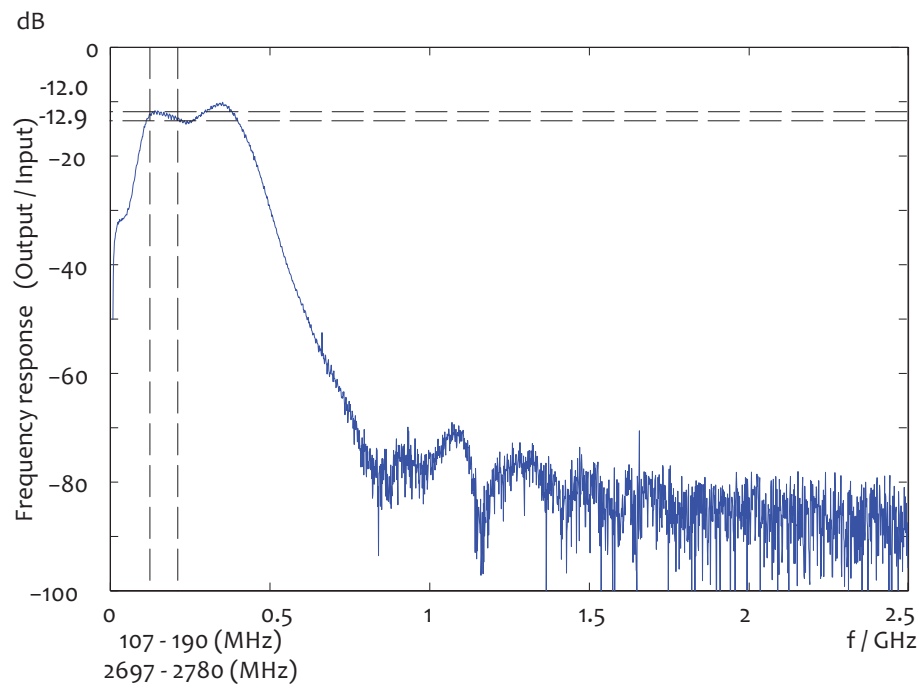
Figure 4.17: Measured USB frequency response

4.3.2. Powersweep

The powersweep measurement indicates the point where the receiver's components start to compress the power level of the signal. At high input levels some devices goes into saturation and its gain decreases. Typicaly, when the gain decrease 1 dB, this point is called 1 dB compression point and the output power level is 1 dB below the expected power level.

For this measurement, the same measurement setup as in the frequency response is employed. However, some internal configuration of the VNA are modified. While the port 1 frequency is set to a constant output frequency of 2450 MHz the output power of this port sweeps from -25 dBm to -5 dBm.
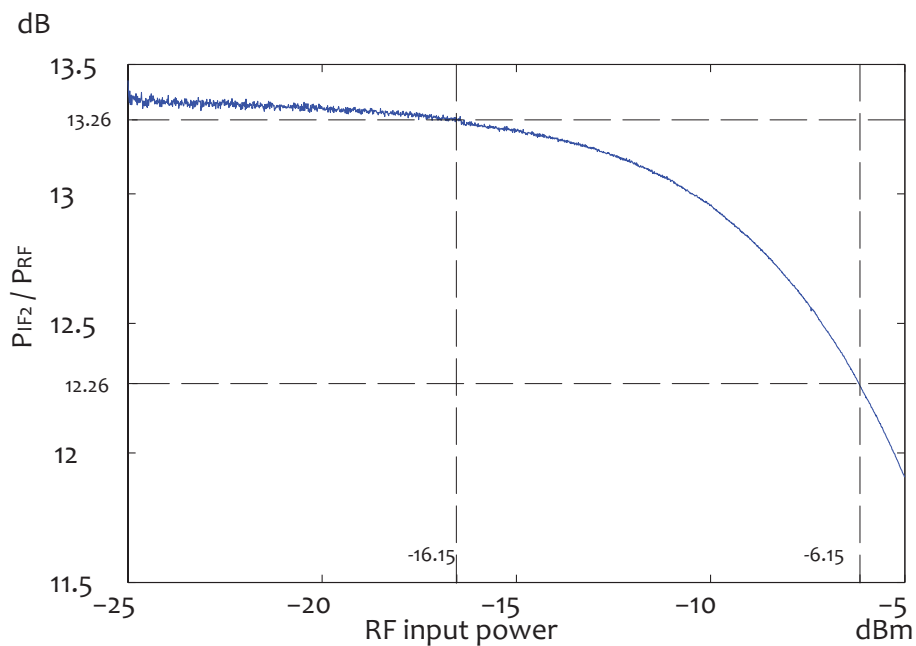
Figure 4.18: Measured 1dB compression point of the receiver

As a result of this measurement, the 1 dB compression point at the input power of -6.15 dBm is shown in Figure 4.18. This limitation is originated in the MAX2043 mixer which has the lower input 1 dB compression point. That value represents the 2.45 GHz receiver stage set to the maximum gain. However, all the passive components not used in this prototype that are placed before the mixer in the receiver board should increase the 1 dB compression point enhancing the behavior of the receiver board.

CHAPTER 5. TRANSMITTER

This chapter describes the 2.45 GHz transmitter circuit designed and built during this master thesis. Also, the power level plan for this board is described and finally the measurement results of the tested transmitter board are shown.

5.1. The 2.45 GHz transmitter circuit

The input signal from the Rapid Prototyping Board is processed in the IF stage and then supplied to the 2.45 GHz transmitter stage. The transmitter IF stage is explained in detail in [9, pag. 28-32]. Due that some of the components in this transmitter board are of the same type as in the receiver board and are designed in the same way as described in Section 4.1. the description of these parts are omitted.

5.1.1. Input and RF conversion stage

The IF2 output signal from the IF stage enters into the 2.45 GHz transmitter stage through the interface "X2" and is then supplied to the mixer, TX_MIXER, as drawn in Figure 5.1. This mixer performs the frequency upconversion from the IF2 frequency f_{IF2} = 140 MHz to the desired output frequency band from 2400 MHz-2483 MHz. As at the receiver the mixer MAX2043 from MAXIM is used. Also the transformer at the differential IF port and the biasing filtering network are as at the receiver. The only difference here is the employed capacitor C3 of 22 pF between the mixer's pins P7 and P8 to reduce the second order intermodulation of the mixer.

The following component is the image rejection filter. The same switchable band pass filter concept as described in Section 4.1.1. is utilized. In Figure 5.1 this stage is composed by the switches SWITCH_A1 and SWITCH_A2 and the BPF TX_BPF from EPCOS. The input and the output matching networks for this filter are already given in Section 3.3.2.

With the IF2 signal upconverted to the RF frequency and filtered, the next component in the signal path is the amplifier TX_AMP drawn in the top of Figure 5.1. This amplifier is an ADL5542 amplifier from Analog Devices. Internally matched to an impedance of 50 Ω this amplifier does not require any external input or output matching network. Only, AC coupling at the input and at the output ports is required. This is realized by the capacitors C13 and C14.

From the linear voltage regulator MC7805ABD2T, shown in Figure 5.4, a voltage of 5 V is supplied to the amplifier via the pin VPOS, and through the biasing inductor L1 connected to the pin RFOUT. The bias voltage at the RFOUT pin is decoupled from the RF path by means of the inductors L13 = 33 nH and L1 = 47 nH and the capacitor C17 = 68 pF for high frequencies, C19 = 1.2 nF for medium frequencies and C16 = 1 μF for low frequencies. A similar bias filtering network composed by C18, C24 and L11 is used for the VPOS pin.
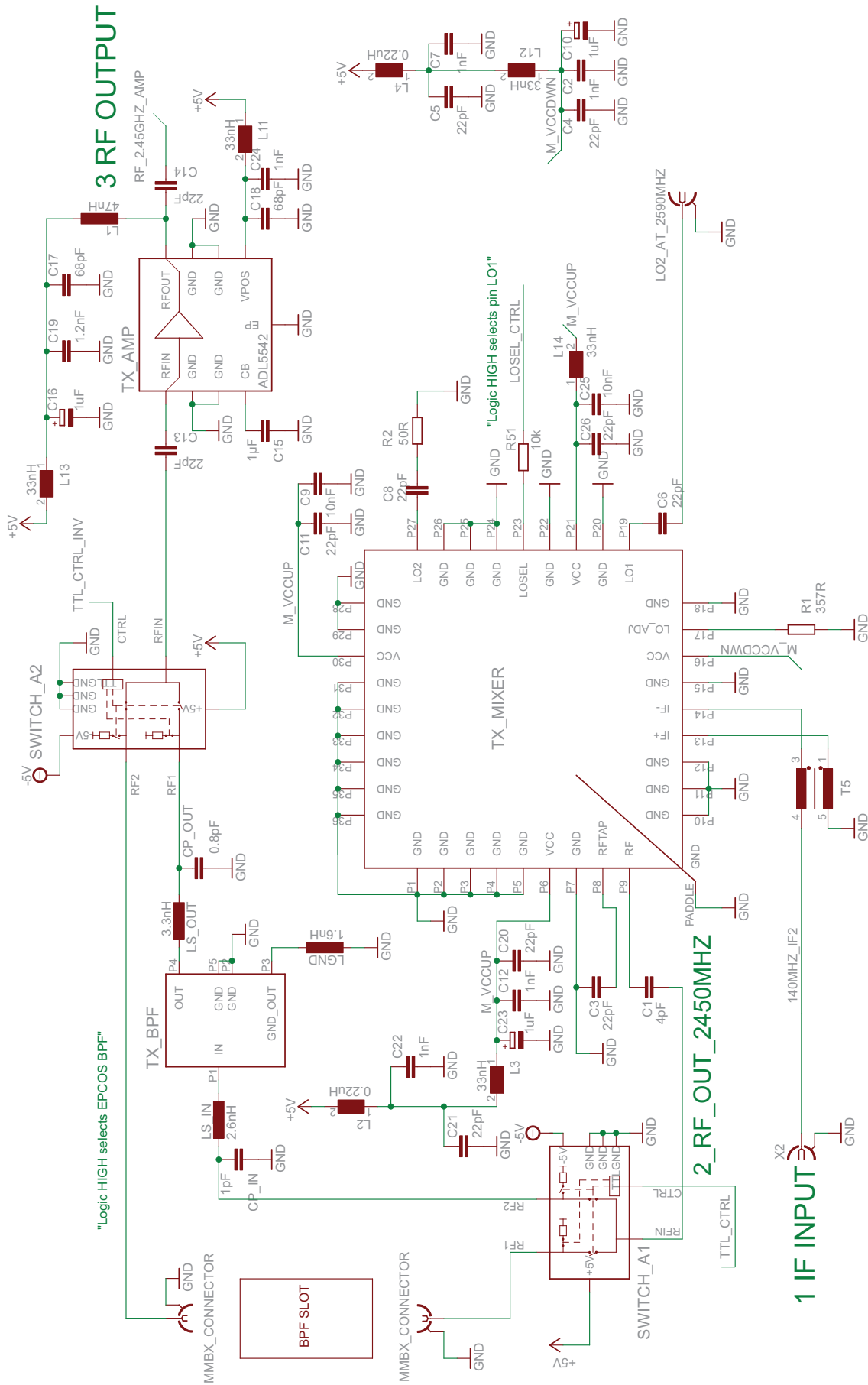
Figure 5.1: Upconversion stage schematic from IF to RF

5.1.2. Mode selection and LPF stage

As it has already been discussed in Section 1.3. the transmitter's maximum allowed EIRP is 36 dBm for the indoor mode and 27 dBm for the outdoor mode. Then, in order to exchange between both modes without reconfigure the transmitter amplifiers gain settings a switchable 10 dB attenuator is employed. This attenuator is a HMC541LP3 from Hittite which is named 10DB_ATT in Figure 5.2. The attenuator is endowed with a TTL[1]/CMOS[2] control input which is connected to the 10DB_ATT_CTRL control line from the control circuit. When the control line is "low" the attenuator is in the 10 dB attenuation state. However, when 10DB_ATT_CTRL is "high" the input signal is 1.1 dB attenuated because the attenuator insertion loss.

As the majority of the used components this IC has AC coupling capacitors, C29 and C30, at the input pin RF1, and at the output pin RF2. Also a simple bias filtering network composed by C31, C32 and L5 is connected to the VDD pin for decoupling the supply voltage from the RF.

Then, the signal is filtered with the same LPF concept as used in the receiver board which is also described in Section 3.3.3. This filter suppresses the harmonic frequencies produced at the mixer stage and supplies the signal to the first directional coupler, TX_CPLR1, of the transmitter.
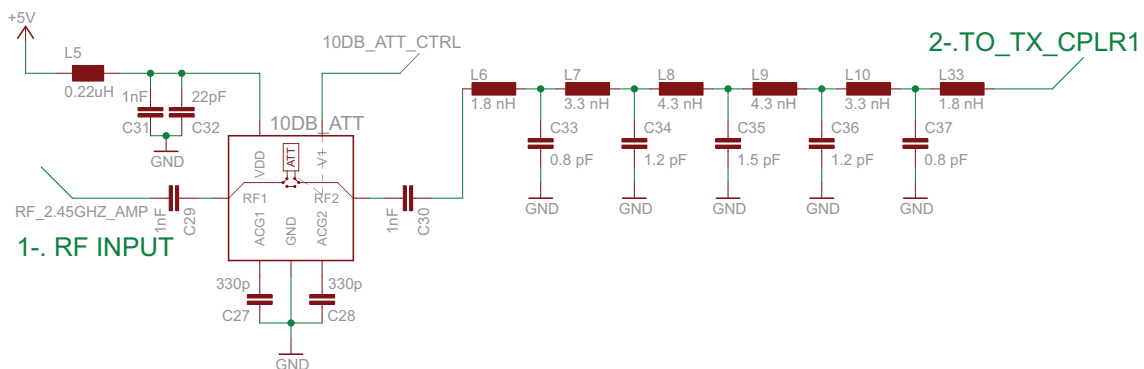
Figure 5.2: Schematic of the 10 dB attenuator and the low pass filter of the transmitter

5.1.3. Power detectors and output stage

The directional coupler TX_CPLR1 shown in Figure 5.3 is the same device, the BDCA1-7-33+ from Minicircuits, as employed in the receiver board. The main output of the TX_CPLR1 coupler, the RF_OUT port, provides its signal through the SMA port called TO_PA to the external power amplifier. Then, the output of this external power amplifier is connected back to the transmitter board through the SMA connector, FROM_PA, to the high power directional coupler TX_CPLR2 shown in Figure 5.3. This high power directional coupler is a SYBD-16-272HP+ from minicircuits with a very low main line loss of 0.25 dB. However,

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[1]Transistor Transistor Logic
[2]Complementary Metal Oxide Semiconductor

if the external power amplifier is not required the TO_PA port can be directly connected to the FROM_PA port at the TX_CPLR2 coupler avoiding this amplifying stage.

In addition, as described in Section 2.1. to increase the frontend possibilities the transmitter has some output ports to add an optional carrier compensation unit which improves the TX–RX isolation. For this purpose, both couplers the TX_CPLR1 and the TX_CPLR2 provide at their forward coupled port a fraction of the transmit signal. This signal can be later connected to the CCU module. This leads a power level which is 9.5 dB reduced, compared to the RF mainline. In the coupler TX_CPLR1 the coupled signal is 6.5 dB attenuated by the coupling losses. Then, the signal is split up by a 3 dB coupler. This leads a power level which is 9.5 dB reduced compared to the RF mainline. Thus, one copy of the split up signal is provided to the CARCOMP_OR port to drive the CCU module and the other copy is provided to the power detector Pwr. Det. 1. This power detector measures the signal power level before the external power amplifier and provides a DC voltage at its pin Vout depending on the transmit power level. This voltage (PDET_BFOR_PA) is connected to the X1 connector to monitor externally the current transmit power level.

This power detector is the same type, an ADL5513, as used in the receiver board and has the same schematic as described in Section 4.1.1.

The coupler TX_CPLR2 has the same purpose as the coupler TX_CPLR1 just after the external power amplifier. However, here the coupled signal is 16.4 dB attenuated by the coupler's coupling factor. Then, the signal is 20 dB attenuated by a LAT-20+ attenuator from Minicircuits. This attenuation is done in order to fed the right amount of power into the next device, a 3 dB coupler. Therefore, the coupled signal is 39.4 dB attenuated. One signal from the 3 dB coupler is fed into the CARCOMP_PA port to drive the CCU module. The other signal part is fed into the power detector Pwr. Det. 2 to measure the signal power level after the external power amplifier.

To avoid overload of a device or worse overload the external PA at its output due to reflections due to a possible antenna mismatch, the reflected power from the antenna port is also measured.

The reverse coupled output port of the coupler TX_CPLR2 gives a 16.4 dB attenuated copy of the reflected signal from the ANT port. Then, the signal is 20 dB attenuated to supply with a suitable power level the power detector Pwr. Det. 3. This power detector provides at the ANT_RVRS_PDET line tbe resulting DC voltage as a measure of this reflected power which is connected to the X1 connector. Then, by means of the external microcontroller, the amount of reflected power is monitored. Therefore, the shutdown of the transmitter can be forced by the microcontroller to protect the board from overload.

Figure 5.3: Power detectors schematic of the transmitter

2-. OUTPUT TO EXT. PA

3-. INPUT FROM THE EXTERNAL PA

4-. ANTENNA OUTPUT

*CLPF unconnected for Max video bandwidth

Pwr. Det. 1

*CLPF unconnected for Max video bandwidth

Pwr. Det. 2

*CLPF unconnected for Max video bandwidth

Pwr Det. 3
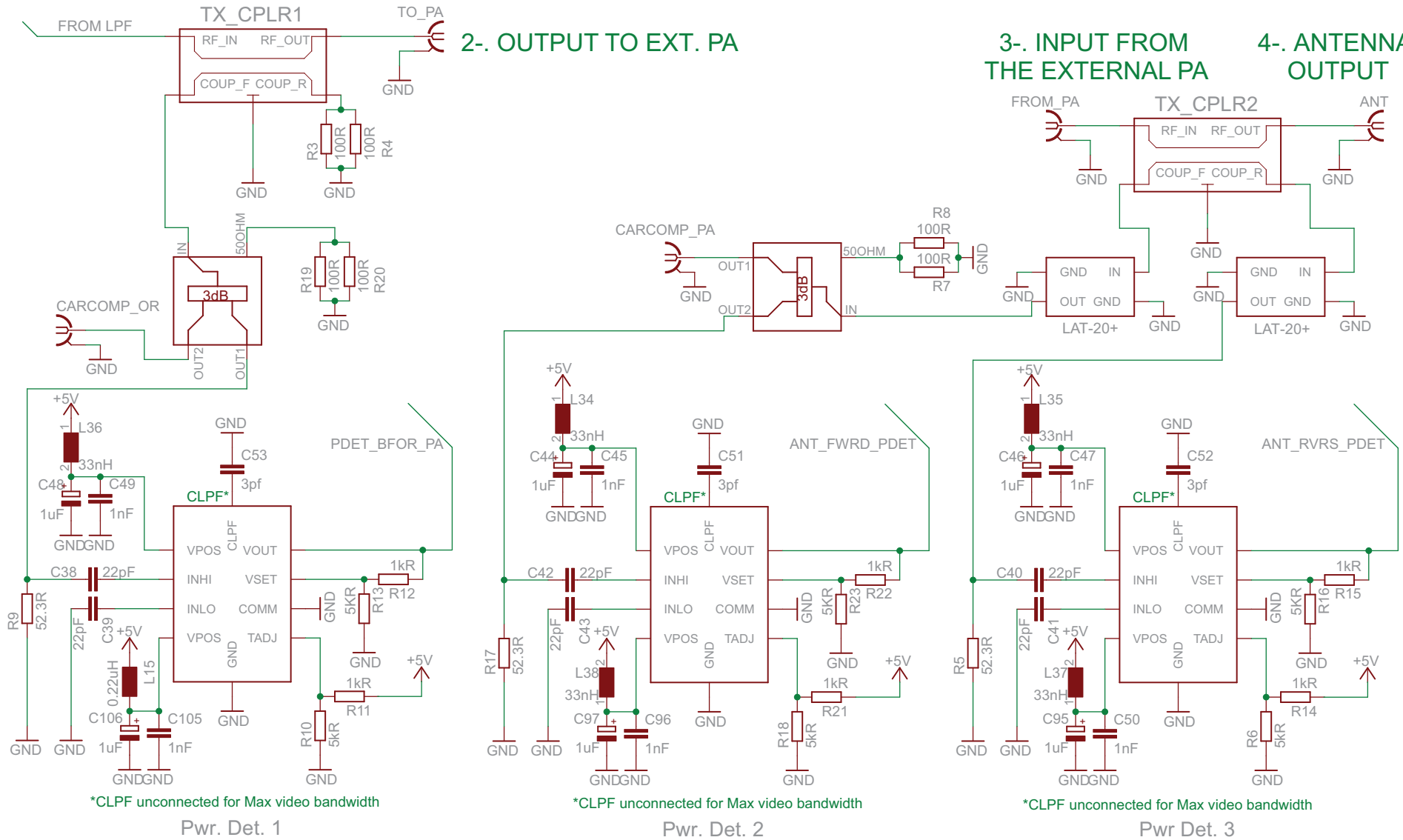
5.1.4. Power supply and control circuits

Figure 5.4 shows the power supply and the control circuits of the transmitter which are similar circuitries as described in Section 4.1.4. for the receiver board.

As in the receiver board, a 25 pin Sub-D connector, the X1 connector, is used for the external controlling and the power supply. Furthermore, via this X1 connector the DC supply voltages of ± 10 V are connected to the internal supply lines. The linear regulators are connected to this supply lines via the 1 A fuses F3 and F4. To further protect the circuit from voltage overloads, the diodes D1 and D2 for the negative voltage line and D3 and D4 for the positive voltage line, conduct if the polarity of the supply voltage is reversed. D2 and D4 are Zener diodes and start conducting also when the supply voltage reaches levels above +12 V(D4) and below -12 V (D2). In both cases the fuses, F3 and F4, break and prevent further damage at the transmitter board. Finally, the voltage regulator MC79M05 provides the voltage of -5 V to the switches, and the voltage regulator MC7805ABD2T provides 5 V to the majority of the devices. For this voltage regulator was calculated a copper heat dissipation area of 440 cm^2 in order to do not overheat this linear regulator.

To managed the control circuits with an external microcontroller, in Figure 5.4 three lines are provided through the resistors R56, R60 and R68. These lines are:

- BPF_SEL to select the onboard or the external BPF.

- OPERATION_MODE_CTRL to select the attenuator state defining the indoor and the outdoor operation mode.

- EN_ENBL_1 to shut down the transmitter board.

For BPF selection, two output control lines are required, the line TTL_CTRL and the line TTL_CTRL_INV, provided by the transistors T9 and T6. This two lines control the switch SWITCH_A1 and the switch SWITCH_A2. On Table 5.1 the resulting band pass filter selection is described depending on the BPF_SEL logic voltage.

Table 5.1: Truth table for the band pass filter path selection

BPF_SEL	SWITCH_A1	SWITCH_A2	BPF selected
High	RF2	RF1	Onboard
Low	RF1	RF2	External

For the attenuator control, when OPERATION_MODE_CTRL is "high" the attenuator is off. When OPERATION_MODE_CTRL is "low", the default status, the attenuator is at the 10 dB attenuation state. All the control circuits are built with a similar schematic for easily controlling. Furthermore, each control circuit can be manually controlled by the jumpers JP1, JP3 and JP4 shown in Figure 5.4.

Figure 5.4: Power supply and control circuits of the transmitter
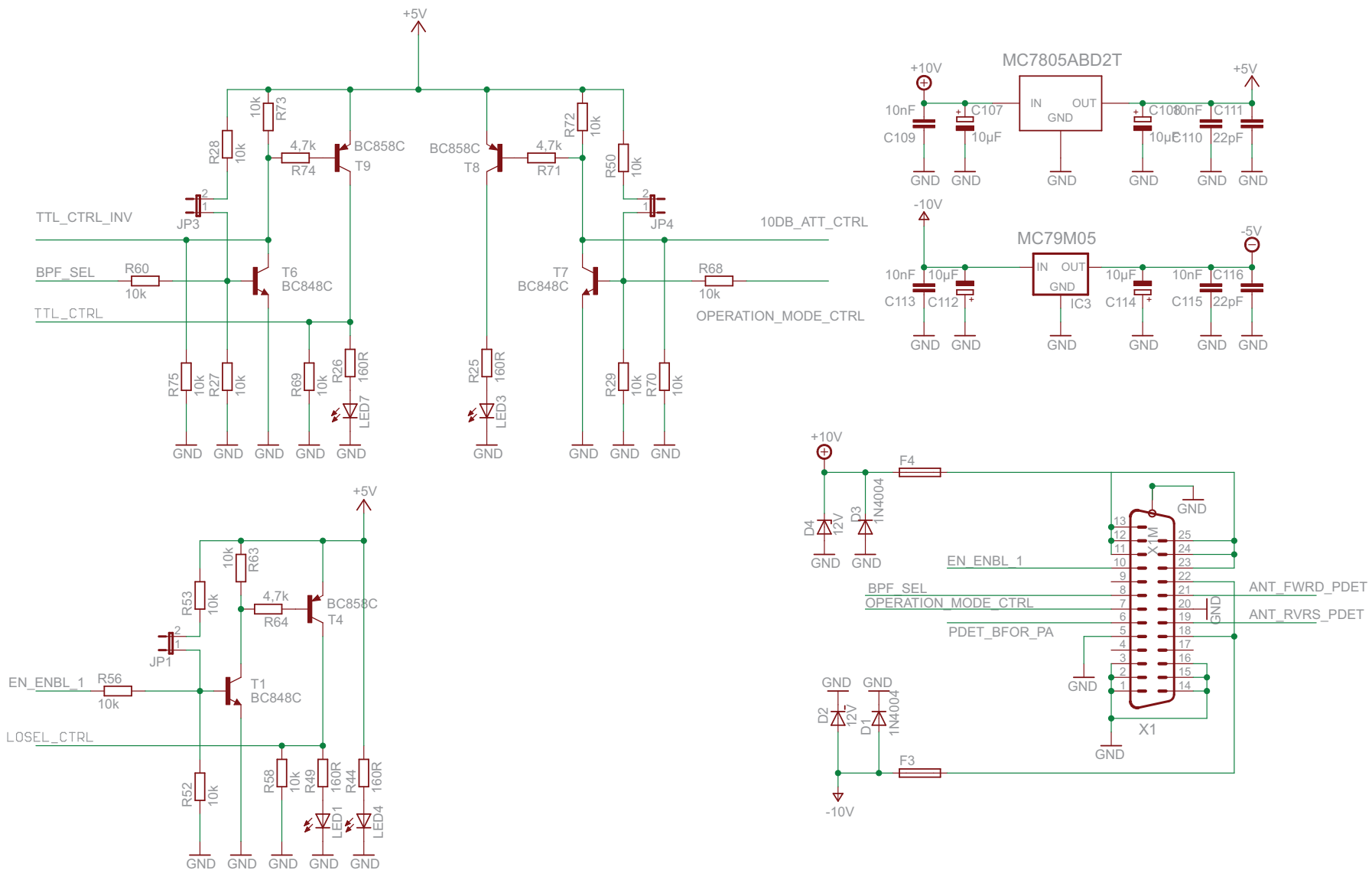
5.2. Power level plan

As for the receiver board, a power level plan for the transmitter board, shown in Figure 5.5, is created to determine the power level at each transmitter stage. In Figure 5.5a the gain, the 1 dB compression point, and the maximum output power for each transmitter device is given. For an assumed input power of −3 dBm, provided by the DAC, the transmitter's VGA is set to 17 dB gain and the 10 dB attenuator is switched off in order to get the maximum legal output power of 36 dBm using the external power amplifier AM-38A.

Figure 5.5b shows the 1 dB compression point, the absolute maximum output power and the carrier power level at each device. The same figure shows that the transmitter works in linear operation even when the maximum EIRP of 36 dBm is transmitted.

In order to do experiments with higher transmitted power than 36 dBm, it is possible to set the VGA to its maximum gain of 23 dB, achieving a theoreticall output power of 42 dBm. However, at this output power the external power amplifier, the AM-38A, is operated strongly non linear. So, the maximum output power is 41 dBm fixed by the saturation output power of this external power amplifier [18]. Nevertheless, because the use of an ASK[3] modulation for the communications, there is not a problem to transmit the message while the modulation index of the ASK signal does not get to small due to the saturation of power amplifier.

---

[3]Amplitude Shift Keying

(a)

		13.56 MHz				140 MHz				2.45 GHz Board										
	Start	Pad	Filter	Amp	Pad	First Mixer	Filter	VGA	Filter	TX Mixer	Switch A1	TX BPF	Switch A2	TX Amp.	Switch	ATT	LPF 1	TX CPLR 1	ext. PA	TX CPLR2
Gain / dB		-3	-0,5	8	-3	-1,7	-13	17	-0,5	-7,8	-1,4	-1,8	-1,4	17	-1,1	0	-1	-1,6	35	-0,2
F / dB		3	0,5	6	3	15	13	7,80	0,5	8,3	1	1,8	1	3,5	1,1	0	1	1,6	3	0,2
Carrier / dBm	-3,00	-6,00	-6,50	1,50	-1,50	-3,20	-16,20	0,80	0,30	-7,50	-8,90	-10,70	-12,10	4,90	3,80	3,80	2,80	1,20	36,20	36,00
Noise / dBm	-106,99																			
NF	1,0000	1,9953	2,2387	8,9125	9,2656	30,9449	50,7907	155,7903	155,8412	158,5357	159,2655	161,2635	162,7881	172,8568	172,9036	172,9036	172,9577	173,0748	173,4532	173,4532
NF / dB	0,00	3,00	3,50	9,50	9,67	14,91	17,06	21,93	21,93	22,00	22,02	22,08	22,12	22,38	22,38	22,38	22,38	22,38	22,39	22,39
SNR / dB	103,99	100,99	100,49	94,49	94,32	89,08	86,93	82,06	82,06	81,99	81,97	81,91	81,87	81,61	81,61	81,61	81,61	81,61	81,60	81,60
1dB out comp. / dBm	47,00	39,00	25,00	12,50	39,00	4,20	23,00	22,00	25,00	14,20	23,30	24,20	23,30	16,80	17,00	30,00	25,00	30,00	40,00	60,00
Abs. max. output /dB	47	39,00	47,00	21,00	39,00	8,30	25,00	27,00	25,00	20,00	24,00	25,20	24,00	28,00	18,00	30,00	30,00	45,00	41,00	43,90
Cumulative Gain / dB		-3	-3,50	4,50	1,50	-0,20	-13,20	3,80	3,30	-4,50	-5,90	-7,70	-9,10	7,90	6,80	6,80	5,80	4,20	39,20	39,00
Manufacturer																				
Device		3dB Pad	Coilcraft P7LP-306L	Mini-Circuits Mar-4SM	3dB Pad	Linear LT5511	Telefilter TFS140AV	Analog ADL5330	Selfmade LP	Maxim MAX2043	Mini-Circuits SWMA-2-50DR	Epcos B9430	Mini-Circuits SWMA-2-50DR	Analog AD5542	Hittite HMC541LP3E	Selfmade LPF	Mini-Circuits BDCA1-7-33+	MA_LTD AM38A	Mini-Circuits SYBD-16-272HP+

k   1,38E-23
Bandwidth / Hz   5,00E+06
Tr / K   2,90E+02

(b)

Figure 5.5: Power level plan at a high gain setting of the transmitter
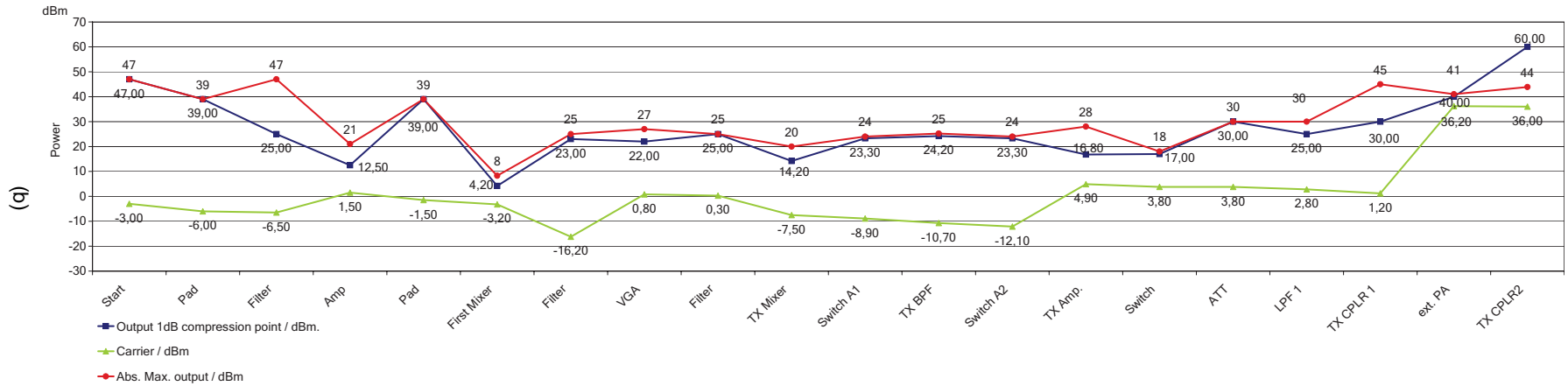
5.3. Measurements

To characterize the transmitter board described in this chapter, the frequency response is measured and a powersweep is performed to measure the linearity of the board. The implemented 2.45 GHz transmitter test board is shown in Figure 5.6.
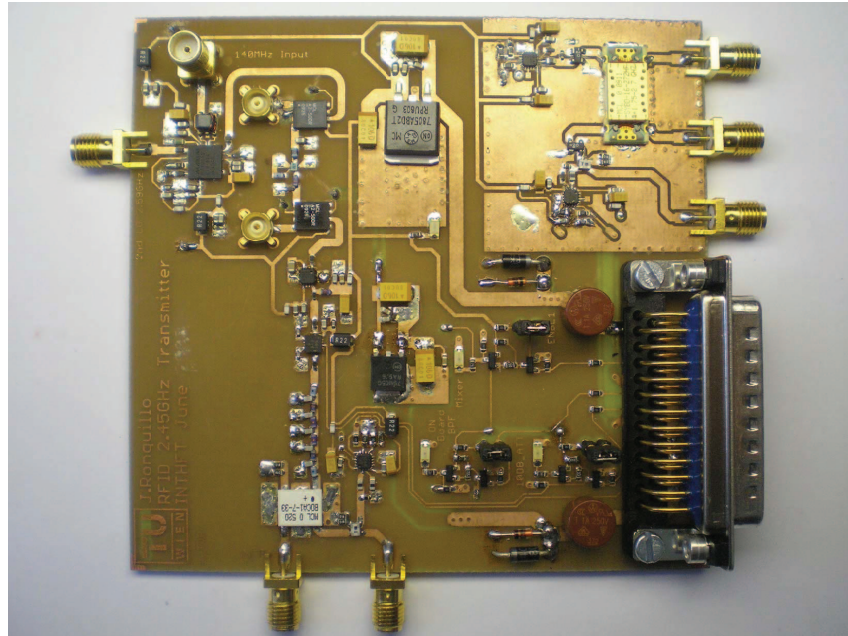
Figure 5.6: Implemented transmitter test board

5.3.1. Frequency response

The measurement of the transmitter frequency response follows the same setup as described in Figure 4.15 for the receiver board. However, at this measurement the measured frequency band is different. For this reason, the ports of the VNA, port 1 and port 2, are configured as indicated in Table 5.2.

Port	Use	Value	Measured band	Unit
ZVA8 port 1	IF output	0.3- 2589.7	107 - 190	MHz
ZVA8 port 2	RF input	0.3- 2589.7	2400- 2483	MHz
ZVA8 port 3	LO2 output	2590	-	MHz

Table 5.2: Transmitter frequency response test equipment frequencies

Due to the different configuration for the indoor and the outdoor mode of the 2.45 GHz transmitter stage, two frequency responses are measured.

For the outdoor mode, the onboard 10 dB attenuator of the transmitter is switched on. Thus, the transmitter is setup to the low gain configuration where a gain of -9.1 dB is expected at the frequency of 2450 MHz. As shown in the frequency response in Figure 5.7,

at this frequency the obtained -9.5 dB conversion gain result is close the expected result. However, in this band from 2400 MHz–2483 MHz, the flatness deviation is ± 1 dB. It could be interesting for MIMO[4] frontends to improve the obtained flatness deviation. However, for the current system this value is enough to transmit a single carrier.
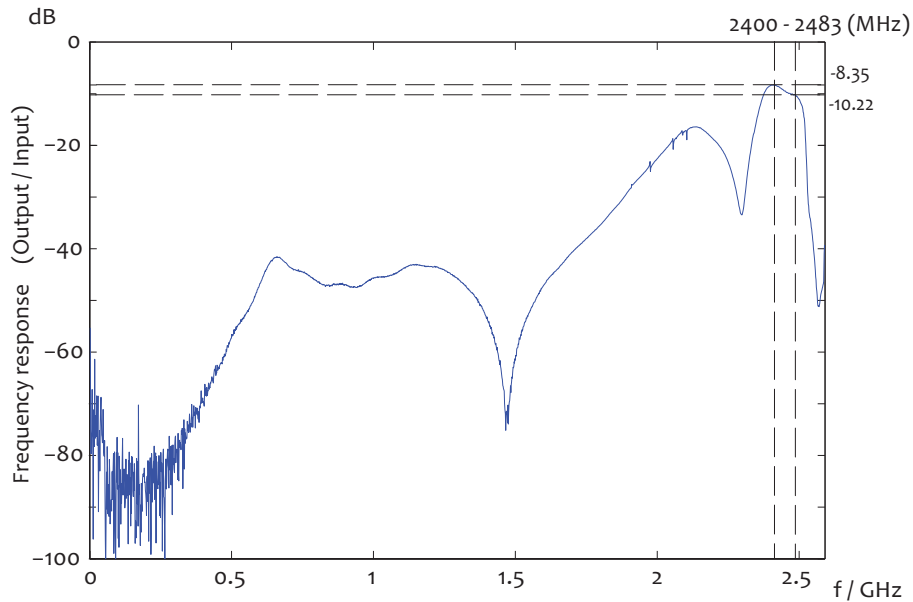
Figure 5.7: Transmitter frequency response: 10 dB attenuator on - outdoor mode

For the indoor mode, the transmitter's 10 dB attenuator is switched off. Therefore, in this configuration, the frequency response measured shown in Figure 5.8, gives a conversion gain of -0.1 dB at the 2450 MHz frequency which approaches to expected conversion gain of 0.9 dB at the same frequency.
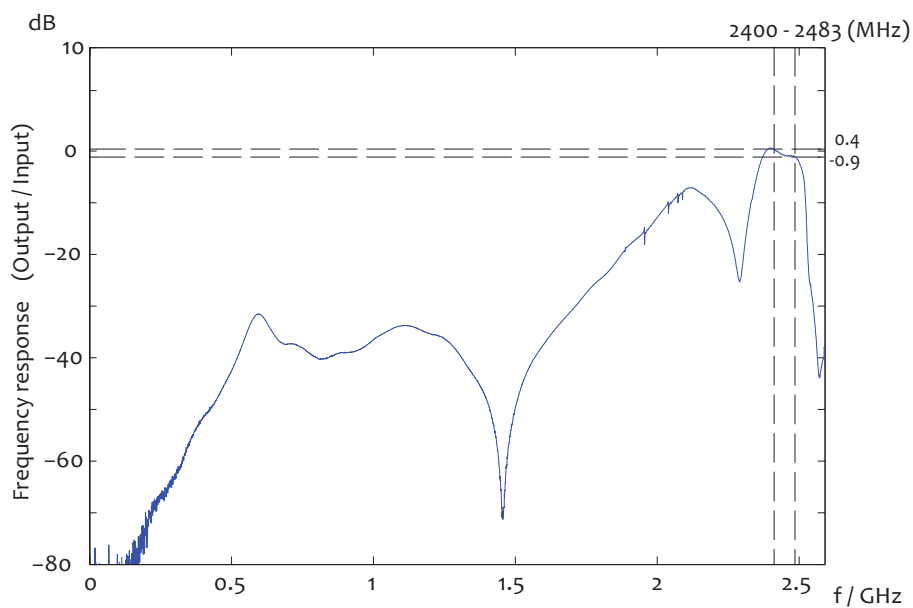
Figure 5.8: Transmitter frequency response: 10 dB attenuator off - indoor mode

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[4]Multiple Input / Multiple Output systems

5.3.2. Powersweep

The linearity measurement for the implemented 2.45 GHz transmitter test board follows the same powersweep method as described in Section 4.3.2. However, the internal configuration of the VNA is modified. Now, the VNA port 1 frequency is configured to a continuous wave of 140 MHz and the output power of this port sweeps from -25 dBm to 12 dBm.
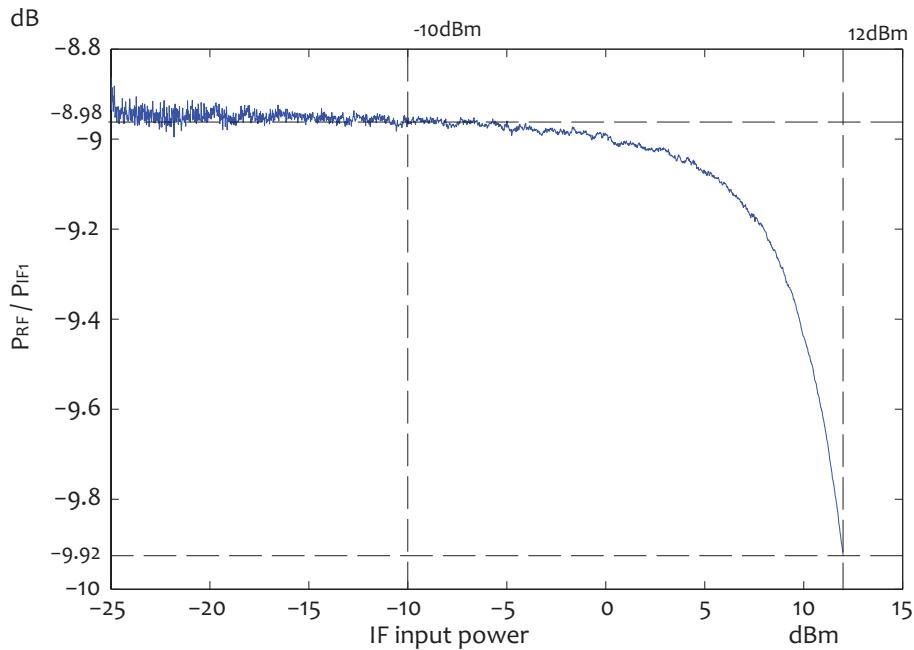
Figure 5.9: Linearity measurement of the receiver prototype

Figure 5.9 shows the measured powersweep for the 2.45 GHz transmitter test board configured at the maximum gain. In this measurement, the external power amplifier is not used. As a result, this transmitter test board has its 1 dB compression point at the input power of 12 dBm.

CHAPTER 6. CONCLUSIONS

In this master thesis I describe my frontend design for a 2.45 GHz RFID testbed. To develop this design, previously, the current situation of the 2.45 GHz RFID regulations is discussed. Also, the different transmit modes, Mode 1 and Mode 2, of the standard ISO 18000/4 (first edition) at this frequency band are briefly explained. Then, the flexible system concept which is easily adaptable to possible regulation changes is developed. This system concept consist of a transmitter, a receiver, a CCU, a power amplifier, antennas, a circulator, signal generators and power splitters.

The main work of this master thesis is to develop a transmitter and a receiver especially at the 2.45 GHz stage. This 2.45 GHz stage is designed in order to be fully compatible and easily integrable with the already developed frontends at the Institute of Communications and Radio Frequency Engineering of the Vienna University of Technology.

In order to achieve these two features the previous frontends have been studied in depth and a transmitter and a receiver PCB form factor has been created. Although the integration process itself was not in the focus of this work, this compatibility with the existing designs in the circuit layouts and the boards interconnections give the opportunity to merge the IF stage of the existing UHF frontend and the 2.45 GHz stage developed in this thesis.

To test some critical components and to test the transmitter and the receiver designed at 2.45 GHz, several two layers test PCBs are developed during this thesis. Furthermore, the transmitter test board and the receiver test board are employed to characterize the most important parameters and verify the good performance of both boards in the frequency domain and at different power levels.

Finally, with the merged circuit a final 4 layer transmitter board and a receiver board can now be implemented and fully integrated in the RFID testbed of the Institute of Communications and Radio Frequency Engineering of the Vienna University of Technology.

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APPENDIX

APPENDIX A. SCHEMATICS

On the following pages the full schematics of transmitter and the receiver of the 2.45 GHz stage are drawn.

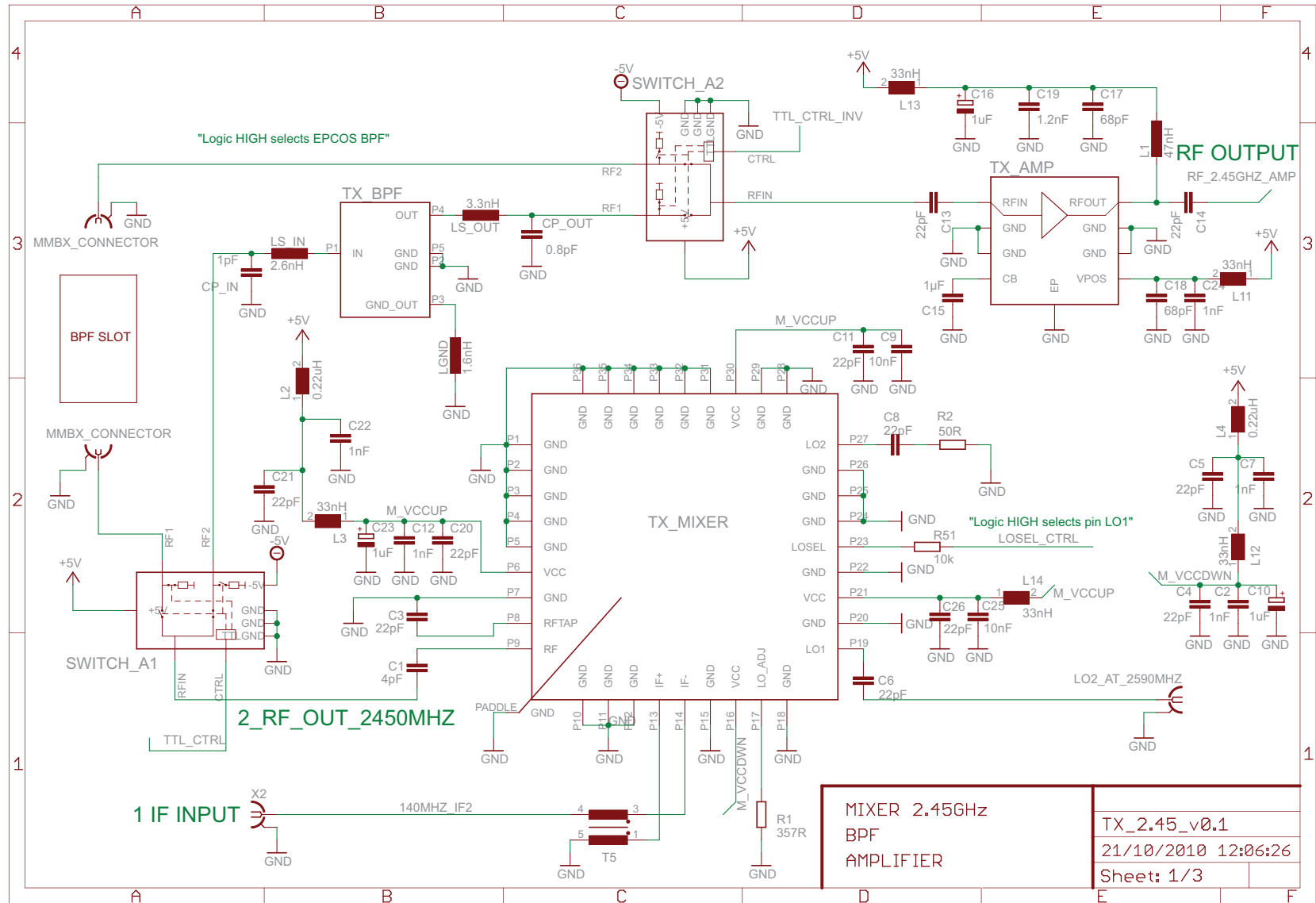Figure A.1: Transmitter schematic 1/3

Figure A.2: Transmitter schematic 2/3

2-. OUTPUT TO EXT. PA

+5V
L5
0.22uH
1nF 22pF
C31 C32
GND
10DB_ATT_CTRL
10DB_ATT
VDD
ATT
V+
RF1 RF2
ACG1 GND ACG2

RF_2.45GHZ_AMPL IN
C29

1-. RF INPUT

330p 330p
C27 C28
GND

L6 L7 L8 L9 L10 L33
1.8 nH 3.3 nH 4.3 nH 4.3 nH 3.3 nH 1.8 nH

1nF C30

C33 C34 C35 C36 C37
0.8 pF 1.2 pF 1.5 pF 1.2 pF 0.8 pF
GND GND GND GND GND

TX_CPLR1
RF_IN RF_OUT
COUP_F COUP_R
PS2
R3 100R 100R R4
GND

TO_PA
GND

FROM_PA TX_CPLR2
RF_IN RF_OUT
COUP_F COUP_R
SYBD-16-272MP+

3-. INPUT FROM
THE EXTERNAL PA

ANT
GND

4-. ANTENNA
OUTPUT

R19 100R 100R R20
GND

500HM
50 OHM
3dB
IN
OUT1
OUT2

CARCOMP_OR
GND

PDET_BFOR_PA

CARCOMP_PA
OUT1 OUT 50 50OHM
GND
OUT2 IN
3dB

R8
100R
100R
R7
GND

GND
P$3 GND IN P$4
GND$2 OUT GND P$1
20DB_ATT GND
LAT-20+

GND
P$3 GND IN P$4
GND$2 OUT GND P$1
20DB_ATT GND
LAT-20+

+5V
L36
33nH
C48 C49
1uF 1nF
GNDGND

C53 3pf
CLPF*
VPOS CLPF VOUT
INHI VSET
INLO COMM
VPOS TADJ
GND
ADL5513

GND
C38 22pF
R9
52.3R
22pF
C39
+5V
0.22uH
L15
C106 C105
1uF 1nF
GNDGND
GND GND

1kR
R13 R12
5kR
GND
GND
+5V
1kR
R11
R10
5kR
GND

Pwr. Det. 3
*CLPF unconnected for Max video bandwidth

+5V
L34
33nH
C44 C45
1uF 1nF
GNDGND

GND
C51 3pf
ANT_FWRD_PDET
CLPF*
VPOS CLPF VOUT
INHI VSET
INLO COMM
VPOS TADJ
GND
ADL5513

C42 22pF
C43
22pF
R17
52.3R
+5V
L38
33nH
C97 C96
1uF 1nF
GNDGND
GND GND

1kR
R23 R22
5kR
GND
GND
+5V
1kR
R21
R18
5kR
GND

Pwr. Det. 1
*CLPF unconnected for Max video bandwidth

+5V
L35
33nH
C46 C47
1uF 1nF
GNDGND

GND
C52 3pf
CLPF*
VPOS CLPF VOUT
INHI VSET
INLO COMM
VPOS TADJ
GND
ADL5513

ANT_RVRS_PDET

C40 22pF
C41
22pF
R5
52.3R
+5V
L37
33nH
C95 C50
1uF 1nF
GNDGND
GND GND

1kR
R16 R15
5kR
GND
GND
+5V
1kR
R14
R6
5kR
GND

Pwr. Det. 2
*CLPF unconnected for Max video bandwidth

COUPLERS &
POWER DETECTORS

TX_2.45_v0.1
21/10/2010 12:06:26
Sheet: 2/3

Figure A.3: Transmitter schematic 3/3

Figure A.4: Receiver schematic 1/4

SWITCH_B1
-5V
"Logic HIGH selects EPCOS BPF"
SWITCH_B2
+5V
CPLR_TO_LNA

TTL_CTRL_INV_A
MMBX_CONNECTOR_1
MMBX_CONNECTOR_2
RX_CPLR1

GND
GND
RF2
BPF SLOT
RF1
RFIN
RF_IN   RF_OUT

CTRL
GND
CTRL

ANT_IN
RFIN
RX_BPF
RF2

RFIN
COUP_F   COUP_R
CCU_IN

GND
RF1
3.3nH
P4
OUT
LS_IN
CTRL

ANTENNA INPUT
CP_OUT
LS_OUT
GND
P5
GND   IN   P1
2.6nH   1pF
TTL_CTRL_A
R12   R13
100R   100R

+5V
0.8pF
P2
GND
CP_IN
100R   100R

GND
1.8nH
P3
GND_OUT
GND
-5V
GND
GND

LGND
GND

GND

+4V
47nH   C134
L34   0.1uF
C133   9pF
GND

LNA
C135
LPF_TO_CPLR

CPLR_TO_LNA
C14
1.5pF
NC   NC
L7   2.2nH   22pF
L55   L56   L57   L58   L59   L60
1.8 nH   3.3 nH   4.3 nH   4.3 nH   3.3 nH   1.8 nH

RFIN   RFOUT
R9   300R
L42   2.2nH
RFGND   NC
C18
C164   C165   C166   C167   C168
0.8 pF   1.2 pF   1.5 pF   1.2 pF   0.8 pF

C17   C15
VBIAS   FB1
1.2pF
GND   GND   GND   GND   GND

0.1uF   100pF
620R   RBIAS
EP
GND   +4V

GND   GND
L52
1   2
33nH

C155   C154
22pF   1nF

GND   GND

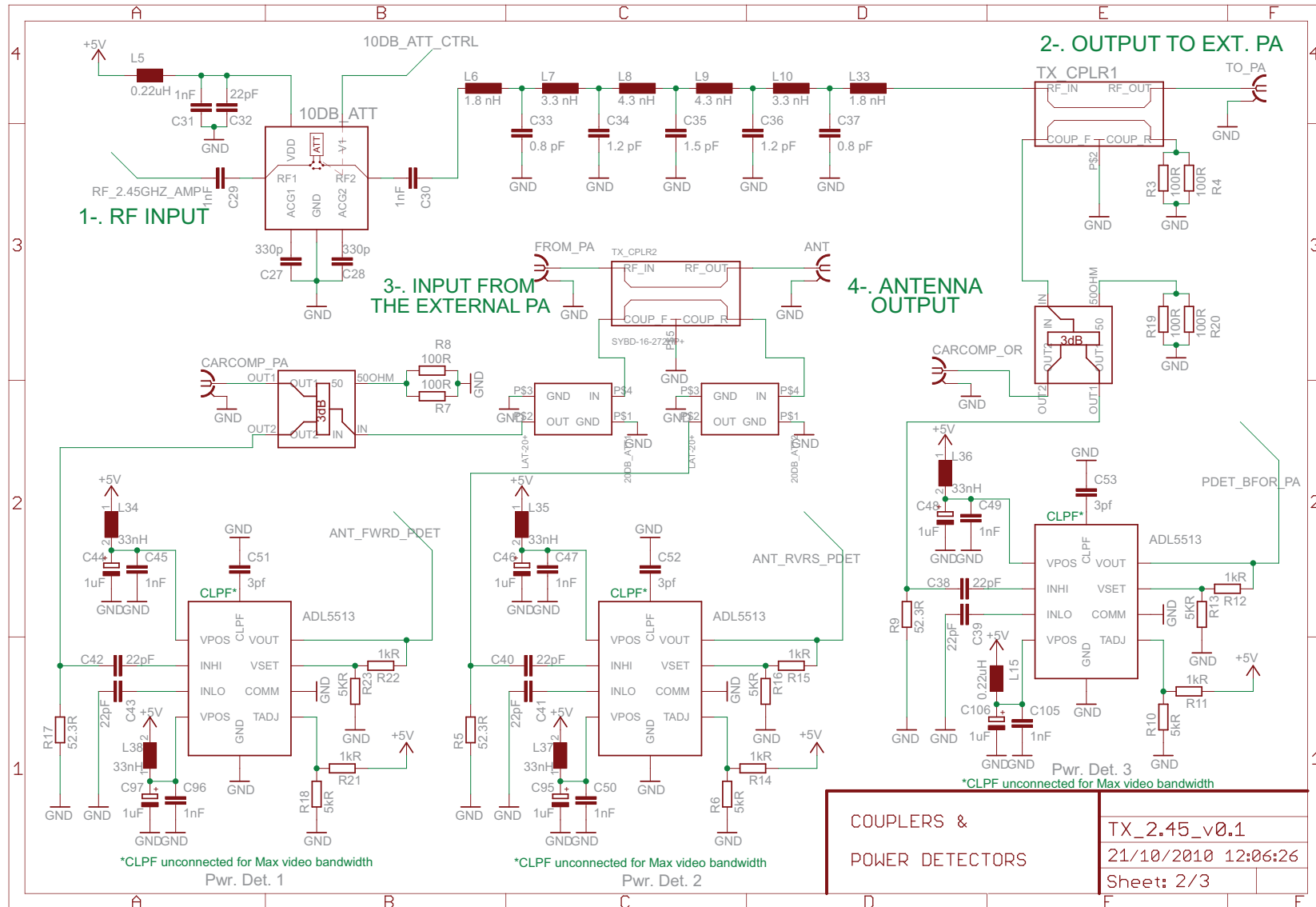RF INPUt, BPF AND LNA

RX_2.45_v0.1
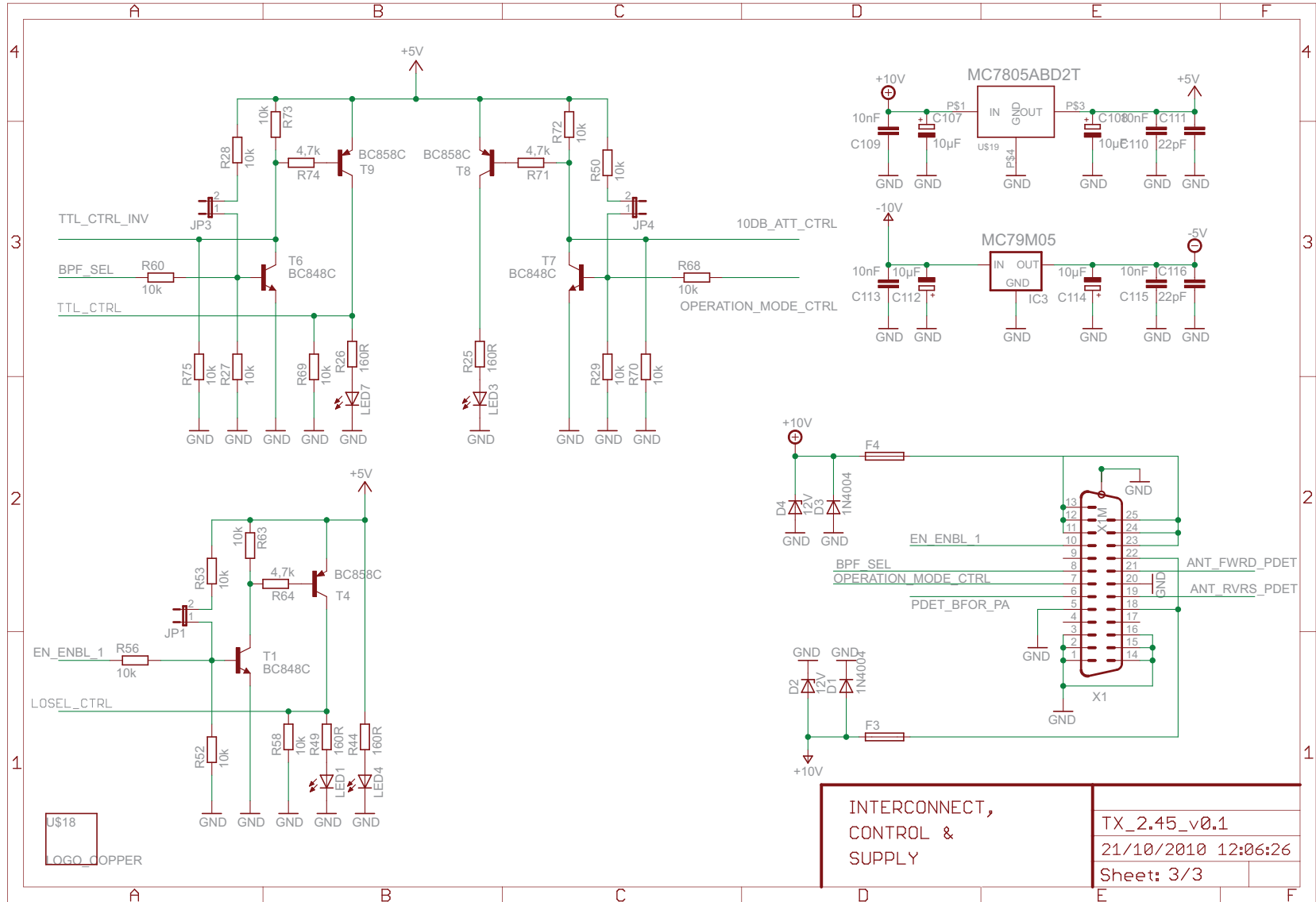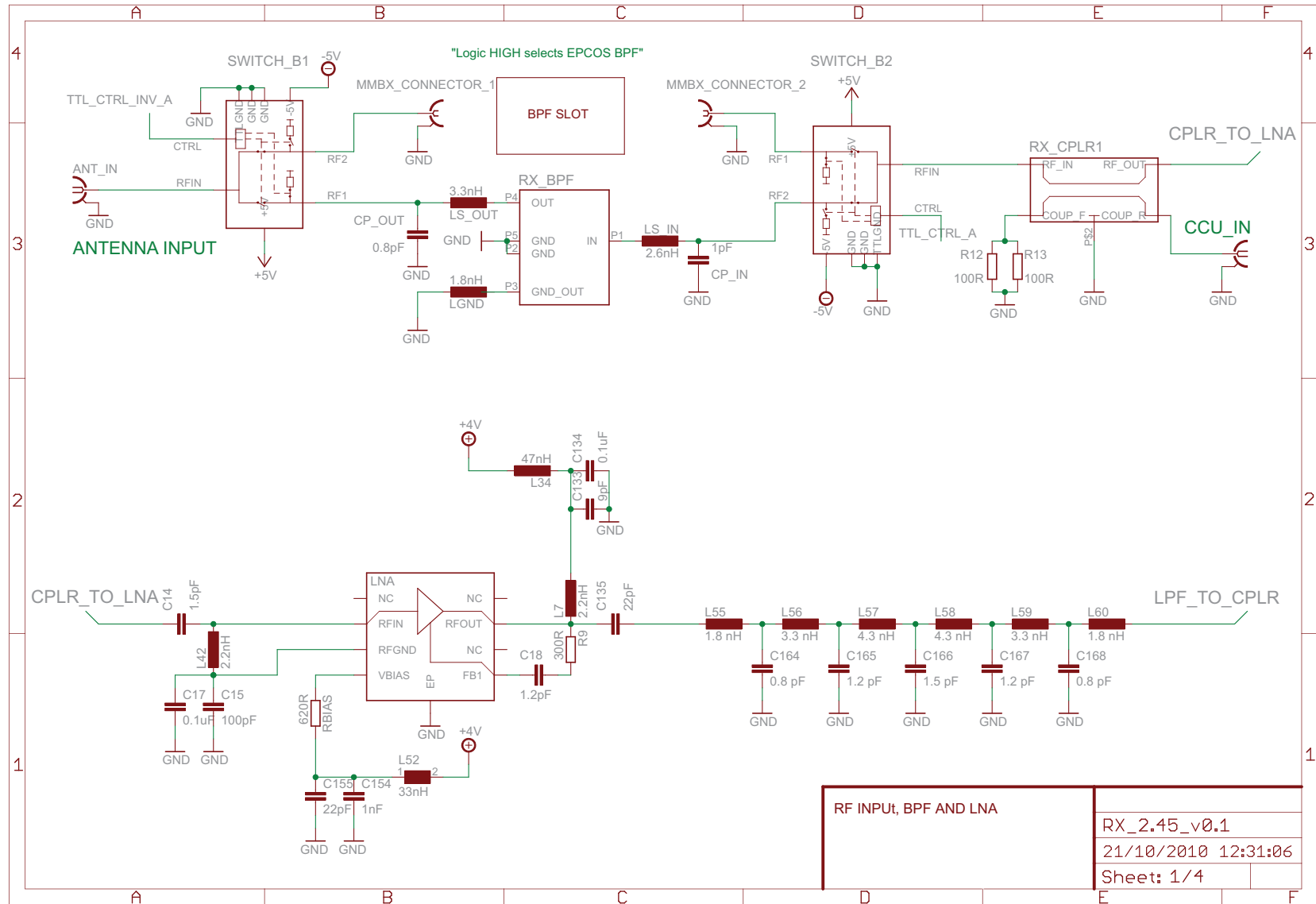21/10/2010 12:31:06
Sheet: 1/4

Figure A.5: Receiver schematic 2/4

Figure A.6: Receiver schematic 3/4

Figure A.7: Receiver schematic 4/4

APPENDIX B. DISTRIBUITORS OF THE DEVICES
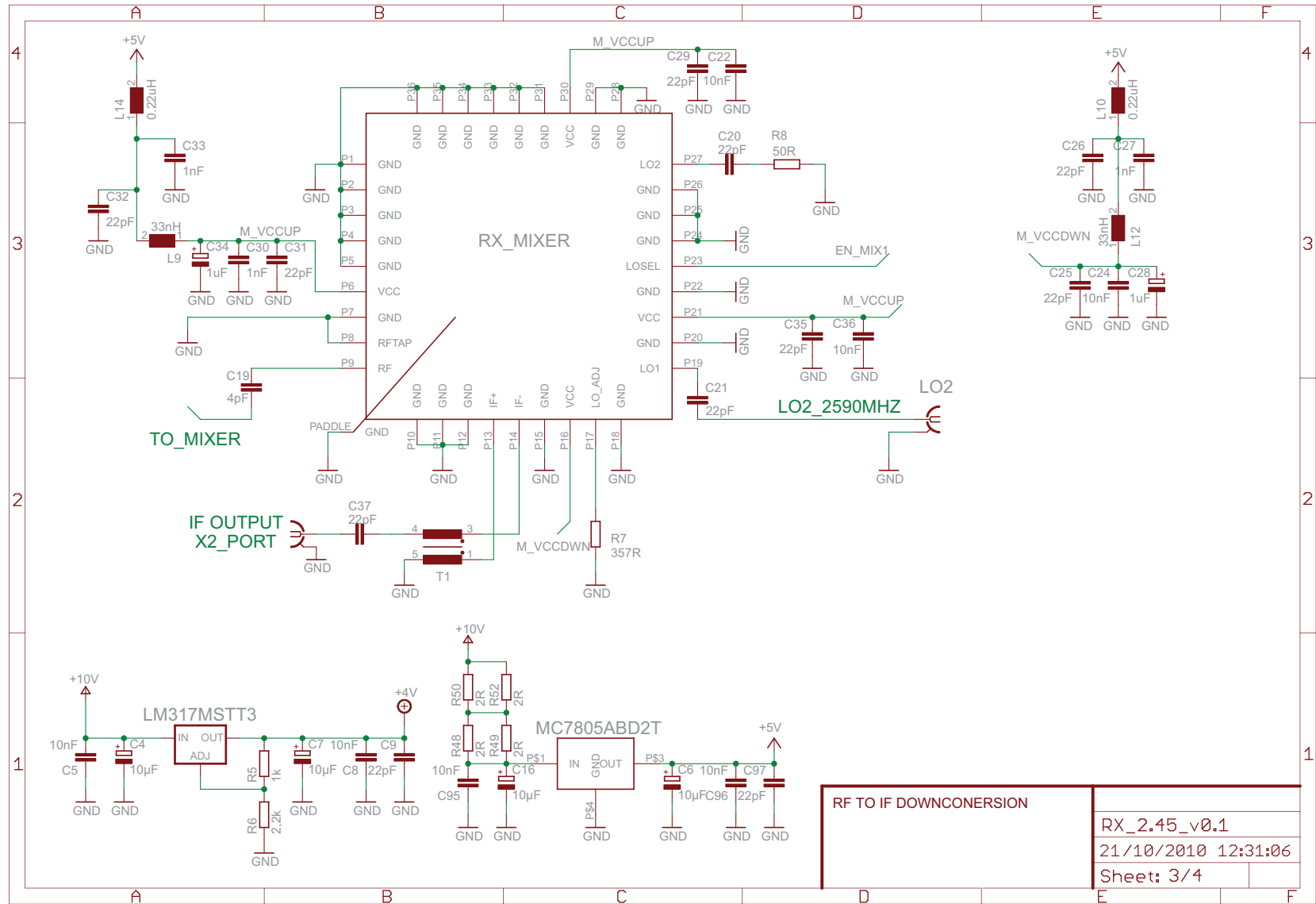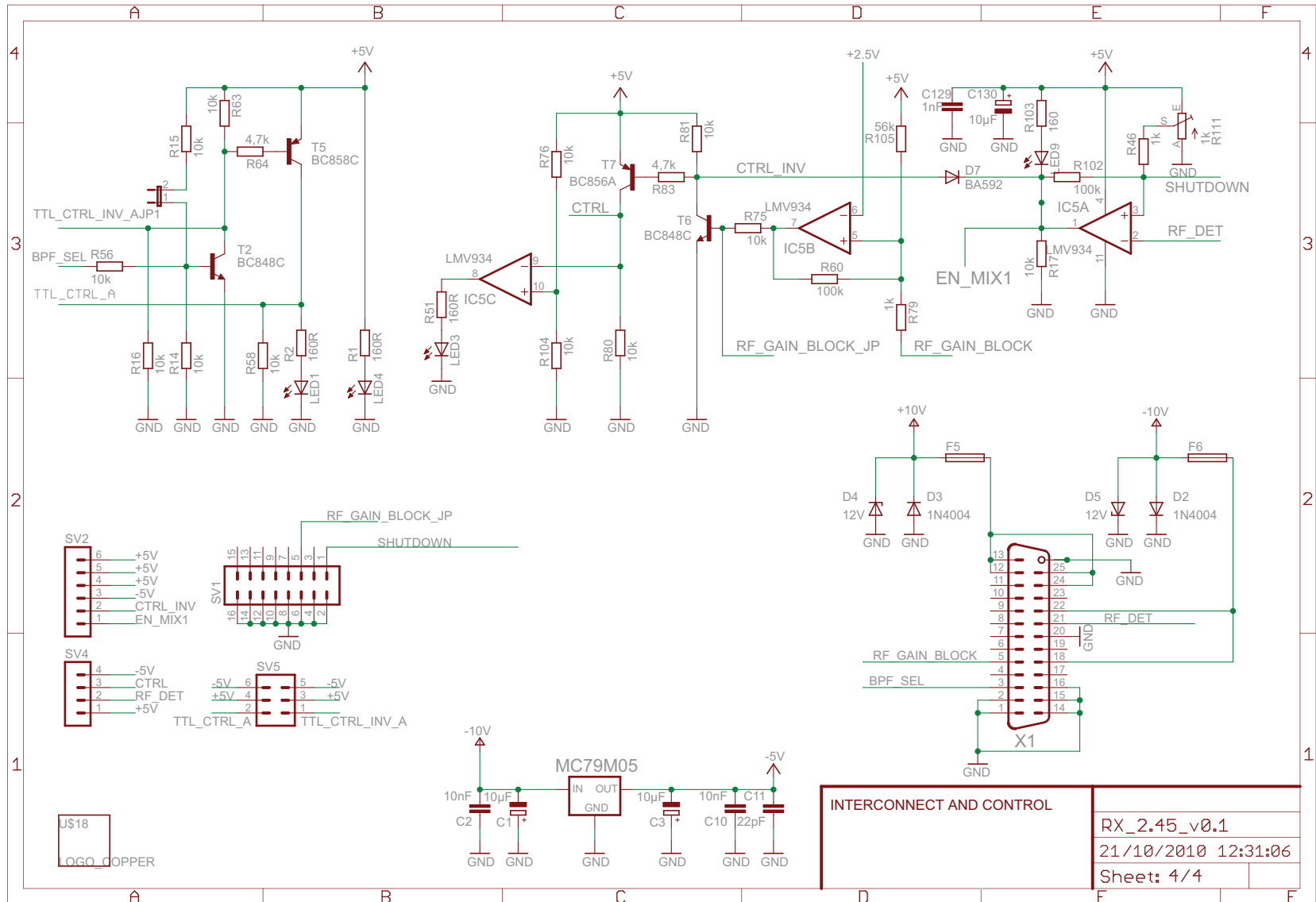
Table B.1: List of the Distributors of devices selected

Device	Model	Manufacturer	Distributor
TX, RX Mixer	MAX2043	Maxim	Digikey
TX Amp.	AD5542	Analog	Farnell
RX Amp.	MGA-30216	Avago	Farnell
LNA	MGA-632P8	Avago	Farnell
Attenuator	HMC541	Hittite	Hittite
Couplers	BDCA1-7-33+	Minicircuits	Municom
TX CPLR2	SYBD-16-272HP+	Minicircuits	Municom
3 dB CPLR1, 2	DB0805A	AVX RF	Farnell
Pwr. Det.	ADL5513	Analog	Digikey
Switches	SWMA-2-50	Minicircuits	Municom
TX, RX BPF	B9430	Epcos	Digikey
LPF 1,2,3	Butterworth	Selfmade	-