Modeling of Load-Transient Response of Direct-Duty-Ratio-Controlled Buck Converter

Teuvo Suntio, Jyri Kivimäki,
Tampere University of Technology, Dept. of Electrical Engineering
Korkeakoulunkatu 3
Tampere, FINLAND
E-Mails: teuvo.suntio@tut.fi, jyri.kivimaki@tut.fi
URL: http/www.tut.fi/en/

Keywords

<<Load transient response>>, <<dynamic modeling>>, <<buck converter>>, <<direct-duty-ratio control>>, <<continuous conduction mode>>

Abstract

This paper provides a simple analytical model for the closed-loop output impedance of a direct-duty-ratio-controlled buck converter, which can be used to predict the behavior of the output voltage during a load-current transient. The modeling method utilizes standard control theory to obtain the model for the sensitivity function based on the crossover frequency and phase margin of the output-voltage feedback loop as well as on a clever estimate for the corresponding open-loop output impedance. The modeling method is validated by means of simulations and experimental tests.

Introduction

The mathematical treatment of load-transient response is presented already in early 1980's [1] based on the dynamic model of a direct-duty-ratio (DDR) controlled converter obtained by means of state-space-averaging method [2]. Similar treatments can be found quite many such as [3-5]. It was observed already in late 1980's [6,7], and confirmed later [8-10] that the application of load-current feedforward would improve the load transient response significantly. The load transient improvements can be obtained by applying output-capacitor-current feedforward as well, because the change in the load current affects the capacitor current [12,13]. The application of the load-current feedforward reduces significantly the size of the open and closed-loop output impedance, and thus improves the load transient response [7,9]. The fastest load responses can be obtained by applying external circuitry, which temporarily shunts the output-filter section of the converter as described for example in [13]. There are many design factors beside the feedforward techniques discussed above, which will affect the obtainable transient response [14,15] such as selection of the power-stage components [16-18], the bandwidth [19-22] and phase margin [23-25] of the feedback loop. It is well-known that the existence of right-half-plane (RHP) zeros in the control dynamics will effectively limit the achievable control bandwidth [15,26,27]. A good example is a boost converter in continuous conduction mode (CCM), where the RHP zero locates close to the resonant frequency of the converter power stage, and therefore, the transient response is poor due to the rather high closed-loop output impedance [26].

The main goal of this paper is to introduce an efficient method to obtain an analytical model of the closed-loop output impedance of a direct-duty-ratio (DDR) or voltage-mode (VM) controlled buck converter. It is well-known that the output-voltage behavior during a step change is governed by the closed-loop output impedance and the applied load-current dynamics [14,15]. The closed-loop output impedance can be constructed analytically, but the resulting order in Laplace domain is rather high and therefore, it cannot be easily transformed into time domain. The methods to solve the problem of obtaining the time-domain transformation are based on the classical control engineering [28] to present

the sensitivity function in a simple second-order mode and the open-loop output impedance in a clever way. The presented method does not, however, give satisfying results in the converters, where the open-loop dynamics is effectively of first-order and the pole locates close to origin such as the peak-current-mode (PCM) - controlled converters [26,29]. In such cases, other methods should be utilized as introduced for example in [15,30,31].

Implications from Experiments

Fig. 1 shows the measured load-transient responses of a buck converter employing direct-duty-ratio (DDR) (Note: known also as voltage-mode control (VCM)) [32], peak-current-mode (PCM) [29], and PCM-control with output-current feedforward (OCF) [9] internal control techniques. The corresponding measured output-voltage-feedback loop gains are shown in Fig. 2, respectively. The power stage is the same all the time, and only the control technique is modified according to the principles introduced explicitly in [9,29,32]. The feedback-loop crossover frequencies are designed to be the same at the input voltage of 50 V (i.e., close to 10 kHz), but the load-transient tests are performed at the minimum input voltage of 20 V, where the crossover frequency of the DDR-controlled converter is reduced to 6 kHz due to the reduction of input voltage by 30 V [26]. The feedback-loop crossover frequency of the PCM-controlled converter does not actually change along the changes in input voltage [26]. Fig. 2 shows that the phase margin (PM) of the PCM- controlled converter is higher than the PM of the DRR controlled converter, which explains the difference in the settling times of the converters.

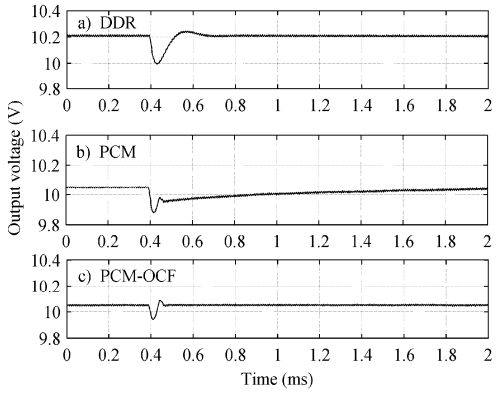

Fig. 1: Load-current responses of a buck converter employing different internal control schemes

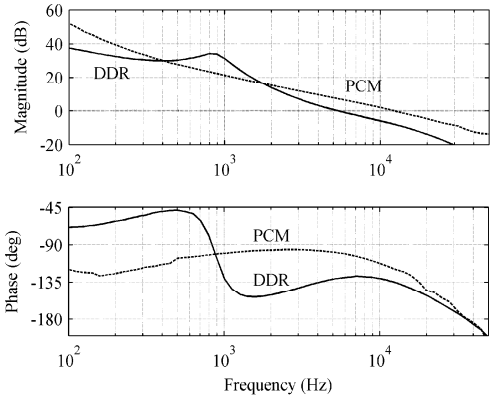

Fig. 2: Measured output-voltage loop gains

The initial voltage dips of the DDR and PCM-controlled (cf. Figs. 1a and b) are approximately the same (i.e., close to 200 mV). The method to estimate the initial voltage dip introduced in [3] (cf. Eq. (1)) would yield 100 mV, when it is applied to the converters in Fig. 1. Eq. (1) does not, however, take into account the effect of the capacitor ESR. When the effect is added, the predicted initial dip will be 180 mV, which corresponds well to the measured dip. The initial voltage dip and the settling time of the PCM-OCF-controlled converter (cf. Fig. 1c) are very small and short compared to the other corresponding responses in Figs.1a and b. It is well known that the initial voltage dip can be estimated also by means of the converter output impedance at the feedback-loop crossover frequency. The measured closed-loop output impedance of the converters are given in Fig. 3. Based on the crossover frequencies and Fig. 3, it may be obvious that the corresponding output impedances of the DDR and PCM-controlled converters are quite equal, and the corresponding output impedance of the PCM-OCF-controlled converter is much smaller than the other impedances. These similarities and differences will explain thoroughly the initial behaviour of the output-voltage load transients in Fig. 1. Fig. 4 shows the open-loop output impedances. It indicates that the output-current feedforward technique introduced in [9] will effectively reduce the magnitude of the output impedance in wide frequency range (cf. PCM vs. PCM-OCF). It is possible to reduce the output impedance down to zero in theory as discussed in [7],

but the consequence of the reduction is that the source impedance will be reflected into the output impedance (cf. [26]), and therefore, obtaining the zero output impedance is in practice impossible.

$$\Delta v_{\text{out}} = \frac{\Delta \text{i}_{\text{out}}^2}{2(V_{\text{in}} - V_{\text{out}})} \cdot \frac{L}{C} \tag{1}$$

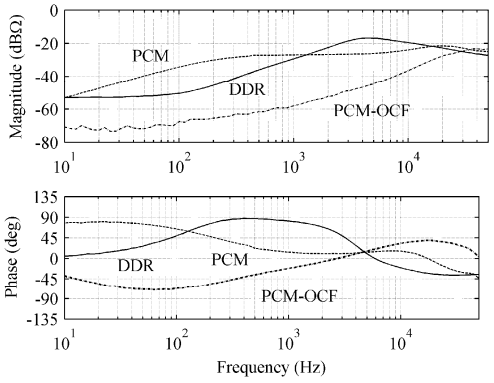

Fig. 3: The measured closed-loop output impedances

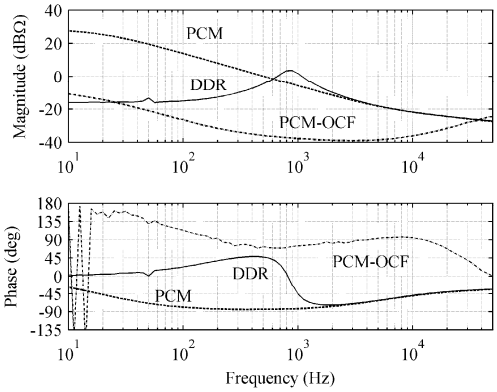

Fig. 4: The measured open-loop output impedances

Modeling Closed-Loop Output Impedance

It is obvious that the output-voltage load-current response can be computed based on Eq. (2) as discussed in [14,15,26,30], where $Z_{\text{o-o}}$ denotes the open-loop output impedance and $L(s)$ denotes the output-voltage feedback loop gain, $\Delta v_{\text{out}}(s)$ and $\Delta i_{\text{out}}(s)$ are the *Laplace*-domain responses of the output voltage and current, respectively. According to Eq. (2), we can conclude that the contributing factors in the load response are the open-loop output impedance as well as the output-voltage feedback-loop gain in the form of sensitivity function ($S(s)$) (cf. Eq. (3)). Deriving a direct inverse Laplace transform of Eq. (2) will be quite complicated due to a large number of zeros and poles (i.e., $Z_{\text{o-o}}$: at least two zeros and two poles; modified PID controller: two zeros and three poles, etc.) Therefore, it would be convenient if the open-loop output impedance and the sensitivity function can be estimated by means of a low number of poles and zeros and the closed-loop output impedance as a product of them.

$$\Delta v_{\text{out}}(s) = \frac{Z_{\text{o-o}}}{1 + L(s)} \cdot \Delta i_{\text{out}}(s) \tag{2}$$

$$S(s) = \frac{1}{1 + L(s)} \tag{3}$$

Estimating sensitivity function

According to Ref. [28], the closed-loop system can be commonly estimated by means of the standard form of second-order transfer function given in Eq. (4), which actually corresponds, in principle, to the complementary sensitivity function ($T(s)$) given in Eq. (5), respectively. The parameters in Eq. (4) are as follows: ω_{ne} denotes the estimate for the undamped natural frequency and ζ_{e} denotes the estimate for the damping factor.

$$\frac{\omega_{\text{ne}}^2}{s^2 + s2\zeta_{\text{e}}\omega_{\text{ne}} + \omega_{\text{ne}}^2} \tag{4}$$

$$T(s)=\frac{L(s)}{1+(Ls)} \tag{5}$$

According to Eqs. (4) and (5), we can solve the formula representing the estimate of the feedback loop gain ($L_{\mathrm{e}}(s)$) as follows

$$L_{\mathrm{e}}(s)=\frac{\omega_{\mathrm{ne}}^2}{s(s+2\zeta_{\mathrm{e}}\omega_{\mathrm{ne}})} \tag{6}$$

The sensitivity function ($S_{\mathrm{e}}(s)$) can be estimated according to Eqs. (3) and (6) by

$$S_{\mathrm{e}}(s)=\frac{s(s+2\zeta_{\mathrm{e}}\omega_{\mathrm{ne}})}{s^2+s2\zeta_{\mathrm{e}}\omega_{\mathrm{ne}}+\omega_{\mathrm{ne}}^2} \tag{7}$$

The classical control engineering [28] states that the feedback-loop crossover frequency (ω_{c}) and the phase margin (PM) are related to the undamped natural frequency and damping factor as follows

$$\begin{aligned}\omega_{\mathrm{c}}&=\omega_{\mathrm{ne}}\sqrt{\sqrt{1+4\zeta_{\mathrm{e}}^4}-2\zeta_{\mathrm{e}}^2}\\ \mathrm{PM}&=\tan^{-1}\left(\frac{2\zeta_{\mathrm{e}}}{\sqrt{\sqrt{1+4\zeta_{\mathrm{e}}^4}-2\zeta_{\mathrm{e}}^2}}\right)\end{aligned} \tag{8}$$

According to Eq. (8), ω_{ne} and ζ_{e} can be computed to be

$$\begin{aligned}\omega_{\mathrm{ne}}&=\frac{\omega_{\mathrm{c}}}{\sqrt{\sqrt{1+4\zeta_{\mathrm{e}}^4}-2\zeta_{\mathrm{e}}^2}}\\ \zeta_{\mathrm{e}}&=\frac{\tan(\mathrm{PM})}{2(1+\tan^2(\mathrm{PM}))^{\frac{1}{4}}}\end{aligned} \tag{9}$$

The system time constant (τ) can be given by $1/\zeta\omega_{\mathrm{n}}$ [28,31]. The settling time of the transients in the system is directly related to the time constant, and therefore, it is easy to understand (cf. Eq. (9)) that the phase margin of the feedback-loop gain has significant effect on the transient behavior as discussed earlier (cf. Figs.1a and 1b). The resonant frequency (ω_{res}) of the system in Eq. (4) can be given by

$$\omega_{\mathrm{res}}=\omega_{\mathrm{ne}}\sqrt{1-2\zeta_{\mathrm{e}}^2} \tag{10}$$

and the corresponding maximum peak magnitude (M_{pe}) by

$$M_{\mathrm{pe}}=\frac{1}{2\zeta_{\mathrm{e}}\sqrt{1-2\zeta_{\mathrm{e}}^2}} \tag{11}$$

Eq. (10) is also the origin from which the optimal damping factor is derived to be $1/\sqrt{2}$ [28] (i.e., the system loses its resonant nature when the damping is higher than the optimal damping factor). Based on the sensitivity function estimate in Eq. (7), Eq. (2) can be given by

$$\Delta v_{\text{out}}(s) = Z_{\text{o-o}} \cdot \frac{s(s+2\zeta_{\text{e}}\omega_{\text{ne}})}{s^2 + s2\zeta_{\text{e}}\omega_{\text{ne}} + \omega_{\text{ne}}^2} \cdot \Delta i_{\text{out}}(s) \tag{12}$$

where ω_{ne} and ζ_{e} are defined in Eq. (9), respectively.

Estimating open-loop output impedance

It is well known [15,29] that the resonant nature of the DDR-controlled converters requires the use of PID-like controllers for being able to increase the phase for stability to exist. The PID-controller transfer function in power electronics application can be given [26] by

$$G_{\text{PID}} = K_{\text{cc}} \frac{(1+s/\omega_{\text{z1}})(1+s/\omega_{\text{z2}})}{s(1+s/\omega_{\text{p1}})(1+s/\omega_{\text{p2}})} \tag{13}$$

For obtaining fast transient response [14,15], the controller zeros (i.e., ω_{zi}) in Eq. (13) are placed in vicinity of the resonant frequency of the power stage for compensating the phase effect of the resonant poles.

The open-loop output impedance of the DDR-controlled buck converter can be given in general [26] by

$$Z_{\text{o-o}} = \frac{r_{\text{a}}(1+s/\omega_{\text{zL}})(1+s/\omega_{\text{zC}})\omega_{\text{n}}^2}{s^2 + s2\zeta\omega_{\text{n}} + \omega_{\text{n}}^2} \tag{14}$$

where r_{a} denotes the resistive losses in series with the inductor, ω_{n} and ζ denote the undamped natural frequency and the damping factor of the power stage, ω_{zL} (i.e., r_{a}/L) denotes the zero related to the output inductor and ω_{zC} (i.e., $1/r_{\text{C}}C$) denotes the zero related to the output capacitor (known also as ESR zero). According to the placing of the controller zeros (i.e., at ω_{n}), the open-loop output impedance can be given (cf. Eq. (14)) by

$$Z_{\text{o-o}}^{\text{e}} = \frac{r_{\text{a}}\omega_{\text{n}}^2}{\omega_{\text{z1}}\omega_{\text{z2}}} \frac{(1+s/\omega_{\text{zL}})(1+s/\omega_{\text{zC}})}{(1+s/\omega_{\text{z1}})(1+s/\omega_{\text{z2}})} \approx r_{\text{a}} \cdot \frac{(1+s/\omega_{\text{zL}})(1+s/\omega_{\text{zC}})}{(1+s/\omega_{\text{z1}})(1+s/\omega_{\text{z2}})} \tag{15}$$

Therefore, Eq. (2) can be given based on the estimates of the system and open-loop output impedance by

$$\Delta v_{\text{out}}(s) \approx r_{\text{a}} \cdot \frac{(1+s/\omega_{\text{zL}})(1+s/\omega_{\text{zC}})}{(1+s/\omega_{\text{z1}})(1+s/\omega_{\text{z2}})} \cdot \frac{s(s+2\zeta_{\text{e}}\omega_{\text{ne}})}{s^2 + s2\zeta_{\text{e}}\omega_{\text{ne}} + \omega_{\text{ne}}^2} \cdot \Delta i_{\text{out}}(s) \tag{16}$$

which can be transformed easily into time domain due to well defined poles and zeros.

The magnitude of the closed-loop output impedance at the crossover frequency (ω_{c}) can be quite easily computed from Eq. (16) yielding

$$\left|Z_{\text{o-c}}^{\text{e}}\right|_{\omega=\omega_{\text{c}}} = r_{\text{a}} \cdot \frac{\sqrt{1+\frac{\omega_{\text{c}}^2}{\omega_{\text{zL}}^2}} \cdot \sqrt{1+\frac{\omega_{\text{c}}^2}{\omega_{\text{zC}}^2}}}{\sqrt{1+\frac{\omega_{\text{c}}^2}{\omega_{\text{z1}}^2}} \cdot \sqrt{1+\frac{\omega_{\text{c}}^2}{\omega_{\text{z2}}^2}}} \cdot \frac{2\zeta_{\text{e}}\sqrt{1+\frac{\omega_{\text{c}}^2}{4\zeta_{\text{e}}^2\omega_{\text{ne}}^2}}}{\sqrt{\frac{\omega_{\text{c}}^4}{\omega_{\text{ne}}^4} + 2(2\zeta_{\text{e}}^2-1)\frac{\omega_{\text{c}}^2}{\omega_{\text{ne}}^2} + 1}} \tag{17}$$

According to Eq. (16), we can also confirm (i.e., $s \to \infty$) that the high-frequency impedance value will corresponds to the ESR (r_C) of the output capacitor as it shall be. In the method presented in [15], the output impedance model has to be corrected for obtaining the known outcome.

The settling time of the transient is usually considered to be multiples of the system time constant $\tau = 1/\zeta_e \omega_{ne}$ [28]: $t_s(\pm 5\%) = 3\tau$ and $t_s(\pm 2.5\ \%) = 4\tau$, respectively. An accurate estimate can be obtained by transforming the *Laplace* or frequency domain equation in Eq. (16) into time domain.

Model Validation

Experimental measurements

The power stage of the DDR-controlled buck converter is given in Fig. 5. The switching frequency of the converter is 100 kHz. The PID controller (cf. Eq. (13)) of the converter is designed in such a manner that the controller zeros are placed at 431 Hz and 3.3 kHz, and the controller poles at 12 kHz and 43 kHz, respectively. The modulator gain ($1/V_m$) (cf. [26]) equals 1/3V. The crossover frequency (ω_c) and PM in Fig. 2 (cf. the curve 'DDR') equal 6 kHz and 51 degrees, respectively. Based the given information (cf. Eq. (9)), the estimated undamped natural frequency (ω_{ne}) and damping factor (ζ_e) can be given as 7.4 kHz and 0.49, respectively.

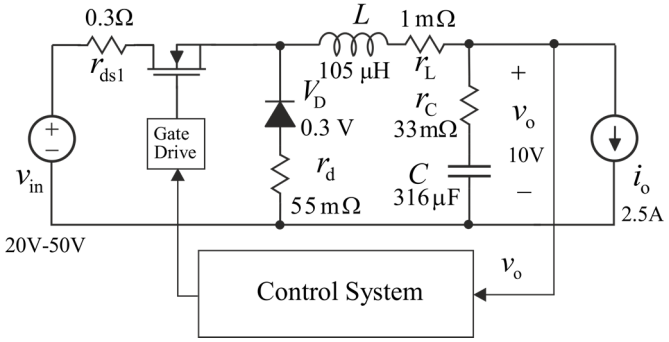

Fig. 5: Experimental DDR-controlled buck converter.

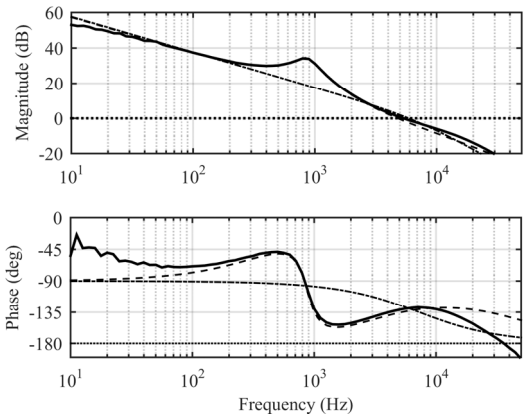

Fig. 6: Measured (solid line), predicted (dashed line), and estimated (dash-dotted lien) output voltage loop gains.

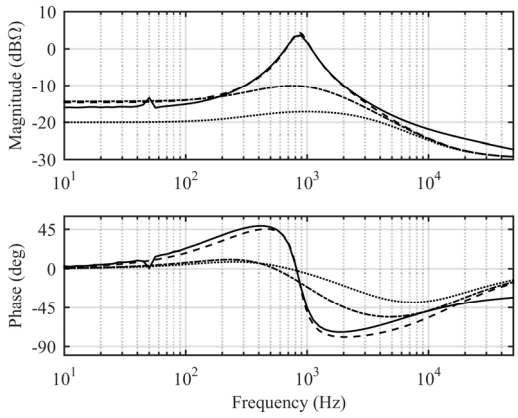

Fig. 7: Measured (solid line), predicted (dashed line), estimated 1 (dash-dotted line), and estimated 2 (dotted line)

Fig. 6 shows the measured, predicted, and estimated output-voltage loop gains for the experimental buck converter in Fig. 5, where the control system is based on an analog controller. The figure shows that the measurement set up contains extra unmodeled circuit elements at the higher frequencies, which makes the model-predicted response to deviate (i.e., the phase) from the measured one significantly. The measured, predicted, and estimated magnitude responses have quite good match.

Fig. 7 shows the measured, predicted, and estimated responses of the open-loop output impedances. The estimate 1 corresponds to the case, where the controller zeros (cf. above) have been replaced by the damped natural frequency ($\omega_{\mathrm{d}} = \omega_{\mathrm{n}}\sqrt{1-\zeta^2}$) (cf. [26],[28]). The estimate 2 corresponds to the case, where the actual controller zeros are used to produce the estimate as instructed in Eq. (15). It may be obvious that the design method to place the controller zero close to the power-stage resonant frequency will yield very good estimates as well (cf. the magnitude estimates at the frequencies below 10 kHz).

Fig. 8 shows the measured and estimated closed-loop output impedances of the experimental buck converter. The measurement shows that the output impedance contain also a series resistance, which is added into the estimate as well. The high frequency part of the estimate deviates slightly from the measured response. The measured (top figure) and estimated (bottom figure) load-transient response of the output voltage are given in Fig. 9. The estimated response describes well the initial dip and settling time but the over-shoot part deviates from the measurement, which is caused by the deviation in the high frequencies in the closed-loop output impedance. Figs. 8 and 9 indicate that the proposed method quite well models the load-current response in practice.

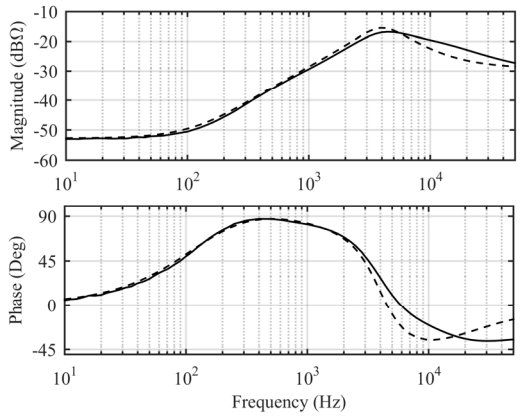

Fig. 8: Measured (solid line) and estimated (dashed line) closed-loop output impedance.

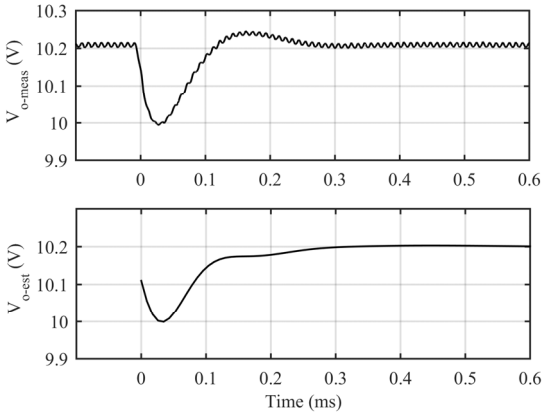

Fig. 9: Measured (top figure) and estimated (bottom figure) output-voltage load transient.

Simulation-based validation

The controller design of the converter, in Fig. 5, was revised for the simulation purposes in such a manner that the controller zeros are placed at the undamped natural frequency at $874\ \mathrm{Hz} = \dfrac{1}{2\pi\sqrt{LC}}$, the first pole to cancel the effect of the ESR zero at $15.3\ \mathrm{kHz} = \dfrac{1}{2\pi r_{\mathrm{C}} C}$, and the last pole at half the switching frequency, respectively. The crossover frequency and PM equal 10 kHz and 60 degrees, respectively. The crossover frequency and PM will give the estimates (cf. Eq. (9)) for the closed-loop-system ω_{ne} and ζ_{e} as 87613 rads/s and 0.6186, respectively.

The obtained output-voltage loop gain (solid line) and the estimated loop gain (dashed line) (cf. Eq. (6)) are presented in Fig. 10 and the corresponding sensitivity functions (cf. Eq. (7)) in Fig.11, where the solid line represent the original response, and the dashed line the estimated response. Figs. 10 and 11 indicate that the estimates model very well the original loop gain and the sensitivity function as well.

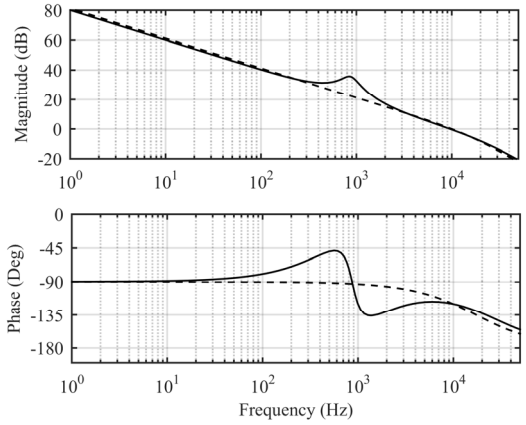

Fig. 10: Output-voltage loop gains: Original (solid line) and estimated (dashed line).

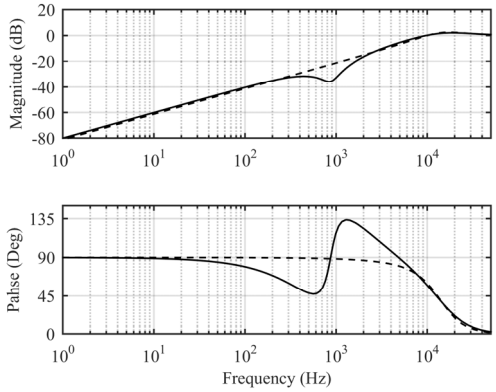

Fig. 11: Sensitivity functions: Original (solid line) and estimated (dashed line).

Fig. 12 shows the predicted and estimated closed-loop output impedance of the converter based on the modified control design. The match is very good as the output-voltage step responses in Fig. 13 also clearly indicates.

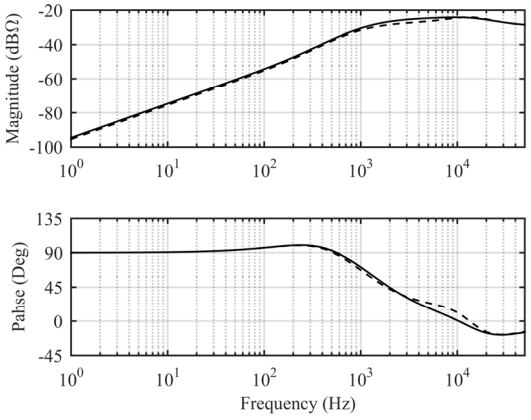

Fig. 12: The predicted (solid line) and estimated (dashed line) closed-loop output impedances.

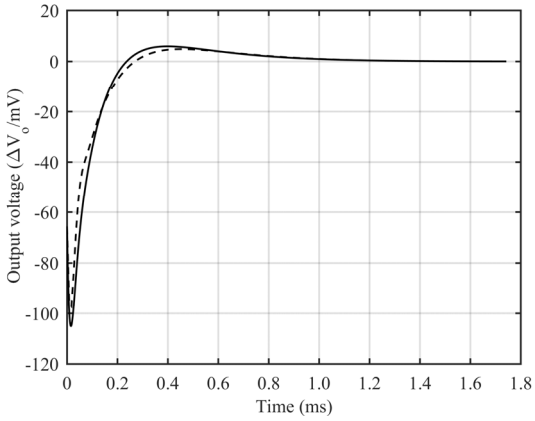

Fig. 13: The predicted (solid line) and estimated (dashed line) response of the output voltage to a step change in output current.

Conclusions

This paper presents a method to model the load-transient response of the output voltage of a DDR-controlled buck converter based on the crossover frequency and phase margin of the output-voltage feedback loop as well as a clever estimation of the open-loop output impedance. The experimental and simulation-based validation indicates that the proposed technique yields very good results. Similar method has not been presented earlier in the open literature as far as the authors know.

References

[1] T. Nabeshima, and K. Harada, "Large-signal transient responses of a switching regulator," *IEEE Trans. Aerosp. Electron. Syst.*, vol. AES-18, no. 5, pp. 545-551, Sep. 1982.

[2] R. D. Middlebrook, and S. Ćuk, "A general unified approach to model switching-converter power stages," *Int. J. Electron.*, vol. 42, no. 6, pp. 521-550, Jun. 1977.

[3] R. Redl, B. P. Erisman, and Z. Zansky, "Optimizing the load transient response of the buck converter," in *Proc. IEEE APEC*, 1998, pp. 170-176.

[4] J. Betten, and R. Kollman, "Easy calculation yields load transient response," *Power Electron. Tech.*, pp.40-48, Feb., 2005.

[5] C. Gezgin, "Predicting load transient response of output voltage in DC-DC converters," in *Proc. IEEE APEC*, 2004, pp. 1339-1344.

[6] R. Redl, and N. O. Sokal, "Near-Optimum dynamic regulation of DC-DC converters using feed-forward of output current and input voltage with current-mode control," *IEEE Trans. Power Electron.*, vol. PE-1, no. 3, pp. 181-191, Jul. 1986.

[7] L. Varga, and N. Losic. "Synthesis of zero-impedance converter," *IEEE Trans. Power Electron.*, vol. 7, no. 1, pp. 152-70, Jan. 1989.

[8] A. V. Peterchev, and S. R. Sanders, "Load-line regulation with estimated load-current feedforward: Application to microprocessor voltage regulators," *IEEE Trans. Power Electron.*, vol. 21, no. 6, pp. 1704-1717, Nov. 2006.

[9] M. Karppanen, M. Hankaniemi, T. Suntio, and M. Sippola,"Dynamical characterization of peak-current-mode – controlled buck converter with output-current feedforward," *IEEE Trans. Power Electron.*, vol. 22, no. 2, pp. 444-451, Mar. 2007.

[10] G. Eirea, and S. R. Sanders, "Adaptive output current feedforward control in VR applications," *IEEE Trans. Power Electron.*, vol. 23, no. 4, pp. 1880-1887, Jul. 2008.

[11] J. Cortés. V. Šviković, P. Alou, et al., "Improved transient response of controllers by synchronizing the modulator with the load step: Application to V^2I_C," *IEEE Trans. Power Electron.*, vol. 30, no. 3, pp. 1577-1590, Mar. 2015.

[12] J. Sha, Y. Chen, J. Xu, and B.W. Williams, "A peak-capacitor-current pulse-train-controlled buck converter with fast transient response and a wide load range," *IEEE Trans. Ind. Electron.*, vol. 63, no. 3, pp. 1528-1538, Mar. 2016.

[13] S. Kapat, P. S. Shenoy, and P. T. Krein, "Near-Null response to large signal transients in an augmented buck converter: A geometric approach," *IEEE Trans. Power Electron.*, vol. 27, no. 7, pp. 3319-3329, Jul. 2012.

[14] T. Suntio and J. Kivimäki, "Physical inside into the factors affecting the load transient response of a buck converter," in *Proc. EPE ECCE Europe*, 2014, pp. 1-10.

[15] B. Choi, "*Pulsewidth Modulated DC-to-DC Power Conversion – Circuits, Dynamics, and Control Designs*," IEEE Press, Inc., John Wiley & Sons, Inc., Hoboken, NJ, USA, 2013.

[16] A. Cantillo, A. De Nardo, N. Femia, and W. Zamboni, "A unified practical design method for capacitors of switching converters," ," *IEEE Trans. Ind. Electron.*, vol. 58, no. 8, pp. 3521-3536, Aug. 2011.

[17] A. De Nardo, N. Femia, G. Petrone, and G. Spagnuolo, 'Optimal buck converter output filter design for point-of-load applications," *IEEE Trans. Ind. Electron.*, vol. 576, no. 4, pp. 1330-1341, Apr. 2010.

[18] P. L. Wong, F. C. Lee, and K. Yao, "Critical inductance in voltage regulator module," *IEEE Trans. Power Electron*., vol. 17, no. 4, pp. 485-492, Jul. 2002.

[19] J. T. Su, and C. W. Liu, "Gain scheduling control scheme for improved transient responses of DC/DC converters," *IET Power Electron.*, vol. 5, no. 6, pp. 678-692, Jul. 2012.

[20] A. T. L. Lee, J. K. O. Sin, and P. C. H. Chan, "Adaptive high-bandwidth digitally controlled buck converter with improved line and load transient response," *IET Power Electron.*, vol. 7, no. 3, pp. 515-526, Mar. 2014.

[21] K. Yao, Y. Ren, and F. C. Lee, "Critical bandwidth for the load transient response of voltage regulator modules," *IEEE Trans. Power Electron.*, vol. 19, no. 6, pp. 1454-1461, Nov. 2004.
[22] J. S. Chang, H. S. Oh, Y. H. Jun, and B. S. Kong, "Fast output voltage-regulated PWM buck converter with an adaptive ramp amplitude control," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 60, no. 10, pp. 712-716, Oct. 2013.
[23] Y. H. Lee, S. C. Huang, S. W. Wang, and K. H. Chen, "Fast transient (FT) technique with adaptive phase margin (APM) for current mode DC-DC buck converters," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 20, no. 10, pp. 1781-1793, Oct. 2012.
[24] M. Di Lorenzo del Casale, N. Femia, P. Lamberti, and V. Mainardi, "Selection of optimal closed-loop controllers for DC-DC voltage regulators based on nominal and tolerance design," *IEEE Trans. Ind. Electron.*, vol. 51, no. 4, pp. 840-849, Aug. 2004.
[25] J. C. Basilio and S. R. Matos, "Design of PI and PID controllers with transient performance specifications," *IEEE Trans. Edu.*, vol. 45, no. 4, pp. 364-370, Nov. 2002.
[26] T. Suntio, *Dynamic Profile of Switched-Mode Converter – Modeling, Analysis and Control*, Wiley-VCH, Weinheim, Germany, 2009.
[27] Huusari J., Leppäaho, J., and Suntio T., 'Dynamic properties of PCM-controlled superbuck converter – Discrete vs. coupled inductor implementation,' *Eur. Power Electron. Drives J. (EPE Journal)*, vol. 20, no. 2, pp. 8-15, Jun. 2010.
[28] K. Ogata, *Modern Control Engineering*, Prentice-Hall: Upper Saddle River, NJ, USA, 1997 (pp. 549-552).
[29] T. Suntio, M. Hankaniemi, and T. Roinila,"Dynamical modelling of peak-current-mode controlled converter in continuous conduction mode," *J. Simul. Modelling Pract. Theory*, vol. 15, no. 10, pp. 1320-1337, Nov. 2007.
[30] B. Choi, "Step load response of a current-mode-controlled DC-to-DC converter," *IEEE Trans. Aerosp. Electron. Syst.*, vol. 33, no. 4, pp. 1115-1121.
[31] J. Kivimäki, M. Sitbon, S. Kolesnik, et al., "Determining maximum MPP-tracking sampling frequency for input-voltage-controlled PV interfacing converters," in *Proc. IEEE ECCE*, 2016, pp. 1-8.
[32] M. Hankaniemi, M. Karppanen, and T. Suntio, "Dynamical characterization of voltage-mode controlled buck converter operating in CCM and DCM," in *Proc. EPE-PEMC*, 2006, pp. 816-821.
[33] T. Suntio, "Unified average and small-signal modeling of direct-on-time control," *IEEE Trans. Ind. Electron.*, vol. 53, no. 1, pp. 287-295, Feb. 2006.