Advanced Architectures for Self-interference Cancellation in Full-duplex Radios: Algorithms and Measurements

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***Abstract*—In this paper, we describe an advanced real-time cancellation architecture for efficient digital-domain suppression of self-interference in inband full-duplex devices. The digital canceller takes into account the nonlinear distortion produced by the transmitter power amplifier, and is thereby a robust solution for low-cost implementations. The developed real-time digital canceller implementation is then evaluated with actual RF measurements, where it is complemented with a real-time adaptive RF canceller. The obtained results show that the RF canceller and the developed digital canceller implementation can together cancel the residual self-interference below the receiver noise floor in real-time for a 20 MHz cancellation bandwidth.**

I. Introduction

Inband full-duplex communications, where transmission and reception occur simultaneously on the same center-frequency, has been receiving a great deal of attention in the recent years [1]–[6]. Especially, the potentially two-fold improvement in spectral efficiency makes inband full-duplex an intriguing technology for the next generation wireless networks [7], [8]. However, in order to realize the throughput gains, the problem of self-interference (SI) must first be solved. This problem is caused by the fact that a full-duplex transceiver will also receive its own transmit signal, which can be as much as 100–120 dB stronger than the desired signal of interest [9]. Moreover, typical filtering or duplexing techniques cannot be applied in this case since the SI is overlapping with the desired signal also in the frequency domain.

There have already been various demonstrator implementations of inband full-duplex transceivers, which are capable of very efficient SI suppression [1]–[3], [10]. In some cases, the SI is in fact fully cancelled below the receiver noise floor [2], [3], [10]. This indicates that the main principles of SI cancellation are already well studied and proven to work efficiently under realistic circumstances.

However, what remains to be shown is implementing a fully *real-time* SI cancellation architecture with realistic cancellation bandwidths. In particular, considering a typical system with two active SI cancellation stages, one in the RF domain and one in the digital domain, in the demonstration implementations reported so far at least the digital cancellation procedure is performed offline on a previously measured and stored signal [2], [3], [10]. Real-time RF cancellation has already been successfully demonstrated by different research groups [2], [11]. On the other hand, to the best of our knowledge, no real-time implementation of a *nonlinear digital SI canceller* has been so far reported in the literature.

Hence, in this work we provide a detailed study of a real-time nonlinear digital SI canceller, which has been implemented on a field-programmable gate array (FPGA). It is shown with actual RF measurements to cancel the residual SI below the receiver noise floor under a wide range of circumstances. Especially, the real-time digital canceller is shown to perform well when combined with a previously implemented real-time adaptive RF canceller. Thus, together these two cancellation stages constitute a highly adaptive and efficient real-time cancellation architecture for an inband full-duplex device.

The rest of this paper is organized as follows. In Section II the general principles behind real-time SI cancellation techniques are described, alongside with the considered full-duplex transceiver architecture. Then, in Section III the implementation of the real-time digital SI canceller is discussed in detail. After this, the measurement results are reported and analyzed in Section IV. Finally, the conclusions are drawn in Section V.

II. Achieving Real-Time Inband Full-Duplex Operation

In order to obtain true inband full-duplex operation in real-time, several adaptive SI cancellation stages are required, which suppress the SI signal below the receiver noise floor under time-varying conditions. In this work, the full-duplex implementation utilizes two active cancellation stages, in addition to which a circulator is used to introduce passive isolation. The circulator also allows the system to have only one shared antenna for both transmission and reception.

A. Overall Full-Duplex Device Architecture

The single-antenna inband full-duplex transceiver considered in this work is illustrated on a general level in Fig. 1. The National Instruments (NI) FlexRIO 5791 is used as the actual transceiver, which is complemented by an external power amplifier (PA) in order to boost the transmit power. The shared antenna operation is facilitated by a circulator, which separates the transmitter and receiver ports while connecting them to the same antenna [2], [3], [12].

Having transmitted the signal, it is coupled back to the receiver via (i) the direct leakage through the circulator, (ii) the reflection from the antenna, produced due to its inherent

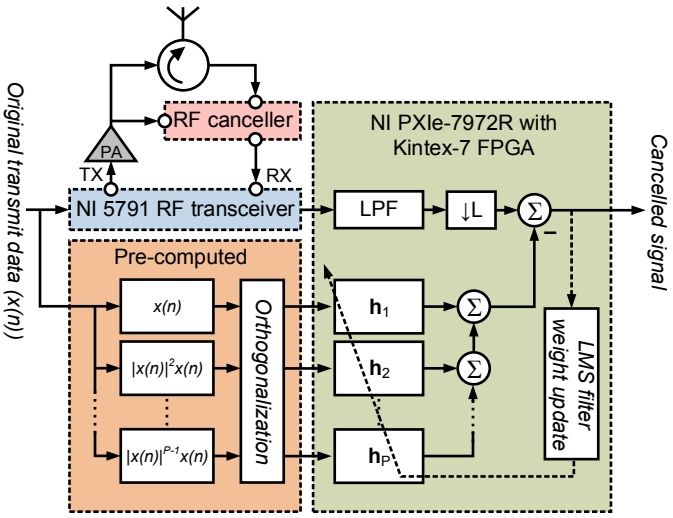

Fig. 1: A block diagram of the real-time implementation of the digital SI canceller. Note that here the coefficient vector $\mathbf{h}$ has been split into the coefficients of the individual basis function as $\mathbf{h}_p$, $p = 1, 3, \ldots, P$.

input impedance mismatch, and (iii) the multipath reflections received by the antenna. In the considered implementation, the direct leakage and the antenna reflection are first suppressed by an active RF canceller, which attenuates the SI to more tolerable levels. Essentially, the used RF canceller constructs a replica of the observed SI with a digitally-controlled adaptive RF filter by utilizing the PA output as a reference signal. For more information regarding the RF canceller, refer to [11].

After RF cancellation, the remaining signal is fed to the NI 5791 receiver, which digitizes it and forwards it to a NI FlexRIO PXIe-7972R FPGA module with a Kintex-7 FPGA board, on which the real-time digital canceller is running. Since both the NI 5791 transceiver and the NI PXIe-7972R FPGA module are connected to the same NI PXIe-1073 chassis, a high-speed data link between them can be established. This means that the digital canceller is capable of processing the received signal in real-time. After digital cancellation, the remaining signal can be fed to a host PC for offline analysis, or its spectrum can be displayed in real-time.

B. Algorithm for Adaptive Nonlinear Digital Self-Interference Cancellation

An integral component in any full-duplex device is the digital canceller [2], [9], [12], as already discussed above. The reason for this is that it is typically not cost-efficient to try to perform all of the SI cancellation in the RF/analog domain. This means that there is some residual SI still in the digital domain, which must be efficiently cancelled using digital signal processing techniques. Furthermore, due to the inherent nonidealities especially in the transmitter, an advanced processing structure incorporating all the significant distortions is required in the digital cancellation stage [2], [3], [9]. In practice, modeling the nonlinearity of the transmitter power amplifier (PA) is typically sufficient, since that is the dominant source of distortion, especially when IQ matching is reasonably good [9].

There is already a wide body of literature regarding the digital SI cancellation [2], [12]–[15], but to the best of our knowledge there are no existing works where a real-time implementation of such a nonlinear digital canceller is described in detail. Hence, in this work we describe an actual real-time FPGA implementation of a nonlinear and fully adaptive digital SI canceller. We also show with actual RF measurements that the real-time digital canceller performs well together with an adaptive RF canceller.

In particular, the implemented digital canceller utilizes a parallel Hammerstein signal model, for which an instantaneous basis function vector can be defined as follows:

$$\mathbf{\Phi}(n) = \begin{bmatrix} \phi_1(x(n)) & \phi_3(x(n)) & \cdots & \phi_P(x(n)) \end{bmatrix}^T, \quad (1)$$

where $\phi_p\left(x(n)\right) = |x(n)|^{p-1}\, x(n)$ is the pth-order nonlinear basis function, $x(n)$ is the original digital transmit waveform, and P is the nonlinearity order of the model [12], [13]. Since the nonlinear canceller is modeling only the transmitter PA, which is producing the majority of the nonlinear distortion, it is sufficient to consider only the odd-order basis functions.

Furthermore, since the different nonlinearity orders are typically highly correlated, they must be first orthogonalized for any adaptive learning algorithm to work efficiently. This can be done by utilizing an orthogonalization matrix, denoted by $\mathbf{S}$, which can be obtained as described in [12]. Then, the orthogonalized basis function vector can be expressed as:

$$\widetilde{\mathbf{\Phi}}(n) = \mathbf{S}\mathbf{\Phi}(n). \quad (2)$$

The actual digital cancellation procedure is simply performed with an LMS-based learning algorithm. Using (2), the input of the overall LMS filter $\mathbf{h}(n)$, consisting of the coefficients of all the basis functions at iteration n, can be written as

$$\mathbf{u}(n) = \begin{bmatrix} \widetilde{\mathbf{\Phi}}(n+M_1)^T & \widetilde{\mathbf{\Phi}}(n+M_1-1)^T & \cdots & \widetilde{\mathbf{\Phi}}(n-M_2)^T \end{bmatrix}^T \quad (3)$$

where M_1 and M_2 are the amounts of pre-cursor and post-cursor memory, respectively. Then, the cancelled signal at time-instant n can be written as

$$y_{DC}(n) = y_{RF}(n) - \mathbf{h}(n)^H \mathbf{u}(n), \quad (4)$$

where $y_{RF}(n)$ denotes the received (and possibly RF cancelled) signal in the digital domain, and $(\cdot)^H$ is the Hermitian transpose. Finally, the coefficients of the canceller are updated as follows:

$$\mathbf{h}(n+1) = \mathbf{h}(n) + \mu y_{DC}^*(n)\mathbf{u}(n), \quad (5)$$

where μ is a the step size and $(\cdot)^*$ denotes the complex conjugate. The coefficient vector is typically initialized as $\mathbf{h}(0) = \mathbf{0}$, assuming no further side-information is available. This type of an LMS-based nonlinear digital canceller is capable of accurate regeneration of the residual SI under a nonlinear PA, while also efficiently tracking the coefficients under time-varying SI channel conditions.

III. Real-Time Digital Canceller Implementation

The implementation of the digital canceller is then done on an FPGA, as already explained, using the Labview programming environment and fixed-point arithmetic. The implementation is illustrated on a general level in Fig. 1, where its block diagram is shown, and the used parameters are listed in Tables I and II. In particular, the NI 5791 is used as the transceiver, and all the computations related to the transmission and reception are done using its internal Virtex-5 SX50T FPGA. The actual LMS learning and cancellation procedure, described by (4) and (5), is then performed on a separate Kintex-7 XC7K325T FPGA, running on an NI PXIe-7972R module. Furthermore, since the NI PXIe-7972R is connected to the NI 5791 transceiver via a high-speed data bus provided by the used NI PXIe-1073 chassis, the digital cancellation can be performed in real-time.

Having received the SI signal, the NI 5791 receiver first digitizes it with a sampling frequency of 130 MHz and using 16 bits for the in-phase (I) and quadrature-phase (Q) components. Since the communication bandwidth in this implementation is 20 MHz, the received SI signal is then low-pass filtered and decimated by a factor of 5 to a sampling frequency of 26 MHz. After this, the signal is forwarded to the Kintex-7 FPGA, on which the digital canceller is running. Note that the clock frequency on the Kintex-7 is still 130 MHz, meaning that 5 clock cycles can be used to produce one output sample of the cancelled signal.

On the FPGA, the LMS iteration described by (4) and (5) is performed for each incoming sample. In particular, in this implementation four basis functions are used, each of them having 27 memory taps. This amounts to 108 coefficients in total, which are updated during each LMS iteration. With the used hardware, this is the highest number of coefficients that can be reliably supported.

In order to simplify the implementation, the orthogonalized basis functions used in the LMS iteration are computed offline, meaning that they can be saved to the internal block random access memory (RAM) of the Kintex-7, without having to generate them in real-time. This is possible due to the fact that the same transmit signal sequence is continuously repeated, which means that only the orthogonalized basis functions corresponding to the repeating sequence must be saved to the memory. Each basis function is stored into the memory with a fixed-point representation using 25 bits as described in Table II. As a future work item, we consider implementing also the basis function generation on the FPGA.

The complexity of the coefficient update rule is decreased by implementing the step size μ as a simple bit shift operation. Moreover, it was observed that using 25 bits for representing the coefficients ensures a sufficient accuracy in the cancellation stage. After canceling the current received sample according to (4), each cancelled sample in $y_{DC}(n)$ is truncated to 16 bits and forwarded for further processing and/or saved to a host PC for offline analysis. Altogether, the digital cancellation processing results in a delay of 17 clock cycles, which corresponds to roughly 130 ns.

TABLE I: The essential parameters of the real-time nonlinear digital canceller implementation.

Parameter	Value
Clock frequency of the canceller	130 MHz
Sampling frequency of the signal	26 MHz
Delay of the canceller	17 cycles (130 ns)
Highest nonlinearity order (P)	7
Number of pre-cursor taps (M_1)	13
Number of post-cursor taps (M_2)	14
Step size (μ)	2^{-13}

TABLE II: The number of bits used at different stages of the digital canceller.

Signal/variable	Integer part	Fractional part
Received signal	1 bit	15 bits
Basis functions (in memory)	8 bits	17 bits
Coefficients	1 bit	24 bits
Canceller output	1 bit	15 bits

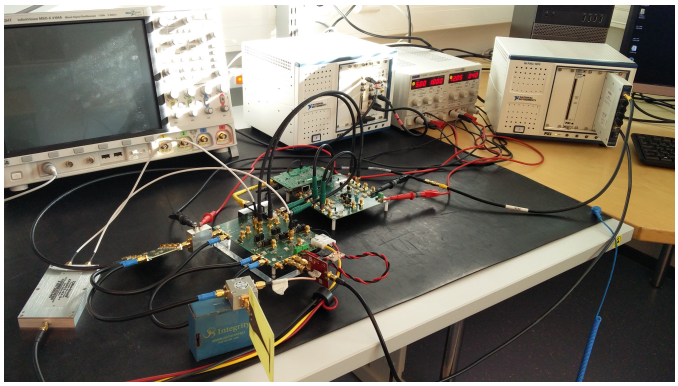

Fig. 2: The RF measurement setup.

TABLE III: The relevant parameters related to the RF measurements.

Parameter	Value
Bandwidth	20 MHz
Center frequency	2.45 GHz
PA gain	24 dB
Receiver noise floor (over 20 MHz)	−87.9 dBm

IV. Measurement Results

Let us then evaluate the performance of the implemented digital SI canceller with actual RF measurements, using the parameters specified in Table III and the measurement setup shown in Fig. 2. In the measurements, the digital canceller is evaluated under two different scenarios: (i) with a previously implemented three-tap RF canceller, and (ii) with an RF attenuator representing analog SI cancellation. The latter case is considered in order to accurately test the limits of the digital canceller in relation to the achieved amount of RF cancellation, since it is impractical to manually vary the cancellation performance of the actual active RF canceller.

In the transmission stage, the output signal of the NI 5791 transmitter is first amplified by an external PA, which provides a gain of 24 dB. When using the RF canceller, part of the PA output signal is routed to the RF cancellation board, resulting

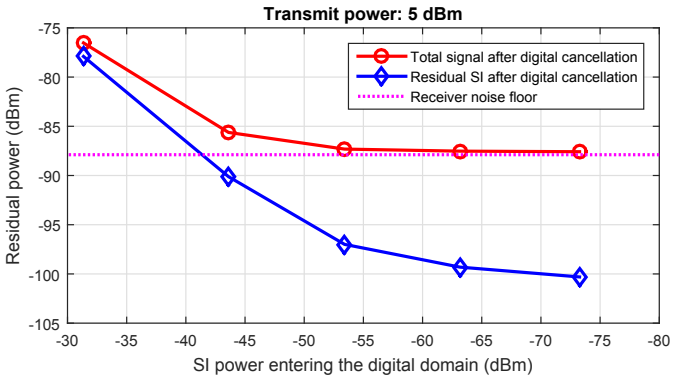

Fig. 3: The residual SI level after digital cancellation for different input SI power levels.

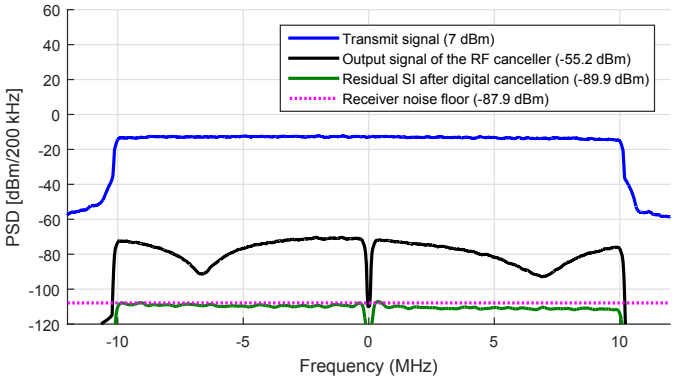

Fig. 4: The signal spectra after the different SI cancellation stages.

in a power loss of 6 dB in the TX path. The remaining PA output signal is then fed directly to the circulator connecting the transmitter and receiver to a shared TX/RX antenna. Note that in the measurements where the RF canceller is not used the PA output is directly connected to the circulator. The overall transmit power is typically in the order 5–12 dBm, depending on the chosen output power level of the NI 5791 transmitter. The received signal is then routed via the circulator either to the RF canceller or to an external RF attenuator, after which it is fed to the NI 5791 RX port and processed in real-time by the digital canceller on the Kintex-7 FPGA.

Furthermore, to properly evaluate the SI cancellation performance of the implemented digital SI canceller, in the post-processing stage the residual SI signal is averaged to remove the noise. This is made possible due to the fact that the transmitter is repeatedly transmitting the same transmit signal sequence. Hence, the residual signal consists of (i) the actual residual SI, which is directly related to the actual transmit signal and hence repeats practically in similar form over and over again, and (ii) the receiver noise and other interference sources which are different for each repeating transmit signal period. Thereby, by averaging over enough of the repeating periods of the transmit signal, only the true residual SI remains and the time-variant noise and interference sources are removed. However, the averaging must be done over sufficiently short periods of time to ensure that the coefficients of the SI cancellers and the actual propagation channel remain constant.

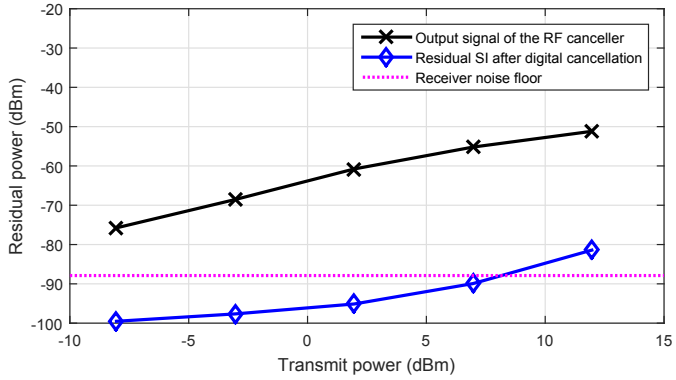

Fig. 5: The residual SI after RF and digital cancellation for different transmit powers.

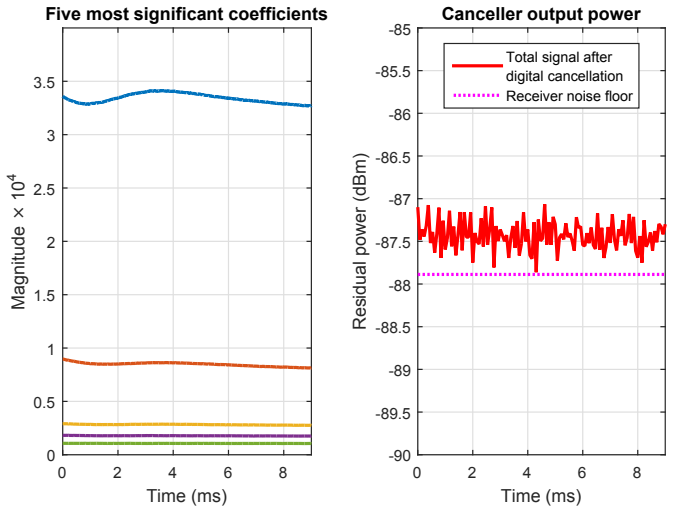

Fig. 6: The magnitudes of the five most significant coefficients while disturbing the antenna, alongside with the corresponding total residual power after the digital canceller.

To first investigate the relationship between RF and digital cancellation, Fig. 3 shows the residual SI level after the digital canceller with respect to the SI power entering the digital domain, with the transmit power being fixed to 5 dBm. The SI power has been varied by replacing the RF canceller with RF attenuators, as explained above, which allows for the precise tuning of the SI power. Since the attenuator directly replaces the RF canceller, from the digital canceller's perspective it can be interpreted as the active RF cancellation level. Moreover, in Fig. 3 both the total residual power and the residual SI power are shown, where the latter has been obtained by the described averaging procedure. Note that by summing the pure residual SI and the known receiver noise power, the total residual signal power is obtained. Overall, Fig. 3 indicates that, in order to push the residual SI well below the receiver noise floor, the SI power level entering the digital domain should be -55 dBm or less. With higher input SI powers, the residual SI power will result in an increased noise-plus-interference floor.

Based on the reported performance of our RF canceller [11], it can be calculated that the SI power after RF cancellation will be in the order of -55 dBm when the transmit power is roughly 7 dBm. Hence, Fig. 4 shows the spectra of the

SI signal in the different stages of the full-duplex transceiver for this particular transmit power. It can indeed be observed that now the residual SI after the digital canceller, which has again been calculated by averaging the total residual signal, is practically at the level of the receiver noise floor, indicating efficient real-time SI cancellation, although the performance with an actual RF canceller is somewhat worse than with the ideal attenuator. Without the averaging, the overall residual signal contains the receiver noise and the noise produced by the RF canceller, and hence its power level is slightly higher. However, in practical systems, canceling the SI below the receiver noise floor is not likely required, since there are other dominating interference sources.

Then, let us investigate the overall integrated cancellation performance with different transmit powers. This shows the boundaries of the current real-time SI cancellation solution, consisting of both the RF and the digital canceller. To this end, Fig. 5 plots the residual SI power after the digital canceller with respect to the transmit power, alongside with the RF canceller output power. It can be observed that the current overall cancellation performance limits the full-duplex transceiver to relatively low transmit powers, in the order of 0–10 dBm. Especially, the real-time digital canceller can suppress the SI by 25–35 dB, which is sufficient for the lower transmit power levels but, in order to support higher transmit powers, also the modeling accuracy of the digital canceller should be improved. Nevertheless, these transmit power levels are already sufficient for the future ultra-dense 5G networks where inter-site distances in the order of 50–100 m are to be expected [16], [17].

Finally, in order to evaluate the tracking capabilities of the digital canceller, Fig. 6 shows the magnitudes of the five most significant coefficients with respect to time, while the antenna is intentionally disturbed. In order to concentrate on the tracking of the digital canceller, the RF canceller has been replaced by a 40 dB attenuator, with the transmit power fixed again to 5 dBm. For reference, the total residual signal power after digital cancellation, including also the receiver noise, is also shown in Fig. 6. It can be observed that the coefficients are following the changes in the environment, while the residual power remains more or less constant. This demonstrates the excellent tracking capabilities of the digital canceller.

V. Conclusion

In this paper, we presented a comprehensive real-time self-interference cancellation solution for inband full-duplex radios, consisting of active RF and digital cancellers operating in real-time. In particular, the developed digital canceller is capable of adaptive learning and nonlinear modeling of the residual self-interference waveform, rendering it capable of efficient cancellation also under a low-cost transmitter power amplifier. The real-time digital canceller was then evaluated with actual RF measurements and was shown to cancel the residual SI below the receiver noise floor when complemented with the active RF canceller. To the best of our knowledge, such performance has not been previously reported for a real-time implementation of a nonlinear digital canceller.

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