Model Predictive Control of the Interleaved DC-DC Boost Converter

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***Abstract*— This paper extends the recently introduced approach to the modeling and control design in the framework of model predictive control of the dc-dc boost converter to the dc-dc parallel interleaved boost converter. Based on the converter's model a constrained optimal control problem is formulated and solved. This allows the controller to achieve (a) the regulation of the output voltage to a predefined reference value, despite changes in the input voltage and the load, and (b) the load current balancing to the converter's individual legs, by regulating the currents of the circuit's inductors to proper references, set by an outer loop based on an observer. Simulation results are provided to illustrate the merits of the proposed control scheme.**

I. Introduction

DC-DC converters are widespread power electronics circuits with advantageous features, such as small size, light weight, and high efficiency. They are used in applications where dc-dc conversion between different voltage levels is needed, like dc power supplies and dc motor drive systems [1]. Despite the fact that the switch-mode dc-dc conversion is a mature technology, the problems associated with these applications and their closed-loop controlled performance still pose theoretical and practical challenges. The emergence of new applications with more demanding performance requirements, coupled with the development of novel computational control techniques, made possible by the increased computational power of the available control platforms, leads to new approaches to the control problem.

In this paper we aim to tackle the problem of the control of the dc-dc parallel interleaved boost converter from the perspective of the model predictive control (MPC). MPC has successfully established itself as a systematic control method with numerous applications, from the automotive [2], power systems operation [3] and fuel cell control [4] to power electronics industry. In the latter the MPC has been implemented for several topologies [5]–[11]. Specifically, in the field of dc-dc converters a number of publications have appeared [12]–[14] where the method demonstrated a significant potential in achieving important performance improvements. The main advantage of this method is its straightforward design procedure. It is based on the discrete-time predicted model of the system, enhanced by an objective function composed of terms that penalize the deviation of the predicted system behavior, and a set of inputs which are derived from the assigned control objectives. In each sampling instant, the input resulting from the minimization of the assigned objective function that yields the best predicted performance of the system is chosen. This input is called optimal.

Regarding the material presented in this paper, the chosen topology is the dc-dc parallel interleaved boost converter. The converter is consisted of two parallel legs, in respect to the power supply and the common load. The benefits arising from the parallelization are many [15]. To name the most important are the cost reduction and the higher reliability. For the first, the components used could be less expensive, since the load current is equally distributed to the individual converter legs, which means that the power stages can handle lower currents. For the latter, since the failure of a parallel leg does not disrupt the converter's operation, this increases the fault tolerance of the topology. However, in reality the parallel legs cannot be identical due to several reasons, such as components mismatching, both in the inductance and in the power semiconductors, and parameter variations caused by the temperature increase. Thus, the power switches should be turned on and off in such a way that the load current will be shared equally to both legs. This is the first control objective. Furthermore, the output voltage of the converter should be regulated to a desired value despite changes in the input voltage and the load. This is the second control objective.

The controller is designed by taking into consideration the control objectives mentioned above. The control method introduced here comprises the two loops that are commonly used in the control operation of the dc-dc converters; an inner loop which drives the currents of the individual legs to specified references, and an outer loop which calculates these references based on the regulation of the output voltage to a desired voltage level. However, as proposed in [16], since the present work extends the research done there for the dc-dc boost converter, the difference in the approach of how these loops are employed is the following: the inner current control regulation problem is posed in the MPC framework, while in the outer loop the inductor current references are derived from the converter's power balance expression, where the estimated load current is used. In order to go into more detail, as shown in [12]–[14], and [17] the inner current control loop is formulated using hysteresis bounds for the parallel legs inductor currents, in the proposed MPC modeling, using soft constraints.

The control method presented here has several benefits. The most prominent are the very fast current dynamics that

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MPC can deliver, combined with the guaranteed robustness and stability of the method, since the closed-loop performance is independent from the operating point. Moreover, excessive iterations and tuning are avoided due to its straightforward implementation, since the control objectives are expressed in the objective function of the optimal controller. In addition, the proposed approach rejects disturbances in the input voltage and the load. Furthermore, due to the model-based nature of the controller and its design simplicity, it can be easily extended to interleaved topologies with more individual legs. On the other hand, the proposed control scheme shows some inherent drawbacks. The use of longer prediction horizon increases exponentially the computational power needed, while the absence of a modulator and the direct manipulation of the converter switches imply a variable switching frequency.

This paper is organized as follows. In Section II, the topology of the considered converter is presented, showing the nonlinear continuous-time state space model, and the derivation of the discrete-time model of the system that is suitable for the controller. In Section III, an optimal control problem incorporating the appropriate control objectives is formulated. The way is explained in which the load estimation setup is employed. Section IV provides simulation results to show the performance of the proposed control scheme. Finally, the paper is summarized in Section V, where conclusions are also drawn.

II. Mathematical Model

A. Continuous-Time Model

The dc-dc parallel interleaved boost converter (Fig. 1) consists of two legs, each of which includes one inductor, L_n, and the corresponding internal resistor R_{Ln}, and the power semiconductors; the controllable switch, S_n, and the dually operated diode, D_n, with $n = 1, 2$. The mathematical representation of the converter in the continuous-time state space is given by the following equations [18]

$$\frac{dx(t)}{dt} = \big(A_1 + A_2 \cdot u(t)\big) \cdot x(t) + B \cdot w(t) \tag{1a}$$

$$y(t) = C \cdot x(t) \tag{1b}$$

where

$$x(t) = [i_{L_1}(t)\ i_{L_2}(t)\ v_o(t)]^T, \qquad w(t) = [v_i(t)\ i_o(t)]^T,$$

$$A_1 = \begin{bmatrix} -\frac{R_{L_1}}{L_1} & 0 & -\frac{1}{L_1} \\ 0 & -\frac{R_{L_2}}{L_2} & -\frac{1}{L_2} \\ \frac{1}{C_o} & \frac{1}{C_o} & 0 \end{bmatrix}, \quad A_2 = \begin{bmatrix} \frac{1}{L_1} & 0 & 0 \\ 0 & \frac{1}{L_2} & 0 \\ 0 & 0 & -\frac{1}{C_o} \end{bmatrix},$$

$$B = \begin{bmatrix} \frac{1}{L_1} & 0 \\ \frac{1}{L_2} & 0 \\ 0 & -\frac{1}{C_o} \end{bmatrix}, \ C = [0\ 0\ 1], \text{ and } u = \begin{bmatrix} 0 & 0 & u_1 \\ 0 & 0 & u_2 \\ u_1 & u_2 & 0 \end{bmatrix}$$

where C_o is the filter capacitance, $i_{L_n}(t)$ the n-inductor current, $i_o(t)$ the load current, $v_o(t)$ the output voltage, and $v_i(t)$ the input voltage. Finally the variable u_n defines the switching position, i.e. $u_n = 1$, when the switch S_n is on, and $u_n = 0$, when the switch S_n is off. Thus, the converter features 2^n operation modes with equal affine equations.

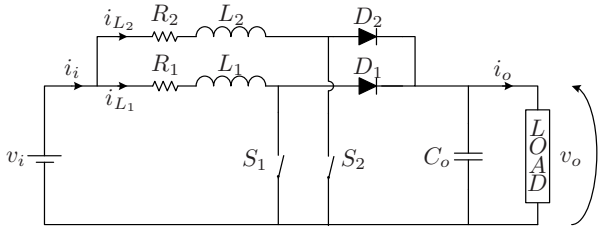


Fig. 1: Topology of the dc-dc parallel interleaved boost converter.

B. Discrete-Time Model

Starting from the continuous-time state space model developed in the previous section, the goal of this section is the derivation of a mathematical model of the converter suitable for the controller. Since MPC is a discrete-time controller the model is discretized using first-order approximation. This leads to the following discrete-time state space model, defined as

$$x(k+1) = \big(A_{1,d} + A_{2,d} \cdot u(k)\big) \cdot x(k) + B_d \cdot w(k) \tag{2a}$$

$$y(k) = C_d \cdot x(k) \tag{2b}$$

where

$$x(k) = [I_{L_1}(k)\ I_{L_2}(k)\ V_o(k)]^T,\ w(k) = [V_i(k)\ I_o(k)]^T,$$

$$A_{1,d} = (I + A_1 \cdot T_s), \qquad A_{2,d} = A_2 \cdot T_s, \qquad B_d = B \cdot T_s,$$

$C_d = C$, and $u(k) = u$

where capital letters denote the discrete time-varying physical quantities, and T_s the sampling time.

III. Controller Design

In this section the design of the nominal controller is presented. The controller design is done in three steps. Firstly, an objective function has to be defined. Hence, the state variables under consideration are predicted in each sampling time, from the affine mathematical models of the converter, derived from the respective switching states. Then, these predicted variables are compared to their reference values, and the calculated errors, bounded by soft constraints, are the optimization variables of the objective function. Once the objective function is formulated, the switching state that minimizes it, is applied to the next sampling period. Finally, a second order Luenberger observer is designed in order to estimate the load current under any kind of circumstances.

A. Control Objectives

The main control objective of the parallel dc-dc boost converter is to command the switching semiconductors so as to achieve an output voltage equal to its desired value, despite measurable changes in the input voltage and unmeasurable variations in the load. Given the input voltage $v_i(t)$, the dc component of the output $v_o(t)$ should be regulated at its reference value v_o^* with suitable choice of the control action, which means by appropriate switching. Moreover, the controller's performance in terms of current sharing is also

taken into consideration. Thus, the controller should act on the switches in such a way that the average input current is distributed equally to both legs of the converter.

B. Constrained Optimal Control

MPC is considered as a controller that has been implemented successfully in the process industry. In a few words, the procedure of the MPC is the following: An objective function is defined, based on the system's dynamics and the problem's constraints. This function is subjected to hard and/or soft constraints, depending on the configuration of the topology, and the performance of the controller that the designer wants to achieve. In a second step, the control action is obtained by minimizing this objective function at each step, over a finite prediction horizon. Such horizon recedes by one sampling interval respectively (receding horizon strategy) [17].

In the control method introduced here, the inner current control regulation problem is formulated and solved as an MPC problem. In order to penalize the deviation of the inductor currents, hysteresis bounds are introduced that are used as soft constraints. These bounds are defined by the maximum and minimum values of the reference inductor currents. In order to describe the degree of violation of the predefined constraints, which are weighted with p_{a_n} and $p_{b_n} \in \mathbb{R}^+$, a slack variable $e_n(k)$ is introduced [19].

$$e_n(k) = \begin{cases} p_{a_n} \cdot (I_{L_n}(k) - I_{L_n,\max}) & \text{if } I_{L_n}(k) \geq I_{L_n,\max} \\ p_{a_n} \cdot (I_{L_n,\min} - I_{L_n}(k)) & \text{if } I_{L_n}(k) \leq I_{L_n,\min} \\ p_{b_n} \cdot |I_{L_n}(k) - I^*_{L_n}| & \text{else} \end{cases} \tag{3}$$

where the terms $I_{L_n,max}$ and $I_{L_n,min}$ are specified as a percentage of the reference $I^*_{L_n}$.

Subsequently an objective function is formulated based on the error variable in (3). Thus, the following function is introduced

$$J(k) = \sum_{\ell=1}^{N} \Big(||e_1(k+l|k)||_1 + ||e_2(k+l|k)||_1 \Big) \tag{4}$$

which penalizes the error's evolution, $e_n(k+l|k)$, over the finite horizon N using the 1-norm (see [12]–[14]).

In order to get the optimal control input, an optimization problem is formulated, which is commonly referred to as constrained finite time optimal control (CFTOC) problem. Due to this method, the control input is achieved by minimizing the objective function (4) subjected to constraints in each sampling period

$$\begin{aligned} &u^*(k) = \arg\min J(k) \\ &\text{subject to eq. (2), and (3)} \end{aligned} \tag{5}$$

The optimal value is applied to the n-legs of the converter, and the procedure is repeated based on new measurements acquired on the following sampling instance.

As already mentioned, the outer loop sets the current reference in such a way that the output voltage is regulated to a desired value. The power balance mathematical expression is used, i.e. $P_{in} = P_{out}$, in order to manipulate the reference inductor currents, and assuming that the power switches are ideal. Furthermore, since one of the goals of the controller is the balancing of the inductor currents in each leg of the converter, the corresponding reference currents must be equal. This means that the reference inductor currents are derived from the input reference current I^*_i, and are equal to $I^*_{L_1} = I^*_{L_2} = I^*_i/2$. This results to the following expression for the reference currents

$$I^*_{L_1} = I^*_{L_2} = \frac{V_i}{R_{L_1} + R_{L_2}} - \sqrt{\Big(\frac{V_i}{R_{L_1} + R_{L_2}}\Big)^2 - \frac{V^*_o \cdot I_o}{R_{L_1} + R_{L_2}}} \tag{6}$$

C. Load Uncertainty

In the vast majority of the applications the load cannot be modeled by a simple resistor. It can be a variable resistor, or in most of the cases, a nonlinear load, such as a power converter. In order to eliminate the undesired steady state error at the output voltage caused from unknown variations in the load, an observer is employed: the load current, which is used in the calculation of the reference inductor currents, is estimated by a second order Luenberger observer [20]. By this the reduction of the hardware cost is achieved, apart from the successful decoupling of the design of the controller from the type and the value of the load.

As shown in [16] the design of a second order Luenberger observer is given by

$$\hat{x}_L(k+1) = A_L \cdot \hat{x}_L(k) + B_L \cdot \bar{u}(k) + H \cdot \bar{y}_L(k) \tag{7a}$$

$$\hat{y}_L(k) = C_L \cdot \hat{x}_L(k) \tag{7b}$$

where

$\hat{x}_L(k) = [\hat{I}_o(k) \;\; \hat{V}_o(k)]^T$, $H = [h_1 \;\; h_2]^T$, $\bar{y}_L(k) = y_L(k) - \hat{y}_L(k) = C_L \cdot \big(x_L(k) - \hat{x}_L(k)\big) = C_L \cdot \bar{x}_L(k)$, $A_L = \begin{bmatrix} 1 & 0 \\ -\frac{T_s}{C_o} & 1 \end{bmatrix}$, $B_L = \begin{bmatrix} 0 & 0 \\ \frac{T_s \cdot I_{L_1}}{C_o} & \frac{T_s \cdot I_{L_2}}{C_o} \end{bmatrix}$, $C_L = [0 \; 1]$

where $\hat{x}_L(k)$ is the estimated state. The observer gain which has to be tuned is given by the matrix $H = [h_1 \; h_2]^T$. Finally, the terms $\bar{x}_L(k)$ and $\bar{y}_L(k)$ represent the errors between the measured and the observed values of the state and the output of the system, respectively.

The error between the state variables and the observed ones at instant $(k+1) \cdot T_s$ is

$$\bar{x}_L(k+1) = (A_L - H \cdot C_L) \cdot \bar{x}_L(k) \tag{8}$$

The above error converges to zero if the observer is stable, at a rate determined by the eigenvalues of the matrix $[A_L - H \cdot C_L]$. If the pair (A_L, C_L) is observable, then the gain H exists which places the observer eigenvalues at these locations, given an arbitrary set of locations in the complex plane.

Considering the gain matrix H, the estimated variables

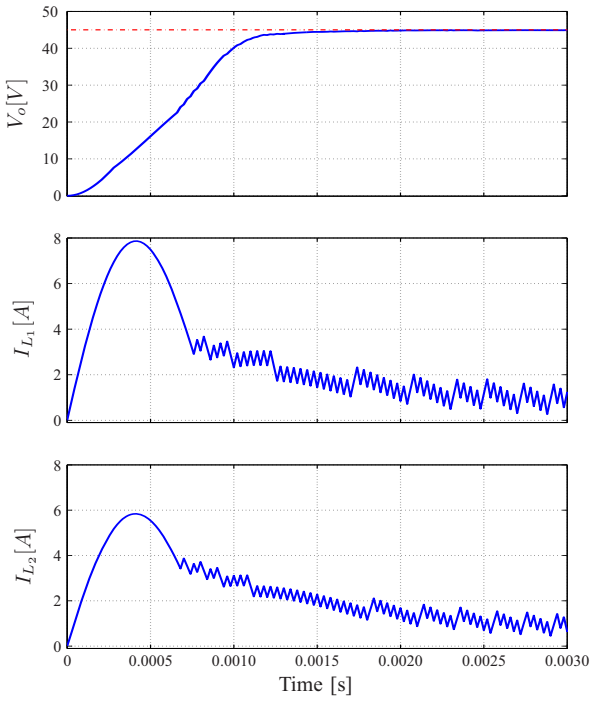


Fig. 2: Simulation results for nominal startup ($V_i = 20\,\text{V}$, $V_o^* = 45\,\text{V}$, $R = 75\,\text{Ohm}$) from initial condition zero (from top to bottom): output voltage (blue solid line) and output voltage reference (light red dashed line), current of the first inductor, current of the second inductor.

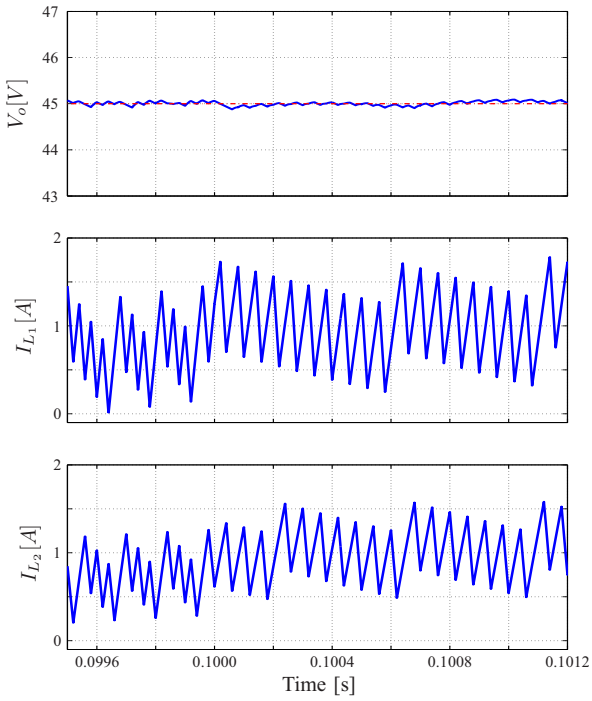


Fig. 3: Simulation results for a step-down change in the input voltage from $V_i = 20\,\text{V}$ to $V_i = 15\,\text{V}$ ($V_o^* = 45\,\text{V}$, $R = 75\,\text{Ohm}$) at time $t = 0.1\,\text{s}$ (from top to bottom): output voltage (blue solid line) and output voltage reference (light red dashed line), current of the first inductor, current of the second inductor.

$\hat{I}_o(k+1)$, $\hat{V}_o(k+1)$ are given by the following equations

$$\hat{I}_o(k+1) = \hat{I}_o(k) + h_1 \cdot (V_o(k) - \hat{V}_o(k)) \tag{9a}$$

$$\hat{V}_o(k+1) = (1-h_2)\cdot \hat{V}_o(k) - \frac{T_s}{C_o}\cdot \hat{I}_o(k) + h_2 \cdot V_o(k) + \frac{T_s}{C_o}\cdot [I_{L_1}(k)\cdot(1-u_1(k)) + I_{L_2}(k)\cdot(1-u_2(k))] \tag{9b}$$

From now on, the estimated current $\hat{I}_o$ will be used instead the actual current I_o, based on equations (9b) and (9a).

D. Inductor Currents Uncertainty

In (6), the internal resistances of the inductors are considered as constants. However, in reality the values of the resistances divert from its nominal values due to the temperature increment during the power supply's operation. Consequently, there exists an error between the calculated reference values and the actual ones [21] that cannot be regarded as trifling for small loads. A proposal to compensate the deviation in the calculation of the reference currents is to augment the state-feedback controller with a different type of external estimation loop, such as a discrete-time Kalman filter [22], which would be able to model the effect of the changing inductor resistances on the inductor currents.

IV. Simulation Results

In this section simulation results are presented in order to demonstrate the performance of the proposed controller under several operating conditions. The dynamic performance is examined for the startup. Also the response to step changes in the desired output voltage level, the input voltage and the load resistance are illustrated. Furthermore, the steady state behavior is investigated in terms of current sharing in the parallel legs of the converter. The parameters of the setup are $L_1 = 0.6\,\text{mH}$, $L_2 = 1.1\,\text{mH}$, $R_{L_1} = 0.35\,\text{Ohm}$, $R_{L_2} = 0.6\,\text{Ohm}$, $C_o = 220\,\mu\text{F}$. Initially the input voltage is $V_i = 20\,\text{V}$, the load resistance $R = 75\,\text{Ohm}$, while the reference output voltage is set equal to $V_o^* = 45\,\text{V}$. Finally, the sampling time $T_s = 20\,\mu\text{s}$.

Regarding the optimal control model, the weighting factors of the constraints are defined as $p_{a_1} = 0.5$, $p_{a_2} = 0.4$, $p_{b_1} = 0.01$, and $p_{b_2} = 0.01$. The bounds of the errors $I_{L_1,\text{max}} = 1.10\cdot I_{L_1}^*$, $I_{L_2,\text{max}} = 1.05\cdot I_{L_2}^*$, $I_{L_1,\text{min}} = 0.90\cdot I_{L_1}^*$, $I_{L_2,\text{min}} = 0.95\cdot I_{L_2}^*$. The prediction horizon is $N = 5$.

A. Startup

The first case to be examined is the startup from zero as initial condition. The converter operates under nominal conditions ($V_i = 20\,\text{V}$, $V_o^* = 45\,\text{V}$, $R = 75\,\text{Ohm}$). As can be seen in Fig. 2, the inductor currents are increased until the capacitor is charged to the desired voltage level. The output voltage reaches its reference value in about 1.8 ms, while no overshoots are observed. Once the transient phenomenon has occurred, the inductor currents reach their nominal values; the output voltage remains constant to the desired level.

B. Input Voltage Step Change

During the previously attained steady-state point of operation, at time $t = 0.1\,\text{s}$, a step change to the input voltage

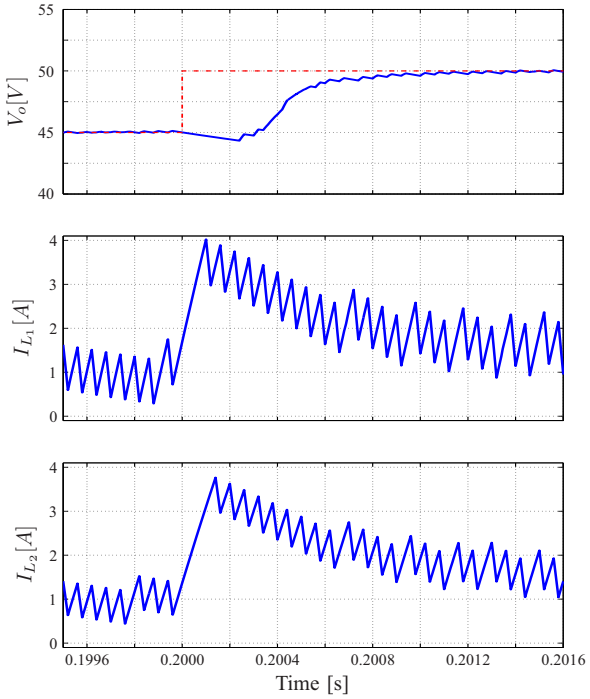


Fig. 4: Simulation results for a step-up change in the output voltage reference from $V_o^* = 45\,\text{V}$ to $V_o^* = 50\,\text{V}$ ($V_i = 15\,\text{V}$, $R = 75\,\text{Ohm}$) at time $t = 0.2\,\text{s}$ (from top to bottom): output voltage (blue solid line) and output voltage reference (light red dashed line), current of the first inductor, current of the second inductor.

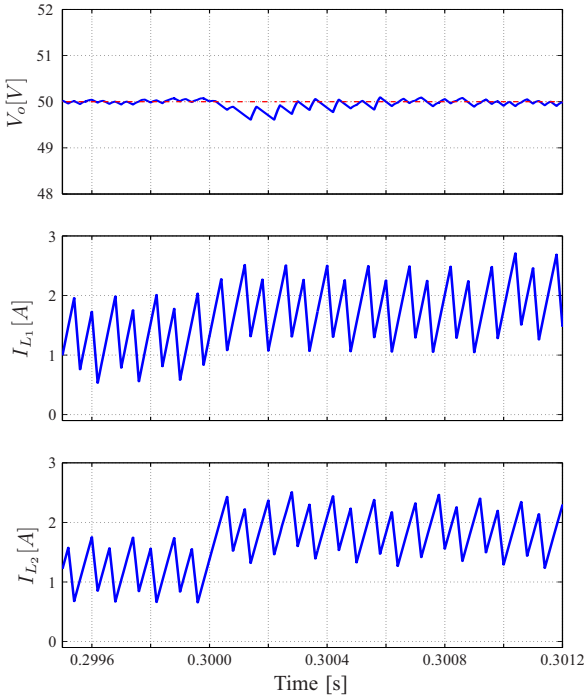


Fig. 5: Simulation results for a step-down change in the load resistance from $R = 75\,\text{Ohm}$ to $R = 50\,\text{Ohm}$ ($V_i = 15\,\text{V}$, $V_o^* = 50\,\text{V}$) at time $t = 0.3\,\text{s}$ (from top to bottom): output voltage (blue solid line) and output voltage reference (light red dashed line), current of the first inductor, current of the second inductor.

is applied, from $V_i = 20\,\text{V}$ to $V_i = 15\,\text{V}$. The response of the converter is depicted in Fig. 3. The output voltage remains practically unaffected, while the controller settles very quickly at the new steady state operating point.

C. Output Reference Voltage Step Change

The performance of the controller is further tested in the presence of a step variation in the output reference voltage. In this case a step-up change of the output reference voltage is considered, at time $t = 0.2\,\text{s}$, from $V_o^* = 45\,\text{V}$ to $V_o^* = 50\,\text{V}$. Again, the currents are increased until the capacitor is charged to the new reference voltage level. The controller exhibits satisfactory transient behavior, since it reaches the new output voltage in about 1.4 ms, with no overshoots. The segment of interest in this test is illustrated in Fig. 4.

D. Load Resistance Step Change

The last case examined is that of a step change in the load resistance occurring at $t = 0.3\,\text{s}$. Starting from the nominal load $R = 75\,\text{Ohm}$, a step-down change to $R = 50\,\text{Ohm}$ is applied. As shown in Fig. 5, the controller manages to adjust to the non-nominal operating conditions, while the system reaches the desired operating point quickly (in about 0.4 ms). The output voltage remains close to its reference value irrespective to the load step.

E. Current Balancing

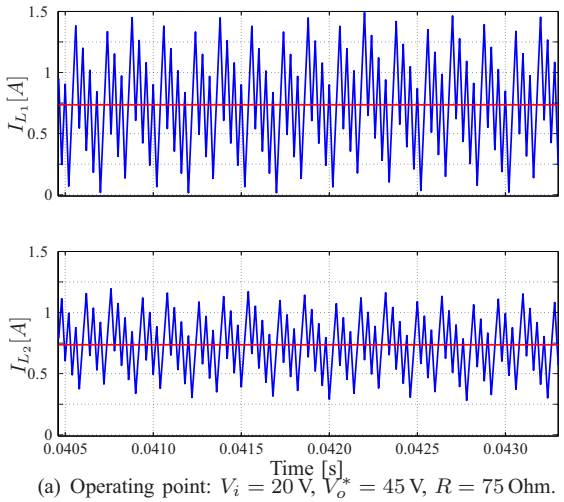
Since one of the control objectives of the controller is the equal current distribution to the individual converter's legs, the steady-state performance is examined. In order to validate the current balancing, the average inductor currents should be calculated. However, the converter operates under variable switching frequency, which means that the integration of the current in one sampling period, T_s, is not accurate. Thus, if the currents are integrated over a large time "window", then we can claim that the outcome of the calculation is precise. The average currents are given by

$$I_{L_n,dc}(t) = \frac{\int_0^{T_{sw}} I_{L_n}(t)dt}{T_{sw}} \tag{10}$$

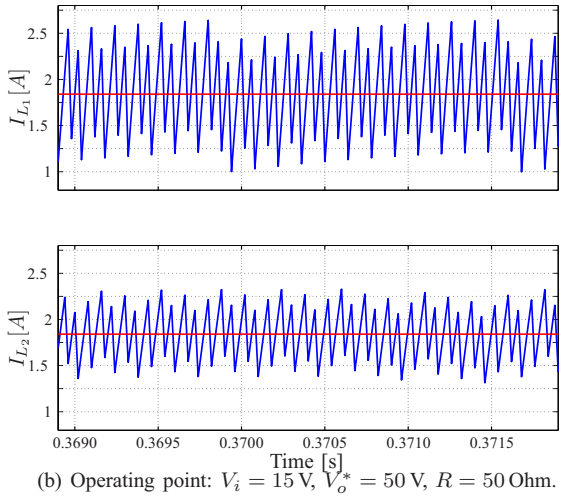
where $I_{L_n,dc}$ is the average current of the n individual inductor, I_{L_n} is the respective actual current, and T_{sw} is the time "window" with $T_{sw} >> T_s$. Fig. 6 shows the current balancing under steady-state operation of the converter for two different operating points. Fig. 6(a) corresponds to the operating point where $V_i = 20\,\text{V}$, $V_o^* = 45\,\text{V}$, and $R = 75\,\text{Ohm}$, while Fig. 6(b) to the operating point where $V_i = 15\,\text{V}$, $V_o^* = 50\,\text{V}$, and $R = 50\,\text{Ohm}$.

V. Conclusion

In this paper, the MPC approach, which was recently introduced for the dc-dc boost converter, is extended to the dc-dc parallel interleaved boost topology that features two individual legs. The proposed control scheme leads to favorable dynamical and robustness properties, in particular during startup and transients. Furthermore, since the con-



(a) Operating point: $V_i = 20\,\text{V}$, $V_o^* = 45\,\text{V}$, $R = 75\,\text{Ohm}$.



(b) Operating point: $V_i = 15\,\text{V}$, $V_o^* = 50\,\text{V}$, $R = 50\,\text{Ohm}$.

Fig. 6: Simulation results for the average and actual inductor currents for two different operating points (from top to bottom for both (a) and (b)): current of the first inductor (blue line) and corresponding average current (red line), current of the second inductor (blue line) and corresponding average current (red line).

troller achieves equal current distribution to the converter legs benefits are derived in terms of cost and reliability. These advantages overshadow the inherent drawbacks of the method, such as the computational complexity and the variable switching frequency. Its straightforward implementation allows the scheme to be easily extended to the interleaved topology with more legs. Simulation results validate the high performance of the proposed method both in steady-state and in dynamic operating conditions.

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