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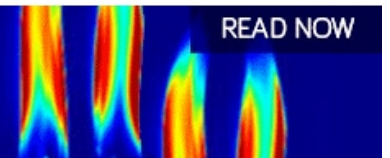
# Effects of growth temperature on electrical properties of GaN/AlN based resonant tunneling diodes with peak current density up to 1.01 MA/cm²

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Evan M. Cornuelle,[1] [iD] Tyler A. Growden,[2] [iD] David F. Storm,[3,a] [iD] Elliott R. Brown,[4] Weidong Zhang,[4] Brian P. Downey,[3] Vikrant Gokhale,[2] Laura B. Ruppalt,[3] James G. Champlain,[3] Prudhvi Peri,[5] [iD] Martha R. McCartney,[5] David J. Smith,[5] David J. Meyer,[3] and Paul R. Berger[1] [iD]

## AFFILIATIONS

[1] Department of Electrical and Computer Engineering, The Ohio State University, Columbus, Ohio 43210, USA

[2] NAS-NRC Postdoctoral Research Fellow Residing at the U.S. Naval Research Laboratory, Washington, District of Columbia 20375, USA

[3] U.S. Naval Research Laboratory, Washington, District of Columbia 20375, USA

[4] Departments of Physics and Electrical Engineering, Wright State University, Dayton, Ohio 45435, USA

[5] Department of Physics, Arizona State University, Tempe, Arizona 85287, USA

[a] Author to whom correspondence should be addressed: david.storm@nrl.navy.mil

## ABSTRACT

Identical GaN/AlN resonant tunneling diode structures were grown on free-standing bulk GaN at substrate temperatures of 760 °C, 810 °C, 860 °C, and 900 °C via plasma-assisted molecular beam epitaxy. Each sample displayed negative differential resistance (NDR) at room temperature. The figures-of-merit quantified were peak-to-valley current ratio (PVCR), yield of the device with room-temperature NDR, and peak current density ($J_p$). The figures-of-merit demonstrate an inverse relationship between PVCR/yield and $J_p$ over this growth temperature series. X-ray diffraction and transmission electron microscopy were used to determine the growth rates, and layer thicknesses were used to explain the varying figures-of-merit. Due to the high yield of devices grown at 760 °C and 810 °C, the PVCR, peak voltage ($V_p$), and $J_p$ were plotted vs device area, which demonstrated high uniformity and application tunability. Peak current densities of up to 1.01 MA/cm² were observed for the sample grown at 900 °C.

Over the past decade, there has been a considerable effort to produce high-performance GaN-based resonant tunneling diodes (RTDs), fueled by the strong demand for affordable, compact, high power millimeter-wave (mm-wave) and terahertz (THz) devices. Applications for such devices are found in spectroscopy, imaging, security, medicine, high-resolution sensing, and broadband communications. RTDs are promising candidates to fill these needs since they are based on ultra-fast electron transportation by means of quantum mechanical tunneling. Quantum tunneling occurs with an increased probability when the electron injection energy level aligns with the discrete energy level in the well and the opposite occurs when the two energy levels misalign. Negative differential resistance (NDR) results from the alignment and subsequent misalignment of the injection and quantum well energy levels under increasing bias, and it is the hallmark of quantum tunneling in these devices. Fundamental oscillations of 712 GHz[1] and 1.92 THz[2] at room temperature have already been reported in InAs/AlSb and InGaAs/AlAs RTD devices, but these lacked significant output power. Recently, using

on-chip biasing and power combining, 1 mW of output power at 260 GHz from an InGaAs-based RTD has been achieved.[3] III-nitride-based RTDs have an inherent potential to achieve higher output power due to their considerably wider bandgap energies. Unfortunately, while great progress has been made,[4–19] GaN-based RTDs are not yet well enough understood to produce devices capable of reaching oscillation frequencies above 1 GHz.[16]

The output power of an RTD-based oscillator can be estimated by $\frac{3}{16}\Delta I \Delta V$, where $\Delta I$ and $\Delta V$ are the differences between the peak and valley currents and voltages, respectively, of the NDR region.[21] Recently, there have been reports of peak tunneling current densities in GaN-based RTDs ranging from 100 kA/cm² up to 930 kA/cm².[11,15,16,18,19] However, their respective peak-to-valley current ratios (PVCRs) are low, which translates to small $\Delta I$. Another recent study has reported a PVCR above 2 in a GaN/AlN RTD, but the current density was relatively low at 30 kA/cm².[22] However, that paper and a previous paper[23] reported 10%–90% switching rise times of 33 ps and 55 ps, respectively, which correspond to fundamental oscillation frequencies in tens of the GHz range. In order to reach frequencies in the THz range, GaN-based RTDs must be fundamentally better understood. In this paper, we report experimental measurements for a series of GaN/AlN RTD devices to determine the effect of growth temperature and device area on electrical characteristics. Statistical analysis of temperature and area dependence on RTD figures-of-merit (i.e., PVCR, peak current density, yield, etc.) was enabled by the high yield and uniformity between samples and devices.

The double-barrier RTD structure illustrated in Fig. 1(a) was grown by plasma-assisted molecular beam epitaxy (PAMBE) in an Omicron/Scienta PRO-75 MBE system equipped with a Veeco® Uni-Bulb™ rf-plasma source for active nitrogen, dual-filament effusion cells for evaporation of elemental Ga and Al, a medium–high temperature effusion cell for the Si dopant source, and *in situ* reflection-high-energy electron diffraction (RHEED). The substrate temperature was monitored by a thermocouple positioned behind the molybdenum wafer mount. All samples were grown on 18 × 18 mm² squares diced from a single 50 mm-diameter freestanding GaN wafer obtained commercially. The freestanding, Fe-doped GaN wafer was semi-insulating, with a nominal resistivity in excess of 1 MΩ-cm, a threading dislocation density (δ) of 3 × 10⁶ cm⁻², and

a thickness of 350 ± 25 $\mu$m. The Ga-polar (0001) c-plane, offcut 0.35° ± 0.15° toward the m-plane, was used for growth. The surfaces were prepared with an aggressive *ex situ* HF, HCl, and solvent-based wet chemical clean described in detail elsewhere,[24,25] immediately prior to loading. Each substrate was degassed under ultra-high vacuum (UHV) conditions for 30 min at 600 °C before being transferred to the deposition chamber.

Once transferred to the deposition chamber, the substrate was ramped to the growth temperature over 20 min. Four samples were grown at substrate temperatures of 760 °C, 810 °C, 860 °C, and 900 °C, respectively. 2 × 1 RHEED patterns were observed from the GaN substrate surfaces at 760 °C, 810 °C, and 860 °C, but not at 900 °C, where only a streaky 1 × 1 pattern was observed. The samples are referred to as Sample A, B, C, and D, respectively. Growth was initiated by first exposing the substrate surface to the nitrogen plasma for 2 min, during which the 2 × 1 reconstructed RHEED pattern faded, and the Ga and Si shutters were then opened. The nitrogen plasma was operated at a constant power and flow of 275 W and 0.80 sccm, respectively, resulting in an N-limited growth rate of ~3 nm/min. The ratio of the Ga and active N fluxes was estimated to be ~1.3:1. Each sample was grown continuously, without any interruption, including the four GaN/AlN heterointerfaces.

Sample A exhibited Ga droplets across the entire sample; the fraction of the surface area covered by droplets was estimated to be 4%. Droplets were observed in a small, isolated region of Sample B and not at all on Sample C or D. We have separately observed rapid Ga desorption from GaN surfaces at substrate temperatures near 900 °C.[26] The as-grown samples were characterized by atomic force microscopy (AFM) and x-ray diffraction (XRD). The Ga droplets were removed by etching for 3–5 min in HCl. Portions of each sample were cleaved and removed prior to device fabrication for observation by transmission electron microscopy (TEM).

XRD over 3° (ω-2θ) centered on the GaN [0002] peak was performed on each sample and subsequently fitted using the dynamical simulation software "MadMax."[28] XRD experimental data and fit for Sample B are shown in Fig. 1(b). The Pendellösung fringes visible here were present on each sample and allowed for accurate extraction of the GaN growth rate: 3.06–3.14 nm/min. Quantum well and barrier thicknesses were determined from the dynamical simulations of the XRD data, as shown in Table I, given the assumption that AlN
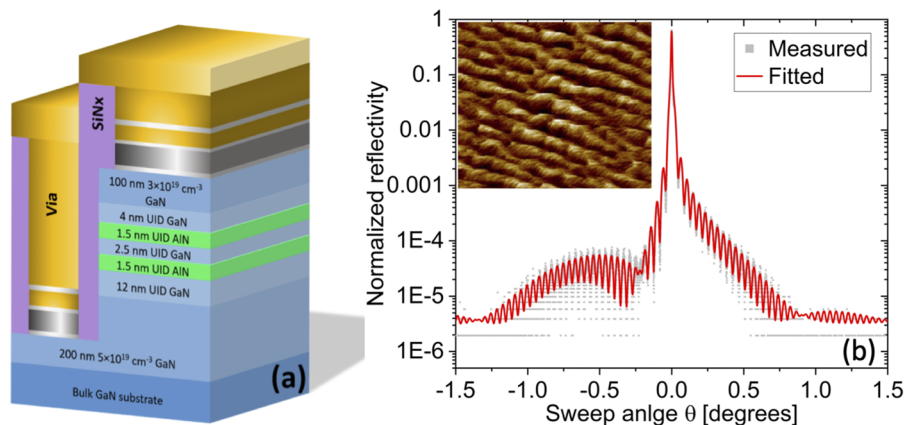


FIG. 1. (a) Device layer stack and (b) XRD and (inset) the 5 × 5 $\mu$m² AFM scan region for Sample B with an rms surface roughness of 0.340 nm.

**TABLE I**. The table indicates the sample ID, substrate temperature measured by the thermocouple, and rms surface roughness by AFM. Also displayed are XRD best–fit parameters and TEM image analysis values for AlN barriers and the GaN quantum well region.

| Sample ID | $T_s$ (°C) | AFM: $R_q$ (nm) | FWHM GaN (0002) (arc-sec) | XRD $t_{AlN}$ (nm) | XRD $t_{GaN}$ (nm) | TEM $t_{AlN}$ (nm) | TEM $t_{GaN}$ (nm) |
|---|---|---|---|---|---|---|---|
| A | 760 | 0.58 ± 0.08 | 40.3 | 1.64 | 2.73 | 1.64 | 2.68 |
| B | 810 | 0.37 ± 0.01 | 28.1 | 1.55 | 2.55 | 1.71 | 2.22 |
| C | 860 | 3.1 ± 0.9 | 30.6 | 1.60 | 2.68 | 1.55 | 2.45 |
| D | 900 | 3.6 ± 0.4 | 32.0 | 1.59 | 2.64 | N/A | N/A |

grows at the same rate as GaN. Results for barrier and well regions should not be taken as exact, but they do provide confidence that the layers were grown within the target thickness range (±1 monolayer).

Surface morphology for each sample was measured by atomic force microscopy (AFM), with the inlaid image in Fig. 1(b) being from Sample B. Measurements were taken over $5 \times 5$ $\mu m^2$ fields of view at three locations along a diagonal for each sample; rms roughness values are presented in Table I. The smoothest surfaces were observed for Samples A and B grown at 760 °C and 810 °C, respectively; higher growth temperatures resulted in rougher surfaces. Large-angle bright-field scanning TEM was performed on Samples A, B, and C, as shown in Figs. 2(a)–2(c). Image analysis to accurately determine the barrier and quantum well thicknesses for each sample was performed using ImageJ[27] software. The results are also shown in Table I. The XRD and TEM data for barrier and quantum well thicknesses were within one monolayer (~0.25 nm) of each other. The variations in the barrier thicknesses extracted from the TEM images correlate with the current densities measured for each growth temperature, as illustrated in Fig. 3(c).

Samples A, B and C were co-fabricated into devices, and Sample D was completed later in a lab with different equipment, which should not have affected measured device performance since the fabrication steps for all samples were equivalent. Device fabrication was performed using standard optical lithography and metal liftoff techniques. Mesa definition was performed with a $Cl_2/BCl_3/Ar$ inductively coupled plasma reactive-ion etch (ICP RIE), producing device areas between 12 $\mu m^2$ and 96 $\mu m^2$ for Samples A, B, and

C and between 1.5 $\mu m^2$ and 48 $\mu m^2$ for Sample D. Ti/Al/Ti/Au [25/100/30/50 nm] ohmic contacts were first deposited and annealed using a two-step rapid thermal annealing process. The samples were first annealed at 400 °C for 180 s and then at 700 °C for 18 s, both in a $N_2$ ambient atmosphere, to improve ohmic contact resistance. The circular transmission line method was used for measuring contact resistivity and contact resistance with mean values of 5.8 $\times 10^{-6}$ $\Omega$-cm$^2$ and 0.217 $\Omega$, respectively. Device side-wall passivation was then implemented with 250 nm SiN$_x$ deposited by plasma-enhanced chemical vapor deposition. Ti/Au ground–signal–ground (GSG) contact pads were deposited by e-beam evaporation through vias in the passivation layer. A detailed description of the device fabrication can be found in previous reports.[13,22]

Representative current–voltage (I–V) curves for each size device across all samples are shown in Fig. 3. The dc I–V measurements were performed by sweeping the applied voltage from −4 V to around +6 V depending on the location of the NDR region. All four samples showed room-temperature NDR. Sample D showed room-temperature NDR on devices up to 20 $\mu m^2$, but then, the differential resistance starting near the expected peak voltage increased and was no longer negative (later referred to as "inflection points"). Samples A and B exhibited room-temperature NDR on devices of all sizes between 12 $\mu m^2$ and 96 $\mu m^2$, albeit with much lower current densities. Samples C and D showed considerably larger currents than Samples A and B. Inflections in the I–V separate from the main NDR region are present in Samples A and B between 2 V and 3 V but are absent in Samples C and D, as shown in Figs. 3(a)–3(d). These
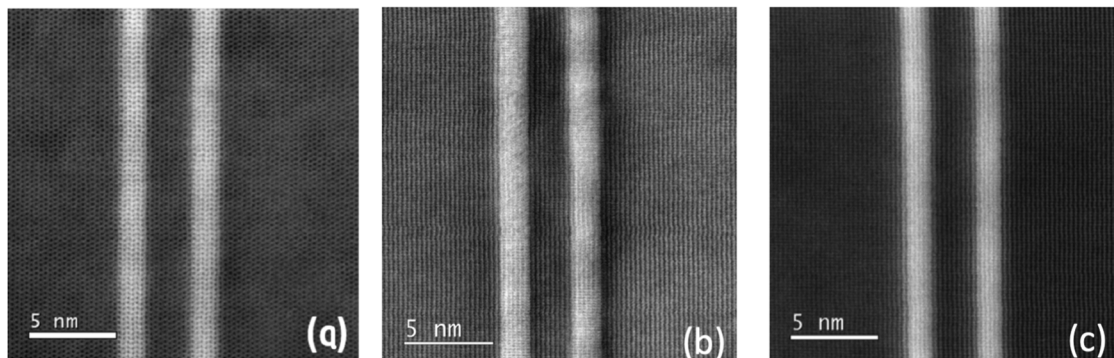


**FIG. 2**. Large-angle bright-field scanning TEM images for (a) Sample A, (b) Sample B, and (c) Sample C.
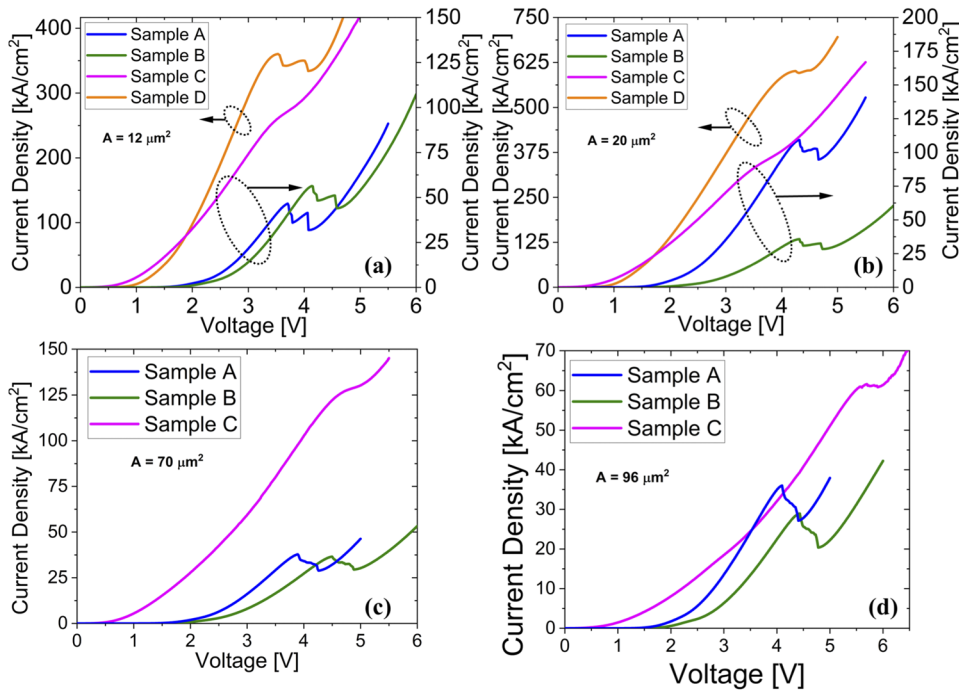
**FIG. 3**. Typical current–voltage characteristics for devices of a certain size for increasing growth temperature: (a) 12 $\mu m^2$ devices, (b) 20 $\mu m^2$ devices, (c) 70 $\mu m^2$ devices on all samples excluding Sample D, and (d) 96 $\mu m^2$ devices on all samples excluding Sample D.

inflection points suggest resonant tunneling through lower quantum well energy levels with a smaller current density. Another possibility is that there are multiple injection mechanisms, as has been previously reported.[22] Samples C and D failed to show this behavior likely because the current is dominated by current mechanisms other than resonant tunneling.

Several figures-of-merit were used to characterize the quality of the RTD, namely, peak current density ($J_p$), yield, peak-to-valley current ratio (PVCR), and peak voltage ($V_p$). The first three of these are displayed in Fig. 4 as a function of substrate growth temperature. The averages and standard deviations for $J_p$ and the PVCR were calculated by measuring all working devices on each sample, where a working device was defined as having room-temperature NDR.

Increased growth temperature came at some cost, namely, the yield of working devices decreased rapidly from a maximum of ~80% for Sample B down to ~2% for Samples C and D, as shown in Fig. 4(b). Average PVCR values followed the same trend as yield, peaking at a value of ~1.26 for 810 °C (Sample B), as illustrated in Fig. 4(a). An interesting feature of these figures-of-merit was the identical trend shared between the PVCR and yield. In general, a large yield is the result of two factors: (1) high growth and fabrication *quality* and (2) *uniformity* of the material across the sample. In contrast, the PVCR is usually an indication of design, growth, and fabrication *quality* but does not require material *uniformity* across the sample. That PVCR and yield follow the same trend is attributed to the fact that they both depend primarily on *quality*, namely, the growth. The
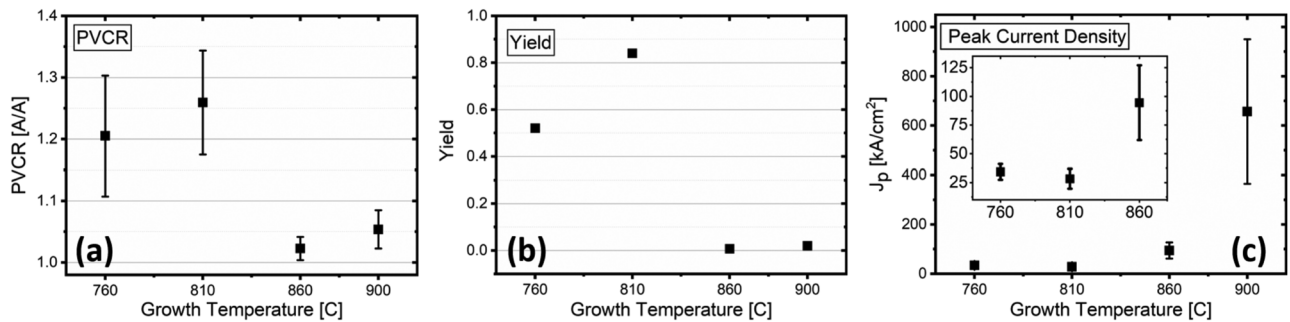


**FIG. 4**. Resonant tunneling diode figures-of-merit as a function of substrate growth temperature: (a) peak-to-valley current ratio, (b) yield of working devices, and (c) peak current density.
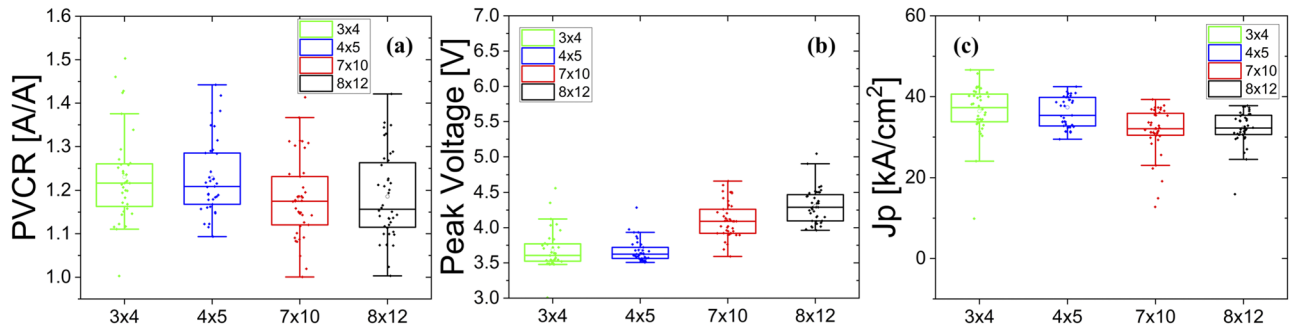
**FIG. 5**. Figures-of-merit for sample A vs device area ($\mu m^2$): (a) PVCR, (b) peak voltage, and (c) current density at peak voltage.

physical mechanisms that determine quality are interface roughness, dislocations, or the presence of any scattering centers that will broaden the electron wavefunction creating non-resonant tunneling electron transportation.

When the growth temperature was increased from 760 °C to 900 °C, $J_p$ increased by an order of magnitude, consistent with the fact that the resonant-tunneling component in an RTD is extremely sensitive to barrier thickness, and also to well thickness to a lesser extent. For the thin barriers (nominally 1.5 nm) used here, reduction in thickness by one monolayer can increase the current density by roughly an order of magnitude.[20] While the large-angle bright-field TEM images illustrated in Figs. 2(a)–2(c) are supportive of this hypothesis, these represent only a snapshot of a small part of the entire device. To verify this would require an exhaustive TEM study that examines a considerable portion of wafers capable of operational devices.

The large number of working devices fabricated for Samples A and B, namely, 231 and 293, respectively, allows for statistical investigation. Each figure-of-merit as a function of growth temperature can be plotted as a function of the device area, as illustrated in Figs. 5 and 6, respectively. Generally, the variance for each distribution describing Sample A is larger than the equivalent distribution in Sample B because of the higher yield for sample B. Variance reduction is proportional to the sample size. Device performance is affected by area in multiple facets. PVCR, peak

voltage, and current density all trend toward lower device performance with an increase in device area, as evident in Figs. 5 and 6. The PVCR decreased with area due to self-heating effects: larger absolute current increases device temperature via Joule heating, subsequently increasing carrier scattering events that contribute to the valley current.[19] Further confirmation stems from the comparison between the PVCR for these two samples and their current densities. The average current density for each size device of Sample A is larger than the equivalent size device of Sample B [Figs. 5(c) and 6(c)], while having an inverse relationship for the PVCR [Figs. 5(a) and 6(a)].

Peak voltage increased with the device area and was a result of fixed external series resistance (~1.5 Ω) in the test network affecting the measured extrinsic voltage when absolute current increased. For the two smallest area devices, the peak voltage distribution is skewed toward larger values and appears to reach a minimum value of ~3.5 V. Although there are slight general trends in these metrics, it is important to note the relative uniformity of the devices. Accompanied by a large number of working devices, it is reasonable to conclude that these devices are of high quality and repeatable. The device space spanned by growth temperature and device size allows for a tuned device based on the specific application. For example, an RTD-based logic circuit requires a large PVCR. A small area device (<12 $\mu m^2$) grown close to 810 °C is suggested to achieve this requirement.
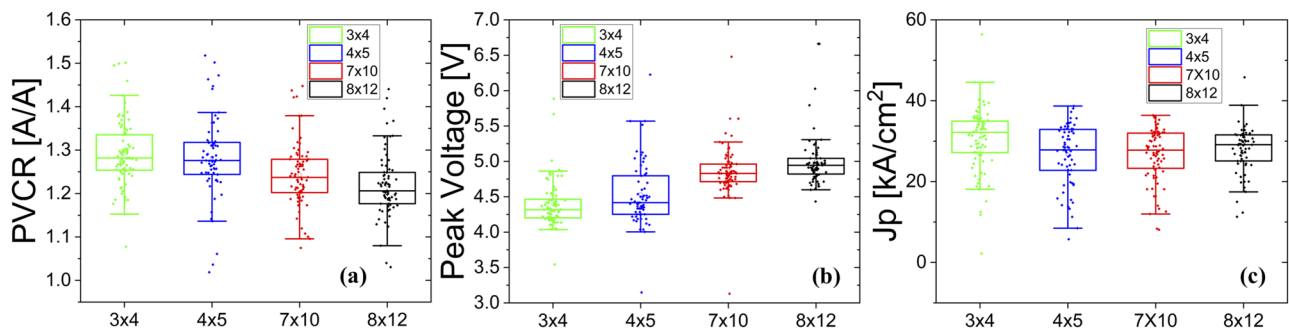


**FIG. 6**. Figures-of-merit for sample B vs device area ($\mu m^2$). (a) PVCR, (b) peak voltage, and (c) current density at peak voltage.
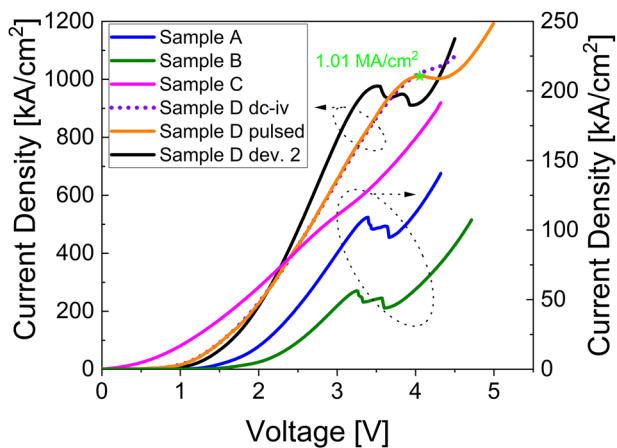
**FIG. 7**. J–V curves for devices with the largest current density on their respective sample.

The previous highest peak current density of 930 kA/cm$^2$ was nominally measured on the same device structure, changing only the substrate to free-standing bulk GaN.[19] Reported here is the first GaN-based RTD exhibiting greater than 1 MA/cm$^2$ peak current density. Sample D was the source of the device. A I–V dc measurement of the device displayed in Fig. 7 shows the lack of room-temperature NDR. It is suspected that the valley current grows via LO phonon-assisted tunneling due to self-heating from resistive effects as the device area increases and eventually masks the NDR.[19] Sample D was affected more than the other samples due to larger absolute current and current density. To reduce the thermal energy increase under steady bias, pulsed measurements were recorded using an Accent DiVA pulsed I–V meter with pulse widths of 200 ns and a duty cycle of $4 \times 10^{-3}$%, which is in contrast to the previous report of 930 kA/cm$^2$ measured at 100% duty cycle. Raw pulsed data from the meter was smoothed using a Savitzky–Golay filter, with the result overlaid in Fig. 7 showing room-temperature NDR. Devices with the largest peak current density on each of the other samples are compared with each other and overlaid in Fig. 7. Sample D produced other devices with comparable current density. One such device is shown in Fig. 7 (black curve) displaying a 100%-duty dc J–V peak current density of 976 kA/cm$^2$.

In summary, trends in figures-of-merit for GaN/AlN RTDs as a function of growth temperature and device area have been observed, leading to record high current densities of >1 MA/cm$^2$. This substrate temperature growth study allowed for statistical analysis of the PVCR, yield, and peak current density, which indicated that current density generally increased with growth temperature at the cost of decreased yield and PVCR. Samples A and B exhibited the highest yield, which allowed for statistical analysis as a function of device area for the PVCR, peak voltage, and peak current density. Generally, an increase in device area reduced the device quality in all four metrics. These findings produce a 2-dimensional "phase-space" between growth temperature and device area that allow for application-specific RTD production and add to the viability for high power applications that require large current density.

## DATA AVAILABILITY

The data that support the findings of this study are available within the article.

Distribution Statement "A" (Approved for Public Release. Distribution Unlimited).

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