Statistical Lifetime Analysis in Memristive Crossbar

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***Abstract*—Emerging devices for future memory technologies have attracted great attention recently. Memristors are one of the most favorable such devices, due to their high scalability and compatibility with CMOS fabrication process. Alongside their benefits they also face reliability concerns. In this sense our work analyzes some sources of uncertainties in the operation of the memristive memory and next proposes an approach to determine the expected lifetime of a memristive crossbar.**

***Index Terms*—Memristor; uncertainty; crossbar; endurance; process variability; RRAM; emerging device**

I. Introduction

Memristors are one of the new emerging devices that receive significant attention as a promising candidate for future nano-scale memory technologies [1]. They can scale down to few nanometers, and also have high switching speed, long retention time, low programming power and non-volatile characteristics [2]. Memristor theory has been under research since many years ago [3], however it has not been until recently that the first physical devices were manufactured successfully [4]. Their device structure is an oxide sandwiched between two electrodes that can switch between two resistance states, a high resistance state (HRS) and a low resistance state (LRS), therefore it can store the data in the state of the resistance value.

Memristors can be differentiated to various types based on their switching mechanism and constructing materials. In this paper we focus on one of the most frequent memristor types, the binary metal oxide resistive switching random access memory (RRAM). The main theory that describes the switching mechanism in this memristor type is based on conductive filamentary (CF) switching [5].

Generally, memristors are organized in a matrix-like structure called crossbar architecture to construct a memory system. The storage cell in the crossbar can be built with only a single memristor (1R) or with one selector such as one transistor and one mermistor (1T1R). Independently from the architecture and the cell structure the desired memory performance depends on the reliable operation of the memristor, however manufacturing at nano-scale sizes makes them susceptible to various kinds of reliability concerns. Two of the most important sources of uncertainty in the design of memristive memories are process variability and endurance. The first causes variation in the nominal high and low resistance value, while the former is a dynamic variation to the resistance values due to aging at each cycle and limits the write cycles. Therefore in this study we analyze the impact of these reliability concerns in the normal operation of memory, and evaluate the read instability due to variability and endurance. Moreover, in this work we propose a novel statistical approach to predict the lifetime of a memristive crossbar.

II. Uncertainty in Memristors

A. Process Variability

Statistical variation in the high and low resistance values of the memristor is a major barrier in reliable operation of the device. There are two types of resistance fluctuation in memristive devices: device-to-device and cycle-to-cycle variability [2], where in this work we consider the first. Manufacturing the memristors at nano-scale sizes, and consequently existing uncertainties in their area, oxide thickness and doping concentration of oxygen vacancies are the origins of the poor device-to-device uniformity. Moreover, the random electroforming process applied to fresh devices can impose different-size initial conductive filament inside the memristor, also resulting to deviations in high and low resistance values. To model all these sources of variability in memristive devices, we consider two normal distributions for the HRS and LRS values [6] with a defined mean and standard deviation value (Fig. 2.a).

B. Endurance

The second critical reliability concern in memristors, which we study, is the endurance degradation. This mechanism reduces the distance window between HRS and LRS values and causes additional variations from the nominal expected values (Fig. 1). Generally endurance depends on different operation factors such as the environment temperature, device switching speed and also the material. In this sense, three types of endurance failure behavior are reported in RRAM devices [7]. In the first mechanism the HRS resistance tends to decrease while the LRS resistance increases during cycles. Fig.1 depicts this degradation mechanism and presents the final failure state of the device as the point that the HRS to LRS resistances ratio decreases below a ratio (K). The second and third endurance mechanisms are due to the abrupt or gradual drop of HRS value during the cycles and getting stuck at LRS value [7].

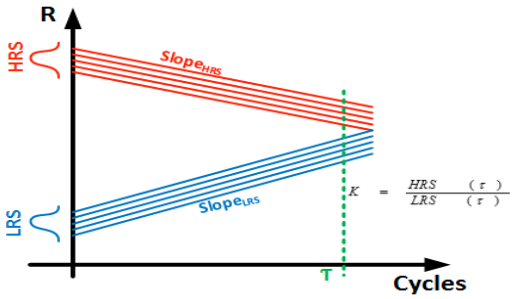


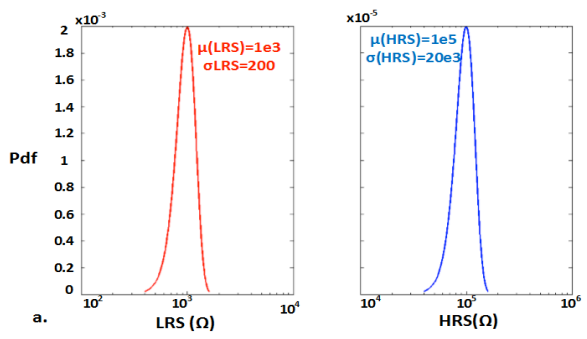
Fig. 1. The LRS and HRS degradation during the write cycles

In this work we focus on the first mechanism as the worst case and analyze its impact in reliability of a memristive crossbar memory.

III. Uncertainty Impact in Memristor Read Cycle

There are different approaches to read the memristance value in a crossbar memory [8]. The main technique is based on the comparison of the selected memristive cell´s current (or voltage) in the crossbar with a reference one [8]. The resistance variations discussed previously can reduce the sense window or even enforce a fault in the read process (for instance sensing LRS instead of HRS or vice versa). To investigate the reliability of the read process in the memristive crossbar we analyze the probability of the error in Matlab while performing the reading operation. Our LRS and HRS resistance values are defined by normal distribution ($\mu LRS=1K\Omega$, $\mu(HRS)=100K\Omega$ and $\sigma(LRS)=\sigma(HRS)=20\%$ as the variability factor, corresponding to their mean and standard deviation values).

Fig. 2.a shows the two truncated LRS and HRS probability distributions of fresh devices between -3σ to $+3\sigma$. Endurance can impose the μ(HRS) and μ(LRS) values to get closer to each other. Regarding to this, Fig. 2.b analyzes the probability of the reading error (*Pe*), as a factor that determines the possibility of an incorrect read operation in respect to a reference resistance value (R_{ref}). The *Pe* graph is plotted while sweeping the reference resistance value (in which below R_{ref} is expected to be in LRS state and higher than R_{ref} the HRS state) along the two LRS and HRS distribution. Each *Pe* graph corresponds to a specific ratio of μ(HRS) and μ(LRS) values and determines the probability of error while performing the read operation in memristive cells. Fig 2.b signifies the importance of considering the simultaneous impact of variability and endurance for robust and reliable memristive memory design.



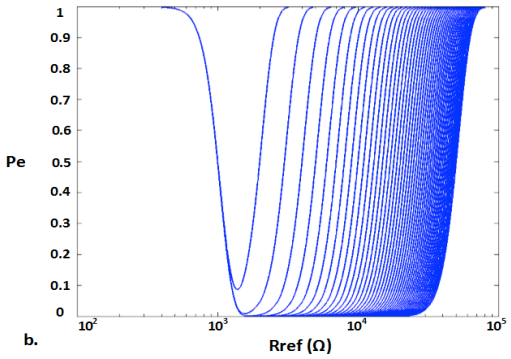


Fig. 2. a)The LRS and HRS probability distributions b)Pe in respect to different values for Rref

IV. Crossbar Lifetime Analysis

In order to estimate the probability distribution of a memristive crossbar lifetime, we first find the probability distribution of a single memristor lifetime, starting from cycle zero. We can estimate the lifetime of a memristor (τ, a random variable) by assuming a linear approximation for the degradation slopes of LRS and HRS. The values for these slopes, as well as *HRS(0)* and *LRS(0)* (which are the resistance values at cycle zero) are all obtained from experimental measurements (Fig. 5 [7]). Then by defining the point of failure for a memristor as the point where the $HRS(\tau)/LRS(\tau)$ ratio becomes equal to K (shown in Fig. 1), we find the point of failure as in (1):

$$K = \frac{HRS(0) - SlopeHRS \times \tau}{LRS(0) + SlopeLRS \times \tau} \qquad (1)$$

Solving (1) would result in obtaining the memristor lifetime (τ), expressed in terms of the number of cycles in (2).

$$\tau = \alpha \times HRS(0) - \beta \times LRS(0) \qquad (2)$$

Where α and β are the coefficients that depend only on the degradation of slopes ($slope_{HRS}$ and $slope_{LRS}$) and the K parameter. Next, from the principle of sum of normal distributions, the mean and variance values for the τ are calculated as in (3) and (4):

$$\mu(\tau) = \alpha \times \mu(HRS(0)) - \beta \times \mu(LRS(0)) \qquad (3)$$

$$\sigma^2(\tau) = \alpha \times \sigma^2(HRS(0)) + \beta \times \sigma^2(LRS(0)) \qquad (4)$$

So, under the previous assumptions (μ and σ of HRS and LRS, same as section III and assuming K=5), the lifetime of a fresh memristor follows a normal distribution in Fig. 3.a.

Regarding this information, in the next step we analytically obtain the probability distribution of the number of cycles up to the first failure in a crossbar with n memristors (n=16 in this example). In other words, we will find the probability distribution of number of cycles for the memristor (i) of the crossbar, which first reaches the critical ratio of K. This can be calculated as the probability distribution of the minimum of independent random variables (τ_i). Assuming a set of τ_i values from a normal distribution, where $1 \le i \le n$, we are intended to calculate the probability density function (*PDF*) of a random

variable named g, where $g=Min\ (\tau_1, \tau_2, \ldots, \tau_n)$. The *CDF* of g is found as in (5):

$$CDF(g) = 1-(1-CDF(\tau))^n \qquad (5)$$

From (5) we calculate the *PDF(g)* as in (6) and (7):

$$PDF(g) = \frac{\partial CDF(g)}{\partial \tau} \qquad (6)$$

$$PDF(g) = n\times(1-\int_{-\infty}^{\tau}\frac{1}{\sigma\sqrt{2\pi}}e^{\frac{-(z-\mu)^2}{2\sigma^2}}dz)^{n-1}\times\frac{1}{\sigma\sqrt{2\pi}}e^{\frac{-(\tau-\mu)^2}{2\sigma^2}} \qquad (7)$$

Fig. 3.a also shows the probability distribution of the crossbar lifetime up to the first failure *(PDF(g))*. We have found the mean and standard deviation of the g by numerical calculation. Next we verify the correctness of the *PDF(g)* with performing 10000 Monte-Carlo experiments. In each experiment we generate n random numbers (τ_1, τ_2, …. , τ_n) from the normal distribution with a known $\mu(\tau)$ and $\sigma(\tau)$, each one representing the lifetime of a single memristor and then we find the minimum value among them. As expected the *PDF(g)* from the Monte Carlo analysis in Fig 3.b perfectly matches with our analytic approach.

In the following we proceed to find the probability distribution of cycles up to the second failure. By having the number of cycles at the beginning (τ) and at the point of first failure (g), we define another random variable (h), which is lifetime at cycle zero minus the time of the first failure as in (8):

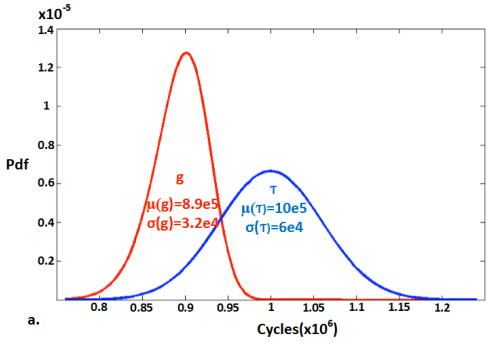
$$h = \tau - g \qquad (8)$$

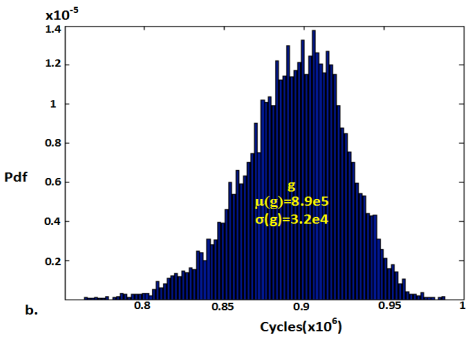
Then equation (9) presents the mean value for the h and (10) presents the standard deviation. Note that since τ and g are not independent random variables the $\sigma(h)$ is calculated by considering the correlation factor (ρ) as in 10:

$$\mu(h) = \mu(\tau) - \mu(g) \qquad (9)$$

$$\sigma(h) = \sqrt{\sigma^2(\tau)+\sigma^2(g)+2\times\rho\times\sigma^2(\tau)\times\sigma^2(g)} \qquad (10)$$

Next, to obtain the crossbar lifetime up to the second failure, similar to the first failure, we need to find the *PDF(y)*, when $y=Min(h_1,h_2, \ldots, h_{n-1})$. It is now *n-1* because one memristor is not considered after the first fail. In this sense Fig. 3.c shows the probability distribution of lifetime for a crossbar up to the second failure (which is the number of cycles for the interval between first and second fail).





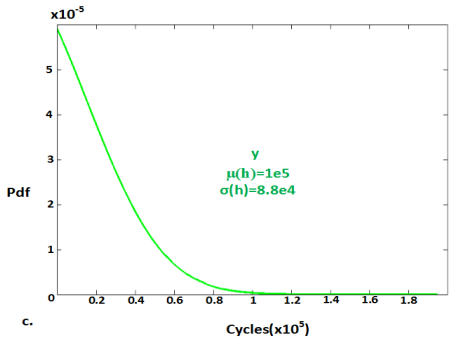


Fig. 3. a)The τ and g probability distributions b)The g probability distribution verified from Monte-Carlo c)The y probability distributions

V. Conclusion

An analytical procedure has been presented to evaluate the lifetime of n-elements crossbar for the first and second failure. The results, verified from Monte Carlo analysis show that the lifetime is highly reduced for posterior fails after the first and mainly second failure. This implies the need to establish efficient reconfiguration mechanisms to achieve reliable memristive crossbar applications.

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