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# Lithography parametric yield estimation model to predict layout pattern distortions with a reduced set of lithography simulations

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**Abstract.**
   A lithography parametric yield estimation model is presented to evaluate the lithography distortion in a printed layout due to lithography hotspots. The aim of the proposed yield model is to provide a new metric that enables the possibility to objectively compare the lithography quality of different layout design implementations. Moreover, we propose a pattern construct classifier to reduce the set of lithography simulations necessary to estimate the litho-degradation. The application of the yield model is demonstrated for different layout configurations showing that a certain degree of layout regularity improves the parametric yield and increases the number of good dies per wafer.

**Keywords:** Design for manufacturability, lithography hotspots, yield estimation, layout design.

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## 1 Introduction

One of the main challenges for continuing technology node scaling down is the resolution limit of lithography tools. Due to a number of technical reasons, the light wavelength is very difficult to scale down and it remains fixed at 193nm for the current and next CMOS generations. Leading-edge foundries are using today's 193nm immersion lithography with double (or multiple) patterning since extreme ultraviolet (EUV) lithography of 13nm wavelength still faces considerable burdens for production of 14nm and even 10nm technology nodes.[1]

The effect of the lithography gap in current and upcoming technologies is to cause severe distortions due to optical diffraction in the printed patterns and thus manufacturing yield is degraded.[2] These distortions also produce a change in the expected circuit parameters (transistor dimensions, wire resistance and capacitance, contact resistances, etc.) causing deviations in the overall circuit specifications of performance and power[3] and thus degrading the parametric yield of a circuit.

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The existence of lithography induced variations is the cause that the usage of RDRs (Restrictive Design Rules) increase in each new technology node.[4] Therefore, it is necessary to rethink layout design in order to obtain cost-effective and efficient designs compared to traditional 2D designs with arbitrary patterns. In order to enhance layout printability, new regular litho-friendly cell designs are being proposed to avoid lithography-unfriendly patterns.[2,5,6] However, the main drawback of regular layouts is that they introduce area overhead. Hence, it is necessary to find a methodology to properly evaluate different layout styles that quantifies the trade-off between the benefits of regular layouts and area penalty.

This work presents a lithography parametric yield estimation model to objectively estimate the amount of lithography distortion that can be expected in a printed layout due to lithography hotspots. The lithography distortion is evaluated using an enhanced version of the yield model presented in a previous work.[7] The main aim of the proposed yield model is to provide a new quantification metric that enables the possibility to objectively compare the lithography impact on different layout design implementations. The framework here presented serves as vehicle to determine the best layout design or to quantify the amount of regularity that can be admitted in a design while at the same time maximizing the number of Good Dies Per Wafer (GDPW).

We propose an efficient lithography hotspot identification framework to find the different layout pattern configurations, simplify them to ease the pattern analysis and classify them using lithography simulations according to their predicted lithography degradation. The lithography hotspot classification and the pattern simplification are key aspects of the framework so the lithography distortion can be captured with a reduced set of lithography simulations.

The yield model is calibrated with delay measurements of a reduced set of identical test circuits implemented in a CMOS 40nm technology and thus actual silicon data is utilized to obtain a more

realistic parametric yield estimation. The goal of this lithography evaluation framework is not to give a perfect prediction of yield impact but to have an objective way of evaluating the layout quality in terms of lithography distortion without an excessive number of lithography simulations and with reduced information from silicon data.

The paper is organized as follows. Related work by other authors is briefly reviewed in Section 2. The yield formulation model is explained in Section 3. Section 4 describes the lithography hotspot framework to identify, simplify and classify the different layout pattern configurations occurring in a layout design. The yield model is calibrated using test chip measurements and it is applied to compare different layout designs in Section 5. The paper concludes in Section 6.

## 2  Related work

The estimation of the lithography impact on yield can be mathematically related to a probability of non-failure of lithography hotspots. Previously, Kobayashi, Kyoh et al. proposed a yield model which considers lithography hotspots to evaluate the degradation of a circuit.[8, 9]

In 2011 Chang, Kagalwalla and Gupta introduced the concept of electrical process window (EPW) that takes into account the effect of lithography distortions of the transistor channel on electrical performance of the circuit and its design margin.[10] This concept is very much related to the topic addressed by the present paper. In Chan's work, distortion in transistors is considered to have a deterministic effect which is evaluated by electrical simulations of library cells and SRAM cells. In our work instead, we consider that the effect of the multiple distortions, both in transistors, interconnections and vias, is statistical. We do not obtain exact values of tolerance, but we adjust our statistical model with measurements in order to use this metric as a comparison tool between different libraries of various layout styles. More recently, Banerjee, Agarwaal, Nassif and

Orshansky also addressed the relation between lithography imperfections and design tolerances with the objective of improving the design-manufacturing interface and the design rules regarding manufacturability.[11, 12]

The precise lithography hotspot identification has also become a concern in both layout design and manufacturing. Several works[13, 14] propose efficient algorithms that analyze the layout to identify critical shapes that produce excessive distortion.

## 3 Parametric yield formulation model

A parametric yield estimation model to assess the lithography distortion in a printed layout is a useful and objective way to compare different layout implementations using physical effects as a basis for evaluation. The goal of this work is to provide an objective way of evaluating the lithography distortion and its impact on yield. In this section, the proposed yield formulation model and how to capture the lithography distortion into the yield model are described.

### 3.1 Yield definition

Yield is defined as the ratio of the number of circuits that are functionally correct and meet the target specifications to the number of manufactured circuits.[3] Yield can be classified in two different types. *Catastrophic yield loss* refers to circuits that suffer from functional failures, such as opens or shorts that cause part of the circuit to not work properly. This kind of failures are traditionally caused by particle defects that falls down into the circuit, as depicted in Figure 1. Critical area analysis is used to predict this kind of yield loss.[15] The other type of yield is referred as *parametric yield loss*. In this case, the circuit is functionally correct but it fails to satisfy either performance or power specifications due to deviations in the circuit parameters. Parametric failures may be caused

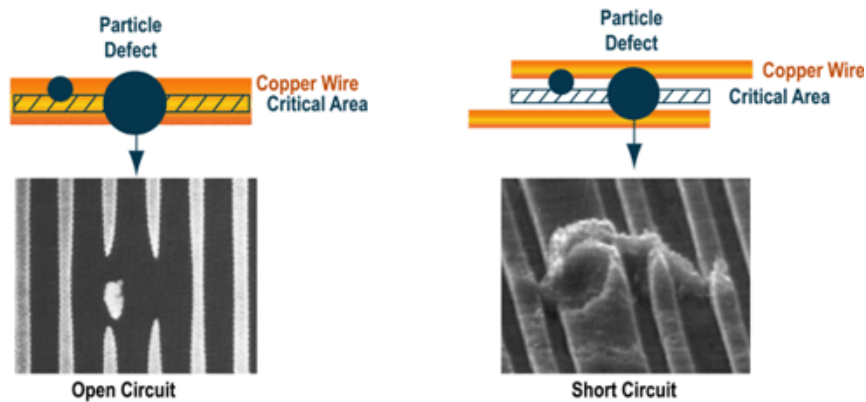by process variations, including printed pattern variations.



**Fig 1** Example of particle defects causing catastrophic yield failures.[16]

The effect of the lithography gap in current and future technologies is to cause a distortion of the shapes actually printed on silicon. For instance, instead of the designed rectangular shapes, rounded shapes are actually printed. This distortion causes a change in the expected parameters of the circuit: transistor dimensions, wire resistance and capacitance, contact resistances, etc. Finally, the change in parameters modifies the overall circuit specifications of performance and power.
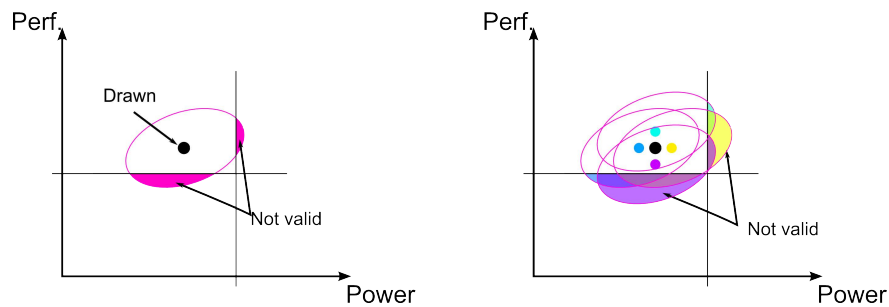


**Fig 2** Region of invalid circuits for Drawn circuit (left) and distorted versions of circuit (right) considering power and performance.

Excessive lithography variations in a poorly controlled process might also cause a wire to break (causing an open circuit) or to merge with a neighboring wire (a short circuit) and thus cause catastrophic yield losses. However, the lithography simulations performed on the 45nm technology node considered in this work produces layout with no catastrophic failures. Therefore,

while certainly lithography hotspots may also induce catastrophic failures, especially in smaller technology nodes, only yield losses associated to parametric failures are considered in this work.

In an ideal process without printed shape distortion there would still be several other sources of variability (for instance, random dopant fluctuations, environmental conditions, and so on) which equally apply to real processes that present some degree of lithography distortion. In the case of an ideal design with no distortion, the parametric yield depends on the proximity of the design at nominal conditions (no variations) to the specification limits. In general, lithography process variations will create a multiplicity of nominal conditions, one for each lithography process condition (see Figure 2). Therefore, parametric yield will be affected. It is generally assumed that distortion is larger for non-regular, 2D layouts[17, 18] and this is the ultimate basis for the efforts in the literature in designing cells with more regular (equidistant, 1D) layout features.

In summary, the idea behind the yield model here presented is to capture the systematic lithography variability that will produce losses on the parametric yield of a circuit. Note that, hereafter, all the yield references correspond to parametric yield.

*3.2  Parametric yield model*

The reasoning behind the yield model here proposed is based on the fact that each individual shape in the layout contributes in some way to the overall circuit specification. The problem is that it is difficult to say how the distortion of each individual shape will influence the overall specification. In fact, the same amount of distortion in a given pattern construct can be bad in one node and good in another, or have no effect at all. For this reason, the effect of each lithography hotspots on the overall specification is considered in the model here presented as a random process with a probability of non-failure, i.e. that the circuit is still valid. Therefore, the overall effect is

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understood as an accumulative probability that depends on the identification of those distortions that produce a significant impact on circuit characteristics (for example, increasing RC constant of wires, or decreasing channel length). In this proposal, layout quality is then evaluated by counting the number of such cases and rating them to obtain a quantification metric.

Total yield can be expressed as a combination of yield due to catastrophic and parametric faults. The first component is the conventional way of estimating yield and it can be represented with the Poisson model as a function of the critical area.[15]

$$Y_{A_{cr}} = e^{-A_{cr} \cdot D_d} \tag{1}$$

where $Y_{A_{cr}}$ denotes the critical area yield, $A_{cr}$ is the critical area and $D_d$ is the density of defects.

Equation 1 does not capture the dependency on lithography and printability variations that also affect both catastrophic and parametric yield. In order to take into account the effect of lithography distortion on yield, the impact of lithography hotspots (*lh*) needs to be analyzed. A lithography hotspot is defined as a pattern construct in a layout susceptible to suffer excessive variation under lithography printing.[13] As already explained, even though lithography hotspots may contribute to catastrophic yield loss, in this work we aim to model only the parametric yield loss component.

The parametric yield formulation here presented is based on the probability $p$ that a particular lithography hotspot in the layout and its associated distortion still makes the circuit valid, i.e., it still complies with the specification. We base our mathematical model on the assumption that the effect of each hotspot on the overall performance is a random process statistically independent of the effect of the other hotspots. While this may be considered as a controversial assumption, it merely reflects the impossibility to accurately model the effect on performance of each individual

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hotspot. Note that even though the hotspots themselves are physically correlated (for example, in a given process corner all rectangles may become wider), in some nodes this variation may be detrimental reducing the performance margin while in other nodes it may increase the margin. The correlation is on the distortion, but its effect on performance is assumed to be uncorrelated.

With this assumption the yield due to a number of hotspots can be calculated as the product of the probability $p_i$ of each hotspot. The expression of yield for a layout with $N_h$ number of hotspots is:

$$Y_{lh} = p_1 \cdot p_2 \cdots p_{N_h} = \prod_i^{N_h} p_i \tag{2}$$

Thus, $p_i = 1$ means that hotspot $i$ has so small distortion that with all certainty it causes the circuit to be inside specifications. Therefore, if all the hotspots had this value, it would mean that there is no (parametric) yield loss due to lithography. Putting Equation 2 in exponential form:

$$Y_{lh} = e^{-\sum_{i=1}^{N_h} \lambda_i} \tag{3}$$

where the parameter $\lambda_i$ (lambda) represents the difficulty to print the hotspot (distortion). Lambda is related to the probability of non-failure as:

$$\lambda_i = -ln(p_i) \tag{4}$$

Lambda is a real positive number, with 0 meaning that the hotspot distortion does not affect yield at all and large values meaning a large impact on yield. Note that the lambda parameter must capture two important aspects. The first aspect is the distortion and variability introduced by lithography

and the second aspect is the tolerance of the specifications, i.e., the design margin. The lambda parameter will be the basis of the proposed yield estimation metric, to which it is necessary to relate an objective measurement of lithography distortion.

*3.3 Lambda model*

The lambda parameter is associated to the probability of non-failure of a lithography hotspot. However, it is not possible to have a true analytical expression for yield loss and associated probability. In the proposed model, the lambda parameter is related to a measurement of the amount of distortion of a lithography hotspot.

The lambda parameter is obtained following several steps. The first step is to have an evaluation of the distortion based on lithography simulations. For this purpose, the LFD tool from Mentor Graphics[19] is used. This tool calculates the printed contours of a layout for different process conditions, known as a process window. From this process window a maximum and minimum printed edge placement are calculated. From these, maximum variation between printed and drawn layout is obtained, which is called Absolute PV-bands. The LFD tool can then calculate the area of the absolute PV-bands (degraded area, $Area_{deg}$) in a defined region of interest (*analysis window*) and compare it to the area of the original layout ($Area_{drawn}$) in the same analysis window in order to obtain a measure of the amount of distortion and variation expected in the printed layout. Figure 3 depicts how the distorted area is obtained in the analysis window. With the obtained data, the LFD tool defines a distortion index (Process Variation Index$^{TM}$, *PVI*) as follows:

$$PVI = \frac{Area_{Abs\_PVband}}{Area_{layout}} = \frac{|Area_{drawn} - Area_{printed}|}{Area_{drawn}} = \frac{Area_{deg}}{Area_{drawn}} \tag{5}$$

This index is a real positive value. Value 0 means a perfect printing and no distortion. In the case of printed contours inside the drawn layout, value 1 is an extreme case that implies that an inner printed shape is not printed and results in null area. For printed contours outside the drawn shapes, the *PVI* could be even larger than 1 for excessively uncontrolled processes. Nevertheless, we take 1 as the practical limit of *PVI* that can be achieved in reasonably controlled processes.

The proposed yield model uses the *PVI* index as an objective measure of the severity of each hotspot and the lambda parameter is calculated from this index. The relation between both magnitudes is based on the observation that lambda, defined by Equation 4, is a number between 0 (for 'perfect' hotspots, not giving any yield loss due to distortion) and, in principle, infinity. On the other hand, the *PVI* index is between 0 (no distortion) and 1 (maximum distortion in a controlled process).
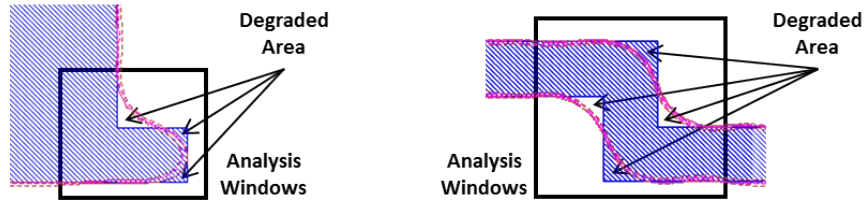


**Fig 3** Lithography distortion of different hotspots and their respective areas of printed (simulated) and drawn layout.

Considering that a certain level of distortion is unavoidable, but does not produce any yield loss, a simple function that relates the lambda index of hotspot *i* (and ultimately, the yield estimation) with the *PVI* index obtained from the LFD is defined as follows.

$$
\lambda_i =
\begin{cases}
0 & PVI_i \leq PVI_{min} \\[2ex]
S \cdot \frac{PVI_i - PVI_{min}}{1 - PVI_i} & PVI_{min} < PVI_i < 1
\end{cases}
\tag{6}
$$

This generic function maps the $PVI_i$ number between 0 and 1 to a new number between 0 and

infinity. The $PVI_{min}$ parameter refers to the minimum tolerable lithography distortion of the printed layout patterns that does not degrade the lithography yield. The parameter $S$ is a scaling factor that must be adjusted to give reasonable estimates of yield loss according to the technology employed, the design margin and the layout design style. The calibration of the yield model using silicon data is illustrated with an example in Section 5.

## 4 Pattern construct - hotspot identification

The concept of a lithography hotspot is related to the concept of Pattern Construct (*PC*): a *PC* contains a central layout polygon (*CLP*) or part of it and all the neighboring edges within a specific distance of interaction. The concept of a hotspot and a pattern construct with simplified neighbors are depicted in Figure 4.
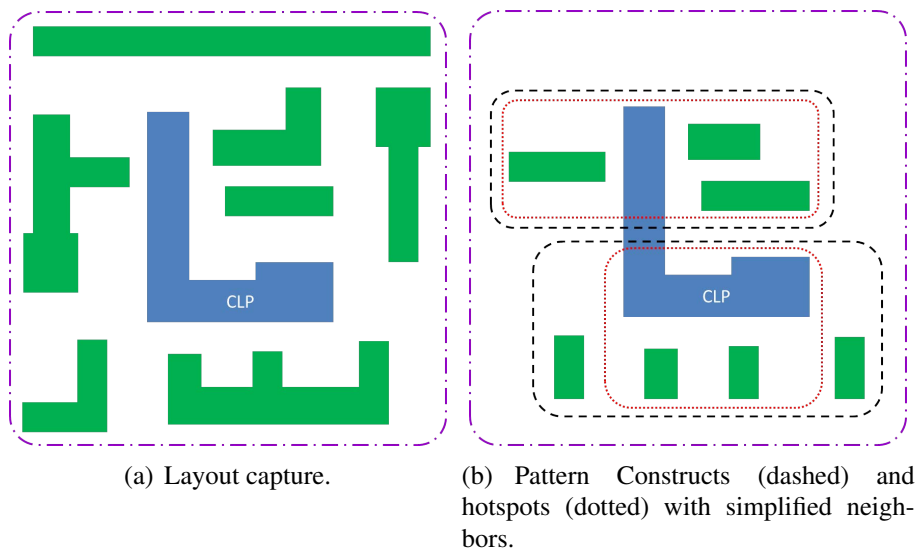


(a) Layout capture.   (b) Pattern Constructs (dashed) and hotspots (dotted) with simplified neighbors.

**Fig 4** Examples of pattern constructs and hotspots. The Central Layout Polygon (*CLP*) is depicted in blue and neighbors in green. The simulated contours of these examples are illustrated later in Figure 8.

Pattern construct identification is required in order to analyze the different layout shapes employed in a design and calculate their *PVI* and lambda indexes. In this work, we present a methodology based on an exhaustive search of all pattern constructs. Computing the *PVI* index for each

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pattern construct is impractical due to the huge number of different patterns in a typical layout. Hence, a pattern simplification is applied in this paper to decrease the amount of lithography simulations as will be explained in Section 4.3. Moreover, the *PVI* index of *compound* pattern constructs can be approximated by combining the lithography information of previously known *basic* pattern constructs and thereby the amount of lithography simulations can be further decreased, as detailed in Section 4.4.

With this methodology a cell library composed of a few hundred cells can be analyzed in some minutes, and a complete circuit with many thousands of gates require a few hours. Several other more efficient and sophisticated approaches for pattern discovery than our proposal are also possible, such as those based on machine learning and/or pattern matching techniques.[13,14] Note that the proposed methodology is aimed at the 45/40nm node where the main interaction occurs between nearest neighbors. For future technologies with more complex interactions, the presented methodology might be updated to incorporate new lithography distortion effects at the cost of increased complexity.

### 4.1  Pattern construct discovery flow

The evaluation framework for hotspot identification and assignment of a severity index is divided in two parts. Firstly, a preliminary *technology characterization* based on accurate lithography simulations where a pattern construct class library is generated, containing the *PVI* index of the most significant identified pattern construct class for each layer. Once this library is obtained, the *evaluation flow* applies this information to the layout under analysis without the need to undertake lithography simulations for their evaluation. The different steps needed to obtain the evaluation of a layout are explained in Figure 5.
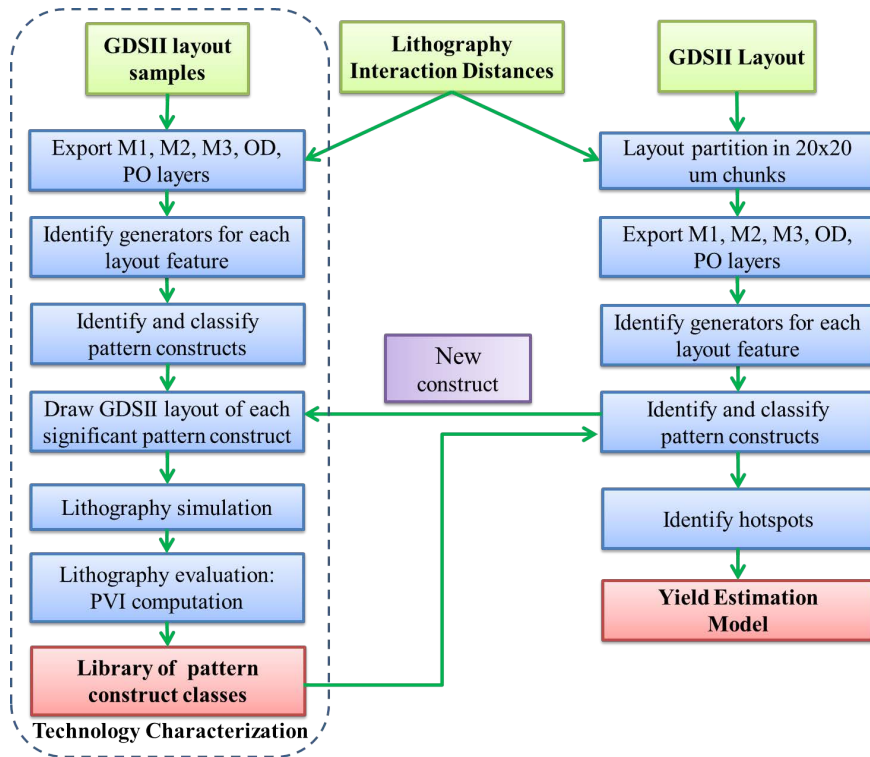
**Fig 5** Steps needed to obtain the evaluation of a layout.

The first part of the design flow is referred to as the technology characterization stage. The aim of this stage is to obtain a library containing the most significant pattern construct classes with its respective lithography evaluation score obtained using lithography simulations. The pattern construct class library can be obtained using as input a small set of training cells with different representative layout configurations. The procedure to find all pattern constructs and classify them into groups is the same as in the evaluation flow and it will be described in the next two sections. Once the pattern constructs are identified and classified, lithography simulations are performed to calculate the *PVI* index for each of them. Using this *PVI* index, only those pattern constructs that suffer excessive variation are considered as hotspots, i.e., those with a *PVI* index larger than a minimum degradation threshold ($PVI_{min}$). After the technology characterization phase, the pattern construct class library that will be used during the evaluation flow is created. Note that the class library is updated in case that a new significant pattern construct is identified in a new layout.

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The evaluation flow extracts all the pattern constructs of the GDSII layout under analysis and then, using the library of pattern construct classes, all hotspots are identified and assigned the previously obtained *PVI* index. The advantage of the previous technology characterization stage is that costly lithography simulations are only performed at that stage and thus the lithography evaluation is highly simplified. Note that if multiple patterning techniques are applied in the manufacturing processing, each GDSII layout will only contain the patterns belonging to the same printing mask. As a final step, the yield estimation model takes the number and type of hotspots as the basis to estimate the impact of lithography printability on layout design.

### 4.2 Pattern construct identification

The analysis of the layout implies the identification of geometric pattern constructs that will later be classified as hotspots, or not, depending on their severity. This analysis requires two inputs: a GDSII file of the layout and a set of lithography interaction distances (*LID*) as detailed in Figure 6. The *LID* must be pre-characterized for each layer using lithography simulations for the technology of interest.

The pattern construct search starts finding all the *generators* of a GDSII layout for each layer. A generator is a rectangular area of a layout which contains all the layout polygons within a specific distance of interaction ($d_{int}$) from each edge around a central layout polygon (*CLP*), as depicted in Figure 4(a). The $d_{int}$ is obtained using the equation detailed next:

$$d_{int} = max\{d_4 + d_{11}, d_4 + d_{12}\} \tag{7}$$

where the $d_i$ are the lithography interaction distances to properly capture the pattern neighborhood

detailed in Figure 6. This distance $d_{int}$ is configured based on the lithography interactions observed between the different layout patterns in the 45nm technology employed. For smaller nodes like 32nm, 22nm or 14nm, this distance might be enlarged, thus increasing the size of the layout generators.

The pattern construct recognition takes vertexes ($V$) and edges ($E$) as the primitive geometries within which the pattern constructs are analyzed. In each generator one or more pattern constructs may be identified according to the following attributes:

- Type of layout pattern construct.

- Vertexes and angles of the layout patterns in the pattern construct.

- The lithography interaction distances of the layout patterns in the pattern construct.

- Relation of the central pattern with closest neighbors: whether they are placed contiguously or oppositely with respect to it and other neighbors.

| $d_i$ | Description |
|-------|-------------|
| 1 | Max interaction between consecutive $V$. |
| 2 | Max interaction between non consecutive $V$. |
| 3 | Min edge length to suffer degradation. |
| 4 | Max external distance of interaction. |
| 5 | Max degradation that extends from a $V$. |
| 6 | Max extension of degradation caused by a $N$. |
| 7 | Max distance to consider contiguous neighbors ($d_7 = 2d_6$) |
| 8 | Max distance to consider opposite $N$ (side direction) ($d_7=d_8$). |
| 9 | Max distance to consider opposite $N$ (front direction) ($d_9=2d_4 + W_{max}$). |
| 10 | Max distance that a $N$ affecting an $E$ can affect a $V$ ($d_{10} = d_5 + d_6$). |
| 11 | Min edge extension of a $N$ to cause distortion. |
| 12 | Maximum width to consider a $N$ harmful. |
| 13 | Line-End layout extension for contacts. |
| $W_{max}$ | Max width of any E affected by a N. |
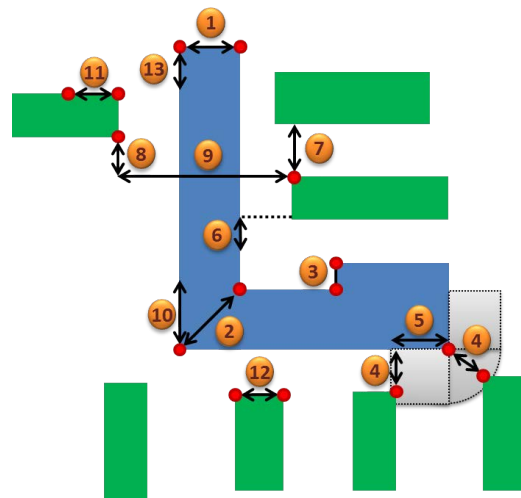


**Fig 6** Lithography Interaction Distances (*LID*). (V) Vertexes; (E) Edges; (N) Neighbors.

Once a pattern construct is identified, it is classified in terms of its difficulty to be printed with the *PVI* index. The value of the obtained *PVI* index depends on the number of shapes and vertexes involved as well as their angles and relative distance. Hotspots are then detected as those pattern constructs with a *PVI* index above a given threshold. The steps of the pattern construct discovery and the hotspot detection are described in Figure 7. The different types of pattern constructs identified are described in the following sections.

```
 1: $\mathcal{D}$ = Lithography Interaction Distances;
 2: $\mathcal{C}$ = GDSII layout Circuit;
 3: $\mathcal{L}$ = Pattern construct class Library;
 4: for all $layers \in \mathcal{C}$ do
 5:    for all $fragments \in \mathcal{C}$ do
 6:       $\mathcal{G}$ = Identify Generators($fragments$);                    ▷ Each $\mathcal{G}$ can have several PCs;
 7:       for all $Generators \in \mathcal{G}$ do
 8:          $V(\mathcal{D},CLP)$ = Identify group of vertexes affecting each other in CLP;
 9:          $NV(\mathcal{D},V)$ = Identify group of neighbors that affects V;
10:          $NE(\mathcal{D},E)$ = Identify group of neighbors that affects E;
11:          Analyze relation between N;         ▷ Opposite N, contiguous N, N affecting EaV;
12:          $pcV2V(NV)$ = Identify Vertex Layout Patterns;
13:          $pcV2E(NE)$ = Identify Edge Layout Patterns;
14:          $pcEaV(pcV2V,pcV2E)$ = Identify combined $pcV2V$ and $pcV2E$;
15:          $PC_{basic}$ = Identify basic PC classes;
16:          $PC_{compound}$ = Identify compound PC classes;
17:          $PC_{new}(PC_{basic},PC_{compound})$ = Identify new high occurrence PC classes;
18:          Update_PClib($\mathcal{L}$,$PC_{new}$);
19:          $lh(PC_{basic},PC_{compound})$ = Identify hotspots($\mathcal{L}$);
20:          $Yield(lh)$ = Compute yield estimation;
```
**Fig 7** Steps of the hotspot detection.

This pattern construct discovery algorithm was built using a custom software implemented in Matlab and C.

## 4.3 Lithography pattern construct classification

In a typical layout there are millions of different pattern constructs and thus hotspot configurations. This is especially true for traditional standard cell designs with non-regular patterns and in this sense the use of regular design styles greatly facilitates the lithographic analysis needed for layout characterization.

Some simplifications are considered in the pattern construct classification algorithm that are aimed at reducing the number of different pattern constructs. First, the neighboring layout polygons are simplified by only considering the edges affecting the central layout polygon instead of the complete neighboring layout polygons. This simplificaton, as shown in Figure 8, shows that very similar lithography results on the central pattern are obtained, compared to the results of the original layout. Second, two pattern constructs are considered equal if they have the same geometric configuration (*class*), independently of the exact distances and dimensions of each element. For instance, a line-end with two different edge lengths are considered to belong to the same class.
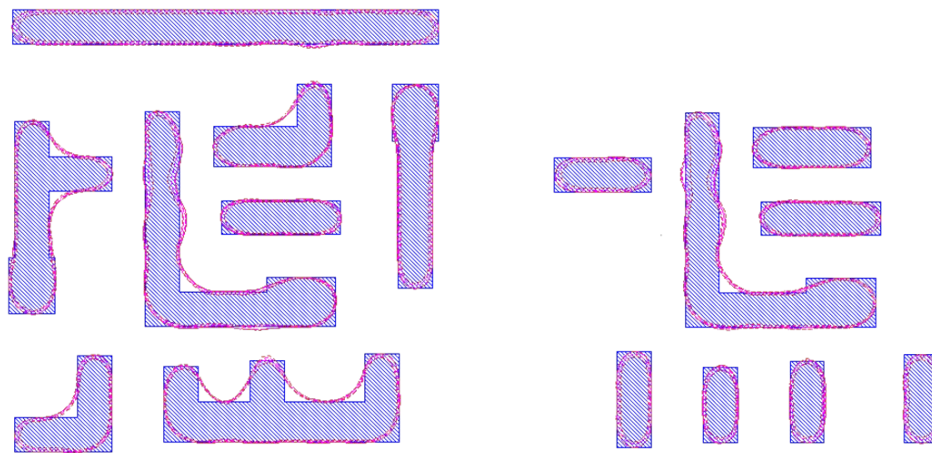


(a) Layout capture without pattern simplification.  (b) Layout capture with pattern simplification.

**Fig 8** Layout capture with lithography simulations to illustrate the pattern neighborhood simplification.

These simplifications might be inaccurate for smaller technology nodes. The aim of this pro-

posal was to minimize as much as possible the lithography effort considering the technology node we had access to (45/40nm).

The different pattern constructs are distributed into classes according to the PC attributes described in Section 4.2 considering the following criteria. Firstly, patterns constructs are classified considering the number of consecutive vertexes of the central layout pattern and their respective angles. However, consecutive vertexes with a small distance between them are discarded in the classification since they obey to special design rules (typically, poly contact enclosures) that improve the printed shape. Secondly, non-consecutive vertexes close to each other (typically, an L shape as depicted in Figure 9) are grouped together as part of the pattern construct. Thirdly, neighboring pattern edges within the range of interaction to one of the vertexes are also included in the pattern construct.

The enumeration of the basic pattern construct classes is graphically depicted in Figure 9 and their explanation is detailed in Table 1. The lithography evaluation of the pattern constructs is described in Section 4.4.
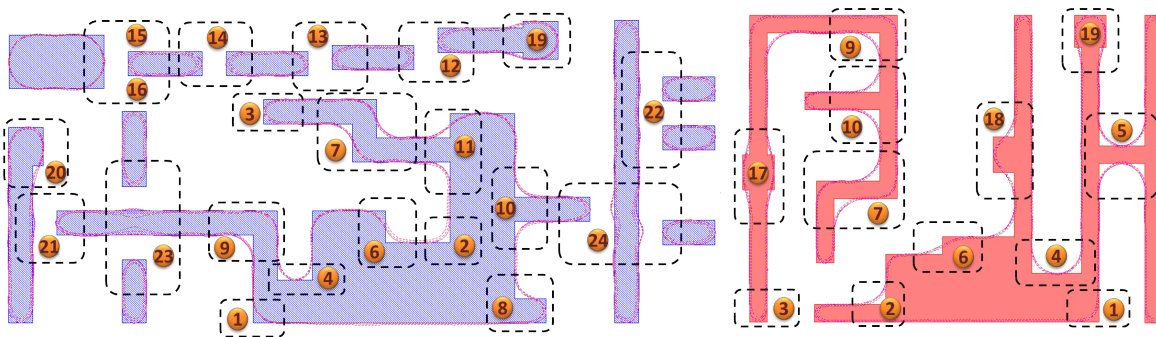


**Fig 9** Lithography Classes. (Left) Diffussion and Metal classes; (right) PO classes.

The classification shown in Table 1 has been obtained analyzing the layout of 24 basic cells designed in different layout styles and it has been tested for 9 benchmark circuits implemented also with different layout configurations. New classes appearing frequently in the layout are character-

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**Table 1** Pattern Construct classes description.

| Class | Name | Description |
|---|---|---|
| 1 | In-vertex | Single 90° corner. |
| 2 | Out-vertex | Single 270° corner. |
| 3 | Line-end (LE) | Two consecutive 90° vertexes. |
| 4 | Out-U | Two consecutive 270° vertexes. |
| 5 | H | Two consecutive 270° vertexes placed closed by another two consecutive 270° vertexes. |
| 6 | Snake | A 90° vertex followed by a 270° vertex. |
| 7 | Double Snake | A 90° vertex followed by a 270° vertex placed closed by another 90° vertex followed by a 270° vertex. |
| 8 | Toe | 90°, 90°, 270° vertexes placed closed by a 90° vertex. |
| 9 | L | 90° vertex placed closed by a 270° vertex. |
| 10 | T | 270° vertex placed closed by a 270° vertex. |
| 11 | T-Hammer | A 90° vertex followed by a 270° vertex placed closed by a 270° vertex. |
| 12 | LE Pull-back Short | Two LE placed in front of each other when less than half of the opposite edges interact between each other. |
| 13 | LE Pull-back Long | Two LE placed in front of each other when more than half but less than all of the opposite edges interact between each other. |
| 14 | LE Pull-back All | Two LE placed in front of each other when both edges with equal length interact between each other with all its length. |
| 15 | LE Pull-back Big Neighbor | Two LE placed in front of each other with the neighboring edge bigger interact between each other with all its length. |
| 16 | LE Pull-back Small Neighbor | Two LE placed in front of each other with the neighboring edge smaller interact between each other with all its length. |
| 17 | Edge Center Enclosure | 270°, 90°, 90°, 270° vertexes placed closed by another 270°, 90°, 90°, 270° vertexes, forming an enclosure |
| 18 | Edge Displaced Enclosure | 270°, 90°, 90°, 270° vertexes placed consecutively. Enclosure displaced to one side of the edge. |
| 19 | LE Center Enclosure | 270°, 90°, 90°, 90°, 90°, 270° vertexes. An enclosure placed at the end of an edge, i.e, in a LE. |
| 20 | LE Displaced Enclosure | 270°, 90°, 90°, 90°, 90°, 270° vertexes. An enclosure displaced to one side of the LE. |
| 21 | Sharp Neigh | Neighboring sharp edge placed towards a layout edge. |
| 22 | Sharp CONT Neighs | Two neighboring sharp edges placed consecutively towards a layout edge. |
| 23 | Sharp Opposite (OP) Neighs | Two neighboring sharp edges placed in front of each other with a layout edge in between. |
| 24 | Sharp DIAG OP Neighs | Two neighboring sharp edges placed each other in one side of a layout edge, but not in front of each other. |

ized and added to the library of simulated classes. The most significant cases depend first on the technology, and second, on the layer analyzed. For example, the poly layer, in general, has more simple constructs than the metal1 layer. Again, it should be noted that for future technology nodes with more complex interactions the proposed classification should be increased in order to more accurately estimate the yield losses.

*4.4 PVI computation of basic classes*

In addition to the basic pattern constructs shown in Figure 9, some shapes in the layout can be considered as combinations of simpler pattern constructs. We call these complex shapes *compound* pattern constructs (see Figure 11 for an example). Basic pattern constructs are simulated to calculate their *PVI* index. In the case of compound pattern constructs, their *PVI* index is calculated from a combination of *PVI* of the basic pattern constructs that they are composed of. This is explained in Section 4.5.

For each identified basic pattern construct class, a representative layout is created to apply a lithography simulation and obtain its *PVI* index. The representative layout takes into account the minimum distances and dimensions allowed by the technology. In this way, slightly different pattern constructs that belong to the same class differing only in dimensions (within the lithography interaction distance of the technology) are assigned the same value of *PVI* and thereby the number of required lithography simulations to characterize the library is greatly reduced. It has to be noted that this simplification will produce more precise results for regular designs with a small set of possible geometric configuration of pattern constructs.

In order to compute the *PVI* index it is necessary to define a geometric region called *analysis window*. This region is initially defined by a rectangular region defined by the outermost vertexes

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in the pattern construct, and then enlarged by displacing each edge of the region up to a distance where the lithography degradation is negligible. Two examples of common analysis windows are depicted in Figure 10(a) for classes 2 and 9. Once the appropriate analysis window is defined for each class, a lithography simulation is performed and the *PVI* index is calculated.

There are two special cases, classes In-vertex (1) and Line-end (3), where the conventional way of defining the analysis window produces unreasonable *PVI* values compared to other classes. These two cases must be analyzed separately studying the utilization of each pattern construct and the geometries of similar patterns. On the one hand, class 1 has a similar class, class Out-vertex (2), and another class, class L (9), can be thought of as a combination of classes 1 and 2. Therefore, the analysis window for class 1 is defined with the same region used for class 2 and class 9. On the other hand, Class 3 (Line End) is similar to Class 19 corresponding to a contact enclosure and therefore, in order to have a fair comparison between these two classes, their analysis window should be the same. Figure 10 illustrates these two special classes comparing them to the related classes.
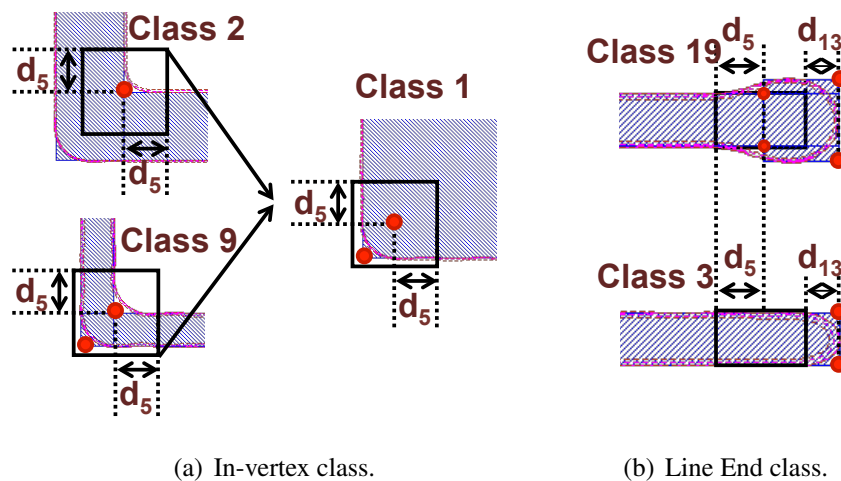


(a) In-vertex class.    (b) Line End class.

**Fig 10** Special pattern construct classes with specific analysis windows. Drawn layout and lithography contours.

*4.5 PVI computation of compound classes*

Additional pattern constructs can be considered as a combination of basic classes, giving rise to compound classes. In order to avoid the lithography simulation of compound classes, their *PVI* can be estimated using the degraded area of the basic classes. In a pattern construct, the following types are identified depending on the different interactions between the central layout polygon and the neighbors:

**Vertex to Vertex pattern constructs** ($pcV2V$)**:** Pattern constructs composed by a set of vertexes that affect each other. For instance, a line-end or a line-end Pull Back Long are two examples detailed in Table 1.

**Vertex to Edge pattern constructs** ($pcV2E$)**:** Pattern constructs formed by neighbors that affect an edge. Multiple contiguous and/or opposite neighbors are identified in this category, as described in Table 1.

**Edge and Vertex pattern constructs** ($pcEaV$)**:** Pattern constructs composed by a combination of vertex to vertex ($pcV2V$) and vertex to edge ($pcV2E$) pattern constructs. The union is produced when the degradation of a neighbor that affects an edge is merged with the degradation extended from a vertex.

The compound *PVI* is computed differently according to these three main categories of pattern constructs. The equations for the estimation of the *PVI* are detailed next:

- **Vertex to Vertex pattern constructs** ($pcV2V$): The degraded area is estimated as the sum of the degraded area of the central layout polygon (*CLP*) without any neighbor ($Area_{deg_{CLP}}$) and *NV* (number of neighboring vertexes) times the degradation introduced by only one

neighbor to a vertex ($Area_{deg_{NV}}$). The *PVI* index is then estimated as this degraded area over the original drawn area of the CLP:

$$PVI_{pcV2V} = \frac{Area_{deg_{CLP}} + NV \cdot Area_{deg_{NV}}}{Area_{drawn_{CLP}}} \qquad (8)$$

- **Vertex to Edge pattern constructs** (*pcV2E*): The degraded area is estimated as *NE* (number of neighboring edges) times the degradation introduced by only one neighbor to an edge ($Area_{deg_{NE}}$). The *PVI* index is then approximated as this degraded area over the original drawn area of the CLP:

$$PVI_{pcV2E} = \frac{NE \cdot Area_{deg_{NE}}}{Area_{drawn_{CLP}}} \qquad (9)$$

- **Edge and Vertex pattern constructs** (*pcEaV*): In this case, the degraded area is estimated as the sum of the degraded area of the central layout polygon (*CLP*) without any neighbor ($Area_{deg_{CLP}}$) and *NV* and *NE* times the degradation introduced by only one neighbor to a vertex ($Area_{deg_{NV}}$) and to an edge ($Area_{deg_{NE}}$) respectively. The *PVI* index is then estimated as this degraded area over the original drawn area of the CLP:

$$PVI_{pcEaV} = \frac{Area_{deg_{CLP}} + NV \cdot Area_{deg_{NV}} + NE \cdot Area_{deg_{NE}}}{Area_{drawn_{CLP}}} \qquad (10)$$

An additional correction is needed when dealing with large pattern constructs which are the repetition of smaller ones, as for example the one shown in Figure 11. In that example, all close vertexes are within the lithography interaction distance and therefore it has to be considered as a

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single large pattern construct. Consequently, the analysis window is also very large. The result is that the resulting *PVI* score is unrealistically small.
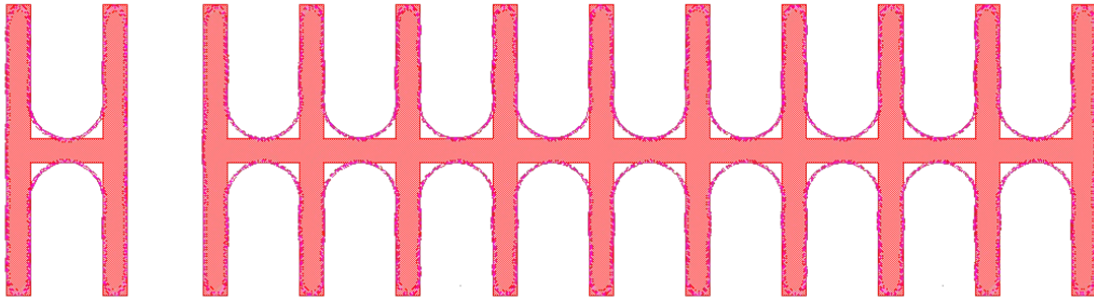


    (a) Basic PC class.         (b) Compound PC class composed by multiple instances of a Basic PC.

**Fig 11** Layout capture with lithography simulations showing two similar PCs with similar *PVI*, but totally different area drawn.

In order to counteract this effect, the *PVI* index of this kind of compound pattern constructs is computed as $N_{EPC}$ times the *PVI* index of the basic pattern construct it is made of. This parameter must be adjusted depending on the layer under analysis, the pattern construct class library utilized and the *PVI* results obtained.

## 5 Yield model calibration and test

In this section, the parametric yield model is calibrated against silicon measurements of design margin. With the obtained parameters, the yield model is applied to evaluate three different layout styles. These layout styles are: (1) fully uni-dimensional layout (F1D), a layout configuration using only 1D shapes in all layers; (2) half uni-dimensional layout (H1D), a layout style using 1D shapes for poly and 2D shapes for the rest of the layers; (3) fully two dimensional layout (F2D), a layout style using 2D shapes in all layers.[6] The different layout styles are illustrated in Figure 12. Three benchmark circuits have been created using these layout styles and routed using either 1D or 2D metal connections as required.
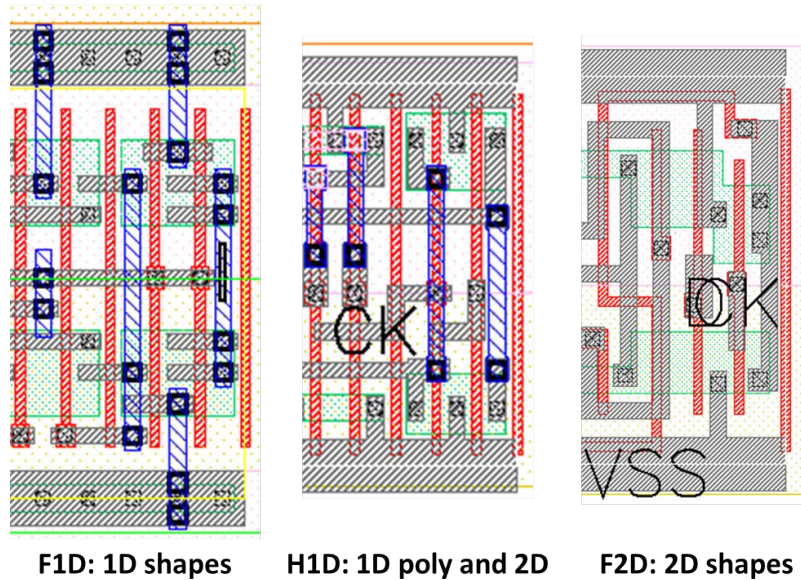
**F1D: 1D shapes      H1D: 1D poly and 2D      F2D: 2D shapes**

**Fig 12** Layout design styles examples. Fully regular layout (F1D), 2D layout with poly 1D (H1D) and a fully 2D (F2D).

### 5.1 Parametric yield measurements

The parameters of the yield estimation model must be calibrated in order to give reasonable values of yield loss according to the technology employed, the layout design style and the design margin. This calibration ensures that the ultimate goal of comparing different layout styles is based on real measurements and not only on a theoretical model. In this section, it is described how the yield estimation model can be calibrated with silicon data using as reference several test circuits implemented in a CMOS single patterning 40nm technology.[20] In this case, delay measurements are used as vehicle to illustrate the calibration methodology but any other metric can be employed, such as power measurements. This section shows that the yield model can be calibrated according to any yield curve obtained from real chip measurements and then these measurements can be related to an estimation of the lithography degradation of a layout design style.

The measurements were made on a test chip composed of 8 instances of voltage controlled delay line (VCDL). The VCDLs were implemented following two different layout styles: a totally

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regular 1D layout and a non-regular 2D layout. Transistors were sized sufficiently large to decrease the effect of random variations and therefore, the main source of variability was the systematic lithography distortion associated to layout dependent variations. The delay of 176 VCDL circuits (8 per chip and 22 chip samples) per layout design style was measured and the distribution of delay was computed as a percentage of the mean (assumed to be nominal) delay. Figure 13 depicts the delay histogram of the 176 VCDL instances where lithography variations make this delay different for each instance.
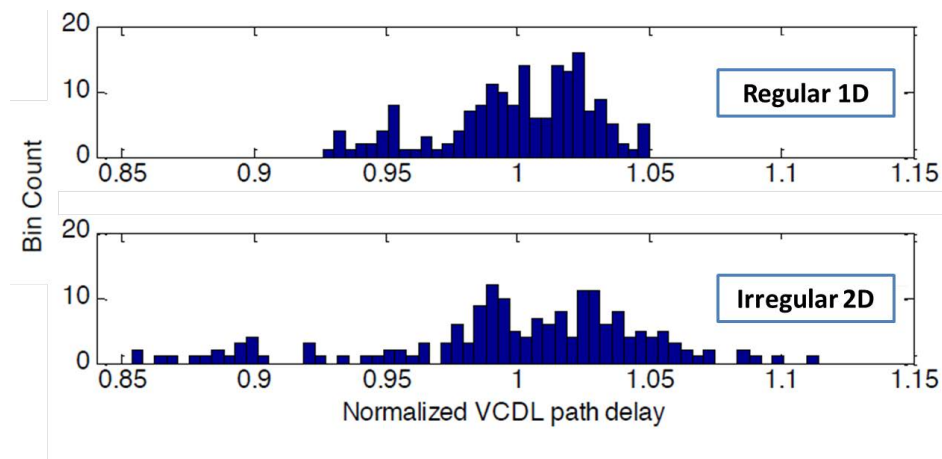


**Fig 13** Histogram of the normalized VCDL path delay for a regular 1D and a non-regular 2D layout design styles.

From the delay distribution, the *yield curve* is computed as the percentage of VCDL circuits with a delay larger or smaller than the nominal delay considering different delay boundaries. The latter boundaries can be interpreted as the necessary delay margin to ensure specification compliance of the circuit or, in other words, the amount of delay variation such that it still meets the timing constraints. Therefore, the yield is computed as the ratio of valid circuits (inside the delay target boundaries) and the total instances manufactured.

It is important to clarify that the delay-based yield measurements analyze the dispersion of the delay with respect to the nominal delay. In other words, the parametric yield measurements

mainly captures the impact of lithography and other sources of variability on the circuit delay. The resulting delay-based yield measurements curves are shown in Figure 14. As obtained from measurements, the curve corresponding to a regular layout presents a higher yield for any delay margin (*Design Margin, DM*) as a result of reduced dispersion in the delay among the samples. The measurements for a non-regular layout presents the lowest yield. Additionally, the mean between these two measurements is computed in order to obtain a third yield curve (*Average*).
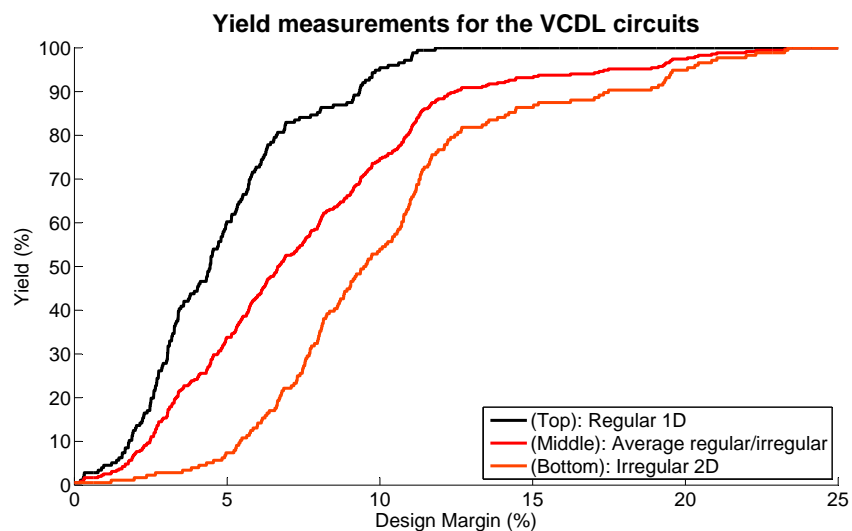


**Fig 14** Parametric yield measurements for the VCDL circuits implemented in silicon.

## 5.2 *Yield model calibration*

The calibration of the parametric yield model is made by means of finding suitable values of parameters $S$ and $PVI_{min}$ of Equation 6, in order to match the theoretical model to the values obtained from measurements. The $PVI_{min}$ is adjusted based on lithography simulations and the $S$ parameter is adjusted using the yield curves corresponding to measured yield from a circuit. The model is employed to compute the yield for three benchmark circuits: a Multiplier (*MUL*), an Image and Video Processor (*IVP*) and a Network-On-Chip Router (*NOCR*).

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Yield measurements for the benchmark circuits under analysis are not available and without loss of generality, it is assumed that the critical delay distribution of one of the benchmark circuits is very similar to the available yield measurements (VCDL circuits). In particular, in order to illustrate the methodology it is assumed that the measured yield curves ($Y_m$) of the VCDL circuits correspond to the *MUL* benchmark. The measured yield obtained from the regular implementation of the test circuit is used as reference for the implemented Multiplier following the F1D layout design style and the measured yield from the non-regular implementation as reference for the F2D. Moreover, another layout configuration is implemented, the NP1D, which based on the observations made from the layouts, it should take yield values in between the regular and the non-regular implementations and thus the *Average* yield curve is used as reference. The yield for the other circuits is subsequently computed using the calibrated model derived from this adjustment.

As previously explained, the value of the $PVI_{min}$ parameter captures the minimum tolerable distortion that does not degrade the parametric yield. This parameter is related to the set of minimum patterns necessary to construct a layout design. The minimum set of patterns corresponds to the set of regular pattern constructs which includes edges, line-ends and enclosures (classes 1, 3, 14, 17 and 19 detailed in Table 1). These patterns are practically perfectly printed in this technology and it is assumed, without loss of generality, that a small distortion on the printed patterns does not cause parametric yield losses. Based on this consideration, the $PVI_{min}$ is computed as the maximum *PVI* value of the regular set of patterns. According to the lithography simulations performed to analyze the pattern constructs in this technology, the value of the $PVI_{min}$ parameter for all the layers, that is, the maximum tolerable distortion that gives perfect yield, is 0.02. Note that any other pattern construct has a *PVI* score that is equal or larger than this $PVI_{min}$.

The scaling parameter *S* must be adjusted for each design margin and for each layout design

style. To do so, it is considered a scenario where all hotspots ($N_h$) of the Multiplier have the same reference *PVI* number ($PVI_{ref}$), computed as the average *PVI* for the $N_h$ hotspots in the Multiplier for each design style. Thereby, the scaling parameter *S* for each layout design style (*DS*) and each design margin (*DM*) using Eq. 3 and 6 is computed as follows:

$$S(DM, DS) = -\frac{ln(Y_m(DM, DS))}{N_h(DS)} \cdot \frac{1 - PVI_{ref}(DS)}{PVI_{ref}(DS) - PVI_{min}} \tag{11}$$

The parameter *S* serves to model the lambda factor which relates the *PVI* index into a degradation score (lambda) that will give a reasonable estimation of parametric yield loss. In other words, it adjusts the yield model with respect to real yield measurements. Therefore, this adjustment calibrates the lambda equation to give yield values in consonance with other layout designs with similar pattern configurations that have been experimentally tested in silicon.
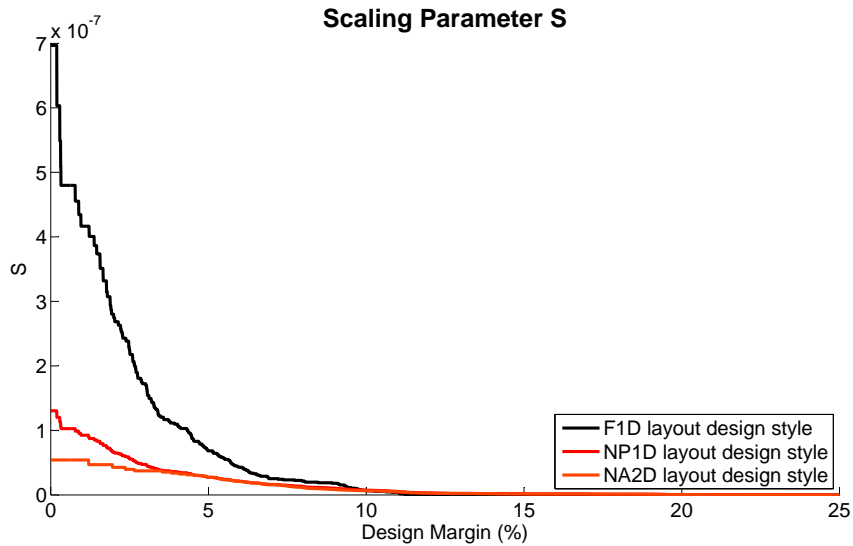


**Fig 15** Scaling parameter *S* for the different layout design styles.

Figure 15 shows the different values of the *S* parameter for the different design margins and layout design styles. Observe that as the design margin increases, the *S* factor of the different layout

styles presents more similar values reflecting the same trend in the yield curves of Figure 14.

The value of *S* obtained from the calibration process using the *MUL* circuit is applied to the model in Equation 6 for the *IVP* and *NOCR* circuits following again the three layout implementations, F1D, H1D and F2D. As it can be observed in Figure 16, the obtained yield for the *IVP* benchmark is slightly below that of the *MUL* benchmark, while the yield of the *NOCR* is above that of the *MUL* benchmark. This differences in yield values obtained with these two circuits compared to the *MUL* reference are mainly caused by the different number of hotspots occurring in each circuit (the number of hotspots in each circuit is shown in Table 2). This difference is even larger for the *NOCR* circuit, specially for the F1D design, since this circuit contains approximately half of the number of hotspots of the reference multiplier.

In order to analyze if these differences are in agreement with the model, a scaled yield curve for these circuits can be computed taking into account the different characteristics of the *IVP* and *NOCR* circuits with respect to the *MUL* circuit. Assuming that for the same layout styles there is the same average *PVI* ($PVI_{ref}$) for any circuit and correspondingly an average $\lambda_{ref}$, it is easy to scale any yield curve $Y_{m_0}$ by knowing the relation between the number of hotspots of each circuit, based on Eq. 3.

$$Y_{m_i}(DM,DS) \cong e^{-\lambda_{ref} \cdot N_{hi}} = Y_{m_0}(DM,DS)^{\frac{N_{hi}}{N_{h0}}} \tag{12}$$

Figure 17 shows that the scaled measured curves (*estimated reference* in the legend) are in good agreement with the points calculated using the *S* parameter and the summation of all hotspots with corresponding *PVI*.
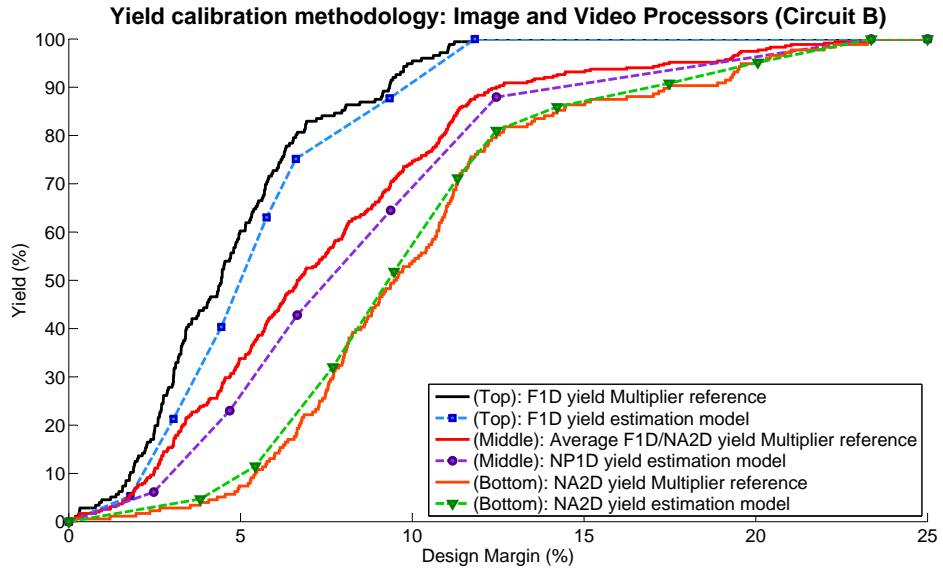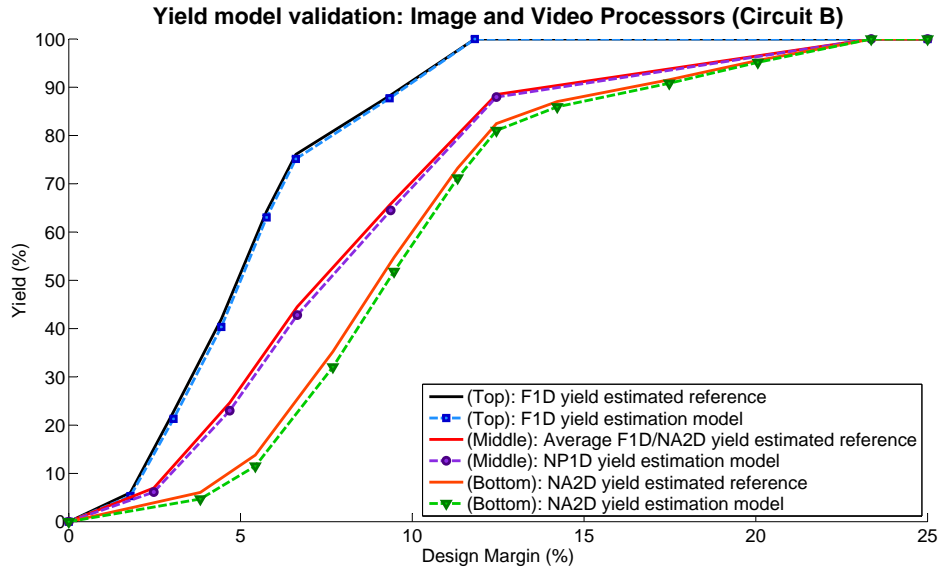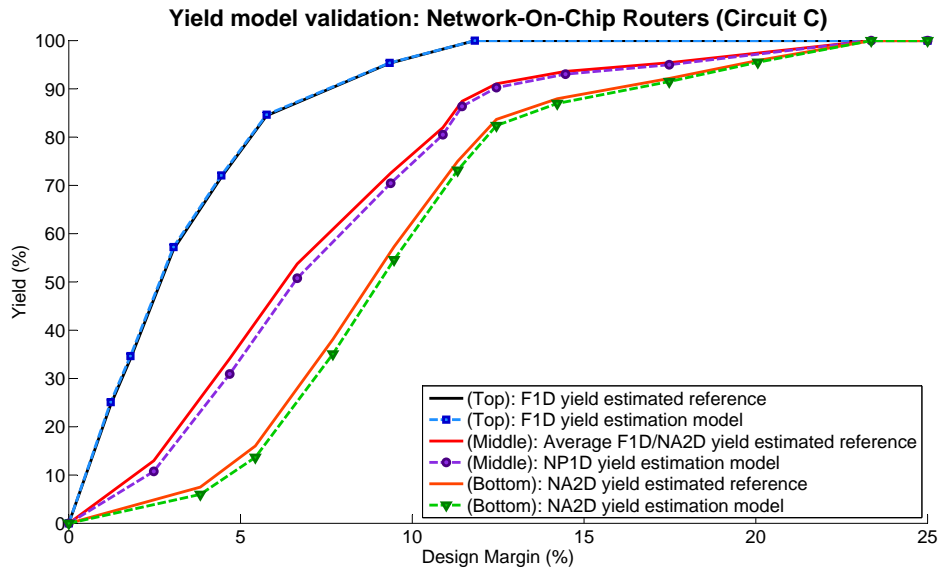
(a) Image and Video Processors (Circuit B)
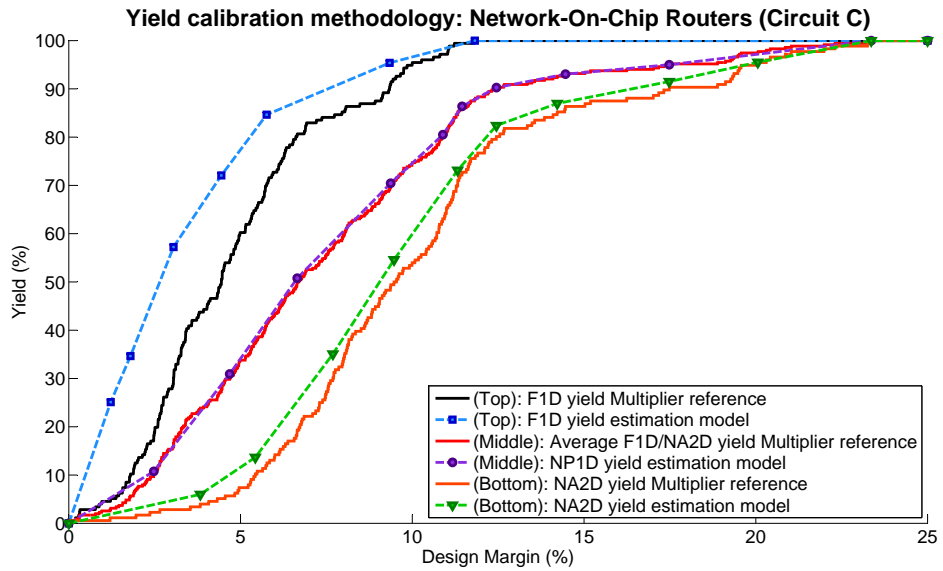


(b) Network-On-Chip Routers (Circuit C)

**Fig 16** Yield estimation using the calibration methodology for different design margins and layout design styles.

(a) Image and Video Processors (Circuit B)



(b) Network-On-Chip Routers (Circuit C)

**Fig 17** Yield model validation using the yield estimated reference for different design margins.

*5.3  Layout evaluation using the proposed parametric yield model*

In this section, the parametric yield model previously calibrated is applied to the three benchmark circuits under analysis for a specific design margin of 11%. These circuits are composed by thousands of instances of the same circuit so that the F2D implementation gives an area of 1 cm$^2$. Note that several instances of the same circuit must be jointly considered since the small area of one single circuit would suffer a parametric yield loss practically negligible. The number of Good Dies Per Wafer (*GPDW*) for a wafer of radius 150 mm is computed in order to better capture the trade-off between area penalty and yield degradation. Also, in order to differentiate the degree of layout regularity employed in each design, a Regularity Metric (*RM*) is computed as the ratio between the number of simple regular patterns constructs (classes 1, 3, 14, 17 and 19 detailed in Table 1) and the number of all the pattern constructs used in the layout.

Observe from Table 2 that the results clearly show that the three circuits implementations following the F1D layout design style, in agreement with Figure 16, present a better yield than styles with more complex layout patterns (H1D, F2D), but at the cost of extra area. Considering the *GDPW* metric, the H1D designs give the highest number of *GPDW* and thus provide the best area/yield ratio. This advantage in *GDPW* is in turn at the cost of using a larger number of complex pattern constructs compared to the most regular design style, the F1D, as the *RM* index indicates.

The yield of these circuits as observed in Table 2 is rather similar across the benchmarks and mostly dependent on the layout design style. Hence, the yield model presented in this work is mostly a means to take informed decisions on what is the most suitable library to use in order to increase the *GDPW* of the circuits. Also note that the numeric results of yield directly depend on the design margin specified for the design and thus they are particular for that case. However, the

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**Table 2** Lithography evaluation metrics. Area, number of pattern constructs ($N_{PC}$), number of hotspots ($N_h$), PVI mean, regularity index (*RM*), yield estimation and Good Dies Per Wafer (*GDPW*).

| Circuit | Multipliers (A) | | | Image and video processors (B) | | | Network-On-Chip routers (C) | | |
|---|---|---|---|---|---|---|---|---|---|
| **Instances** | 2500 | | | 3900 | | | 6950 | | |
| **Layout** | F1D | H1D | F2D | F1D | H1D | F2D | F1D | H1D | F2D |
| **Area (cm$^2$)** | 1.69 | 1 | 1 | 1.56 | 1 | 1 | 1.36 | 1 | 1 |
| **N$_{PC}$ x10$^6$** | 4127 | 2577 | 2363 | 3954 | 2764 | 2427 | 3085 | 2313 | 1974 |
| **N$_h$ x10$^6$** | 142 | 759 | 763 | 175 | 886 | 663 | 67 | 680 | 613 |
| **PVI$_{mean}$** | 0.069 | 0.073 | 0.129 | 0.069 | 0.069 | 0.136 | 0.065 | 0.071 | 0.135 |
| **PVI$_{std}$** | 0.047 | 0.050 | 0.041 | 0.046 | 0.046 | 0.037 | 0.046 | 0.046 | 0.043 |
| **RM (%)** | 94.41 | 74.56 | 69.02 | 92.83 | 72.75 | 73.70 | 96.33 | 75.49 | 70.99 |
| **Yield (%)** | 97.02 | 78.72 | 64.74 | 96.36 | 77.55 | 66.80 | 98.67 | 81.63 | 68.97 |
| **GDPW** | 355 | 504 | 414 | 384 | 496 | 428 | 456 | 522 | 441 |

qualitative results to decide the best library choice in terms of yield or *GDPW* remain generally valid.

The pattern construct simplification used to decrease the number of lithography simulations make the lithography evaluation for complex 2D designs (H1D, F2D) less accurate than the evaluation for regular designs (F1D). Hence, one of the advantages of regular designs is that the yield can be calculated with less effort since most of the pattern constructs are regular and the lithography simulations are done for the specific pattern construct used in these designs.

## 6 Conclusions

In this paper we presented a new layout quality metric based on a parametric yield estimation model that enables the possibility to analyze and compare different layout implementations in terms of lithography degradation. A lithography hotspot discovery algorithm was implemented in order to capture the lithography distortion of the layout with a reduced set of lithography simulations. The lithography evaluation framework can be used to compare different layout implementations and also capture those patterns that excessively degrades manufacturing yield. The yield model was

demonstrated for three different benchmark circuits and three different layout design styles.

The yield estimation model is based on the assumption that the effect of each hotspot on performance is statistical in nature. For this reason, the model requires a calibration procedure taking as a reference parametric yield measurements (e.g. delay or power) of different layout styles. The value of parameter $S$ as a function of design margin and layout style is obtained from this calibration procedure and applied to any circuit. Since the model is calibrated using either delay or power yield measurements, it is expected that the model numerical results depend on the magnitude used in the calibration. However, for the purpose of layout quality evaluation this dependence is not important. The use of the model as prediction of the actual parametric yield would need to be validated with an extensive set of measurements and should therefore be the object of future work.

The yield model tested on different benchmark circuits shows that the uni-dimensional designs evaluated in this work potentially present an enhanced parametric yield compared to traditional 2D designs at the cost of an excessive area penalty. Therefore, layouts with an intermediate degree of regularity can benefit from a certain yield enhancement and similar area compared to fully 2D styles, thus producing designs with a higher number of *GDPW*.

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    (b) **Figure 17(b)**: Network-On-Chip Routers (Circuit C)

**Authors Biographies**

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