Voltage Balancing Method for a Seven-Level Stacked Multicell Converter Using Reduced Switching Transitions

Amer M. Y. M. Ghias⁽¹⁾ Josep Pou⁽¹⁾⁽²⁾ Vassilios G. Agelidis⁽¹⁾ Mihai Ciobotaru⁽¹⁾

(1) Australian Energy Research Institute & School of Electrical Engineering and Telecommunications,
The University of New South Wales, UNSW Sydney, NSW 2052, Australia.

(2) Terrassa Industrial Electronics Group & Department of Electronic Engineering,
Technical University of Catalonia, Catalonia, Spain.

Email: amer.ghias@student.unsw.edu.au.

Abstract—This paper proposes a voltage balancing method for a seven-level stacked multicell converter (SMC) based on phase disposition pulse-width modulation (PD-PWM) using reduced switching transitions. This method is called optimal-transition voltage balancing method. The selection of the optimal transition sequence is performed by minimizing a cost function and the transitions that would result in more switchings of the converter semiconductor devices are avoided. The simulation results show a significant reduction of the average switching frequency as compared to the use of the optimal-state voltage balancing method, while maintaining the balance of the FC voltages. Moreover, the proposed PD-PWM voltage balancing method is robust to unbalanced linear loads, non-linear loads and transients.

Index Terms—Multilevel converter; Stacked multicell converter; Capacitor voltage balancing; Pulse-width modulation.

I. INTRODUCTION

In the recent years, hybrid multilevel converters have been introduced and are considered competitive solutions in highpower applications [1]. They require to store less energy than the popular multilevel topologies, i.e. the cascaded multi-modular converter [2], the modular multilevel converter (MMC) [3], the diode-clamped converter (DCC) [4], and the flying capacitor (FC) converter [5]. Hybrid multilevel converters allow for higher voltage/power ratings, lower total harmonic distortion (THD), and lower power losses, when compared with the conventional two-level converter [6], [7] and also with some of the popular multilevel topologies. Fig. 1 shows the stacked multicell converter (SMC) which is a hybrid multilevel topology. The SMC is capable of providing a higher number of voltage levels with reduced FCs than the conventional multilevel FC converter.

Like in the other multilevel topologies, this newly hybrid multilevel converter also requires capacitor voltage balancing for the acceptable performance of the converter. In [9]–[15] phase-shifted pulse width modulation (PS-PWM) was applied to the SMC, which provides natural voltage balancing. However, natural voltage balance depends on the load conditions and the dynamics slow down with different types of loads,

specially non-linear loads. Some references in [9]–[12] used a booster to achieve faster voltage balancing dynamics. This balance booster consists of a passive RLC filter and thus introduces some power losses and makes the overall converter large.

There are a few active voltage balancing methods found in the technical literature [16]-[18]. In [16], a direct torque control method was proposed. This method regulates the FC voltage; however, no line-to-line voltage is shown and analyzed in the paper. Another method was proposed in [17] which uses a sliding mode observer. This method performs very well and does not require any voltage sensors. However, the method itself is complicated and requires a lot of computations. Finally, an active voltage balancing method was proposed in [16] for hybrid converters such as the active neutral-pointclamped (ANPC) converter and the SMC. The method requires evaluation of a cost function for the selection of the redundant states using space vector modulation (SVM) in a four-level SMC. The authors suggested increasing the number of voltage levels to extend the operating range of the converter, which is apparently not an optimal solution.

The solutions discussed above do not analyze the effect of the voltage balancing process on the switching frequencies in the power devices of the SMC. This paper presents a capacitor voltage balancing method that uses reduced switching transitions. Phase-disposition pulse-width modulation (PD-PWM) is applied and voltage balance is performed by a proper selection of the switching transitions by using a cost function. The switching frequencies of the power devices are compared to the optimal-state voltage balancing (OSVB) method [19], which is based on optimizing the switching states independently and it does not avoid the non-optimal switching transitions. The modulation method proposed in this paper selects the minimum transitions between consecutive states. It is therefore called optimal-transition voltage balancing (OTVB) method. The analysis shows that by using the OTVB method, a significant reduction in the switching frequencies can be achieved as compared to OSVB. The voltage ripples in the FCs are also

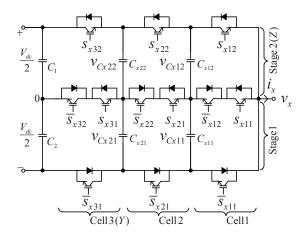


Fig. 1. Circuit diagram of a 3×2 SMC.

analyzed for the two voltage balancing methods.

The rest of the paper is organized as follows. Section II describes the operating principle of a seven-level SMC and the OSVB method. Section III introduces the OTVB method for reducing the switching frequencies in the power devices. Section IV presents selected simulation results to verify the effectiveness of the proposed voltage balancing method on a seven-level SMC. Also, switching frequencies on the power devices and capacitor voltage ripples are compared with those produced by the OSVB method. Finally, the conclusions are summarized in Section V.

II. OPERATING PRINCIPLE OF THE SMC CONVERTER

Fig. 1 shows a circuit diagram of a phase-leg of a sevenlevel SMC. It consists of three cells (Y = 3) of FC converter, which are integrated to form two stages/stacks (Z = 2). It is a 3x2 SMC topology. The converter comprises four FCs, the upper FCs C_{x12} and C_{x22} , are in the Stage 2, while the lower FCs C_{x11} , C_{x21} are in the Stage 1, where the subscript x is used for phase identification $x=\{a,b,c\}$. The dc bus consists of two capacitors C_1 and C_2 , each of them is regulated to operate at a half of the dc-link voltage $(V_{dc}/2)$. During normal operation, the mean voltage of the FCs C_{x11} and C_{x12} has to be maintained at $V_{dc}/6$, whereas it has to be maintained at $V_{dc}/3$ for the FCs C_{x21} and C_{x22} . The output voltage v_{x0} consists of seven $(3 \times 2 + 1)$ voltage levels, i.e. 0, $V_{dc}/6, V_{dc}/3, V_{dc}/2, 2V_{dc}/3, 5V_{dc}/6, V_{dc}$. The switch control function is defined as s_{xyz} , where y denotes the switch number corresponding to a particular cell in the phase-leg x of the SMC converter $y = \{1, ..., Y\}$ (Y = 3), and z defines the Stage $z = \{1, ..., Z\}$ (Z = 2). The switch control functions can take two values $s_{xyz} = \{0, 1\}$, meaning "0" and "1" that the switch is off and on, respectively. The switch pairs in each phase leg $(s_{x\,yz}$ and $\overline{s}_{x\,yz})$ operate in a complementary manner.

The OSVB method is based on minimizing a cost function for the Stage z, which is given as follows [18]–[20]:

$$J_{xsz} = \frac{1}{2} \sum_{i=1}^{Y-1} C_{xjz} (v_{Cxjz} - V_{Cxjz}^*)^2,$$
 (1)

where x identifies the phase, and s is the switching state $s=\{0,..,7\}$ of stage z. For example, $J_{a1\,2}$ is the cost function calculated for phase a (x=a), at Stage 2 (z=2) and Switching State 1 (s=1), i.e. $s_{a32}=0$, $s_{a22}=0$, and $s_{a12}=1$. j is the index used for the identification of each FC $j=\{1,2\}$, being C_{xjz} a particular FC and V_{Cxjz}^* its reference voltage.

The cost function in (1) is positively defined and it becomes zero if all the FC voltages are at the reference values. Therefore, the cost function in (1) should be minimized. The minimization process can be performed using a differentiating method, which is given as:

$$\frac{d}{dt}J_{xsz} = \frac{d}{dt}\frac{1}{2}\sum_{j=1}^{Y-1} C_{xjz}(v_{Cxjz} - V_{Cxjz}^*)^2$$

$$= \sum_{j=1}^{Y-1} (\Delta v_{Cxjz}i_{Cxjz}) \le 0,$$
(2)

where Δv_{Cxjz} is the voltage deviation of a FC $(\Delta v_{Cxjz} = v_{Cxjz} - V_{Cxjz}^*)$, and i_{Cxjz} is the current in each FC, which depends on the selected redundant switching state and load current, as shown in Table I. When the modulator defines two particular voltage levels for the following switching period at Stage z, the cost function is evaluated for all redundant switching states available for those levels. Based on the calculated values, the switching states that provide the minimum value to the cost function are the ones selected and are used for the gating signals.

It should be noted that the optimal switching states between two consecutive voltage levels are selected independently one from another. The OSVB method does not avoid the non-optimal transitions, i.e. those transitions that produce more switching events, thus resulting in higher switching frequencies for the power devices. The OTVB proposed in this paper overcomes this problem because it avoids the use of non-optimal transitions.

III. PROPOSED VOLTAGE BALANCING METHOD

The switching transitions between consecutive voltage levels of all the possible combinations of switching states from $000\{0\}$ to $111\{7\}$ are shown in Fig. 2. The transitions between two switching states shown by solid lines are called optimum transitions, as those transitions involve changing only one bit. Therefore, they produce the minimum number of switching events. On the other hand, the transitions represented by dashed lines are non-optimal, as more than one bit changes in the transition between consecutive levels. For example, a minimum transition is produced when switching between the States $001\{1\}$ and $101\{5\}$ (see Fig. 2), while the transition between the States $001\{1\}$ and $110\{6\}$ is a non-optimal one. Hence, if the non-optimal transitions are chosen, the switching frequencies of the power devices increase. Additional switching events can be produced due to the transitions within the same voltage level. Nevertheless, those transitions can be avoided by using sawtooth carriers [20].

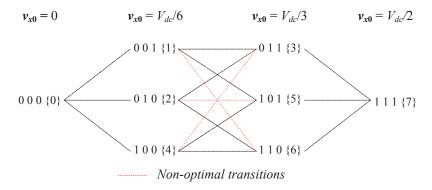


Fig. 2. Switching transitions between consecutive voltage levels of the Stage z.

TABLE I 3×2 SMC Converter: Voltage Levels, Switching States, FC CURRENTS, AND EFFECTS ON THE FC VOLTAGES

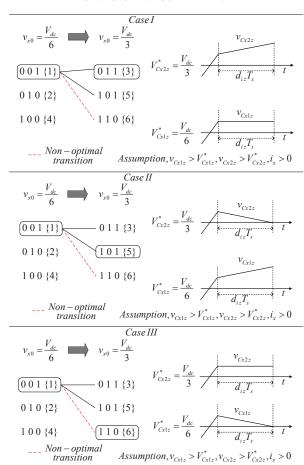
Output Voltage		Switching States				FC Currents		FC voltages	
Level (v_{x0})		s_{x3z}	s_{x2z}	s_{x1z}	st.#	i_{Cx2z}	i_{Cx1z}	v_{Cx2z}	v_{Cx1z}
4	$\frac{V_{dc}}{2}$	1	1	1	{7}	0	0	х	X
3	$\frac{V_{dc}}{3}$	1	1	0	{6}	0	i_x	X	↑
		1	0	1	{5}	i_x	$-i_x$	↑	↓
		0	1	1	{3}	$-i_x$	0	+	X
2	$\frac{V_{dc}}{6}$	1	0	0	{4}	i_x	0	↑	X
		0	1	0	{2}	$-i_x$	i_x	↓	↑
		0	0	1	{1}	0	$-i_x$	X	\downarrow
1	0	0	0	0	{0}	0	0	X	X
No	te: The cl	nargin	g/discl	nargin	g effec	ts in th	e FC ar	e given	
assuming that i_x is positive $(i_x > 0)$ with the following									
	notatio	on.							

notation:

- ↑ Capacitor voltage increases
- ↓ Capacitor voltage decreases
- x No change in the capacitor voltage

Moreover, the switching frequencies of the power devices can be further reduced by avoiding the non-optimal transitions between consecutive levels. However, avoiding the nonoptimal transitions will worsen the FC voltage balance. This effect is shown in the example in Table II, where three cases are given. In the Case I, the converter is switching from State 001{1} to State 011{3}, and in Case II the switching is from State 001{1} to State 101{5}. Both Cases I & II are optimal transitions, however none of the final states provide optimum voltage balance, since the voltage in one of the FCs increases and tends to go far beyond the reference value (capacitors C_{x2z} and C_{x1z} in the Cases I and II, respectively). On the other hand, in the Case III the switching transition is from State $001\{1\}$ to State $110\{6\}$, which is a non-optimal one. However, the State $110\{6\}$ is the best from the point of view of voltage balancing, since none of the voltages in the FCs deviates further from the reference values. Therefore, if this state is

TABLE II CASE STUDY OF OSVB METHOD



avoided because it produces additional switching transitions, and either of the two states in Case I or II are chosen, the voltage balancing will be less effective. This can be partially compensated by using a modulation method that chooses the optimal sequence considering the two states simultaneously, and not only the optimal states separately. As a result, the FC voltage balance will improve.

The cost function in [18], [20] is modified to select the

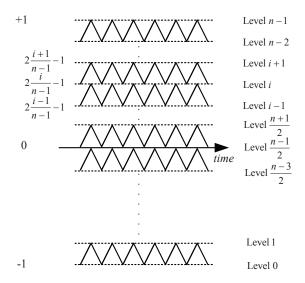


Fig. 3. Carriers in PD-PWM.

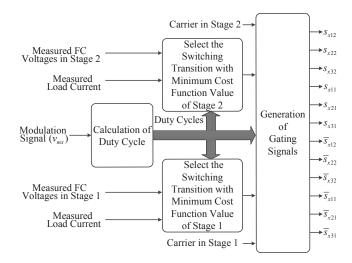


Fig. 4. Block diagram of the proposed OTVB method.

switching transitions between two states of different voltage levels and is given as:

$$J_{xi\,z-i+1\,z} = J_{x,i\,z}d_{i\,z} + J_{x,i+1\,z}d_{i+1\,z},\tag{3}$$

where x identifies the phase $(x=\{a,b,c\})$, i is the first state, i+1 is the second state, $d_{i\,z}$ [0,1] is the duty cycle of the first state of the Stage z, and $d_{i+1\,z}$ [0,1] is the duty cycle of the second state of the Stage z. As shown in Fig. 3, the duty cycle of an output voltage level of the Stage z using PD-PWM can be obtained as follows:

for
$$2\frac{i}{n-1} - 1 \le v_{mx} \le 2\frac{i+1}{n-1} - 1:$$

$$d_{iz} = (i+1) - (n-1)\frac{v_{mx} + 1}{2},$$
(4)

and for
$$2\frac{i-1}{n-1} - 1 \le v_{mx} \le 2\frac{i}{n-1} - 1:$$

$$d_{iz} = (n-1)\frac{v_{mx} + 1}{2} - (i-1),$$
(5)

where n is the number of level and v_{mx} is the modulation signal that ranges in the interval [-1,1] under linear operation mode. When v_{mx} is positive z=2, otherwise, z=1. The cost function of the transitions between two different voltage levels is positively defined, and if all the FC voltages are regulated at their reference value, it becomes zero. Hence, in order to achieve voltage balance, this cost function needs to be minimized at any switching period using differentiation. Thus, differentiating (3), the following expression is obtained:

$$\frac{d}{dt} j_{xi z-i+1 z} = \sum_{j=1}^{Y-1} \Delta v_{Cxjz} (i_{Cxjz,i} d_{iz} + i_{Cxjz,i+1} d_{i+1 z}) \le 0,$$
(6)

where $i_{Cxjz,i}$ and $i_{Cxjz,i+1}$ are the capacitor currents of the corresponding states of the Stage z. They depend on the load currents and the redundant switching states, as shown in Table I. Δv_{Cxjz} are the voltage deviations of the FCs $(\Delta v_{Cxjz} = v_{Cxjz} - V_{Cxjz}^*)$.

When the modulator defines two particular voltage levels for the following switching period at the Stage z, the cost function is evaluated for all the redundant optimum switching transitions available for those levels. Based on the calculated values, the switching transition that provides the minimum value to the cost function is selected. In order to avoid additional switching events, all the non-optimal transitions are disregarded in the selection process. Once the optimal switching transition is selected, the two consecutive switching states are determined, which define the gating signals of the SMC. Fig. 4, shows a block diagram for the implementation of the proposed voltage balance method.

IV. PERFORMANCE EVALUATION

In this section, the proposed voltage balancing method is applied to a seven-level SMC in MATLAB/Simulink [21] using PLECS Blockset [22]. In the simulations, the dc voltage is $V_{dc}=100V$ and a linear RL Y-connected load ($R=44\Omega, L=6 \mathrm{mH}$) is connected to the converter output. The value of the FCs is $C=400 \mathrm{\mu F}$. The fundamental and the carrier frequencies are $f=50\mathrm{Hz}$ and $f_s=2\mathrm{kHz}$ respectively. The converter is tested with unbalanced load, non-linear load and under transients.

The dynamic behavior of the proposed voltage balancing method is shown in Fig. 5. In this test, an unbalanced condition is introduced in the linear RL load ($R_a=8.8\Omega,R_b=79.2\Omega,R_c=44\Omega$). The line-to-line voltage v_{ab} and the capacitor voltages ($v_{Ca\,11},v_{Cb\,12},v_{Cb\,21}$, and $v_{Cb\,22}$) are shown in Fig. 5(a). In the simulation, the initial capacitor voltages were $V_{Ca\,11}=4$ V, $V_{Ca\,12}=22$ V, $V_{Cb\,21}=26$ V, $V_{Cb\,22}=50$ V and regulated to the desired voltages, i.e. 16.67 V, 16.67 V, 33.33 V, and 33.33V respectively. One can observe that the capacitor voltages reach their nominal values in about 20 ms. Once in the steady-state condition, the modulation index m

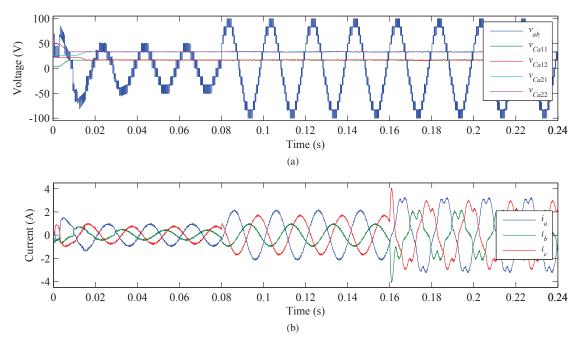


Fig. 5. The SMC is operated using the proposed OTVB method under unbalanced linear load. A step change in the modulation index from m=0.4 to m=0.9 occurs at 80ms and at 160ms a non-linear load is added: (a) line-to-line voltage (v_{ab}) and FC voltages $(v_{Ca11}, v_{Ca12}, v_{Ca21}, \text{and } v_{Ca22})$ (b) output currents $(i_a, i_b, \text{and } i_c)$.

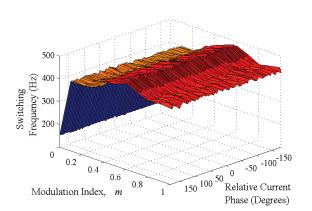
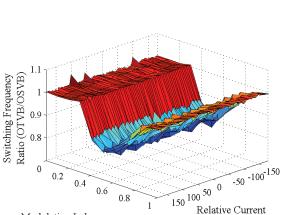


Fig. 6. Switching frequency of the power devices using the OTVB method.



Phase (degrees)

Fig. 7. Switching frequency ratio (OTVB/OSVB) of the power devices.

Modulation Index, m

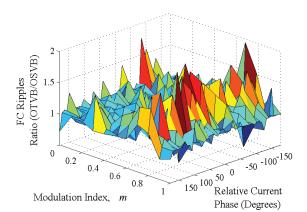


Fig. 8. FC voltage ripples ratio OTVB/OSVB.

changes from 0.4 to 0.9. at 80 ms, and later at 160 ms a non-linear load consisting of a three-phase diode rectifier with a dc-side load made of a capacitor and a resistor of $30\mu F$ and 88Ω , respectively, is added. It should be noted that during these transients the capacitor voltages of the SMC are not affected. Hence, the proposed voltage balance method proves to be robust not only under steady-state operating conditions with unbalanced and non-linear load but also under transients.

Fig. 6 shows the average switching frequency of the power devices using the OTVB method. All possible relative current phase angles and modulation indices have been considered. In order to achieve the maximum amplitudes of the output voltage fundamentals under linear mode, a zero sequence has been added to the modulation signals of the converter. The zero sequence is given by $-(v_{mx\,max}+v_{mx\,min})/2$, where $v_{mx\,max}$

and $v_{mx\,min}$ are the maximum and minimum values of the modulation signals of the converter, respectively. As it can be noticed in Fig. 6, the output current phase angle does not significantly affect the switching frequency.

Fig. 7 shows the switching frequency ratio of both voltage balancing strategies, i.e. OTVB over OSVB, for all modulation indices and load power factors. It can be remarked that with the OTVB method there is a reduction of the switching frequency of about 5% on average for high modulation indices. Such a reduction in the switching frequency is significantly larger for low modulation indices.

Fig. 8 shows the FC voltage ripples ratio OTVB over OSVB. It can be noted that with the OTVB method there is an increase in the voltage ripples of about 50% on average for high modulation indices. Such an increase in the voltage ripples becomes smaller for low modulation indices.

In summary, using the OTVB method a reduction of about 5% of the switching frequencies in the power devices for high modulation indices can be achieved at the expense of increasing the FC voltage ripples.

V. CONCLUSION

This paper has presented a voltage balancing method for a seven-level SMC using a reduced switching transition. This method is based on calculating a cost function considering the FC voltage deviations and the output currents. The proposed cost function evaluates minimum switching transitions, i.e. the two consecutive states between consecutive voltage levels. Only the minimum switching transitions are evaluated and the one that gives the lower value to the cost function is selected. The proposed method has been implemented in a seven-level SMC and tested against unbalanced loads, nonlinear loads and transients. It performs very well in regulating the FC voltages to the desired levels. The results have been compared with a modulation method that does not avoid nonoptimal transitions and optimizes switching states instead of transitions, i.e. OSVB. Simulation results have been presented that show that for high modulation indices, the average switching frequencies of the devices are reduced by about 5% when using the proposed OTVB method. This reduction comes at the cost of increasing the FC voltage ripples. Hence, there is a tradeoff between switching frequency reduction and increased FC voltage ripples.

ACKNOWLEDGMENT

This work has been supported by the University of New South Wales, Australia Energy Research Institute and the School of Electrical engineering and Telecommunications.

It has also been supported by the Ministerio de Economia y Competitividad of Spain under project ENE2012-36871-C02-01.

REFERENCES

 T. A. Meynard, H. Foch, F. Forest, C. Turpin, F. Richardeau, L. Delmas, G. Gateau, and E. Lefeuvre, "Multicell converters: derived topologies," *IEEE Trans. Ind. Electron.*, vol. 49, no. 5, pp. 978-987, Oct 2002.

- [2] F. Z. Peng, J. S. Lai, J. W. McKeever, and J. VanCoevering, "A multilevel voltage-source inverter with separate dc sources for static VAr generation," *IEEE Trans. Ind. Appl.*, vol. 32, no. 5, pp. 1130-1138, Sep./Oct. 1996
- [3] A. Lesnicar and R. Marquardt, "An innovative modular multilevel converter topology suitable for a wide power range," in *Proc. IEEE Power Tech Conference*, 23-26 June 2003, vol. 3, pp. 6.
- [4] A. Nabae, I. Takahashi, and H. Akagi, "A new neutral-point-clamped PWM inverter," *IEEE Trans. Ind. Appl.*, vol. IA-17, no. 5, pp. 518-523, Sep./Oct. 1981.
- [5] T. A. Meynard and H. Foch, "Multi-level conversion: High voltage choppers and voltage-source inverters," in *Proc. 23rd Annual IEEE Power Electronics Specialists Conference (PESC)*, 29 Jun-3 Jul 1992, vol. 1, pp. 397-403
- [6] J. S. Lai and F. Z. Peng, "Multilevel converters A new breed of power converters," *IEEE Trans. Ind. Appl.*, vol. 32, no. 3, pp. 509-517, May/Jun. 1996.
- [7] S. Kouro, M. Malinowski, K. Gopakumar, J. Pou, L. G. Franquelo, B. Wu, J. Rodriguez, M. A. Perez, and J. I. Leon, "Recent advances and industrial applications of multilevel converters," *IEEE Trans. Ind. Electron.*, vol. 57, no. 8, pp. 2553-2580, Aug. 2010.
- [8] G. Gateau, T. A. Meynard, and H. Foch, "Stacked multicell converter (SMC): properties and design," in Proc. 32nd Annual IEEE Power Electronics Specialists Conference (PESC), 2001, vol. 3, pp. 1583-1588.
- [9] L. Delmas, G. Gateau, T. A. Meynard, and H. Foch, "Stacked multicell converter (SMC): control and natural balancing," in *Proc. 33rd Annual IEEE Power Electronics Specialists Conference (PESC)*, 2002, vol. 2, pp. 689-694
- [10] B. P. McGrath, T. Meynard, G. Gateau, and D. G. Holmes, "Optimal modulation of flying capacitor and stacked multicell converters using a state machine decoder," *IEEE Trans. Power Electron.*, vol.22, no.2, pp. 508-516, March 2007.
- [11] A. K. Sadigh, S. H. Hosseini, M. Sabahi, and G. B. Gharehpetian, "Double flying capacitor multicell converter based on modified phase-shifted pulsewidth modulation," *IEEE Trans. Power Electron.*, vol. 25, no. 6, pp. 1517-1526, June 2010.
- [12] S. H. Hosseini and M. Sadeghi, "Reduced stacked multicell converter with minimized stored energy of flying capacitors," in *Proc. 2nd IEEE PES International Conference and Exhibition on Innovative Smart Grid Technologies (ISGT Europe)*, 5-7 Dec. 2011, pp. 1-5.
- [13] J. Aguillon-Garcia, J. M. Fernandez-Nava, and P. Bauelos-Sanchez, "Unbalanced voltage effects on a single phase multilevel inverter due to control strategies," in *Proc. IEEE 26th Annual International Telecom*munications Energy Conference, 19-23 Sept. 2004, pp. 140-145.
- [14] J. M. F. Nava and P. B. Sanchez, "Stacked multicell converter controlled by DSP," in *Proc. IEEE International Conference on Electronics, Communications and Computers*, 16-18 Feb. 2004, pp. 69-74.
 [15] M. Ben Smida and F. Ben Ammar, "Modeling and DBC-PSC-PWM
- [15] M. Ben Smida and F. Ben Ammar, "Modeling and DBC-PSC-PWM control of a three-phase flying-capacitor stacked multilevel voltage source inverter," *IEEE Trans. Ind. Electron.*, vol. 57, no. 7, pp. 2231-2239, July 2010
- [16] A. Bennani, T. Meynard, and G. Gateau, "Direct torque control for stacked multicell (SMC) VSI fed induction machine," in *Proc. European Conference on Power Electronics and Applications (EPE)*, 2005, pp. 1-10.
- [17] A. M. Lienhardt, G. Gateau, and T. A. Meynard, "Digital sliding-mode observer implementation using FPGA," *IEEE Trans. Ind. Electron.*, vol. 54, no. 4, pp. 1865-1875, Aug. 2007.
 [18] A. Leredde and G. Gateau, "Control of the DC link capacitor voltage
- [18] A. Leredde and G. Gateau, "Control of the DC link capacitor voltage on a new four-level SMC based topology," in *Proc. IEEE International Symposium on Industrial Electronics (ISIE)*, 27-30 June 2011, pp. 1851-1856.
- [19] A. M. Y. M. Ghias, J. Pou, V. G. Agelidis, and M. Ciobotaru, "Optimum State Voltage Balancing Method for Stacked Multicell Converters," in Proc. IEEE Ind. Electron. Conference (IECON), Nov. 2013 (in press).
- [20] A. M. Y. M. Ghias, J. Pou, M. Ciobotaru, and V. G. Agelidis, "Voltage balancing strategy for a five-level flying capacitor using phase disposition PWM with sawtooth-shaped carriers," in Proc. IEEE Ind. Electron. Conference (IECON), Oct. 2012, pp.5013-5019.
- [21] Matlab/Simulink, http://www.matlab.com.
- [22] PLECS, http://www.plexim.com.