Optimum State Voltage Balancing Method for Stacked Multicell Converters

Amer M. Y. M. Ghias[1] Josep Pou[1][2] Vassilios G. Agelidis[1] Mihai Ciobotaru[1]

[1]Australian Energy Research Institute & School of Electrical Engineering and Telecommunications, The University of New South Wales, UNSW Sydney, NSW 2052, Australia.

[2]Terrassa Industrial Electronics Group & Department of Electronic Engineering, Technical University of Catalonia, Catalonia, Spain.

Email: amer.ghias@student.unsw.edu.au.

***Abstract*—This paper presents a voltage balancing method for stacked multicell converters based on phase disposition pulse-width modulation. This method is based on minimizing a cost function to determine the optimum redundant state for capacitor voltage balance for each particular voltage level. The robustness of the proposed voltage balancing method is verified against static and dynamic unbalanced load conditions. Furthermore, a significant reduction in the switching frequencies of the power devices is achieved by using sawtooth carriers instead of standard triangular carriers without affecting the voltage balancing capability.**

***Index Terms*—Multilevel converter; Stacked multicell converter; Capacitor voltage balancing; Pulse-width modulation.**

I. Introduction

Hybrid multilevel converters have been introduced in the recent years and are considered competitive solutions for medium and high power applications [1], since they require to store less energy when compared with the popular multilevel topologies, i.e. the cascaded multi-modular converter [2], the modular multilevel converter (MMC) [3], the diode-clamped converter (DCC) [4], and the flying capacitor (FC) converter [5]. The hybrid multilevel converters allow high voltage/power ratings, lower total harmonic distortion (THD), and lower power losses, when compared with the conventional two-level converter [6], [7] and also to some of the popular multilevel topologies. Fig. 1 shows the stacked multicell converter (SMC), which is one hybrid multilevel topology. The SMC is capable to provide a higher number of voltage levels with reduced FCs, when compared with the conventional FC converter.

Similar to the other multilevel topologies, this newly hybrid multilevel converter also requires capacitor voltage balancing for proper performance of the converter. In [9]–[15] phase-shifted pulse-width modulation (PS-PWM) was applied to the SMC, which provides natural voltage balance. However, natural voltage balance depends on the load conditions and the dynamics slows down with different types of loads, specially non-linear loads. In [9]–[12], a booster was used to achieve faster voltage balancing dynamics. This balance booster consists of a passive RLC filter and thus introduces some power loses, reduces converter's reliability and increases its size.

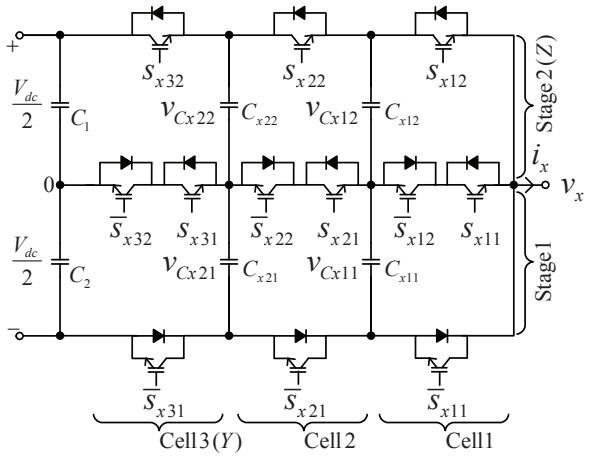


Fig. 1. Circuit diagram of a 3×2 SMC.

There are a few active voltage balancing methods found in the technical literature [16]–[18]. In [16], a direct torque control method was proposed. This method regulates the FC voltages; however, no line-to-line voltage is shown and analyzed in the paper. Another method was proposed in [17] which uses a sliding mode observer. This method performs well and it does not require any voltage sensors. However, the method itself is complicated and requires a lot of computations. Finally, an active voltage balancing method was proposed in [18] for hybrid converters such as the active neutral-point-clamped (ANPC) and the SMC. The method consists on evaluating a cost function for the selection of the redundant states using space-vector modulation (SVM) for a four-level SMC. The authors suggest increasing the number of voltage levels to extend the operating range of the converter, which is obviously not an optimal solution.

The solutions discussed above for SMCs do not report on the effects of the voltage balancing methods on the switching frequencies in the power devices. This paper presents a capacitor voltage balancing method using phase disposition pulse-width modulation (PD-PWM) and reports the switching frequency evaluation on a seven-level SMC. Voltage balance is performed by proper selection of redundant switching states by using

TABLE I
3 × 2 SMC CONVERTER: VOLTAGE LEVELS, SWITCHING STATES, FC CURRENTS, AND EFFECTS ON THE FC VOLTAGES

Output Voltage Level (v_{x0})		Switching States				FC Currents		FC voltages	
		s_{x3z}	s_{x2z}	s_{x1z}	$st.\#$	i_{Cx2z}	i_{Cx1z}	v_{Cx2z}	v_{Cx1z}
4	$\frac{V_{dc}}{2}$	1	1	1	{7}	0	0	x	x
3	$\frac{V_{dc}}{3}$	1	1	0	{6}	0	i_x	x	↑
		1	0	1	{5}	i_x	-i_x	↑	↓
		0	1	1	{3}	-i_x	0	↓	x
2	$\frac{V_{dc}}{6}$	1	0	0	{4}	i_x	0	↑	x
		0	1	0	{2}	-i_x	i_x	↓	↑
		0	0	1	{1}	0	-i_x	x	↓
1	0	0	0	0	{0}	0	0	x	x

Note: The charging/discharging effects in the FC are given assuming that i_x is positive ($i_x > 0$) with the following notation:
↑ Capacitor voltage increases
↓ Capacitor voltage decreases
x No change in the capacitor voltage

a cost function. Switching frequencies on the power devices are evaluated by comparing triangular and sawtooth carrier waveforms. Also, the FC ripples are analyzed for both types of carriers. The analysis shows that using sawtooth carriers a significant reduction in the switching frequencies can be achieved without effecting the FC voltage ripple and voltage balancing efficiency. Moreover, the quality of the line-to-line output voltage is analyzed in terms of fast Fourier transform (FFT) and total harmonic distortion (THD) for the two carrier waveforms.

The rest of the paper is organized as follows. Section II describes the operating principle of the SMC. Section III explains the proposed FC voltage balancing method. Section IV introduces the use of sawtooth carriers for the reduction of the switching frequencies in the power devices. Section V presents simulation results on a seven-level SMC to verify the effectiveness of the proposed voltage balancing method. Also some discussions on using triangular and sawtooth carriers is done by examining the average switching frequencies of the power devices, FFT and THD of the line-to-line voltages. Finally, the conclusions are summarized in Section VI.

II. OPERATING PRINCIPLE OF THE SMC CONVERTER

Fig. 1 shows a circuit diagram of a phase-leg of a seven-level SMC. It consists of three cells ($Y = 3$) of flying capacitor (FC) converter, which are integrated to form two stages/stacks ($Z = 2$). It is called 3x2 SMC. The converter comprises four FCs, the upper FCs C_{x12} and C_{x22}, are in the Stage 2, while the lower FCs C_{x11}, C_{x21} are in the Stage 1, where the subscript x is used for phase identification x=$\{a, b, c\}$. The dc bus consists of two capacitors C_1 and C_2, each of them is regulated to have a half of the dc-link voltage ($V_{dc}/2$).

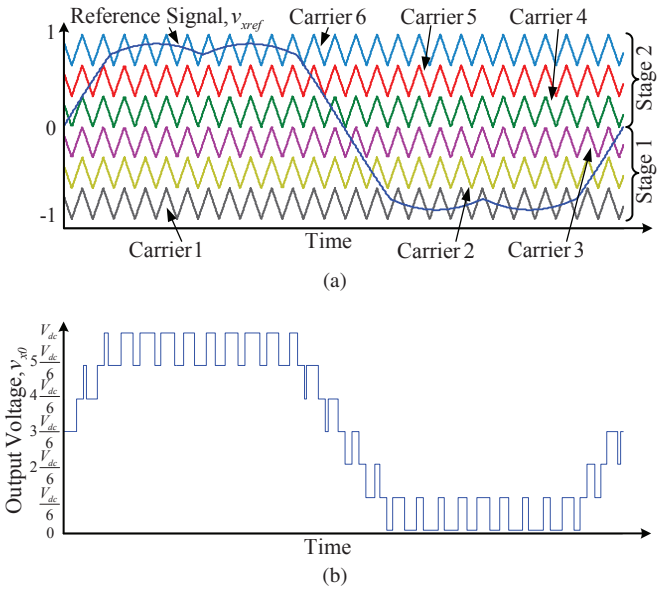


Fig. 2. PD-PWM technique for 3 × 2 SMC: (a) reference signal (v_{xref}) and carriers, and (b) output voltage (v_{x0}).

During normal operation, the mean voltage of the FCs C_{x11} and C_{x12} has to be maintained at $V_{dc}/6$, whereas it has to be maintained at $V_{dc}/3$ for the FCs C_{x21} and C_{x22}. The output voltage v_{x0} consist of seven $(3 \times 2 + 1)$ voltage levels, i.e. 0, $V_{dc}/6$, $V_{dc}/3$, $V_{dc}/2$, $2V_{dc}/3$, $5V_{dc}/6$, V_{dc}. The switch control function is defined as $s_{x\,yz}$, where y defines the switch number corresponding to a particular cell in the phase-leg x of the SMC converter $y = \{1, ..., Y\}$ $(Y = 3)$ and z defines a particular switch associated with the stage $z = \{1, ..., Z\}$ $(Z = 2)$. The switch control functions can take two values $s_{x\,yz} = \{0, 1\}$, meaning "0" and "1" that the switch is off and on, respectively. The switch pairs in each phase leg ($s_{x\,yz}$ and $\overline{s}_{x\,yz}$) operate in a complementary manner.

Fig. 2(a) shows a reference signal and the carrier signals using PD-PWM, which is applied to a 3 × 2 SMC. In this converter, PD-PWM requires six carriers. The upper three carriers in Stage 2 have the same amplitude and frequency and are arranged in a level shifted manner. The same characteristics apply to the lower three carriers in Stage 1. A sinusoidal reference signal is modified by adding a zero sequence in order to achieve maximum fundamental amplitude under linear mode (v_{xref}). The zero sequence is given by $-(v_{xref\,max} + v_{xref\,min})/2$, where $v_{xref\,max}$ and $v_{xref\,min}$ are the maximum and minimum values of the reference signals considering all phase-legs of the converter. The reference signal (v_{xref}) is compared with the triangular carriers to generate the gating signals. PD-PWM does not provide natural balancing for the capacitor voltages; nevertheless, when combined with the proposed balancing method capacitor voltage balance can be achieved.

III. VOLTAGE BALANCING METHOD

The proposed voltage balancing method is developed using PD-PWM. The PD-PWM will define the particular voltage

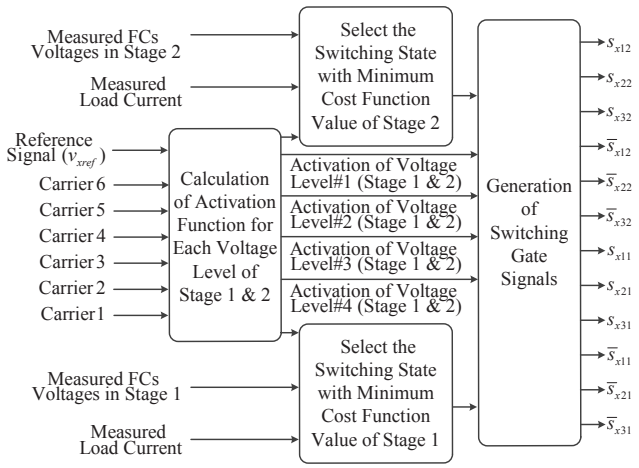


Fig. 3. Block diagram of the proposed voltage balancing method.

level that has to be provided at the output of the SMC. The optimal redundant switching state is selected for each voltage level at any switching period by evaluating a cost function to help for the capacitor voltage balance. The cost function is defined as in [18], [19]:

$$J_{xs\,z} = \frac{1}{2}\sum_{j=1}^{Y-1} C_{xjz}(v_{Cxjz} - V^*_{Cxjz})^2, \tag{1}$$

where x identifies the phase, and s is the switching state $s = \{0, .., 7\}$ of Stage z; for example, $J_{a1\,2}$ is the cost function calculated for phase a at stage 2 ($z = 2$) and switching state 1, i.e. $s_{a32} = 0$, $s_{a22} = 0$, and $s_{a12} = 1$. j is the index used for the identification of each FC $j = \{1, 2\}$, being C_{xjz} a particular FC and V^*_{Cxjz} its reference voltage.

The cost function in (1) is positively defined and it becomes zero if all the FCs voltages are at the reference values. Therefore, the cost function in (1) should be minimized. The minimization process can be performed using a differentiating method, which is given as:

$$\begin{aligned}\frac{d}{dt}J_{xs\,z} &= \frac{d}{dt}\frac{1}{2}\sum_{j=1}^{Y-1} C_{xjz}(v_{Cxjz} - V^*_{Cxjz})^2 \\ &= \sum_{j=1}^{Y-1}(\Delta v_{Cxjz} i_{Cxjz}) \leq 0,\end{aligned} \tag{2}$$

where Δv_{Cxjz} is the voltage deviation of a FC ($\Delta v_{Cxjz} = v_{Cxjz} - V^*_{Cxjz}$), and i_{Cxjz} is the current in each FC, which depends on the selected redundant switching state and load current, as shown in Table I. When the modulator defines two particular voltage levels for the following switching period at Stage z, the cost function is evaluated for all redundant switching states available for those levels. Based on the calculated values, the switching states that provide the minimum value to the cost function are the ones selected and are used for the gating signals. Fig. 3 shows the method of the proposed modulation strategy for one phase-leg of 3×2 SMC.

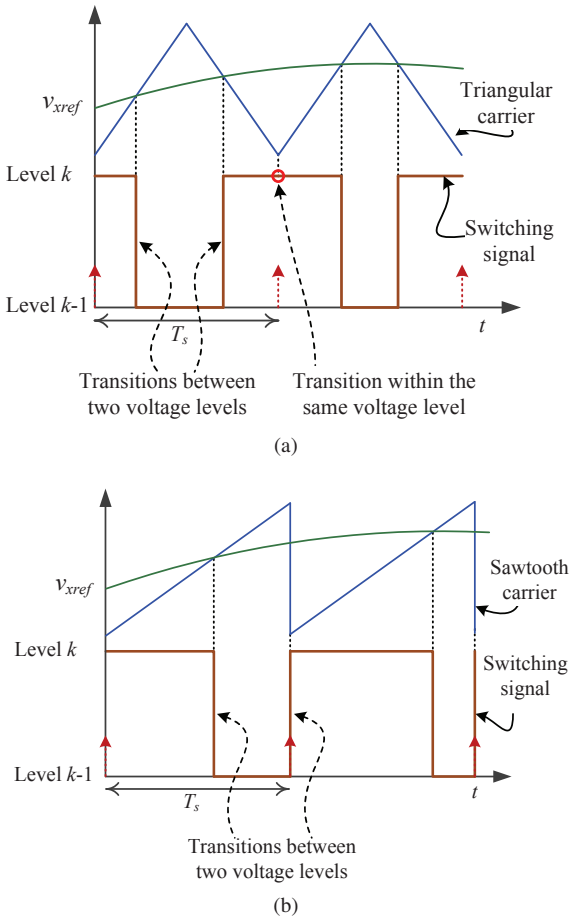


Fig. 4. Swithing frequency reduction example: (a) transitions between two consecutive voltage levels and possible transitions within the same voltage level when using triangular carrier, and (b) transitions between two voltage levels using sawtooth carriers.

IV. Reduction of The Switching Frequencies Using Sawtooth Carriers

Triangular carriers are normally used for the modulation (Fig. 2). When using these carriers, once a switching period has ended, the following one will usually start providing the same voltage level as in the previous instant (Fig. 4(a)). Since the evaluation of the cost function is performed during the previous switching period and the new switching state is applied at the sampling instant, the selected switching state may change within the same level because of voltage balancing requirements. This fact leads to additional switching events in the power devices. This can be avoided by changing the shape of the carriers [19].

Fig. 4(b) shows the case of using sawtooth-shaped carriers for the modulation. As it can be noted, no transition within the same voltage level can happen when changing from one switching period to the next one. On the contrary, the transitions are between consecutive levels. Hence, a significant amount of switching transitions can be avoided by using sawtooth carriers.

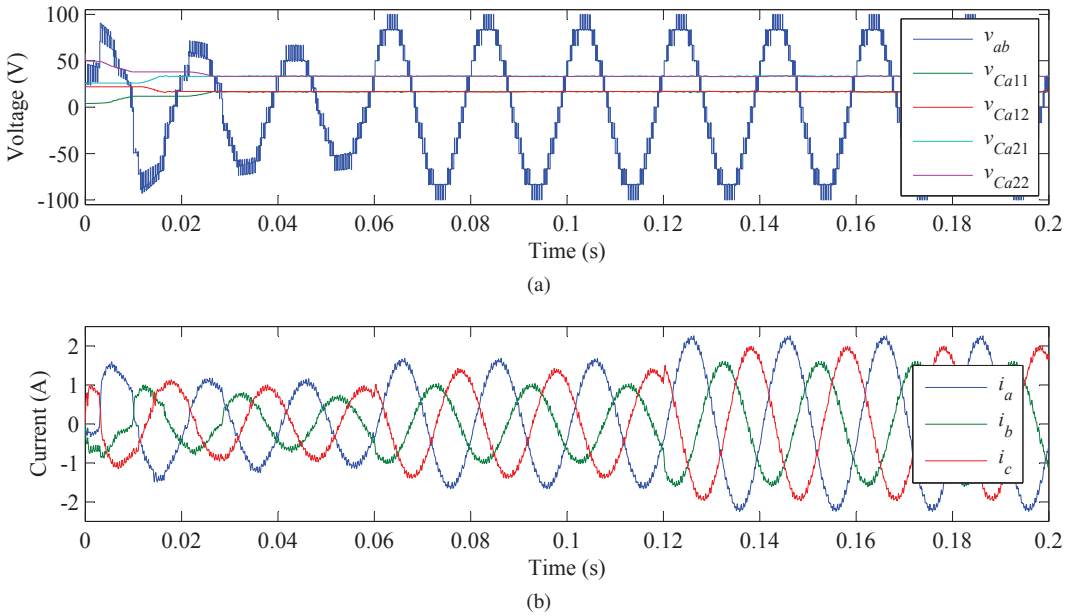


Fig. 5. The SMC under unbalanced linear load. A step change in the modulation index from $m = 0.6$ to $m = 0.9$ occurs at 60ms and at 120ms a linear load is added: (a) line-to-line voltage (v_{ab}) and FC voltages ($v_{Ca11}, v_{Ca12}, v_{Ca21}$, and v_{Ca22}), and (b) output currents (i_a, i_b, and i_c).

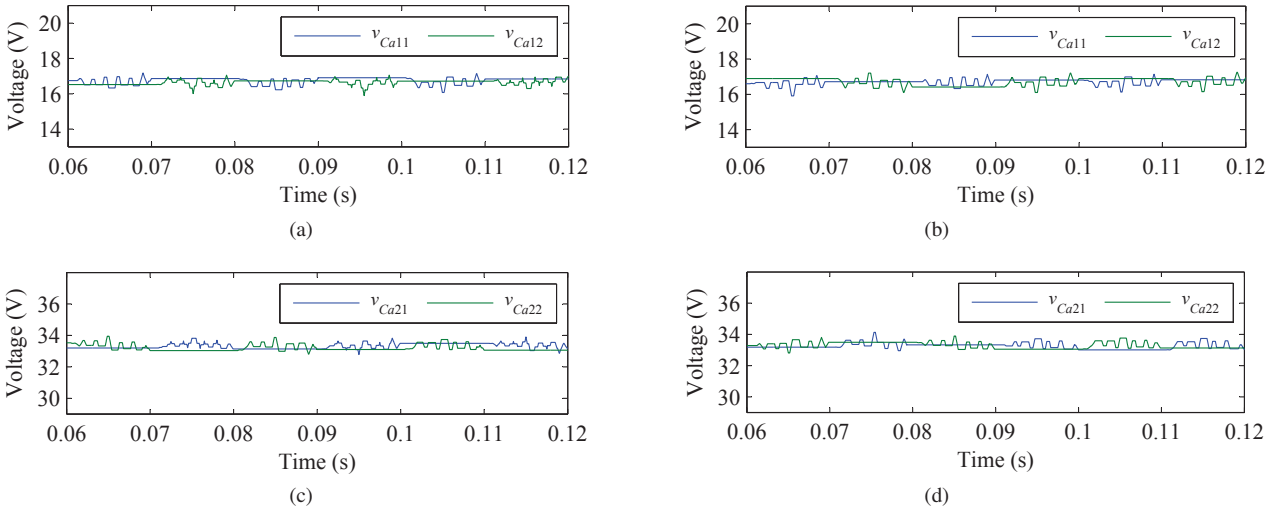


Fig. 6. Capacitor voltages of the SMC operating under unbalanced linear load: v_{Ca11} and v_{Ca12} using (a) triangular carriers, and (b) sawtooth carriers, v_{Ca21} and v_{Ca22} using (c) triangular carriers, and (d) sawtooth carriers.

V. Performance Evaluation

Simulation tests are performed on three-phase 3×2 SMC shown in Fig. 1. The converter has been simulated using MATLAB/Simulink [20] and PLECS Toolbox [21]. In the simulations, the dc voltage is $V_{dc} = 100V$ and a Wye-connected linear RL load ($R = 44\Omega, L = 6$mH) is connected to the converter output. The value of the FCs is $C = 400\mu$F. The fundamental and the carrier frequencies are $f = 50$Hz and $f_s = 2$kHz, respectively. The performance of the proposed voltage balancing method is evaluated in terms of switching frequencies, FFT, and THD values of a line-to-line output voltage for these two carriers, i.e. triangular and sawtooth carriers.

The dynamic behavior of the proposed voltage balancing method operating over a linear unbalanced load (RL) is shown in Fig. 5. An unbalanced condition is introduced in the linear load ($R_a = 22\Omega, R_b = 66\Omega, R_c = 44\Omega$). In this simulation, the initial capacitor voltages were $V_{Ca\,11} = 4$V, $V_{Ca\,12} = 22$V, $V_{Ca\,21} = 26$V, $V_{Ca\,22} = 58$V and regulated to the desired voltages, i.e. 16.67 V, 16.67 V, 33.33 V, and 33.33V, respectively. It can be observed from Fig. 5(a) that the capacitor voltages reach their reference values in about 30 ms. Once in the steady-state condition, the modulation index m changes from 0.6 to 0.9 at 60 ms, and later, at 120 ms, an additional Wye resistive load of about 88Ω is connected. It can

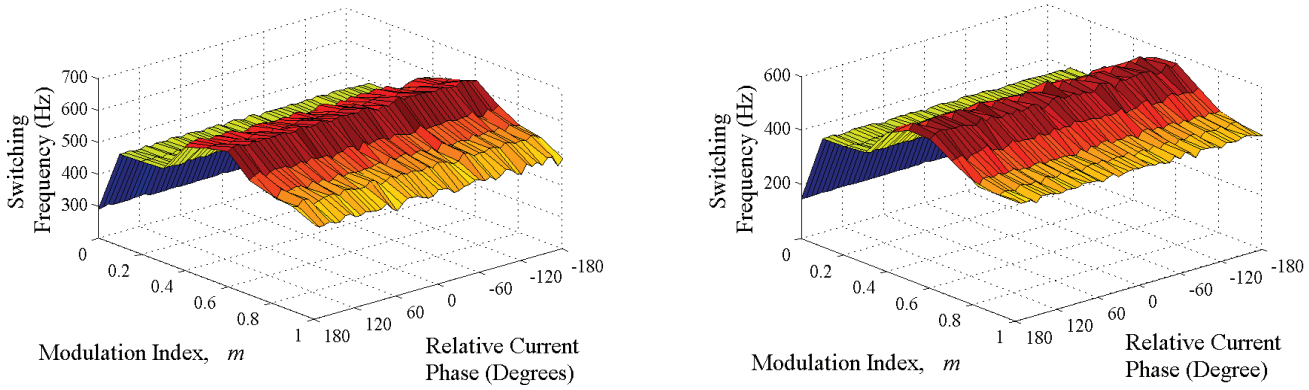


Fig. 7. Switching frequencies of the power devices: (a) using triangular carriers and (b) sawtooth carriers.

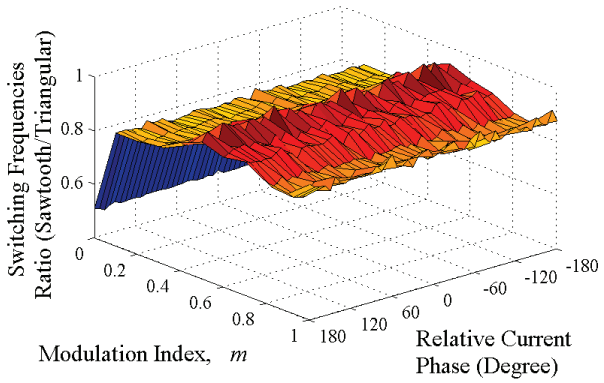


Fig. 8. Switching frequency ratio (sawtooth/triangular) of the power devices.

be noted from Fig. 5 that during these transients the capacitor voltages of the SMC are not affected. Hence, the proposed voltage balancing method proves to be robust not only in the steady state operating under unbalanced load condition but also under dynamic operating conditions.

Fig. 6(a) and Fig. 6(b) show the capacitor voltages ($v_{Ca\,11}$, $v_{Ca\,12}$) for triangular and sawtooth carriers, respectively. As observed, the voltage ripples are almost the same for both carriers. The same can be observed for the capacitor voltages $v_{Ca\,21}$ and $v_{Ca\,22}$ in Fig. 6(c) and Fig. 6(d).

Fig. 7(a) and Fig. 7(b) show the average switching frequencies of the power devices using triangular and sawtooth carriers, respectively. All possible output current phase angles and modulation indices (m) under linear modulation have been considered. It can be seen from the figures, that the output current phase angle does not significantly affects the switching frequency.

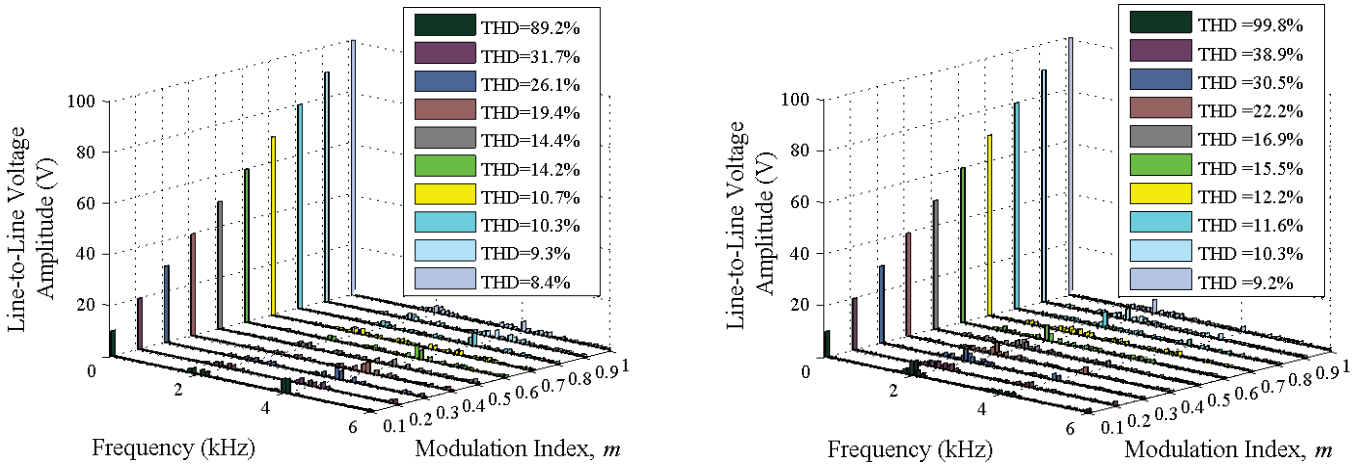
Fig. 8 shows the switching frequency ratio between using sawtooth and triangular carriers for all modulation indices and load power factors. From Fig. 8, it should be remarked that with sawtooth carriers there is a reduction of the switching frequency of about 15% on average for large modulation indices. Such a reduction in the switching frequency is even more significant for low modulation indices.

The FFT of the line-to-line output voltages is shown in Fig. 9(a) and 9(b) for triangular and sawtooth carriers, respectively. These figures show the output voltage spectra for modulation indices ranging from [0.1, 1]. It can be observed that the harmonic components at the carrier frequency (2 kHz) have higher amplitude when using the sawtooth carriers. In the case of sawtooth carriers, the THD is increased by about 1% on average for large modulation indices, and for lower modulation indices the increase is significantly higher. Nevertheless, such an increase in the distortion is produced at high frequencies (around the carrier frequency and above) and no low-frequency distortion appears in any case. Thus, such harmonic components can be easily filtered.

The voltage ripples in the FCs are almost the same using both carriers. The main advantage of using sawtooth over triangle carriers is that it produces significantly less switching frequencies and thus lowers the switching losses.

VI. Conclusion

This paper has proposed a capacitor voltage balancing method for SMCs using PD-PWM. This method calculates the cost function using FC voltage deviations and the load current. It then selects the minimum cost function value of the redundant states at each sampling period. The proposed voltage balancing method is applied to a seven-level SMC. It shows to be very robust under unbalanced loads and transients conditions, as the capacitor voltages are well regulated at the desired levels. Moreover, the seven-level SMC is analyzed using triangular and sawtooth carriers. Simulation results show that the switching frequency of the device is reduced by about 15% using the sawtooth carrier waveforms when compared with the triangular ones. This result agrees with the theoretical analysis, as in sawtooth carriers there are no transitions within the same voltage levels during the sampling instant. The THD values using sawtooth carriers are not significantly increased and the voltage ripples of the FCs remain the same.



(a) (b)

Fig. 9. FFT of the line-to-line voltage for different modulation indices (m) and frequency modulation index $m_f = 40$ using (a) triangular carriers and (b) sawtooth carriers.

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