

Optimal Control of VSC for STATCOM Applications

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Abstract: In this work, a voltage source converter (VSC) is configured to perform STATCOM tasks and generate reactive power. An optimal \mathcal{H}_∞ controller has been successfully implemented including an anti-windup compensator. Data from an experimental test bench is provided and compared with simulation results showing good accuracy level.

Keywords: Optimal Control, VSC, STATCOM, Modeling, Test Bench, Experimental Results.

1. INTRODUCTION

A Flexible AC Transmission System (FACTS) device provides reactive power to the grid enhancing controllability and improving the performance of the transmission system. Among the family of converter-based FACTS devices, Static Synchronous Compensator (STATCOM) is a reliable device and has been installed in many countries around the world (Acharya and Mithulananthan, 2005; Singh et al., 2009). The usual interest of a STATCOM device is to control transmission voltage by reactive power shunt compensation.

However, these devices can be used for various applications depending on the control functions implemented (Zhang et al., 2004). Some authors (El-Moursi et al., 2010) have analyzed the benefits of using STATCOM to mitigate voltage fluctuations and Sub-Synchronous Resonance (SSR). Wind farm integration in power system by using STATCOM has been studied by (Saad-Saoud et al., 1998; Han et al., 2008), and the mitigation of unbalanced voltages is considered by (Li et al., 2007). The impact and stability analysis of the presence of STATCOM devices in the power system have been performed by (Cañizares et al., 2003; Khederzadeh and Ghorbani, 2011).

Given the practical usage of STATCOMs in the electrical systems it is important to investigate the possible control capabilities of this devices. It is interesting as well modeling the operation and control functions of a STAT-

COM and analyze its response and behavior. The control of a STATCOM has been studied by several authors, (Garcia-Gonzalez and Garcia-Cerrada, 1999) developed a PI controller design, (Hochgraf and Lasseter, 1998) has implemented a PID controller for direct and inverse sequence control during unbalanced voltage situation. Linear optimal control based on LQR applied to STATCOM have been studied by (Rao et al., 2000; Lee and Sun, 2002) for power system oscillation suppression and (Soto and Pena, 2004; Sahoo et al., 2002) considered converter control based on feedback linearization techniques.

Other authors have considered the use of \mathcal{H}_∞ optimal control, (Liang et al., 2005; Yang et al., 2011; Zhang et al., 2006). The application of the loop-shaping \mathcal{H}_∞ method is studied by (Farsangi et al., 2002; Rahim and Kandlawala, 2004) for FACTS and STATCOM applications and the use of \mathcal{H}_∞ has been analyzed by (Samir and AL-Baiyat, 2005) for STATCOM control design.

In this work, the design of the STATCOM controller is cast as a mixed sensitivity problem (Sánchez-Peña and Sznajer, 1998). In the first stage a complete model of the system is developed in order to design the controllers and evaluate the response of the system before implementing them in the test bench. In a second stage the \mathcal{H}_∞ controller is implemented in a fixed-point Digital Signal Processor (DSP) embedded in a back-to-back converter configured as a STATCOM device. The \mathcal{H}_∞ control techniques provide a more systematic design procedure and also may achieve better performance. However, the implementation in a fixed-point DSP results more complex than standard PI controllers. The optimal controllers are of higher orders which demands a larger number of code lines, thus, needing more computing time and memory. As a consequence, a

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careful implementation of the control algorithm is necessary in order to avoid unpredictable behaviors.

This paper is organized as follows. In Section 2 a description of the system is given and the main aspects are highlighted. In Section 3 the controller design is discussed. In Section 4, the experimental results are compared with simulations. In Section 5 the conclusions of this work are summarized.

2. SYSTEM DESCRIPTION

The system studied consists of two main parts: an AC side that comprises the grid and the impedances and a DC side composed of a capacitor bank. Interconnecting these two sides there is an IGBT bridge that is commanded by a control board. In Fig. 1 a picture and a schematic view of the real system can be seen.

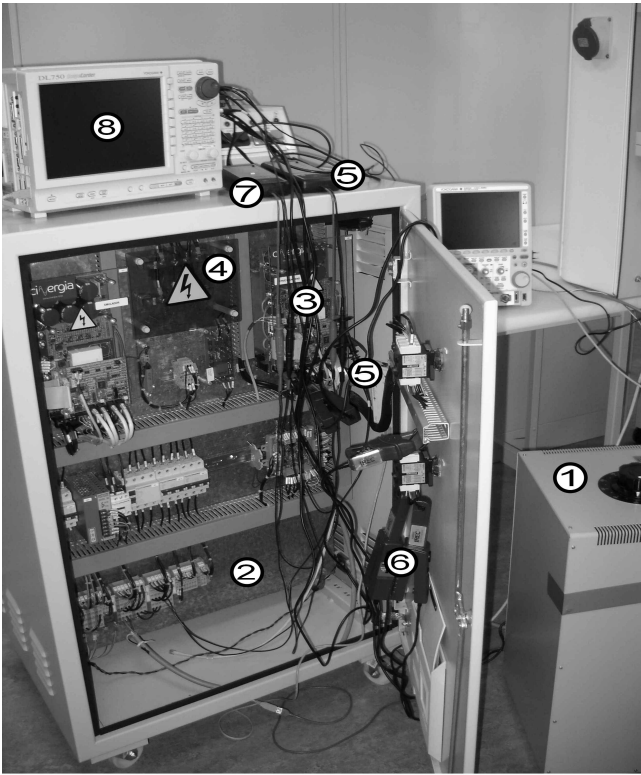


Fig. 1. Schematics of the experimental test bench: (1) Autotransformer, (2) Inductances (located behind), (3) Voltage Source Converter, (4) Capacitor Bank, (5) AC Voltage measurement, (6) AC Current measurement, (7) DC Voltage measurement, (8) Data acquisition system.

The experimental test bench provided by Cinergia (Cinergia, 2010) consists of a 5.5 kW back-to-back converter

connected to the electrical grid by means of an autotransformer, in this way the input voltage can be limited. Between the autotransformer and the converter are located the line inductances. The controllers have been implemented in a TMS320F2808 DSP which is part of the control board that commands the IGBT bridge.

A schematic view of the system can be seen in Fig. 2 and a description is given below. The grid is modeled as an infinite bus using a 3-phase generator which is connected to the converter through an RL branch. The choice of an ideal grid is adequate because the system is not considered to be capable of making any changes in the grid voltages. In the qd reference frame (Park, 1929) the AC currents are described by the following equation (Krause, 1986).

$$\frac{d}{dt} \begin{bmatrix} i_q \\ i_d \end{bmatrix} = \begin{bmatrix} -r/L & \omega_e \\ -\omega_e & -r/L \end{bmatrix} \begin{bmatrix} i_q \\ i_d \end{bmatrix} + \begin{bmatrix} -1/L & 0 \\ 0 & -1/L \end{bmatrix} \left(\begin{bmatrix} v_{lq} \\ v_{ld} \end{bmatrix} - \begin{bmatrix} v_{zq} \\ v_{zd} \end{bmatrix} \right) \quad (1)$$

where i_q and i_d are the qd currents, v_{lq} and v_{ld} are the converter qd voltages, v_{zq} and v_{zd} are the grid qd voltages and ω_e is the electrical angular velocity. This last variable will be assumed constant during the design stage. The grid voltages are projected into a voltage oriented synchronous reference frame which implies that v_{zd} can be assumed to be zero.

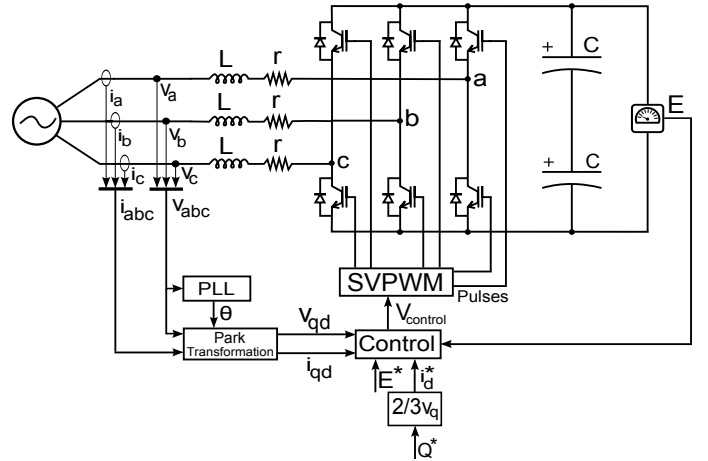


Fig. 2. Schematic view of a STATCOM device

The VSC includes the IGBT bridge and the capacitor bank, the IGBT bridge applies the pulse sequence generated by the Space-Vector Pulse Width Modulation (SVPWM) block at 12 kHz of commutation frequency. The DC voltage (E_{DC}) is measured at the capacitor bank and sampled by the control system. The voltage in the DC bus (Junyent-Ferré et al., 2007) is governed by

$$\frac{dW}{dt} = \frac{2}{C} \left(\frac{3}{2} v_{zq} i_q \right), \quad (2)$$

where $W = E_{DC}^2$.

The active and reactive powers in the qd frame are given by

$$P = \frac{3}{2} v_{zq} i_q, \quad Q = \frac{3}{2} v_{zq} i_d,$$

respectively. Since v_{zq} is usually constant in normal operation, the current i_q is associated to the active power and the current i_d to the reactive power.

3. CONTROL DESIGN

The control block represented in Fig. 2 samples the AC voltages (V_{abc}) and currents (I_{abc}) and the DC voltage (E) at the switching frequency. A discrete Phase-Locked Loop (PLL) delivers the phase angle (θ) at each sample time allowing to perform the Park transformation computing the control law in a $dq0$ frame.

The output of the controller are the AC voltages ($V_{control}$) used by the SVPWM module to generate the pulse sequence that drives the IGBT bridge. The control system has the mission of keeping stable the DC voltage at its reference signal (E^*) while tracking the d-axis current reference signal (i_d^*). A schematic view of this controller can be seen in Fig. 3.

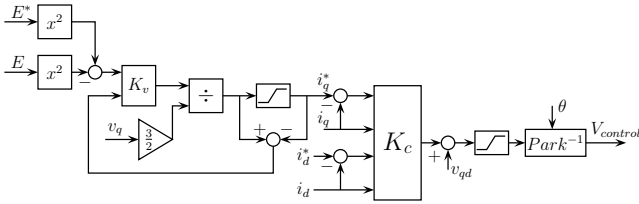


Fig. 3. Schematic view of the controller

The control scheme has a double-loop structure with anti-windup and a feed-forward in the voltage loop. The \mathcal{H}_∞ optimal control has been used for the design of the inner and the outer loop controllers, (Sánchez-Peña and Szaier, 1998). By using this optimal control scheme it is avoided the need of additional decoupling terms and it can improve the fault ride-through capability of the system. Since interactions are exploited during the design process, because of the multi-variable nature of the controller, it may be more effective than decentralized controllers and achieve a better performance (Bianchi et al., 2011). The proposed control does not deal with model uncertainty. However, \mathcal{H}_∞ optimal control is used here to maintain coherence with the anti-windup compensation.

It is common to use an average model of the converter, where high frequency effects are neglected, for controller design purposes. In the average model the system is represented by three AC voltage sources and a DC current source linked by the power flow transfer balance. The control design process is divided in three parts in a similar way that (Bianchi et al., 2011). The first step consisted of designing the current controller K_c solving a mixed-sensitivity problem (Sánchez-Peña and Szaier, 1998). The aim of the design is to minimize the $\|\cdot\|_\infty$ (∞ -norm) of the closed-loop transfer function. The transfer function from the voltages to the currents is denoted by $G(s)$, in Fig. 4 a schematic view of the controller design is plotted.

In the design setup shown in Fig. 4 the aim is to minimize the ∞ -norm of the transfer function from w to z where the reference signal i_{qd}^* is considered a perturbation and the output and the integral of the error are the variables

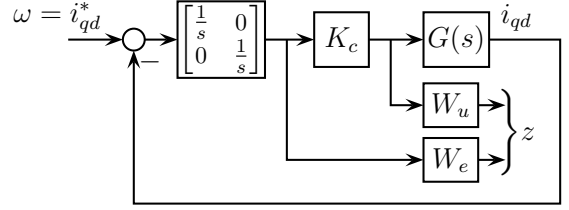


Fig. 4. Setup for the current controller design

to optimize. The transfer function W_u weights the control action to avoid large values of it. The errors are weighted with the integral action and the function W_e to ensure zero steady-state errors. In this work, the weights are scalar values, thus, no poles are added to the system, and are selected to have a fast response tracking the current reference signals. Since the output of $G(s)$ are the qd current (i_{qd}) and the states are known, the system can be described as a state-feedback scheme and formulated as a PI controller resulting in a reduced order controller. This way becomes easier to implement the controller in the real system and reduces the memory used and the computing time in the processor.

In a similar way is designed the voltage controller K_v using instead a new plant model $G'(s)$ which includes the previously computed controller K_c . Taking into account that v_q is a measured variable equation (2) can be linearized pre-multiplying it by the factor $\frac{2}{3v_q}$. This factor and the DC dynamics (2) are included in the $G'(s)$ definition as well. In the voltage controller design it is only considered the behavior of the q current (i_q), this leads to a SISO design where only the ∞ -norm of q voltage (V_q) is considered. In this case the weights W_e and W_u are scalar values too and have been chosen to obtain a null error and steady-state convergence and to avoid excessive control actions when there are variations in the DC voltage.

In the final stage of the design process the anti-windup compensation is included, the design is based on the scheme proposed in (Weston and Postlethwaite, 2000). In this design (Fig. 5) the signal prevents current saturation by acting on the voltage controller and influencing its response. This technique permits the introduction of compensation terms that act during saturation and do not affect the normal operation.

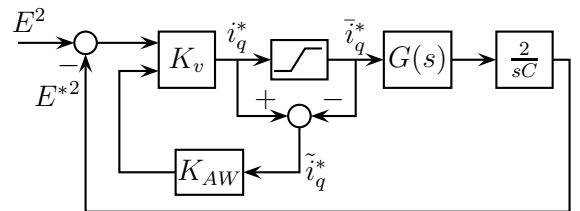


Fig. 5. Anti-windup design scheme

An additional pole placement constraint is added to the constraints on the ∞ -norm of the closed-loop transfer in order to make possible the discrete time implementation of the controller. Using these constraints can be ensured that the poles of the controller are slow enough to be implemented with a switching frequency of 12 kHz in

the converter. The discretization of the linear controllers is achieved by means of the Tustin transformation for a sample frequency of 12 kHz coincident with switching frequency of the SVPWM algorithm.

4. EXPERIMENTAL RESULTS

In this section a comparison between simulation results and experimental results is shown. The model has been developed under Matlab/Simulink[®] platform and the electrical subsystems have been implemented using the SimPowerSystems Toolbox. In order to test the system emulation of a STATCOM device only one IGBT bridge and the capacitor bank (half of the back-to-back converter) are used. By means of the autotransformer the voltage is regulated as a 30% of the grid voltage which is 400 V phase-to-phase with a frequency of 50 Hz.

The parameters of the system can be found in Table 1.

Table 1. System parameters

L (mH)	r (Ω)	C (μF)	freq (kHz)
4.6	0.3	1020	12

The weights (W_e and W_u) used in the designs of these controllers can be seen in Table 2, where $I_{2 \times 2}$ is the identity matrix of 2×2 .

Table 2. Controller weights

Voltage controller		Current controller	
W_e	W_u	W_e	W_u
1	3	$250I_{2 \times 2}$	$0.01I_{2 \times 2}$

The results shown are obtained by commanding a sequence of reactive current (i_d^*) setpoints while keeping stable the DC voltage at 300 V. A comparison of several variables is provided in the next figures. The data measured from the test bench have been filtered with a low-pass filter of 1 kHz. The change in the reactive current provided by the STATCOM can be seen in Fig. 6, the reactive current reference signal sequence is plotted in this figure as well.

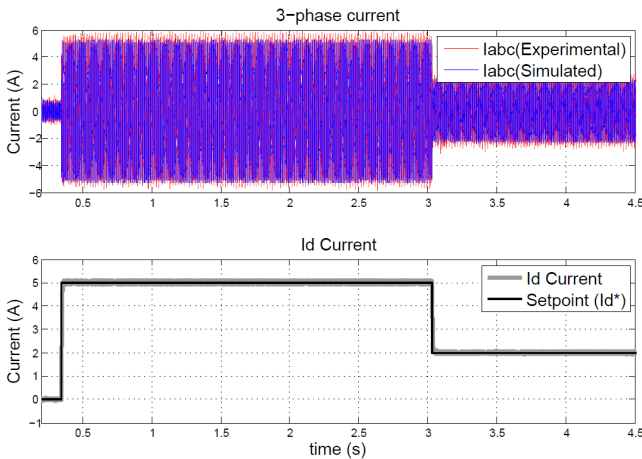


Fig. 6. Three-phase currents and reactive current reference signal

In Fig. 6 can be observed the fast tracking response of the i_d current since the plots match perfectly and the instantaneous reactive current generation observed

in the three-phase current plot. In order to provide a more detailed view of the transients, enlarged plots of the changes in current setpoints are shown in Fig. 7 and Fig. 9. A detailed view of the current generated when the current setpoint is increased (going from 0 to 5 A) can be seen in Fig. 7.

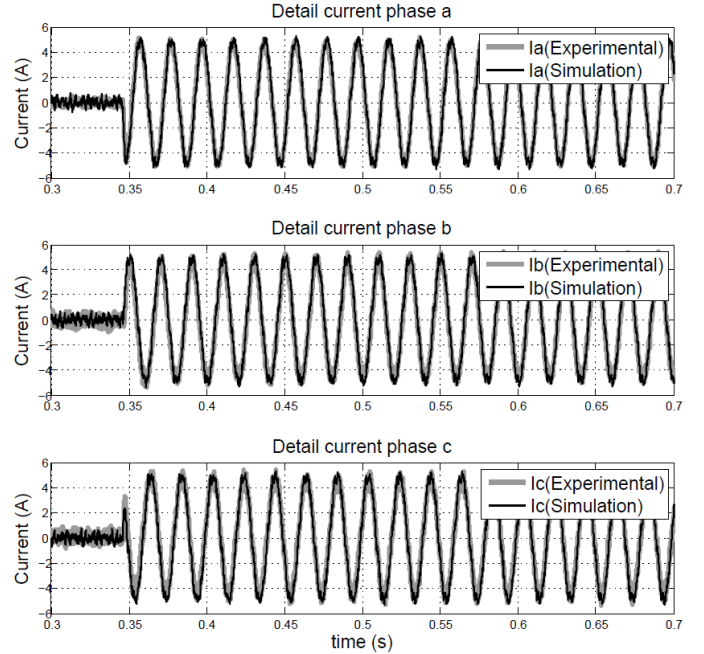


Fig. 7. Comparison between the experimental and the simulation results. Detail of the current evolution for a change from 0 to 5 A in the reactive current reference

The DC-bus voltage evolution can be seen in Fig. 8, in this figure the reference signal (E^*), the measured, and the simulated voltages are plotted. It can be observed a slight variation in the voltages when the reactive current reference signal changes. This small transient can be noticed as well in the experimental data but it is diffuse because of the measurement noise.

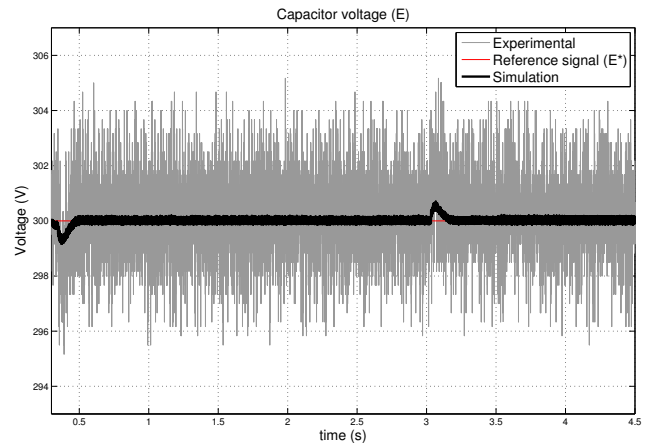


Fig. 8. DC voltage corresponding to changes in the reactive current reference

Little differences can be observed in the comparison of experimental and simulation results, mainly due to noise

captured by the sensors during the experimental tests. A similar observation can be made in Fig. 9 where a detailed view of the transient when the current setpoint is decreased (going from 5 to 2 A) is shown.

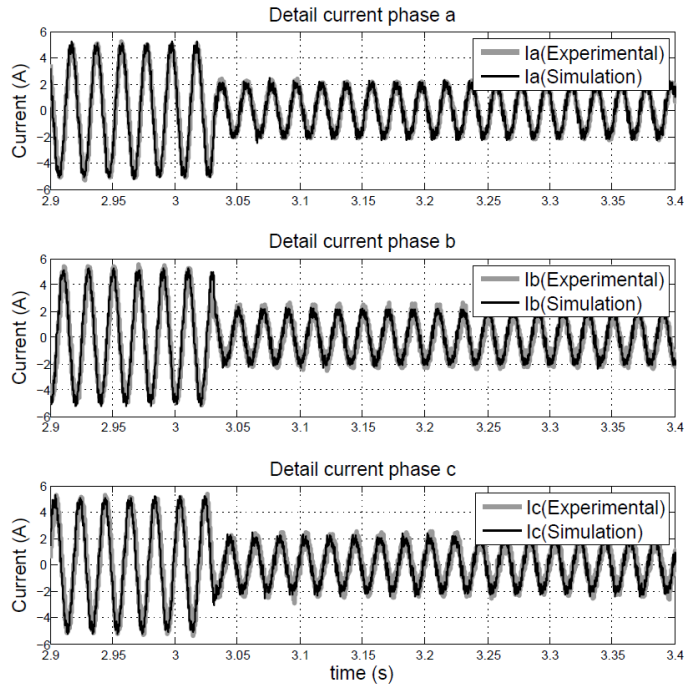


Fig. 9. Comparison between the experimental and the simulation results. Detail of the current evolution for a change from 5 to 2 A in the reactive current reference

In Fig. 10 a comparison of the voltages can be seen, both signals overlap perfectly in this plot since the voltages are not distorted by the action of the converter.

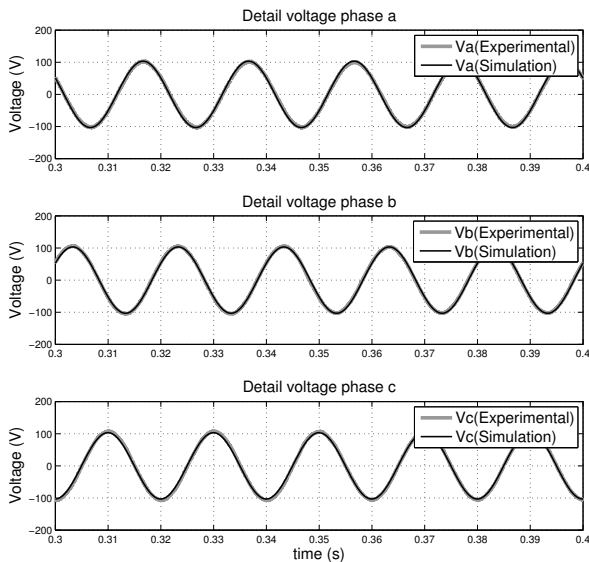


Fig. 10. Grid voltage in the abc frame. Gray lines correspond to the experimental results and black lines to simulation results.

A comparison of a voltage phase and a current phase is plotted in Fig. 11, this way the difference in the phase can

be clearly seen. If both signals were in the same phase no reactive power would be generated.

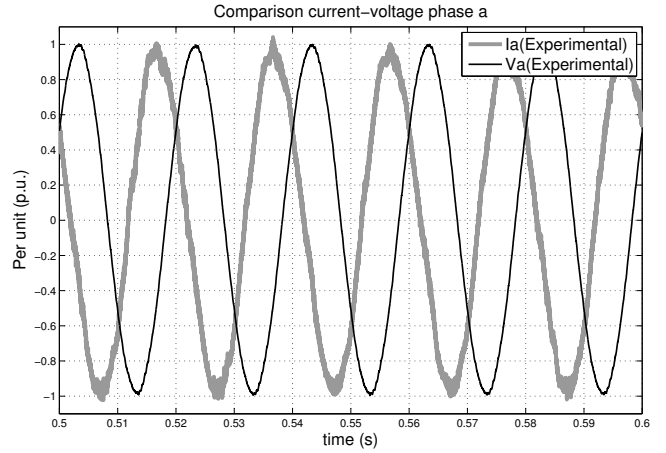


Fig. 11. Grid voltage and current of one phase showing the 90 degrees phase lag corresponding to a pure reactive power generation

The reactive power generated is computed with the former data and is shown in Fig. 12.

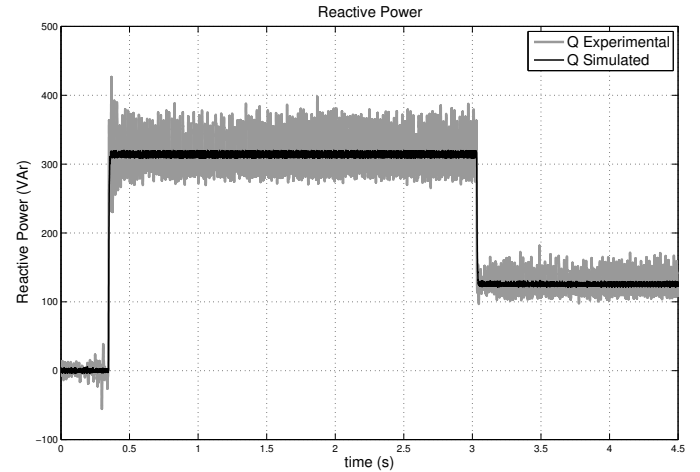


Fig. 12. Reactive power generated according to the changes in the reactive current references

Notice that the same current injection process can be done at higher frequencies for harmonics compensation, for space reasons only results at fundamental frequency are shown.

5. CONCLUSION

In this paper an \mathcal{H}_∞ optimal control scheme for STATCOM has been proposed. Special emphasis has been put on the implementation of the control algorithm in the DSP embedded in the back-to-back converter working as a STATCOM. As a previous step to the real implementation, a model has been developed with the aim of the controller design and also to evaluate the controller behavior. Fixed-point DSP are commonly used in the control of back-to-back converters which impose serious restrictions on the

control algorithm implementation. Simulation and experimental results have been presented which show a good prediction of the response of the system by the model used to design the controller. It is also observed a satisfactory behavior of the control in the experimental test bench.

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