Impact of gate tunnelling leakage on CMOS circuits with full open defects

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Interconnecting lines with full open defects become floating lines. In nanometric CMOS technologies, gate tunnelling leakage currents impact the behaviour of these lines, which cannot be considered electrically isolated anymore. The voltage of the floating node is determined by its neighbours and leakage currents. After some time an equilibrium is reached between these effects. Theoretical analysis and experimental evidence of this behaviour are presented.

Introduction: Open defects are among the most abundant defects in CMOS circuits. An interconnecting open defect consists of the partial or total breaking of a line. The majority of opens isolate the line completely and are referred to as *strong* or *full* opens [1]. Over recent decades, research effort has been devoted to the characterisation of CMOS circuits with open defects [2–4]. However, relatively little attention has been given to opens below the range of sub-180 nm feature size. For these nanometric technologies, the gate oxide thickness is below 30Å and various tunnelling mechanisms lead to significant gate leakage currents [5]. The impact of such non-negligible gate leakage currents on the behaviour of floating lines is addressed in this Letter.

Full open defect model: In the presence of a full open defect, the downstream gates of the defective line are in a floating state. In this situation, the response of the circuit is known to depend on several factors [4] such as (a) the capacitances between the floating line and its neighbouring lines of the semiconductor structures, (b) the parasitic capacitances of the transistors driven by the floating line and (c) the trapped charge in the oxide. Moreover, the logic response of the circuit to the floating voltage depends on the logic input threshold voltage of the downstream gates for each particular test pattern (Byzantine effect). The inclusion of gate leakage current is considered and presented in the following Section to characterise the behaviour of *full* open defects in nanometric CMOS circuits.

Gate direct tunnelling leakage current: The shrinking of feature size in present technologies has led to an important change in the leakage components of CMOS transistors [5]. Such devices have gate leakage current through the gate oxide owing to direct tunnelling mechanisms which is expected to become a significant component of the static power consumption of thin-oxide nanometric CMOS transistors [5]. The density of leakage current flowing through the $Si/SiO_2/Si$ structure of a gate terminal is modelled according to [5]:

$$J_n = AE_{ox}^2 \exp\left(\frac{-B[1-(1-V_{ox}/\phi_{ox})^{3/2}]}{E_{ox}}\right) \quad (1)$$

where constants A and B are defined as $A = q^3/16\pi^2\hbar\phi_{ox}$ and $B = 4(2\,m^*)^{1/2}(\phi_{ox})^{3/2}/3\hbar q$; V_{ox} being the voltage drop across the oxide, t_{ox} the oxide thickness, $E_{ox} = V_{ox}/t_{ox}$ the electric field across the oxide, q the free electron charge, $\hbar$ the reduced Plank's constant, ϕ_{ox} the tunnelling barrier height (3.1 eV for NMOS and 4.5 for PMOS structures), m^* the effective (carrier) mass of an electron (0.4 m_o) or a hole (0.32 m_o) and m_o the free electron mass.

Gate leakage current consists of different contributions, namely, gate-to-substrate leakage current (I_{gb}), parasitic leakage currents through gate-to-substrate/drain extension overlap regions (I_{gs}, I_{gd}) and gate-to-inverted channel tunnelling current (I_{gc}) [5].

Defective CMOS gate with leakage current: To illustrate the effect of leakage gate current on a defective CMOS gate, let us assume the defective inverter shown in Fig. 1. The direct tunnelling components depending on the state of the transistors are shown. Their magnitudes are derived from (1). Since the global input line of the inverter has a *full* open, the gate terminals of the two transistors become floating wires and the voltage at the input and at the output of the inverter might have intermediate voltages between GND and V_{DD}. Fig. 1 shows this situation.

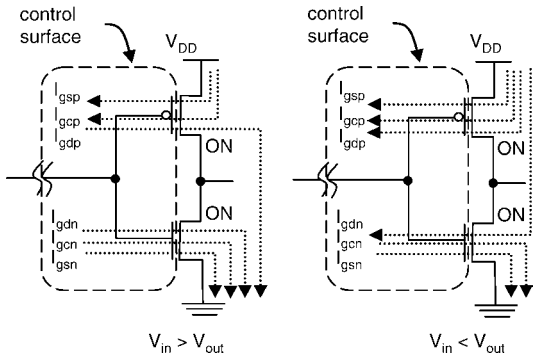

Fig. 1 *CMOS inverter with its input signal floating owing to full open*
Voltage at input node assumed to be in a range turning on both transistors. Otherwise, gate-to-channel components would not exist

The voltage at the input node evolves from its initial value to a final quiescent state (V_{INQ}) owing to leakage currents flowing into and out of the node. The final steady state of the floating node is reached when a resulting null current ($\Sigma I_j = 0$) is generated at the control surface that contains the floating node (see Fig. 1). To determine the steady state V_{INQ}, the intersection between the (V_{in}, V_{out}) curve for $\Sigma I_j = 0$ and the static transfer function of the inverter is used. This quiescent state depends on the technological parameters of (1) and on the topology of the transistors of the defective circuit. Fig. 2 illustrates the calculated current ($I_{in} = \Sigma I_j$) for the inverter of the 0.18 µm technology used in our experiments. Fig. 2 shows the I_{in} current surface for all (V_{in}, V_{out}) values and the resulting zero current curve as a level curve ($I_{in} = 0$). Similar results have been obtained with HSPICE simulations. The final quiescent state of the defective inverter is shown in Fig. 3.

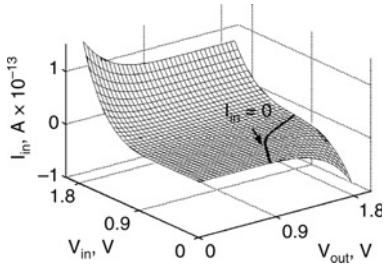

Fig. 2 *Resulting sum of all leakage gate current components (I_{in}) at floating input of defective CMOS inverter illustrated in Fig. 1 for a technology with $t_{ox} = 30$Å and minimum size for transistors (curve level for $I_{in} = 0$ illustrated)*

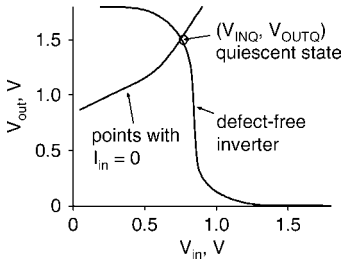

Fig. 3 *Quiescent state of defective inverter obtained from intersection between pairs (V_{in}, V_{out}) causing $I_{in} = 0$ and DC transfer characteristic of defect-free inverter*

Experimental results: In this Section, experimental results for a CMOS 0.18 µm NXP Semiconductors circuit are presented. Fig. 4*a* illustrates the time behaviour of the I_{DDQ} (with normalised current units) for two different patterns of the defective device. Similar time-dependent I_{DDQ} behaviour has been previously observed [6]. The two considered patterns activate the defect and set the faulty net to a logic value opposite to that of the defect-free case. The quiescent current does not decrease down to the defect-free value but remains higher than twice this current value. The time evolution also affects the logic behaviour of the fault since it behaves as a SA1 under nominal conditions. However, when the faulty net reaches its final quiescent state, after some time it behaves as a SA0.

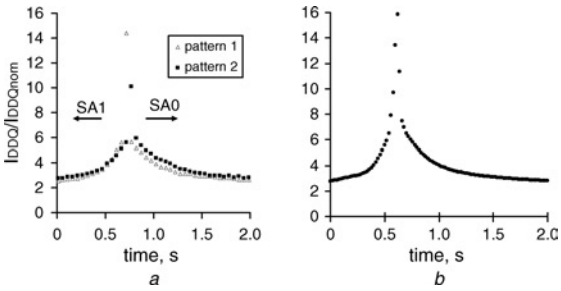

Fig. 4 *Time-dependent behaviour of experimental defective device (HP-82000) and of defective device for patterns 1 and 2*

a I_{DDQ} time-dependent behaviour of experimental defective device (HP-82000)
Quiescent current consumption normalised to defect-free value
b HSPICE (BSIM4.0) simulated I_{DDQ} time-dependent behaviour of defective device for patterns 1 and 2
Time behaviour depends on initial state of floating node and on test pattern driving downstream gate. In this particular case, both patterns 1 and 2 drive downstream gate in same way

The experimental behaviour of the defective device agrees with the prediction derived from what has been presented in the preceding Sections. The capacitive divider created by the floating node and all the parasitic capacitances to the neighbouring structures and the trapped charge determine the voltage value of the floating net at the beginning of its transient evolution. This initial voltage is interpreted as a logic 1 although the defect-free value is a logic 0, thus leading to a SA1 faulty behaviour. However, the gate tunnelling leakage current causes the floating net to evolve to a quiescent state different from the initial one.

The downstream gate of the defective net consists of a single inverting stage. Its final quiescent state is presented in Fig. 3. The voltage at the floating net is interpreted as a logic high value and a non-negligible quiescent current is flowing about twice the defect-free value (as observed in the tail of Fig. 4*a*).

The proposed analysis predicts the final state of a full open defect. In addition, it is possible to verify whether the transient behaviour experimentally measured is consistent with the predicted behaviour by HSPICE simulations. For this purpose, Fig. 4*b* shows the simulated transient behaviour of the current consumption for the gate driven by the floating node. The BSIM4.0 model has been used for the transistor in order to include the gate leakage current effect. As derived from Fig. 4*b*, the simulated time behaviour is consistent with the experimental measurements. In the simulation, an equivalent coupling capacitance of 110fF at the floating node and no trapped charge have been assumed.

Conclusion: Full open defects in interconnection lines of nanometric CMOS circuits have been analysed. The voltage of the floating line generated by the full open depends on its topological characteristics, namely parasitic capacitances to neighbouring structures, transistor capacitances of the downstream gate(s) and trapped charge. However, owing to the reduction of the oxide thickness in nanometric CMOS technologies, gate tunnelling leakage also impacts the behaviour of circuits with full open defects. The Letter shows that floating lines cannot be considered electrically isolated anymore and that they are subjected to transient evolutions until reaching a quiescent state, determined by the technology and the downstream gate(s). For future technologies, gate leakage current is expected to increase significantly [ITRS]. Therefore, the analysed phenomenon will become observable in a shorter transient time after which the predicted quiescent voltage on the floating line will be reached. Theoretical analysis as well as experimental evidence of this behaviour have been presented for an industrial chip of 0.18 μm technology.

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