Output-Capacitorless CMOS LDO Regulator Based on High Slew-Rate Current-Mode Transconductance Amplifier

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***Abstract*— A low quiescent current output-capacitorless CMOS LDO regulator based on a high slew-rate current-mode transconductance amplifier (CTA) as an error amplifier is presented. Load transient characteristic of the proposed LDO is improved even at low quiescent currents, by using a local common-mode feedback (LCMFB) in the proposed CTA. This provides an increase in the order of transfer characteristic of the circuit, thereby enhancing the slew-rate at the gate of pass transistor. The proposed CTA-based LDO topology has been designed and post-layout simulated in HSPICE, in a 0.18 μm CMOS process to supply a load current between 0-100 mA. Post-layout simulation results reveal that the proposed LDO is stable without any internal compensation strategy and with on-chip output capacitor or lumped parasitic capacitances at the output node between 10-100 pF.**

I. INTRODUCTION

Low-dropout regulators (LDO) are widely used either alone in many integrated power management circuits or as post regulators of switching converters, as they can provide wideband and reliable regulated low noise supply voltage for noise-sensitive analog and RF loads [1]. The typical structure of an LDO consists of an error amplifier, a pass transistor controlled by the error amplifier, a feedback network, and an output capacitor. Most of conventional LDOs use a large off-chip capacitor for stability requirements [1, 2]. However, large capacitors can not be implemented as on-chip capacitors. Therefore, output-capacitorless LDOs are needed for SoC applications. However, doing so will cause that the distance between poles at the output node of the LDO and the gate of the pass transistor decreases and, thus, the stability of the circuit worsens, significantly. Additionally, it will increase the output voltage deviations, ΔV_{out}, when a sudden change occurs in the load current. Therefore, having a stable output-capacitorless LDO with small ΔV_{out} and proper settling time (T_{settle}) is a design target.

Some papers in connection with output capacitorless LDOs have been reported in recent years [3-7]. The reported LDO in [3] has an ultra fast transient response characteristic with an on-chip output capacitor of 0.6 nF, which occupies a large silicon area. Moreover, it consumes significant high quiescent current of 6 mA and, thus, it is not appropriate for low power design. In [4], a slew-rate enhancement stage is used between the output of LDO and the gate of pass transistor which increases the slew-rate at the gate node of the pass transistor and provides proper transient response. Similarly, in [5], a capacitor multiplier stage is used between these two nodes in order to provide enough distance between the dominant and non-dominant poles and also minimize the effect of feedback loop-bandwidth limitation, improving the dynamic performance of the LDO. However, these solutions add more power consumption. LDOs based on the flipped voltage follower (FVF) were introduced in [6, 7] which suffer from weak load and line regulation and the need to have minimum load current for stability.

The transient response of an LDO is determined by both the loop gain bandwidth and the slew-rate at the gate of pass transistor (SR_G) [2]. Increasing the bandwidth makes the compensation process more difficult and, therefore, the bandwidth of LDOs is generally low. Additionally, if SR_G is much slower than the gain-bandwidth product, transient voltage spikes appear at the output voltage node during fast load transient [1]. Thus, SR_G should be increased in order to have a proper transient response. Using a high slew-rate current-mode error amplifier instead of a voltage-mode one, which suffers from limited slew-rate, can improve the transient response while also decreasing power consumption. In [8], a class-AB push-pull amplifier was used as error amplifier to source and sink more current for charging and discharging the gate capacitor (C_g) of the pass transistor during the transient event. However, in low power mode, this amplifier will be capable to generate a considerable current into the output load only if a relatively large input voltage is applied to it. This fact causes high output voltage deviations in the LDO transient response. Additionally, the LDO output current range is between 50 μA to 50 mA and the stability of the regulator goes down significantly for output current less than 50 μA.

This paper presents an output-capacitorless LDO based on a new class-AB current-mode transconductance amplifier (CTA) with capability of generating a considerable current even if the input voltage is not very large. Using this circuit as an error amplifier in the proposed LDO, it results in a

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proper transient response with small ΔV_{out} even for low quiescent currents.

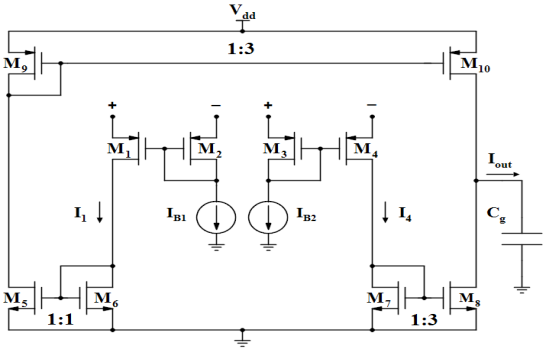

Figure 1. Class-AB transconductance amplifier used in [8].

II. Proposed CTA Error Amplifier

Slew-rate (SR_G) in a class-A OTA is proportional to the maximum bias current that the output capacitor can sink or source. However, increasing the bias current in order to increase SR_G will cause more static power loss. Therefore, using a class-AB amplifier instead of class-A can eliminate this limitation. Fig. 1 shows the class-AB transconductance amplifier which was applied in the LDO reported in [8]. Applying the differential voltage V_{id} to the input nodes, will cause that currents I_1 and I_4 always change in different directions. Assuming all transistors operate in the saturation region and neglecting body and channel length modulation effects, the large signal analysis can be derived as:

$$I_1 = \frac{\beta_1}{2}\left(V_{id} + V_{SG2} - |V_{tp}|\right)^2 = \frac{\beta_1}{2}\left(V_{id} + \sqrt{\frac{2I_{B1}}{\beta_2}}\right)^2 \quad (1)$$

$$I_4 = \frac{\beta_4}{2}\left(-V_{id} + V_{SG3} - |V_{tp}|\right)^2 = \frac{\beta_4}{2}\left(-V_{id} + \sqrt{\frac{2I_{B2}}{\beta_3}}\right)^2$$

in which $\beta = \mu_p C_{ox}(W/L)$ and V_{tp} is the threshold voltage of input PMOS transistors. According to the aspect ratios of current mirrors and neglecting channel length modulation effect, the output current is $I_{out} = 3I_1 - 3I_4$. Thus, the transfer characteristic (i.e., I_{out} versus V_{id}) is a second order function of V_{id}. If one can increase the order of the transfer characteristic without decreasing the speed of signal path, this will enhance the slew-rate for the same V_{id}. Using local common-mode feedback (LCMFB) technique can be a suitable approach for this purpose [9, 10]. Fig. 2 shows the proposed current-mode transconductance amplifier (CTA) in which LCMFB technique is used to enhance the slew-rate of the amplifier. When no differential voltage is applied to the input ports, currents I_1 and I_4 are equal to I_{B1}=I_{B2}=I_B. In this situation no current flows through R_1 and R_2. After applying a differential voltage of V_{id} to the input ports, a differential current $I_d = I_1 - I_4$ is created and the currents through resistors will be $I_R = (I_1 - I_4)/2$. The drain current of transistors M_6 and M_7 will be a common-mode current $I_{cm} = (I_1 + I_4)/2$. Therefore, the gate and drain voltages of M_6 and M_7 will change as follows:

$$V_{d6} = V_{g6,7} + R_1 I_d/2 \quad V_{d7} = V_{g6,7} - R_2 I_d/2 \quad V_{g6,7} = V_{tn} + \sqrt{\frac{2I_{cm}}{\beta_{6,7}}} \quad (2)$$

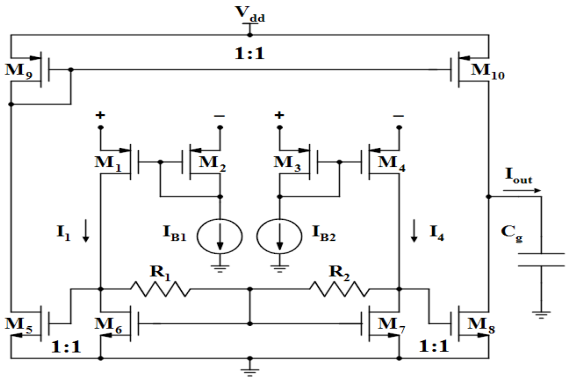

Figure 2. The proposed CTA.

The resistors R_1 and R_2 act as a common-mode feedback circuit [11] and control the common-mode voltage level at the drain of M_6 and M_7 without altering the differential mode behavior of the circuit. According to (2), the currents of transistors M_5 and M_8 are, respectively:

$$I_5 = \frac{\beta_5}{2}\left(V_{g6,7} + \frac{R_1 I_d}{2} - V_{tn}\right)^2 = \frac{\beta_5}{2}\left(\sqrt{\frac{2I_{cm}}{\beta_{6,7}}} + \frac{R_1 I_d}{2}\right)^2 \quad (3)$$

$$I_8 = \frac{\beta_8}{2}\left(V_{g6,7} - \frac{R_2 I_d}{2} - V_{tn}\right)^2 = \frac{\beta_8}{2}\left(\sqrt{\frac{2I_{cm}}{\beta_{6,7}}} - \frac{R_2 I_d}{2}\right)^2 \quad (4)$$

Assuming M_9 and M_{10} are similar, the output current is $I_{out} = I_5 - I_8$. For V_{id}>0, the output current is $I_{out} \approx I_5$, and, similarly, for V_{id}<0, $I_{out} \approx -I_8$. Therefore, when V_{id}≠0, the output current is equal to:

$$I_{out} = I_5 - I_8 \approx \pm\frac{\beta_{5,8}}{2}\left(\sqrt{\frac{2I_{cm}}{\beta_{6,7}}} + \frac{R_{1,2}|I_d|}{2}\right)^2 \quad (5)$$

Considering the second order relationship between I_d and V_{id} according to (1), the transfer characteristic of the proposed amplifier (I_{out} versus V_{id}) is a 4th order function of V_{id}. As a consequence, the circuit can enhance SR_G by generating a considerable current into the output.

III. Proposed LDO

The transistor-level schematic of the proposed LDO is shown in Fig. 3. It consists of the proposed CTA as the error amplifier, the pass transistor M_p, the on-chip output capacitor, and the reference buffer. The aspect ratio of the pass transistor has been set to W/L=6000μm/0.18μm to provide a 100-mA load current at 200 mV dropout voltage. The LDO is configured in a unity feedback structure to have the output voltage equal to the reference one. When an error between these voltages is sensed by the error amplifier, the CTA generates a suitable current to source or sink the gate capacitance of M_p. For example, in case that the load current increases, the output voltage will drop. Thus, the drain current of M_4 increases and that of M_1 decreases. It will cause the increase of the drain terminal voltage of M_7 and the decrease of the drain voltage of M_6. Therefore, the drain current of M_8 increases and those of M_5, M_9, and M_{10} decrease and, hence, the gate capacitance of M_p is discharged so that more drain current is sourced to the load, increasing the output voltage. An analogous dual mechanism occurs when the load current decreases.

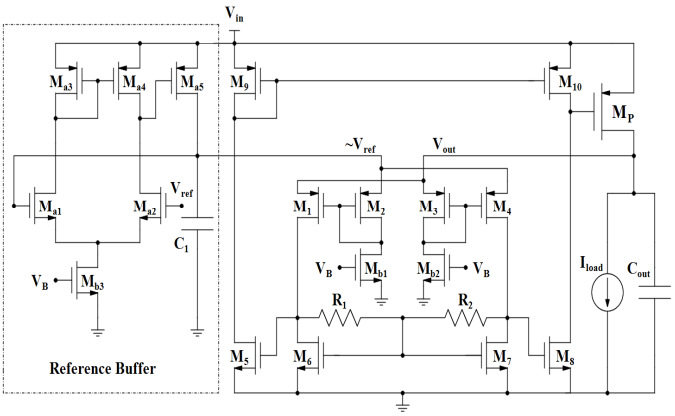

Figure 3. Schematic of the proposed LDO

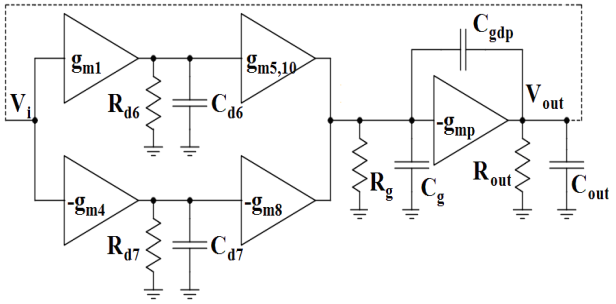

Figure 4. Small signal model of the proposed LDO

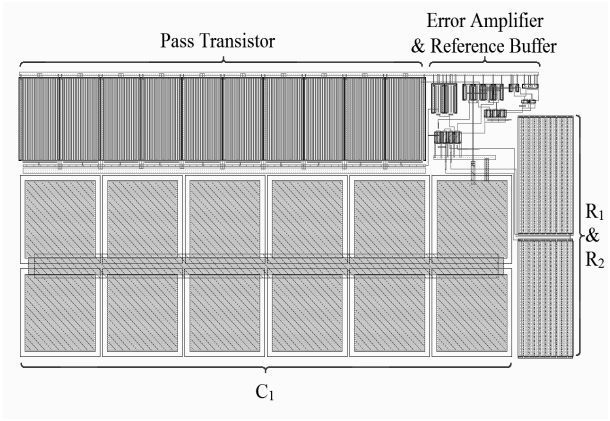

Figure 5. Layout of the proposed LDO

The small signal model of proposed LDO is shown in Fig. 4, in which g_{mi}, R_{di}, and C_{di} are the transconductance, output resistance, and capacitance at the drain terminal of transistor M_i, respectively. Also R_g-C_g and R_{out}-C_{out} are the equivalent resistance and capacitance at the gate and drain terminals of M_p. Carrying out small signal analysis on the circuit, the DC gain, and pole-zero positions are as bellow:

$$A_0 \approx 2g_{m1}R_{d6}g_{m8}R_g g_{mp}R_{out} \tag{6}$$

$$p_1 = \frac{-1}{R_g C_g} \quad p_2 = \frac{-1}{R_{out}C_{out}} \quad p_3 = \frac{-1}{R_{d6}C_{d6}} \quad z_1 = \frac{g_{mp}}{C_{gdp}} \tag{7}$$

Considering $R_{d6} = R_{d7} \approx R_{1,2}$, $R_g = r_{o8} \| r_{o10}$, and $R_{out} \approx 1/g_{m1} \| r_{op}$, and assuming C_g, $C_{out} >> C_{d6}$, C_{gdp}, the pole P_3 and the zero Z_1 will be located at frequencies higher than

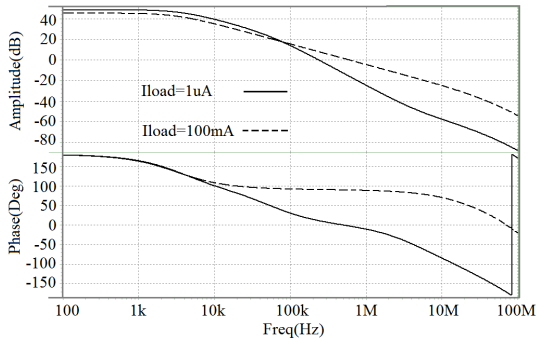

Figure 6. Open loop AC response of the proposed LDO

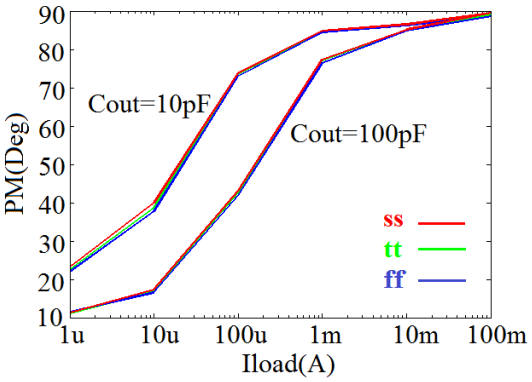

Figure 7. Phase margin of the proposed LDO for different load currents, output capacitors, and process variation

two other poles and the unity gain frequency (ω_T). Therefore, it is possible to model the loop gain as a transfer function with two poles at frequencies below ω_T. With an increase in the load current or for a small output capacitor, the distance between the poles becomes wider and, thus, the phase margin will be enhanced. Moreover, if R_1 and R_2 are voltage-controlled resistors (transistors biased in the triode region), the phase margin can be adjusted by changing the resistors for a certain lumped capacitance at the output.

IV. Circuit Characterization

The proposed LDO topology has been designed and laid out, as shown in Fig. 5, to source the nominal load current between 0-100 *mA* and the obtained performance metrics correspond to HSPICE post simulations in a 0.18 µ*m* CMOS process. In order to test the LDO for different values of output capacitor, C_{out} is not included in the layout and the core area of the chip without the output capacitor is 110×230 μm^2. The dropout voltage of the LDO is set to 200 *mV* for 1.2-2 *V* input voltage V_{in}. The total quiescent current of the LDO, including the current consumed by the reference buffer circuit, is only 3.7 µ*A*. Fig. 6 shows the simulated open loop AC response of the proposed LDO for light and heavy load currents with C_{out}=100 *pF*. For an accurate AC response analysis, the values of phase margin for different load currents and output capacitors by considering the effect of process variation are shown in Fig. 7. As it can be seen, even under the worst condition (large output capacitor and light load current) the proposed LDO is stable and has still an adequate phase margin and has a less sensitivity to the process variation.

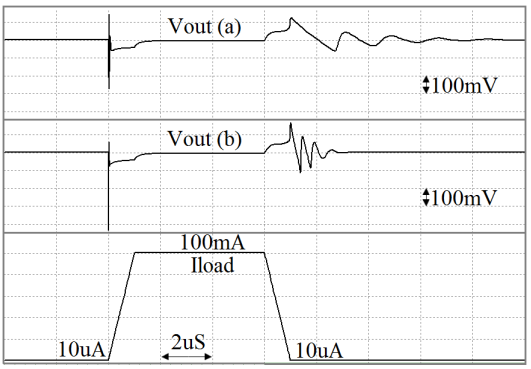

Figure 8. Load transient of the LDO (a) C_{out}=100 pF, (b) C_{out}=10 pF

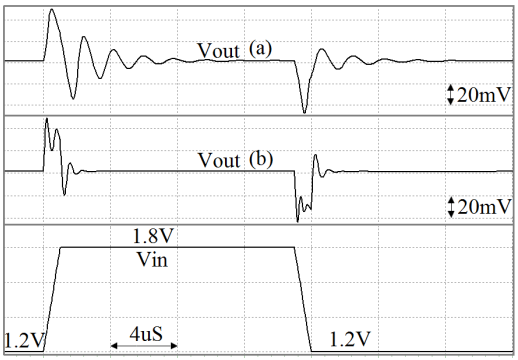

Figure 9. Line transient of the LDO (a) C_{out}=100 pF, (b) C_{out}=10 pF

Fig. 8 shows the load transient response of the LDO for two output capacitors when the load current is changed between light to heavy values with rise and fall times of 1 μs. As it is obvious, the proposed LDO is stable even for the worst condition and its T_{settle} and ΔV_{out} are 6 μs and 277 mV, respectively. Line transient response of the LDO is shown in Fig. 9, in which the line voltage is changed between 1.2 V and 1.8 V with rise and fall times of 1 μs. It indicates that, for all cases, the LDO has a T_{settle} and ΔV_{out} less than 9 μs and 47 mV, respectively.

Table I provides a performance comparison between the proposed LDO and recent works. In order to have a fair comparison, the other LDOs are simulated in HSPICE with the parameters mentioned in the papers. The figure of merit ($FOM = \Delta V_{out} C_{out} I_Q / I^2_{out,\max}$) used in [3] is adopted here to compare the transient response of different LDOs. A lower FOM implies better transient response achieved by the LDO. Notice that using a high slew-rate CTA with very low quiescent current in the proposed LDO helps to achieve lower FOM in comparison to the other reported alternatives.

V. Conclusion

An output-capacitorless CMOS LDO regulator based on a high slew-rate CTA is presented. The load transient characteristic of the LDO is improved by using a LCMFB technique in the proposed CTA which results in an increase of its nonlinear transfer characteristic order. Post-layout simulation results in a 0.18 μm CMOS process show that the proposed LDO is stable for a wide load current range between 0-100 mA without any internal compensation capacitor and with output capacitor in the range of 10-100 pF while its total quiescent current is only 3.7 μA.

TABLE I. Performance comparison

Parameter	[4]	[5]	[6]	[8]	**This Work**
Tech [μm]	0.35	0.35	0.35	0.18	**0.18**
V_{IN} [V]	1.8	3	1.2	1.2	**1.2**
V_{OUT} [V]	1.6	2.8	1	1	**1**
I_{OUT} [mA]	100	50	50	50	**100**
I_Q [μA]	20	66	95	1.2	**3.7**
C_{OUT} [pF]	100	100	20	100	**100**
T_{settle} [μs]	≈8	≈4	≈1.4	≈4.4	**≈6**
ΔV_{OUT} [mV]	100	110	200	490	**277**
CE (%)	99.98	99.86	99.81	99.99	**99.99**
FOM [fs]	20	290	152	23.5	**10.2**

Acknowledgments

This work has been partially supported by Micro-ISTI, and the Spanish Ministry of Science and Innovation thanks to projects TEC2010-15765, and RUE CSD2009-00046 (Consolider-Ingenio 2010).

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