Low cost OFDM based transmitter for underwater acoustic communications

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***Abstract*— on this work a low cost OFDM transmitter for underwater sensor networks is presented. The transmitter is based on a low power microcontroller that governs a DDS in order to generate the output data -OFDM symbols- avoiding the IFFT computations. This solution represents a new design perspective for the current UWSN -mainly based on FPGAs or DSPs, allowing to reduce the cost, the power consumption and the size of the current transmitters.**

Keywords— UWSN; OFDM; acoustic communications; DDS

I. INTRODUCTION

For many years, underwater sensor monitoring has been performed using autonomous data-loggers, which are subsystems that record data for a period of time. This offline monitoring has been widely used because the challenges that present the underwater environment related with communications: the strong signal attenuation, the transmission loss, the multi-path propagation, the Doppler spread, the time variation of the channel and the addition of background noise [1].

As is known, the most appropriate way to transmit data underwater is acoustically, and is currently a growing work area with constant contributions and improvements. Nowadays, some commercial acoustic modems are in the market, but the prices -around 6000€- and the power consumption, make them inappropriate for low cost underwater sensor networks [2]. On the other hand, most of them are not suitable for short distances -below 100m.

Low cost, low size and low power consumption are desirable needs for environmental underwater sensors. Sensors can be deployed at different places in the area of study, and operate autonomously using batteries. With an appropriate acoustic transmitter installed on them, data can be shared between nodes or monitored wirelessly; but this update must respect the initial requirements imposed by the medium; and therefore, low cost and low power consumption are the desired objectives in acoustic transmitters designs.

Significant improvements and contributions have been made recently in the underwater communications area and the underwater sensor networks [3][4][5]. For example, FSK coherent demodulation has been performed in [6] using a low power microcontroller with a MAC unit. This solution allows reducing consumption taking advantage of a better bandwidth than a non-coherent modulation

But at present, OFDM is the most robust modulation which can be used in the underwater environment. And some works show the improvements in terms of higher throughput and lower transmission error rate.

OFDM is not a new modulation technique. The OFDM computational demand is the cause of the delay of this technology, and it had to wait until the arrival of powerful processors with reasonable prices.

OFDM is commonly implemented in FPGAs or DSPs, however such solutions could be oversized for small sensors applications and also could not meet the low-power specifications.

Low power microcontrollers could be an interesting choice since nowadays there are some models with DSP capabilities. However, the computational load and memory required for FFT and IFFT computations make them unfeasible.

This paper presents a new perspective addressed to OFDM, avoiding the generation of symbols through IFFTs computations.

The solution proposed includes a low power microcontroller that governs a direct digital synthesizer -DDS- which generates the OFDM symbols. Together with the power amplifier circuit presented, are the parts of a new type of transmitter for low-cost underwater sensor networks.

II. DESIGN AND HARDWARE DESCRIPTION

The scheme of the design presented is shown in Figure 1. An ultra-low power microcontroller is the core of the design; it acquires data from the sensor -so it has an analog to digital module integrated- and governs a DDS in order to create the data to transmit –symbols.

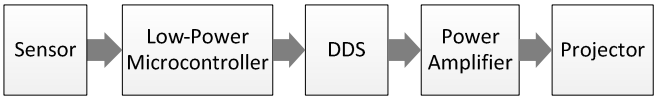

Fig. 1. Transmitter design scheme

Funded by Spanish Ministry of Economy and Competitiveness

978-1-4799-0002-2/13/$31.00 ©2013 IEEE

DDSs are being used increasingly and they represent an alternative to traditional analog solutions for frequency synthesis. It is because they offer some performance benefits as ease of synchronization to obtain quadrature signals and a faster transition frequency, among others. They offer micro-Hertz tuning resolution of the output frequency and sub-degree phase tuning capability -all under complete digital control, commonly SPI- and extremely fast hopping speed in tuning output frequency or phase. On the other hand, they are compact and require little power and space. Because of these characteristics and the ease of control them, DDSs are an interesting solution in order to synthesize the symbols to transmit.

Currently, DDSs have only a single output. Therefore, to get a formally OFDM transmission, multiple DDS are needed -as much as carriers are required. In this way, the different modulated carriers are generated in parallel by each DDS. Since master clock and SPI bus could be shared between DDSs, it is possible to get a precise synchronization between them. This proposal requires that all DDSs signals are added before the power amplifier stage; it can be done using operational amplifiers. Figure 2 shows a complete outline of the proposal.

In this paper, for initial testing of the concept, only one DDS has been used, getting a single carrier.

III. IMPLEMENTATION AND CONSIDERATIONS

One of the most important considerations in the design has been the power consumption, so components have been selected meticulously. Moreover, the design allows the possibility of shut-down the different parts of the design in order to reduce power consumption during idle periods.

Low power strategy was devised since UWSN are not collecting data continuously –the usual variables under study change slowly. So, to extend the life of the battery we propose to power-down the microcontroller, the DDS and the power amplifier stage during idle operations. Only microcontroller wakes up to acquire and to transmit data. The DDS and the power amplifier stage only wake up, when the microcontroller needs to transmit data – this can be every time new data is acquired, or when data exceeds certain thresholds.

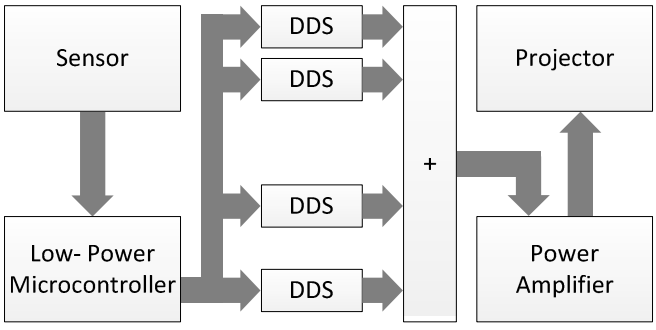

Fig. 2. Proposal outline

Another aspect to consider is the size, but for the first prototype, the most suitable package was selected to allow easy assembly and test.

In the following subsections the different parts of the design are explained along with the results

Microcontroller and DDS

For this proposal, the considerations to taken into account in the selection of a suitable microcontroller, are reduced to three points: low consumption, integrated analog to digital converter –to acquire the signal from the sensor, and a SPI module in order to control the DDS – the majority are controlled by this standard.

To meet these points, the PIC16LF88 microcontroller with nanoWatt technology has been selected. To get an idea of its power consumption, in sleep mode it consumes 200nA at 2V.

The DDS AD9833 from Analog Devices has been chosen for this prototype; with 12.65mW of power consumption it is not the most low-power DDS but the package –MSOP, is more suitable for the prototype. Currently, the AD9837 with 8.5mW is the most low-power DDS.

The microcontroller has been configured to operate using its internal oscillator to reduce consumption. A CMOS clock with enable pin was selected in order to provide the master clock signal to the DDS. When DDS is not used –during no transmissions- the microcontroller turns off the CMOS clock and power consumption is reduced.

Amplifier stage

A power amplifier for piezoelectrics requires that the stage could drive current to capacitive loads and have a moderately high slew rate.

The projector used for testing the prototype is the Brüel & Kjaer 8103. The Calibration chart of the hydrophone shows a capacitive load about 4nF – including integral cable. With this capacitance, the power operational amplifier OPA454 could offer signal amplification up to 180 kHz at 12V.

An important consideration about this amplifier is it has an enable pin to disable the output stage reducing the quiescent current to conserve power, one of the requirements desired.

In order to provide the necessary current a parallel amplifier circuit is proposed, figure 3. This implementation could offer up to 50mA. If more current is required because de piezoelectric characteristics, more OPA454 could be connected in parallel.

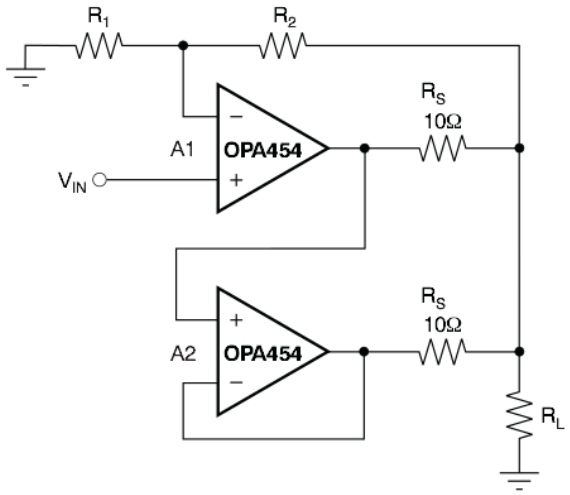

Fig. 3. Proposed power amplifier stage

IV. TESTS AND RESULTS

To validate the spurious and the quality of the signal synthesized by the DDS, the microcontroller has been programmed to send to the DDS the commands required to generate a sinusoid signal of 80 kHz, and with a DAQ acquisition board the signal has acquired and analyzed.

The DAQ has been configured for 2Msps and results of the test are shown in Figure 3. There is a clean signal but analyzing FFT, some spurious are observable because synthesizing process. The most important is at twice the generated signal, 160 kHz, because could be a frequency used in underwater acoustic communications, however there are 62dB of difference between the signal generated.

Spurious from 200 kHz are not as important because the medium attenuate them quickly.

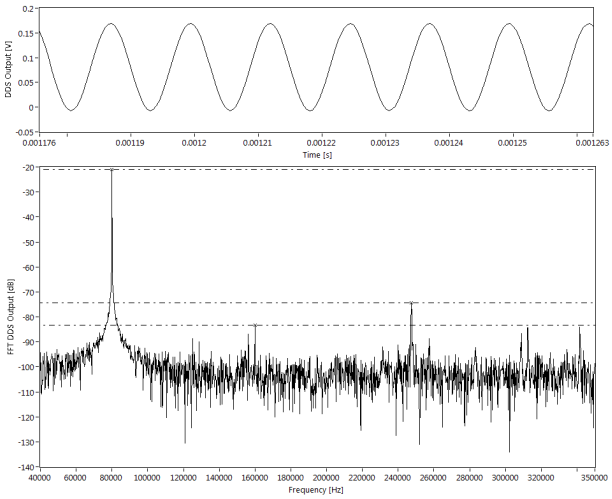

Fig. 4. Analysis of DDS signal output

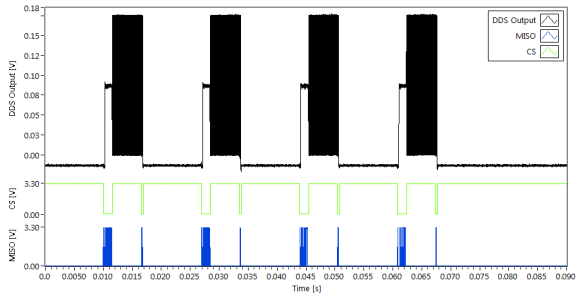

Fig. 5. Symbols generated

A test of transmission was performed. In the test, the microcontroller was programmed to govern the DDS generating four symbols phase-modulated (8 bits of transmission) equispaced by a guard time -principles of OFDM. The carrier frequency chosen was 80 kHz.

In the test, there were generated the four QPSK constellations, starting at 45º. The duration of the symbol was 5ms, the guard time 10ms. Both timings are managed by the microcontroller; when times expire, the microcontroller sends the appropriate command to DDS: shut-down or wake up and generate signal with a particular phase. The figure 5 shows the SPI signals –chip select and data- together with the symbols generated.

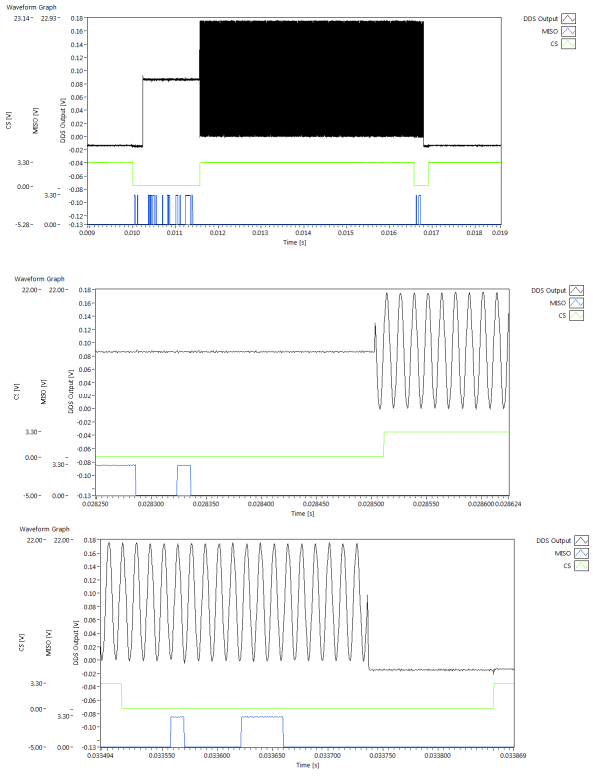

Fig. 6. Generated symbol in detail

Figure 6 shows a generated symbol in detail. Because the low frequency used in the SPI bus compared with DDS the master clock used 25MHz, the DDS starts before the chip select signal has released. It is a known time and has to be taken into account to control perfectly the time of symbol and the guard time.

V. CONCLUSIONS AND FUTURE WORK

On this paper a low cost transmitter for underwater sensor networks is presented. The solution proposed represents a new design perspective since OFDM symbol is generated in a synthesized form, avoiding IFFT computations.

The transmitter is able to change the carrier frequency in a simple way to adapt to the medium –channel equalization.

Related with OFDM, parameters such as carrier frequency, the time of the symbol, preamble and guard time are variables that can be easily modified by code, depending on the environment or communication features desired.

The power amplifier stage for the piezoelectric or projector can be done easily and at low cost using a power operational amplifier. The considerations for choosing a correct amplifier that works at low voltages are reduced to have a moderately fast slew rate and to remain stable when driving a large capacitive load.

For the moment, functionality tests have been developed. Currently, is being developed the complete software for the autonomous transmitter. On this upgrade, the microcontroller will use a look-up table to encode the data -acquired by the ADC- into blocks of phase commands to the DDS.

ACKNOWLEDGMENT

This work was supported by the Spanish Ministry of Economy and Competitiveness under the research project: "*Redes de sensores submarinos acústicos aplicados al seguimiento de especies de interés comercial*" (TRA2009_0294).

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