SRAM Stability Metric under Transient Noise

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***Abstract*— The conventional way to analyze the robustness of an SRAM bit cell is to quantify its immunity to static noise. The static immunity to disturbances like process and mismatch variations, bulk noises, supply rings variations, temperature changes is well characterized by means of the Static Noise Margin (SNM) defined as the maximum applicable series voltage at the inputs which causes no change in the data retention nodes. However, a significant number of disturbance sources present a transient behavior which is ignored by the static analysis but has to be taken in consideration for a complete characterization of the cell's behavior. In this paper, a metric to evaluate the cell robustness in the presence of transient voltage noise is proposed based on determining the energy of the noise signal which is able to flip the cell's state. The Dynamic Noise Margin (DNM) metric is defined as the minimum energy of the voltage noise signal able to flip the cell.**

Keywords-6T SRAM; data retention; dynamic robustness; voltage noise induced SRAM failures; energy metric

I. INTRODUCTION

Current nanometric IC processes need to assess the robustness of memories under any possible source of disturbance: process and mismatch variations, bulk noises, supply ring variations, temperature changes, aging and environmental aggressions such as RF or on-chip couplings. The noise margin is defined as the maximum disturbing signal that can be tolerated by a device when used in a system while still operating correctly. If the noise is a DC source a static noise margin is implied. If the noise is a time varying signal a dynamic noise margin is implied.

The static approach has been well researched over the years [1, 2, 3]. The metric used to evaluate the circuit's robustness to static noise is called Static Noise Margin. In this situation a series voltage noise is assumed. In the case of the 6T SRAM cell this translates in voltage noise sources at the inputs of the two crossed coupled inverters as shown in Fig. 1. Lohstroh J. in [4] defines the worst case static noise as the DC disturbance which is adversely present in all logic gates in an infinitely long chain of gates. Therefore, the Static Noise Margin of the SRAM cell is defined as the maximum amount of noise voltage that can be tolerated at the inputs of the crossed coupled inverters while the cell retains its data, assuming equal and opposite DC noise offsets. The worst case static series voltage, from now on referred to as Static Noise Margin (*SNM*), can be found graphically by drawing and mirroring the inverter Voltage Transfer Characteristics (VTC). The two curves have three intersection points, and the 'butterfly curve' is obtained. The Static Noise Margin is given by the side of the maximum square which can be inscribed in the wings of the butterfly.

While the DC voltage noises are smaller than the SNM, the butterfly curve is preserved, only its shape changes–in the sense that one of its wings becomes larger than the other. The extra noise that the cell can undertake without losing its state is given by the size of the maximum square that can be inscribed in the smaller wing of the butterfly. As a consequence, when the DC voltage noises are equal to the static noise margin ($|V_n|=SNM$) the smaller wing of the butterfly disappears and the two voltage transfer characteristics have, in this situation, only two intersection points. The cell is said to be at the verge of stability. At this point any extra perturbation no matter how small will cause the cell flip. Any noise larger than the static noise margin ($|V_n|>SNM$) will drive the voltage transfer characteristics further apart.

However, an important number of disturbance sources present a transient behavior. One of the most researched transient disturbances that can affect the SRAM behavior is α particle and neutron strike – single event upsets (SEU) causing soft errors [5]. Other transient disturbances like the ones caused by cross talks or inductive couplings should be taken in consideration too.

The noise margin is referred to as *Dynamic Noise Margin* if the cell is perturbed by a transient signal. Checking the robustness using dynamic noise margins requires time dependent analysis. The spectral and time dependent properties of the specific noise patterns should be considered. When a transient noise of given amplitude affects a sensitive node of the SRAM cell, the bistable feedback-driven nature of the cell determines whether the noise will be filtered or will evolve to eventually flip the state [4].

Because of the nonlinear cross coupling between the internal nodes of an SRAM cell, it is difficult to analytically characterize its dynamic behavior [6]. Since there is usually no analytical solution for a nonlinear system, the state space analysis is the most common technique of behavior analysis [7]. All the existing models for dynamic SRAM robustness analysis [6, 9, 10] are based on variable decoupling and piece-wise linearization.

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The same analysis is performed in [9 ,10] with the difference that the noise source is assumed to be a particle strike – single event upset (SEU) at the zero storing node, modeled as a double exponential function. The dynamic stability analysis in this approach is based on finding the critical charge, i.e. the minimum amount of charge required to be deposited by a particle strike in order to flip the SRAM state.

E. I. Vatajelu et al in [11] proposed a method for dynamic functionality margin estimation, based on the phase plane analysis. The authors present a new technique for *separatrix* approximation under random process variability. The technique is used to determine the probability of failure of an SRAM cell in read/write operation modes. A different approach has been taken in the analysis of the dynamic robustness of the 6T SRAM cell in data retention mode. An energy based metric has been proposed for robustness characterization in the presence of transient voltage pulses by E. I. Vatajelu et al in [12]. In this paper, the energy based method for SRAM dynamic analysis is described by means of phase plane representations and the validated by assuming a variety of transient voltage disturbances.

In the next section, the dynamic behavior of the bit cell is analyzed assuming voltage pulse noise sources affecting its internal nodes and the dynamic robustness metric is defined. In the third section, the new DNM metric is verified by proving its validity when different transient voltage disturbances affect the cell's behavior. In the fourth section different 6T SRAM designs are compared in terms of static and dynamic robustness. Finally, the fifth section concludes the work presented in this paper.

II. DYNAMIC NOISE MARGIN METRIC

The purpose of this paper is to analyze the SRAM cell robustness in data retention mode under the influence of transient voltage disturbances at the internal nodes (Fig. 1a). Due to its nature, the SRAM cell can be modeled by using the modified nodal analysis [7]. And taking into consideration also the voltage disturbances the SRAM cell is modeled by the nonlinear system:

$$C \cdot \begin{bmatrix} dV_R/dt \\ dV_L/dt \end{bmatrix} = \begin{bmatrix} I_R(V_R, V_L, V_n) \\ I_L(V_L, V_R, V_n) \end{bmatrix} \quad (1)$$

where (V_R, V_L) are the nodal voltages, (I_R, I_L) are the currents charging the capacitances C and V_n are the voltage disturbances. State-space and phase-space analyses are suitable for the characterization of such a nonlinear system.

State space refers to the space whose axes are the state variables. The state of the system can be represented as a vector within that space. A phase space is a space in which all possible states of a system are represented, with each possible state of the system corresponding to one unique point in the phase space. Nonlinear systems often have multiple steady-state solutions. Phase space analysis of nonlinear systems provides an understanding of which steady-state solution that a particular system will converge to. A phase portrait is a geometric representation of the trajectories of a dynamical system in the phase plane [7]. The phase portrait of the undisturbed SRAM cell in data retention mode, together with its steady-state solutions is illustrated in Fig. 1b.

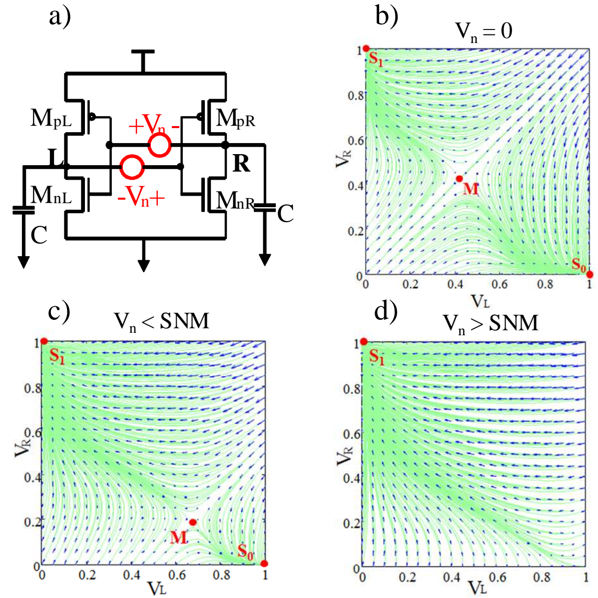


Figure 1 – SRAM cell analysis in data retention mode a) Simulation setup for dynamic robustness evaluation assuming voltage noise sources at the cell's internal nodes and phase portraits for b) undisturbed memory cell, c) cell disturbed by a noise lower than SNM, d) cell perturbed by a noise larger than SNM

The steady-state solutions, or equilibrium points, of an SRAM bit cell are obtained by solving the system (1) for $dV_R/dt = dV_L/dt = 0$. In this way the SRAM cell is found to have three equilibrium points: two stable (associated with the logic '0' – S_0 and with the logic '1' – S_1) and one unstable saddle point (metastable – M). These equilibrium points are also illustrated in Fig. 1.

While the phase portrait of a memory cell shows three steady-state solutions the cell is stable. Since the noise sources V_n affect directly the nodal voltages (V_R and V_L), the SRAM cell's phase portrait changes under their disturbing influence. While the noise V_n is smaller than the static noise margin (SNM) the SRAM cell remains stable. This can be seen by analyzing the resulting phase portrait (illustrated in Fig. 1c). The cell's trajectories converge to one of three points, two stable equilibrium points and one unstable similar to the unperturbed case. In fact the two stable equilibrium points are not affected by the noise, only the unstable one is. Depending on the noise polarity the unstable saddle point is pushed closer to one or the other equilibrium point. The larger the noise, the closer the metastable points gets to a stable point. When the noise level becomes equal to the SNM, the phase portrait shows only two steady-state solutions and when the noise is larger than SNM, only one steady-state solution remains (Fig. 1d).

According to the static approach, any noise larger than SNM will render the cell unstable. In practice, a noise larger than SNM can be sustained for a certain period of time before data cell occurs. Assuming the cell's internal nodes are perturbed by voltage pulse characterized by amplitude V_n and duration t_n the

pairs (V_n, t_n) which bring the cell to the verge of instability can be used to define the cell's dynamic robustness. For certain noise amplitude, critical noise duration (T_{crit}) can be defined as the minimum noise duration which causes a flip in the cell's state. The critical duration for each voltage pulse can be evaluated by using the phase portrait. The procedure for critical noise duration estimation in the phase plane is explained in detail in [12]. The critical pulse width as a function of noise pulse amplitude is illustrated in Fig. 2a. It can be observed that for small noises, approaching the Static Noise Margin (SNM) the critical pulse with asymptotically approaches infinity. On the other hand, for large noise amplitudes the critical pulse width approaches zero asymptotically.

Looking at this problem from a different perspective one can say that each disturbance transmits energy to the cell, and if this energy is high enough a data flip will be observed. Based on signal processing theory, the energy of a continuous time signal *x(t)* can be defined as [13]:

$$E_s = \int_{-\infty}^{\infty} |x(t)|^2 \, dt \qquad (2)$$

In the present analysis, since the applied noise is a continuous time signal, (2) can be written as:

$$E_{sn} = V_n^2 \cdot t_n \qquad (3)$$

where E_{sn} is the signal energy of the noise. Hence the signal energy of the critical noise pulse can be expressed as:

$$E_{s_crit} = V_n^2 \cdot T_{crit} \qquad (4)$$

The dependence of the signal energy of the critical pulse as a function of the noise amplitude is illustrated in Fig. 2b.

Stability analysis is concerned with identifying the minimum possible unintended violations that will destroy the data stored by the cell. Over the years, this minimum violation has been evaluated for the SRAM cell in terms of:

- *Voltage* (Static Noise Margin (SVM) [1-4], the Dynamic Noise Margin (DNM) [4], [8], [11])
- *Current* (static current noise margin (SINM) [14], critical charge (Q_{crit}) [5], [6])
- *Power* (the static power noise margin (SPNM) [14])

In the present work as in [12] the minimum unintended violation that will destroy the data stored by the cell is expressed in terms of *Energy*. The dynamic robustness metric of an SRAM cell in data retention mode is defined as the minimum signal energy of the voltage pulses able to flip the cell. In other words, the minimum signal energy among the critical signal energies:

$$DNM = min(E_{s_crit}) \qquad (5)$$

as illustrated in Fig. 2b. One can also say that the cell is robust to any noise whose signal energy is smaller than this value.

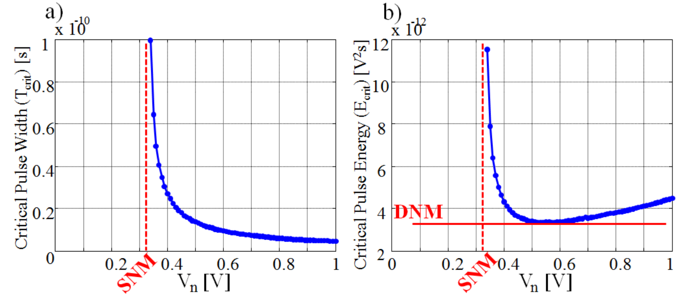


Figure 2 – a) Critical pulse width vs. noise amplitude for dynamic stability; b) Critical pulse energy vs. noise amplitude for dynamic stability.

Dissimilar to robustness metrics previously described, the minimum energy metric proposed here is not intended for absolute cell characterization, but rather as a method of comparative robustness assessment.

The next section presents an evaluation of the dynamic noise margin as the minimum signal energy required to flip a cell's state under the assumption of different transient voltage noises. The purpose of this evaluation is to demonstrate that:

- the *min(E_{s_crit})* metric is in fact an appropriate tool for comparative robustness assessment
- using a rectangular voltage pulse to emulate a transient disturbance on the cell's nodes is an appropriate approximation.

III. Proposed DNM Metric Validation

Since one can argue that a rectangular pulse shaped voltage noise is not a realistic assumption, the metric previously described is evaluated under different voltage noise shapes, namely rectangular, exponential and triangular. These noise sources have been considered in order to generalize and validate the proposed *min(E_{s_crit})* metric and they are illustrated in Fig. 3.

In these situations the critical time is no longer the pulse width, but the time factor (t_n) characterizing the critical pulses. For the completion of this analysis four different pulses have been defined: two exponential (with different frequencies), one symmetrical triangular and one exponential (double exponential). These noises are defined as:

- Rectangular – characterized by signal amplitude (V_n) and duration (t_n), the rise and fall regions are assumed instantaneous.

$$V_N(V_n, t_n) \qquad (5)$$

- Triangular – characterized by signal amplitude and (V_n) rise and fall times (τ_r and τ_f). In this case the rise time and the fall time are equal and their values are determined as half of the total noise duration (t_n).

$$V_N(V_n, \tau_r, \tau_f) \text{ with } \tau_r = \tau_f = t_n / 2 \qquad (6)$$

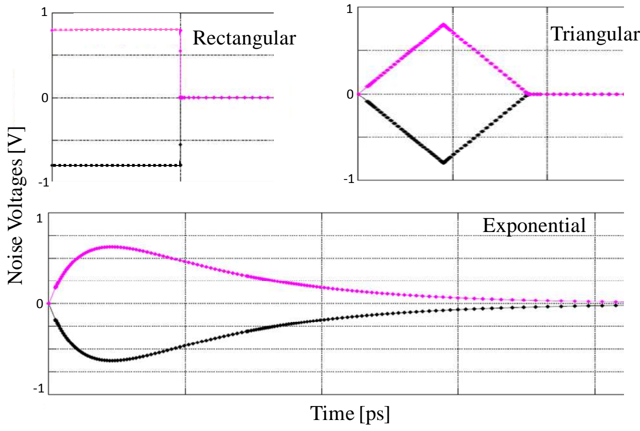


Figure 3 – Voltage noise shapes using to model the transient disturbance of the internal nodes of the SRAM cell.

- Exponential – composed of two exponential pulses, much like the current noise used to model the single event upsets. The difference is that in this case the noise is voltage and it is applied at the internal nodes of the cell. The exponential pulse is characterized by signal amplitude (V_n) and time constants (τ_1 and τ_2)

$$V_N(t) = V_n \cdot \left(exp\left(-t/\tau_1\right) - exp\left(-t/\tau_2\right)\right) \quad (7)$$

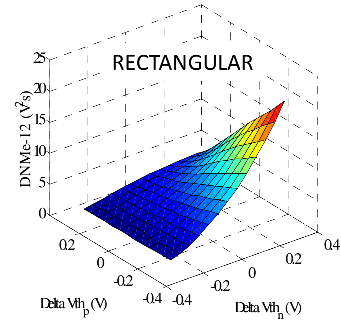
with $\tau_1 = 5 \cdot t_n$ and $\tau_2 = t_n$.

In order to determine the critical pulse, the noise amplitude is kept constant (like in the case where a rectangular pulse is used to model the noise at the internal nodes of the SRAM cell) and the duration factor (t_n) is increased until a state flip is observed in the SRAM cell in data retention mode. In this way, the critical duration factor is obtained ($t_{n\text{-}crit}$). The time required for the cell to flip its state under the disturbing influence of the critical pulse gives the critical time: T_{crit}.

The dynamic noise margin, as the minimum signal energy that can flip the cell´s state is obtained by integrating in time the square voltage pulse from the initiation of the noise until the state flip occurs, i.e. the critical time T_{crit}.

$$DNM = min(E_{s_crit}) = min\left(\int_0^{T_{crit}} V_N^2(V_n, \tau_{crit})dt\right) \quad (8)$$

In continuation the proposed DNM metric has been evaluated for a family of SRAM cells in order to demonstrate its utility in comparative robustness assessment. The SRAM cells used for this analysis have the same transistors sizes, but different transistor threshold voltages. Starting from a reference cell, the threshold voltage has been varied by ±30% for both PMOS and NMOS transistors. The simulations have been performed on SRAM cells designed using 45nm predictive technology model (PTM) transistors [15] in the HSPICE environment. Three models for the transient disturbance at the internal nodes are considered: rectangular voltage pulse, triangular voltage pulse and exponential voltage pulse. The three dimensional signal energy surfaces obtained by simulation are illustrated in Fig. 4.



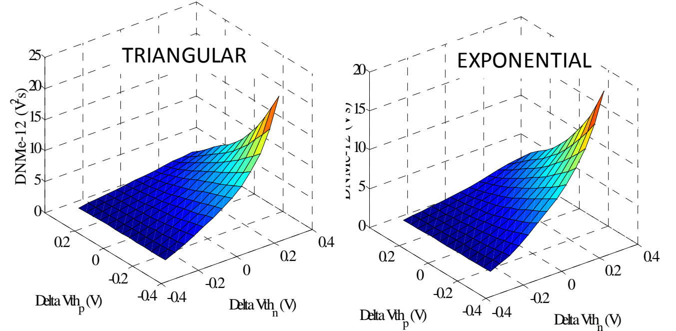


Figure 4 – Energy based metric for a set of different SRAM cells considering V_{TH} variations – rectangular, exponential and triangular pulses considered.

On the x axes of the three graphs is the threshold voltage variation of the two NMOS transistors, on the y axes is the threshold voltage variation of the two PMOS transistors, while on the z axes is the minimum energy signal which is able to flip the cell's state.

The signal energy surfaces have the same approximate shape, very similar maximum and minimum values, as it can be observed in Table 1 as well as in Fig. 4. This similitude between the minimum signal energy spectrums leads to the conclusion that the metric proposed in this paper is suitable to be used in comparative robustness assessment between SRAM cells.

In Table 1 the minimum and maximum values for the proposed DNM metric are included. The values have been obtained for the same combination of transistors' threshold voltage and are very similar. The minimum metric value has been obtained for the cell having the lowest threshold voltages and the values are around 1.25 signal energy units, with the larger value for the rectangular voltage pulse and the lowest for the triangular voltage pulse. The maximum metric value has been obtained for the cell having the highest values of transistor threshold voltages and the values are around 20 signal energy units. In this situation the higher value is again obtained for the rectangular pulse, while the lowest value is obtained for the exponential pulse.

Another information present in Table 1 is the value obtained for Kendall's Tau constant. This is a coefficient commonly used to measure the association between measured quantities. It is a measure of rank correlation, the similarity of the orderings of the data. In our particular case, Kendall's Tau gives a measure of the correlation, in terms of monotonicity between the data extracted using the different noise sources.

TABLE 1 – COMPARISON BETWEEN DATA EXTRACTED FROM SIMULATIONS USING THE THREE PROPOSED VOLTAGE NOISE SOURCES

Pulse Type	Rectangular	Triangular	Exponential
min (DNM) $10^{-12}[V^2s]$	1.36	1.15	1.22
max(DNM)$10^{-12}[V^2s]$	20.7	21.1	19.4
Tau kendall	1	0.99355	0.99421

The comparison is preformed against the data set obtained when the rectangular pulse is used. If this constant takes the value 1, there is perfect monotonicity correlation between data sets. Lower values represent lower correlation. The data presented in Table 1 include large values of Kendall's Tau, this means that there is a high correlation between the DNM metrics obtained using the different noise sources. This validates the proposed $min(E_{s_crit})$ metric for different voltage noise shapes as a suitable tool for comparative dynamic robustness assessment when different SRAM cells are analyzed.

In the next section, the robustness of different SRAM cells is compared using the proposed dynamic noise margin metric and the classical Static Noise Margin (SNM) metric.

IV. PROPOSED DYNAMIC NOISE MARGIN VS. STATIC NOISE MARGIN

Traditionally, the Static Noise Margin is used to determine the robustness of an SRAM cell and also to compare different SRAM designs in terms of robustness. In this work the defined metric has also been included in the comparison of different cells. The studied cells are designed in 45nm PTM technology [14]. Assuming different cells with different threshold voltages, and different cells with different dimensions, their robustness has been compared both statically and dynamically. The comparison has been performed against a reference cell. The reference cell is considered the one with zero variation in transistor width and transistor threshold voltage respectively.

In Fig. 5 the relative static and dynamic robustness metrics are illustrated as contour levels for a family of SRAM cells, with different transistor widths.

The left side figure represents the relative static noise margins. All the cells on the black line have the same static noise margin as the reference cell. The blue contours represent cells with lower static robustness while the red contours represent the cells with higher robustness then the reference cell. However the static robustness variation is small over the entire design space in Fig. 5. The minimum SNM is 6% smaller than the one of the nominal cell and the maximum SNM is 4% larger than to one of the reference cell. This results in a 10% variation over the entire assumed design space.

The right side figure represents the relative dynamic noise margins. All the cells on the black line have the same dynamic noise margin as the reference cell. The contours above the black line represent cells with lower dynamic robustness while the contours below the black line represent the cells with higher robustness then the reference cell. In this case, of transient disturbances, dynamic robustness variation is large over the entire design space in Fig. 5. The minimum DNM is 10% smaller than the one of the nominal cell but the maximum DNM is 85% larger than to one of the reference cell. This results in a 95% variation over the entire assumed design space.

This high discrepancy between the static and dynamic noise margin metrics emphasizes the need for the proposed dynamic metric. While in a static analysis there is practically no difference between the maximum and minimum obtained values, in a dynamic analysis a high variation is observed.

In Fig. 6 the relative static and dynamic robustness metrics are illustrated as contour levels when transistors threshold voltages are changed when compared to the reference cell. The dashed lines represent the relative static noise margin contours, while the continuous lines represent the relative dynamic robustness contours. All the cells on the red dashed line have the same static noise margin as the reference cell, and the ones on the continuous red line have the same dynamic noise margin as the reference cell.

When compared to the reference cell, two situations can be identified:

- The static and dynamic robustness metrics are consistent (they both show an increase/decreased robustness compared to the reference cell) for all the cells in the white regions of Fig. 6.
- The static and dynamic robustness metrics are inconsistent (one of the metrics shows increased robustness while the other shows decreased robustness when compared to the reference cell) for all the cells in the shaded regions of Fig. 6.

In the inconsistency scenario again two situations can be observed when compared to the reference cell

- The static metric shows a decrease in robustness, while the dynamic metric shows an increase (the cells in the light grey areas)
- The static metric shows an increase in robustness, while the dynamic metric shows a decrease (the cells in the dark grey area)

From these inconsistencies the need of dynamic robustness analysis is apparent. Since a significant number of disturbance sources present a transient behavior, a dynamic noise margin metric is very useful in conjunction with the static noise margin metric for a more complete understanding of the SRAM cell robustness.

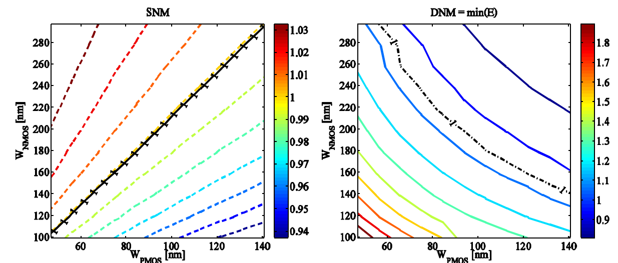


Figure 5 – relative static and dynamic noise margins of different SRAM cells for different transistor widths.

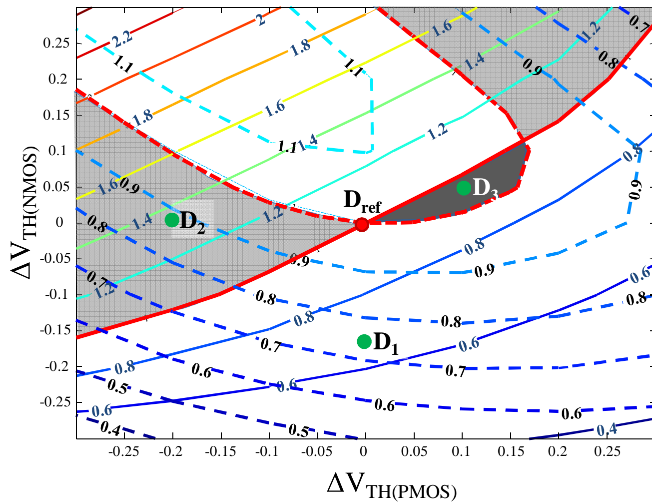


Figure 6 – Contour levels of relative static and dynamic robustness metrics: continuous lines are used to illustrate the relative dynamic metric while dashed lines are used to illustrate the relative static metric. The red circle represents the reference cell (D_{ref}).

V. CONCLUSIONS

In order to characterize an SRAM cell in terms of dynamic noise robustness, a DNM metric has been proposed. It is based on the energy of the noise pulse and is defined as the minimum energy of the voltage pulses able to flip the cell.

The application of the DNM metric allows the determination of the resilience of a cell to dynamic noise. A method to estimate the DNM has been proposed based on evaluating the critical pulse duration of a certain voltage noise pulse. The DNM is given by the minimum energy pulse achieving to flip the cell causing a failure.

The proposed metric has been used to evaluate the dynamic robustness of SRAM cells in data retention modes assuming different voltage noise shapes affecting the internal nodes. This is done in order to generalize and validate the proposed metric. Using Kendall's tau constant the monotonicity correlation between the data sets is demonstrated, proven that the proposed metric can be used over a range of voltage noise pulse shapes, not only when rectangular pulses are assumed.

Examples of application of the metric (DNM) in different cells show the advantage of using the DNM metric to assess the robustness of the cell and its resilience to failures caused by dynamic voltage noise.

REFERENCES

[1] E. Seevinck, F. J. List, and J. Lohstroh, "Static-noise margin analysis of MOS SRAM cells," Journal of Solid-State Circuits, pp. 748–754, 1987

[2] S. Mukhopadhyay, Q. Chen and K. Roy, "Memories in scaled technologies: a review of process induced failures, test methodologies and fault tolerance," Design and Diagnostics of Electronic Circuits and Systems (DDECS), pp. 1–6, April 2007

[3] E I Vatajelu, J Figueras, "Supply voltage reduction in SRAMs: Impact on Static Noise Margins," IEEE International Conference on Automation, Quality and Testing, Robotics, 2008., vol.1, pp.73-78.

[4] J Lostroh, "Static and Dynamic Noise Margins of Logic Circuits," IEEE Journal of Solid-State Circuits, vol. 14, no. 3, pp. 591-598, June 1979

[5] D Leroy, R Gillard, E Schaefer, C Beltrando, S-J Wen, R Wong, "Variation of SRAM alpha-induced soft error rate with technology node", IEEE Internaltional On-Line Testing Symposium, 2008, pp. 253-257

[6] B Zhang, A Arapostathis, S Nassif, and M Orshansky, "Analytical modeling of SRAM dynamic stability," in International Conference on Computer Aidded Design, San Jose, 2006, pp. 315-322.

[7] H K Khalil, Nonlinear Systems, 3rd ed.: Prentice Hall, 2001.

[8] Y Zhang, P Li, and G M Huang, "Separatrices in high-dimensional state space: system-theoretical tangent computation and aplication to SRAM dynamic stability analysis," in Proceedings of Design Automation Conference (DAC), Anaheim, 2010, pp. 567-572.

[9] R Garg, P Li, and S P Khatri, "Modeling dynamic stability of SRAMs in the presence of single event upsets (SEUs)," in International Symposium on Circuits and Systems, 2009, pp. 1788-1791

[10] R Nasser, Y Boulghassoul, J Draper, S DasGupta and A Witulski, "Critical charge characterization for soft error rate modeling in 90nm SRAM," in International Symposium on Circuits and Systems, 2007, pp.1879-1882

[11] E I Vatajelu, G Panagopoulos, K Roy and J Figueras, "Parametric failure analysis of embedded SRAMs using fast & accurate dynamic analysis," IEEE European Test Symposium (ETS), 2010, pp. 69-74

[12] E I Vatajelu, A Gomez-Pau, M Renovell and J Figueras, "Transient Noise Failures in SRAM Cells: Dynamic Noise Margin Metric," IEEE Asian Test Symposium (ATS), 2011, pp. 413-418

[13] J G Proakis and D K Manolakis, "Digital Signal Processing", Prentice Hall, Fourth Edition, 2006.

[14] C Wann et al., "SRAM cell design for stability methodology," in *IEEE International Symposium on VLSI-TSA*, 2005, pp. 21-22.

[15] Predictive Technology Model: http://ptm.asu.edu/.