Voltage Balancing Method for the Multilevel Flying Capacitor Converter Using Phase-Shifted PWM

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***Abstract*—In flying capacitor (FC) converters, phase-shifted pulse-width modulation (PS-PWM) provides natural voltage balancing. However, for a practical application, a more robust balancing mechanism of maintaining the FC voltages at the desired values is required. This paper proposes a new closed-loop voltage balancing method for multilevel FC converters using PS-PWM. The proposed method balances the voltages of the FCs by modifying the duty cycle of each switch of the FC converter using a proportional (P) controller. The crossed effect between FC currents and duty cycles is considered and is used for FC voltage balancing. The Simulation results verify that the proposed voltage balancing method is very robust to different operating conditions, such as load transients and non-linear loads.**

***Keywords*-Multilevel converter; Flying capacitor (FC) converter; Capacitor voltage balancing; Phase-shifted pulse width modulation (PS-PWM).**

I. INTRODUCTION

In high-power applications the conventional two-level voltage source converter (VSC) does not provide optimum system performance and efficiency. One solution is to use multilevel VSCs that allow high power and voltage/current ratings, low total harmonic distortion and low losses [1]. Among the multilevel converter topologies, the most popular ones are the cascaded multi-modular converter [2], the diode-clamped converter (DCC) also called neutral-point-clamped (NPC) converter [3], and the flying capacitor (FC) converter [4].

Among these multilevel converters, the FC converter has attracted a great deal of interest because of its easier extension to converters of a higher number of levels (n>3), as compared to its counterpart, the NPC converter. This is due to the difficulties of achieving capacitor voltage balance in an NPC converter of a high number of levels. Nevertheless, there are some issues in the FC converter which need to be considered during the design stage, such as the initial FC charging process, capacitor voltage ripples, and voltage imbalance of the FCs.

Voltage ripples play an important role in sizing the capacitors used in the FC converter topology. A practical interest nowadays is to reduce the capacitor values in order to decrease the physical size of the system. Besides that, using smaller capacitance values can enable the use of thin film capacitors [5], which have lower losses and provide higher reliability as compared to electrolytic capacitors [6]. On the other hand, the use of small capacitors will produce larger voltage imbalances that may risk the integrity of the FCs and the switches of the power converter. Furthermore, the quality of the output voltages becomes deteriorated. Nevertheless, the FC voltage ripples could be reduced by using an appropriate modulation method [7] along with a proper FC voltage balancing method. Hence, it is very necessary to design a proper voltage balancing method, which would not only produce less voltage ripples but also ensure safe and secure operation of the power devices.

There are many voltage balancing approaches in the literature for the FC converter used in different applications. The balancing methods presented in [8] and [9] use phase disposition pulse-width modulation (PD-PWM). Natural voltage balance is achieved based on the carrier rotation for different switches. However, it is only valid under certain load conditions. Furthermore, the control becomes more complex for converters with a higher number of voltage levels, as different triangular functions for individual switches have to be arranged at different voltage levels. In [10], another natural balancing method was discussed using phase-shifted pulse-width modulation (PS-PWM). In [11], a study of the multilevel FC converter is conducted in frequency domain. A passive RLC filter is used to enhance the voltage balancing process of the FCs. The solution seems to be good, as it does not require any voltage sensors. However, using RCL filter produces extra power losses and increases the cost of the system. In addition to that, the balancing process slows down with dynamic load conditions. A similar study was conducted in [12] and [13], using time domain analysis. The voltage balancing methods discussed in [8]-[13] use open loop strategies and are mostly based on the modification of the carrier phases in PD-PWM and PS-PWM. The FC voltages, however, fail to retain their desired level when there are disturbances due to nonlinearities or asymmetries in the system. Therefore, an active compensation based on a feedback control algorithm is required to balance the FC voltages.

There are several approaches using the feedback control algorithm discussed in [14]-[20]. In [14], a closed loop control strategy based on a linearization method is used for balancing the capacitor voltage for dc-dc converters; however no work has been reported on dc-ac converter systems. In [15], the proposed balancing method is based on the addition of a small square wave to the modulation; however, this method disturbs the output voltage. In [16], the balancing algorithm uses redundant switching states to adjust the switching time along

with a proportional integral (PI) controller. In that case, the controller parameters need to be tuned for different operating conditions to achieve optimal performance and moreover it affects the output voltage. In [17]-[19], the balancing algorithms are based on the evaluation of the cost functions. Space-vector modulation (SVM) is used in [17], while a similar voltage balancing algorithm is implemented using PD-PWM in [18] and [19]. The particular redundant switching state [18] or sequence [19], that provides the minimum value of the cost function, is selected at any switching period. This voltage balancing method seems to be very effective since it provides fast voltage balancing dynamics. However, it produces larger voltage ripples as compared to PS-PWM [7]. Finally, in [20], a PI controller is used to compensate for the voltage errors in the FCs using PD-PWM. However, the control becomes difficult for converters with a high number of levels. The authors suggest delaying the measured capacitor voltage signals to regulate the FC voltages, yet this method is based on a trial and error strategy.

The majority of the solutions described above are complex, require significant processing time to achieve voltage balancing, and deteriorate the output voltage quality. The objective of this paper is to present a novel voltage balancing method for the FC capacitor converter that is very efficient and can be easily extended to any number of levels. It is implemented using PS-PWM and is based on a proportional (P) controller. The effects between the FC currents and the duty cycles of the switches are identified and used for voltage balancing. The proposed approach is relatively simple to implement in any multilevel FC converter application. Furthermore, the voltage balancing dynamic performance is very good. Although the proposed method has been applied to the five-level FC converter system, it can be easily extended to an FC converter with any number of levels.

The rest of the paper is organized as follows. Section II describes the operating principle of a FC converter. Section III explains the proposed FC voltage balancing method. Section IV presents the simulation results on a five-level FC topology to verify the effectiveness of the proposed voltage balancing method. Finally, the conclusions are summarized in Section V.

TABLE I

FIVE-LEVEL FC CONVERTER: VOLTAGE LEVELS, FC CURRENTS, AND SWITCHING STATES

Output Voltage Level (v_{x0})		Switching States					FC Currents			FC Voltages		
		s_{x4}	s_{x3}	s_{x2}	s_{x1}	*St.#*	i_{Cx3}	i_{Cx2}	i_{Cx1}	v_{Cx3}	v_{Cx2}	v_{Cx1}
5	V_{dc}	1	1	1	1	{15}	0	0	0	x	x	x
4	$3V_{dc}/4$	1	1	1	0	{14}	0	0	i_x	x	x	↑
		1	1	0	1	{13}	0	i_x	$-i_x$	x	↑	↓
		1	0	1	1	{11}	i_x	$-i_x$	0	↑	↓	x
		0	1	1	1	{7}	$-i_x$	0	0	↓	x	x
3	$V_{dc}/2$	1	1	0	0	{12}	0	i_x	0	x	↑	x
		1	0	1	0	{10}	i_x	$-i_x$	i_x	↑	↓	↑
		0	1	1	0	{6}	$-i_x$	0	i_x	↓	x	↑
		1	0	0	1	{9}	i_x	0	$-i_x$	↑	x	↓
		0	1	0	1	{5}	$-i_x$	i_x	$-i_x$	↓	↑	↓
		0	0	1	1	{3}	0	$-i_x$	0	x	↓	x
2	$V_{dc}/4$	1	0	0	0	{8}	i_x	0	0	↑	x	x
		0	1	0	0	{4}	$-i_x$	i_x	0	↓	↑	x
		0	0	1	0	{2}	0	$-i_x$	i_x	x	↓	↑
		0	0	0	1	{1}	0	0	$-i_x$	x	x	↓
1	0	0	0	0	0	{0}	0	0	0	x	x	x

Note: The charging/discharging effects in the FC are given assuming that i_x is positive (i_x>0) with the following notation:
↑ => Capacitor voltage is charging
↓ => Capacitor voltage is discharging
x => No change in the capacitor voltage

II. OPERATING PRINCIPLES OF THE FC CONVERTER

Fig. 1 shows a schematic diagram of a three-phase five-level FC VSC, in which three FCs are integrated in each phase. During normal operation, the mean voltage values of the FCs C_{x1}, C_{x2}, and C_{x3}, should be maintained at $V_{dc}/4$, $V_{dc}/2$, and $3V_{dc}/4$, respectively, where the subscript 'x' is used for the phase identification x={a, b, c}, and 'V_{dc}' is the voltage of the dc bus. Consequently, the voltage across each switch is only one quarter of the dc-link voltage. The switch control function is defined as s_{xy}, where the subscript 'x' is used for phase

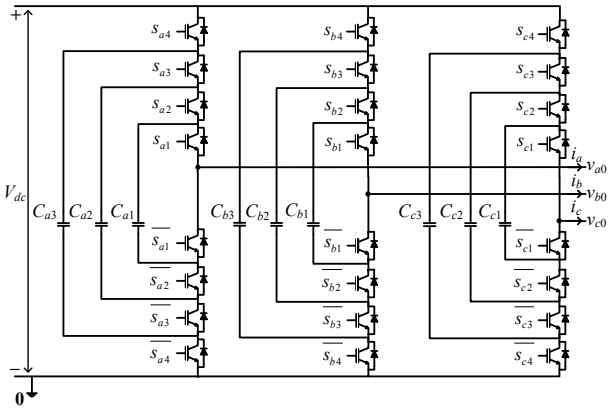

Fig. 1. Circuit diagram of a five-level FC VSC.

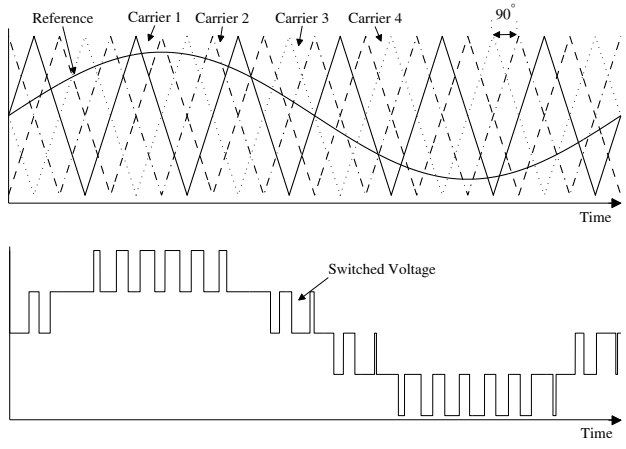

Fig. 2. Five-level PS-PWM carrier disposition and switched phase voltage.

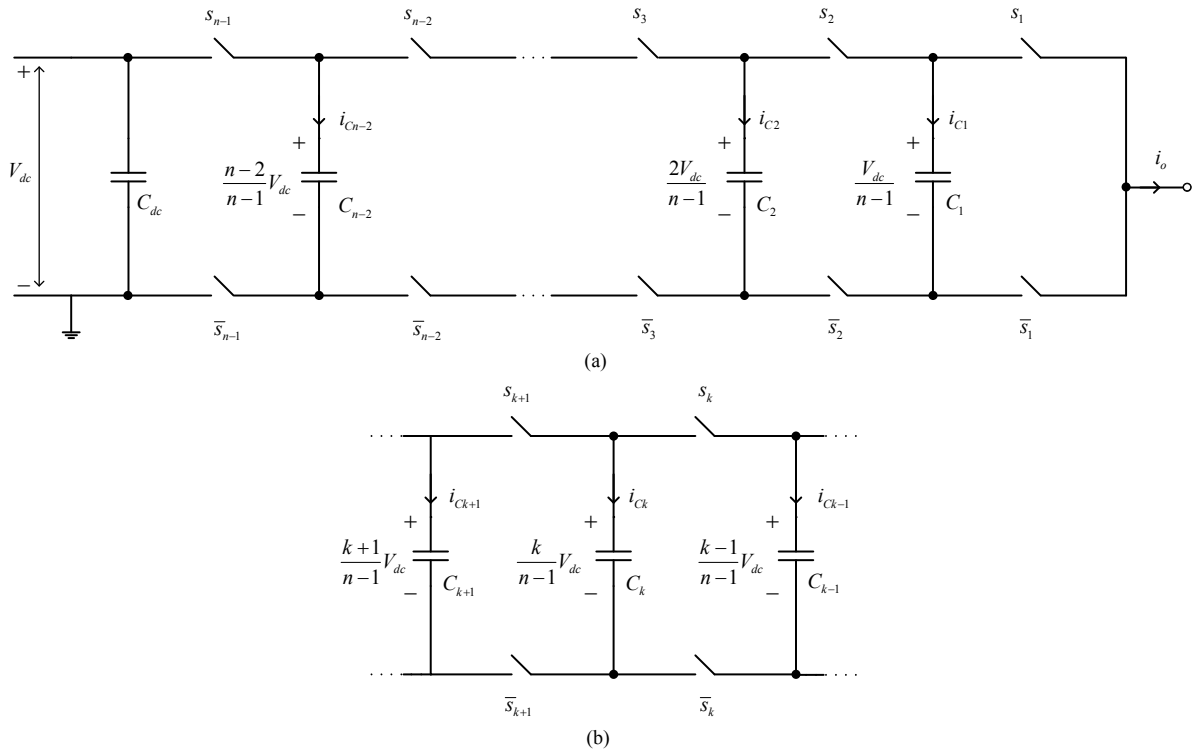

Fig. 3. One leg of a FC converter: (a) General *n*-level cell imbricated chain representation and (b) a section of the chain.

identification, and '*y*' defines the particular switch in the phase leg of the FC converter (y={1,…,4}). The switch control functions can take two values s_{xy}={0,1}, meaning "0" and "1" that the switch is off and on, respectively. The switch pairs in each phase leg $s_{x1}-\overline{s}_{x1}, s_{x2}-\overline{s}_{x2}, s_{x3}-\overline{s}_{x3}$, and $s_{x4}-\overline{s}_{x4}$ operates in a complementary manner.

Each phase can generate five output voltage levels. Taking the dc negative rail as a reference, the potential output voltage levels are 0, V_{dc}/4, V_{dc}/2, 3V_{dc}/4, and V_{dc}. Using Kirchhoff's voltage and current laws, the line-to-ground voltage v_{x0} and the currents through the FCs (i_{Cx1}, i_{Cx2} and i_{Cx3}) can be written as:

$$v_{x0} = s_{x4}V_{dc}+(s_{x3}-s_{x4})v_{Cx3}+(s_{x2}-s_{x3})v_{Cx2}+(s_{x1}-s_{x2})v_{Cx1}, \quad (1)$$

$$i_{Cx1} = (s_{x2}-s_{x1})i_x, \quad (2)$$

$$i_{Cx2} = (s_{x3}-s_{x2})i_x, \text{ and} \quad (3)$$

$$i_{Cx3} = (s_{x4}-s_{x3})i_x. \quad (4)$$

Based on (1)-(4), the line-to-ground output voltage and FC currents are determined for all switching states and shown in Table I. The switching states are indicated by binary notation representing the control functions of the upper switches of the leg. It can be seen in this table that the redundant switching states for the voltage levels V_{dc}/4, V_{dc}/2, and 3V_{dc}/4 define different current paths through the FCs, which helps to

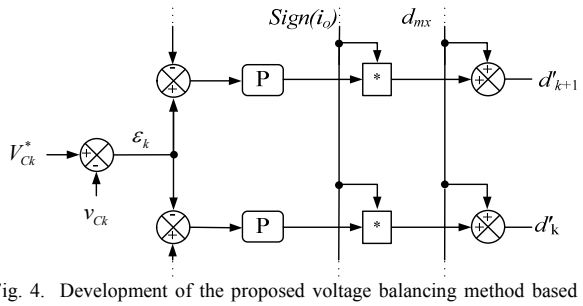

Fig. 4. Development of the proposed voltage balancing method based on (6).

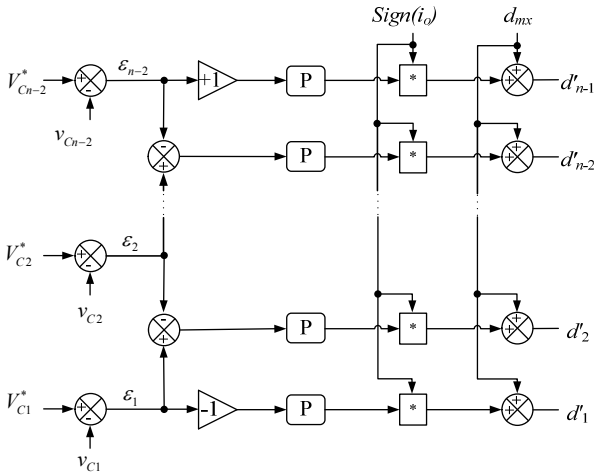

Fig. 5. Proposed voltage balancing method for n-level FC converter.

achieve voltage balance.

Fig. 2 shows a PS-PWM method for a five-level VSC. For this converter, the PS-PWM requires four carriers of the same amplitude and frequency, which are phase shifted to one another by 90°. A reference sinusoidal modulation signal is compared with all four triangular carriers to define the voltage level that has to be generated at the output. Using this method, natural voltage balancing can be achieved. However, this natural voltage balancing is usually slow and depends on the loading conditions. Therefore, an active balancing method may still be required to regulate the FC voltage at their desired level with improved dynamics under transient conditions and nonlinear loads.

III. Proposed Voltage Balancing Method

Fig. 3(a) shows a general *n*-level FC converter leg. The proposed voltage balancing method is developed based on analyzing a particular cell section of FC converter as shown in Fig. 3(b). According to (2)-(4) the current through a capacitor is represented by:

$$i_{Ck} = (s_{k+1} - s_k) i_o. \tag{5}$$

It can be observed that the current through a capacitor is affected by the control signals associated to the two adjacent switches. The locally-averaged representation of the capacitor current in (5) is calculated over a switching period and is shown in (6):

$$\overline{i_{Ck}} = (d_{k+1} - d_k)\overline{i_o}, \tag{6}$$

where '$\overline{i_{Ck}}$' and '$\overline{i_o}$' are the locally-averaged currents of the capacitor 'C_k' and the output current, respectively. 'd_{k+1}'and 'd_k' are the duty cycles of the switch 's_{k+1}'and 's_k', respectively.

Assuming a positive output current (i_o>0), equation (6) shows that by increasing the duty cycle d_{k+1} will increase the locally-averaged current through the capacitor, whereas the opposite effect will be produced if d_k is increased. If the voltage of the capacitor C_k is greater than its reference value, a negative current should be imposed to this capacitor. Therefore, the duty cycles d_k and d_{k+1} should be increased and decreased, respectively. On the other hand, if the output current is negative (i_o<0), the duty cycles should be manipulated in the opposite direction to accomplish voltage balance. Based on this analysis, the voltage balancing method is develop and shown in Fig. 4. The complete method for a general *n*-level FC converter is shown in Fig. 5.

TABLE II
Flying Capacitor Converter Parameters

Circuit Parameter	Value
DC Link Voltage	200 V
Flying Capacitors	100 µF
Load Resistance	40 Ω
Load Inductance	4 mH
Carrier Frequency	2 kHz
Fundamental Frequency	50 Hz
Control Parameter (*P*)	0.03

The voltage balancing dynamic of a general capacitor C_k can be analyzed based on the following equations:

$$\overline{i_{Ck}} = C_k \frac{d\overline{v_{Ck}}}{dt} \Leftrightarrow \frac{d\overline{v_{Ck}}}{dt} = \frac{\overline{i_{Ck}}}{C_k}. \tag{7}$$

From (6) and (7), one can obtain:

$$\frac{d\overline{v_{Ck}}}{dt} = \frac{\overline{i}_o (d'_{k+1} - d'_k)}{C_k}, \tag{8}$$

where,

$$d'_{k+1} = d_{k+1} + \Delta d_{k+1}, \tag{9}$$

$$d'_k = d_k + \Delta d_k, \text{and} \tag{10}$$

$$d_k = d_{k+1} = d_{mx}, \tag{11}$$

'd'_{k+1}' and 'd'_k' are the final duty cycles of the corresponding switches.

Assuming small variation around the operating point, using (9), (10) and (11) in (8), we obtain:

$$\frac{\Delta\overline{v_{Ck}}}{\Delta t} = \frac{\overline{i}_o (\Delta d_{k+1} - \Delta d_k)}{C_k}. \tag{12}$$

The variations of the duty cycles are given by a proportional controller, as follows:

$$\Delta d_{k+1} = (\varepsilon_k - \varepsilon_{k+1}) P, \text{and} \tag{13}$$

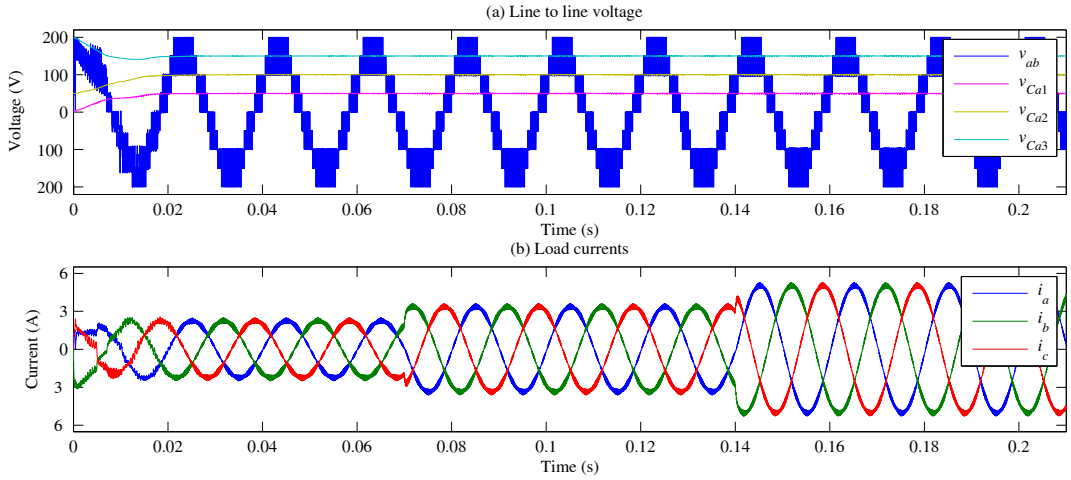

Fig. 6. Five-level FC converter under different load condition: (a) a line-to-line voltage 'v_{ab}' and FC voltages of phase 'a', and (b) three phase load currents.

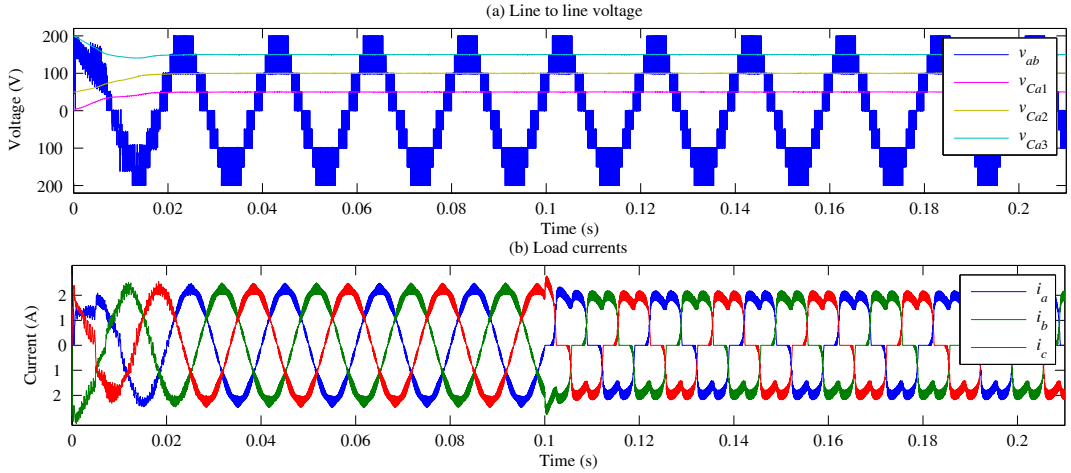

Fig. 7. Five-level FC converter under non-linear load condition: (a) line-to-line voltage 'v_{ab}' and FC voltages of phase 'a', (b) three phase load currents.

$$\Delta d_k = (\varepsilon_{k-1} - \varepsilon_k)P, \tag{14}$$

where 'ε_{k-1}', 'ε_k', and 'ε_{k+1}' are the voltage errors in the capacitors C_{k-1}, C_k, and C_{k+1} , respectively, and 'P' is the proportional control parameter.

Substituting (13) and (14) in (12):

$$\frac{\Delta \bar{v}_{ck}}{\Delta t} = \frac{\bar{i}_o P(2\varepsilon_k - \varepsilon_{k+1} - \varepsilon_{k-1})}{C_k}. \tag{15}$$

Equation (15) defines the balancing dynamic of the proposed voltage control and can be used to optimize the controller gain parameter (P) to achieve a satisfactory system performance.

IV. Simulations Results

In this section, the proposed voltage balancing method is applied to the five-level FC VSC from Fig. 1. The system has been simulated using the MATLAB/Simulink [21] environment, and the models of the FC VSC have been implemented using PLECS Toolbox [22]. The parameters of the converter system are shown in Table II.

The dynamic response provided by the proposed voltage balancing control method is shown in Fig. 6. In this simulation, the initial capacitor voltages were V_{Ca1}=0V, V_{Ca2} =50V and V_{Ca3}=200V, and regulated to the desired voltages, i.e. 50V, 100V, and 150V, respectively. Observe that the capacitor voltages reach their reference values in about 20 ms. Once in steady state condition, there is a step change in the load (resistor changes from 40 to 27 ohms) at t=70 ms, and later, at t=140 ms, the load resistance changes from 27 to *18* ohms. Observe that during the transients the voltages on the FC remain unaffected. Hence, the proposed voltage balance control proves to be robust not only in the steady state but also under dynamic operating conditions.

Fig. 7 shows the behavior of the system operating over a non-linear load. The simulation starts with the same linear load used in Fig. 6 (an R-L load). At the instant t=100 ms, the linear load is disconnected and a three-phase diode rectifier is connected instead, with a dc-side load capacitor and resistor of 10 µF and 80 Ω, respectively. It can be noted that the voltages in the FCs are maintained at their reference values even when the load becomes such a strong non-linear one. Thus the proposed voltage balancing method proves to be robust even under this particular non-linear load operation.

V. Conclusion

This paper proposed a new voltage balancing method for FC converters operating with PS-PWM. The method has been formulated for a general number of levels (n) and tested on a five-level FC converter. The proposed method is based on a proportional controller which is able to remove the steady-state errors. This is because when the capacitor voltages are at their reference values, i.e. the voltage errors are zero, no control action is required. The proposed method can regulate the FC capacitor voltages to their reference values and maintains the quality of the output voltages, even under transient load conditions and non-linear loads.

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