

# Voltage Balancing Strategy for a Five-level Flying Capacitor Converter Using Phase Disposition PWM with Sawtooth-Shaped Carriers

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**Abstract-** The flying capacitor (FC) multilevel converter has attracted a great deal of interest in the recent years because of its easier extension to converters of a higher number of levels ( $n>3$ ), as compared to its counterpart the diode-clamped converter (DCC). This is due to the difficulties of achieving capacitor voltage balance for the DCC. On the other hand, the voltages in the flying capacitors of the FC converter can be controlled thanks to the availability of redundant switching states. The main focus of this paper is to develop a voltage balancing scheme for a five-level FC converter based on phase disposition pulse-width modulation (PD-PWM). Since there are multiple states that produce the same output voltage at the leg of the converter, such a redundancy is used to regulate the FC voltages at their desired levels. The selection of the optimal states is performed by minimizing a cost function. A drawback observed when using standard symmetrical triangular carriers for the PD-PWM, is the additional switching events that are produced due to transitions within the same voltage level. Nevertheless, this fact can be avoided by using sawtooth carrier waveforms instead. Simulation results for the sawtooth carriers show a reduction of the switching frequency of about 20% as compared to the use of standard triangular carriers while maintaining the FC voltage balance. Moreover, by analyzing the results, it can be seen that the proposed PD-PWM voltage balancing scheme is robust to static and dynamic loading conditions.

## I. INTRODUCTION

Due to recent advances in semiconductor devices, the interest of using voltage source converters (VSCs) have significantly increased for high power/voltage applications [1]. However, the conventional two-level VSC fails to meet optimum system performance and efficiency such as filter size, losses, total harmonic distortion (THD), etc. The solution to improve performance and efficiency for high voltage systems is the use of multilevel VSCs that allow high power handling capability with reduced harmonics and lower switching losses [2]. Among the multilevel converter topologies, the most popular ones are the cascaded multimodular converter [3], the diode-clamped converter (DCC) [4] and the flying capacitor (FC) converter [5]. The three-level DCC is also known as Neutral-Point-Clamped (NPC) converter.

The main challenge associated with multilevel converters is the voltage balancing of the individual capacitors. Although the NPC topology has been widely used by industry, the main issue with this topology is the proper regulation of the

neutral-point (NP) potential. The NP voltage maintains balance in the steady state as long as the average current injected into the NP is zero. Yet, still some current deviations may be seen when looking over a switching period; hence appearing some low-frequency NP voltage oscillations. Some modulation strategies can avoid such ripples [6], but they increase the switching frequency in the power devices and the distortion in output voltages. Furthermore, the voltage balancing control of  $n$ -level DCC topologies with a high number of levels ( $n>3$ ) becomes complex and impractical.

In the three-level FC converter, the control of the voltages in the flying capacitors is relatively simple; it can be performed independently per each phase by simply alternating the available two redundant switching states. A similar voltage balancing technique can be applied to FC topologies with a higher number of levels ( $n>3$ ). However, in this case there are more redundant states to deal with, and also more flying capacitors to be controlled. Each redundant state produces different effects on the capacitor voltages. Subsequently, controlling the voltages across the capacitors becomes a challenge.

The balancing schemes listed in [7], [8] are based on rotating the carriers for different switches and are valid only under certain load conditions. Moreover, the control becomes more complex for converters with a higher number of voltage levels, as different triangular functions for individual switches have to be arranged at different voltage level. In [9], the natural balancing effect was discussed using phase-shifted pulse-width modulation (PS-PWM), and in [10] the addition of a passive filter was used to boost the voltage balancing process of the flying capacitors. The voltage balancing schemes discussed in [7]-[10] use open loop strategies and are mostly based on modifying the carrier phases in PS-PWM. The flying capacitor voltages, however, fail to retain its desired level when there are disturbances due to nonlinearities or asymmetries in the system. Therefore, additional compensation based on a feedback control algorithm is required to balance the FC voltages.

There are several approaches using the feedback control algorithm discussed in [11]-[15]. They are based on changing the switching pattern for the control of FC voltages. In [13], the algorithm uses redundant switching states to adjust the time of the switching function; however, the algorithm is

based on phase-shifted pulse-width modulation (PS-PWM) which is spectrally sub-optimal. In [14], the voltage balancing control is based on space-vector modulation (SVM) by selecting the appropriate redundant switching states. This voltage balancing scheme seems to be very effective. The authors however do not perform any switching frequency analysis for the proposed voltage balancing strategy and neither they have evaluated the spectrum of the output voltages. Finally, in [15] a proportional-integral (PI) controller is used to compensate for the voltage errors in the flying capacitors. However, the dynamic of the system for balancing capacitor voltages is slower using PI controllers than by selection of optimal redundant states in the modulation [14]. Furthermore, tuning of the PI parameters is required [16], and it becomes difficult for converters with a high number of levels. Additionally, for converters with a number of levels higher than three ( $n>3$ ) the authors in [15] suggest delaying the measured capacitor voltage signals to regulate the flying capacitor voltages, yet this scheme is based on a trial and error strategy.

The majority of the solutions discussed above do not analyze the effect of the voltage balancing schemes on the switching frequencies in the power devices. This paper is focused on the capacitor voltage balancing analysis and the switching frequency evaluation of a five-level FC converter. The PD-PWM is applied and the voltage balance is performed by a proper selection of redundant switching states by using a cost function. The switching frequencies of the power devices are evaluated for two kinds of PWM carriers; triangular and sawtooth waveforms. The analysis shows that by using sawtooth carriers, a significant reduction in the switching frequencies can be achieved. The quality of the line-to-line output voltage is analyzed in terms of fast Fourier transform (FFT) and THD for the two carrier waveforms.

The rest of the paper is organized as follows. Section II describes the operating principle of a five-level FC converter. Section III explains the proposed FC voltage balancing

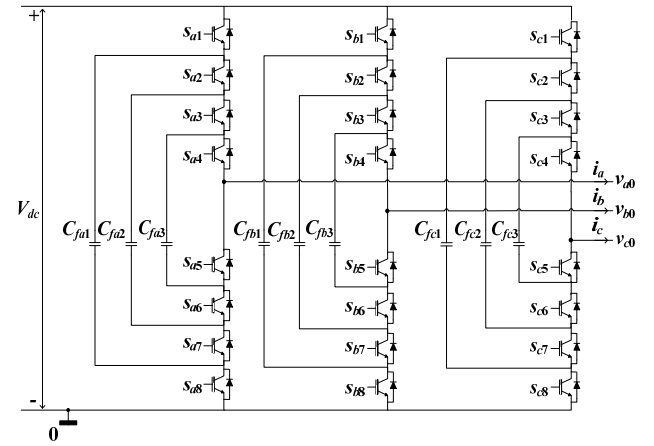


Fig. 1. Circuit Diagram of a five-level FC VSC.

scheme. Section IV discusses the comparison of using triangle and sawtooth carriers for reducing the switching frequency in the power devices. Section V presents some simulation results in order to verify the effectiveness of the proposed voltage balancing scheme on a five-level FC topology, and also to show switching frequency reduction of the power devices when operating with sawtooth carriers. Additionally, a line-to-line voltage is analyzed in terms of FFT and THD. Finally, some conclusions are summarized in Section VI.

## II. OPERATING PRINCIPLE OF FLYING CAPACITOR CONVERTER

Fig. 1 shows a schematic diagram of a three-phase five-level FC VSC, in which three FCs are integrated in each phase. During normal operation, the mean voltages of the FCs  $C_{fx1}$ ,  $C_{fx2}$ , and  $C_{fx3}$ , should be maintained at  $3V_{dc}/4$ ,  $V_{dc}/2$ , and  $V_{dc}/4$  respectively, where the subscript 'x' is used for the phase identification such as  $x=a, b$ , or  $c$ , and ' $V_{dc}$ ' is the voltage of the dc bus. Consequently, the voltage across each switch is only one quarter of the dc-link voltage. The switch control function is defined as  $s_{xy}$ , where the subscript 'x' is

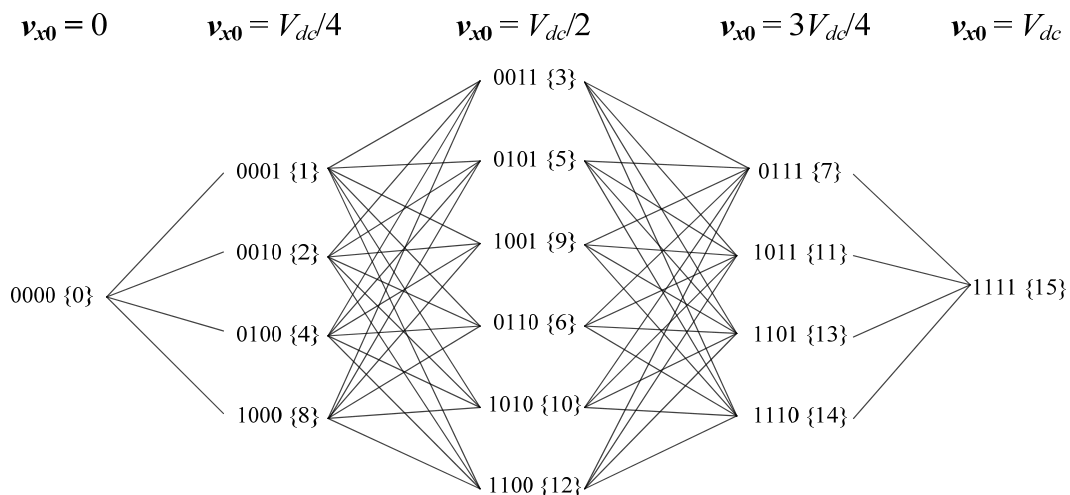


Fig. 2. Switching states and possible transitions between consecutive voltage levels.

used for phase identification and ‘y’ is used to identify the particular switch in the phase leg of FC converter ( $y=1,\dots,8$ ), which can take two values  $s_{xy}=\{0,1\}$ , meaning “0” and “1” that the switch is off and on, respectively. The switch pairs in each phase leg  $s_{x1}-s_{x8}$ ,  $s_{x2}-s_{x7}$ ,  $s_{x3}-s_{x6}$  and  $s_{x4}-s_{x5}$ , operate in a complementary manner. Each phase can generate five output voltage levels, with respect to the dc negative rail “0”, i.e. 0,  $V_{dc}/4$ ,  $V_{dc}/2$ ,  $3V_{dc}/4$  and  $V_{dc}$ . Using Kirchhoff’s voltage and current laws, the line-to-ground voltage  $v_{x0}$  and the currents through the FCs ( $i_{cx1}$ ,  $i_{cx2}$  and  $i_{cx3}$ ) can be written as:

$$v_{x0} = s_{x1}V_{dc} + (s_{x2} - s_{x1})v_{C1x} + (s_{x3} - s_{x2})v_{C2x} + (s_{x4} - s_{x3})v_{C3x}, \quad (1)$$

$$i_{Cx1} = (s_{x1} - s_{x2})i_x, \quad (2)$$

$$i_{Cx2} = (s_{x2} - s_{x3})i_x, \quad \text{and} \quad (3)$$

$$i_{Cx3} = (s_{x3} - s_{x4})i_x \quad (4)$$

Based on these fundamental equations, the line-to-ground voltage and FC currents are determined for all switching states and shown in Table I. The switching states are indicated by binary notation representing the control functions of the upper switches of the leg. It can be seen in this table that the redundant switching states for the voltage levels  $3V_{dc}/4$ ,  $V_{dc}/2$ , and  $V_{dc}/4$  define different current paths through the flying capacitors. Fig. 2 shows the possible transitions between consecutive voltage levels, considering the sixteen switching states of a leg. As in Table I, the binary notation of the switch control functions is also represented by its decimal number in curly brackets.

Fig. 3 shows a PD-PWM scheme for a five-level VSI. PD-PWM requires four carriers of the same amplitude, frequency and phase which are arranged into contiguous bands that fully occupy the linear modulation range. A reference sinusoidal

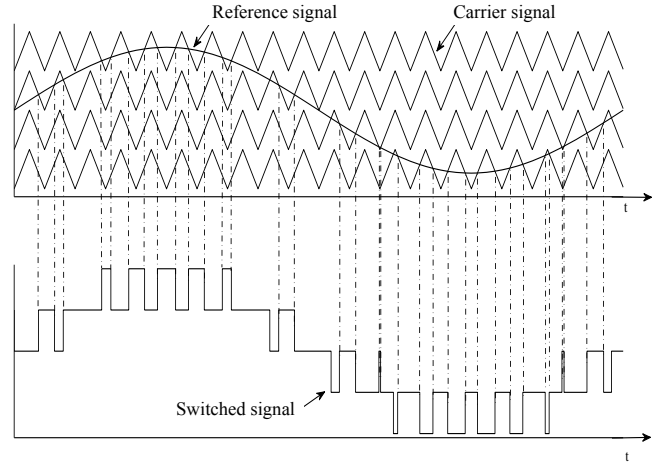


Fig. 3. Five-level PD modulator with the switched phase voltage.

modulation signal is compared with the four triangular carriers to define the voltage level that has to be generated at the output. This strategy is spectrally superior to other carrier layouts because it produces large harmonic concentration at some specific frequencies that cancels in the line-to-line voltages, hence reducing the output harmonic distortion [10]. However, PD-PWM does not provide natural capacitor voltage balance. Therefore, an active balancing scheme is required to stabilize the flying capacitors voltages to the desired levels.

### III. VOLTAGE BALANCING SCHEME

Fig. 4 shows the scheme of the proposed modulation strategy for one phase of a five-level FC VSC. It includes a voltage balance control based on minimizing a cost function, given as follows [14]:

$$J_{xz} = \frac{1}{2} \sum_{j=1}^{n-2} C_{fj} (v_{cjx} - v_{cjx}^*)^2, \quad (5)$$

where ‘x’ identifies the phase, and ‘z’ is the switching state  $z=\{0,\dots,15\}$ ; for example,  $J_{a12}$  is the cost function calculated for phase *a* and switching state {12}, i.e.  $s_{a1}=1$ ,  $s_{a2}=1$ ,  $s_{a3}=0$ , and  $s_{a4}=0$  (or 1100). *j* is the index used for the identification of each flying capacitor  $j=\{1,2,3\}$ , being  $C_{fj}$  a particular flying capacitor and ‘ $v_{Cjx}^*$ ’ its reference voltage.

This cost function is positive defined and if all the FC voltages equal their reference value, it becomes zero.

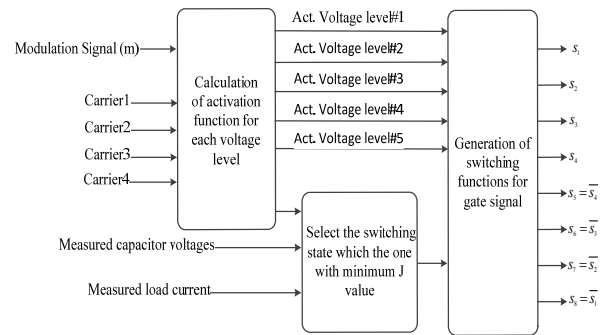


Fig. 4. Block diagram of five-level FC capacitor voltage balancing implementation scheme using phase disposition modulation for single phase.

TABLE I  
FIVE-LEVEL FC CONVERTER; VOLTAGE LEVELS, FC CURRENTS, AND SWITCHING STATES

Output Voltage Level ( $v_{x0}$ )	Switching States	FC Currents			FC Voltages							
		$s_{x1}$	$s_{x2}$	$s_{x3}$	$s_{x4}$	$St.\#$	$i_{Cx1}$	$i_{Cx2}$	$i_{Cx3}$	$v_{C1x}$	$v_{C2x}$	$v_{C3x}$
5	$V_{dc}$	1	1	1	1	{15}	0	0	0	x	x	x
	$3V_{dc}/4$	1	1	1	0	{14}	0	0	$i_x$	x	x	↑
		1	1	0	1	{13}	0	$i_x$	$-i_x$	x	↑	↓
		1	0	1	1	{11}	$i_x$	$-i_x$	0	↑	↓	x
		0	1	1	1	{7}	$-i_x$	0	0	↓	x	x
3	$V_{dc}/2$	1	1	0	0	{12}	0	$i_x$	0	x	↑	x
		1	0	1	0	{10}	$i_x$	$-i_x$	$i_x$	↑	↓	↑
		0	1	1	0	{6}	$-i_x$	0	$i_x$	↓	x	↑
	$V_{dc}/4$	1	0	0	1	{9}	$i_x$	0	$-i_x$	↑	x	↓
		0	1	0	1	{5}	$-i_x$	$i_x$	$-i_x$	↓	↑	↓
		0	0	1	1	{3}	0	$-i_x$	0	x	↓	x
2	$V_{dc}/4$	1	0	0	0	{8}	$i_x$	0	0	↑	x	x
		0	1	0	0	{4}	$-i_x$	$i_x$	0	↓	↑	x
		0	0	1	0	{2}	0	$-i_x$	$i_x$	x	↓	↑
		0	0	0	1	{1}	0	0	$-i_x$	x	x	↓
1	0	0	0	0	{0}	0	0	0	x	x	x	

Note: The charging/discharging effects in the FC is given assuming that  $i_x$  is positive ( $i_x > 0$ ) with the following notation;  
 ↑ = Capacitor voltage is charging  
 ↓ = capacitor voltage is discharging  
 x = no change on the capacitor voltage

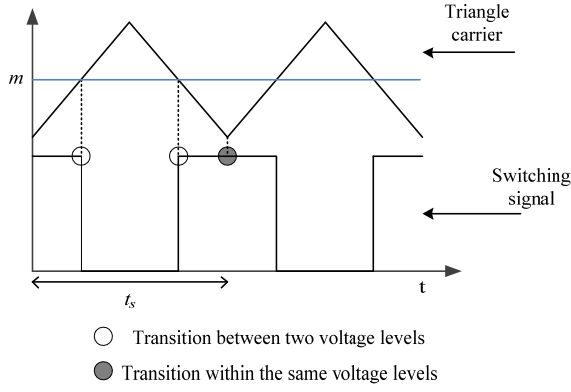


Fig. 5. Example of transition between two consecutive voltage levels and possible transition within the same voltage level when using triangle carriers.

Therefore, this cost function has to be minimized at any switching period to attain voltage balance. One of the methods for minimizing the cost function is through differentiation of (5), as follows:

$$\frac{d}{dt} J_x = \frac{d}{dt} \frac{1}{2} \sum_{j=1}^{n-2} C_{fj} (v_{cjx} - v_{cjx}^*)^2 = \sum_{j=1}^{n-2} (\Delta v_{Cjx} i_{Cjx}) \leq 0 \quad (6)$$

where  $\Delta v_{cjx}$  is the voltage deviation of a flying capacitor ( $\Delta v_{cjx} = v_{Cjx} - v_{Cjx}^*$ ), and  $i_{Cjx}$  is the current in each FC, which depends on the selected redundant switching state and load current, as shown in Table I.

When the modulator defines two particular voltage levels for the following switching period, the cost function is evaluated for all redundant switching states available for those levels. Based on the calculated values, the switching state that provides the minimum value to the cost function are the ones selected. They are therefore used to define the gating signals.

#### IV. REDUCTION OF THE SWITCHING FREQUENCIES USING SAWTOOTH CARRIERS

Triangle carriers with symmetric slopes are normally used

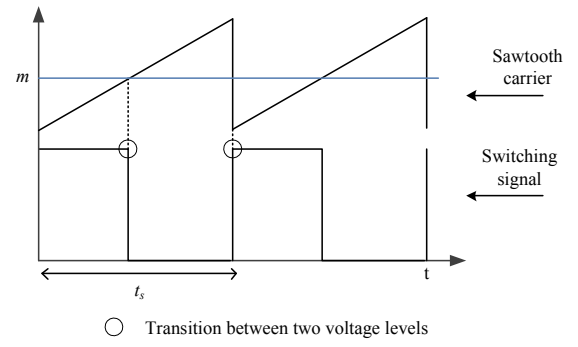


Fig. 6. Transition between two voltage levels using sawtooth carrier.

for the modulation (Fig. 3). When using these carriers, once a switching period has finished, the following one will usually start providing the same voltage level as in the previous instant (Fig. 5). Since evaluation of the cost function is performed during the previous switching period and applied in the actual one, the particular switching state may change within the same level because of voltage balancing requirements. This fact leads to additional switching events in the power devices. This phenomenon can be avoided by changing the shape of the carriers.

Fig. 6 shows the case of using sawtooth-shaped carriers for the modulation. Observe that in this case there is no transition within the same voltage level when changing from one switching period to the next one. Hence, a significant amount of switching events can be avoided by using sawtooth carriers.

#### V. PERFORMANCE EVALUATION AND ANALYSIS USING DIFFERENT CARRIER WAVEFORMS

In this section, the modulation strategy with the proposed voltage balancing scheme is applied to a five-level FC VSI in MATLAB/Simulink using PLECS blockset. Two carrier waveforms are analyzed and compared; triangle and sawtooth. The performance of the proposed voltage balancing

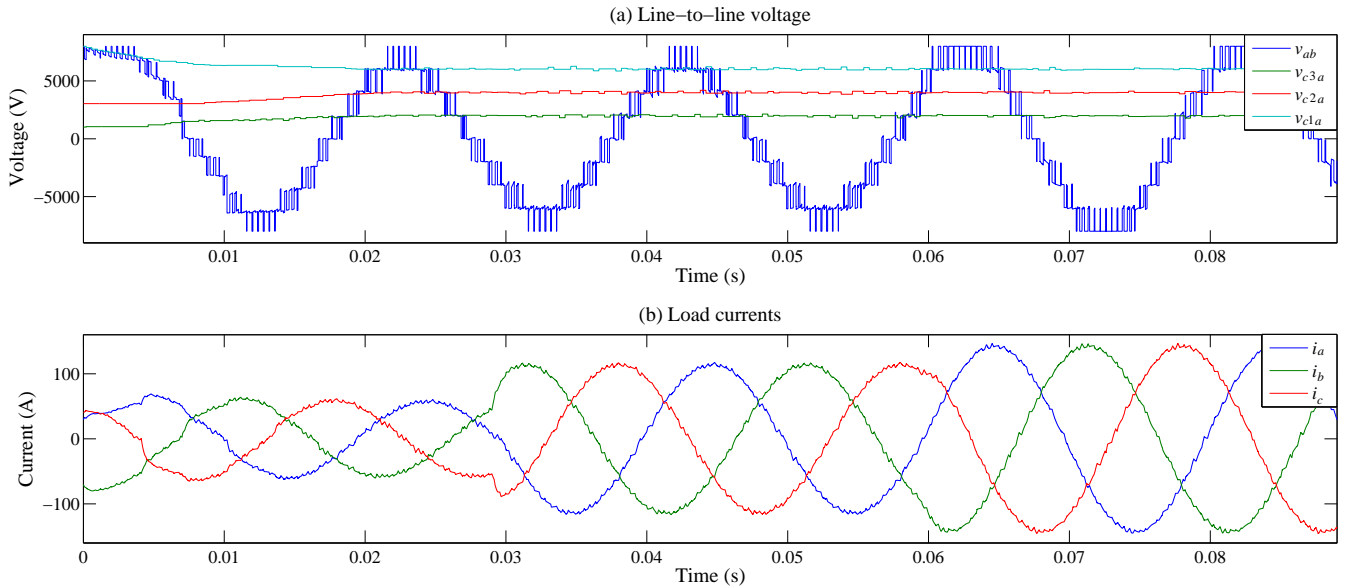


Fig. 7. Five-level FC line-line voltage under different load condition: (a) line-line voltage 'v<sub>ab</sub>' and FC voltages of phase 'a', (b) three phase load current under different load conditions.

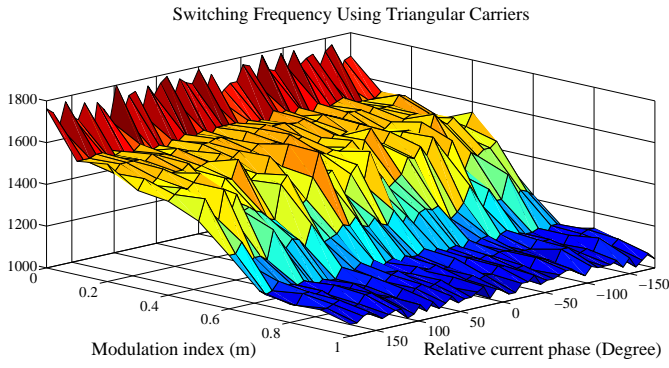


Fig. 8. Switching frequency of device using triangle carrier in terms of all operating conditions in terms of modulation index and load side power factor.

scheme is evaluated by comparing switching frequencies, FFT and THD of a line-to-line output voltage. In the simulations, the dc voltage is  $V_{dc}=8$  kV and a Wye R-L load rated at 1 MVA with  $\cos\phi=0.99$  is connected to the converter output. The value of the FCs is  $C=100$   $\mu$ F. The fundamental and the carrier frequencies are  $f=50$  Hz and  $f_s=2.5$  kHz, respectively.

The dynamic response of the close loop voltage balancing scheme is shown in Fig. 7. In this simulation, the initial capacitor voltages were  $v_{C1a}=8$  kV,  $v_{C2a}=3$  kV and  $v_{C3a}=1$  kV, and regulated to the desired voltages, i.e. 6 kV, 4 kV, and 2 kV, respectively. Observe that the capacitor voltages reach their reference values in about 25 ms. Once in the steady state condition, there is a step change in the load (resistor changes from 64 to 32 ohms), and later, at  $t=60$  ms, the modulation index changes from  $m=0.8$  to  $m=1$ . Observe that during the transients the voltages on the FC remain unaffected. Hence, the proposed voltage balance control proves to be robust not only in the steady state but also under dynamic operating conditions.

Figs. 8 and 9 show the average switching frequency of the power device (transistor) using triangle and sawtooth carriers, respectively. All possible output current phase angles and modulation indices have been considered. In order to achieve the maximum amplitudes of the output voltage fundamentals under linear mode, a zero sequence has been added to the modulation signals of the three-phase system. The zero sequence is given by  $v_o=-(v_{max}+v_{min})/2$ , where  $v_{max}$  and  $v_{min}$  are the maximum and minimum values of the modulation

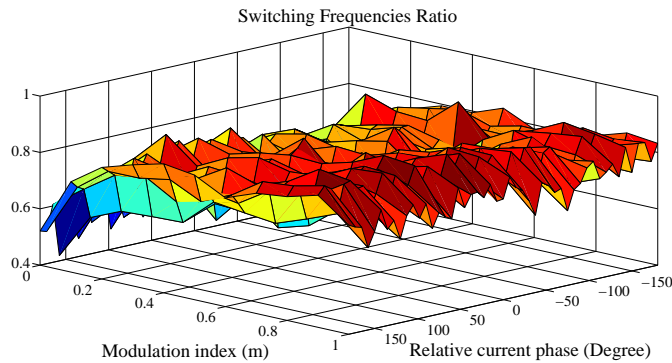


Fig. 10. Switching frequencies ratio (sawtooth/triangle) of device using triangle carrier in terms of all operating conditions in terms of modulation index and load side power factor.

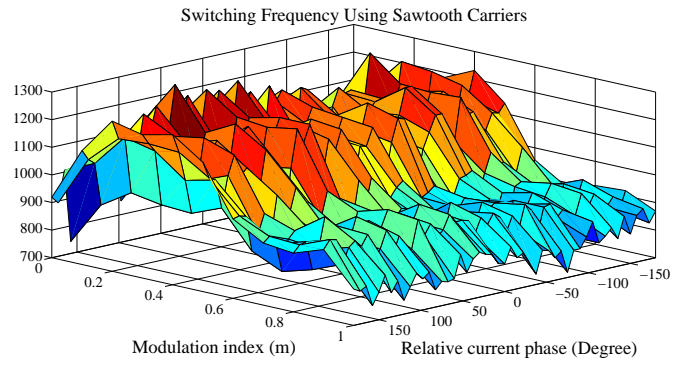


Fig. 9. Switching frequency of device using sawtooth carrier in terms of all operating conditions in terms of modulation index and load side power factor.

signals of the three-phase system, respectively. In these figures, one can observe that the output current phase angle does not significantly affect the switching frequency. On the other hand, large modulation indexes produce less switching frequency than low modulation indices in both cases; i.e. triangle and sawtooth carriers. This is due to the fact that at high modulation index, the output voltage is synthesized mostly using the higher and lower voltage levels. All the transitions between nearby levels to these extreme ones require the minimum number of switching events i.e. only one switch changes whenever there is a transition between the switching states. As a result, low switching frequencies are produced during those transitions.

Fig. 10 shows the switching frequency ratio of both modulation strategies, i.e. sawtooth over triangle carriers, for all modulation indices and load power factors. It should be remarked that with sawtooth carriers there is a reduction of the switching frequency of about 20% on average for large modulation indexes. Such a reduction in the switching frequency is even larger for low modulation indexes.

Fig. 11 shows the line-to-line output voltage THD for the two cases; triangle and sawtooth carriers. In the case of sawtooth carriers the THD is increased by about 4%. Nevertheless, such an increase in the distortion is produced at high frequencies (around the switching frequency and above) and no low-frequency distortion appears in any case. Thus, such harmonic components can be easily filtered. The line-to-line output voltage spectra are shown in Fig. 12 and Fig. 13, where the FFT has been performed for sawtooth and triangle carriers, respectively. The figures show the output voltage

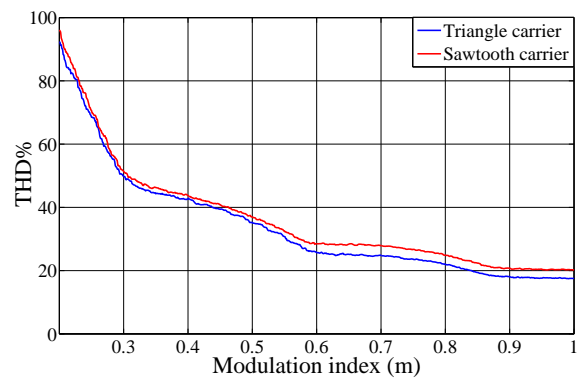


Fig. 11. THD of line-line voltage using triangle and sawtooth carrier.

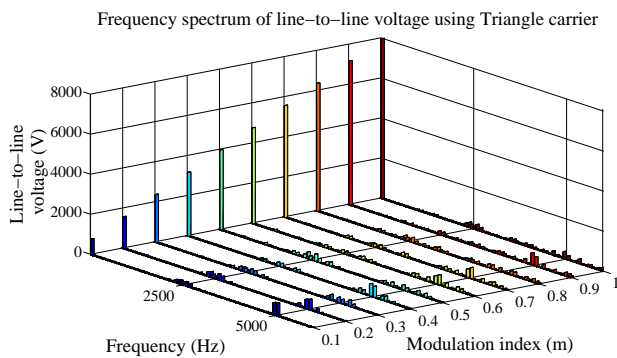


Fig. 12. FFT of the line-line voltage based on different modulation index using triangle carrier.

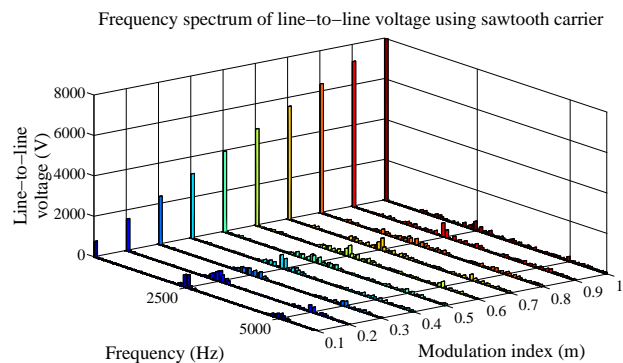


Fig. 13. FFT of the line-line voltage based on different modulation index using sawtooth carrier.

spectra for modulation indexes ranging from 0.1 to 1.

In summary, sawtooth carriers produce more THD and worse output voltage spectra; however, they are easily filtered because the increased distortion is produced at around and above the switching frequency. On the other hand, it produces significantly less switching frequencies and thus lower switching losses.

## VI. CONCLUSION

This paper implements a voltage balancing scheme for multilevel FC converters using PD-PWM. This scheme is based on calculating a cost function considering the FC voltage deviations and the load current. The redundant switching state that gives the lower value to the cost function is selected for each output voltage level. The voltage balancing method is implemented in a five-level FC converter and tested against static and dynamic load conditions. It performs very well in regulating the FC voltages to the desired levels, thus proving the robustness of the voltage balancing algorithm.

Moreover, two carrier shapes for PD-PWM have been studied; triangle and sawtooth waveforms. Simulation results show that the average switching frequency of the devices is reduced by about 20% using the sawtooth carriers as compared to the triangle ones. The reason for such a reduction in the switching frequency is due to the fact that in sawtooth carriers there are no transitions among redundant switching states (those that provide the same output voltage level). This switching frequencies reduction comes at the cost of increasing the THD of the output voltages. Nevertheless, this increase in the THD is produced by high frequency harmonics (around and above the switching frequency); therefore, they can be easily filtered. Hence, there is a tradeoff between switching frequency reduction and increased output voltage THD voltage.

Further reduction in the switching frequencies of the power devices can be achieved if critical transitions between two consecutive voltage levels were also avoided. This will be analyzed in future work.

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