Closed loop controlled ring oscillator: a variation tolerant self-adaptive clock generation architecture

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***Abstract*—In this work we propose a self-adaptive clock based on a ring oscillator as the solution for the increasing uncertainty in the critical path delay. This uncertainty increase forces to add more safety margins to the clock period which produces a circuit performance downgrade. We evaluate three self-adaptive clock systems: free running ring oscillator, infinite impulse response filter controlled RO and TEAtime controlled ring oscillator. The safety margin reduction of the three alternatives is investigated under different clock distribution delay conditions, dynamic variation frequencies and the presence of mismatch between the ring oscillator and the critical paths and the delay sensors.**

I. Introduction

Modern digital systems rely on synchronous circuit architectures. On any synchronous circuit the clock is the most critical signal and its period is a critical parameter that has to be carefully selected. The clock period has to be long enough to accommodate the critical path delay plus the set-up time and the clock-to-output delay of the registers. Since there is an uncertainty component in the delay of every logic gate due to the process, voltage, temperature, voltage and aging (PVTA) variations a safety margin has to be added to the clock period. This safety margin ensures a correct operation of the synchronous system. The more margin added, the more unlikely to fail the chip is. But a price is paid: less performance. Alternatively the safety margin can be added, instead of to the clock period, to the supply voltage. In this case the yield is increased but at the price of more power consumption.

PVTA variations can be classified as static or dynamic and spatially homogeneous or heterogeneous. Table I classifies the most common variations following this taxonomy.

TABLE I
Common sources of variability classified by its temporal, static or dynamic, and spatial, homogeneous or heterogeneous, behaviour.

	Static	Dynamic
Homogeneous	• Die to die (D2D) process variations.	• Voltage regulation module (VRM) ripple. • Room temperature variations. • Off chip voltage drops.
Heterogeneous	• Within die (WID) process variations. • Device to device random (RND) process variations.	• Simultaneous switching noise (SSN). • IR drop. • Temperature hotspots. • Ageing.

The margin added to the clock period or supply voltage has to be carefully determined. PVTA variations produce a delay uncertainty which is hard, in some cases, or impossible, in others, to predict. Different techniques like corner analysis, SSTA, etc; are used to estimate the safety margin that, once added to the clock period or the supply voltage, produces a desired yield.

As the transistors minimum size shrinks the uncertainty due to process variations increases as well as the aging effects become more important [1], [2]. In parallel, the transistor size reduction makes possible more complex circuits. This complexity increase lead to a richer running situations which difficult to estimate the supply voltage variations such as IR drop and/or simultaneous noise (SSN).

In a similar way, the temperature of the circuit can vary depending on the computation carried out on it since the amount of demanded current by its different blocks depend on the executed instructions. On top of this the temperature also depends on the temperature of the environment where the chip operates.

As the amount of uncertainty reaches its highest value and its estimation during the design stage consumes more and more resources a new paradigm in the synchronous circuit ecosystem is needed. We propose in this article the self-adaptation of the clock period as a solution to ensure the correct operation of any synchronous circuit under the effect of PVTA variations.

In section II we show the natural capability of ring oscillators (RO) to act as self-adaptive clock sources that can cope with PVTA variations. Also, in this section, its weaknesses are revised. In section III a closed loop control architecture for the ring oscillator is proposed in order to cope with the RO weaknesses. In section IV the simulation results are presented and the advantages and disadvantages of the closed loop controlled RO in front of a free running ring oscillator are discussed. And finally, in section V the conclusions are exposed.

II. RO ADAPTATION TO PVTA VARIATIONS

A ring oscillator (RO) is an oscillating circuit: a chain of inverting and non inverting stages, where the chain output is connected to the chain input.

ROs, due to its oscillating nature, can be used to generate clock signals but, in digital systems, they are not used to carry out this duty because its high sensitivity to PVTA variations. This high sensitivity is normally accounted as a source of clock indetermination.

Contrary to be an undesired effect, the RO sensitivity to PVTA variations can be the key point to build a clock signal source which period is adapted to the circuit environment conditions. This change of perspective will lead us to stop relying on fixed clock signals like PLLs and reduce the safety margins added, during the design stages, to the clock period and/or the supply voltage. As a side effect of this, the resources and time spent in the design stages will be also reduced.

Let us assume an ideal case in which the RO suffers the same PVTA variations as all the candidates to operate as a critical path (CP) and the clock distribution is instantaneous (fig. 1). Under these naive operating condition assumptions it is obvious that the RO generated clock will adapt its period to the instantaneous delay suffered by the gates in the die. Unfortunately these conditions do not take place in reality.

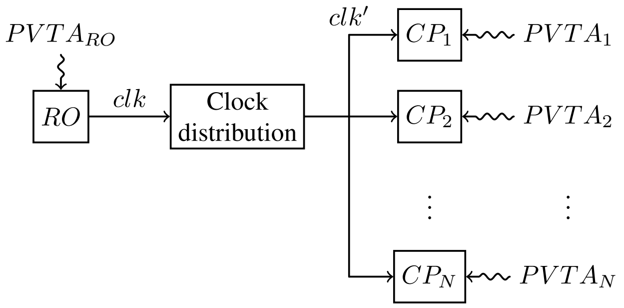

Fig. 1. Free running ring oscillator (RO) used as a self-adaptive clock generator. The main elements that undermine the performance of RO as a self-adaptive clock generator are depicted: the mismatch between the variations suffered by the RO and the circuit critical paths (CP); and the clock distribution network which introduces a delay between the generated and the delivered clock signal to the CPs.

A. RO limitations

The limitations of the RO clock generation are caused by the mismatch between the PVTA variations that take place in the RO gates and all the other gates circuit, among them, the critical path.

This mismatch can be caused by the heterogeneity of the variations along the die such as within die variations (WID) due to process, different IR drops on V_{dd}, temperature differences in the chip, etc. Also the mismatch can arise if the variations are homogeneous but have a dynamic component. Since the clock generated by the RO need to be distributed all along the die through a clock distribution network (CDN). The CDN imposes a delay, t_{clk}, between the generated clock and the delivered clock signals. The period of the delivered clock, at the end of the CDN, will be adapted to the variations that occur t_{clk} before, not at that instant.

Against heterogeneous variations, static or dynamic, the RO can fail reducing the safety margin or, eventually, will increase the needed value. RO circuit adapts its period to the environment conditions near it. RO can not sense the variations along the die since it acts like a point sensor.

The homogeneous dynamic variations (HoDV) can be partially addressed by the RO clock. The mismatch, introduced by the clock distribution delay, between the clock period and the CPs delay, considering only the presence of an HoDV $\nu(t)$, depend on the period of the dynamic variation, T_ν, and the clock distribution delay, t_{clk}, introduced by the CDN. The mismatch between the RO and a CP, $\Delta\nu(t, t_{clk}, T_\nu)$, will be equal to:

$$\Delta\nu(t, t_{clk}, T_\nu) = \nu(t, T_\nu) - \nu(t - t_{clk}, T_\nu) \qquad (1)$$

1) Periodic HoDV: Considering HoDV as a periodic function, $\nu(t) = \nu_0 \sin(2\pi {T_\nu}^{-1} t + \phi)$, the worst mismatch due to an HoDV will be equal to:

$$\Delta\nu(t_{clk}, T_\nu) = 2\nu_0 \left\| \sin\left(\pi \frac{t_{clk}}{T_\nu}\right) \right\| \qquad (2)$$

The boundary that limits the safety margin reduction for a periodic HoDV is $t_{clk}/T_\nu < 1/6$ or $(n - 1/6) < t_{clk}/T_\nu < (n+1/6)$ for $n \geq 1$, where n is a positive integer. Within these constrains the use of a RO reduces the value of the needed safety margin. If t_{clk} do not fulfil these constrains the adaptive clock will need more safety margin than the fixed clock.

2) Single event HoDV: For a single event, like a fast voltage drop along the whole die, assuming a triangular shape with a duration of T_ν and an amplitude ν_0, the mismatch due to the CDN delay will be equal to:

$$\Delta\nu(t_{clk}, T_\nu) = \begin{cases} 2\nu_0 \dfrac{t_{clk}}{T_\nu} & \text{if } 0 \leq t_{clk}/T_\nu \leq 1/2 \\ \nu_0 & \text{if } t_{clk}/T_\nu > 1/2 \end{cases} \qquad (3)$$

If t_{clk} is larger than half of the event duration the safety margin needed by a normal clock system and the RO will be the same. Therefore there is no reason to use the adaptive system.

Eq. 2 and 3 clearly express the trade-off between the CDN delay and the maximum dynamic variation frequency we can tolerate for a given maximum mismatch. This trade-off relates not only the the maximum frequency of the dynamic variation with CDN delay also the clock domain size since it is directly related with CDN delay.

As a short conclusion we can say that the free running RO can be useful to reduce the safety margins introduced to cope with HoSV and HoDV with frequencies much lower than $1/t_{clk}$. In section III we propose a more complex architecture in order to cope with heterogeneous variations, which the RO can not fight, as well as improve the adaptation to dynamic variations.

III. Closed loop controled RO

To cope with the spatial heterogeneity of the PVTA variations we propose to disseminate sensors all over the clock domain. As sensors we propose the time digital converter (TDC) [3]. TDC outputs, every clock cycle, the number of crossed gates, or stages, by an alternating signal during the last period. This integer number give us a sense of the delay suffered by the gates near each TDC. If the output of the TDC is low means that the logic gates are experimenting an extra delay due to the variations; or vice-versa when the output is high. The stages of the TDCs and the RO are supposed to be equal. This equivalence will not take place in reality, for this reason we will have to take into account heterogeneous static and dynamic variations.

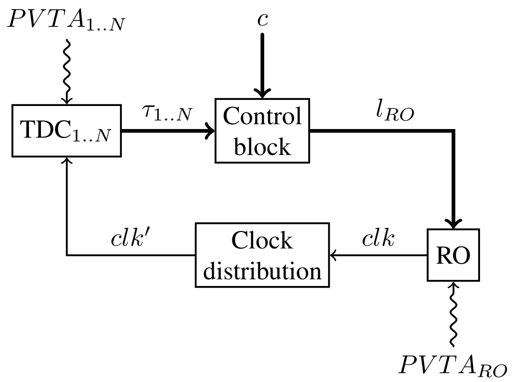

Fig. 2. Closed loop controlled ring oscillator architecture. The main signals are labelled: the set-point c which is the only input of the clock generation system, the ring oscillator length l_{RO}, the generated clock clk, the distributed clock clk' and the i-th TDC lecture τ_i. Also we point out that the clock generator, the RO, and the sensors, the TDCs, could suffer different variations.

Once we have some sensors on the core we can compare, at each period, the worst sensor output τ, this is the lowest output among all the TDCs, with a given set-point c and then take some actions over the RO, *i.e.* changing its length l_{RO}, in order to adapt the clock period to the variations that the RO can not sense. This closed loop controlled RO architecture is depicted in Fig. 2.

By having a clock managed by a closed control loop with a set-point input the clock period has not to be set during the design stage, so the CPs delays do not need to be estimated. Simply, once the chip is produced and it is running, we only need to choose the correct set-point c that allows the system to run without any error and/or maximizes the computation throughput. Therefore the pipeline needs, at least, error detection capacities.

From this point, in this article, the delay and the period are not measured any more in seconds. We will measure it into number of stages. In fact the units of c, l_{RO} and τ_i are number of stages. c is the output we want to get from the TDCs τ_i and l_{RO} is the length of the RO.

The architectural view in Fig. 2 can be translated, since every event is triggered by the clock edges, into a discrete control system view as shown in Fig. 3. As a first approximation to the problem we modelled the action of the RO, CDN and TDC as simple delay chain with the addition of perturbations, that account for the heterogeneous and homogeneous variations.

When the RO length l_{RO} is changed the clock period changes the value of its period in the next clock period. Then this clock has to be distributed through the CDN and will take M periods to arrive to the registers. The value of M will depend on the period of the clock signal $T_{clk}[n]$ at each step and the delay of the CDN t_{clk}: $M[n] = \lceil t_{clk}/T_{clk}[n] \rceil$. Once the clock arrives to the registers the TDCs outputs the number of crossed stages τ during the last period. τ is compared with the set-point c in order to generate a error value $\delta = c - \tau$. δ is injected into the control filter $H(z)$ that will, after one period, give the new l_{RO}.

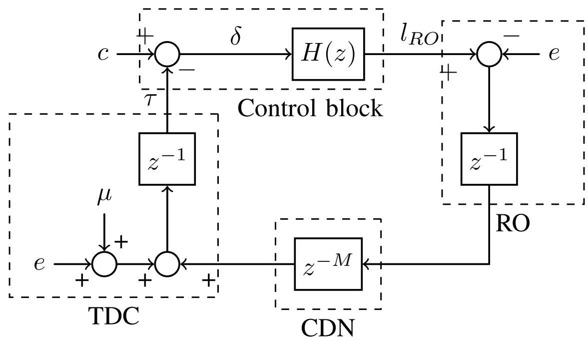

Fig. 3. Discrete system view of the closed loop controlled ring oscillator. The Main blocks of the architecture are labelled. The system inputs are labelled: the set-point c, homogeneous variation e and heterogeneous variation μ. As well as important signals: RO length l_{RO} and adaptation error δ. The CDN number of samples M delay depends on the input value to the CDN block and the CDN delay in number of stages: $M = \lceil t_{clk}/T_{clk} \rceil$.

The period of the clock generated by the RO can be influenced by an homogeneous variation e, which affects equally the TDCs. When the same variation affects to the RO and the TDC the output of the TDC would not vary. Therefore, in the discrete control system schema (Fig. 3), the perturbations in the TDC and in the RO had to operate with opposite sign. To take into account heterogeneous variation an other perturbation, μ, is added to TDC.

A. Control block constrains

Once the control loop is defined it is possible to find out how the two most important magnitudes, δ and l_{RO}, behave when some change occur in the perturbations, *i.e.* e and/or μ, or set-point, c.

As depicted in Fig. 3 we can derive, in the z-domain, the l_{RO} and δ expressions as function of the combined inputs $p(z)$ assuming $H(z) = N(z)/D(z)$:

$$H_{l_{RO}}(z) = \frac{l_{RO}(z)}{p(z)} = \frac{N(z)}{D(z) + N(z)z^{-M-2}} \tag{4}$$

and

$$H_{\delta}(z) = \frac{\delta(z)}{p(z)} = \frac{D(z)}{D(z) + N(z)z^{-M-2}} \tag{5}$$

where

$$p(z) = c(z) + \left(1 - z^{-M-1}\right) z^{-1} e(z) - \mu(z) z^{-M-2} \tag{6}$$

If we assume that $p(z)$ will be equal to a Heaviside step, when $t \to \infty$, the desired value for δ and l_{RO} will be:

$$\lim_{t\to\infty} h_{l_{RO}}(t) * u(t) \neq 0 \tag{7}$$

$$\lim_{t\to\infty} h_{\delta}(t) * u(t) \quad = 0 \tag{8}$$

this is that under a minimum perturbation the value of l_{RO} changes to counteract it (7) and, consequently, the error value δ tends to zero (8). Using the final value theorem we can re write (7) and (8) as (9) and (10) respectively:

$$\lim_{z\to 1} (z-1) H_{l_{RO}}(z) U(z) \neq 0 \tag{9}$$

$$\lim_{z\to 1} (z-1) H_{\delta}(z) U(z) \quad = 0 \tag{10}$$

which led us to a a set of constrains of $N(z)$ and $D(z)$:

$$N(1) \neq 0 \tag{11}$$

$$D(1) = 0 \tag{12}$$

B. Control block implementations

In this section we propose two different implementations of the control filter $H(z)$. The first, an infinite impulse response (IIR) filter and, the second, a TEAtime [4], [5] implementation.

The IIR control block architecture proposed is depicted in fig. 4. It is slightly different to standard IIR filters due to the constraints found in sec. III-A and some implementation constraints, like the aim of reducing the clock generation circuit area overhead. Due to this we choose to operate over the integers avoiding the use of floating coma operations. Secondly the gain values all along the IIR control block are constrained to powers of two, thanks to this, these gains can be realized with a minimum number of logic gates; only adding zeros, or ones for the negative values, to the right or to the left of the signal bus. Because we choose to operate over the integers we add two gains, one at the input (k_{exp}) and one, with the inverse value of the input one, at the output $\left({k_{exp}}^{-1}\right)$ in order to reduce the rounding error inside the control block. Another difference with common IIR filters is the k^* gain (fig. 4) added to assure the fulfilment of constrains 11 and 12 when the IIR has more than one coefficient. Also we added an extra delay after k^* gain in order to take into account the possible need of a large adder to implement the control block that could be necessary to pipeline it.

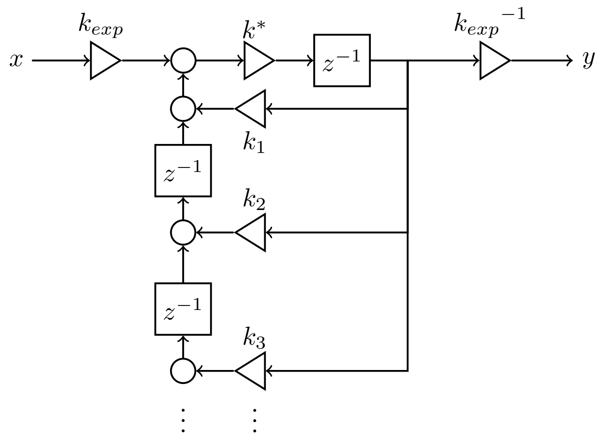

Fig. 4. IIR control block implementation proposal.

The transfer function of the proposed IIR filter (fig. 4) is the following:

$$H_{IIR}(z) = \frac{z^{-1}}{\dfrac{1}{k^*} - \displaystyle\sum_{i=1}^{N} k_i z^{-i}} \tag{13}$$

To fulfil the constrains 11 and 12 the filter coefficients had to follow the next relation:

$$k^* = \left(\sum_{i=1}^{N} k_i\right)^{-1} \tag{14}$$

For the TEAtime implementation, the control block $H_{TEA}(z)$, is depicted in fig. 5. In this case there are no parameters to set and therefore the constraints do no apply in this case.

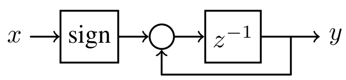

Fig. 5. TEAtime control block implementation proposal inspired from [4], [5].

IV. ARCHITECURE SIMULATION

To perform the simulations we used the Simulink software from Mathworks. We simulated the adaptive response of three different systems: the proposed IIR controlled RO, a TEAtime controlled RO and a free running RO.

The chosen gain parameters for the IIR controlled RO are: $k_{exp} = 8$, $k^* = 1/2$, $k_1 = 1$, $k_2 = 1/2$, $k_3 = 1/4$, and $k_4 = k_5 = 1/8$. With this values we achieve a balance between filter adaptation velocity and low output ripple. k_{exp} value is chose to assure that the minimum perturbation propagates through all the branches of the filter. The set-point value for all the simulations is $c = 64$, this is the desired TDCs lecture. The amplitude of the periodic perturbation e is set equal to $0.2c$, this is a 20% homogeneous variation.

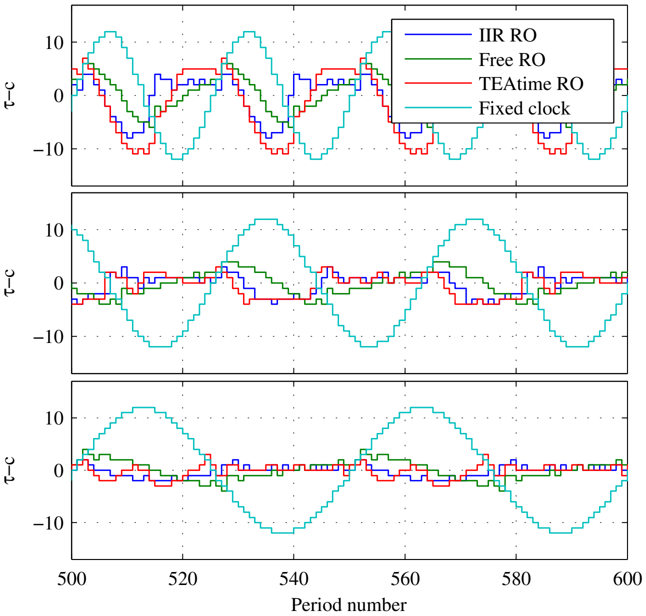

Fig. 6. Timing error $\tau - c$ for different clock generation systems. For the three plots the parameter are: set-point $c = 64$, HoDV amplitude equal to the 20% of c, and the clock distribution delay equal one clock period, this is equal to c stages. And no mismatch between RO and TDC had been introduced. Upper plot: the perturbation period is set to $25c$. In this case the safety margin is slightly reduced. Middle plot: the perturbation period is set to $37.5c$. An appreciable adaptation error reduction takes place once the perturbation frequency is decreased. Lower plot: the perturbation period is set to $50c$. The Adaptation error is reduced to a minimum value.

1) Homogeneous dynamic variation: In fig. 6 the timing error $\tau - c$ due to a HoDV of different frequencies is shown for a CDN delay equal to c stages. In the top plot The perturbation period is equal to $25c$ stages, this is 25 times the nominal period value. In this plot is possible to see that the negative timing error which is equal, in absolute value, to the needed safety margin, is quite closer to the margin that would need a fixed clock to assure a error free operation, nevertheless the amplitude of the timing error is reduced.

In the middle plot of fig. 6 the perturbation period is augmented to $37.5c$ stages. As the perturbation period is augmented the system can adapt the clock frequency better and, consequently, reduce the impact of the HoDV.

And finally, in the fig. 6 lower plot, the perturbation period is increased to $50c$ stages. Once the perturbation is low enough its impact on the timing error $\tau - c$ gets even more reduced.

In fig. 6 Is possible to see that the different adaptive clock generation systems evaluated can reduce the timing error due to a HoDV but its hard to say which one achieves the greatest reduction, this is the best adaptation. For this reason we use a figure of merit: the relation between the mean clock period of the adaptive clock to the fixed clock period or relative adaptive period, $\langle T_{clk} \rangle / T_{clk\,fixed}$, when both assure a error free operation. Both clocks with the needed margins added and, for the adaptive case, taking into account the over

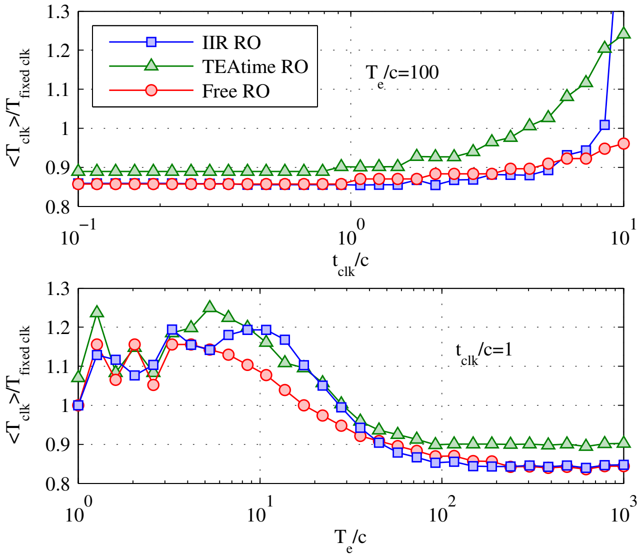

Fig. 7. Relative adaptive period for three different adaptive control systems under HoDV. Upper plot: The variation period is kept constant, $T_e = 100c$, and the CDN delay is varied. For the whole range until $t_{clk}/c = 5$ the IIR RO show the best performance, just slightly better than the free RO. Lower plot: The CDN delay is kept constant, $t_{clk} = c$, and the perturbation period is varied. The free RO is the first architecture to reduce the fixed clock safety margin at high frequencies. At mid frequencies, around $T_e = 100c$, the IIR RO is the best option. And for low frequency perturbations, $T_e > 200c$, the IIR RO and the free RO performance is very similar.

estimation of the delay ($\tau - c > 0$).

In fig. 7 $\langle T_{clk} \rangle / T_{clk\,fixed}$ is shown for different scenarios under a HoDV. In fig. 7 upper plot the perturbation period is kept fixed, $T_e = 100c$, and the CDN delay is changed. Up to $t_{clk}/c = 5$ the IIR RO is slightly the best option. For higher CDN delay valyes the free RO show the best adaptation to HoDV. In fig. 7 lower plot the CDN delay is kept constant and the perturbation period is varied. Here the free running RO is the best option for high frequency HoDV, it is the first architecture to reduce the fixed clock safety margin ($T_e/c \approx 20$). For $T_e/c \geq 40$ IIR RO shows the best adaptation to HoDV closely followed by the free RO.

To conclude the HoDV adaptation results can be translated in terms of period measured in seconds. If we assume that the set-point $c = 64$ generates, in ideal conditions, a clock period $T_{clk} = 1$ns. Under a CP delay variation up to 20% the clock period has to be set to $T_{clk} = 1.2$ns, or in the number of stages nomenclature the set-point should be changed to $c = 77$. If CDN delay and perturbation period scenario lead the adaptive clock to reduce the needed c, which assures an error free operation, up to 10%, this reduction can be translated as a reduction of 0.12ns in the clock period, which is a 60% reduction of the added safety margin.

2) Heterogeneous dynamic variation: In fig. 7 we shown that the free running RO is the architecture that copes with HoDV under the biggest range of conditions as the best or near the best option. But as we consider the HeDV, introduced through a mismatch offset μ as indicated in fig. 3, the best

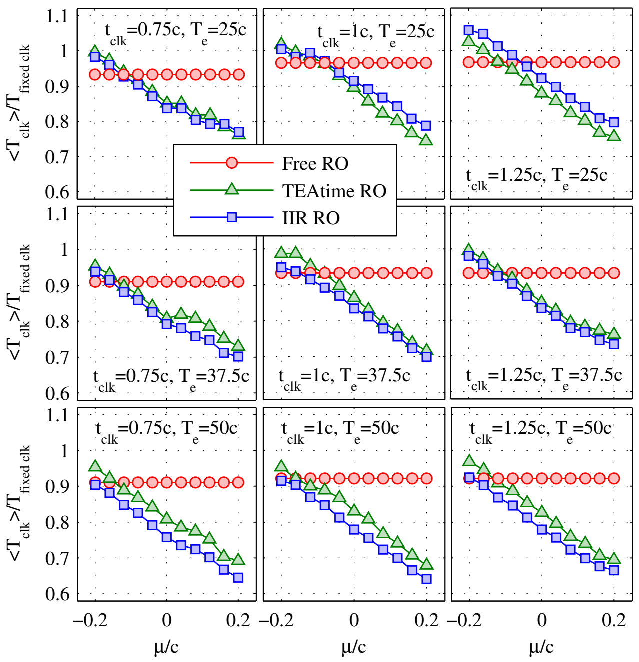

Fig. 8. Relative adaptive period for different CDN delay and variation period values when there is a static mismatch μ between the RO and the TDC. On almost any situation the IIR RO is the architecture that ensures the greatest safety margin reduction. Only for high frequency HeDV (upper row) TEAtime RO or free RO surpass the IIR RO when $\mu/c < -0.1$.

adaptive clock generation system option will not be the free RO any more. In fig. 8 the relative adaptive period, for different perturbation period and CDN delay scenarios, is shown when there is a mismatch, up to 20%, μ between the RO and the TDC which are also under a HoDV. Fig. 8 shows that IIR RO is the best option except for high frequency HeDV (upper row) where TEAtime shows the best safety margin reduction when $\mu/c > -0.1$, otherwise the free RO is the best option. IIR RO manages to reduce the fixed clock safety margin on al the situations unless for high frequency HeDV combined with big CDN delay and high mismatch μ (upper-right plot).

To conclude the HeDV adaptation results if we assume that the set-point $c = 64$ generates, in ideal conditions, a clock period $T_{clk} = 1$ns. Under a delay variation, due to HoDV, up to 20% and a delay variation, due to HeDV, also up to 20%; the clock period has to be set to $T_{clk} = 1.4$ns, or in the number of stages nomenclature the set-point should be changed to $c = 90$. If CDN delay and perturbation period scenario lead the adaptive clock to reduce the needed c, which assures an error free operation, up to 20%, this reduction can be translated as a reduction of 0.28ns in the clock period, which is a 70% reduction of the added safety margin.

V. Conclusions

In this paper we studied theoretically the effects of the clock distribution delay in the presence of homogeneous variations, static and dynamic. We showed that, in presence of homogeneous dynamic variations, the clock distribution delay induces a heterogeneous variation between the clock generation circuit and the critical paths on the clock domain. This induced mismatch supposes a limitation to the adaptive clock systems in terms of clock domain size.

Also we argued that the heterogeneous, static or dynamical, variations may not be corrected by a concentrated adaptive clock generation system like a free running ring oscillator. To cope with heterogeneous variations we proposed a closed loop architecture with delay sensors, TDCs, disseminated along the clock domain.

Thanks to have a set-point input we propose a new clocking paradigm where the clock value is not set during the design and/or test stages. Instead of this we propose a system that tries to minimize the difference between the minimum sensors outputs and the set-point. The set-point value could be adapted as function of the timing errors during a time window and/or the performance necessities.

We modelled, at a very high level, the action of dynamic perturbations on the ring oscillator and the TDC sensors as well as the effect of a variation mismatch between them.

Since the proposed system acts like a closed control loop we find some constrains for the control block when it is an infinite response filter.

Finally we ran a functional simulation showing that the free running ring oscillator can not be used alone as a source of adaptive clock since its generated clock is only adapted to the variations suffered by the very near environment of the ring oscillator circuit. And that the IIR controlled ring oscillator generates the most adapted clock signal under heterogeneous variations which are likely to appear in modern integrated circuits.

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