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Design of a 20 GHz DPI Method for SOIC8

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***Abstract*—The direct power injection (DPI) test defined in IEC 62132-4 measures the conducted immunity of integrated circuits (ICs) up to 1 GHz. As the frequency of functional and interference signals is increasing, we would like to characterise immunity for higher frequencies as well.**

In this paper, we show why typical IEC 62132-4 compliant DPI set-ups become inaccurate when going up to 20 GHz. We propose to determine the power P_{trans} actually transmitted to the device under test (DUT) by using offline short-open-load-thru (SOLT) or thru-reflect-line (TRL) calibration. Furthermore, we design a low-cost FR4 printed circuit board (PCB) that allows for testing of SOIC8-packaged ICs. We verify that this board has acceptable and reproducible losses up to 20 GHz, as well as acceptable crosstalk.

***Index Terms*—EMC, immunity, integrated circuit, DPI, GHz, centrimetre, modelling, low-cost, calibration, crosstalk, loss**

I. Introduction

The international allocation of industrial, scientific and medical bands around 2.4 GHz, 5.8 GHz, and 24 GHz suggests that we will see an increasing density of electronic appliances that use multi-GHz carriers and internal frequencies.We therefore expect to encounter more and more EMC challenges past one GHz.

We show in Section II, by means of examples, that there might be interesting conducted immunity issues in the $1-20$ GHz frequency band. We sketch what is needed to study these interesting issues in order to build an ICIM-CI (IC immunity model for conducted immunity) in Section III. In Section IV, we indicate why the DPI set-up as proposed in IEC 62132-4 does not necessarily comply with these requirements, and propose an alternative calibration. Armed with the requirements and trying to avoid the pitfalls described before, we design a low-cost test IC fixture in Section V. We verify the set-up by measurement and simulation in Section VI. Conclusions and recommendations for further research are given in Section VII.

II. Why Multi-GHz Conducted Immunity Measurements?

In [1], the conducted susceptibility transmitted power threshold of a simple digital circuit reportedly was +18 dBm in the $1-2$ GHz band, and +20 dBm in the $2-4$ GHz band. The current mirror studied in [2] starts to offset around 5 GHz with less than +10 dBm incident power.

Radiated immunity tests also show increasing susceptibility above 10 GHz [3]; the transmitted power threshold of a particular digital circuit is estimated to be as low as −5 dBm at 20 GHz [4].

Finally, extension of the DPI frequency range is also foreseen in roadmaps [5]. These observations suggest that there are interesting conducted immunity issues above 1 GHz.

Until what frequency will these interesting conducted immunity issues continue? For wire bonded packages, the bondwire plus leadframe inductance is in the order of some nH. For flip-chip packages, the 'lead' inductance is lower, but still in the same order of magnitude [6]. To get a feel, 2 nH equals 251 jΩ at 20 GHz; the die starts to electrically float. Consequently, with rising frequency, it becomes harder to couple functional as well as disturbing signals. This might explain the popularity of Antenna on Chip (AoC) solutions for 60 GHz [7], but also Antenna in Package (AiP) for 2.4 GHz [8]. Therefore, we expect interesting immunity issues above, say, 20 GHz to be mainly in *radiated* immunity. For this paper, albeit arbitrary, we set ourselves the upper frequency goal of 20 GHz.

III. ICIM-CI Measurement Requirements

To create IC immunity models, one needs to be able to detect failure while injecting a known perturbation. To detect failure, we need to provide typical signals and impedances to the DUT, while monitoring its functional behaviour. To inject a known perturbation, we need a known high frequency (HF) power source and we need to know the loss and crosstalk introduced by the DUT fixture. Let us now elaborate these requirements.

A. Typical signals and impedances

To get the DUT to function representatively of a certain application, it needs input signals and output terminations that all have representative voltages and impedances. We will now determine these requirements for the case of an LM7805

voltage regulator, which only has an input, an output and some ground pins. Although this case study is simple with respect to industrial cases, it is our expectation that the method can be extrapolated to more complex ICs.

The datasheet specifications ($C_{\text{in}} = 100\,\text{nF}$, $C_{\text{out}} = 330\,\text{nF}$, both tantalum [9]), suggest a mask for the impedance seen by the regulator input and output pins. We suppose that the input filter capacitor serves only to feed the regulator by low enough an impedance, so we impose $|Z_{\text{supply}}| < 5\,\Omega$ (the ESR) up to 30 MHz (the expected resonance frequency of the input filter capacitor). The output filter capacitor, however, may really be part of the regulator closed loop, so $\Im\mathfrak{m}\{Z_{\text{load}}\} < 1/(\omega 330 \times 10^{-9})$. In order to draw the typical load current, $\Re\mathfrak{e}\{Z_{\text{load}}\} \approx 125\,\Omega$. We impose these criteria up to 10 MHz (the expected resonance frequency of the output filter capacitor).

B. Fixture Loss

To induce failure, we need to transmit a certain microwave perturbation P_{trans} to the pin under test (PUT). As we have finite available power, the power lost in the fixture must be *reasonable*. What loss can be accepted is hard to say, for we do not yet know what immunity levels we are to encounter above 1 GHz.

On the one hand, the series impedance presented by the bonding rises linearly with the frequency ($\text{j}\omega L$). On the other hand, earlier radiated immunity tests show a decrease of immunity beyond 12 GHz [3, 4].

As we do not yet know the immunity behaviour beyond 1 GHz, we conclude that we should make an effort to keep the fixture loss low.

If the fixture loss can not be neglected, we need some means to correct our measurement results for the loss. Consequently, the loss needs to be *known*.

To the extent that we suppose the loss to remain the same, the loss needs to be *reproducible*.

C. Fixture Crosstalk

Recall that with the DPI test, we try to inject continuous wave (CW) power into a single pin. However, when power is leaked to a neighbouring pin, we observe the joint susceptibility of the PUT and its neighbouring pin. This leakage is called far-end crosstalk: the forward propagating power leaked from one transmission line to forward propagating power in a neighbouring line. In reality, there is always some crosstalk, so we should ask the question: what crosstalk is acceptable?

We assume that the immunity of an entire IC is the minimum of the individual immunities of its pins; we thereby neglect complex interactions between multiple disturbing signals. Under this assumption, the worst acceptable crosstalk is the largest difference between the immunity of any two neighbouring pins.

For example: the immunity level of pin 6 of a ATA6662 LIN transceiver at 10 MHz reportedly was $-10\,\text{dBm}$ of transmitted power, while the neighbouring pin 7 has an immunity level of $+9\,\text{dBm}$ of transmitted power [10]. Suppose that the test fixture has $-15\,\text{dB}$ of far-end crosstalk between the traces of pin 6 and pin 7. When injecting on pin 7, one will observe an immunity level of $+5\,\text{dBm}$, caused by the susceptibility of pin 6, instead of $+9\,\text{dBm}$, proper to pin 7.[1] To unambiguously characterise the immunity of the pins of this IC, a fixture with better than $-20\,\text{dB}$ far-end crosstalk would be preferable.

Lacking more available immunity data of neighbouring pins, we target a far-end crosstalk better than $-20\,\text{dB}$. More important than having little crosstalk, though, is to *know* the crosstalk; this way one is warned for misinterpretations of DPI data.

IV. Injection Set-up And Method

We will discuss three ways of setting up the HF injection and discuss their advantages and disadvantages. Each set-up tries to improve upon the former.

A. IEC 62132-4

The set-up proposed by IEC 62132-4 [11] is shown in Figure 1: it consists of a PCB with the DUT and some peripherals, and a directional coupler that allows for measuring the incident and reflected power. The difference $P_{\text{inc}} - P_{\text{refl}} = P_{\text{trans}}$ is taken to be the power really dissipated by the IC.

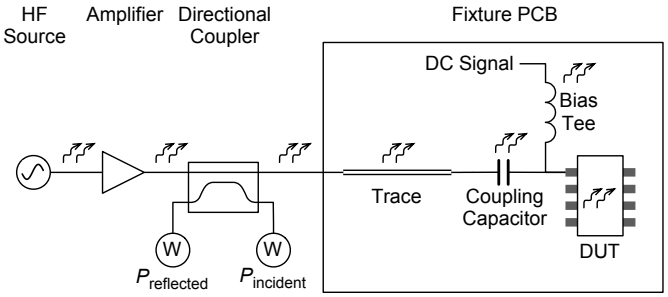


Figure 1. HF injection path of the DPI set-up proposed in IEC 62132-4. The heat waves symbolise lost power. The goal of the set-up is to deliver a known HF power to the IC under test via one particular pin.

In other words, the transmitted power at the output of the directional coupler is considered equal to the transmitted power at the IC pin. This is true to the extent that the on-PCB loss is negligible. For that reason, the standard requires the insertion loss not to exceed 3 dB [11, §7.4].

The great advantage of this approach is that it is simple: one can design a PCB with all necessary periphery, measure incident and reflected power when the DUT fails and register the difference as being $P_{\text{trans,threshold}}$.

With regard to accuracy, there are mainly two critical remarks to be made. First of all, when the PUT is very reflective, $P_{\text{inc}} \approx P_{\text{refl}}$, the watt metre errors dominate the P_{trans} reading. In practical cases the error is the worst for low frequencies, and amounts between $-\infty\,\text{dB}$ and $+8\,\text{dB}$. [12]

Secondly, the PCB loss increases with frequency. In practical cases, in the $1-3\,\text{GHz}$ range, the difference between the true and the measured P_{trans} can go down to $-10\,\text{dB}$. [12]

[1] This simple example supposes all pins to have the same Z_0 impedance.

B. PCB Modelling

An improvement upon both inaccuracies was proposed earlier [13]. The measurement set-up can be the same as in Figure 1, in this proposal, however, only the incident power P_{inc} at failure will be recorded. To obtain the transmitted power P_{trans}, all of the set-up is modelled in SPICE, then simulated with the recorded incident power $P_{\text{inc,threshold}}$, and the transmitted power $P_{\text{trans,threshold}}$ is calculated.

Practically, the used PCB is generic for a particular package, and has almost the same and well known layout for each pin. The layout allows to solder bias tees and other peripheral circuitry for every pin. Passive components that make up the bias tees are separately measured, modelled and entered in the simulation. The DUT is modelled by measuring its S-parameters with a vector network analyser (VNA), after calibrating using a calibration kit that moves the reference plane up to the DUT pins. Finally the S-parameters are converted to a SPICE model with IdEM.

The advantage of this approach is that it improves accuracy by about 10 dB [12]. Furthermore, one can change peripheral passives while experimenting and easily adapt the simulation that translates P_{inc} to P_{trans} accordingly. Of course, a PCB model and a library of trustworthy passive models must be available.

The disadvantage of this approach is that the PCB must be very carefully modelled. For example, neighbouring bias tee capacitors have mutual inductance that cannot be neglected from 1 GHz upwards [14]. Also, the dispersive permittivity must be known to correctly model traces as transmission lines. Furthermore, it is hard to route a generic PCB that has exactly the same layout for each pin, while still providing footprints to solder any peripheral circuitry. Particularly, the fan-out of the traces will quickly impose corners that have different angles for each pin. With rising frequency, these differences have increasing influence.

C. Minimal PCB

Recognising that above problems arise from a dense PCB, we asked ourselves the question: is it really necessary to place all periphery close to the DUT? To investigate the impact, we entered the impedance of the source and load networks specified in Section III-A into an ADS simulation. We then added 5 cm of 50 Ω coplanar grounded waveguide, and compared the impedance shift in Figure 2. The 70 mΩ increase in series resistance is barely visible. Only above resonance, the inductance rises with frequency and then, transmission line resonances appear. In this case, the impedance shift in the functional frequency range is negligible, and the requirements stated in Section III-A are met. We expect this to hold true in general, at least for ICs with moderate functional frequencies (tens of MHz). Therefore, we decide to put the source and load networks off-board.

Now that all peripheral circuitry is placed off-board, the PCB only serves to fan out the DUT pins to connectors. Hence, the peripheral circuitry must be connectorised, too; let us call

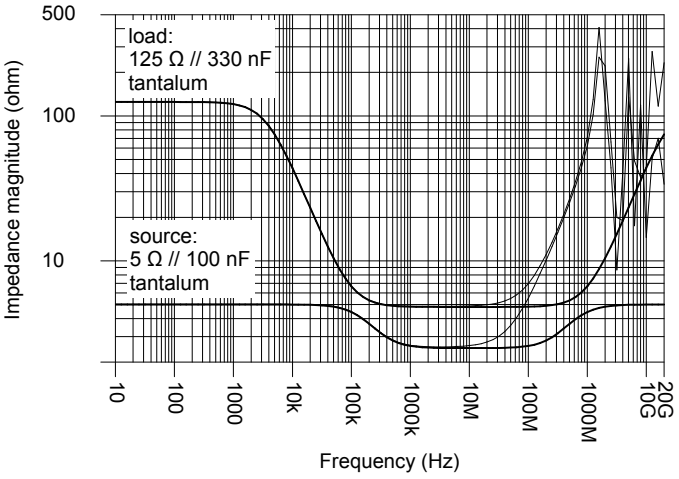


Figure 2. Impedance of specified source and load (thick curves) and the same impedances in series with 5 cm of 50 Ω trace (thin curves).

every connectorised part of the peripheral circuitry a peripheral module. Refer to Figure 3 to see how a DUT, mounted on a fixture may connect to its peripheral modules (i.e. a bias tee, a filter capacitor, a load emulator and a DC block). The peripheral modules may be custom PCBs for a particular DUT, or commercial-of-the-shelf (COTS) modules, which may be reused between DPI set-ups.

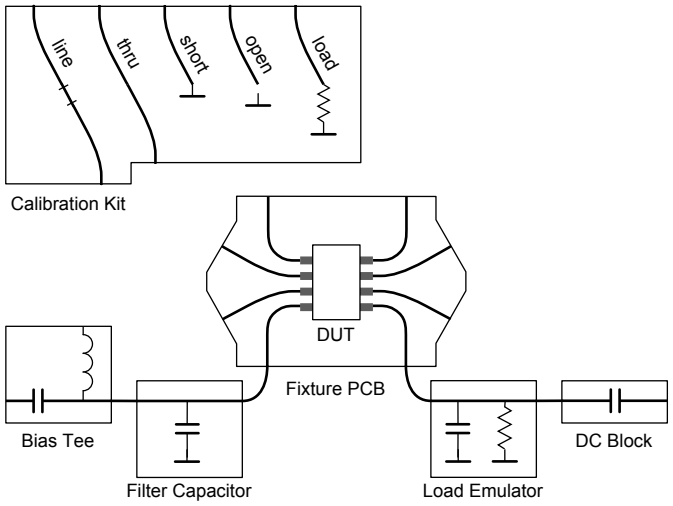


Figure 3. DUT fixture with example periphery. Signal generator and directional coupler not shown.

To know the transmitted power P_{trans}, we propose to measure the S-parameters of all modules and the cables/adapters that interconnect them. Similarly to the previous approach, we only measure the incident power P_{inc} at the generator output, and then calculate the power incident at the PCB by simulation with SPICE/IdEM, MATLAB RF toolbox or Python's `scikit-rf` package [15].

To calculate the power transmitted to the DUT from the power incident on the PCB, we need a model of the DUT and of the feeds that lead to it (a feed consists of a connector and

a trace). We propose to obtain both by means of a calibration. That is, a calibration kit is produced in the same PCB panel as the fixture, in order to closely mimic the feed. The feed is reproduced with different terminations (open, short, load, thru or line) to allow a short-open-load-thru (SOLT) or thru-line-reflect (TRL) calibration. Any VNA can calibrate on these standards and thus extract the S-parameters of the DUT without its surrounding feeds.

The S-parameters of the feeds can be extracted as follows. We here take the simple example of a short-open-load (SOL) calibration with ideal standards, but the same method can be applied to a SOLT or TRL calibration and/or with non-ideal standards. We start by measuring and saving the S_{11}-parameter of the short, open and load standards on the calibration kit. Note that the VNA is calibrated to move the reference plane to the connectors of the calibration kit. The measured S_{11}-parameter of each standard hence describes the feed and the termination (short, open or load). Let the feed be described by $\mathbf{S}$, the reflection coefficient of the termination by Γ. The measured S_{11} parameter then is the apparent reflection coefficient $\hat{\Gamma}$ (cf. Figure 4):

$$\hat{\Gamma} = S_{11} + \frac{S_{21}S_{12}\Gamma}{1 - S_{22}\Gamma}. \tag{1}$$

From the three measured reflection coefficients $\hat{\Gamma}$ of the open, short and load standards $\Gamma = \{+1, -1, 0\}$, one can numerically solve for three unknowns, typically the directivity S_{11}, the source match S_{22} and the reflection tracking product $S_{21}S_{12}$ [16]. As the connector and trace are passive and behave linearly for all reasonable voltages, we know them to be reciprocal: $S_{21} = S_{12} = \sqrt{S_{21}S_{12}}$. This way, we estimate all S-parameters of the feed.

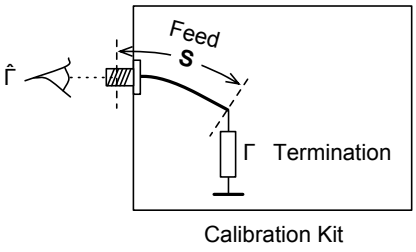


Figure 4. Definition of feed (described by $\mathbf{S}$), termination (described by the reflection coefficient Γ) and the apparent termination (described by the measured reflection coefficient $\hat{\Gamma}$).

Practically, we can let `scikit-rf` perform any calibration (SOL, SOLT, TRL) with ideal or non-ideal standards, extract the found S-parameters and export them to Touchstone format for use as a feed model in IdEM/SPICE or ADS, for example.

The advantage of this approach is that we no longer need to model the PCB(s), but we can base the P_{trans} calculation on measurements only. In case of doubt, or in order to improve the set-up, each module can be separately verified against analytical equations or SPICE simulations. Furthermore, if the peripheral modules are necessary to measure representative S-parameters, they can be incorporated in the VNA calibration.

The disadvantage may be software tool set-up and the instruction of lab personnel.

V. Fixture Design

Recall the goal of the fixture PCB: to connectorise the IC pins with low loss. To only have to calibrate once, the feeds need to be electrically equivalent. Secondarily, to promote experimentation, we would like the fixture to be low-cost.

SOIC8 is a common IC package, for which we already had a generic DPI PCB [10]. In order to perform a cross validation with this PCB, we decided to develop a fixture for the SOIC8 package. Recommended footprints for this package vary and also depend on the industrial soldering technique used. We chose to take a typical maximum pin width 0.5 mm and add 0.1 mm to facilitate DUT placement, without introducing too much coupling uncertainty. The pad length is rather tight with respect to different recommendations: 1.52 mm.

To avoid losing power on a trace-pad discontinuity, we decide to use a waveguide with the same width as the pad. To keep the fixture low-cost, we choose a standard Eurocircuits 4-layer FR4 stack-up [17]. To distribute a ground reference with low impedance, we opt for a ground plane. As the trace will end up on the outer layer, we have the choice between a microstrip and a coplanar grounded waveguide (CPGW). A 0.6 mm microstrip on layer 1 with layer 2 as a ground plane was calculated to have a characteristic impedance of 56.7 Ω, using ADS LineCalc and supposing a permittivity $\varepsilon_r = 4.1$. If we want the CPGW to continue until the IC pads, there needs to be a trace of ground in between the pads, which has a minimum width of 0.15 mm in standard Eurocircuits technology. This implies a maximum lateral gap of 0.26 mm, which corresponds to a 49.8 Ω CPGW, when using layer 2 as a ground plane. For this particular trace width and substrate thickness, the characteristic impedance of a CPGW approaches 50 Ω the closest.

Another advantage of a CPGW is that it has less capacitive crosstalk between neighbouring traces; the ground in between serves as a shield. Furthermore, budget board-edge SMA connectors are available that launch a CPGW wave with a SWR (standing wave ratio) below 1.5 for $18 - 26.5$ GHz [18]. For these reasons, we chose to use a CPGW.

We would like to make a generic SOIC8 fixture PCB, so we need to connectorise all IC pins, four at both sides, with a 1.27 mm pitch. The connectors practically need 1 cm board edge. Consequently, the traces from the pads to the connectors have to fan out. The mildest taper is a circle segment, so we use arc-shaped traces. To keep the feeds electrically equivalent, the centerline length of the arcs must be equal.[2] Consequently, the PCB is not rectangular.

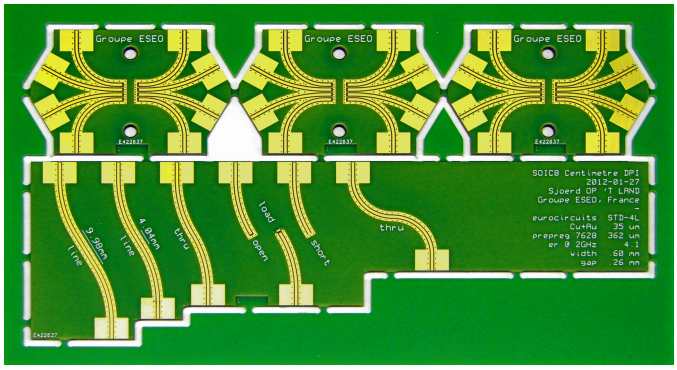
The calibration kit reproduces the feeds with short, open, load, thru and line standards. The load is a 50 GHz 0402 flip-

[2]In fact, conducted waves tend to 'cut the corners'. As a rule of the thumb, the effective length of a microstrip arc is $w\theta/2$ shorter than its centerline length, where w is the trace width and θ is the arc's angle [19]. The CPGW traces in our design are compensated according to this rule.

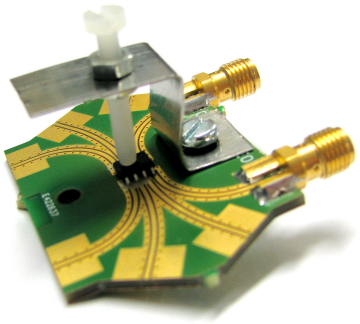
chip 50 Ω resistor [20], that matches the trace width. Line standards are effective for a phase shift between 20° and 160°, and are provided for $1-8$ GHz (9.98 mm) and $2.5-20$ GHz (4.04 mm). A thru standard is provided for both bend radii, to verify that the feeds are indeed electrically equivalent.

Drawing bent traces is possible in some layout tools, such as Altium or ADS, but drawing the corresponding non-rectangular board outline and placing equidistant stitching vias can only be done manually. This laborious task is error-prone and needs to be done over if any elementary parameter changes (trace length, trace radius) or when a fixture for another package needs to be designed.

Therefore, a Python script was written that generates the fixture and calibration kit layout, and exports it in Gerber (layout) and Excellon (drill) format. This script could be reused for other fixture designs. The resulting layout is shown in Figure 5a.



(a) Panel, consisting of one calibration kit and three fixture PCBs.



(b) One fixture with steel spring and nylon bolt. Pin 1 and 8 are connectorised, all other pins are shorted to ground with silver conductive pen.

Figure 5. Realised fixture.

VI. Results

As a simple way of gauging the feed loss, we measure the S_{21} parameter of the thru standards on the calibration loss. The large radius thru transfer amounts -3.7 dB at 20 GHz (Figure 6), which suggests a feed loss of 1.9 dB. The small radius thru transfer differs maximally ± 0.3 dB and $+3$ ps (equivalent to 1.5 mm) from the large radius thru.

To validate our proposed calibration method, we measure the short, open, load, thru and line standards, and extract

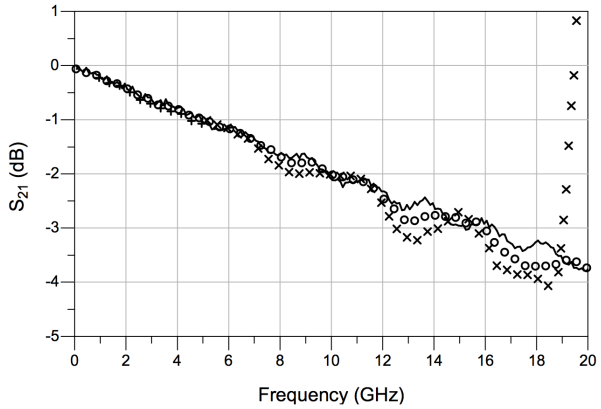


Figure 6. Measurement of the S_{21} parameter of the large radius thru (solid line). Circuit simulation of thru by connecting two feed models back-to-back, where the feed models are obtained by measuring SOLT (○), TRL $1-8$ GHz (+) and TRL $2.5-20$ GHz (×) standards and extraction according to Section IV-C.

a feed model as described at the end of Section IV-C. We then cascade two feed models back-to-back in ADS and then simulate the end-to-end transfer; if the feed model is good, this transfer should correspond to the measured thru transfer. The simulation results are compared with the large radius thru measurement in Figure 6. The feed model based on SOLT measurements results in a transfer that deviates maximally 0.5 dB over the $0-20$ GHz frequency range. When the second line standard surpasses 150°, it starts to deviate heavily.

In order to understand the source of the deviations, we check the step response of the SOL standards with a time domain reflectometer (TDR). As we know the propagation velocity, we can map the round-trip-time to a physical position along the line, see Figure 7. We notice that the standards differ about 5 Ω just after the board edge at 70 ps, and we conclude that the soldering is not consistent from standard to standard.

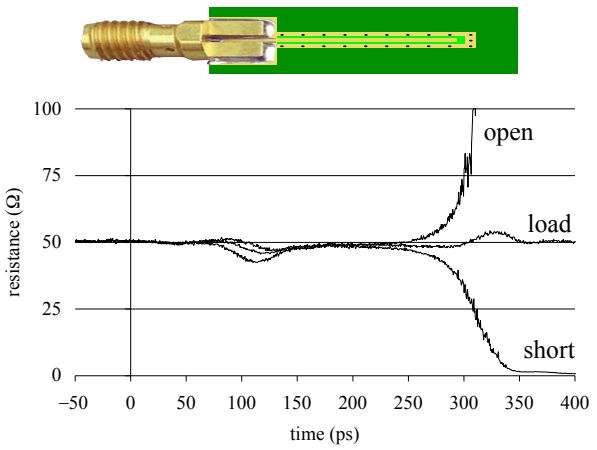


Figure 7. Time domain reflectometry of the short, open and load standards (rise time of 35 ps). The image of the open standard is warped according to ADS LineCalc delay data, $t = 0$ ps corresponds with the SMA reference plane.

It is physically impossible to directly measure the far-end crosstalk, because there is no place for two SMA connectors

next to each other at the place of the DUT. Therefore we perform an electromagnetic simulation of the PCB with Agilent Momentum and obtain about −25 dB far-end crosstalk (and −19 dB worst case at 14 GHz) between a neighbouring large radius and small radius feed. To roughly validate the simulation, we cut the fixture in half and short the IC pads with copper tape, and also simulate the near-end crosstalk with all far-ends shorted to ground. The results are compared in Figure 8. We notice that, on average, the simulation is 5 dB too optimistic. We conclude that the far-end crosstalk of the fixture may be about −20 dB with worst case peaks of −14 dB.

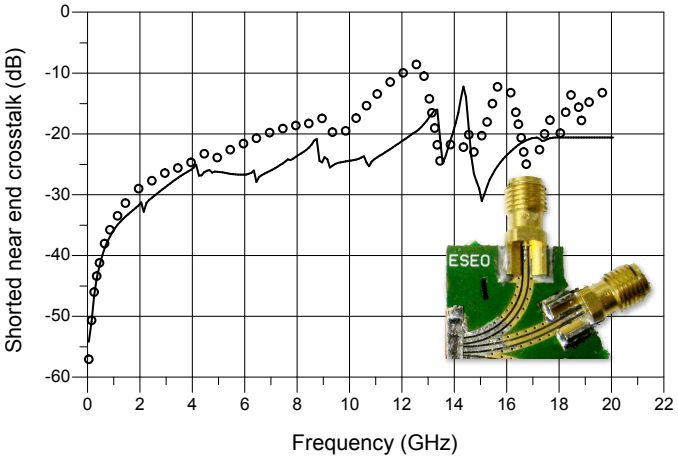


Figure 8. Measurement (○) and Agilent Momentum electromagnetic simulation (solid line) of the near-end crosstalk between a neighbouring large radius and small radius feed, with all far-ends shorted to ground.

VII. Conclusions and Recommendations

It is not functionally necessary to place all peripheral circuitry on a DPI test PCB, so we developed a simple fixture that only connectorises a SOIC8-packaged IC. To know the HF power transmitted to the DUT in a DPI test to within about ±0.3 dB, one can simple measure the SOLT standards that represent the feed and extract the S-parameters of the feed.

Our fixture uses budget SMA connectors on a standard FR4 substrate and has a feed loss of 1.9 dB at 20 GHz. The worst case far-end crosstalk between neighbouring traces is estimated to be about −14 dB. The reproducibility of the feed is limited by the consistency of the connector-PCB soldering.

The logical next step would be to use this fixture to actually perform DPI measurements. It would be interesting to see what conducted immunity issues appear beyond 1 GHz, and whether the proposed method works in practice and with more complicated ICs.

The fixture itself can also be improved: a smart soldermask could be used to make the soldering more consistent. Soldering with a silver solution might also prove more robust to mechanical stress.

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References

[1] Olivier Maurice and Jacques Pigneret. “Digital circuit susceptibility characterization to RF and microwave disturbances”. In: *Radiation and Its Effects on Components and Systems, 1997. RADECS 97. Fourth European Conference on*. 1997, pp. 178 –181. DOI: 10.1109/RADECS.1997.698884.

[2] Johan Loeckx. “Methods for simulating and analysing the effects of EMC on Integrated Circuits”. PhD thesis. Katholieke Universiteit Leuven, 2010.

[3] C. McConaghy. *Microwave component susceptibility, FY86: Final report*. Tech. rep. UCID-20923. Lawrence Livermore National Lab., CA (USA), 1986. URL: http://www.osti.gov/energycitations/product.biblio.jsp?osti_id=6760696.

[4] R. Perdriau et al. “Exploration of radiated electromagnetic immunity of integrated circuits up to 40 GHz”. In: *Electronics Letters* 47.10 (Dec. 2011), pp. 589 –590. ISSN: 0013-5194. DOI: 10.1049/el.2011.0333.

[5] Mohamed Ramdani et al. “The Electromagnetic Compatibility of Integrated Circuits — Past, Present, and Future”. In: *IEEE Transactions on Electromagnetic Compatibility* 51.1 (2009), pp. 78–100. ISSN: 0018-9375. DOI: 10.1109/TEMC.2008.2008907.

[6] Fujitsu. *Flip-Chip Ball Grid Arrays*. URL: http://www.fujitsu.com/downloads/MICRO/fma/pdf/fcbga.pdf.

[7] Y.P. Zhang and Duixian Liu. “Antenna-on-Chip and Antenna-in-Package Solutions to Highly Integrated Millimeter-Wave Devices for Wireless Communications”. In: *Antennas and Propagation, IEEE Transactions on* 57.10 (2009), pp. 2830 –2841. ISSN: 0018-926X. DOI: 10.1109/TAP.2009.2029295.

[8] *Antenna in Package Design Methodology*. URL: http://www.insightsip.com/images/stories/download/technical_documentation/aip_methodology_whitepaper_isip.pdf.

[9] *LM78LXX Series 3-Terminal Positive Regulators*. Texas Instruments. 2012. URL: http://www.ti.com/lit/ds/symlink/lm78l05.pdf.

[10] F. Lafon et al. “Immunity Modeling of Integrated Circuits: an Industrial Case”. In: *IEICE Transactions on Communications* E93-B.7 (2010), pp. 1723–1730.

[11] *IEC 62132-4 Integrated circuits - Measurement of electromagnetic immunity 150 kHz to 1 GHz - Part 4: Direct RF power injection method power injection method*. IEC, 2005.

[12] Frédéric Lafon et al. “Extending the Frequency Range of the Direct Power Injection Test: Uncertainty Considerations and Modeling Approach”. In: *EMC Compo 2009*. 2009.

[13] Frédéric Lafon et al. “An Industry-Compliant Immunity Modeling Technique for Integrated Circuits”. In: *2009 Kyoto International Symposium on EMC*. 2009.

[14] Frédéric Lafon. “Techniques and methodologies development to take into account EMC constraints in automotive equipment design”. PhD thesis. INSA Rennes, 2011.

[15] *scikit-rf 0.1*. URL: http://packages.python.org/scikit-rf/.

[16] Doug Rytting. *Network Analyzer Error Models and Calibration Methods*. Presentation. 2002. URL: http://www-ee.uta.edu/online/adavis/ee5349/NA_Error_Models_and_Cal_Methods.pdf.

[17] Eurocircuits. *Standard board build up 0-8 layers*. URL: http://www.eurocircuits.com/index.php/technology-guidelines/pcb-multilayer-build-ups.

[18] *Johnson High Frequency End Launch Connectors*. Catalogue. 2005. URL: https://emersonconnectivity.com/OA_MEDIA/catalog/pdf_endlaunchBROCHUREFINAL.pdf.

[19] *Bends in transmission lines*. Microwaves101 Online Encyclopedia. 2011. URL: http://www.microwaves101.com/encyclopedia/mitered_bends.cfm.

[20] *Thin Film Microwave Resistors*. Vishay Sfernice. URL: http://www.vishay.com/docs/53014/ch.pdf.