
# ICECS 2012

## 19th International Conference on Electronics, Circuits, and Systems

*Seville, Spain*
*December 9 -12*

# *Proceedings*



IEEE Catalog Number: CFP12773-USB
ISBN: 978-1-4673-1259-2



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# Sense/Drive Architecture for CMOS-MEMS Accelerometers with Relaxation Oscillator and TDC

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***Abstract*—This paper reports a mixed-signal architecture for capacitive accelerometers conditioning based on capacitance ratio to frequency conversion and high-precision digital frequency demodulation with coarse-fine time-to-digital converter (TDC) and delay-locked loop (DLL). Furthermore, the front-end has a capability to apply pulse-controlled electrostatic actuation which can be used for the accelerometer self-test or for closed-loop operation if an external digital feedback controller is added. Since the design is dominated by standard digital circuitry, the presented concept allows rapid prototyping, what is especially important in case of microsensors monolithically integrated in advanced CMOS processes where classic analog circuits are difficult to scale-down.**

***Index Terms*—Accelerometer, CMOS-MEMS, Surface Micromachining, Inertial Sensor, Relaxation Oscillator, Tapped Delay Line, Time-to-Digital Converter, TDC**

## I. Introduction

MEMS (micro electromechanical systems) accelerometers are currently becoming more and more ubiquitous devices. Especially rapid growth in the consumer electronics applications strongly encourages to find cheap and short time-to-market solutions for accelerometer design and production.

A possible way to meet these requirements is full integration of MEMS and standard CMOS electronics fabrication by means of standard CMOS metal layer micromachining. The mechanical performance and reliability are so far much worse than in case of custom MEMS processes. Despite this, in many high-volume noncritical applications the advantages of such devices like very low-cost unitary price, possible integration in a complex system-on-chip (e.g. single-chip wireless sensor node), smaller parasitics and mechanical feature size can outweigh the drawbacks.

State-of-the-art electronic interfaces for capacitive MEMS accelerometers are usually complex mostly-analog circuits. The most common sensing architectures are based on continuous-time voltage synchronous modulator/demodulator [1] or switched-capacitors charge amplifier [2]. Despite providing very good performance (electronic noise approaches the mechanical noise), they are hardly scalable to modern CMOS nodes, since all the critical blocks are analog. Even more, usually an additional analog-to-digital converter or embedding the sensor into a mechanical delta-sigma loop [3] is required to provide a digital output.

An approach addressing these issues is presented in this work. By using little amount of relatively simple on-chip analog electronics (comparators and charge-pump for DLL, current-starved inverters and some switches) and implementing a significant part of the circuit using standard digital flow (digital decoder) or as a regular array of simple semi-custom cells (delay line), we obtain easily scalable design and portable architecture between deep-submicron and nanometric CMOS processes. Application of on-chip time-to-digital converter (TDC) [4] improves the standard digital demodulation method based on counters [5], and offers performance competitive with other state-of-the-art solutions.

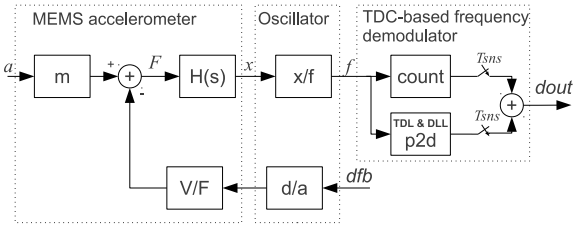


Fig. 1. Block diagram of the presented architecture.

The paper is organized as follows. In the second section the main concept of the architecture is sketched, including a brief descriptions of its main blocks and most important details of their implementation. In the following section a physical design is shown; also some simulations and performance estimations are demonstrated. Finally, the conclusion is stated.

## II. Architecture

The block diagram of the presented architecture is depicted in Fig. 1. In open loop, the MEMS accelerometer converts the input acceleration $a$ into the proof mass displacement $x$, which defines the capacitance ratio controlling the relaxation oscillator frequency $f$ – the time reference for coarse-fine TDC. By measuring constant sensing time $T_{sns}$, the TDC effectively returns fractional number of oscillation periods during $T_{sns}$ and its output *dout* is an average digital value of $f$ over $T_{sns}$. The integer component of *dout* (number of full oscillator period during $T_{sns}$) comes from synchronous counter. The fractional component is obtained by phase quantization at the end of the sensing time (fine calculation), which is performed by strobing the tapped delay line (TDL) state. TDL is enclosed in a delay-locked loop (DLL), that adapts its delay to $1/f$. Finally, sensing can be time-multiplexed with pulse-width/density-modulated (PWM/PDM) electrostatic actuation signal *dfb*, allowing the self-test or closed-loop operation if an external digital feedback controller is added.

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### A. CMOS-MEMS capacitive accelerometer

The presented architecture fits to any kind of accelerometer based on differential capacitive half-bridge, like comb in-plane or three-plate out-of-plane devices. The goal application of the architecture are CMOS-MEMS integrated devices of both types, that are going to be built of standard CMOS interconnection metals and released using isotropic oxide etching, where promising results have been reported [6, 7].

The dynamic behavior of an accelerometer can be very well approximated with a simple second-order mass-spring-damper system, which in the Laplace domain is given by the following equation:

$$H(s) = \frac{x(s)}{a(s)} = \frac{1}{s^2 + \frac{b}{m}s + \frac{k}{m}} \tag{1}$$

where $a$ is the input acceleration, $x$ is the displacement of the proof mass $m$, $b$ is the damping coefficient and $k$ is the spring constant. Assuming frequencies below the resonance peak, the displacement of the proof mass is proportional to the input acceleration:

$$x \approx -\frac{m}{k}a = -\frac{1}{\omega_0{}^2}a, \tag{2}$$

where $\omega_0$ is the device undamped resonant frequency. The displacement changes the half-bridge $C_{top}$ and $C_{bot}$ capacitances:

$$C_{top} = \frac{\varepsilon A}{d_0 - x}; \quad C_{bot} = \frac{\varepsilon A}{d_0 + x}, \tag{3}$$

where $A$ is the capacitor area, $\varepsilon$ is the permittivity of a medium between the plates (air by default), and $d_0$ is the zero-acceleration gap of the capacitor.

In addition, an electrostatic force can be applied by voltage-driving the accelerometer electrodes:

$$F_{el} = \frac{1}{2}\varepsilon A \left( \frac{V_{tm}^2}{(d_0 - x)^2} - \frac{V_{bm}^2}{(d_0 + x)^2} \right), \tag{4}$$

where $V_{tm}$ is top-mid voltage and $V_{bm}$ is bottom-mid voltage.

### B. Oscillator

The signal processing starts with a relaxation oscillator controlled by the accelerometer capacitance ratio. The oscillator (Fig. 2) is based on a topology for differential capacitive sensors [8] upgraded by using sawtooth oscillation scheme, which improves the noise performance [9]. Simple differential-pair based comparators are applied. In addition to the basic sensing oscillation mode, the circuit has reset/shut down and PWM/PDM force-feedback modes, described in the following.

*1) Sensing mode:* A transient simulation showing the oscillator working principle can be seen if Fig. 2. The oscillator output signal *osc* controls the switches charging the integrating capacitors $C_1$ and $C_2$ and switches connecting the supply and ground to the accelerometer *top* and *bot* nodes, that form the capacitive half-bridge inputs. The accelerometer *mid* plate is a bridge output node. The square wave voltage amplitude of this node is a function of the capacitance ratio inside the accelerometer, hence the proof mass position and acceleration. Then, the amplitude is converted to a time interval by detecting the crossing with a ramp voltage generated with one of the integrating capacitors $C_1$ and $C_2$. The crossing detection by a comparator changes the oscillator output and the other half-period begins. Ideally, if crossing detection delay is neglected, the output frequency is given by:

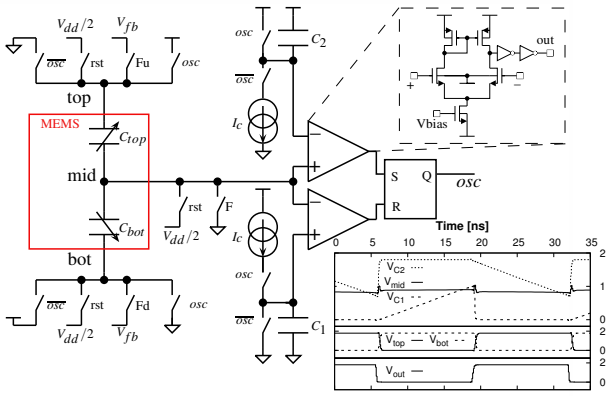


Fig. 2. Sensing oscillator topology including schematic of the comparator circuit, and transient simulation of oscillator internal voltages demonstrating its working principle.

$$f = \frac{I_c}{2C_I V_{dd}}\left(1 + \frac{C_{bot}}{C_{top}}\right) = \frac{I_c}{C_I V_{dd}}\left(\frac{d_0}{d_0 + x}\right) \tag{5}$$

where $I_c$ and $V_{dd}$ are the charging current and supply voltage respectively, while $C_I = C_1 = C_2$.

In practical cases $x \ll d_0$, therefore (5) becomes:

$$f \approx \frac{I_c}{C_I V_{dd}}\left(1 - \frac{x}{d_0}\right) = f_0\left(1 + \frac{ma}{kd_0}\right) \tag{6}$$

where $f_0$ denotes a zero acceleration frequency.

*2) Reset/shut down mode:* In order to remove the charge from the high-impedance *mid* node, a periodic reset is performed. During this state all the terminals of the MEMS device are clamped to $V_{dd}/2$, and the integrating capacitors are discharged.

*3) PWM/PDM self-test/closed-loop actuation mode:* During this mode, the integrating capacitors are discharged and the accelerometer *mid* node is grounded. The force pulses are applied by clamping one of the *top* and *bot* nodes to the ground, while the other one to the constant $V_{fb}$ voltage, which can exceed supply voltage to provide sufficient force feedback dynamic range. Assuming the pulse frequency is much higher than the accelerometer bandwidth and mass displacement much smaller than the MEMS gap $d_0$, the equivalent acceleration generated by a feedback pulse is given by the following expression:

$$a_{fb} = K\frac{\varepsilon A {V_{fb}}^2}{2m{d_0}^2} \tag{7}$$

where $K$ is the pulse duty cycle.

### C. Coarse-fine TDC

A TDC circuit (see Fig 3) is built of 11-bit synchronous counter, 144-tap voltage-controlled TDL embedded in charge-pump DLL, counter sampling-and-synchronizing block and TDL decoder. A selection between 64- or 128-bit mode depending on the input frequency range is provided. When the loop is locked, the output of 128th (64th) cell is delayed

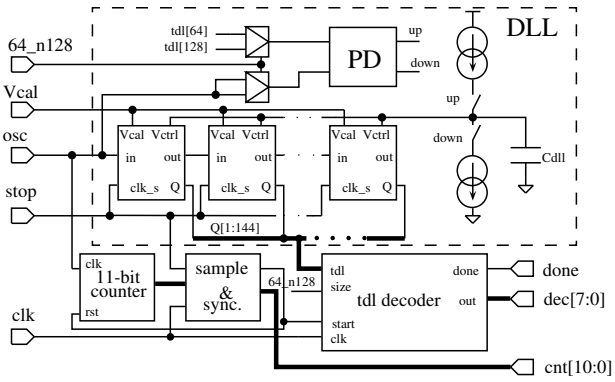


Fig. 3. Simplified schematic of applied TDC.

by 360° with respect to the oscillator output. In order to guarantee capturing the full period in case of positive delay offset, additional cells (133 to 144 or 65 to 72) are used for the further decoding.

The delay cell is formed by a current-starved inverter pair (Fig. 4). The delay is controlled by a gate voltage of two NMOS transistors pairs. One pair is used for calibration and control of the maximum cell delay, another one is driven by the charge pump output voltage. Each cell input is loaded by a D-latch. In order to balance the delay of the falling and rising edges, the intermediate node connecting current-starved inverters is additionally loaded by a dummy inverter.

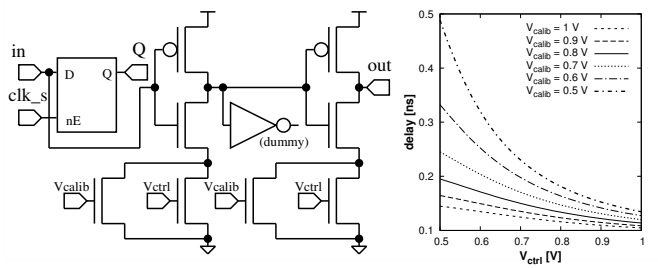


Fig. 4. Delay cell schematic and its delay vs. control voltage characteristic.

Since accelerometer bandwidth is not bigger than a few kilohertz, while the oscillator frequency is tens of megahertz, if sufficient locking-range is provided, the DLL can easily adjust the total delay of TDL to the oscillator period $1/f$ (time reference for TDC). With these assumptions, the TDL forms an oscillator phase quantizer and by applying measurement of constant time $T_{sns}$ defined as a time difference between rising slopes of *stop* and *rst* signals (generated from an external reference clock), a precise digital demodulation scheme is obtained. The digitized value of the average oscillator frequency in the $i_{th}$ sampling period can be calculated by:

$$f_i = \frac{n_i + \frac{m_i}{M}}{T_{sns}}, \tag{8}$$

where $n_i$ is the latched counter value, $m_i$ is the latched TDL value (after decoding), $M$ is an effective length of the delay line (the number of cells delaying the oscillator output by one period) and $T_{sns}$ is the sensing time (see Fig. 5). If $M = 2^K$,

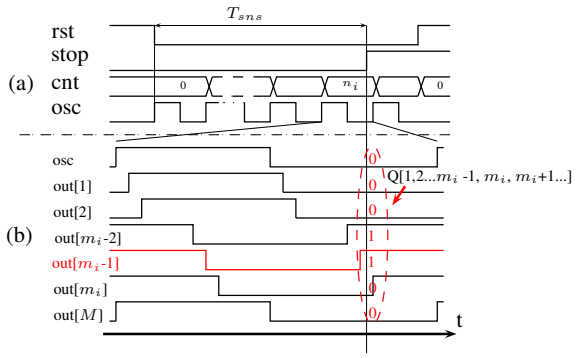


Fig. 5. Measurement cycle: (a) coarse counting of full oscillator periods, (b) zoomed-in final oscillator period and slope propagation in the delay line. Fine measurement is done by latching the delay line state (bus $Q$) with sampling clock edge and detecting in the bit patterns the transition from series of ones to series of zeros. In the presented example, the decoder returns $m_i$. DLL preserves one oscillator period delay of the $M^{th}$ cell output.

where $K$ is a natural number, hardware implementation of (8) is trivial:

$$f_i = \frac{1}{2^K T_{sns}}(2^K n_i + m_i) \tag{9}$$

The oscillator pulse counter, sampler-and-synchronizer block and TDL-decoder form the semi-custom digital part of the TDC. In order to avoid error in case of counter sampler setup/hold violation and to solve issues related to synchronization between *stop* and decoder clock *clk*, a result-consistent sampling scheme is used [10]. The TDL decoder detects the position of the first transition from the series of ones to the series of zeros (see Fig. 5). This position is a fine estimation of the phase difference between the arrival of the latest *osc* rising edge in the counter and the *stop* rising edge. In order to perform this task, a specific hardware algorithm based on line contents correlation with a bit mask containing series of ones and series of zeros has been implemented. The algorithm is robust with respect to some spurious errors in the line as well as the delay offset.

## III. Design, Simulations and Results

### A. Chip design

A test-chip has been designed in 150 nm CMOS technology with six metal layers and thick metal. The chip contains a set of CMOS-MEMS accelerometer prototypes integrated with the front-end described in this paper. The digital part was described in VHDL and synthesized with Cadence RTL Compiler and Encounter Digital Implementation for maximum $f$ and *clk* frequency of 200 $MHz$. The TDL was done as a regular repetition of custom delay cells compatible with standard-logic cells grid. The remaining parts of the DLL and the oscillator were prepared fully-custom. In order to reduce substrate coupling between the digital core and the other blocks, a deep n-well isolation was used to separate digital ground. The layout is shown in Fig. 6.

### B. Simulations and performance estimations

In Fig. 7, a post-layout transient simulation of the front-end response to self-test 3.3 $V$ PWM drive with a duty cycle of 5% (max. 50%) equivalent to $-4.3\,G$ acceleration step, is shown.

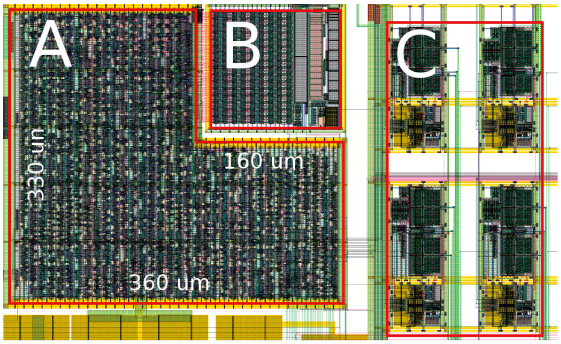


Fig. 6. Presented architecture has been implemented in $0.15\mu m$ technology. A – TDC digital core including chip configuration unit and serial data output interface, B – TDL and DLL, C – four oscillators connected to some test MEMS structures or pads. The two oscillators on the top have slightly different topology to support accelerometers with asymmetrical capacitances.

The parameters of Verilog-A accelerometer model were set in accordance with the estimations made on one of the integrated accelerometer prototypes as follows: $d_o = 1\,\mu m$, $k = 1.1\,N/m$, $m = 0.78\,\mu g$, $f_0 = 5.9\,kHz$, $C_0 = 128\,fF$. Obtained zero-acceleration frequency is $f_0 = 38.85MHz$ with an oscillator charging current $I_c = 50\mu A$ ($C_I = 500\,fF$) and comparator current $300\,\mu A$. The TDC sensing time $T_{sns}$ is $5\,\mu s$, and is time-multiplexed with oscillator PWM driving mode of the same duration. With these settings the frequency LSB of digital output is $1.56\,kHz$ what is an equivalent of 0.009% of relative capacitance change and $7.64\,mG$ acceleration LSB for the simulated accelerometer. Oscillator jitter is expected to worsen the performance, however due to the averaging nature of the pulse counting its impact is not going to be critical. The simulated INL and DNL of the delay line due to mismatch and ramp shape of the control voltage is within one LSB. The INL that can appear due to a constant delay offset can be easily removed by further processing stages.

The presented results are just a proof of concept and do not set the performance limit of the architecture. By extending $T_{sns}$ or reducing the sampling rate by decimation, better resolution can be obtained. An improvement can be also made by adding an external controller and closing the feedback loop, so that a mechanical sigma-delta modulator would be obtained.

## IV. Conclusion

In this paper, a relaxation oscillator and TDC-based mixed-signal architecture for capacitive microaccelerometers was presented. The main novelty, apart from the relaxation oscillator with sawtooth topology, controlled by the differential capacitive sensor and allowing PWM time-multiplexed actuation, is the digital demodulation scheme employing coarse-fine TDC with DLL. This improves the digital output accuracy in comparison to bare pulse counting, thus relax the clock and oscillator frequency requirements.

Fair output resolution despite moving the circuit *center of gravity* from a standard analog to the time-interval/frequency and digital processing makes the architecture especially attractive for accelerometers integrated monolithically with advanced CMOS technologies.

The test-chip has been taped out and as soon as the chips are available, the concept is going to be experimentally verified.

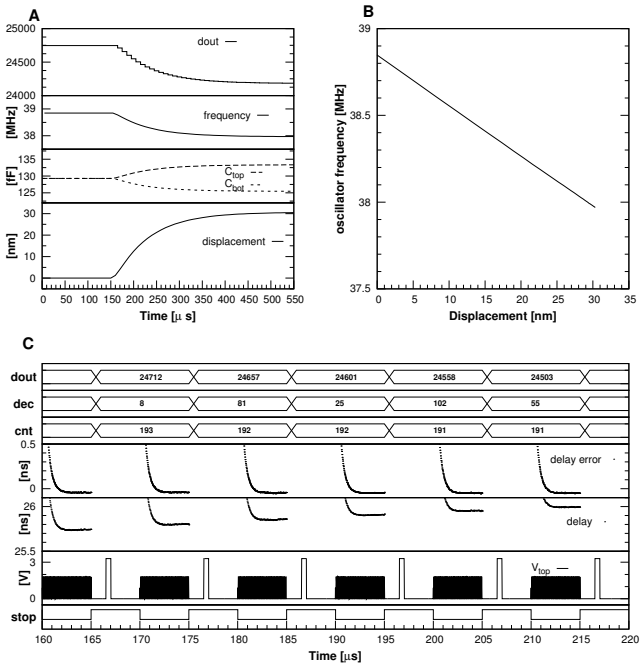


Fig. 7. Post-layout simulations of oscillator and TDC connected to a MEMS accelerometer (Verilog-A model). A - response of the accelerometer, oscillator and TDC on the self-test $3.3\,V$ PWM driving pulses equivalent to $-4.3\,G$ acceleration; B - frequency vs. mass displacement plot obtained from A; C - time multiplexing of drive and sense modes, and oscillator tracking by DLL.

## Acknowledgement

This work was supported in part by the Spanish Ministry of Science and Innovation under Projects TEC2008-06028 and TEC2011-27047, and the European Social Fund (ESF). Piotr Michalik holds an FPU scholarship of the Spanish Ministry of Education.

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