

All optical implementation of a stochastic logic gate using a VCSEL with external optical injection

Sandro Perrone, Cristina Masoller & Ramon Vilaseca

Departament de Fisica i Enginyeria Nuclear, Universitat Politècnica de Catalunya, Colom 11, 08222 Terrassa, Spain

Abstract—We perform numerical simulations of the dynamics of two VCSELs optically coupled in a master-slave configuration. We show that the interplay of nonlinearity and spontaneous emission noise can yield logic behavior, and the emergent outcome of such system is a reliable logic gate. Specifically in our case represents an all-optical logic gate, with the logic input encoded in the strength of the light injected in the slave laser by the master laser, and the fast and robust response decoded from the polarization state of the light emitted by the slave laser.

Keywords—VCSELs, polarization bistability, polarization switching, optical injection

I. INTRODUCTION

In nonlinear systems the interplay of bistability and noise can result in non-trivial noise-induced effects that can potentially be exploited for applications [1]. A recent example is the numerical demonstration of the implementation of a stochastic logic gate using a vertical-cavity surface-emitting laser (VCSEL) by exploiting the interplay of polarization bistability and noise [2]. In Ref. [2] the logic input was encoded in the laser injection current and the logic output was decoded from the polarization of the emitted light. The aim of the present work is to explore an all-optical implementation of the VCSEL-based logic gate. With this aim we study numerically the polarization-resolved dynamics of a VCSEL that receives optical injection from another laser (master-slave configuration). We demonstrate the phenomenon of logic stochastic resonance (LSR), by which the slave laser gives a robust polarization response to two logic inputs directly encoded in the strength of the polarized light injected from the master laser.

Our simulations show that for adequate parameters the polarization of the slave laser switches between two linear orthogonal polarizations (referred to as X and Y) in response to changes in the injection strength of the master laser. Three injection levels allow codifying the input combination of OR or AND logic gates, and the laser polarization the logic output, as displayed in Table 1: the output light polarizations decrypt the logic response as 1 for X-polarized light and 0 for Y-polarized light.

OR Logic Gate		Output Laser Response	Input combination codified with level
Inputs		Output	
1	1	1	X mode
1	0	1	X mode
0	1	1	X mode
0	0	0	Y mode

Table 1 Input combinations for an OR gate codified with injections strength of master laser, E1, E2, E3, and response polarization which decodifies the logic response (X=1, Y=0).

The spontaneous emission noise is a key parameter for the correct operation of the stochastic logic gate. Figures 1 and 2 show the temporal behavior of the output response modes along X and Y direction, with very low and high noise strength respectively. Clearly, the presence of noise helps to switch in a bistable system such as is a VCSEL laser. In Fig. 1, the asterisks represents bits evaluated wrong with a criteria 80-20 (by this criterion the polarization response is considered positive if at least 80% of total power as sum between X and Y polarization, during the bit time, is emitted along the correct polarization). It is clear that these mistakes are due to the delay in the switching events, as the response is not so fast in becoming higher than the energy barrier. But adding white noise provides a fast energy impulse to switch to the other state.

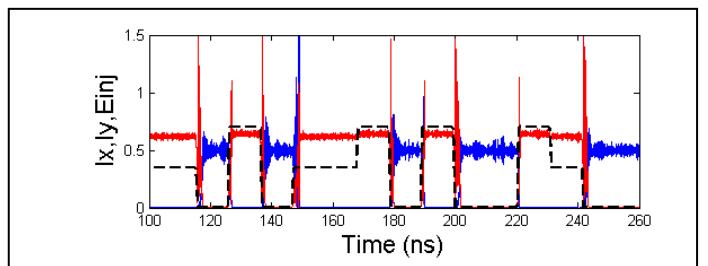


Figure 1. Intensities of the polarization modes x (red line) and y (blue line) in the output of the Slave Laser. Black dashed line represents the injection strength light along the y direction by the Slave laser. All the parameters values were taken such as Ref[2]. $\gamma_a=0.5$; $\gamma_s=50$; $\gamma_n=1$; $\gamma_P=50$; $K=300$; $\alpha=3$; $D=1e-7$; $P/P_0=0.007$; $\Delta P/P_0=0.007$.

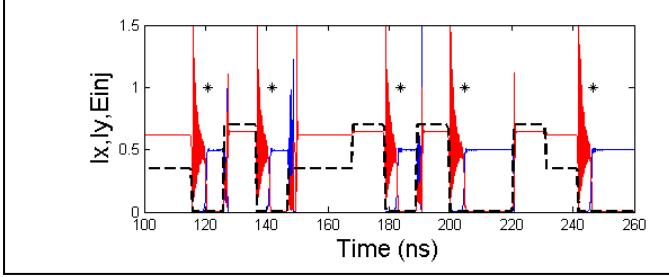


Figure 2. As Fig. 1 but with noise strength $D=1e-2$, without wrong bits.

Figure 3 shows the probability of success of an OR logic gate as a function of the bit time. It is clear how for the 70-30 criterion the probability goes to 1 for smaller bit times. We can even observe that the minimum bit time whose probability goes to one for 80-20 criterion is around 15-20 ns, which is almost half time compared with the response in the setup of Ref.[2], where the input was applied to the laser current.

Figure 4 shows the probability of success of an OR logic gate as a function of the noise strength. The probability of a correct response has a wide region where is equal to 1, but on the other hand, counter intuitively, when the noise is almost absent the probability of success decreases smoothly.

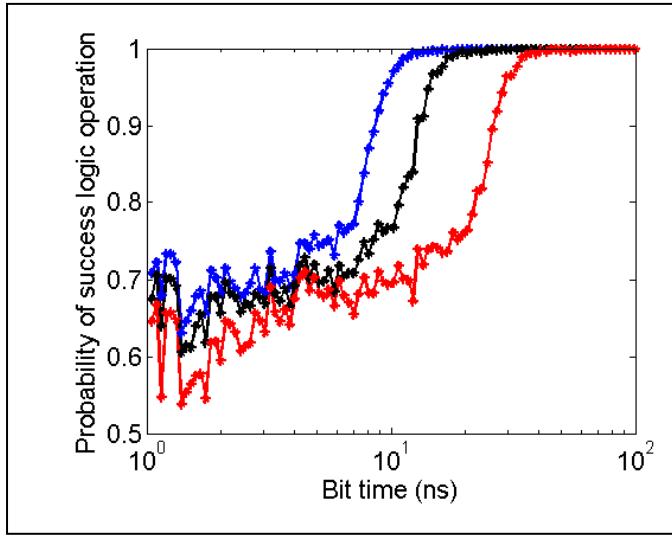


Figure 3. Probability of success of logic OR operation as function of the bit time. Red line is plotted using 90-10 criteria, black line by 80-20 and blue line by 70-30 criteria. The noise strength used is $D=1e-4$, the other parameters are as in Fig. 1. The probability is calculated over 1000 bits.

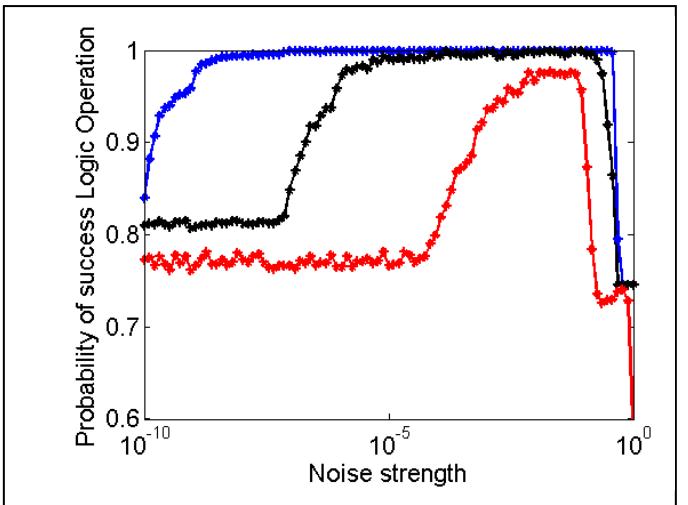


Figure 4. Probability of success of logic OR operation as function of the noise strength D . Red line is plotted using 90-10 criteria, black line by 80-20 and blue line by 70-30 criterion. The bit time used is 20 ns, other parameters are as in Fig. 1. The probability is calculated over 1000 bits.

CONCLUSIONS

We have shown numerically that in a master-slave configuration made by VCSEL laser, there is a wide region of noise strength where the probability of success of logic gate operation function is equal to 1 (see Fig. 3). Thus definitely, the noise help to improve the performances of the stochastic logic gate, giving a reliable and correct logic response, evenly robust to variations of the laser parameters. Actually, in the temporal series of the polarizations intensities (Fig. 1 and 2), for low noise strength, some mistakes appears due to the switching delay between polarizations and input control which highlight as the systems have a stochastic dependence induced by the presence of noise such as in a double well system. In the solitary laser configuration (Ref. [1]) the minimum bit time to get a probability of success equal to 1 is around 30-40 ns, whereas in our numerical calculations we got a probability equal to 1 for shorter bit time as 15-20 ns (see Fig. 3). Besides, considering that the switching time scale is faster than in previous implementation (Ref. [1]) with a three-level modulation of the VCSEL current, the master-slave configuration presents a clear advantage for applications where high switching frequencies are required.

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