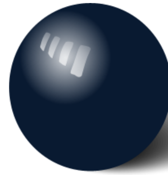

PROJECT: TERASCALE RELIABLE ADAPTIVE MEMORY SYSTEMS
FP7-INFSO-IST-248789

PROCESS VARIABILITY IN SUB-16nm bulk CMOS technology

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Table of Contents

1. Introduction 1
2. Variability scenarios 2
 2.1. Objectives and introduction 2
 2.2. Variability scenarios 2
3. References 5

1. Introduction

The aim of WP3 is to deliver key mechanisms to mitigate and reduce variability and increase reliability at layout, circuits and system level, as well as to determine and propose innovative compensating and fault tolerant techniques considering the PVT variability and corresponding yield impact. The key effects of that environmental fluctuations and process variations are exposed in this deliverable. These objectives will be developed during the second and third year of the project, milestones 4 to 8. Figure 1 shows the global framework of technologies and cell type objective of Work Package 3 (WP3). At device level we differentiate between devices modelled by TRAMS whose characteristics as well as variability and reliability performances are a goal of the project (Bulk CMOS is scheduled for M12 (Milestone MS2), Finfets for M18 (Milestone MS3), CNT for M18, the rest for M30 (Milestones MS5,6)) and medium/long term technology devices with promising characteristics for memory systems that although they are not objective of device modelling in TRAMS they will be considered at a exploratory level at circuit and system level (Task 2.3, M36). In this last set of technologies we will include Metal-Insulator-Metal devices (MIMs) [1], RRAM [2], electromechanical CNT arrays (MCNT) [3], Nanobridge devices [4], Metal-Insulator-Semiconductor (MIS) [5], Phase change memories (PCM) [6], Ferromagnetic RAMs [7], MRAM [8] and other devices. The objective of T2.3 will be the analysis of new memory cells such as 1T-SRAM and CB. In this first year and in relation with deliverable D3.6, Task 3.1 has been dedicated to evaluate the impact of the PVT variations in a set of SRAM and DRAM cells (red boxes in Figure 1), using device models previously available (PMT for Silicon and Stanford for CNTFET) and including the new and original results from WP1 with the device modelling and variability evaluation from 18 and 13 bulk CMOS technologies.

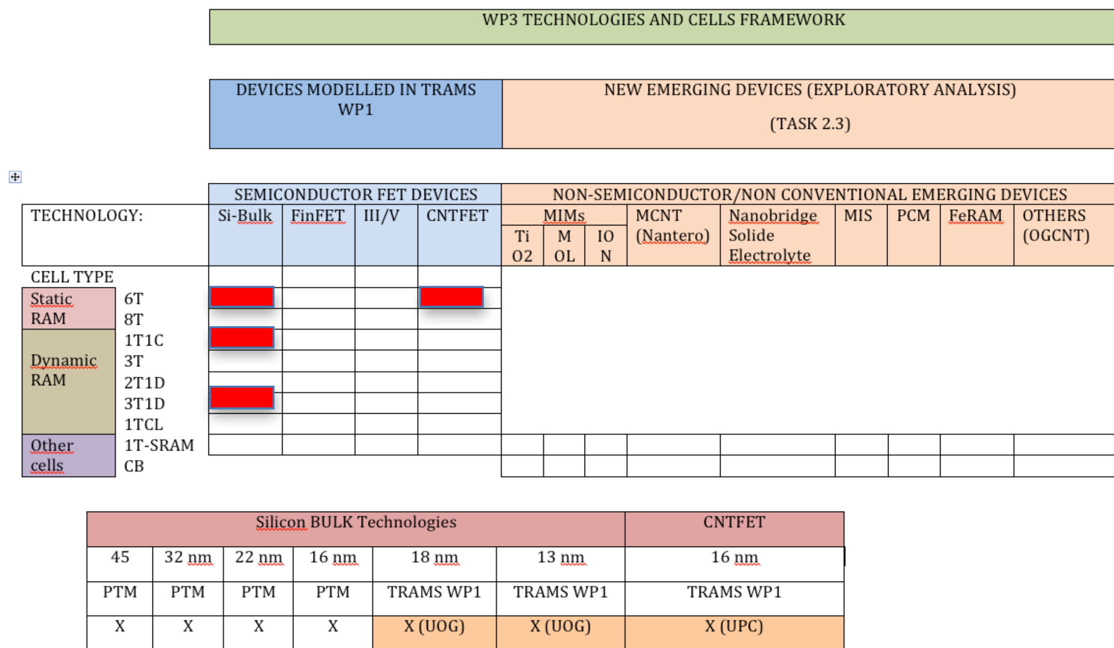

Figure 1. Framework of technologies and memory cells considered in WP3. Red boxes show the technologies and cell considered in this deliverable.

2. Variability scenarios

2.1. Objectives and introduction

The aim of this document is the analysis of the environmental (power supply voltage and temperature) fluctuations, the process variability for different technology nodes including sub-22nm as well as BTI degradation and SEU impact on memory circuits. We will evaluate basic 6T, 1T1C and 3T1D bit cells, and 32KB and 4MB cache memory circuits for 6T and 3T1D and we consider the following Si-bulk CMOS technologies 45, 32, 22, 18, 16, 13 and CNT (equivalent to 16nm node). Device models for 45, 32, 22 and 16 nm are the ones known as Predictive Technology Models (University of Arizona [9]), the models for 18 and 13 nm are results of WP1, and the CNT analysis uses a modification of the models of Stanford (see section 8) with preliminary results about variability from TRAMS WP1..

Section 4 is dedicated to SRAM memories characterized by the 6T memory cell. Section 4.1 analyses the impact of VT and node variations on speed parameters and energy consumption, and in section 4.2 the robustness of the cell in front of process parameter variations is presented.

Section 5 analyses DRAM memories, characterized by 1T1C in section 5.1 and 3T1D in the rest. Section 5.2 analyses the impact of VT and node variations on speed parameters. In section 5.3 the robustness of the 3T1D cell in front of process variation is investigated and in section 5.4 the analysis of the impact of BTI degradation of 3T1D on memory performances and yield is presented. The impact of the process variation on the cache memory performances (both 6T and 3T1D) are analysed in Section 6. In section 7 the impact of SEU on the memories reliability is investigated, and in Section 8 the performances of CNT in comparison with the rest of Si-bulk technologies are presented (for the 6T cell).

2.2. Variability scenarios

The margin of temperature variation considered in this document is, in general, the range 25 ^{o}C to 110 ^{o}C. The margin of V_{DD} variations due to RI and RdI/dt has been considered as a +/-10% of the nominal power supply used in each technology. For process variation we have considered the following different models:

Process variation model used for PTM technologies

For the four Si-bulk CMOS technologies, 45, 32, 22 and 16 nm, covered by PTM we have considered the process variations of the threshold voltage of the devices (V_{th}) and the device geometry (L and W).

For the Vth we have assumed a Gaussian distribution and independent components for random variation (due to random dopants distribution, RDD and line edge roughness, LER) and correlated Gaussian for systematic variations. Geometry variations have been modelled as systematic Gaussian distributions. In all the analysis at system level (cache) both systematic and random variations have been considered and in the case of analysis at cell level, only Vth random variations are contemplated. For each technology we have considered different variation scenarios, standard for 45nm, moderated and high for 32nm and moderated, high and very high for 22 and 16nm. Table 1 shows the standard deviations or second moment of the respective

distributions. The levels of variability assumed in the high and very high variability scenarios are consequent with that observed and deduced for 18 and 13 nm technologies, result of Work Package 1.

Technology	Scenario	total systematic 100 x 1 σ/nominal	random(*)(**) 100 x 1 σ/nominal	Geometry 100 x 1 σ/nominal
		Vth	Vth	L,W
45 nm	standard	2%	4%	2%
32nm	moderated	3%	6%	2%
	high	4%	15%	2%
22nm	moderated	4%	8%	2.5%
	high	4%	15%	2.5%
	very high	5%	30%	2.5%
16nm	moderated	5%	10%	3%
	high	5%	20%	3%
	very high	6%	40%	3%

(*) (random dopants distribution, RDD, and line edge roughness, LER), non correlate (**) for minimum size, for general case correct with /sqrt(WL)

Table 1. Process variation model for the analysis with PTM technologies

Process variation model used for WP1 technologies

Devices models for 18 and 13 nm technologies provided by WP1 present a very high variability on V_{th}, caused by RDD and LER mechanisms. The standard deviations have been obtained from WP1 analysis and are given in Table 2.

Process variation model used for CNT technology

The process variation model for CNTFET technology is part of the work done in WP1 (Task 1.1), an introduction to the variation model used is presented in Section 8.

device	σ Vth	100xσ/nominal
18nm NMOS	66.7mV	33%
18nm PMOS	116mV	58%
13nm NMOS	78.8mV	39%
13nm PMOS	116mV	58%

(*) (random dopants distribution, RDD, and line edge roughness, LER), non correlate (**) for minimum size, for general case correct with /sqrt(WL)

Table 2. Vth process variation model for analysis with 18 and 13 nm CMOS devices (VDD=0.9 volts).

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