Capacitor Voltage Balance Limits in a Multilevel-Converter-Based Energy Storage System

Sendoa Burusteta[1], Josep Pou[2], Salvador Ceballos[1], Iker Marino[1], José Ángel Alzola[1]
[1]TECNALIA RESEARCH & INNOVATION
Parque Tecnológico de Bizkaia, Edif. 700
48160 Derio, Basque Country - Spain
Tel.: +34 / 946430069.
Fax: +34 / 946460900.
E-Mail: sendoa.burusteta@tecnalia.com, salvador.ceballos@tecnalia.com, iker.marino@tecnalia.com, joseangel.alzola@tecnalia.com
URL: http://www.tecnalia.com

[2]TECHNICAL UNIVERSITY OF CATALONIA
Colom, 1
08222 Terrasa, Catalonia - Spain
Tel.: +34 / 937398306.
Fax: +34 / 937398016.
E-Mail: josep.pou@upc.edu
URL: http://www.upc.edu

Acknowledgements

This work has been supported by the Ministerio de Ciencia e Innovación of Spain and the European Regional Development Fund (ERDF) under the project ETF - New Concepts in Energy Storage for Medium and Large Scale - PID-590000-2009-4. This work has also been developed under the EOLO project in the CTP frame with support of the Departamento de Educación, Universidades e Investigación, Dirección de Política Científica Proyectos de Investigación of the Basque Country, and the Comissionat per a Universitats i Recerca del Departament d'Innovació, Universitats i Empresa of the Generalitat de Catalunya.

Keywords

«Energy storage», « Renewable energy systems», «Multilevel converters», « Modulation strategy», «Converter control»

Abstract

This paper studies an energy storage system based on a three-level DC-DC converter and a grid-connected neutral-point-clamped inverter. The main advantages of this multilevel power conversion system are highlighted and the neutral-point voltage oscillations are analyzed. A modulation algorithm for the DC-DC converter which includes the neutral-point voltage balance control is used to improve the voltage balancing capabilities of the inverter. Some figures are presented to show the extended operating areas without neutral-point voltage oscillations thanks to the contribution of the DC-DC converter to the voltage balance. Finally, some guidelines to size the DC-link capacitors are given for a practical application.

Introduction

The negative environmental effects of the current energy model based on fossil fuels, the upward trend in energy demand, and the progressive depletion of the fuel reserves force to move towards an energy model based on clean and renewable energy sources. Nevertheless, the imbalance between renewable

generation and power demand, as well as the variability and the difficulty to predict them, hinder their integration into the electrical grid. Current advances in storage technologies make energy storage systems (ESSs) interesting options to improve grid integration of renewable energies. Furthermore, ESSs can provide many other beneficial services like grid voltage and frequency stabilization, peak shaving, power quality, transmission and distribution upgrade deferral, arbitrage or backup and black start capacity. Energy storage technologies that are suitable for the electrical grid can be classified into mechanical, thermal, electromagnetic, and electrochemical systems. The last ones have aroused great interest for the grid connection. The main electrochemical options are lead-acid, sodium-sulfur, lithium-ion, and flow batteries. Each of them has some particular characteristics related with power and energy density, lifetime, cost and efficiency; but a common feature is that all of them provide a DC voltage that varies with the state of charge (SOC).

Grid-connected ESSs applications with a wide DC operating voltage range require of power conversion systems (PCSs), made up of DC-DC and DC-AC bidirectional converters, as an interface between the energy storage devices and the grid. It is also possible to connect directly the batteries to the DC-AC converter without the use of a DC-DC converter, avoiding losses associated with this converter. There are two alternatives to perform this direct connection. The first alternative consists on increasing the voltage level of the energy store device to reach the minimum DC-link voltage required for grid-connection of the inverter. The ESS should be able to exchange energy with the grid until the electrochemical system is discharged to its minimum voltage. This issue could force to oversize the batteries increasing the overall cost of the system. Furthermore, the inverter power devices have to be sized to withstand the maximum voltage provided by the electrochemical system when it is fully charged, and the battery management complexity increases due to the higher number of storage modules connected in series. The second alternative entails the use of a transformer to step-up the inverter AC voltages to reach the necessary levels for grid connection. This allows to keep lower voltage levels at the DC side of the inverter and hence requiring less energy storage modules connected in series. Some drawbacks are that the low-frequency transformer is a heavy and bulky element. Besides, although the DC-link voltage level can be lower, it would still change within a wide range. In addition, the switching devices of the inverter have to withstand high current levels.

On the other hand, the use of a DC-DC converter in the topology has the advantage of stepping-up the DC-link voltage and feeding the inverter with a constant DC-link, independently of the SOC of the electrochemical device. This fact softens the inverter power devices requirements. In addition, having a standard PCS with a DC-DC converter able to work with different energy storage voltages, improves flexibility of the system for different applications, and helps to reduce costs due to enabling mass production.

Minimizing the conversion losses in the charging and discharging processes of the ESS is a key factor. Besides, another aspect to bear in mind is the high size and weight of the filters in both sides of the PCS. Multilevel converter topologies are a good solution to improve these issues in medium and high voltage applications, compared with traditional two-level (2L) converters. There are three main multilevel topologies; the diode-clamped, the floating-capacitor, and the cascaded H-bridge converters [1]–[3]. Among them, the three-level (3L) diode-clamped converter, also known as neutral-point-clamped (NPC) converter, is perhaps the most used nowadays. Since the introduction of the DC-AC NPC converter in 1981[4], it has been widely investigated [5]–[8]. One important drawback in this topology is that a low-frequency voltage oscillation may appear in the neutral-point (NP) for some operating conditions, especially when operating with high modulation indices and low power factors. Because of such NP voltage oscillation, the DC-link capacitors and the power semiconductors of the converters have to withstand higher voltages, and additionally, the grid voltages generated include low-frequency harmonics [5]. Thus, it is interesting to determine the operating conditions in which the converter does not produce NP voltage imbalances. The connection of a 3L DC-DC converter with an NPC DC-AC converter can contribute to improve the operation area.

Bidirectional Multilevel DC-DC/DC-AC Connection in ESS

Fig. 1 shows the PCS with the selected multilevel-based structure. Since both converters make use of the NP connection, the voltage balance can be handled globally considering the whole system.

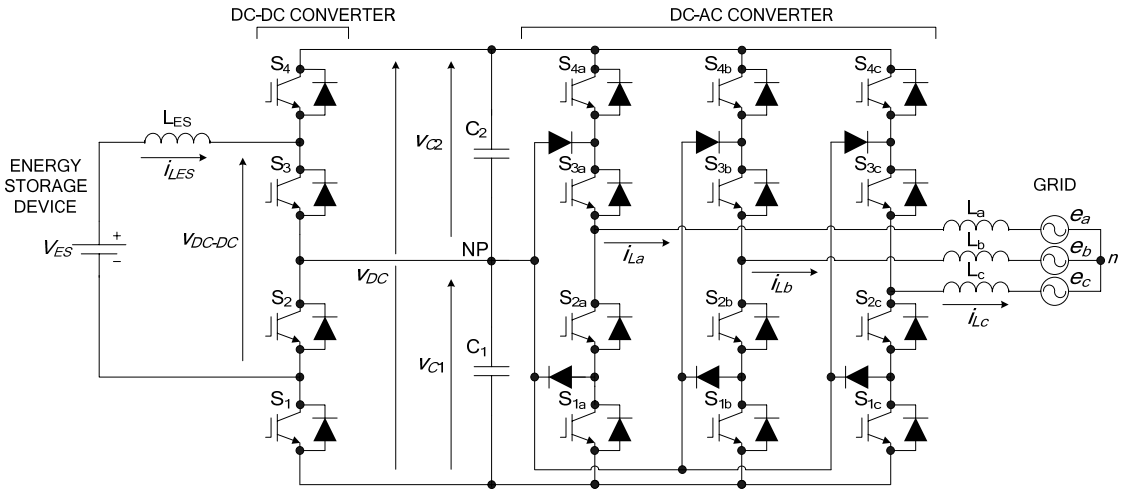

Fig. 1: 3L DC-DC and NPC DC-AC Converter

This section is focused on the bidirectional 3L DC-DC converter derived from one leg of an NPC inverter [9], [10], which has similar advantages to those of its DC-AC counterpart. Compared with a conventional 2L DC-DC converter, the studied 3L topology has more switches but they are rated at half of the DC-link voltage. Due to the 3L waveform generated, smaller reactive components are required. Some consequences are that the efficiency of the system increases and its overall size decreases, together with the capability of handling higher voltages. This bidirectional DC-DC converter has two operation modes, boost mode for ESS charging process and buck mode for discharging process. The main features of the commutation states are shown in Table 1, where the variables s_i are the control functions of the DC-DC converter switches S_i, being $i = \{1,2,3,4\}$. When the control function s_i take the unity value, the switch S_i is activated; otherwise it is deactivated ($s_i = \{0,1\}$).

Table I: Commutation states in boost (discharge) and buck (charge) mode

Commutation States	$v_{DC\text{-}DC}$	NP Voltage ($v_{NP} = v_{C1}$)	
		BOOST ($i_{LES} > 0$)	BUCK ($i_{LES} < 0$)
$s_1 = 1$ & $s_3 = 1$	v_{C1}	$\uparrow v_{NP}$	$\downarrow v_{NP}$
$s_1 = 1$ & $s_4 = 1$	$v_{C1} + v_{C2}$	-	-
$s_2 = 1$ & $s_3 = 1$	0	-	-
$s_2 = 1$ & $s_4 = 1$	v_{C2}	$\downarrow v_{NP}$	$\uparrow v_{NP}$

In both operation modes, there are two commutation states that produce approximately the same voltage (provided that $v_{C1} \approx v_{C2} \approx v_{DC}/2$), but one increases the NP voltage while the other one decreases it. Selection of a proper redundant state for NP voltage balance is studied in the next section.

In addition, for the same maximum current ripple and number of switching events, the value of the filter inductance used in this DC-DC converter can be half of that in a conventional one. On the other hand, it is possible to increase the number of switching events to double (so that the average switching frequency of each power devices would be the same than in a 2L DC-DC converter), and reduce the value of the inductance by a quarter [11], [12]. In both cases, the efficiency is increased and the size of the converter decreased. To illustrate this issue, Fig. 2 represents the peak-to-peak current ripple through the inductor at the energy-storage-side Δi_{LES}. The current ripple has been normalized by the

maximum ripple produced in the 2L DC-DC converter. The normalized current ripple is represented as a function of the modulation index of the DC-DC converter $m_{DC} \in [0,1]$. In steady state and assuming a negligible inductance resistor this modulation index becomes:

$$m_{DC} = \frac{V_{ES}}{V_{DC}} \tag{1}$$

The current ripple produced in a conventional 2L DC-DC converter and in a 3L converter with the same and double switching events is shown in this figure.

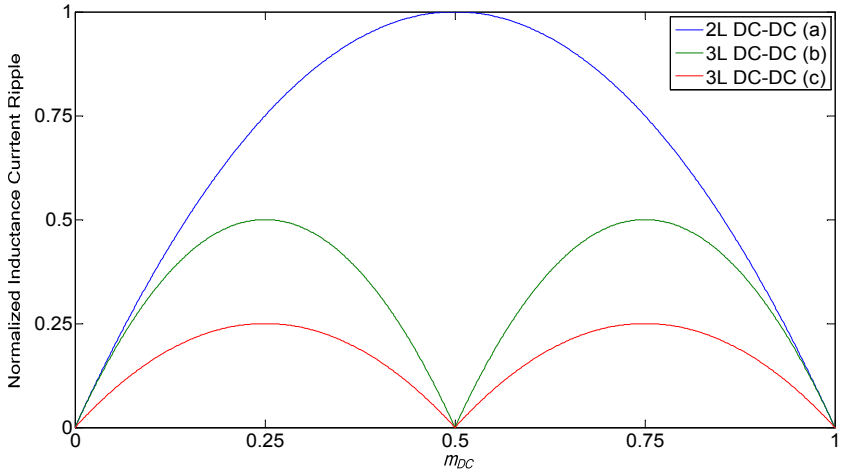

Fig. 2: Normalized inductance current ripple in (a) a 2L DC-DC converter and in a 3L one with (b) the same, and (c) double switching events

The maximum value allowed of the inductance current ripple $\Delta i_{LES,max}$ determines the size of the filter. Hence, it can be observed the filter reduction in a 3L DC-DC converter compared with a 2L DC-DC converter. Table 2 shows the reduction of the value of the energy-storage-side inductance for the studied cases.

Table II: Equations of inductance current ripple and reduction of inductance

DC-DC Converter	Peak-to-Peak Current Ripple Through the Inductor, Δi_{LES}	$\Delta i_{LES,max}$	Reduction of Inductance
2L (a)	$\frac{V_{ES}}{Lf_s}\left(1-\frac{V_{ES}}{V_{DC}}\right)$	$\frac{V_{DC}}{4Lf_s}$	1
3L (b)	$\frac{V_{ES}}{Lf_s}\left(1-2\frac{V_{ES}}{V_{DC}}\right)_{m_{DC}<0.5}$ $\frac{V_{ES}-V_{DC}}{Lf_s}\left(1-2\frac{V_{ES}}{V_{DC}}\right)_{m_{DC}>0.5}$	$\frac{V_{DC}}{8Lf_s}$	$\frac{1}{2}$
3L (c)	$\frac{V_{ES}}{L2f_s}\left(1-2\frac{V_{ES}}{V_{DC}}\right)_{m_{DC}<0.5}$ $\frac{V_{ES}-V_{DC}}{L2f_s}\left(1-2\frac{V_{ES}}{V_{DC}}\right)_{m_{DC}>0.5}$	$\frac{V_{DC}}{16Lf_s}$	$\frac{1}{4}$

NP Voltage Balance Control

The control of NP voltage is carried out by the modulation strategies. The nearest-three-vector (NTV) space-vector modulation (SVM) is applied to the DC-AC NPC converter [5]. The AC reference voltage vector $\vec{V}_{REF}$ should be generated by the three nearest vectors of the space-vector diagram, as shows Fig.3. In this diagram, the numbers associated with each vectors represent the commutation

state of the inverter for phase a, b and c respectively; 0 indicates that the corresponding phase is connected to the bottom of the DC-link, 1 to the NP and a 2 to the top.

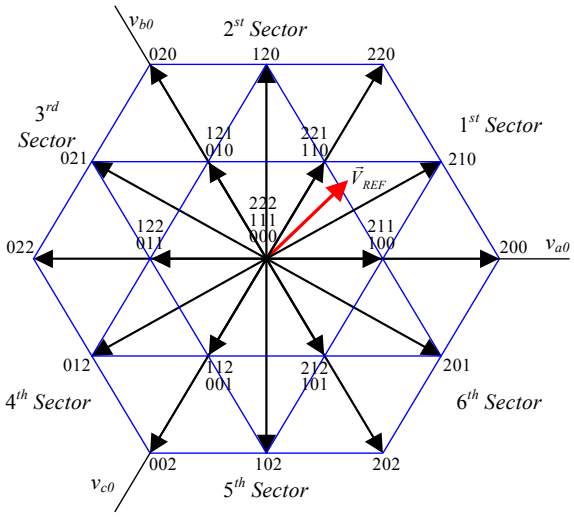

Fig. 3: Space-vector diagram of the NPC converter

Four sets of vectors can be seen in the diagram; the large vectors (200, 220, 020, 022, 002, and 202), the medium vectors (210, 120, 021, 012, 102, and 201), the short or redundant vectors (100-211, 110-221, 010-121, 011-122, 001-112, and 101-212), and the zero vectors (000, 111, and 222). Unlike the zero and large vectors, the medium vectors produce voltage imbalances on the capacitors caused by the connection of one phase to the NP. Proper selection of the short vectors can contribute to compensate for such imbalances. In the NTV modulation strategy, only one vector from each pair of redundant short vectors is used at each commutation period. The selection of this vector is made in order to balance the DC-link capacitor voltages, and it depends on the instantaneous voltage imbalance and the direction of the grid currents. Despite the NP voltage balancing control provided by the short vectors, some low-frequency NP voltage oscillations may appear for some operating points of the converter [5].

A similar voltage balance approach is used in the modulation strategy of the DC-DC converter. According to Table 2, this converter offers two redundant states to provide the voltage level $v_{DC}/2$ to the energy storage device. The difference between them is that one increases the value of NP voltage v_{NP}, while the other decreases it; therefore, when this voltage level is required, the optimal state is selected at each commutation period to help for NP voltage balance. A carrier-based modulation strategy is used in this converter. In this case, the DC reference voltage is compared with two triangular carriers as shown in Fig. 4, with the resulting energy storage device current. The selection of the redundant commutation state is based on v_{NP} and the direction of the energy storage device current i_{LES}, as it is shown in Table 3. It is only necessary to know the value of the third column ($\Delta v_{NP} \cdot i_{LES}$) for the selection of the optimal redundant state, obtained by means of multiplication of both variables. Using this modulation strategy, the DC-DC converter contributes actively to the control of the NP voltage and improves the voltage balance capabilities of the NPC converter.

Operation Area with Voltage Balancing Control

The complete multilevel grid-connected ESS presented in Fig.1 is considered for the NP voltage balance analysis performed in this section. The 3L DC-DC converter can contribute to compensate for the imbalances produced by the NPC DC-AC converter, since both of them share the same NP. Fig. 5 shows the limiting areas in which voltage balance can be achieved for different modulation indexes of the multilevel DC-DC converter m_{DC} and constant inverter output current amplitude. Different DC-AC converter modulation indexes m_{AC} and relative phase of the AC currents are represented. The area below the corresponding limiting line shows working conditions in which there are no NP voltage

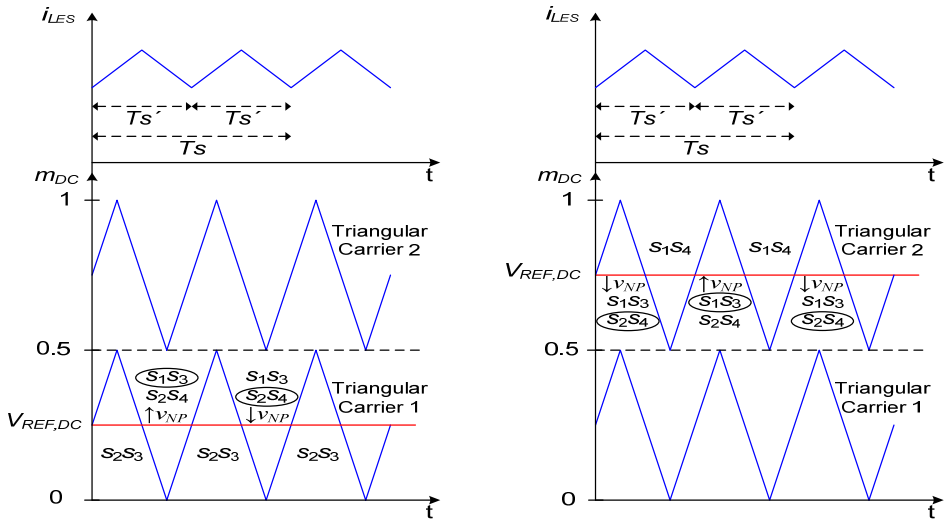

Fig. 4: PWM modulation for NP voltage balance when (a) $m_{DC} < 0.5$ and (b) $m_{DC} > 0.5$

Table III: Selection of redundant commutation states in PWM modulation

$\Delta v_{NP} = (v_{NP} - v_{DC} / 2) > 0$	$i_{LES} > 0$	$\Delta v_{NP} \cdot i_{LES} > 0$	Selection of Redundant Commutation States
0	0	1	$s_2 = 1$ & $s_4 = 1$
0	1	0	$s_1 = 1$ & $s_3 = 1$
1	0	0	$s_1 = 1$ & $s_3 = 1$
1	1	1	$s_2 = 1$ & $s_4 = 1$

oscillations. Above these limiting boundaries, the DC-DC converter cannot fully compensate for voltage imbalance and some NP voltage oscillations with a frequency three times higher than that of the AC voltages appear. When the m_{DC} is equal to 1 or 0, the DC-DC converter does not provide any current to the NP, being these situations the worst cases for the voltage balancing point of view. On the other hand, when the modulation index m_{DC} becomes closer to 0.5 the capability of the system to preserve voltage balance increases. At $m_{DC} = 0.5$, the output of the DC-DC converter is connected continuously to the NP; therefore, the balancing current provided to the NP is the maximum.

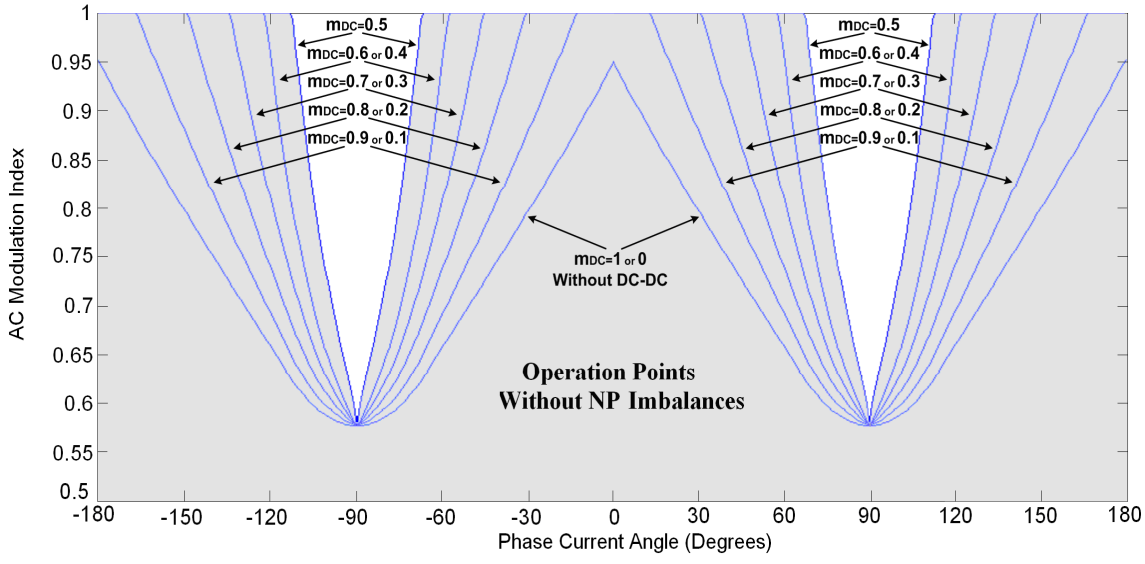

Fig. 5: Limits of NP current control

To verify the information given in Fig. 5 some simulations have been carried out. Fig. 6 shows the DC-link capacitor voltages for some operating conditions of the system. For this example, the DC-link voltage is V_{DC} = 700 V being the capacitors C = 1000 µF. The value of the grid side current is I_{RMS} = 100 A, the grid frequency f = 50 Hz, the modulation index m_{AC} = 1, and the relative phase current angle φ = –60º.

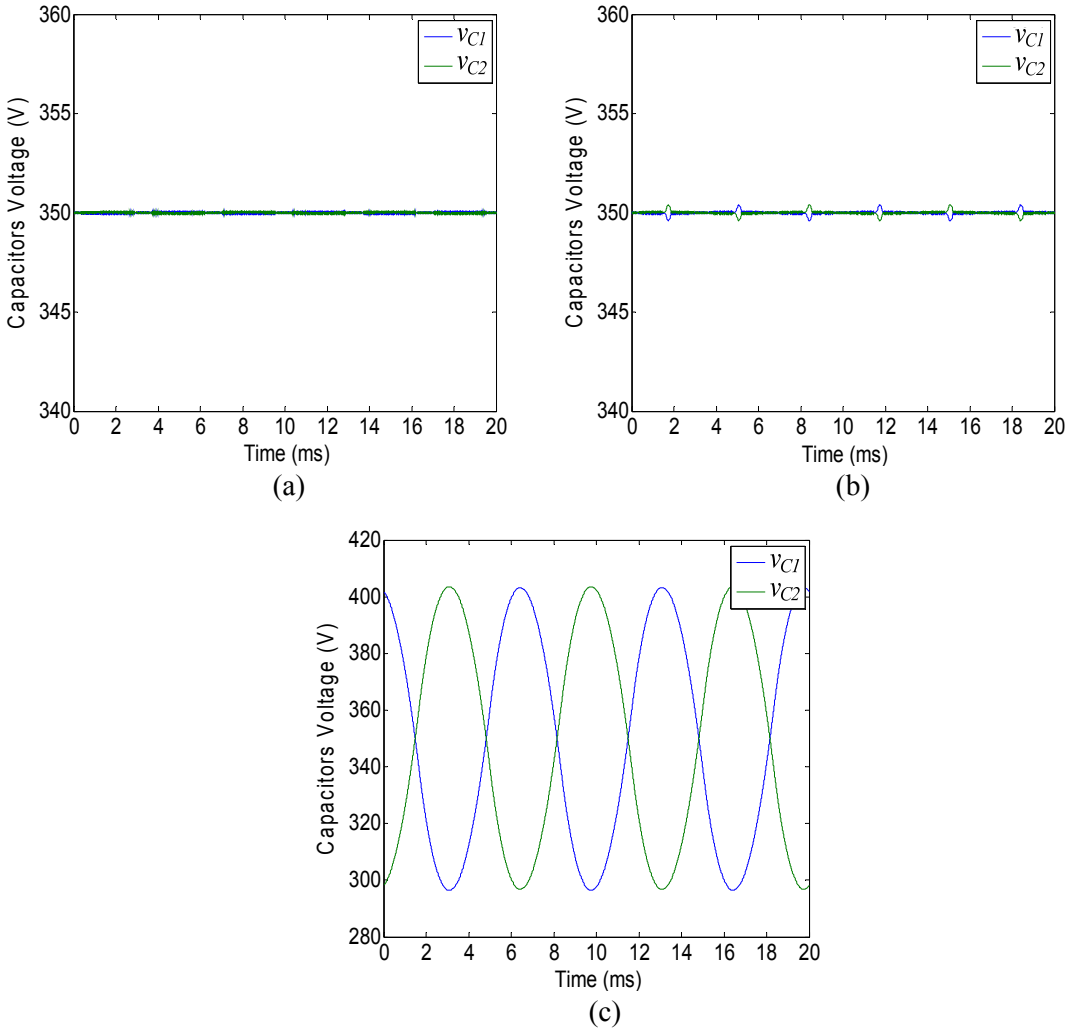

Fig. 6: DC-link capacitors voltage for the case I_{RMS} = 100 A, f = 50 Hz, m_{AC} = 1 and φ = –60º with: (a) m_{DC} = 0.5, (b) m_{DC} = 0.6 including a 3L DC-DC converter in the topology, and (c) m_{DC} = 0.6 without a 3L DC-DC converter

Fig. 6(a) is obtained for a particular operating point where voltage balance can be achieved. There is no low-frequency voltage oscillation, since this operation point belongs to the area below the curve m_{DC} = 0.5 in Fig. 5. In contrast, in Fig. 6(b), a tiny low-frequency voltage oscillation appears, because this operating point is above the area of curve given by m_{DC} = 0.6. Finally, Fig. 6(c) shows the same operating conditions but without any voltage balancing contribution from the multilevel DC-DC converter. In this case, the amplitudes of the low-frequency voltage oscillations are much higher. This implies that the voltage stress of the semiconductors and the DC-link capacitors is increased. Additionally, the grid voltages generated by the converters become significantly distorted.

In order to provide information for determining the value of the DC-link capacitors for the worst case m_{DC} = 1, (m_{DC} = 0 is not a practical situation), the normalized amplitude of the low-frequency NP voltage oscillations (ΔV_{NPn} / 2) defined as

$$\frac{\Delta V_{NPn}}{2} = \frac{\frac{\Delta V_{NP}}{2}}{\frac{I_{RMS}}{fC}} \tag{2}$$

is presented in Fig. 9, where ΔV_{NP} is the peak-to-peak value of the NP voltage oscillations. In this representation, the rms value of the AC output currents is kept constant.

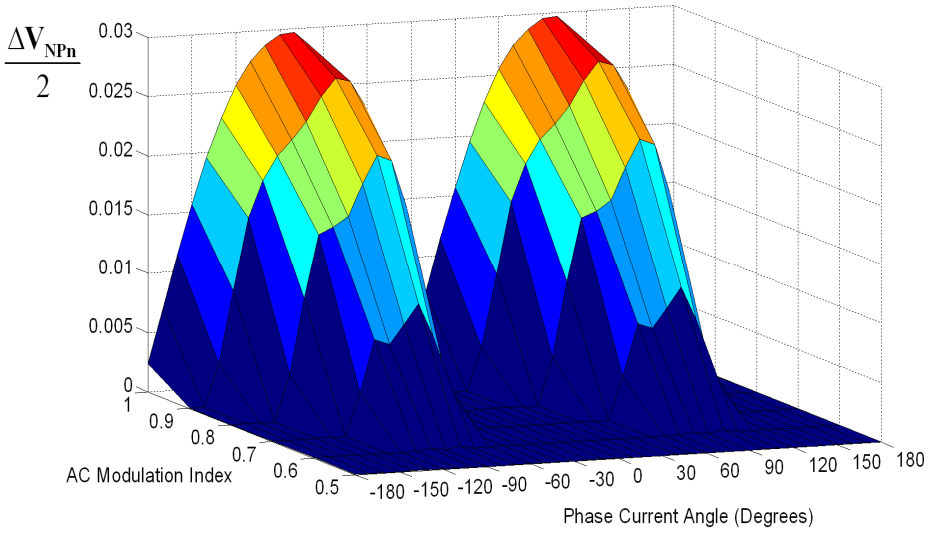

Fig. 7: Normalized NP voltage ripple in worst case

The maximum value is achieved when the phase current angle is $\varphi = -84º$ or $\varphi = +96º$, reaching a value of normalized NP ripple of 0.0297. For example, in the case that the maximum NP voltage amplitude allowed were 50 V, the grid frequency f =50 Hz and the output current I_{RMS} = 100 A, the value of the DC-link capacitor can be obtained by means of (2), as shown in (3).

$$C = \frac{\Delta V_{NPn}}{\Delta V_{NP}} \frac{I_{RMS}}{f} = \frac{0.0297}{50} \frac{100}{50} = 1188 \ \ \mu F \tag{3}$$

Conclusion

Multilevel converters are selected for a grid-connected ESS application. Some advantages of this multilevel-based configuration over the classical one based on 2L converters are that the overall system efficiency is improved, and both, the value of the inductances and the switching frequency of the power devices, can be reduced. The drawback of the voltage imbalances produced in the DC-link capacitors by the NPC converter are notably improved with the use of a 3L DC-DC converter which shares the same NP connection. Hence, the operating area without low-frequency voltage oscillations is extended, and it is presented for the first time in this paper. Furthermore, some guidelines to size the DC-link capacitors are given. In conclusion, the proposed multilevel-based ESS topology offers many advantages, and the NP voltage imbalances produced by the NPC converter are no longer a problem thanks to the use of the 3L DC-DC converter. Thus, this may be a practical solution for the future ESSs.

References

[1] J. Rodríguez, J.-S. Lai and F. Z. Peng: Multilevel inverters: a survey of topologies, control, and applications, IEEE Trans. Ind. Electron., Vol. 49, no. 4, pp. 734-738, Aug. 2002.

[2] L. G. Franquelo, J. Rodríguez, J. I. Leon, S. Kouro, R. Portillo, and M. A. M. Prats: The age of multilevel converters arrives, IEEE Ind. Electron. Mag., Vol. 2, no.2, pp. 28-39, Jun. 2008.

[3] S. Kouro, M. Malinowski, K. Gopakumar, J.Pou, L. G. Franquelo, B. Wu, J. Rodríguez, M. A. Pérez, and J. I. Leon: Recent advances and industrial applications of multilevel converters, IEEE Trans. Ind. Electron., Vol. 57, no. 8, pp. 2553-2580, Aug. 2010.

[4] A. Nabae, I. Takahashi, and H. Akagi: A new neutral-point-clamped PWM inverter, IEEE Trans. Ind. Appl., Vol. IA-17, no. 5, pp. 518-523, Sep./Oct. 1981.

[5] J. Pou, R. Pindado, D. Boroyevich, and P. Rodríguez: Evaluation of the low-frequency neutral-point voltage oscillations in the three-level inverter, IEEE Trans. Ind. Electron., Vol. 52, no. 6, pp. 1582-1588, Dec. 2005.

[6] A. Calle, J. Rocabert, S. Busquets-Monge, J. Bordonau, S. Alepuz and J. Peracaula: Three-level three-phase neutral-point-clamped back-to-back converter applied to a wind emulator, in Proc. EPE´09, Barcelona, Spain. Sep. 2009.

[7] J. Rodríguez, S. Bernet, P. K. Steimer, and I. E. Lizarra: A survey on neutral-point-clamped inverters, IEEE Trans. Ind. Electron., Vol. 57, no. 7, pp. 2219-2230, Jul. 2010

[8] S. Ceballos, J. Pou, J. Zaragoza, E. Robles, J. L. Villate, and J. L. Martín: Fault-tolerant neutral-point clamped converter solutions based in including a fourth resonant leg, IEEE Trans. Ind. Electron., Vol. 58, no. 6, pp. 2293-2303, Jun. 2011

[9] X. Ruan, B. Li, Q. Chen, S.-C. Tan, and C. K. Tse: Fundamental considerations of three-level DC-DC converters: topologies, analyses and control, IEEE Trans. Circuits and Systems I, Vol. 55, no. 11, pp. 3733-3743, Dec. 2008.

[10] H. Wu and X. He: Single phase three-level power factor correction circuit with passive lossless snubber, IEEE Trans. Power Electron., Vol.17, no. 6, pp. 946-953, Nov. 2002.

[11] M. T. Zhang, Y. Jiang, F. C. Lee, and M. M. Jovanovic: Single-phase three-level boost power factor correction converter, in Proc. IEEE APEC'95, Dallas, USA, pp. 434–439 Mar. 1995.

[12] P. J. Grbović, P. Delarue, P. L. Moigne, and P. Bartholomeus: A bidirectional three-level DC-DC converter for the ultracapacitor applications, IEEE Trans. Ind. Electron., Vol. 57, no. 10, pp. 3415-3430, Sep. 2010.