IEICE TRANS. ELECTRON., VOL.E94–C, NO.12 DECEMBER 2011

BRIEF PAPER

A New Approach to Modeling the Impact of EMI on MOSFET DC Behavior

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SUMMARY A simple analytical model to predict the DC MOSFET behavior under electromagnetic interference (EMI) is presented. The model is able to describe the MOSFET performance in the linear and saturation regions under EMI disturbance applied to the gate. The model consists of a unique simple equivalent circuit based on a voltage dependent current source and a reduced number of parameters which can accurately predict the drift on the drain current due to the EMI source. The analytical approach has been validated by means of electric simulation and measurements and can be easily introduced in circuit simulators. The proposed modeling technique combined with the nth-power law model of the MOSFET without EMI, significantly improves its accuracy in comparison with the *n*-th power law directly applied to a MOSFET under EMI impact.

key words: *MOSFET, electromagnetic compatibility (EMC), electrical modelling, direct power injection*

1. Introduction

Electronic systems are disturbed by electromagnetic interference (EMI) which can potentially disrupt their operation. In fact, the impact of EMI in analog circuits has been deeply investigated and it has been observed that EMI provoke a voltage offset shift due to non-linear MOSFET behavior [1]. This fact has been taken into account in the design of electronic devices based on MOSFET transistors [2], [3]. In this context, the modeling and prediction of interference effects play an outstanding role in the electromagnetic compatibility (EMC) field. Likewise, accurate models of MOSFET are required in order to design and implement modern electronic circuits. From the previous reported works, the *n*-th power law model has been revealed as one of the most successful DC MOSFET modeling techniques in the linear and saturation regions [4], [5]. Unfortunately, this modeling technique directly applied to MOSFET subjected to EMI impact, decreases its degree of accuracy in comparison with the free EMI case. In this paper, a new MOSFET model based on a combination of the *n*-th power law model together with a voltage gate and voltage EMI dependent current source is proposed in order to accurately describe the transistor behavior under EMI impact.

Manuscript received April 5, 2011.
Manuscript revised July 20, 2011.

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DOI: 10.1587/transele.E94.C.1906

2. Experimental

In order to measure the impact of the EMI on the DC behavior of the MOSFET, the direct power injection (DPI) method has been applied [6]. Specifically, nMOSFET samples with aspect ratio of 10 μm/0.38 μm fabricated in 3.3 V CMOS 90-nm Freescale Semiconductor process have been evaluated. The developed test is based on the experimental setup described in Fig. 1. An interference signal with an amplitude and frequency sweep ranges of V_{EMI}=0 V (free EMI disturbance)-1.2 V and f=1–100 MHz is generated by means of a signal generator and coupled to the

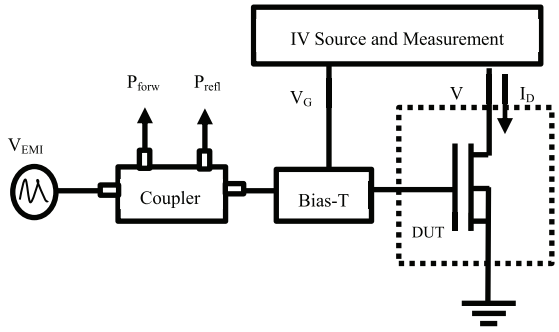

Fig. 1 Experimental setup.

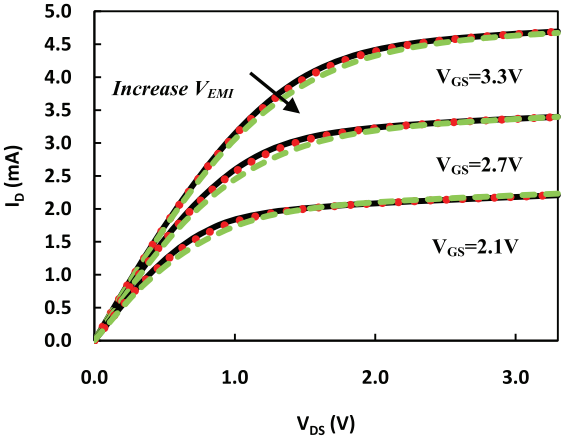

Fig. 2 Experimental I_D-V_{DS} characteristics under EMI conditions. Continuous lines correspond to MOSFET without EMI and dot and dashed lines correspond to I_D-V_{DS} under EMI of 0.6 V and 1.2 V, respectively. Curves for V_{GS} = 3.3 V, 2.7 V and 2.1 V are shown.

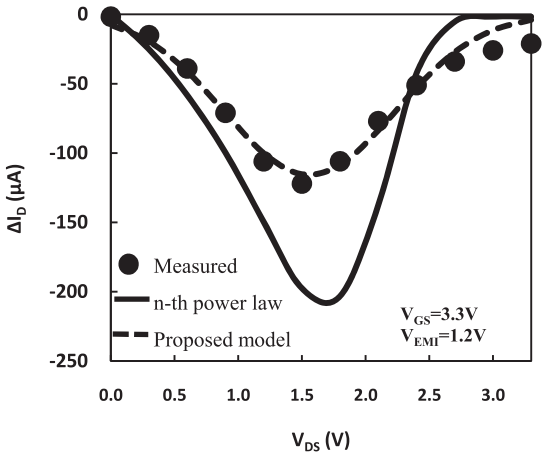

Fig. 3 Drain current shift due to EMI.

Table 1 *n*-th power law parameters without EMI.

V_{th}	m	n	K	B	λ_0
1.134	0.678	0.995	1.267	$73.48 \cdot 10^{-6}$	0.038

transistors' gate through a bias-T block. By using a double current-voltage source and measurement instruments (Keithley 2636A), the DC gate and drain voltage have been generated and the drain current, (ID) has been measured. Figure 2 illustrates the experimental I_D-V_{DS} behavior with and without interference. Curves for V_{GS}=3.3 V, 2.7 V and 2.1 V are depicted at V_{EMI}=0 V, 0.6 V and 1.2 V (f=10 MHz). Free EMI disturbance corresponds to the continuous line, 0.6 V to the dotted line and 1.2 V to the dashed line. In all the interference cases, a drain current degradation is observed. This degradation is shown by decreasing the I_D with regard to the free EMI case. The degree of degradation increases with the amplitude interference level and it is mainly observed in the transition between linear and saturation region.

3. Proposed Model

In order to estimate the absolute value of the impact of the interference disturbance, the drain current shift between free-EMI and disturbed samples corresponding to V_{GS}=3.3 V shown in Fig. 2 has been calculated and plotted in Fig. 3 (for case: V_{EMI}= 1.2 V). As expected, the difference is higher at the transition between linear and saturation regions. With the aim to evaluate this current drain shift with a circuit simulator, the drain current has been fitted with the *n*-th power law MOSFET model according to Algorithm 1. The extracted *n*-th power law parameters in the devices under test without EMI are summarized in Table 1.

It is important to remark that the model fits the experimental data with an error lower than 0.5%. The model has been included in a circuit simulation reproducing the experimental setup (i.e., by taking into account a sinusoidal EMI source). The comparison between measurements (dot symbols, Fig. 3) and *n*-th power law model simulation (continuous line, Fig. 3) under EMI conditions reveals a significant variation.

$V_{DSAT} = K \cdot (V_{GS} - V_{th})^m$

If $V_{GS} < V_{th}$

$I_D = 0$

elseif $V_{DS} < V_{DSAT}$

$I_D = B \cdot (V_{GS} - V_{th})^n \cdot (1 + \lambda_0 \cdot V_{DS}) \cdot \left(2 - \frac{V_{DS}}{V_{DSAT}}\right) \cdot \frac{V_{DS}}{V_{DSAT}}$

else

$I_D = B \cdot (V_{GS} - V_{th})^n \cdot (1 + \lambda_0 \cdot V_{DS})$

end if

Algorithm 1 *n*-th power law drain current model.

Table 2 Fitting constants of expression (1) using the data of Fig. 3.

C_1	C_2	C_3
80.41	1.12	0.47

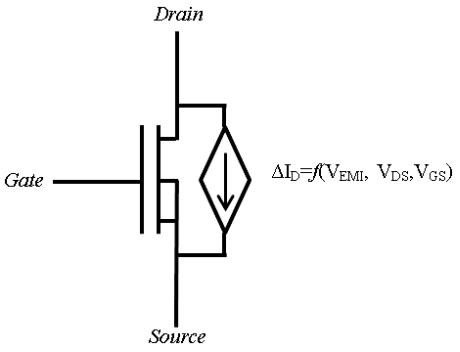

Fig. 4 Proposed MOSFET model under EMI conditions.

Although the *n*-th power law model can accurately reproduce the DC MOSFET behavior, it overestimates the drain current shift roughly by a factor of two with regard to the experimental data. In fact, this variation roughly corresponds to a 3%, with respect to the actual current, which is clearly higher than the intrinsic error of the *n*-th MOSFET model (0.5%). Therefore, some additional corrections describing this shift effect are required. A parametric analysis of the experimental data in Fig. 3 has been performed in terms of several MOSFET variables. The study reveals that the drain current shift produced by interference signals, ΔI_D, depends on V_{EMI}, V_{DS} and V_{GS} according to Eq. (1),

$$\Delta I_D = -C_1 \cdot V_{EMI}^2 \cdot e^{-C_2(V_{DS} - C_3 \cdot V_{GS})^2} \quad (1)$$

where C_1, C_2 and C_3 are fitting constants, which are summarized in Table 2. According to this analytical method, the proposed circuit describing the DC behavior of MOSFET samples under EMI impact is based on the *n*-th power law model together with an extra voltage dependent current

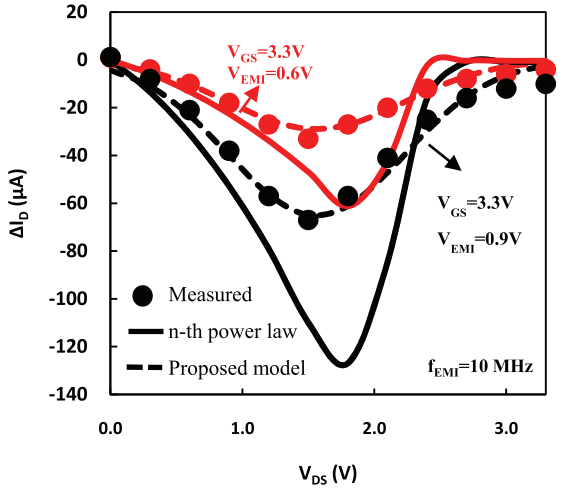

Fig. 5 Validation of the proposed model under different EMI amplitude.

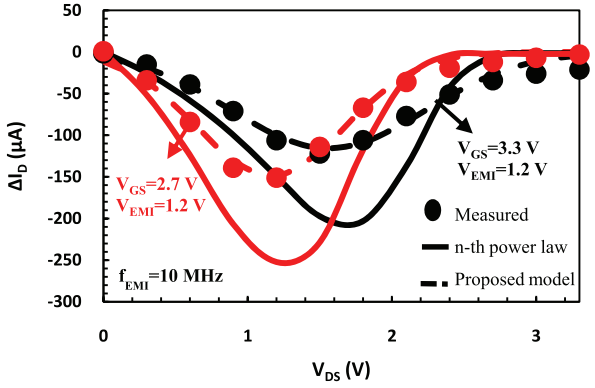

Fig. 6 Validation of the proposed model under different V_{GS} conditions.

source, $\Delta I_D = f(V_{EMI}, V_{DS}, V_{GS})$, in parallel between drain and source nodes, as shown in Fig. 4.

4. Results

In order to validate the proposed model, the simulation results under different EMI conditions and V_{GS} values are compared with experimental data. Similar behavior under different interference signal frequency it has been observed, as expected theoretically. Figure 5 and Fig. 6 depicted the validation results of the proposed model under differences interference amplitude and V_{GS} values, respectively. As can be observed, the model accurately reproduces the current drain shift by combining the n-th power law parameter extraction without interference conditions with the proposed ΔI_D source.

5. Conclusions

In summary, a simple analytical circuit model to predict the DC MOSFET behavior under EMI has been proposed. The model consists of a V_{EMI}, V_{DS} and V_{GS} dependent current source and a reduced number of constants. Simulated and experimental results reveal a good accuracy in the prediction of the drift on the drain current due to the EMI source located at the transistor's gate. The proposed modeling technique combined with the n-th power law model of the MOSFET without EMI disturbance, significantly improves its accuracy in comparison with the nth-power law directly applied to a MOSFET under EMI impact. Therefore, it can be easily included in circuit simulators.

Acknowledgments

This work has been supported by the Spain-MICINN under Project TEC2010-18550 and AGAUR 2009 SGR 1425.

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