Maximum IR-Drop in On-Chip Power Distribution Networks of Wire-Bonded Integrated Circuits

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***Abstract*— A compact IR-drop model for on-chip power distribution networks in wire-bonded ICs is presented. Chip dimensions, metal coverage and piecewise distribution of the IC consumption are taken into account to obtain closed form expressions for the maximum IR-drop as well as its place. Comparison with simulations shows an error as small as 2% in most the cases.**

I. INTRODUCTION

The design of a good and reliable on-chip power distribution network (PDN) of digital ICs is a very complex task because designers cannot anticipate all the details of the design. Power supply noise (PSN) depends on the place, size and activity of the different blocks configuring the circuit. So, to check that PSN is below the specified value it is necessary to simulate the complete circuit, which is clearly unfeasible in large ICs. The help of specific CAD tools alleviates this problem but, due to the simulation time, they are primarily intended for use in post-layout verification after the design is complete. Thus, a failure in the design involves a costly rework of the PDN. This promotes over-dimensioning, resulting in the sacrifice of valuable routing resources. For these reasons the use of pre-layout tools, which give approximate results for the expected PSN in the early stages of PDN design, becomes a necessity [1][5][7-9].

Static power supply noise (IR-drop), is due to the drop voltage produced in the PDN resistances caused by the supply current, whereas dynamic PSN results from the current transients exciting the distributed inductances and capacitances of the PDN. Despite being partial, the knowledge of the IR-drop is very important in PDN design for a number of reasons, e.g., its impact on the circuit performance [6] and the electromigration issues.

The purpose of this paper is to analyze the IR-drop in the PDN of wire-bonded ICs. Our results extend the ones presented in [1] and [7], which analyze only the case of constant current in the whole IC, by considering realistic cases for the distribution of the IC consumption. In our model, the PDN is approximated as a continuous layer of conductive material and the IR-drop at any point is found by solving a partial differential equation, i.e. the Poisson equation, with the proper boundary conditions and source function. From this starting point, the paper gives compact expressions for the position and value of the maximum IR-drop. The analysis is tested for different combinations of the PDN parameters such as chip dimensions, metal coverage, sheet resistances, and current distribution, all of which are representative of real ICs, and the results are compared with simulations.

II. PROBLEM FORMULATION

A typical on-chip PDN is a mesh of perpendicular wires strongly connected in the crossing points. As sketched in Figure 1, horizontal wires may be made with the upper metal layer available, and the vertical ones are made with the second upper metal layer. A large number of vias strongly connect the wires at the crossing points. The proportion between the width of the metal and the distance between wires is called *metal coverage* M_C of the given layer. Thus, M_C = 0.5 means that 50% of the surface is covered by the PDN wires and the other 50 % is free for routing other signals. The PG/G is usually made by two or more perpendicular metal layers, so metal coverage could be different in X and Y direction, which will be identified as M_{CX} and M_{CY}. Figure 1 shows a square IC with five, twenty-five, seventy-five and three hundred and seventy-five horizontal and vertical wires for the power grid. There, $M_{CX} = M_{CY} = 0.2$.

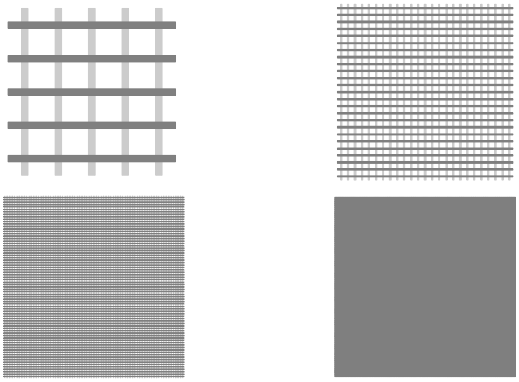

Figure 1. Four square power grids with 5×5, 25×25, 75×75, and 375×375, regularly spaced wires.

In this Figure only the power grid is represented. It is assumed that a parallel mesh exists for the ground signal. In the peripheral bounding IC packages, the power/ground pads are usually connected at the four sides of the PDN. Each pad

connects directly to one or more PDN wires, or the connection is made through peripheral power/ground rings. The first solution saves space but has the drawback that an important IR-drop may exist near the points where the supply pads connect to the PDN. The second solution ensures a better current distribution but at cost of more space. In this report we assume that the PDN has ideal power and ground rings, thus ensuring that the nominal supply voltage V_{DD} is present at the four sides of the PDN. However, as we analyze the voltage *drop*, not the absolute voltage, we take the power ring voltage as zero. The problem of the IR-drop near to supply pads in PDN without supply rings is not analyzed here.

As Figure 1 shows, each wire of the power grid can be thought as a set of metal segments connected in series at the crossing points. Each segment has a given resistance, according equation (1):

$$R_{segX} = R_{SX}\frac{P_X}{W_X} = \frac{R_{SX}}{M_{CX}} \qquad R_{segY} = R_{SY}\frac{P_Y}{W_Y} = \frac{R_{SY}}{M_{CY}} \tag{1}$$

Where R_{SX} and R_{SY} are the metal sheet resistances, and P_X, P_Y, W_X and W_Y are the pitch and width of the segments in X and Y axes, respectively (see Figure 2).

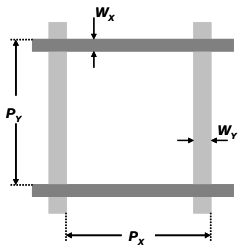

Figure 2. Wire segments.

In its turn, the current consumed by the IC flows from the power pads to the ground pads through the power and ground grids. So, the current drawn by the portion of the IC below a crossing point can be represented as a local current sink connected to this point. In this way, the power grid and the whole IC below it can be modeled by a mesh of cells with the equivalent electrical circuit depicted in Figure 3. There, the grid is composed by $M\times N$ wires, current sinks $I_{i,j}$ are the local current consumption in the cell i,j, and $R_{segX}/2$ and $R_{segY}/2$ are a half of the resistances R_{segX} and R_{segY}. A conductor with zero resistance models the power ring surrounding the periphery of the power grid. A similar equivalent circuit can be drawn for the ground grid.

As shown in Figure 3, this configuration is well adapted to calculate the IR-drop by using the method of finite differences. Notice, however, that this method approximates a continuous problem by a discrete version of it, whereas our problem is discrete from the beginning. So, by finding the IR-drop in the power grid using the model of Figure 3, we find a solution which is as *exact* as the assumptions made. However, at this point the only assumption made is zero voltage at the four sides of the power grid, which is a very weak assumption if power/ground rings are available.

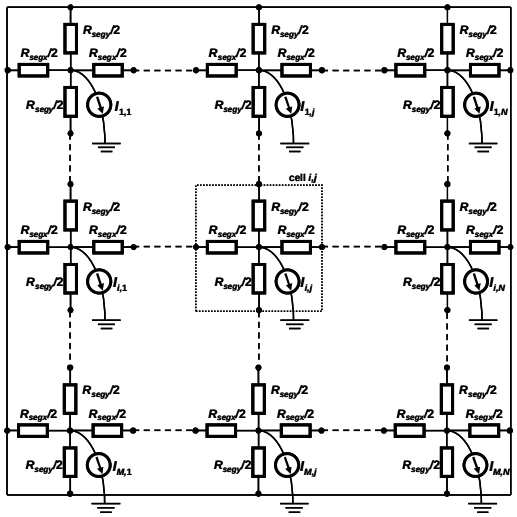

Figure 3. Electrical model of the power grid.

By applying Kirchhoff current law to the i,j cell we can write for the crossing point i,j:

$$\frac{V_{i,j-1}}{R_{segX}} + \frac{V_{i,j+1}}{R_{segX}} + \frac{V_{i-1,j}}{R_{segY}} + \frac{V_{i+1,j}}{R_{segY}} - 2V_{i,j}\left(\frac{1}{R_{segX}} + \frac{1}{R_{segY}}\right) = I_{i,j} \tag{2}$$

Formula (2) should be properly modified for the cells at the four corners and at the four sides of the PDN. By doing so, it is possible to write in matrix form the set of equations for current balance at the whole power grid, as follows:

$$\mathbf{GV} = \mathbf{I} \tag{3}$$

Where **G** is the $(M\times N)\times(M\times N)$ matrix of coefficients (conductances) of the $(M\times N)\times 1$ unknown voltages $V_{i,j}$ and **I** is the $(M\times N)\times 1$ column of currents $I_{i,j}$. The voltages $V_{i,j}$ are identified as the IR-drop voltage at each cell.

For Dirichlet problems as the one considered here, it is shown that **G** has the required properties to be invertible [4]. Thus, it is possible to calculate **V** as follows:

$$\mathbf{V} = \mathbf{G}^{-1}\mathbf{I} \tag{4}$$

It is clear that if the current drawn by each cell $I_{i,j}$ is constant and M and N are odd numbers, the maximum IR-drop is at the cell placed at the center of the PDN.

For given IC dimensions L an H, if the number of wires N and M is large enough, for constant metal coverage, the power grid looks like a continuous plate of conductive material (see Figure 1) with effective sheet resistances R_{sx} and R_{sy} in the X and Y directions, as follows

$$R_{sx} = \frac{R_{SX}}{M_{CX}} \frac{P_X}{P_Y} \qquad (5)$$
$$R_{sy} = \frac{R_{SY}}{M_{CY}} \frac{P_Y}{P_X}$$

In these conditions, the static IR-drop in the PDN follows closely the solution of the Poisson equation (6), [1][7].

$$\frac{1}{R_{sx}} \frac{\partial^2 V}{\partial x^2} + \frac{1}{R_{sy}} \frac{\partial^2 V}{\partial y^2} = J \qquad (6)$$

where V is the IR-drop voltage, R_{sx} and R_{sy} are the effective sheet resistances of the PDN in X and Y respectively, and J is the current density function.

Notice the relationship between equations (3) and (6). Equation (3) can be interpreted as the discrete approximation of equation (6), as is usual in the finite differences method to solve Poisson equation. But the opposite is also true: equation (6) can be interpreted as the continuous approximation of (3), and all the analytical methods to solve Poisson equation will be useful to get its solution. This approximation is more accurate when the number of wires N and M are large. How large they must be?

The following example sketches the answer to this question. It shows the difference between the solution of (3) and of (6) for the maximum IR-drop voltage, as a function of N and M. Figure 4 shows the calculated IR-drop in the center cell of a square PDN with $R_{SX} = R_{SY} = 0.1$ Ω/square and $M_{CX} = M_{CY} = 0.1$ as a function of N (here $N = M$). The current drawn by the IC, $I = \sum I_{i,j}$ is uniformly distributed over the surface, so current density J and $I_{i,j}$ are constant. Circles are the values obtained with equation (3), and the line is the value obtained from the continuous approximation (6). The axis X is the number of wires and the Y axis is the IR-drop voltage at the center of the PDN, in mV.

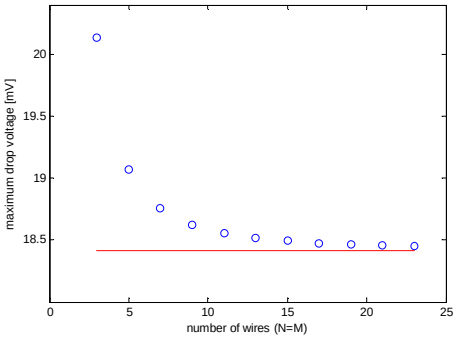

Figure 4. Maximum IR-drop in a square power grid as a function of the number of wires (circles) (3), and from the continuous approximation (6), line.

As can be seen, the continuous approximation value is asymptotically close to the discrete values from relatively small N. Figure 5 shows the difference in % between the maximum IR-drop according to (3) and from (6) for the same example.

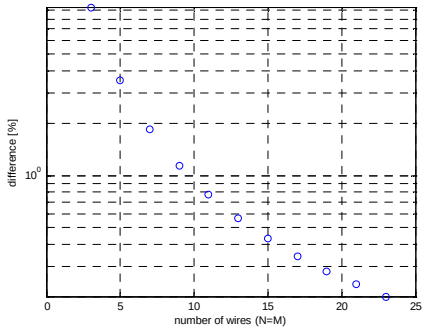

Figure 5. Difference in % between maximum IR-drop according to (3) and (6) for the example.

As can be seen, the difference falls below 1% for $N = M = 11$, and decreases almost exponentially with N. Other examples show similar results. It is worth to comment that these results are independent of the PDN size, provided that the total IC current I be constant, being the only significant parameters the metal coverage and the sheet resistances.

In realistic PDNs, N and M are usually in the range of several tens to about one hundred. So, the problem of the IR-drop can be analyzed by using the continuous approximation (6) with a negligible error. This is the approach followed by Shakeri in [1] and Huang in [8], and also in this paper.

Equation (5) is the link between the physical and geometrical variables of the PDN, as metal width and pitch, metal coverage, and sheet resistance, and its mathematical representation in equation (6). Moreover, by a change of variables, it is possible to further simplify equation (6) in order to work with only a single value for the effective sheet resistance, R_s. To do so, we first define the following constant:

$$k = \sqrt{\frac{R_{sx}}{R_{sy}}} \qquad (7)$$

Next, we change the independent variables in the following way:

$$x \to \frac{x^*}{k}, \qquad y \to k y^* \qquad (8)$$

And now (6) transforms into

$$\frac{\partial^2 V}{\partial x^{*2}} + \frac{\partial^2 V}{\partial y^{*2}} = J R_s \qquad (9)$$

where

$$R_s = \sqrt{R_{sx} R_{sy}} \qquad (10)$$

Indeed, the PDN dimensions (length L and height H) change according to (8). They will now be

$$L^* = Lk, \qquad H^* = \frac{H}{k} \qquad (11)$$

The anisotropic problem (6) is thus converted into the isotropic one (9) at the small price of making a change in the IC dimensions, (11).

For the sake of simplicity and without loss of generality, in the rest of the paper we will work with equation (9), and isotropic sheet resistance R_s according to (10), and will remove the superscript * in x, y, H and L.

III. MAXIMUM IR-DROP

According to equation (9), V is the IR-drop voltage of a PDN in V, R_s is the isotropic sheet resistance in Ω, and J is the current density function in A/m^2. The IR-drop at the boundaries of the whole IC is assumed to be zero volts.

This paper analyzes the following two cases to find explicit equations for the position and value of the maximum IR-drop, which are parameters of maximum interest in PDN design:

1. Constant R_s and J
2. Constant R_s but different J

A. First case: constant R_s and J

In this case, the equation to solve and the boundary conditions become

$$\frac{\partial^2 V}{\partial x^2}+\frac{\partial^2 V}{\partial x^2}=R_s J \quad \text{for } (x,y)\in D, \qquad V=0 \quad \text{at } \partial D \tag{12}$$

where D is just the rectangle $0 \le x \le L$, $0 \le y \le H$ and ∂D is the boundary. System (12) can be solved by finding the Green's function $G(x, y, x_0, y_0)$ of the problem and integrating it over D. In this case, the Green's function may be obtained in terms of a classical double Fourier series, which is the approach followed in [1], or of a single Fourier series [3][4], the one corresponding to one of the two variables, x or y. The latter approach has the advantage that the resulting solution turns out to have much better convergence properties than the standard double Fourier series, so truncation yields far more accurate approximations. Since we are dealing with the case of constant R_s and J, this problem is symmetric in both x and y variables, and the maximum IR-drop takes place at the centre of the rectangle, which is given by

$$V_{\max}=\frac{4IR_s}{r\pi^3}\left(\frac{\pi^3}{32}-\sum_{k=0}^{\infty}\frac{(-1)^k}{(2k+1)^3}\frac{1}{\cosh\dfrac{(2k+1)\pi r}{2}}\right) \tag{13}$$

where $I = JHL$ is the total current of the IC and $r = H/L$ is the aspect ratio of the rectangle. The series in (13) is strongly convergent, so we may keep just the first term as an approximation to the maximum value of V:

$$V_{\max}\approx\frac{4IR_s}{r\pi^3}\left(\frac{\pi^3}{32}-\frac{1}{\cosh\dfrac{\pi r}{2}}\right) \tag{14}$$

the relative error being less than 0.12 % in the worst case (r = 1). Now, by reversing the change of variables (8) and dimensions (11), and considering (5), it is possible to find the required wire width and pitch in each metal layer for the maximum IR-drop specified.

Notice how expression (14) extends the one shown in [1], which is only for square ICs, to the more general case of rectangular ICs.

B. Second case: constant R_s but different J

In this section we deal with regular PDNs whose sheet resistance, R_s, is constant throughout the chip, but whose current consumption is now piecewise constant. In particular, we consider a set of N different rectangular blocks, each of which has a constant current density, J_k. k = 1, 2, … N, The IC domain is, as before, a rectangle, D, with sides L and H. We denote by l_k and h_k the dimensions of block k.

In this case, we can also derive expressions for the IR-drop voltage at each point of the chip by simple linear decomposition of the problem into N simpler equations, one for each block, that is, $V = \sum V_k$, where V_k satisfies

$$\frac{1}{R_s}\nabla^2 V_k = J(x,y)=\begin{cases}J_k & \text{for } (x,y)\in D_k\\ 0 & \text{for } (x,y)\in D-D_k\end{cases} \qquad V_k=0 \quad \text{at } \partial D \tag{15}$$

where D_k are rectangular areas with the same current consumption and $D = \cup D_k$. At this point, we can also use the previously derived single Fourier series of the Green's function to obtain the corresponding solution when there is a different current consumption in each block.

The idea is again to decompose the problem with N different blocks into N problems where only one of the blocks has a non-vanishing current consumption. We thus start by considering a single block whose bottom left corner is denoted by (x_1, y_1) and upper right corner by (x_2, y_2), and with a current density of J_k. Now, to derive the corresponding voltage drop at any point of the IC, we just need to integrate the single Fourier series representation of the Green's function [3][4].

The result is shown in the equations (16-19).

$$V_k(x,y)=-\frac{2J_kR_sL^2}{\pi^3}\sum_{n=1}^{\infty}\frac{\sin\dfrac{n\pi x}{L}\left(\cos\dfrac{n\pi x_1}{L}-\cos\dfrac{n\pi x_2}{L}\right)}{n^3\sinh\dfrac{n\pi H}{L}}\cdot \cdot\begin{cases}f_{1n}(y) & \text{if } 0\le y\le y_1\\ f_{2n}(y) & \text{if } y_1\le y\le y_2\\ f_{3n}(y) & \text{if } y_2\le y\le H\end{cases} \tag{16}$$

where

$$f_{1n}(y)=\sinh\frac{n\pi y}{L}\left(\cosh\frac{n\pi(y_2-H)}{L}-\cosh\frac{n\pi(y_1-H)}{L}\right) \tag{17}$$

$$f_{2n}(y)=\sinh\frac{n\pi y}{L}\left(\cosh\frac{n\pi(y_2-H)}{L}-\cosh\frac{n\pi(y-H)}{L}\right)+\sinh\frac{n\pi(y-H)}{L}\left(\cosh\frac{n\pi y}{L}-\cosh\frac{n\pi y_1}{L}\right) \tag{18}$$

$$f_{3n}(y)=\sinh\frac{n\pi(y-H)}{L}\left(\cosh\frac{n\pi y_2}{L}-\cosh\frac{n\pi y_1}{L}\right) \tag{19}$$

On one hand, it is readily seen that the maximum IR-drop takes place inside the consuming block, that is to say, $x_{\max}\in(x_1,x_2)$ and $y_{\max}\in(y_1,y_2)$. This means the maximum of V_k is actually an interior one and therefore the partial derivatives with respect to x and y does vanish at that point. On

the other hand, the series in (16) is indeed convergent at least like $1/n^2$, but it can be manipulated in the region where the maximum lies (that is, in D_k) in order to obtain an even much convergent one. By noting that part of the series (16) and (18) can be expressed in terms of Bernoulli polynomials [10], we obtain a new strongly convergent series, as shown in (20):

$$V_k(x,y) = -\frac{JR_s}{2}\left(x^2 + \frac{x_2^2 - x_1^2 - 2Lx_2}{L}x + x_1^2\right) - \frac{2JR_sL^2}{\pi^3}\sum_{n=1}^{\infty}\frac{\sin\frac{n\pi x}{L}\left(\cos\frac{n\pi x_1}{L} - \cos\frac{n\pi x_2}{L}\right)}{n^3\sinh\frac{n\pi H}{L}} \cdot \left(\sinh\frac{n\pi y}{L}\cosh\frac{n\pi(H-y_2)}{L} + \sinh\frac{n\pi(H-y)}{L}\cosh\frac{n\pi y_1}{L}\right) \quad (20)$$

Note that now the convergence of the remaining series is exponentially fast. That is to say, the absolute error when truncating after the N-term of the series is easily found to be bounded by

$$|e_N| \le \frac{3}{4N^2}\left(e^{-\frac{N\pi(y_2-y)}{L}} + e^{-\frac{N\pi(y-y_1)}{L}}\right) \quad (21)$$

We note that if y_2 - y_1 is small, this absolute error is no longer exponentially small and it only decays quadratically. This must be taken into account when dealing with very small blocks. In particular, by keeping the first term in (20), we obtain a closed form approximate expression for the voltage drop inside the block. We now find the position of the maximum IR-drop in terms of this approximate expression by differentiating it with respect to y and finding the zeroes. This provides a rather simple expression for the y-coordinate of the maximum:

$$y_{\max} \approx \frac{L}{\pi}\tanh^{-1}\left(\frac{1}{\tanh\frac{\pi H}{L}} - \frac{\cosh\frac{\pi(y_2-H)}{L}}{\cosh\frac{\pi y_1}{L}\sinh\frac{\pi H}{L}}\right) \quad (22)$$

As for the x-coordinate, note that we could also have obtained a similar solution as (20) in terms of variable y instead of x. By doing so and repeating the same steps as before, we obtain the dual expression for the x-coordinate of the maximum IR-drop:

$$x_{\max} \approx \frac{H}{\pi}\tanh^{-1}\left(\frac{1}{\tanh\frac{\pi L}{H}} - \frac{\cosh\frac{\pi(x_2-L)}{H}}{\cosh\frac{\pi x_1}{H}\sinh\frac{\pi L}{H}}\right) \quad (23)$$

It is thus natural to consider expressions (22) and (23) as an approximation for the position of the maximum IR-drop. These expressions turn out to be rather accurate, as shown in Table I. We note that only when the blocks are very small and/or the consuming block is close to the boundary does the relative error become larger than 2%.

Table I. Position of the maximum IR-drop for a square chip of 100 units per side with a single consuming block, for seven different blocks. The approximate position corresponds to expressions (22)-(23). This approximate solution is compared with the solution of (15) obtained from simulation.

	Block edges	(22)-(23) (x_{max}, y_{max})	Simul. (x_{max}, y_{max})	|%rel. error|
1	(10,30)-(70,50)	(44.0519,40.7741)	(43.578,40.689)	1.08
2	(10,10)-(90,90)	(50,50)	(50,50)	0
3	(40,40)-(50,50)	(45.1598,45.1598)	(45.0,45.0)	0.36
4	(70,10)-(90,15)	(76.5431,13.6801)	(79.2934,13.1250)	4.22
5	(35,20)-60,40)	47.7470,31.8199)	(47.3664,31.2070)	1.96
6	(40,30)-(70,70)	(54.3546,50)	54.3886,49.7665)	0.47
7	(50,25)-(90,65)	(65.3135,45.9974)	(65.7756,45.5592)	0.96

As for the value of the maximum IR-drop, Tables II and III compare the value of the maximum voltage drop when equation (15) is solved by simulation with the corresponding value obtained by retaining only the first term in series (20), and evaluating it at the position of the maximum given by (22)-(23). It is clear that decreasing block size and greater proximity of the block to the boundaries lead to worse approximations using only the first term. However, upon taking some more terms in the series, the relative error is small.

Table II. Maximum IR-drop for a small chip of 1.3 mm length, 2.5 mm height, and with a single active block with J = 1 A/mm^2 and sheet resistance R_s = 0.3 Ω/square for two sets of places for the active block; the first four correspond to a large active block [A], while the following four correspond to a small one, [B]. Column 3: numerical solution to (15). Column 4: approximate solution using (20) with one or more terms whenever the relative error is > 7%.

	Block edges [mm]	Simul. [V]	(20) [V]	|% rel. error|
[A]	(0,0)-(0.7,2.5)	0.0359	0.0359	**0.06**
	(0.5,0)-(1.1,2.0)	0.0374	0.0374	**0.08**
	(0.1,0.2)-(0.5,2.2)	0.0214	0.0215	**0.25**
	(0.23,0.65)-(1.23,2.15)	0.0482	0.0482	**0.03**
[B]	(0.1,0.2)-(0.5,0.5)	0.0076	0.0115 (N=1)	43.53
			0.0081 (N=2)	**6.61**
	(1.0,0.6)-(1.2,1.1)	0.0059	0.0070 (N=1)	19.33
			0.0061 (N=2)	**4.15**
	(0.8,0.5)-(0.9,0.7)	0.0024	0.0035 (N=1)	42.9
			0.0027 (N=2)	10.54
			0.0025 (N=3)	**1.61**
	(0.1,0.6)-(0.2,1.1)	0.0027	0.0032 (N=1)	17.11
			0.0029 (N=2)	**5.94**

We also note that the data in Table III correspond to a larger IC than that in Table II. As a consequence, for some blocks we find that the IR-drop is relatively large. This would imply increasing the metal coverage (if possible), or considering the use of another kind of package (flip-chip). As can be seen, this type of tradeoffs can be easily checked with comparatively a small effort, by applying a few closed form formulas.

Table III. Maximum IR-drop for a square chip of 3.5 mm per side with a single active consuming block with J = 1 A/mm^2 and sheet resistance R_s = 0.3 Ω/square for two sets of places for the active block; the first four correspond to a large active block [A], while the following three correspond to a small one, [B]. Column 3: numerical solution to (15). Column 4: approximate solution using (20) with one or more terms whenever the relative error is > 7%.

	Block edges [mm]	Sim [V]	Expr. (20) [V]	|% rel. err|

[A]	(0,0)-(1.4,3.5)	0.1303	0.1349	**3.53**
	(0.35,1.0)-(2.45,2.8)	0.1797	0.1823	**1.45**
	(0.35,0.35)-(2.1,2.1)	0.1471	0.1550	**5.37**
	(2.1,1.75)-(3.15,3.15)	0.0813	0.0977 (N=1)	20.2
			0.0824 (N=2)	**1.35**
[B]	(2.1,1.75)-(2.45,2.45)	0.0260	0.0341 (N=1)	31.2
			0.0277 (N=2)	**6.54**
	(2.8,0)-(3.5,0.7)	0.0189	0.0395 (N=1)	109.5
			0.0286 (N=2)	51.3
			0.0228 (N=3)	20.6
			0.0201 (N=4)	**6.34**

C. *Specific configurations of the block*

Expression (20) becomes particularly simple for some specific configurations. For instance, for a single consuming block located symmetrically with respect to the chip, the maximum IR-drop lies exactly at the centre, that is, $x_{max} = L/2$, $y_{max} = H/2$. Furthermore, if l and h are the dimensions of the block, then $x_1 = (L-l)/2$, $x_2 = (L+l)/2$, $y_1 = (H-h)/2$ and $y_2 = (H+h)/2$. Substituting all these quantities in (20) gives de simplified expression (24):

$$V_{\max} = \frac{JR_s}{8} l(2L-l) - \frac{4JR_s L^2}{\pi^3} \sum_{k=0}^{\infty} \frac{\sin\frac{(2k+1)\pi l}{2L} \cosh\frac{(2k+1)\pi(H-h)}{2L}}{(2k+1)^3 \cosh\frac{(2k+1)\pi H}{2L}} \quad (24)$$

If the block is centred with respect to one of the two coordinates, that is, the center of the chip is on either $x = L/2$ or $y = H/2$, expression (20) is also simplified. If, in particular, the block is vertically symmetric, then $y_{max} = H/2$ and furthermore, $y_1 = (H-h)/2$ and $y_2 = (H+h)/2$. Then,

$$V_{\max} = -\frac{JR_s}{2}\left(x_{\max}^2 + \frac{x_2^2 - x_1^2 - 2Lx_2}{L} x_{\max} + x_1^2\right) - \frac{4JR_s L^2}{\pi^3} \sum_{k=1}^{\infty} \frac{\sin\frac{k\pi x_{\max}}{L}\left(\cos\frac{k\pi x_1}{L} - \cos\frac{k\pi x_2}{L}\right)\cosh\frac{k\pi(H-h)}{2L}\sinh\frac{k\pi H}{2L}}{k^3 \sinh\frac{k\pi H}{L}} \quad (25)$$

where x_{max} can be calculated by the same process as that used to obtain equation (23).

Table IV compares the maximum IR-drop for symmetric blocks according to equations (24)-(25) including only one term in the summation, and those obtained from simulation.

Table IV. Maximum IR-drop for a square IC of 1 mm^2 with a single consuming block with J = 1 A/mm^2, and sheet resistance R_s = 1 Ω/square, for seven different symmetric blocks. Comparison between simulated solution in column 2, and the approximate corresponding to symmetric blocks (only the first term of expressions (24)-(25)), in column 3.

Block edges [mm]	Simul. [V]	(24) or (25)[V]	|% rel. error|
(0,0)-(0.5,1.0)	0.04599	0.04718	**2.57**
(0.1,0.1)-(0.9,0.9)	0.06874	0.06867	**0.10**
(0.4,0.3)-(0.7,0.7)	0.02835	0.02934	**3.49**
(0.2,0)-(0.7,1.0)	0.05693	0.05707	**0.25**
(0.3,0.3)-(0.5,0.7)	0.02046	0.02176	**6.35**
(0.1,0.4)-(0.8,0.6)	0.02698	0.02728	**1.11**
(0.1,0.35)-(0.7,0.65)	0.03443	0.03527	**2.44**

IV. CONCLUSIONS

This paper provides compact expressions to calculate the position and value of the maximum IR-drop in wire-bonded ICs. The findings can be summarized as follows: (*i*) for rectangular ICs of any size with a uniform current distribution, the maximum IR-drop is at the center of the chip and its approximate value is given by (14) with a maximum relative error of 0.12%; (*ii*) for rectangular ICs of any size with a non-uniform current distribution, the position of the maximum IR-drop when only one block is active is approximated by expressions (22) and (23), and its value is given by expression (20); (*iii*) for symmetric blocks, such expression can be further simplified. Due to the linearity of the governing partial differential equation, the absolute maximum IR-drop in the whole IC can be calculated by summing the contribution of each block (expression (20)). When the results for the place and value of maximum IR-drop are compared with those obtained by simulation, the maximum relative error is below 2% in most of the cases using a single term in the expressions. In the worst cases of small blocks close to the IC boundaries (where the maximum IR-drop is small), the maximum relative error increases, but falls to a small value by increasing the number of terms in the expressions.

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