Solving problems in cooperative learning classes at the EETAC – UPC

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Abstract

In this paper, a problem solving activity belonging to the Digital Circuits and Systems (CSD) course at the EETAC – UPC, is presented, describing from the initial learning objectives to the final student assessment and course processing. The learning goals of the activity include content-related and cross-curricular skills. The activity is organised as a large open-ended problem which has to be carried out by the whole class, forcing team work and project management skills in order to succeed. Taking into account the results of this experience, we propose a successful and efficient alternative to the classic methodology to teach electronic engineering.

Key words: Electronic engineering, digital systems, cooperative learning, problem-based learning, student learning portfolio, authentic assessment, teaching content through English.

1. Introduction

The compulsory subject Digital Circuits and Systems (CSD), located in the third (2A) semester of the Bachelor studies in Telematics Engineering and Telecommunications Systems (240 ECTS, 4 years), has been running now for three semesters since the reorganisation and adaptation to the EHEA of the old Bachelors in Telecommunication Engineering and Telematics (3 years), which now are in extinction.

On completion of the subject, students will be able to develop generic competences like: work cooperatively in teams to plan and develop activities; monitor the time spent in each tasks; document their work – employing as much English language as possible [1] – using text processing software, graphics tools, project management applications and other office software, paying attention to the quality criteria stipulated in the subject guides; maintain and publish a cooperative group e-portfolio to show learning results and reflexion.

With reference to the specific content, students will be introduced in the design of digital systems based on programmable logic devices (PLD), field programmable gate arrays (FPGA) and microcontrollers, using the latest electronic design automation tools (EDA) and developing boards available. They will be trained as professionals, following industry-standard design flows, going from the initial specifications of real-world applications, to the final prototyping and laboratory measurements. Our aim in this paper is explain a concrete example describing how both, the specific materials and the generic skills integrate together as a whole to produce meaningful learning.

Our course portfolio web [2], where we make visible our systematic instructional methodology of teaching (see Figure 1), contains practically all of our materials which have been developed since the beginning of our teaching innovations in 2002/03, and it may be used to get a deeper inside on the paper content. Furthermore, the paper will contain hyperlinks to relevant documents or pictures to better explain the specific technical content of the example project.

Paper content will include the following sections: learning objectives, understanding the problem, devising a plan, carrying out the plan, assessing group and individual learning, and results and discussion.

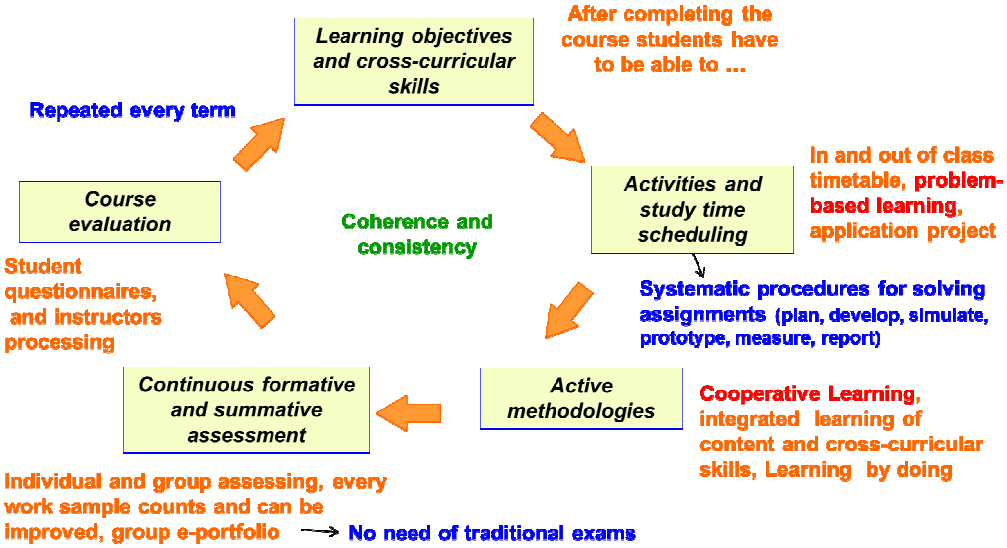

Figure 1. *The systematic instructional methodology*

2. Learning objectives

The complete list of CSD course learning objectives can be read at this link [a]. Particularly, the cross-curricular and content-related goals of the example discussed in this paper which comes from the course's Chapter III, can be read at this link [b].

In order to fulfil the objectives, the idea, as shown in Figure 1, is to prepare problem-based activities that are going to be solved recreating a truly cooperative environment in which not only the 3-member base groups, but all the class have to be involved in order to succeed. The problem solving strategy is adapted from Pólya (1945) [3], and goes through four consecutive phases: (1) understanding the problem; (2) devising a plan, (3) carrying out the plan; and (4), looking back. Therefore, in the following sections, and for a very specific example, the most remarkable issues attaining each phase will be discussed.

3. Understanding a problem

Let's take, as shown in Figure 2, one of the course "real-world" design examples, the 4-bit serial multiplier presented in Chapter III [c] on dedicated processors. As a solution to the problem, students have to configure the Lattice complex programmable logic device (CPLD) in the HWD-LC4128V [d] board represented in Figure 2 so that it behaves as specified. The problem's web page [e] will contain all the files, pictures and related materials discussed in this paper.

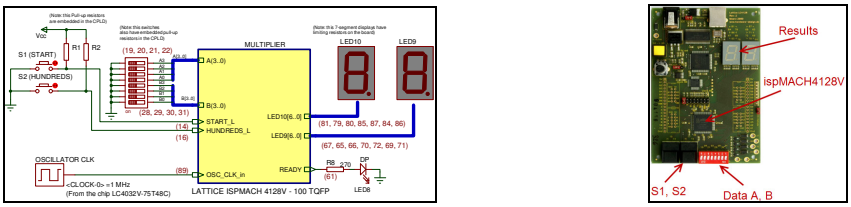

Figure 2. *The problem of a 4-bit binary serial multiplier and the target board with the PLD chip where to verify the solution (Ctrl+Click to follow the link of the picture in normal size [f], [g])*

Aiming to understand the project, class discussions with instructor's guidance on the way to approach the solution to the problem, are held during initial sessions: some general materials concerning how the design has to work, which has to be the initial specifications, the expected results, the algorithm that the digital circuit has to solve in order to multiply unsigned numbers, how this large problem can be decomposed into smaller and easy to design blocks, which references can be studied on similar arithmetic problems, etc. The purpose is to present an open-ended [h] problem (see Figure 3), which certainly can be solved satisfactorily in different ways; however, we will try to approach a solution using as much knowledge from precedent chapters as possible. Thus, giving the students another opportunity to revise and deeply understand previous concepts at the same time of learning new ones.

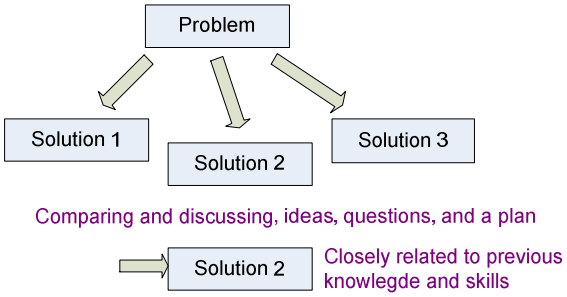

***Figure 3**. The open-ended problem solving.*

The assignment (EX3 [i]) is carefully arranged to facilitate the preparation of a quality document or an oral presentation. The whole structure and the main sections involved in a typical CSD exercise can be seen in Table 1. It is organised having in mind the idea that necessarily all the group members have to contribute if they really pretend to produce a task with enough quality to get a high mark.

***Table 1.** Typical CSD exercise main sections.*

1. Group names and fairness statement	2. Acknowledgements to people who assisted the group
3. Introduction	4. Topic list
5. Group's study time	6. Abstract
7. Table of content	8. Assignment
9. Problem solution	10. References
11. Group's study plan	12. Topics and activities checklist
13. Grading grid including self-assessment	14. Questions

For instance, Table 2 shows the checklist to highlight the relations between topics, activities through which topics will be learned, and students in command of every activity. Most of the tasks are carried out in base groups, while some important topics, the ones related to what we call basic knowledge, are specified to be done by each student individually.

***Table 2**. Topics and activity checklist.*

Topics	Activities (EX3 [i] assignments)	Group member in charge			Comments
		1	2	3	
Organise and discuss project specifications	a)				
Concept of a datapath	b)				
Concept of "flags" or operation indicators	b)				
The concept of a control unit (FSM)	b)				
Use the VHDL test bench entity to simulate designs	c)				Individual
Use VHDL statements ASSESS and REPORT	d)				Individual
Planning the achievement of a complex project as a sequence of phases which includes every time more specifications	e) f) g)				
Top-down strategy to plan the project and a bottom-up sequence to design component by component up to the top.	h) i) j)				Individual
Digital auxiliary modules	k)				
Do an oral presentation of the project	l)				

This first phase in problem solving ends when the top-down project organization with all the details such as the number of hierarchical blocks involved and their functionality, signals and file names, nested diagrams and the like are clarified. These materials are uploaded [j] at the course web page to be used as a common reference frame to all the class. They will be updated with newer information for the time the problem is being developed, and will guide the consecution of the final solution. These materials also serve for future references, for instance, for student in their final bachelor's thesis.

4. Devising a plan

Once the problem is understood, a plan has to be elaborated to be carried out through next sessions in and out of the classroom. The schedule must contain, at least:

1) Revision of common theory associated with the problem, so that they can learn and do by themselves most of the tasks.
2) A task for every cooperative group in class to be solved following the known design flow and tools from previous chapter (this term: VHDL, vendor dependent CAD and simulation tools like Lattice ispLEVER Classic and Aldec Active-HDL; however, in other terms, another set of tools from different vendors like Altera or Xilinx, are used).
3) Common tasks to be performed by everybody to introduce and put into practice new concepts.
4) Due date for handing in deliverables uploading them at the group's ePortfolio.
5) Quality criteria setting the standards to which the groups must adjust their solutions.

Figure 4 shows the internal architecture of the multiplier, the cooperative group in charge of each block design, and the connection to previous chapters so that they can find valid references to start with.

At the problem web page, a table [k] will include the name and the main details associated to each block to be designed. All the groups will have to respect the naming conventions and coding styles, in order to make them all compatible. Therefore, the idea that not only the cooperative group, but all the class (company) goes on the same ship (project) and has to speak the same language (quality criteria) in order to succeed, is extremely reinforced [4] through all the activity. Student and base groups realise how important is their implication and personal work, and they wonder why they cannot get the highest marks if there are some groups or individuals who do not perform as expected.

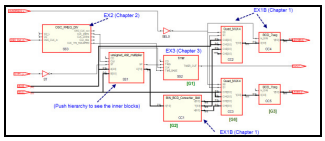

Figure 4. *Top – down hierarchical planning for the 4-bit multiplier [G7] (Ctrl+Click to follow the link of the picture in normal size [l]).*

Figure 5 shows the internal planning of the 4-bit unsigned serial multiplier presented as a dedicated processor which is going to execute the "add & shift" algorithm.

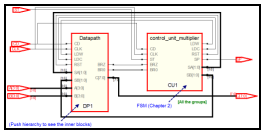

Figure 5 *The internal architecture of the unsigned 4-bit multiplier presented as a dedicated processor. [Instructor] (Ctrl+Click to follow the link of the picture in normal size [m]).*

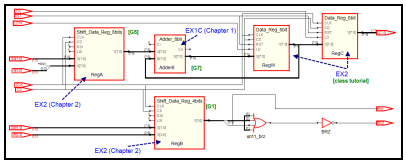

***Figure 6**. Schematic of the datapath internal architecture [Instructor] (Ctrl+Click to follow the link of the picture in normal size [n]).*

5. Carrying out the plan

This is the project phase where each base group is responsible to design and test the block assigned to them before the due date. It is a bottom-up strategy. All the previous training from chapters I and II on combinational circuits and sequential systems, may be applied here. Students know that their component has to work as expected in order to be used in the large project of the multiplier. They also notice that their component will become a new part in the course library [o] of components to be used in future semesters. All these facts contribute to keep them motivated and up to date.

Some of the project's important blocks, like the unsigned multiplier control unit, which state diagram is represented in Figure 7, are considered apart and solved by the whole class. In this way, instructors try to avoid any gap in what is considered basic knowledge.

Some groups or even the instructors are also responsible for the VHDL structural code associated with the multiplier, thus, schematics like the ones represented in previous figures can the automatic drawn by the RTL netlist tool. This tactic makes possible to partially simulate and compile the whole project even if all of its components are not yet completely designed.

Once designed and validated, the component is uploaded at the group's ePorfolio page, so that it is made available instantly to all the class, facilitating that students learn from their own works.

At this point, it must be said that working with the professional electronic design automation (EDA) tools which are downloaded from the vendors web pages or acquired under school licenses, is essential because they see that even their "academic" assignment looks like a professional one, they work like real engineers in the field using the same set of instruments and processes, they appreciate that most of the study time invested in the course is highly worthwhile. And even more, the learning materials and exercises will be available *forever* at the course's web page and at their own open portfolios once the course finished.

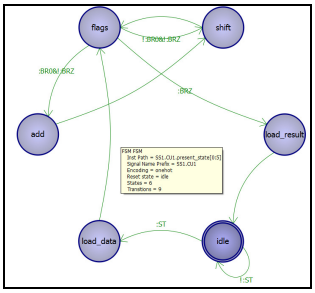

***Figure 7** Multiplier's control unit state diagram (Ctrl+Click to follow the link of the picture in normal size [p]).*

6. Assessing group and individual learning

The cooperative group ePortfolio [q] based on Google Sites is where all the course materials and reflexions produced by the students are located. Every class has its online agenda [r] where to find the cooperative group link to their ePortfolio.

In order to verify individual accountability and prevent hitchhiking [5], an individual test (see this example [s]) is given to each student, while in class, instructor observes groups behaviour and

records the frequency with which each member contributes to the group's work. In this way, students promptly realise (generally, while in the first month of classes) that if they do not contribute fairly or rely too much in other members' work, they have to make their mind up, in the sense of changing their behaviour, or instead, abandoning the course.

Equation (1) shows the way to calculate the final grade. It is composed by a weighted sum of up to 15 terms.

$$G = EX\ (30\%) + IT\ (25\%) + AP\ (20\%) + eP\ (15\%) + ActP\ (10\%) \quad (1)$$

$$EX = EX1A + EX1B + EX1C + EX2 + EX3 + EX4A + EX4B$$

$$IT = IT1 + IT2 + IT3 + IT4$$

$$eP = eP1\ (5\%) + eP2\ (10\%)$$

$$AP = APdoc\ (5\%) + APpre\ (15\%)$$

7. Results and discussion

Using the active methodology based on cooperative group work on solving "real" problems [4], a large number of students get involved and show better opinion in the course than previously, when this subject matter was organised in theory and laboratory sessions in a traditional individualistic (and competitive) fashion of teaching. Many improvements and systematic design of instruction positively tested and reported [t] [6] in the old bachelor degree subjects of Digital Electronics and Electronic Digital Systems, are applied again in this new subject.

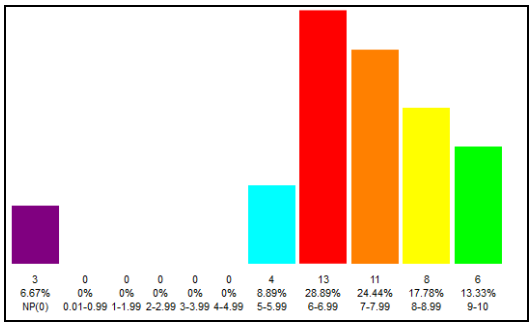

Figure 8 *Student CSD grades for semester 10/11 Q1.*

In addition to the formative assessment associated to each activity, some questionnaires are introduced by the school staff and by the instructors (SEEQ [u]), in order to have a fast feedback on how student are learning, enabling the option of making changes and adaptations on the go or once the course has finished (see Figure 1). Figure 9 shows results from three questions, but the feedback section [v] of the web page contains an updated archive of questions and answers.

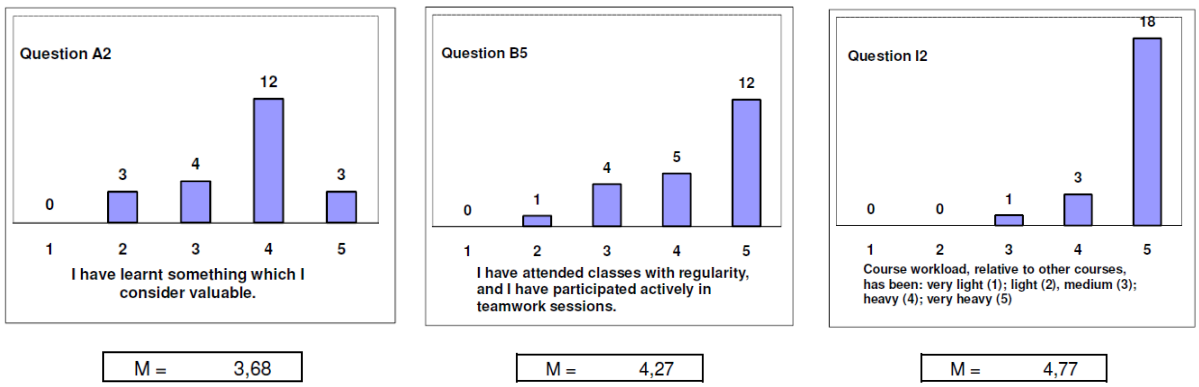

Figure 9*. Three questions from the SEEQ questionnaire for semester 10/11 Q1.*

Digital systems are an area of knowledge which changes and evolves at a fast pace, making the teaching very demanding to both instructors and students. Our methodology, integrating content and cross-curricular skills, emulating the proceedings of a company which designs applications, has appeared to be quite effective. However, there is still room for improvements in the course organisation, most of which may be detected gathering information on the course development and analysing before starting a new semester, as shown in Figure 1. To name a few:

- The individual test on basic knowledge (IT), tied to the related exercise on the corresponding chapter, has to be used more effectively to assess individual accountability, in a way that any student with these exams failed cannot pass the course.
- Course content still has to be adjusted so that the workload is kept under normal parameters (6 ECTS). We realise that students find it very hard learning in only a term all the specific content[1], so an elective subject should be proposed to get a better coverage of the subject area at this bachelor level.

Our work demonstrates that the systematic instructional methodology carried on in CSD, but perfectly extensible to other similar subjects in engineering studies, which is based on *active* teaching of both, content and cross-curricular skills, achieve substantial improvement over a more traditional approach mainly based on lectures, laboratory assignments and examinations on content. From the student side, some of the benefits reported are: less failure and abandon, more motivation and participation in class activities, higher grades and consequently, deeper understanding of the subject content. From the instructor side, the initial drawback associated with the learning of the mechanical use of the methodology, is far compensated by advantages like true cooperation between teaching staff, constant revision and update of subject materials, overall class performance, which ends benefiting collaterally other subjects and the school in general.

8. References

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References to additional links:

[a] http://digsys.upc.es/ed/CSD/units/CSD_acord.pdf

[b] http://digsys.upc.es/ed/CSD/prob/Ch3/P10/objectives.docx

[c] http://digsys.upc.es/ed/CSD/units/Ch3/E1Ch3u.html

[d] http://digsys.upc.es/ed/components/components.html#HWD

[e] http://digsys.upc.es/ed/CSD/prob/Ch3/P10/Prob3_10.html

[f] http://digsys.upc.es/ed/CSD/prob/Ch3/P10/fig2.gif

[g] http://digsys.upc.es/ed/CSD/prob/Ch3/P10/fig2b.png

[h] http://mste.illinois.edu/users/aki/open_ended/WhatIsOpen-ended.html

[i] http://digsys.upc.es/ed/CSD/terms/1011Q2/EX/EX3/CSD_10_11_Q2_EX3_Multiplier.docx

[j] http://digsys.upc.es/ed/CSD/terms/1011Q2/probl.html#EX3

[k] http://digsys.upc.es/ed/CSD/terms/1011Q2/probl.html#EX3P3

[l] http://digsys.upc.es/ed/CSD/prob/Ch3/P10/fig4.png

[m] http://digsys.upc.es/ed/CSD/prob/Ch3/P10/fig5.png

[n] http://digsys.upc.es/ed/CSD/prob/Ch3/P10/fig6.png

[o] http://digsys.upc.es/ed/components/components.html

[p] http://digsys.upc.es/ed/CSD/prob/Ch3/P10/fig7.png

[q] http://digsys.upc.es/ed/CSD/eportfolio/CSDportfolio.html

[r] http://digsys.upc.es/ed/CSD/terms/1011Q2/probl.html

[s] http://digsys.upc.es/ed/CSD/terms/1011Q2/IT/3GT21_IT3.docx

[t] http://digsys.upc.es/ed/general/organitzacio.html

[u] http://digsys.upc.es/ed/CSD/feedback/Full_Questionaire_SEEQ_English_CSD_v1.pdf

[v] http://digsys.upc.es/ed/CSD/feedback/CSDfdbk.html