Gate Leakage Impact on Full Open Defects in Interconnect Lines

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***Abstract*—An Interconnect full open defect breaks the connection between the driver and the gate terminals of downstream transistors, generating a floating line. The behavior of floating lines is known to depend on several factors, namely parasitic capacitances to neighboring structures, transistor capacitances of downstream gate(s) and trapped charges. For nanometer CMOS technologies, the reduction of oxide thickness leads to a significant increase in gate tunneling leakage. This new phenomenon influences the behavior of circuits with interconnect full open defects. Floating lines can no longer be considered electrically isolated and are subjected to transient evolutions, reaching a steady state determined by the technology, downstream interconnect and gate(s) topology. The occurrence of such defects and the impact of gate tunneling leakage are expected to increase in the future. In this work, interconnect full open defects affecting nanometer CMOS technologies are analyzed and the defective logic response of downstream gates after reaching the steady state is predicted. Experimental evidence of this behavior is presented for circuits belonging to a 180 nm and a 65 nm CMOS technologies. Technology trends show that the impact of gate leakage currents is expected to increase in future technologies.**

***Index Terms*—Gate leakage current, interconnect line, interconnect open, nanometer technology, open defect.**

I. Introduction

INTERCONNECT open defects are becoming more common in CMOS technologies due to the increasing number of contacts and vias [1] and the replacement of aluminum by copper in interconnections [2]. An interconnect open defect consists of the partial or total breaking of the electrical connection between two points of an interconnect line. A high percentage of open defects completely isolates the two end points of the line, referred to as *strong* or *full* opens. Nevertheless, a non-negligible number of such defects becomes only partial disconnections of the affected line, being then known as *weak* or *resistive* opens [3].

During the last few decades, intensive research effort has been devoted to the characterization of CMOS Integrated Circuits (ICs) with open defects. The first works dealt with full open defects [4]–[12]. Some [13], [14] addressed the special case of a full open generating a thin disconnection which enables electrons and holes to tunnel through creating a current through the disconnected points. In recent years, considerable interest has been focused also on the characterization of resistive open defects [15]–[20].

Studies have addressed the impact of open defects for a wide spectrum of technologies, including the deep submicron domain. In this context, gate oxide thickness may already be scaled below 20 Å, leading to an increase in gate leakage currents caused by tunneling mechanisms in such a way that these currents become comparable to subthreshold leakage currents [21].

In order to characterize interconnect full open defects in nanometer CMOS technologies, both layout information and gate leakage currents need to be considered. In the presence of such defects, gate leakage currents become non-negligible and generate a transient response of defective nets [22], [23]. In older technologies, gate leakage currents were negligible, and could therefore be discarded. However, for nanometer technologies, gate leakage currents become non-negligible. In this context, previous works proposing test approaches targeting interconnect open faults [24]–[27] can no longer assure their effectiveness with the influence of gate leakage currents.

The paper is organized as follows. In Section II, the fundamentals of gate leakage currents are reviewed. Section III analyses the electrical model of interconnect full open defects. The behavior of the floating line influenced by gate leakage currents is reported in Section IV. Section V generalizes the case when the floating line has a fan-out. Test implications derived from influence of gate leakage currents is presented in Section VI. Experimental validation of the work for floating lines belonging to two different technology nodes is provided in Section VII. Future trends of the influence of gate leakage currents on floating lines for nanometer technologies are reported in Section VIII. Finally, some conclusions are drawn.

II. Direct Gate Tunnelling Leakage Currents

In CMOS technologies, three different tunneling phenomena can contribute to the transistor gate leakage current. The physical mechanisms causing these currents are known as Fowler-Nordheim, direct and trap-assisted tunneling. In nanometer CMOS technologies, for ultrathin silicon oxide layers and low electric fields, the direct tunneling mechanism becomes the major contributor to the total gate leakage current. Therefore, throughout the paper the impact of the direct tunneling current contribution is analyzed in circuits with open defects.

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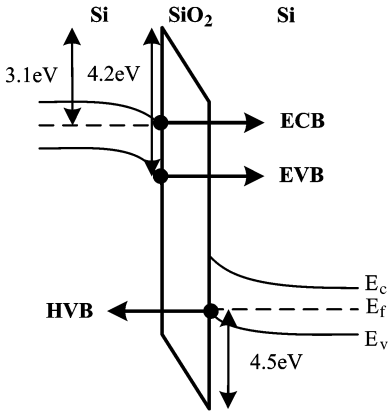

Fig. 1. Schematic representation of the direct tunneling components in a $\mathrm{Si/SiO_2/Si}$ structure [28].

Focusing on the direct tunneling current mechanism, there are three main leakage components in the structure [28], as shown in Fig. 1: (a) electron conduction-band tunneling (ECB), (b) electron valence-band tunneling (EVB), and (c) hole valence-band tunneling (HVB). Depending on the region of operation of the (nMOS or pMOS) transistor, each mechanism may have a different level of impact. In fact, for nMOS transistors in the OFF state or channel inversion, electrons tunneling from the conduction band (ECB) are the main contributors to the gate leakage [29]. On the contrary, holes tunneling from the valence band (HVB) mainly contribute to the gate leakage of pMOS transistors. Finally, electrons tunneling from the valence band (EVB) generate the substrate current in both nMOS and pMOS transistors. However, this contribution is at least one order of magnitude lower than that of the other two current components. Furthermore, in accordance with the difference in the barrier height between HVB and ECB, the gate leakage current in pMOS transistors can be between one and two orders of magnitude lower than the gate leakage current in nMOS transistors of the same size. For each of the three mechanisms, current density can be modeled by the expressions reported by Schuegraf and Hu in [30].

The flow path followed by the direct tunneling current must also be considered since it varies with the semiconductor structure beneath the oxide [29]. Fig. 2 illustrates the gate current components (I_g): I_{gb} is the gate-to-substrate leakage current, I_{gso} and I_{gdo} are leakage currents through the gate-to-source/drain extension overlap regions and I_{gc} is the gate-to-inverted channel tunneling current. Part of I_{gc} is subsequently collected by the source (I_{gcs}) whereas the rest goes to the drain (I_{gcd}).

III. Electrical Model of Interconnect Full Open Defects

This section analyses the behavior of interconnect full open defects. First, the classical approach to model opens in interconnect lines in old technologies, where gate leakage currents are negligible, is reviewed, and second the effect of gate leakage currents is considered for nanometer technologies.

It has been traditionally reported that a full open on an interconnect line generates a floating wire (see Fig. 3). The electrical behavior of the floating line is known to depend on several factors [12], namely (a) capacitances between the floating line and its neighboring lines (C_{Ni}) and semiconductor structures ($\mathrm{C_{WELL}}$ and $\mathrm{C_{SUBSTRATE}}$), (b) all parasitic capacitances created by the transistors driven by the floating line (an inverter in the example of Fig. 3) and (c) the charge trapped on the floating structure accumulated during the manufacturing process. Observe that the floating line voltage is pattern dependent since every pattern may set a different state at the neighboring nodes. For this reason, for a floating node (FN) coupled with N neighbors and the open located out of the influence of the first k neighbors, the floating node voltage can be predicted by knowing the state of the $N-k$ influencing neighboring signals and using the following expression:

$$V_{FN} = \frac{\sum_{i=k+1}^{N} C_{up\_i}}{\sum_{i=k+1}^{N} C_{up\_i} + \sum_{i=k+1}^{N} C_{down\_i}} V_{\mathrm{DD}} + V_{Qo} \quad (1)$$

where the first term is the capacitance divider created by all parasitic capacitances connected to the floating line, $\sum \mathrm{C_{up\_i}}$ denotes the total parasitic capacitance of neighboring structures set to $\mathrm{V_{DD}}$ and $\sum \mathrm{C_{down\_i}}$ stands for capacitances derived from neighboring structures set to ground. The second term, $\mathrm{V_{Qo}}$, represents the equivalent voltage added by the trapped charge.

According to (1) and given a test pattern, the state of the neighboring lines (together with the trapped charge) determines the voltage on the floating line, which remains constant until the next pattern is applied. However, for nanometer technologies,

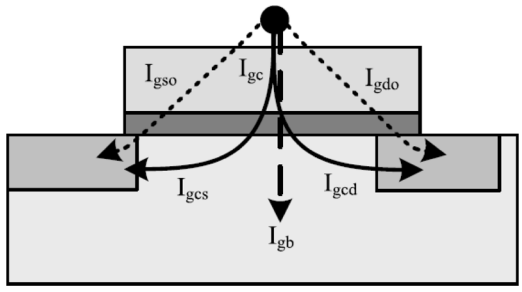

Fig. 2. Current components generated by direct tunneling based on the flow path [31].

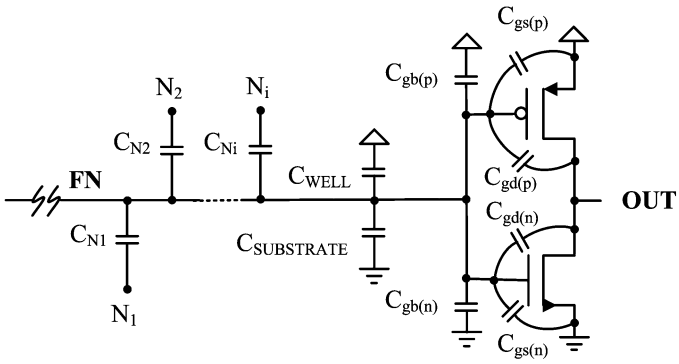

Fig. 3. Traditional electrical model of a full open defect affecting an interconnect line in a non-deep-submicron technology.

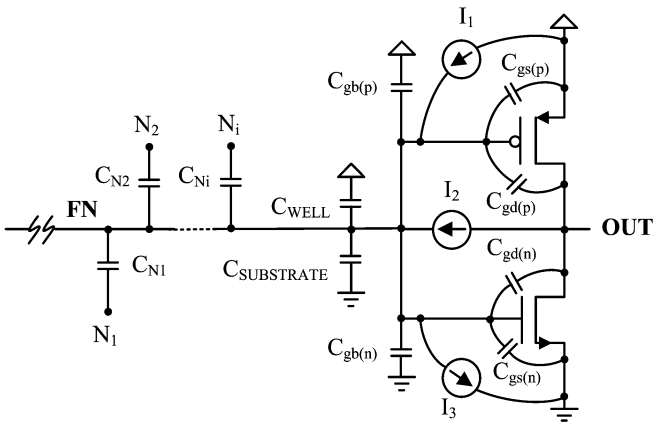

Fig. 4. Electrical model of an interconnect full open defect considering the gate leakage currents [32].

the floating line is not electrically isolated from the rest of the circuit due to non-negligible leakage currents flowing through the gate terminals of downstream transistors. Thus, the electrical model in Fig. 3 is not accurate enough. That is why a new electrical model including the effect of gate leakage currents is illustrated in Fig. 4.

As reported in Section II, gate leakage currents inject charge into/out of the floating node. Therefore, the influence of currents is included in the electrical model by incorporating current sources. For the example in Fig. 4, the effect of all the leakage components is summarized by three current sources (I_1, I_2 and I_3), which include the effect of different leakage current components. The notation has been defined in Section II (see Fig. 2):

$$I_1 = I_{gso(p)} + I_{gcs(p)} \tag{2}$$

$$I_2 = I_{gdo(p)} + I_{\mathrm{gcd}(p)} + I_{gdo(n)} + I_{\mathrm{gcd}(n)} \tag{3}$$

$$I_3 = I_{gso(n)} + I_{gcs(n)}. \tag{4}$$

Notice that as the gate-to-bulk leakage currents are much lower than the rest of components, for simplicity, the formers have been considered negligible in the electrical model depicted in Fig. 4.

IV. Defective Line Behavior

The behavior of a defective line including gate leakage currents is discussed in this section. First, its dynamic evolution is examined and second, the final steady state is predicted.

A. Dynamic Behavior Analysis

Based on the electrical model in Fig. 4, once a new test pattern is applied to the circuit, an initial voltage is induced in the defective line. However, this is not a quiescent state but the initial state of a transient evolution caused by the charge injection from or to the gate terminals of the transistors driven by the defective line. Hence, gate tunneling leakage currents cause the floating line to evolve from the initial state induced after the application of the test pattern. In order to illustrate the nature of this dynamic behavior, let us assume a floating line driving

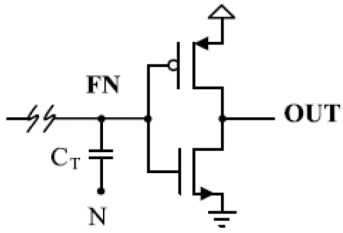

Fig. 5. Floating line driving a CMOS inverter.

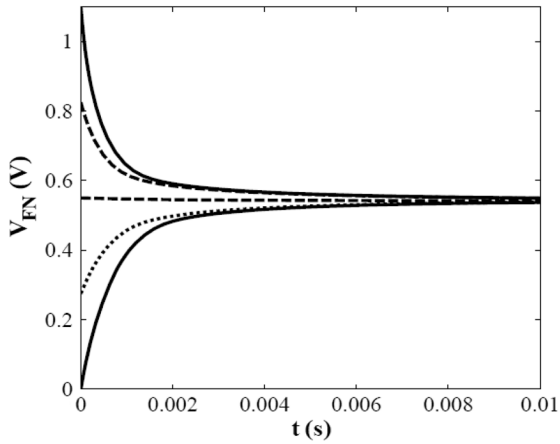

Fig. 6. Transient response of the floating line in Fig. 5 considering different initial states.

a low power inverter manufactured in a 65 nm STMicroelectronics technology, as shown in Fig. 5. Electrical simulations were carried out to observe the dynamic response of the defective line considering different initial states of the floating line. The results in Fig. 6 were obtained assuming a short line with a total neighboring parasitic capacitance ($\mathrm{C_T}$) of about 1 fF. The line voltage evolves for a few ms until reaching the steady state. It is remarkable that the steady state is the same for all cases regardless of the initial state of the line. However, the initial state does have an impact on the time required to reach the steady state. The further the initial state from the final steady state, the longer the time required to reach such a state.

The results in Fig. 6 were obtained for a short line, i.e., the open defect was assumed to be located at the far end of the interconnect line, next to the downstream (inverter) gate. The open location strongly influences the transient evolution although it does not affect the steady state voltage reached. Longer floating lines, i.e., open defects located close to the driver, generally result in higher total parasitic capacitances connected to them. Thus, their behavior shows longer transient evolutions. This is illustrated in Fig. 7 for different parasitic capacitances (line lengths) and assuming an initial zero voltage state in the floating line. In the case of $\mathrm{C_T}$ equal to 10 fF a few tenths of ms are required to reach the steady state. Nevertheless, if $\mathrm{C_T}$ equals 100 fF more than 200 ms are required to reach the steady state.

So far, the results assume that the neighboring lines related to the floating line are in a quiescent state and therefore do not affect the floating node. During the application of a logic test, a

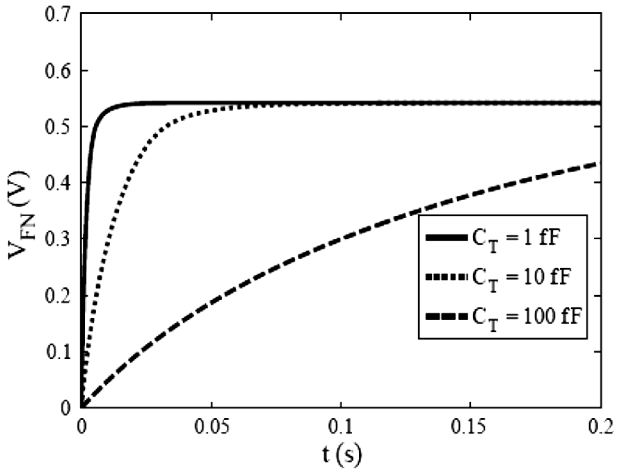

Fig. 7. Transient response of the floating line driving an inverter for different neighboring parasitic capacitances.

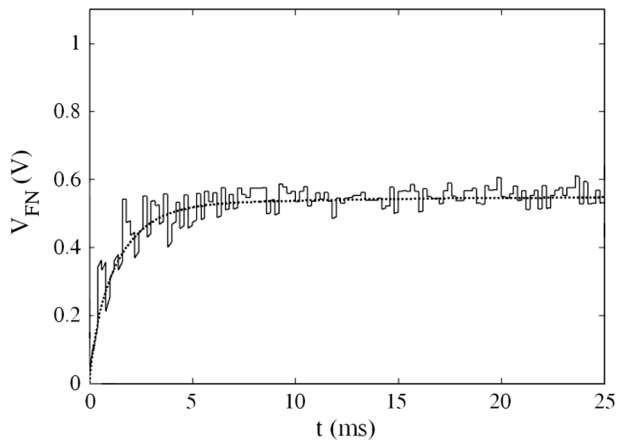

Fig. 8. Transient response of the floating line driving an inverter applying different test patterns (C_T = 1 fF).

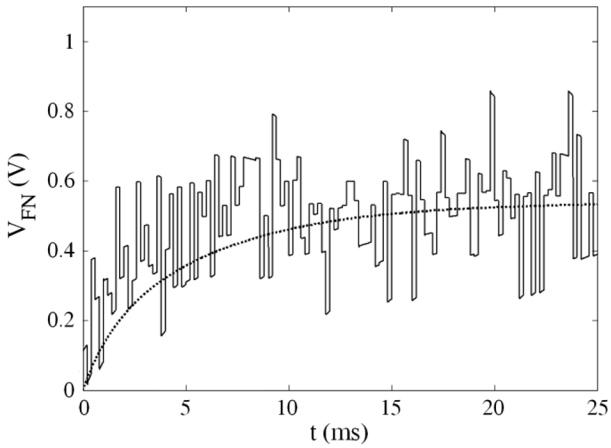

Fig. 9. Transient response of the floating line driving an inverter applying different test patterns (C_T = 10 fF).

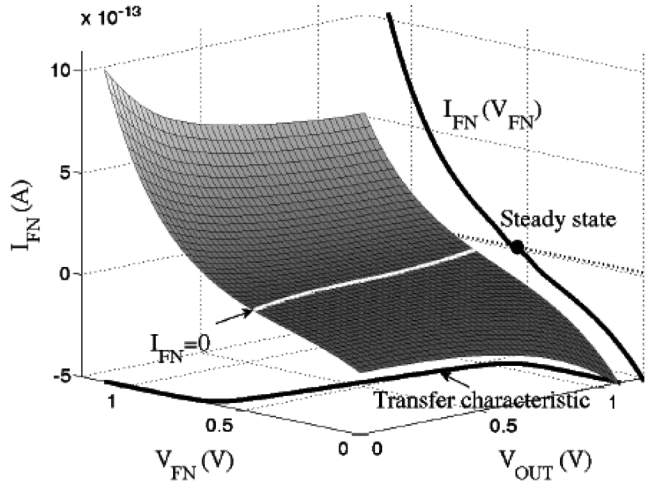

Fig. 10. Sum of all gate leakage components I_{FN} at the floating node driving an inverter of 65 nm STMicroelectronics.

pull-up or pull-down of the floating line may occur with every application of a new pattern due to the neighboring parasitic capacitances. The importance of this pull-up/down depends on the floating line topology. Simulation results showing this influence are presented in Figs. 8 and 9 for two total neighboring parasitic capacitances (C_T).

For a short line (Fig. 8), the neighboring parasitic capacitances do not have a strong influence and the floating line voltage is mainly determined by the gate leakage currents. On the other hand, for longer lines (Fig. 9), the pull-up or pull-down induced by the neighboring lines greatly affects the floating line behavior. However, during test application gate leakage currents also affect the floating line behavior. Based on the results in Fig. 9 it is derived that the application of the same pattern at the beginning or at the end of the test may lead to different logic interpretations of the floating line.

B. Steady State

The condition determining the final steady state is derived using Kirchoff's current law; that is, the sum of all gate leakage currents flowing into and out of the defective line must be null. Indeed, the simulation results in Fig. 6 reveal that the steady state of the floating line does not depend on its initial voltage. Based on the electrical model in Fig. 4 and assuming a floating line driving an inverter, the following relationship must be met:

$$I_{FN} = I_1 + I_2 - I_3 = 0. \tag{5}$$

From the current density expressions reported in [30], it is possible to predict each gate leakage component for every pair of voltage combination (V_{FN}, V_{OUT}) at the input and output of the driven gate. After the computation of these current components their sum (I_{FN}) can be rearranged as a three-dimensional plot [22], similarly to that depicted in Fig. 10 for the same inverter used in previous simulation results. The intersection between the 3-D surface and the plane $I_{FN} = 0$ yields the possible steady states of the floating line (white curve in Fig. 10).

The expression for predicting the gate leakage currents is derived assuming a defect-free downstream CMOS circuit since the open defect does not modify the physical structure of the transistors. Thereby, the defect-free static transfer characteristic is also valid to relate the input and output voltages of the inverter (bottom curve in Fig. 10). Hence, the intersection between the

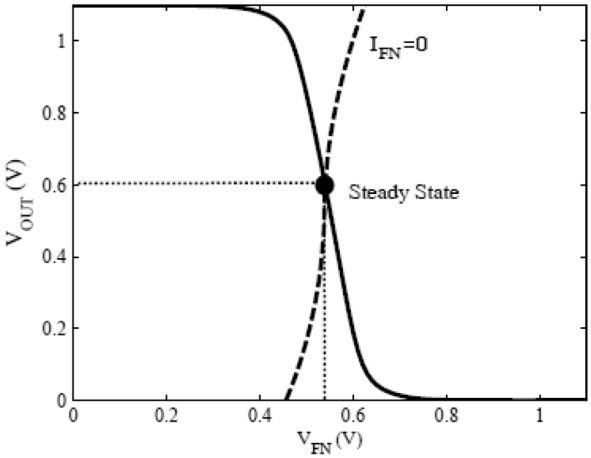

Fig. 11. Steady state of the floating node in Fig. 5.

$(V_{FN}, V_{\rm OUT})$ pairs resulting in $I_{FN} = 0$ and the transfer characteristic of the inverter determines the final steady state of the floating line, as shown in Fig. 11. For this particular case, an intermediate voltage (interpreted as a degraded logic 0) is obtained at the input of the inverter (floating line).

The methodology presented here can be used to predict the steady state voltage of a floating node caused by an interconnect open defect. However, note that it is not necessary to predict all gate leakage currents for every possible voltage combination between the input and the output of the affected gate. If the transfer characteristic of the inverter is previously considered, given an input voltage, the output is automatically determined. Therefore, only a subset of $(\mathrm{V_{FN}}, \mathrm{V_{OUT}})$ pairs must be considered. Using this simplifying information, the gate leakage current is illustrated in Fig. 10 as a function of the input voltage $\mathrm{I_{FN}(V_{FN})}$. Now, the input voltage where $\mathrm{I_{FN}(V_{FN})}$ is null results in the same steady state voltage prediction obtained in Fig. 11. From here on, this approach is used to find the steady state voltage.

V. Defective Floating Line With Fan-Out

In the previous analysis, the impact of gate tunneling currents has been considered when the floating line is driving a single gate. The proposed methodology is now generalized to the case of a floating line driving a set of downstream gates. For this purpose, and without loss of generality, let us assume a floating line driving both an inverter and a 2-input NAND gate, as illustrated in Fig. 12. The gate leakage currents coming from the two transistor pairs must be considered. In addition, depending on the test pattern applied, the NAND gate can be excited in two different ways derived from the logic state of input A. This influences the gate leakage current flowing into and out of the floating line. Indeed, if A is set to logic 0, the output of the NAND gate $(\mathrm{V_{OUT(ND)}})$ is set to $\mathrm{V_{DD}}$, whereas if A is set to logic 1, $\mathrm{V_{OUT(ND)}}$ depends on the floating line voltage. Therefore, two different steady states are induced to the floating line due to the impact of the gate leakage currents depending on the logic state of A.

In order to predict the steady state of the floating line, a methodology similar to that in the previous section is applied

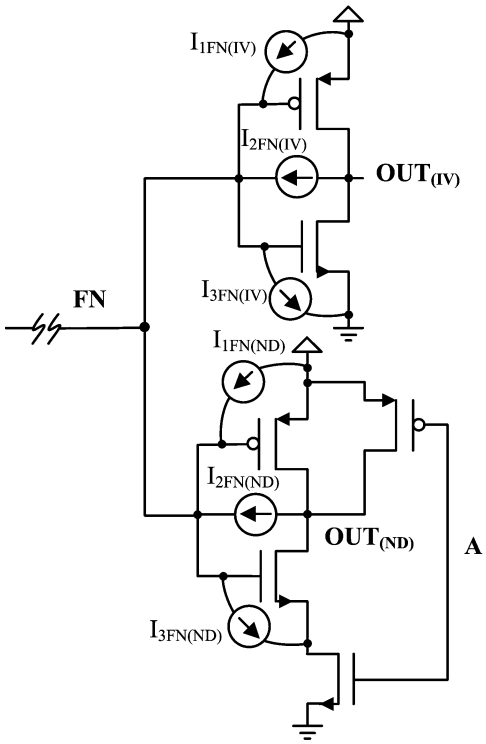

Fig. 12. Floating line driving an inverter and a 2-input NAND gate.

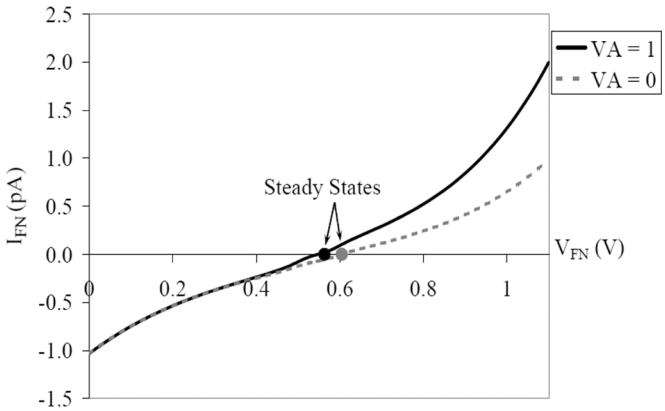

Fig. 13. Sum of all gate leakage components $\mathrm{I_{IN}}$ versus the floating line voltage at the defective node FN for both NAND states.

(see Fig. 10). The information about the transfer characteristic is used to avoid a four dimensional plot for the present case. Indeed, given $\mathrm{V_A}$, both output voltages ($\mathrm{V_{OUT(IV)}}$ and $\mathrm{V_{OUT(ND)}}$) are determined and $\mathrm{I_{FN}}$ is predicted as a function of $\mathrm{V_{FN}}$ (i.e. $\mathrm{I_{FN}(V_{FN})}$) like in the process of Fig. 10. The results for the two possible states of the NAND gate are shown in Fig. 13.

The steady state of FN ($\mathrm{I_{FN}} = 0$ condition) varies with the excitation of the NAND gate. A difference of about 50 mV is detected in the steady state of the illustrative example, which may affect the logic interpretation of the floating line voltage. Although it is always interpreted as a (degraded) logic 0, if A is set to logic 0, the steady state voltage is pushed to the uncertainty region of the transfer function of the inverter (the NAND gate responds with a $\mathrm{V_{OUT(ND)}} = 1$ to $\mathrm{V_A} = 0$).

In general, a floating line with fan-out may have as many steady states as different excitations of the downstream gates. These excitations induce different steady states, leading to different interpretations of the defective line voltage depending on the test pattern applied.

VI. Test Implications

The impact of gate leakage currents on the behavior of CMOS circuits with interconnect full open defects results in new test implications so far not considered. Traditionally, interconnect full open defects have been tested by applying stuck-at (SA) patterns that drive the coupled neighboring lines to logic (0 or 1) voltages. Improvements in the detectability of such defects consist of applying logic test patterns for a SA1 (SA0) at the target node, requiring the neighboring lines to generate the maximum (minimum) pull-up (down) coupling capacitance to the target node. However, for nanometer technologies, this testing strategy ensures the optimum test state and detectability condition only after application of the test pattern. Subsequently, the gate leakage currents generate a dynamic behavior of the floating net, as described in Section IV-A. This transient behavior is not noticeable for two successive test vectors. Nonetheless, a test usually comprises a high number of test patterns. The total test time can be thus of the same order of magnitude (or higher) as that of the transient behavior induced by the gate leakage currents. Therefore, the influence of gate leakage currents should be taken into consideration throughout the test.

The test implications due to the influence of gate leakage currents depend on the floating line topology. Three situations of the open give rise to the following types of floating lines: a) short lines, b) long lines and c) intermediate length lines. The corresponding test implications are described in the next subsections.

A. Short Lines

When the floating line is short, the gate leakage currents dominate its behavior (see Fig. 8). The transient behavior generated by the gate leakage currents may increase or reduce the faulty net voltage according to the relationship between the initial state and the steady state. During test application, for every test pattern, the floating line voltage is pulled-up/down due to effect of the neighboring parasitic capacitances. However, this voltage change is not considerable since the line is short and the coupling capacitances are small.

In order to classify the possible detectability scenarios and without loss of generality, let us assume that the test comprises a set of patterns, only one of which $(\mathrm{P_1})$ detects a SA1 in the defective line. Four different detectability conditions are possible for a short floating line in a 65 nm technology, as reported in Fig. 14(a)–(d) by representative simulations results. Assume observability of the logic states of the downstream gate at some primary outputs of the IC:

a) In the initial state, the floating line is interpreted as a logic 1, but the gate leakage currents generate a transient evolution, causing the voltage to be interpreted as a logic 0 in the steady state. Then, the target node voltage decreases until reaching the $\mathrm{V_{LTH}}$ of the downstream gate $(\mathrm{t_1})$. From this point, the defect detectability can no longer be guaranteed. Thus, the defect is observable as long as pattern $\mathrm{P_1}$ is applied before $\mathrm{t_1}$.
b) Both in the initial state and in the steady state the floating line voltage is interpreted as a logic 0. At no time is $\mathrm{P_1}$ suitable to detect the open defect.
c) Both in the initial and in the steady state the floating line voltage is interpreted as a logic 1. The defect is always detectable by $\mathrm{P_1}$, irrespective of the instant at which the pattern is applied.
d) In the initial state, the floating line voltage is interpreted as a logic 0. However, the gate leakage currents generate a transient evolution in such a way that the voltage is interpreted as a logic 1 in the steady state. If $\mathrm{P_1}$ is applied before the target node voltage increases and reaches $\mathrm{V_{LTH}}$, $(\mathrm{t_2})$, the open is not detected, whereas if $\mathrm{P_1}$ is applied after $\mathrm{t_2}$, the defect is detected.

The four possible test scenarios and the detectability intervals are summarized in Table I. Equivalent results are derived for a single pattern detecting a SA0 in the defective net.

When applying a SA test, both SA faults (SA1 and SA0) are usually detected by at least one test pattern. In such situations, open detectability depends on the transient evolutions illustrated in Fig. 14. For instance, for the cases in Figs. 14(b) and 14(c), the open is detected as one of the SA patterns generates a failure. However, the cases in Figs. 14(a) and 14(d) should be carefully considered, since the application of the SA patterns throughout the test determines whether one, both or neither of the SA patterns generates a failure in the presence of a full open. For instance, assume that the floating line has a similar behavior to that in Fig. 14(a). If the pattern detecting a SA1 is applied before $\mathrm{t_1}$ and the pattern detecting a SA0 is applied after $\mathrm{t_1}$, both patterns detect the open. In contrast, if the pattern detecting a SA0 is applied before $\mathrm{t_1}$ and the pattern detecting a SA1 is applied after $\mathrm{t_1}$, then the open escapes the test.

From these results, it can be concluded that the best test scenario to detect an open defect generating a short floating line is when a SA like behavior is induced in the floating line (Figs. 14(b) and 14(c)). In such situations the open is detected with a SA test. In cases where no SA like behavior is reported, the steady state prediction may be useful in detecting the open. A transition fault test [33] like the one applied for resistive defects is also helpful in this case since no transition is propagated through the defective line.

B. Long Lines

For long lines, the corresponding total parasitic capacitance is high and the gate leakage currents require more time to generate transient behavior. In such situations, if the total test time is much shorter than the time required by the gate leakage currents to influence the floating line, the effect of the currents is negligible and the classical approach can be used to predict the floating node voltage (1). Fig. 15 is a representative example of this case, corresponding to the simulation results for a long floating line in a 65 nm technology. Note how a pull-up/down of the floating line occurs with every application of a new pattern. The influence of the gate leakage currents is, in this case, negligible.

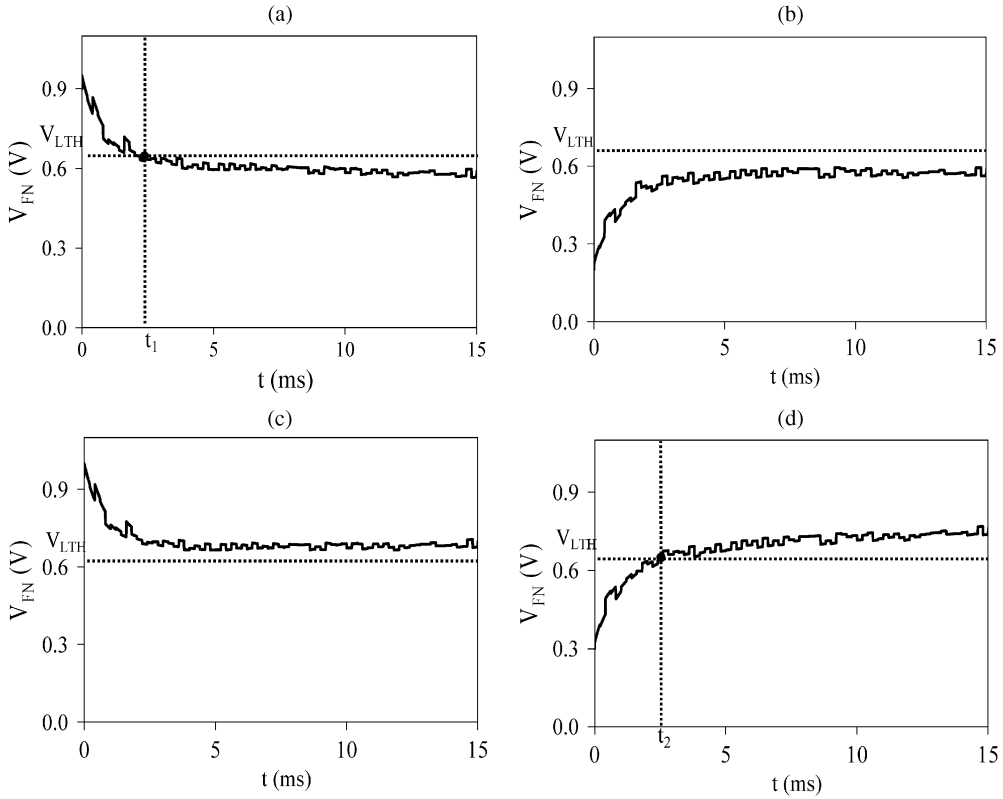

Fig. 14. Detectability interval of a short floating line for a SA1 pattern exciting the open during the application of a whole test depending on the initial state (IS) and the steady state (SS): (a) $(\mathrm{IS},\mathrm{SS}) = (1,0)$, (b) $(\mathrm{IS},\mathrm{SS}) = (0,0)$, (c) $(\mathrm{IS},\mathrm{SS}) = (1,1)$, and (d) $(\mathrm{IS},\mathrm{SS}) = (0,1)$.

TABLE I
OPEN DETECTABILITY FOR A SINGLE PATTERN DETECTING A SA1 IN THE DEFECTIVE LINE

Initial State	Steady State	Detectability interval
0	0	--
0	1	$[t_2,+\infty]$
1	0	$[0,t_1]$
1	1	$[0,+\infty]$

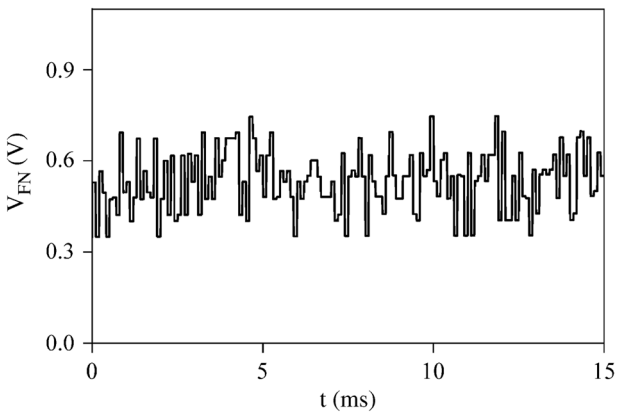

Fig. 15. Long floating line behavior dominated by the neighboring parasitic capacitances.

Like in older technologies, open detectability depends mainly on the neighboring parasitic capacitances.

C. Intermediate Length Lines

The two previous sub-sections consider the cases where one of the factors, either, leakage gate currents or coupling neighboring capacitances, dominates the floating line behavior. Nevertheless, sometimes neither the gate leakage currents nor the parasitic capacitances strongly dominate it. In these situations, both factors are important and should be considered for detecting opens. An illustrative example of this situation is given in Fig. 9. The exact behavior and detectability implications depend on the floating line topology.

VII. EXPERIMENTAL RESULTS

This section presents results for real silicon to experimentally corroborate the impact of gate leakage currents in the presence of interconnect full open defects. These results were obtained for devices manufactured in a 65 nm technology although a device designed in a 180 nm technology was used to illustrate transient behavior.

A. 65 nm Technology Device

An experimental design (see Fig. 16) was built in the 65 nm CMOS065-SOI technology from STMicroelectronics, the experiments were carried out using a power supply voltage of 1.1 V. The circuit comprises a set of interconnect full open defects which were intentionally injected at certain specific locations. The floating lines generated by such defects drive downstream inverters from the low power standard cells library provided by the technology. These interconnect lines are 50 or 100 μm in length and are cross-coupled to a set of neighboring lines. Full controllability and observability of the design are achieved,

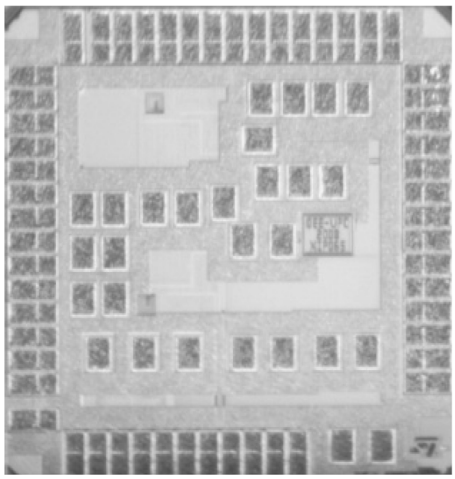

Fig. 16. Photograph of the design fabricated in a 65 nm technology.

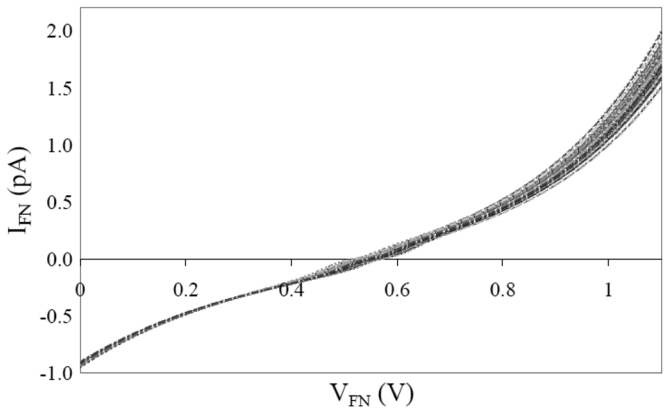

Fig. 17. Monte Carlo simulations for the gate leakage current flowing through the floating node $(\mathrm{I_{FN}})$. The steady state voltage is obtained when $\mathrm{I_{FN}}$ is equal to 0.

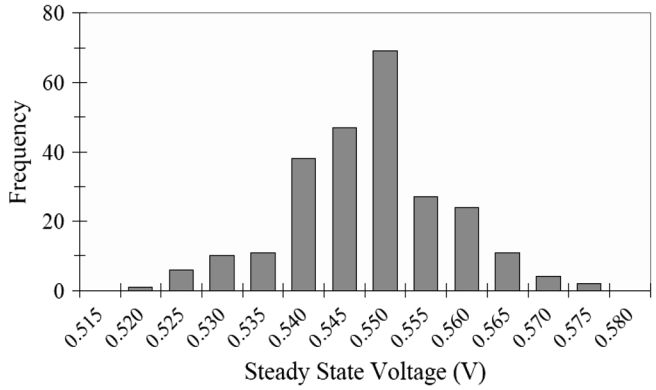

Fig. 18. Monte Carlo simulations for the steady state voltage of the floating line (always interpreted as a logic 0).

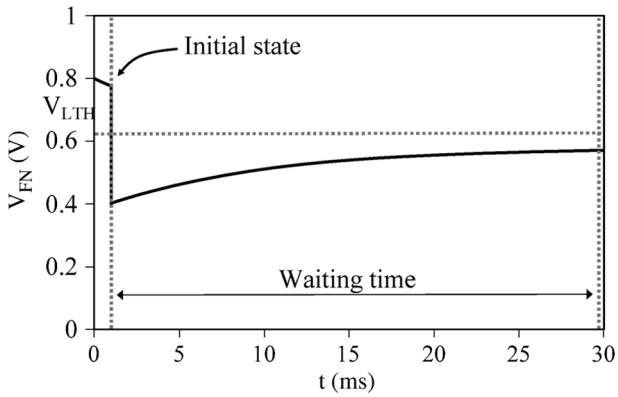

Fig. 19. Timing condition for the experiments to measure the steady state of the floating lines.

i.e., the logic interpretations of floating lines are observable and every neighboring line is controllable.

Prior to the experimental characterization of the defective devices, process variability was evaluated to characterize its impact on the logic behavior of downstream gates (inverters in this case). Under nominal conditions, electrical simulations predict the behavior of floating lines driving single inverters interpreted as logic 0 although the resulting steady state voltage is an intermediate value. Monte Carlo simulations were also performed to observe the variability of the steady state voltage with process variations. The simulation results of the total gate leakage current flowing through the floating node $(\mathrm{I_{FN}})$ related to the floating node voltage are illustrated in Fig. 17. The steady state voltages correspond to the floating node voltage where $\mathrm{I_{FN}}$ is equal to 0. Fig. 18 shows the histogram of the results for the steady state voltage. It is remarkable that variability induces a few tenths of mV around half the power supply value. However, the transfer function of the inverter causes the steady state voltage to be always interpreted as a logic 0.

Experiments were performed on a 50 and a 100 μm floating line to corroborate the steady state results obtained from electrical simulations. A test pattern was applied to generate a neighborhood state for the two lines. Subsequently, without modifying the excitation of the circuit and after a sufficient delay (tens of ms) to ensure that the floating lines had reached their corresponding steady state, the response of the downstream gates was measured. An example of the expected evolution of a floating line is given in Fig. 19. The same experiment was conducted considering different initial excitations of the neighborhood. Both floating lines were always interpreted as logics 0, corroborating the results obtained through simulation.

In the second part of the experimental work, the transient behavior of the floating lines was forced by adding a second test pattern at a certain time after the floating lines have reached the steady state (Fig. 20). As the logic interpretation of the steady state voltage of the floating nodes was always a logic 0, different initial voltages (all interpreted as a logic 1) were generated at the defective nodes by the second test pattern to measure the time (δ) required by the floating nodes to be interpreted again as a logic 0. An initial pattern was applied to the circuit to generate an initial excitation on the neighboring lines. Subsequently, delay time was allowed for the floating nodes to reach the corresponding steady states. The second pattern was then applied to set all neighboring lines to 1 (all-1 pattern), generating a pull-up on the floating lines. The magnitude of the pull-up depends on the difference between the initial pattern and the all-1 pattern. The greater the difference, the higher the magnitude.

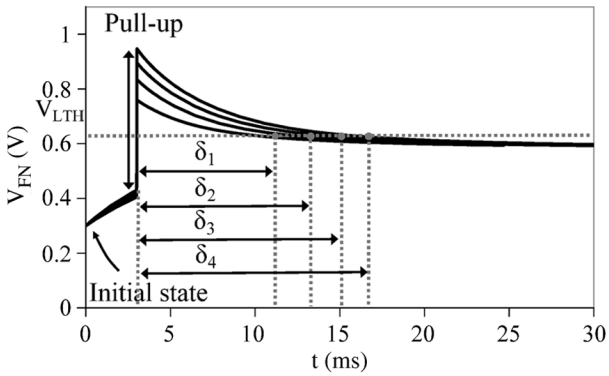

Fig. 20. Timing condition for the experiments to measure the transient behavior of the floating lines.

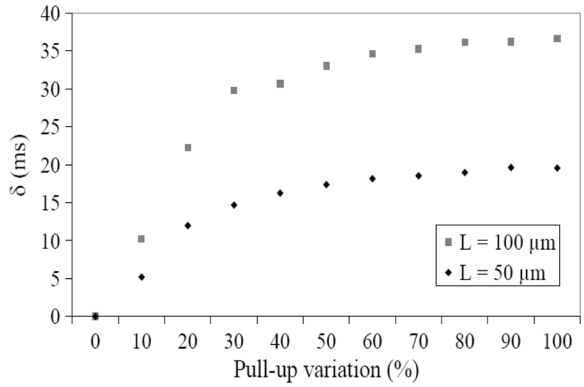

Fig. 21. Transient behavior results for the floating lines.

The experimental results are illustrated in Fig. 21. The x axis represents the pull-up variation, which is the percentage of parasitic neighboring capacitances changing from 0 to 1 between the initial pattern and the all-1 pattern. The delay δ (time between the application of the all-1 pattern and the interpretation of a logic 0 at the floating node) increases with pull-up variation. This is consistent since with greater pull-up variations the initial floating node voltage is further away from the steady state voltage. Note that this behavior was already observed in the simulations of Fig. 6.

The relationship between the duration of the transient behavior and the capacitance involved in the evolution is shown in Fig. 21, where delays corresponding to the 100 μm floating line are larger than those of the 50 μm floating line. Furthermore, both sets of measurements are in good agreement with the corresponding results obtained from the electrical simulation of the circuit. Finally, it is worth mentioning that for null pull-up variation (the initial and the final pattern are the all-1 pattern) the delay is 0 and the floating node voltage is not modified. Thus, this voltage is already the steady state voltage, which is always interpreted as a logic 0.

B. 180 nm Technology Device

The impact of gate leakage currents has already been observed in older technologies. An example in this sub-section illustrates the time evolution of defective transient behavior. The results refer to an industrial test chip design (VECTOR4) manufactured in a 180 nm technology from NXP Semiconductors.

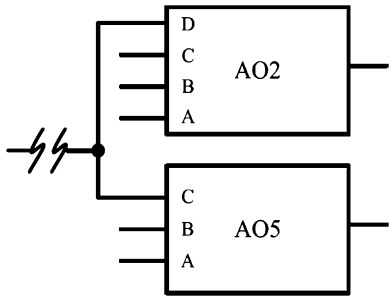

Fig. 22. Full open defect diagnosed in an industrial test CMOS circuit.

The pass/fail information obtained on the tester for such devices was logged for a set of different test patterns. Subsequently, an in-house diagnosis tool was used and it was concluded that this device might contain an interconnect full open defect. In order to analyze the effect of gate leakage currents, an electrical analysis was performed, as shown next.

Based on the information obtained with the diagnosis tool, a fault related to the output net of an inverter which, in turn, drove two instances (see Fig. 22) was reported as the most likely scenario. With this behavior, the suspicious net failed in both directions, i.e., it sometimes failed as a logic 0 and sometimes as a logic 1. In addition, the device also showed a transient behavior. After a few seconds, the logic behavior was different. In this case, it was observed that the same suspicious net behaved as a SA0.

The floating node voltage is not accessible. However, this 180 nm technology still allows useful information related to the floating node behavior to be extracted by monitoring the current consumption of the device. The results for three different test patterns activating the defect are given in Fig. 23. Pattern 15 activates the path through gate AO5. The path through gate AO2 is activated by pattern 3, and both paths are activated by pattern 19. For patterns 3 and 15, current consumption increases until reaching its maximum and then decreases. Two current peaks corresponding to the two activated paths are observed for pattern 19. For every excitation, the corresponding steady state is reached after a few seconds of transient behavior, resulting in a higher current consumption than expected for the defect free device. Furthermore, in the steady state the suspicious net voltage is interpreted as a logic 0 for the three patterns.

The prediction of the steady state voltage for the three possible configurations of the downstream gates is illustrated in Fig. 24. The voltage is always interpreted as a (degraded) logic 0 although every configuration determines a different steady state voltage. Nevertheless, the difference amounts to just a few tenths of mV. This prediction corroborates the experimental logic behavior obtained on the tester.

As the steady state voltage predicted is a degraded 0, extra current is consumed. Simulations were performed to predict the current consumption of the downstream gates in the steady state. The results can be seen in Fig. 25, where current consumption is related to the floating node voltage. Assuming nominal parameters, gate AO2 is able to generate around 40 μA whereas gate AO5 can only generate 35 μA. These currents are slightly lower than those experimentally measured. Nevertheless, a process

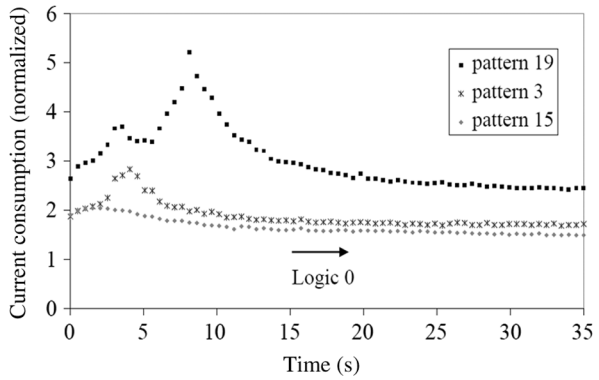

Fig. 23. Measured current consumption of the defective circuit depending on the input vector applied [32].

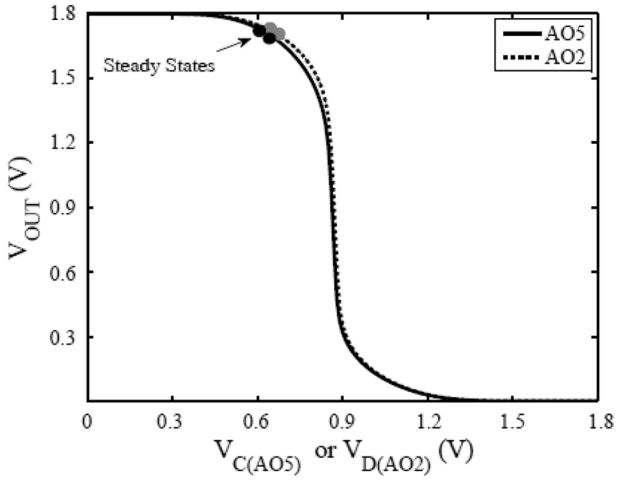

Fig. 24. Final steady state predicted for the floating node of the defective circuit in Fig. 22.

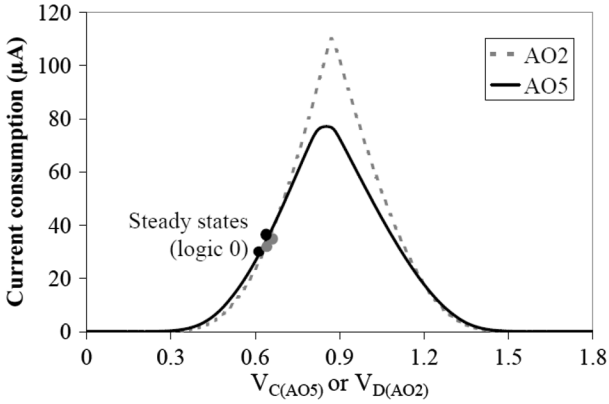

Fig. 25. Current consumption vs V_{IN} simulation relationship of the downstream gates of the defective device.

TABLE II
LOW POWER TECHNOLOGY

Technology node *(nm)*	*L = 1 μm* *δ (μs)*	*L = 10 μm* *δ (μs)*	*L = 100 μm* *δ (ms)*	*L = 1 mm* *δ (ms)*
45	*252*	*861*	*7.023*	*68.42*
32	*77*	*340*	*3.011*	*29.52*
22	*17*	*96*	*0.943*	*9.33*

TABLE III
HIGH PERFORMANCE TECHNOLOGY

Technology node *(nm)*	*L = 1 μm* *δ (μs)*	*L = 10 μm* *δ (μs)*	*L = 100 μm* *δ (ms)*	*L = 1 mm* *δ (ms)*
45	*14*	*33*	*0.23*	*2.21*
32	*18*	*69*	*0.60*	*5.92*
22	*17*	*89*	*0.82*	*8.14*

variation causing a steady state voltage a few tenths of mV higher than the nominal one should give similar current consumption values to those measured by the tester (see Fig. 23 for experimental evidence). Assuming nominal parameters in the SPICE simulation (Fig. 25), the current peaks of the two gates are approximately obtained for the same input voltage. However, the current behavior over time of pattern 19 shows that the two current peaks do not completely overlap, as expected from simulation. As the voltage of the floating net evolves, the corresponding current peaks are reached at different times, and therefore at two voltages of the defective line further away than expected from simulation results.

VIII. FUTURE TRENDS

The technology node has a strong influence on the impact of gate leakage currents in the presence of interconnect open defects. The obtained experimental results show that, for a 180 nm technology, transient evolutions due to the impact of gate leakage currents were in the order of seconds. Nevertheless, for a 65 nm low power technology transient behaviors decrease some orders of magnitude to a few ms. In 180 nm technologies, these transient evolutions are too slow to influence the defective behavior of the device during test. In 65 nm technologies they are still too slow to have an impact on the behavior of the floating line during a test cycle. However, if the test is long, the evolutions might be in the same order of magnitude or even lower than the total test time, thus affecting the defective behavior of the circuit.

It is important to predict the scaling of transient evolutions with future technologies. SPICE simulations based on PTM (Predictive Technology Model) were carried out to measure transient evolutions for different technology nodes. Tables II and III summarize the results obtained for low power and high performance technologies, respectively. All of them incorporate high k dielectric. The measures refer to the time required by the floating node to reach the steady state (δ) assuming a zero volts as initial state of the floating node. The downstream gate was an inverter of minimum feature size. Different floating line lengths were taken into consideration.

For low power technologies, transient evolutions decrease for every technology node. For a 22 nm technology, δ values range from a few μs up to a few ms depending on the line length. However, no such distinct trend exists for high performance technologies. Transient evolutions remain in the same order of magnitude and even increase for far future technologies. In the near future, transient evolutions in high performance technologies are shorter than those corresponding to low power technologies. Nonetheless, with every technology node, the gap between them

decreases in such a way that, for a 22 nm technology, times are quite similar.

Two main factors influence the scalability of leakage currents, i.e., gate oxide thickness and power supply voltage. The smaller the oxide thickness, the higher the gate leakage. On the contrary, the lower the power supply voltage, the lower the gate leakage. The trend in Tables II and III can be explained by the difference in parameter scalability between low power and high performance technologies. In low power technologies, oxide thickness is still reduced appreciably with every technology node. Therefore, although power supply voltage is also decreased, oxide thickness is the dominant factor. However, in high performance technologies, predictions are that oxide thickness is slightly reduced with every technology node. Thus, in such cases the reduction in power supply voltage also affects the scalability of gate leakage currents. Simulation results generally show that transient evolution times for open interconnects are reduced in future technologies. Hence, the impact of gate leakage currents on interconnect full open defects increases with every new technology. These transient evolutions times are small enough compared to a typical total test application time, which may influence the failing behavior of defectives devices with interconnect full open defects.

IX. Conclusions

Full open defects in interconnect lines of nanometer CMOS circuits have been analyzed. The floating line voltage generated by the full open depends on its topological characteristics, namely parasitic capacitances to neighboring structures, transistor capacitances of the downstream gate(s) and trapped charge. Furthermore, due to the reduction in oxide thickness in nanometer CMOS technologies, gate tunneling leakage also affects the behavior of circuits with full open defects. Floating lines cannot be considered electrically isolated and are subjected to transient evolutions until reaching a steady state determined by the technology and downstream gate(s). Theoretical analysis as well as experimental evidence of this behavior are presented for real devices belonging to 65 nm and 180 nm CMOS technologies. Trends show reductions down to a few μs in transient evolutions of floating lines for future technologies, which are on the order of typical total test times. The transient behavior generated by gate leakage currents is not noticeable for two successive test vectors. However, a test comprises a high number of patterns which means that the total test time can be of the same order of magnitude as that of the transient behavior induced by the gate leakage currents. Therefore, the exact influence of gate leakage currents strongly depends on the floating line topology.

If the line is short, the leakage current is the dominant factor. Applying a set of patterns where only one of which excites the open, depending on the relationship between the initial and the final steady states, four different behaviors are possible. First, if the initial and the final steady states set the floating line voltage to the value opposite to that of the defect-free case, the defect is always observable. Second, if the initial and the final steady states set the floating line voltage to the defect-free value, the open defect is not observable. Third, if the floating line voltage is set to the defect-free value in the initial state and to the opposite value in the steady state, the defect is not observable until the transient evolution changes the logic interpretation of the floating line voltage. Finally, if the initial state sets the floating line voltage to the value opposite to that of the defect-free case, and the steady state sets the voltage to the same value as that of the defect-free case, the open is observable until the point where the transient evolution changes the logic interpretation of the floating voltage.

When the line is long, the gate leakage currents do not influence the defective line, which is mainly determined by the neighboring parasitic capacitances, like in older technologies.

For intermediate length lines, both factors (gate leakage currents and neighboring parasitic capacitances) are important and should be considered for detecting opens. The exact behavior and detectability implications depend on the floating line topology.

Thus, these behaviors derive important test implications for the detectability conditions of interconnect full open defects in nanometer technologies.

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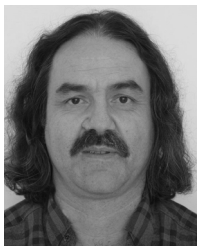

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