Electromagnetic Compatibility of CMOS circuits along the lifetime

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Abstract: The continuous scaling of CMOS circuits has set the MOSFET transistor in the nanoelectronic era. In this context, the functionality and complexity of integrated circuits (ICs) are growing up. However, the operation voltage has been continuously reduced. The higher complexity of ICs has allowed including electronic systems in a lot of safety critical applications (*i.e.*, automotive, aeronautics and/or medical applications). Therefore, the functionality of these electronic equipments must be assured and the risk of electromagnetic interference (EMI) must be reduced during their lifetime. Nowadays, circuits' robustness to electromagnetic interference is checked in a burn-in component, without taking into account the impact of the natural devices' aging. However, shrunk dimensions imply the appearance of several wear out mechanisms, which can limit the functionality of the circuits and modify their electromagnetic performance. Therefore, the time dependence of electromagnetic behaviour, which is known as Electromagnetic Robustness or Electromagnetic Reliability (EMR), should be evaluated. The switching noise is probably one of the main EMC emission problems in CMOS circuits. It is know that wear out mechanism affects the switching behaviour of CMOS circuits. Therefore, some effects on EMC performance of these circuits should be expected. In this work, the switching noise behaviour or CMOS circuits under one of the most important reliability problems are analysed by means of electrical simulation. In order to do that, a characterization of wear out mechanism on single MOSFET is presented and modelled. The results show a reduction on the frequency switching noise emission in circuits subjected to wear out, due to the reduction of the drain current of MOSFET.

1. Introduction

The continuous scaling of CMOS circuits has set the MOSFET transistor in the nanoelectronic era. In this context, the functionality and complexity of integrated circuits (IC) are growing up. However, the operation voltage has been continuously reduced. The higher complexity of IC has allowed including electronic system in a lot of safety critical applications (i.e., automotive, aeronautics and/or medical application). Therefore, the functionality of these electronics equipment must be assured and the risk of electromagnetic interferences must be reduced during their lifetime.

Nowadays, circuits' robustness to electromagnetic interferences (EMI) is checked in a burn-in component [1], without taking into account the impact of the natural devices' aging. However, shrunk dimensions cause the appearance of several time dependent failure mechanisms, which can limit the functionality of the circuits and modify their electromagnetic behaviour [2]. Therefore, the time dependence of electromagnetic behaviour, which is known as Electromagnetic Robustness or Electromagnetic Reliability (EMR), should be evaluated. In this paper, for the first time, the impact of one of the main time dependent reliability problem, the negative bias temperature instability (NBTI) on the switching noise emission has been analysed.

It is mainly accepted that NBTI is ascribed to the formation of Si/SiO2 interface states and the oxide positive charge [3]. Regarding to this problem, the dominating work has been concentrated on discrete transistor parameter shift, rather than on circuit performance. At device level, it has been demonstrated that NBTI effect on pFET is manifested as a gradually increment of the threshold voltage (V_{th}). Therefore, the drive current is reduced [4]. The NBTI under static and dynamic conditions has also been reported. These investigations show that the voltage threshold shift (ΔV_{th}) under dynamic stress is almost half of DC case, due to the recovery properties of NBTI [5]. At circuit level, the NBTI effects have not been deeply investigated. However, some works have pointed out that NBTI provoke a signal noise margin (SNM)

reduction on SRAM cell [2]. According to the authors' knowledge there is not any work focused on the effects of NBTI in the EMC behaviour. In this paper, the impact of NBTI on the overall behaviour and the switching noise emissions of CMOS ring oscillator have been evaluated.

This paper is structured as follows: in Section II the impact of NBTI on single pFET is obtained experimentally and the voltage threshold shift is experimentally quantified. In Section III, the impact of NBTI on oscillation frequency and switching noise of a 41 stages ring oscillator has been evaluated through simulation, using the data measured on Section II. In Section IV, the conclusions are summarized.

2. Measuring the impact of NBTI

This investigation has started by measuring the voltage threshold shift (ΔV_{th}) due to NBTI on a single pFET. In order to do that, a stress-measure-stress sequence has been followed in the experiment, with exponentially increasing periods of time. During the measurement phase, the I_D-V_G pFET characteristic has been measured. During the NBTI stress phase, a constant voltage of 0V has been applied to the pFET gate and the rest of the terminals have been biased at 2V. In order to accelerate the NBTI effects the experiments have been done at 125ºC. In Fig. 1 the I_D-V_G pFET behaviours at different stress time are plotted, As it is shown, a voltage threshold shift is produced in the transistor due to NBTI, the ΔV_{th} time dependence shows a power law dependence, depicted in Fig. 2, which matches with the theoretical prediction [2].

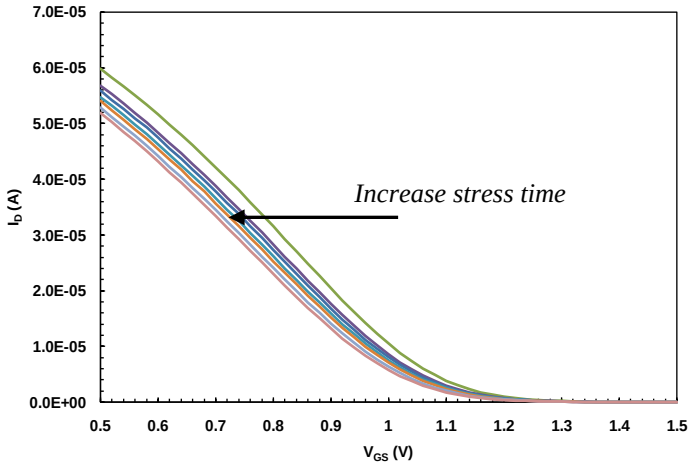


Fig.1 *I_D-V_G behavior of pFET for different stress time.*

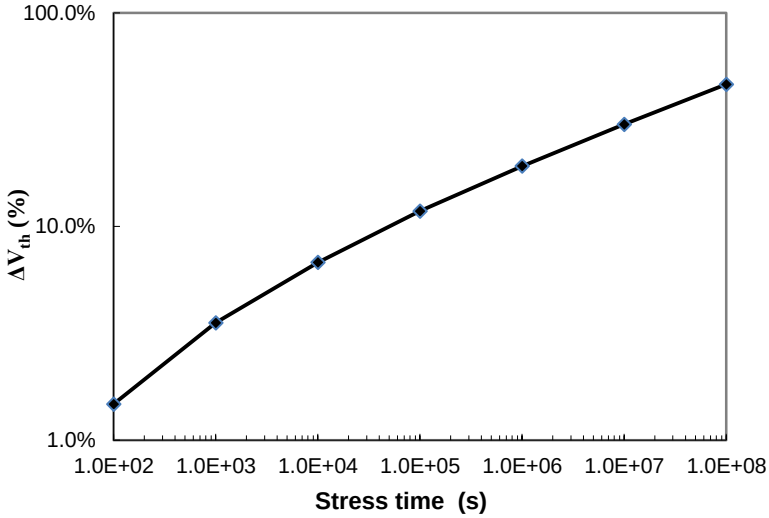


Fig. 2: *ΔV_{th} of single pFET against NBTI stress time.*

3. EMC Behaviour under NBTI

The switching noise is probably one of the main EMC emission problems in CMOS circuits. It is well known that switching noise is a common impedance coupling [6]. In order to reduce it, several strategies can be followed, such as reducing the common impedance and/or including intra or extra-chip decoupling capacitance. In the previous paragraph it has been shown that NBTI affects the I_D-V_G behaviour of the pFET. Therefore, some effect on switching noise behaviour should be expected. In order to analyse the impact of NBTI on switching noise, a CMOS ring oscillator has been simulated with commercial *Agilent ADS* software. The BSIM4 model extracted from PTM website [7] has been used and the voltage threshold shift of the pFET has been shifted following the time dependence response obtained experimentally in Fig.2. In Fig.3 the schematic of the internal oscillator under investigation is shown. The oscillator is based on 40 inverters plus 2 input NAND gate (the NAND gate is included as enable). The aspect ratios for the CMOS inverters are 1.0µm/90nm and 3µ/90nm for nFET and pFET, respectively.

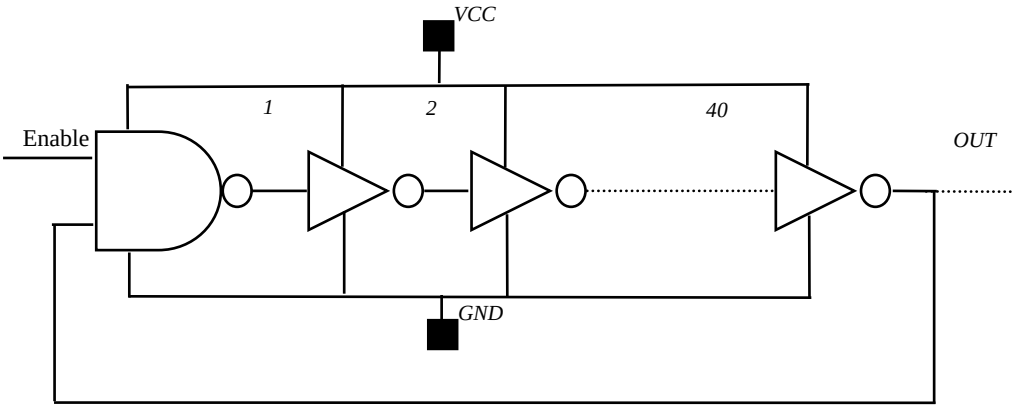
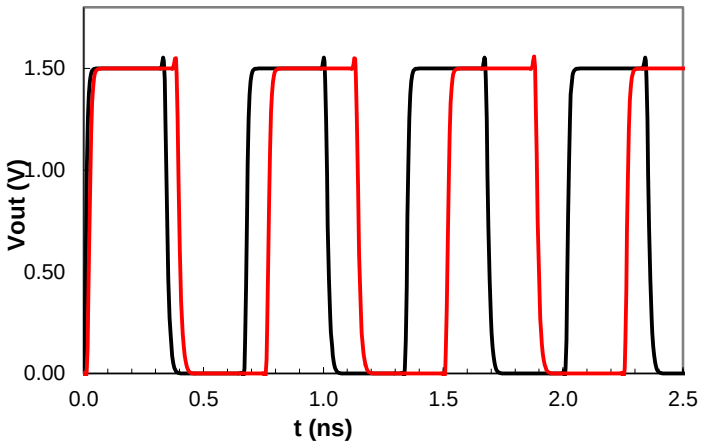
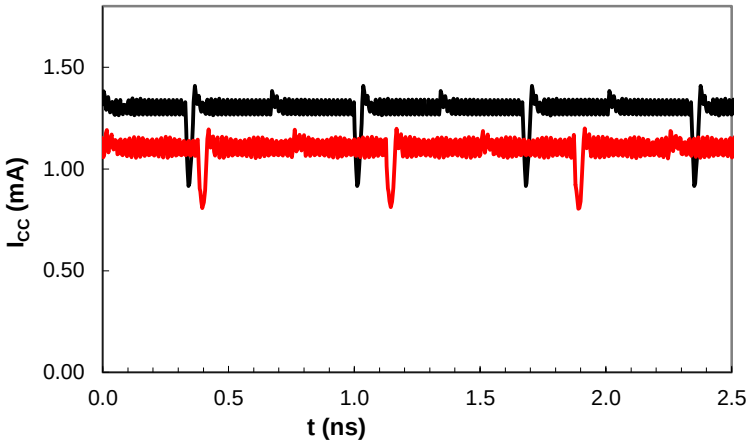


Fig. 3: *Ring oscillator under evaluation.*

In Fig 4a, the output voltage behaviour of CMOS ring oscillator has been plotted without stress (black line) and after 10^8 seconds, almost 3 years NBTI stress (red line). In both cases, the ring oscillator is working. However, a reduction of oscillation frequency from 1.5GHz to 1.3GHz after 3 years is observed, which is expected since the NBTI provokes the reduction of the pFET drain current (Fig.1). In order to have an idea about the switching noise behaviour the current consumption it is shown for similar stress time (Fig.4b). As it is observed, the current consumption is reduced after 3 years, due to the reduction of oscillation frequency. Moreover, some sharp transitions on I_{CC} are observed during the output transition which provokes a shift on the supply voltage due to the common impedance coupling. In Fig. 4c the noise spectrum on I_{CC} has been plotted, before and after 10^8s stress. Before stress (black line) a high power density about 1.5GHz (and his respective harmonics) is observed due to the sharp point on I_{CC} during the output transitions, and a high density power is also observed about 61GHz, with correspond with the transitions of each CMOS inverter. After stress, the same behaviour is observed with a frequency oscillation shift; 1.3GHz instead of 1.5GHz and 53GHz instead of 61GHz, due to the frequency oscillation reduction, as expected.



a)



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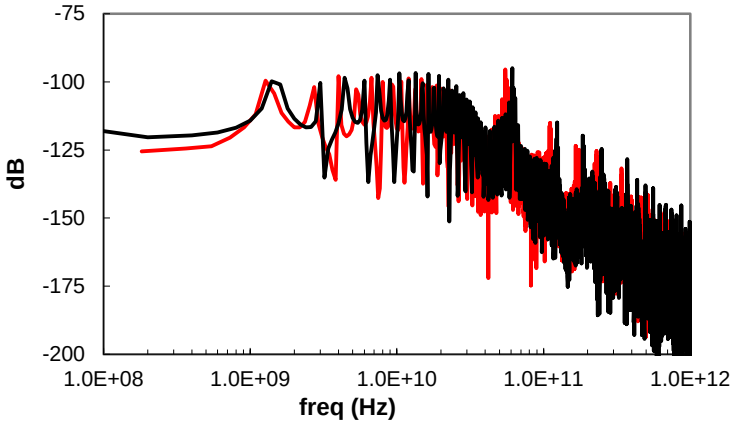

c)

Fig. 4: *Ring oscillator behaviour before (black) after stress (red).*
a) Voltage output, b) current consumption, c) Spectrum of current consumption.

4. CONCLUSIONS

In this paper the impact of aging on the electromagnetic behaviour of CMOS ring oscillator has been evaluated. Specifically, the NBTI effect on switching noise has been evaluated. After 3 years NBTI stress, the ring oscillator is still working, with a reduction about 13% of the oscillation frequency. Therefore, a current consumption reduction is observed. Regarding to the electromagnetic emission, the energy is mainly in 61GHz before stress and 53GHz after stress; which corresponds with the transition of each CMOS inverter.

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