

# Design Guidelines towards Compact Litho-Friendly Regular cells

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## Abstract

Integrated circuit design advances into the nanoscale era towards more compact, higher performance and lower power devices. However, the large number of transistors per die has entailed an increase of device variability due to sub-wavelength lithography and layout complexity impacting manufacturability. Therefore, regular designs has emerged as an alternative cell design style towards more litho-friendly designs aiming to combat the increase number of process variations in current nanoscale technologies and beyond. Thereby, several regular layout fabrics with various degrees of regularity that exploits the potential benefits of regular designs and an area overhead estimation thereof are provided throughout this work.

## 1 Introduction

Over the years, CMOS technology has not ceased to scale down and has enabled the production of increasingly complex products at lower cost, as Moore's Law predicted. Nevertheless, deep sub-micron technologies has entailed an increase of the design-process interdependencies and process variations that are influencing both integrated circuit (IC) performance and yield [1]. In order not to jeopardize circuit quality, these variations must be mitigated or at least taken into account during the circuit and layout design stage to fully realize its potential.

On-chip variations are generally classified in two categories, random and systematic. Random or statistical process variations are related to atomistic effects inherent in nanoscale devices. Line Edge Roughness, Interface Roughness, or Random Dopant Fluctuations [2] are some sources of circuit degradation caused by this type of variation. On the other hand, systematic variations refer to critical process limitations and different manufacturing process conditions. At the same time, systematic variations can be divided in two groups. Firstly, across-field (position in reticle) variations which are related to photolithographic process parameters and etching sources such as dose, focus, and exposure variations, lens aberrations, mask errors and variations in etch loading. Secondly, the type of variations analyzed throughout this work, the layout dependent variations (layout structure and the surrounding topological en-

vironment) which are predictable and can be modeled as a function of deterministic factors.

The major source of circuit performance degradation associated to layout dependent variations comes from lithography imperfections; printability becomes highly hampered and neighborhood-pattern dependent as lithography tools are being pushed to operate at their resolution limit. This has led to hot-spots, corner rounding or poor Across Chip Line-width Variation (ACLV) among other undesirable perturbations [3]. Resolution Enhancement Techniques (RETs) are currently used to correct pattern distortion and reduce variability [4]. For instance, Optical Proximity Correction (OPC) and Phase Shift Mask (PSM) techniques are two examples of post-layout enhancement methods. However, existing design rules cannot guarantee a design that fully exploits the benefits of RETs since it becomes nearly an NP-hard problem to perform an efficient analysis of layout patterns during the design optimization stage, the number of different layout shape occurrences is large [5].

As lithography advances into the 45nm technology node and beyond, a paradigm shift in design style is required to drive higher performance with smaller circuit features. Regular cell design has emerged as an alternative to traditional 2-D standard cells towards a more lithography-friendly design style [3] [6] [7] [8] [9]. 2-D refers to layouts with jogged polygons, while regular or 1-D refers to a layout with parallel straight lines (in vertical or horizon-

tal direction), with gaps (or commonly called cuts) as required to implement circuit functions. Additionally, regularity is also related to the context dependency problem, which refers to the fact that identical shapes (belonging to the same layer) printed in different locations of a cell will actually print differently if they are not equally surrounded. Thereby, using 1-D layout style with equally spaced and surrounded poly gates, several lithography induced perturbations can be dramatically decreased and manufacturability is enhanced due to the reduced number of geometry patterns and lithography interactions that must be analyzed. For instance, in [9] a similar regular strategy is proposed although the lithography constraints are not as precisely depicted as herein.

Implementing circuits other than memories following regular layout styles may lead to significant area overhead, according to [9] [10]. This overhead may be caused by the fabric's architecture and the limitations of traditional computer-aided design tools that are not optimized to fulfill regular fabrics requirements. Therefore, regular layout styles must be properly adjusted to minimize area penalty while at the same time maximizing circuit reliability and performance. In addition, transistor ordering and intra-cell routing algorithms must be enhanced in order to minimize the area penalty that regular constraints might cause. In [8], a regular routing algorithm is presented, although applied to VeSFET transistors.

The aim of this paper is to provide an area comparison between different regular designs and traditional standard cell designs. The regular cell design styles are created by UPC (ALARC) and Nangate (Nangate regular on-grid). Nangate cells are focused on minimizing cell area penalty with the exploit of transistor ordering and routing algorithms that considers regularity constraints. ALARC cells aims to minimize lithography-induced variations in order to increase circuit reliability.

The rest of the paper is organized as follows. In section 2 insights on lithography-aware design style are provided. The characteristics of the regular fabrics presented throughout this work are outlined in section 3. In section 4 an area comparison between the proposed regular styles and commercial cells is performed. The paper concludes in section 5 providing some interesting future avenues of research.

## 2 Lithography effects

While the benefits for manufacturability of layout regularity have been clearly demonstrated [5], a regular design does not directly imply that lithography variations are mitigated. Cell parameters such as cell pitch, gate length, metal widths, etc. must be properly adjusted in order to fully exploit the potential benefits of regularity.

Therefore, in order to model lithography perturbations and identify places in a layout where optical effects may affect functionality, we use a Calibre Litho-Friendly Design

(LFD) [11] rule deck provided by North Carolina State University (NCSU) based on an open-source 45nm technology Physical Design Kit (PDK) [12]. This PDK uses a Predictive Technology Model (PTM) that provides customizable and predictive model files for future transistor and interconnect technologies. Next, the lithography constraints that have to be taken into account during the design stage to reduce lithography variations are outlined, although for a more detailed study refer to [13].

### 1. Channel length line-pattern resolution.

- (a) Gates must be surrounded side by side by other poly lines to minimize the gate length narrowing. All diffusion strips must be surrounded side by side by dummy poly lines.
- (b) Poly lines must be equally spaced so systematic poly-induced variations affect equally throughout all poly lines (regularity constraint). Hence, the across chip line-width variation (ACLV) between transistors is minimized.
- (c) An excessive poly pitch between contiguous poly lines dramatically augments the gate length degradation.
- (d) Drawn gate length becomes directly dependent on poly gate spacing and this relation can be easily modeled due to regularity constraint 1b.

### 2. Contacts and Vias enclosures.

- (a) *Diffusion Contacts*: SD contacts must be properly enclosed by the active region in order to avoid them to fall outside the oxide strip.
- (b) *Poly contacts*: Poly contacts must be perfectly surrounded by the poly region extension created specifically for this connection to enhance the reliability of the input connection.
- (c) *Vias and contacts*: Metal lines must be wide enough so vias and contacts do not fall outside the metal layers and diffusion strips.
- (d) *Power rail vias*: Wider metal lines (e.g. the power supply rails) requires a wider enclosure to avoid vias falling outside the metal layer. In order to avoid this problem, we can connect vias on top of the substrate contacts, i.e., half pitch displaced from the routing grid so vias will be inside the power supply.

### 3. Metal Connections.

- (a) All metal shapes are unidirectional in order to avoid proximity effects such as corner rounding or pinching due to hammerhead shapes.
- (b) Spacing must be properly designed in order to avoid shorts between contiguous metal lines. Additionally, metal lines must be equally

spaced in order to first maximize regularity and second ease routability.

#### 4. Input placement.

- (a) The shape of the poly contact enclosure should be rectangular, aligned with the poly shape and avoiding an abrupt change in poly width which might cause the poly gate to pinch.
- (b) The number of poly contacts must be minimized in order to decrease the number of poly irregularities.
- (c) Poly contacts are preferably placed on the ends of the poly gate to avoid the double narrowing/widening effect.
- (d) Inputs should be placed far enough from the active region in order to obtain a regular line-pattern resolution in the channel region.

#### 5. Poly extension.

- (a) The poly gate end without a poly contact should be sufficiently extended so the line-end rounding will fall outside the active region.

### 3 Regular cell styles

Regular designs tend to be rather similar at first glance (each regular design contains unidimensional poly gates and unidimensional diffusion strips). The difference between design styles lies in small details that configures the cell that in the end determines the characteristics and performance of the cell. In this section, two regular design styles, UPC ALARC style and Nangate Regular on-grid style are depicted. Additionally, two variants of each regular design style are provided aiming to optimize specific cell characteristics.

#### 3.1 ALARC architectures

Up to this point, we have seen different lithography constraints that must be jointly considered to minimize lithography perturbations. Furthermore, regular designs are characterized by having only unidimensional shapes. Therefore, an adaptive lithography-aware regular cell design structure (ALARC) that takes into account all the lithography features previously outlined is presented in this section. Note that a regular litho-friendly design presents an undoubted advantage compared to traditional standard cell designs; the effort of resolution enhancement techniques such as optimal proximity correction (RET-OPC) is dramatically reduced since all lithography imperfections can be fast identified and corrected during the creation of the cell design template. Next are described the general characteristics of the ALARC cell templates.

#### Common aspects

- All NMOS transistors lie in a single row near the bottom of the cell and all PMOS transistors lie in a single row near the top of the cell (this is akin to the single-row layout style of standard cells).
- Active regions can contain any number of equal width transistors.
- Dummy polysilicon lines are placed between different active regions and at the cell boundaries.
- Metal1 lines are used for horizontal connections and metal2 for vertical ones.
- All metal lines belonging to the same layer are equally spaced and placed over the routing grid, except the power supply rails that are half track displaced.
- The cell height of each cell is determined by the minimum height necessary to map all logic gates necessary for a given circuit.
- Substrate contacts are placed on the power supply rails.
- Transistor Ordering algorithm is provided by Nangate (outperforms Euler-path algorithms).
- Intra-cell routing is performed manually and it considers lithography effects.

By considering all the previous characteristics, two regular cell architectures are defined for optimizing different cell parameters. *ALARC MAX LITHO* takes lithography constraints to the limit and it aims to enhance at maximum line-pattern resolution in the cell. *ALARC MIN AREA* aims to minimize cell area penalty by alleviating lithography constraints.

#### Specific aspects

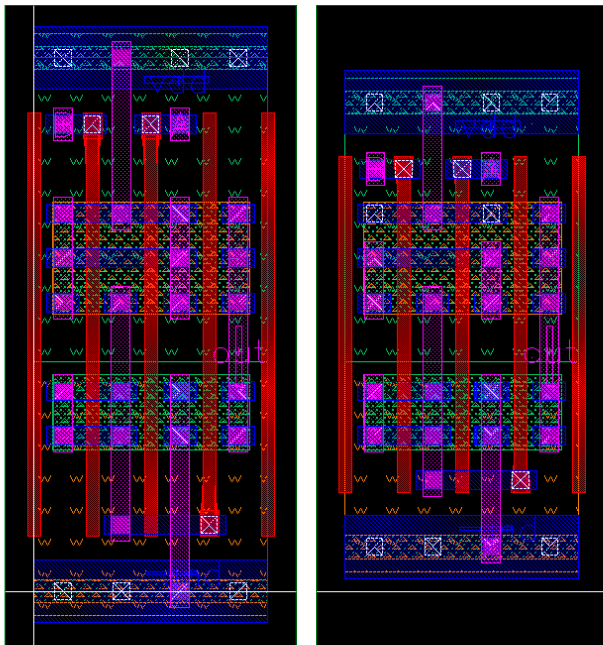
##### • *ALARC MAX LITHO*

- The number of cell tracks necessary for the cells used throughout this work is 12.
- Inputs must be placed on the ends of polysilicon gates.
- The minimum spacing between a polysilicon-input connection and its respective active region is established as 260nm. This is equivalent as not allowing any active region below the closest horizontal routing track from any polysilicon contact. This design rule is clearly depicted in figure 1(a).
- Polysilicon contact enclosures are optimized to completely wipe out the narrowing/widening suffered inside the channel region (this effect is caused by the irregularity introduced by the enclosure).

- **ALARC MIN AREA**

- The number of cell tracks necessary for the cells used throughout this work is 10.
- Inputs are preferably placed at both ends of polysilicon gates, although they may be placed in any other place except over the channel.
- The spacing restriction between polysilicon contacts and active regions can be omitted only if routability is not satisfied otherwise (augments litho-variations in the channel).
- Polysilicon contact enclosures directly depends on the spacing between the active region and polysilicon contacts. Hence, whenever the previous spacing restriction is not satisfied, an alternative enclosure is employed in order to minimize the channel narrowing/widening distortion. Note that only 4 types of enclosures are required and they can be perfectly defined during the cell template design. Observe from figure 1 the different type of enclosures used in these designs.

Figure 1 illustrates an implementation of both ALARC design variants. Finally, it is important to highlight that the employment of either the *MAX LITHO* or the *MIN AREA* template depends on the designer; the limit between area penalty, reliability and lithography accuracy varies according to the overall circuit performance requirements.



(a) AND2 using template ALARC MAX LITHO (b) AND2 using template ALARC MIN AREA

**Figure 1:** AND2 logic gate designed following ALARC rules.

## 3.2 Nangate cell architectures

The gridded cell architectures from Nangate represent a trade-off between layout regularity and cell density. Both architectures have polysilicon, metal and via shapes placed on a grid with pitch equal to half the cell grid pitch. The main objective of this gridded layout strategy is to reduce lithography perturbations, generating cells that are DRC clean by construction. This is achieved by confining the allowed layout patterns to a subset of the patterns from the technology design rules and by defining a cell grid that implicitly respects all the design rules for these allowed patterns. The next subsections detail the characteristics of the Nangate cell architectures.

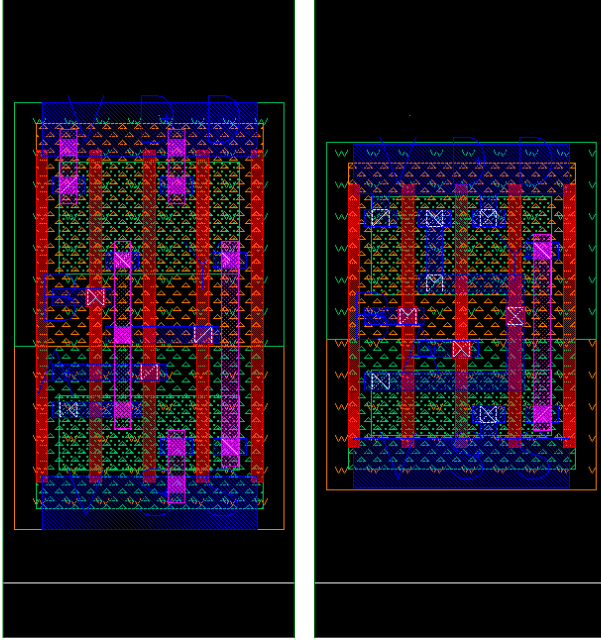
### Common aspects

- All NMOS transistors lie in a single row near the bottom of the cell and all PMOS transistors lie in a single row near the top of the cell.
- Active regions can contain any number of transistors, all with the same width.
- All contacts, vias, polysilicon and metal wires should be placed on the routing grid.
- Dummy polysilicon lines are placed between different active regions and at the cell boundaries.
- The power rails are in metal1 over the cell boundary.
- The cell height of each cell template is defined based on the routing resources required for routing a DF-FRS using the specified routing layers and allowed directions.
- The cell pitch  $x$  is defined as the Gate-OD\_Contact-Gap-Gate minimum space.
- Field polysilicon, metal1 (with the exception of power rails) and metal2 wires have always the minimum allowed technology width.

### Specific aspects

- **Nangate 9 tracks (9T)**
  - Metal1 routing: vertical and horizontal.
  - Metal2 routing: vertical only.
  - Cell height: 9 tracks.
  - Inputs are placed in two rows between the NMOS and PMOS transistors.
  - The cell pitch  $y$  is defined in such a way that two horizontal Metal1 wires can be placed in adjacent rows with the same  $x$  coordinates.
- **Nangate 10 tracks (10T)**
  - Metal1 routing: horizontal only.
  - Metal 2 routing: vertical only.

- Cell height: 10 tracks.
- Inputs are placed in three rows between the NMOS and PMOS transistors.
- The cell pitch  $y$  is defined in such a way that two vias can be placed in adjacent rows with the same  $x$  coordinate.



(a) AND2 using template Nangate 10T (M1 1D) (b) AND2 using template Nangate 9T (M1 2D)

**Figure 2:** AND2 logic gate designed following Nangate rules.

## 4 Experimental results

In this section it is analyzed the area impact between the cell fabrics presented throughout this work. Cells are created using an open source 45nm technology provided by the NCSU [12]. Additionally, these designs are compared with cells created using a real commercial 45nm technology.

### 4.1 Cell style area comparison

The area overhead can qualitatively be appreciated from figures 1 and 2 (all figures are equally scaled). The area impact of utilizing all regular features for Nangate fabrics is about 27% (area penalty of nangate 10T with respect to Nangate 9T). This area penalty is mainly caused by the employment of unidimensional metal shapes, besides the consequent increase in the vertical cell pitch and number of tracks. Observe that nangate regular fabric (nangate 10T), has up to 24% area penalty when comparing it to a real commercial technology (Commercial HD), although

nangate 9T architecture does not have any area overhead. When considering lithography effects to enhance circuit performance and reliability, the area overhead augments up to 64% (ALARC MIN AREA fabric) compared to both nangate 9T and Commercial HS. This overhead is related to 1D layout style restriction (which affects equally any regular layout) and by the increase in both cell pitches. Observe that the area is almost doubled when boosting line-pattern resolution and reliability (ALARC MAX LITHO). Finally, the considerable improvement in terms of printability and better variability control between ALARC cells and traditional standard cells is detailed in [13].

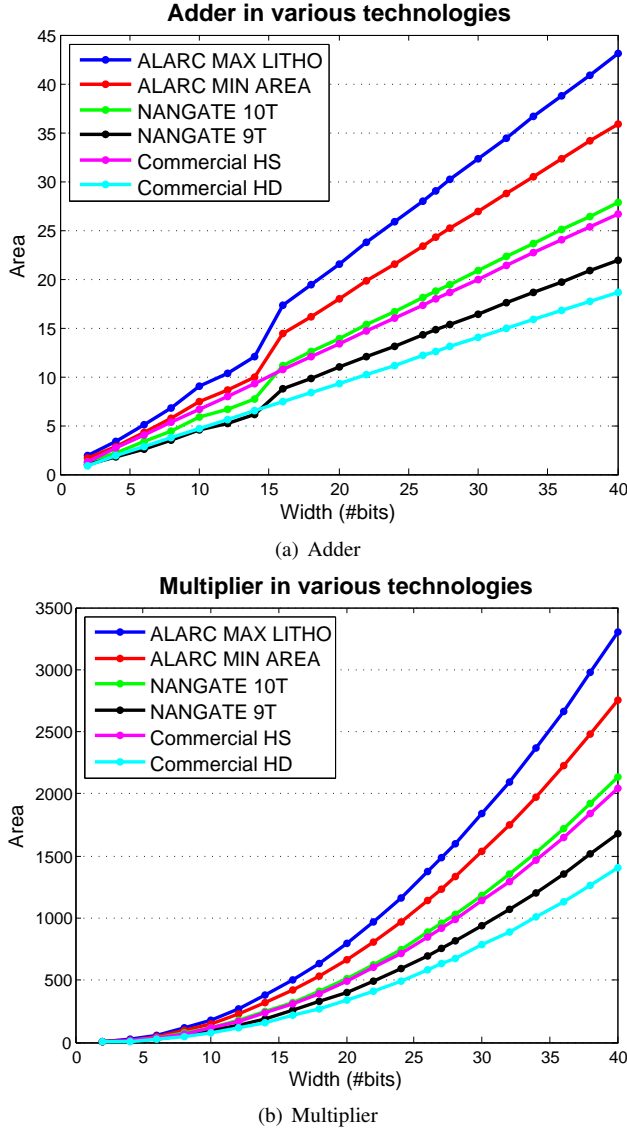
Table 1 shows an area comparison of two representative common logic functions, an AND2 and a DFFSR logic gates. To analyze the behavior of cells designed in various fabrics and technologies, the area results are normalized with respect the Nangate 9T fabric.

### 4.2 Benchmark implementations area comparison

Note that a circuit level implementation gives a more realistic area overhead estimation. Thereby, figure 3 shows an area comparison of adders and multipliers with different number of bits for various layout design styles. Note that the area results for both circuits are normalized using the nangate 9T 2 bits adder and 2 bits multiplier respectively. Lithography-aware regular fabrics (ALARCs) presents an area overhead compared to the commercial HD designs of 135% for the ALARC MAX LITHO and a 100% penalty for the ALARC MIN AREA, which again are mainly caused by the increase in the cell pitches. Observe that slight area penalty is suffered by Nangate 10T regular fabric compared to the commercial HS (High Speed), approximately 4%, although it increases up to 52% when considering the commercial HD fabric (High density). The major difference compared to the cell area study (table 1) lies between the Nangate 9T and Commercial HD that the area increases about 20%, when the cell area overhead was almost negligible. This area penalty might be caused by different intra-cell routing, i.e., despite having equal cell size, the commercial cell might use less metal resources or better input allocation that favour place and route of the complete circuit. Additionally, note that the Commercial design uses a different technology compared to the other fabrics that utilizes the FreePDK design kit and thus part of the area discrepancy might be caused by differences in the design rules.

**Table 1:** Cell area comparison between different fabrics for an AND2 and a DFFSR logic gates.

Architecture	AND2	DFFSR	Tracks	X Pitch	Y Pitch	L drawn
<i>Nangate 9T</i>	1	1	9	230	140	50
<i>Nangate 10T</i>	1,27	1,27	10	230	160	50
<i>ALARC MAX LITHO</i>	1,97	1,97	12	250	190	55
<i>ALARC MIN AREA</i>	1,64	1,64	10	250	190	55
<i>Commercial HS (High Speed)</i>	1,22	1,11	-	-	-	-
<i>Commercial HD (High Density)</i>	0,97	0,99	-	-	-	-



**Figure 3:** Circuits implemented using various technologies.

## 5 Conclusions and future avenues of research

In this work we have shown that a 1D regular design (Nangate 10T) presents an area overhead of 52% compared to commercial standard cells (Commercial HD); the semi-regular design nangate 9T suffers only a 20% of area penalty compared also with the commercial HD. Furthermore, when considering a regular lithography-aware design, the area overhead is 100% for the ALARC MIN AREA and 135% for the ALARC MAX LITHO compared to the Commercial HD.

The numerical values for the regular fabrics presented in this work (Nangates and ALARCs) are based on the FreePDK 45nm technology kit and they may differ from a real technology. For other technologies, lithography simulations should be run to determine appropriate parameters of the ALARC cells. Note that all designs presented throughout this work are still under development and in the future, it is expected to create litho-friendly regular fabrics that will combine the potential benefits of all regular implementations presented herein. Moreover, the yield improvements achieved by using more regular designs are part of the future work. To conclude, the regular designs presented in this text show the directions of the SYNAPTIC project in terms of cell design architectures and the implications of regularity and lithography in cell design.

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