Converter Structure-Based Power Loss and Static Thermal Modeling of The Press-Pack IGBT-Based Three-Level ANPC and HB VSCs Applied to Multi-MW Wind Turbines

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***Abstract* -- The wind turbine converters demand high power density due to nacelle space limitation and high reliability due to high maintenance cost. Once the converter topology with the semiconductor switch technology is selected, the converter power density and reliability are dependent on the component count and the switch thermal performance which is determined by the converter load profile and the converter structure. In this study, the converter-structure based power loss and thermal models are developed for the medium voltage full-scale 3L-ANPC-VSC and 3L-HB-VSC utilizing press-pack IGBT-diode pairs and interfacing a 6MW wind turbine to a medium voltage grid. The switching power loss models are built using the experimentally obtained switching power loss data from a full-scale 3L-ANPC-VSC leg. The static thermal models are developed considering the double-sided cooling of the switches by the cooling plates. For the experimental model verifications, a test setup with a single-phase full-scale 3L-ANPC-VSC is introduced. Using the power loss and thermal models, the switch junction temperatures are obtained on simulation for the wind turbine grid interface. The power density and reliability of the VSCs are discussed and compared with respect to these junction temperatures as well as the counts of press-pack switches, gate driver, and cooling plate.**

***Index Terms*-- Press-pack IGBT, ANPC, HB, power loss, thermal model, power density, reliability, wind turbine**

I. INTRODUCTION

Boosted from 4.3% (688MW) in 2006 to 6.0% (1877MW) in 2008 [1], the share of multi-MW (>2.5MW) wind turbines in the fast growing wind energy market has been increasing significantly. As the grid codes regulating the wind turbine connections are getting stricter, the interface between wind turbine and electricity grid for penetrating MWs of wind power becomes a challenge. Consequently, the full-scale power electronic converters, which process all the wind turbine output power while ensuring compliance with the grid codes, are attracting more interest than ever. Although the full-scale converters can be designed as parallel low voltage converter units [2], a single medium voltage (MV) converter unit [3] becomes more preferable due to its smaller footprint, less cabling cost, and less component count as the turbine output power increases beyond 5MW.

The MV power electronic converters are generally realized as multi-level (ML) voltage source converters (VSC) instead of 2L-VSCs in order to improve the figures of switch power losses, harmonic distortion, *dv/dt*, and common mode voltage/current [4]. In the literature, there are three main ML-VSC topologies, which are neutral point clamped (NPC), flying capacitor (FC), and cascaded H-bridge (CHB) [4], [5]. For MV AC drive applications, these topologies have been studied in the literature extensively [4], [5] and compared in detail [6]. Also, there are several studies about these topologies applied to wind turbines [2], [7], [8].

Among ML-VSCs, 3L-VSCs have found the highest interest because of their lower cost, higher power density, and higher reliability as a result of less component count than >3L-VSCs. Among 3L-VSCs, 3L-NPC-VSC has domination in the AC drive market [5]. As an improvement for 3L-NPC-VSC's inherent problem of unequal power loss distribution, its clamping branches are reinforced with active clamping switches and 3L Active NPC (ANPC) is formed (Fig. 1) [9]. Besides, 3L-HB-VSC shown in Fig. 2 assures equal power loss distribution inherently [10]. Furthermore, its modulation flexibility enables that the same power loss distribution as 3L-NPC-VSC can be obtained [11].

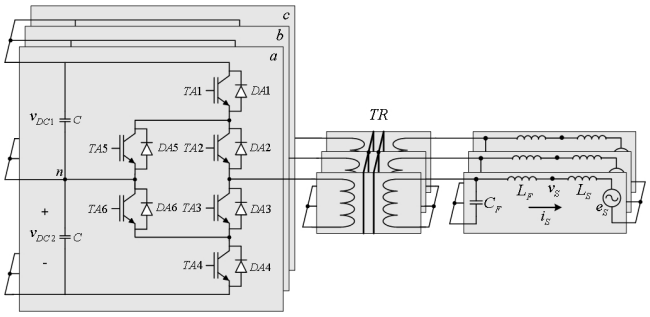

Fig. 1. Three-phase 3L-ANPC-VSC connected to a MV grid

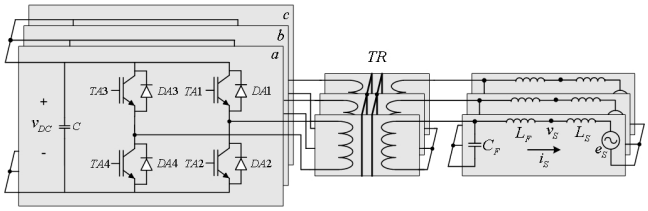

Fig. 2. Three-phase 3L-HB-VSC connected to a MV grid

Compared to the AC drive applications, the wind turbine applications demand higher power density due to nacelle space limitation and higher reliability due to high maintenance cost. Therefore, the switch technology selection in association with the converter topology is even more critical for the wind turbine applications. Among the state-of-the-art MV switches, the press-pack IGBT appears to be advantageous over IGBT modules and IGCTs regarding power density and reliability because it possesses all the attributes of double-sided cooling, wire-bondless contacts, snubberless operation, small gate drivers, high switching frequency at rated voltage and current [12].

In addition to the converter topology and switch technology, the switch thermal performance limits the converter power density and reliability [9]. While the maximum switch junction temperature determines the power density, the switch junction temperature variations due to the converter load profile along with the converter structure determine the switch lifetime [13], [14] and thereby, converter reliability in a sense. Therefore, the accurate converter structure-based power loss and thermal models are required in order to quantify the power density and reliability.

In this paper, first, the press-pack IGBT-based 3L-ANPC-VSC and 3L-HB-VSC are introduced in regards to the conduction paths affecting switching power losses and the pulse-width modulation (PWM) method utilizing these conduction paths. Secondly, the power loss modeling approach is introduced such that the switch current- and commutation path-dependent switching loss functions are derived using the switching energy loss figures obtained via double-pulse switching tests. Next, the static thermal models consisting of thermally resistive elements are developed regarding the physical converter structure with the press-pack switches featuring double-sided cooling and using the manufacturers' thermal data. After the test setup including a full-scale single-phase 3L-ANPC-VSC for verification of the power loss and static thermal models is introduced, these models are applied to the three-phase 3L-ANPC-VSC and 3L-HB-VSC interfacing a 6MW wind turbine with a grid on simulation and their switch junction temperatures are obtained. Finally, the power density and reliability of 3L-ANPC-VSC and 3L-HB-VSC are discussed comparatively with respect to the switch junction temperatures and the converter components including only IGBT-diode pairs, cooling plates, and gate drivers.

II. 3L-ANPC-VSC AND 3L-HB-VSC

The VSCs shown in Fig. 1 and Fig. 2 are able to produce three-level output voltages such as V_{DC1}, 0, $-V_{DC2}$ for 3L-ANPC-VSC and V_{DC}, 0, $-V_{DC}$ for 3L-HB-VSC. Assuming $V_{DC1}=V_{DC2}=V_{DC}$, the same voltage blocking capability is required for the switches of both VSCs. Each voltage level can be produced by specific conduction paths depending on the output current direction. For instance, Fig. 3 and 4 show the conduction paths required for generating V_{DC1} & 0 and V_{DC} & 0. In the following, the definition and PWM utilization for the two different zero voltage producing paths are explained.

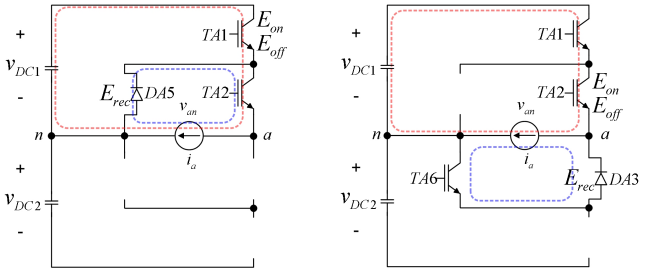

Fig. 3. *Mode-I* (left) and *Mode-II* (right) conduction paths of 3L-ANPC-VSC for $v^*_{an}>0$ and $i_a>0$

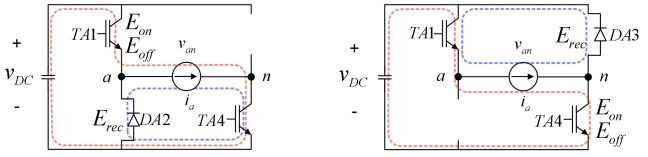

Fig. 4. *Mode-I* (left) and *Mode-II* (right) conduction paths of 3L-HB-VSC for $v^*_{an}>0$ and $i_a>0$

A. Mode Definition

The utilization of one of the two zero voltage generating paths together with a non-zero voltage generating path during a PWM period is termed as *Mode* in this study. For 3L-ANPC-VSC, *Mode-I* uses the zero voltage producing path inside the contour of the non-zero voltage producing path while *Mode-II* uses the one outside this contour (Fig. 3). Similarly, *Mode-I* and *Mode-II* can be defined for 3L-HB-VSC (Fig. 4). It should be noted that *Mode-I* implies a *Type-I* commutation and *Mode-II* implies a *Type-III* commutation defined in [9] for 3L-ANPC-VSC. Associated with *Mode-I* and *II*, the switching energy losses move from a switch to

another, where these losses are classified as IGBT turn-on E_{on}, IGBT turn-off E_{off}, and diode reverse recovery E_{rec} losses. Table I and II summarizes these losses with respect to *Mode*, reference voltage v^*_{an}, and current i_a for phase *a*.

TABLE I
SWITCHING LOSSES ON THE IGBT-DIODE PAIRS OF 3L-ANPC-VSC

	Mode-I				*Mode-II*			
	$v^*_{an}>0$		$v^*_{an}<0$		$v^*_{an}>0$		$v^*_{an}<0$	
	$i_a>0$	$i_a<0$	$i_a>0$	$i_a<0$	$i_a>0$	$i_a<0$	$i_a>0$	$i_a<0$
TA1-DA1	E_{on}, E_{off}	E_{rec}	-	-	-	-	-	-
TA2-DA2	-	-	-	-	E_{on}, E_{off}	E_{rec}	E_{rec}	E_{on}, E_{off}
TA3-DA3	-	-	-	-	E_{rec}	E_{on}, E_{off}	E_{on}, E_{off}	E_{rec}
TA4-DA4	-	-	E_{rec}	E_{on}, E_{off}	-	-	-	-
TA5-DA5	E_{rec}	E_{on}, E_{off}	-	-	-	-	-	-
TA6-DA6	-	-	E_{on}, E_{off}	E_{rec}	-	-	-	-

TABLE II
SWITCHING LOSSES ON THE IGBT-DIODE PAIRS OF 3L-HB-VSC

	Mode-I				*Mode-II*			
	$v^*_{an}>0$		$v^*_{an}<0$		$v^*_{an}>0$		$v^*_{an}<0$	
	$i_a>0$	$i_a<0$	$i_a>0$	$i_a<0$	$i_a>0$	$i_a<0$	$i_a>0$	$i_a<0$
TA1-DA1	E_{on}, E_{off}	E_{rec}	E_{on}, E_{off}	E_{rec}	-	-	-	-
TA2-DA2	E_{rec}	E_{on}, E_{off}	E_{rec}	E_{on}, E_{off}	-	-	-	-
TA3-DA3	-	-	-	-	E_{rec}	E_{on}, E_{off}	E_{rec}	E_{on}, E_{off}
TA4-DA4	-	-	-	-	E_{on}, E_{off}	E_{rec}	E_{on}, E_{off}	E_{rec}

B. PWM Approach

This study adopts the modulation of 3L-NPC-VSC as the base modulation method and proposes the utilization of its modulation signals via appropriate mappings in order to modulate 3L-ANPC-VSC and 3L-HB-VSC. This approach takes the following fact a priori: all these three converters can produce any of the three voltage levels by conducting two semiconductors at a time. Once generated via phase disposition type pulse-width modulation (PD-PWM) for 3L-NPC-VSC (Fig. 5), the modulation signals of 3L-NPC-VSC are mapped over the ones of 3L-ANPC-VSC and 3L-HB-VSC shown in Table III and IV such that the predefined conduction paths by *Mode I* and *II* are used. It should be noted that *Mode-0* in Table III implies the usage of the zero path which the current direction allows since the clamping IGBTs are either nonexistent or turned-off.

Utilization of *Mode-I* and *Mode-II* during an electrical cycle T_e determines the distribution of the total switch power losses over the VSCs. For proper PWM operation, mode transitions are permitted only at the beginning of the PWM period T_{PWM}. Obviously, homogeneous power loss distribution is aimed for the best electrical and thermal utilization of the switches. Therefore, a mode sequence in T_e should be defined. In this study, the mode sequence is set as the consecutive and equal utilization of *Mode-I* and *Mode-II* in order to homogenize the switching power loss P_{sw} distribution approximately. For the total power loss homogenization attempts in 3L-ANPC-VSC, an extra effort considering the conduction power losses P_{con} and operating conditions should be undergone as in [9].

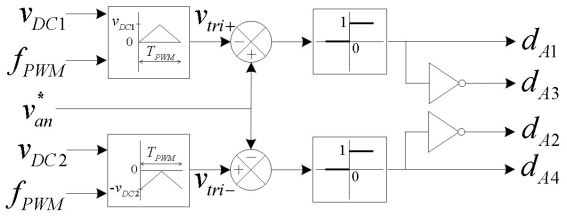

Fig. 5. PD-PWM for phase-*a* of 3L-NPC-VSC

TABLE III
PWM SIGNAL MAPPING FOR 3L-ANPC-VSC

	Mode-0	*Mode-I*		*Mode-II*	
	All v^*_{an}	$v^*_{an}>0$	$v^*_{an}<0$	$v^*_{an}>0$	$v^*_{an}<0$
$d_{A1,ANPC}$	d_{A1}	d_{A1}	d_{A2}	d_{A2}	d_{A1}
$d_{A2,ANPC}$	d_{A2}	d_{A2}	d_{A1}	d_{A1}	d_{A2}
$d_{A3,ANPC}$	d_{A3}	d_{A4}	d_{A3}	d_{A3}	d_{A4}
$d_{A4,ANPC}$	d_{A4}	d_{A3}	d_{A4}	d_{A4}	d_{A3}
$d_{A5,ANPC}$	*0*	d_{A3}	d_{A4}	d_{A4}	d_{A3}
$d_{A6,ANPC}$	*0*	d_{A1}	d_{A2}	d_{A2}	d_{A1}

TABLE IV
PWM SIGNAL MAPPING FOR 3L-HB-VSC

	Mode-I		*Mode-II*	
	$v^*_{an}>0$	$v^*_{an}<0$	$v^*_{an}>0$	$v^*_{an}<0$
$d_{A1,HB}$	d_{A1}	d_{A2}	d_{A2}	d_{A1}
$d_{A2,HB}$	d_{A3}	d_{A4}	d_{A4}	d_{A3}
$d_{A3,HB}$	d_{A4}	d_{A3}	d_{A3}	d_{A4}
$d_{A4,HB}$	d_{A2}	d_{A1}	d_{A1}	d_{A2}

III. POWER LOSS MODELING

The switching energy losses depend on IGBT/diode current I_C/I_F and voltage V_{CE}/V_{KA} as well as stray inductance L_σ of the IGBT/diode commutation path, IGBT gate resistance R_G, and junction temperature T_j [15] as given in (1)-(3). Besides, the conduction power losses depend on I_C/I_F and T_j as given in (4), (5).

$$E_{on} = f_{on}(I_C, V_{CE}, T_j, L_\sigma, R_G) \quad (1)$$

$$E_{off} = f_{off}(I_C, V_{CE}, T_j, L_\sigma, R_G) \quad (2)$$

$$E_{rec} = f_{rec}(I_F, V_{KA}, T_j, L_\sigma, R_G) \quad (3)$$

$$P_{con,IGBT} = I_C \cdot V_{CE,sat}(I_C, T_j) \quad (4)$$

$$P_{con,diode} = I_F \cdot V_F(I_F, T_j) \quad (5)$$

Once obtained accurately, these loss functions can be employed along with a specific VSC's electrical model. Although P_{con} data derived from manufacturer datasheets given is quite directly usable, the switching energy loss data cannot be directly usable because L_σ and R_G used in manufacturer tests may significantly deviate from the ones of practical VSCs. Furthermore, the VSCs such as ANPC employ different commutation paths with different L_σ values. Therefore, double-pulse tests, through which the switching

energy loss data are collected, should be applied to the switches mounted on either the VSCs or the test circuits with the same L_σ as the VSCs in order to extract accurate switching loss data. In the following, the switching loss data extraction from a practical 3L-ANPC-VSC and then the power loss modeling via utilization of both the switching and conduction power loss data along with the electrical models are explained.

A. Switching Loss Data Extraction

The double-pulse tests, which are standard tests for switch characterization, are applied to the 3L-ANPC-VSC prototype shown in Fig. 6 (with the parameters in Table VII) for the commutation paths with different L_σ. Thereby, the switching loss figures are collected when T_j equals ambient temperature of 20-25°C. Moreover, these losses can be fitted to the linear functions of I_C/I_F as in (6)-(8). In order to obtain the temperature dependent switching loss data, these tests should be done for T_j between 25°C and 125°C.

$$E_{on} = a_0 + a_1 I_C \tag{6}$$

$$E_{off} = b_0 + b_1 I_C \tag{7}$$

$$E_{rec} = c_0 + c_1 I_F \tag{8}$$

The commutation loops for *Mode-I* and *Mode-II* are represented by darker colors on the simplified VSC structure (Fig. 7) and the simplified circuit diagram (Fig. 8) for $v^*_{an}>0$. As given in (9) and (10), *Mode-II* results in longer path and higher L_σ than *Mode-I*. For these two modes, the switch voltage, current, and power waveforms for $I_C\approx$1200A and V_{CE}=2500V are experimentally obtained (Fig. 9-12). Via the IGBT turn-on waveforms in Fig. 9 and 10, $L_{\sigma,ANPC,MI}$ and $L_{\sigma,ANPC,MII}$ can be estimated as ~200nH and ~400nH by using (11) describing the initial V_{CE} fall accross L_σ resulting almost constant dI_C/dt [16]. This inductance difference affects E_{on} and E_{rec} significantly while E_{off} remains almost the same.

$$L_{\sigma,ANPC,MI} = 2L_{\sigma1} + L_{\sigma2} + L_{\sigma4} \tag{9}$$

$$L_{\sigma,ANPC,MII} = 4L_{\sigma1} + L_{\sigma2} + 2L_{\sigma3} + L_{\sigma4} \tag{10}$$

$$L_\sigma = (V_{DC} - V_{CE})(dI_C/dt)^{-1} \tag{11}$$

For *Mode-II*, the experimental switching loss data and the corresponding linear functions are shown in Fig. 13. Using the parameters derived from the data and given in Table V, the switching energy loss functions are shown in Fig. 14.

For the 3L-HB-VSC, the commutation loops of *Mode-I* and *Mode-II* are identical and their stray inductances are the same (Fig. 15). Since these inductances are close to $L_{\sigma,ANPC,MI}$ as in (12), the switching loss functions derived for *Mode-I* of 3L-ANPC-VSC can be directly applied to 3L-HB-VSC.

$$L_{\sigma,HB} = 2L_{\sigma1} + L_{\sigma4} \approx L_{\sigma,ANPC,MI} \tag{12}$$

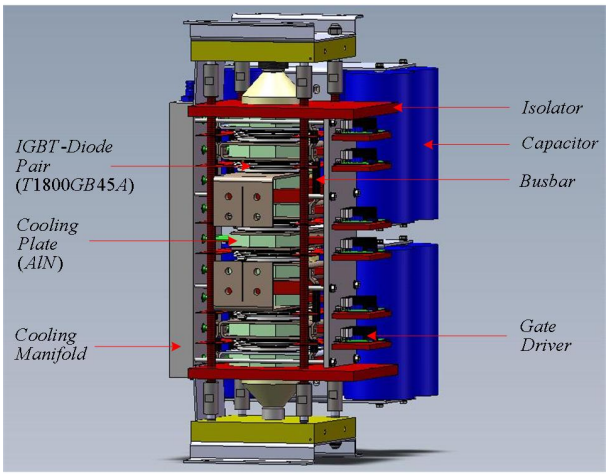

Fig. 6. Single leg structure of 3L-ANPC-VSC

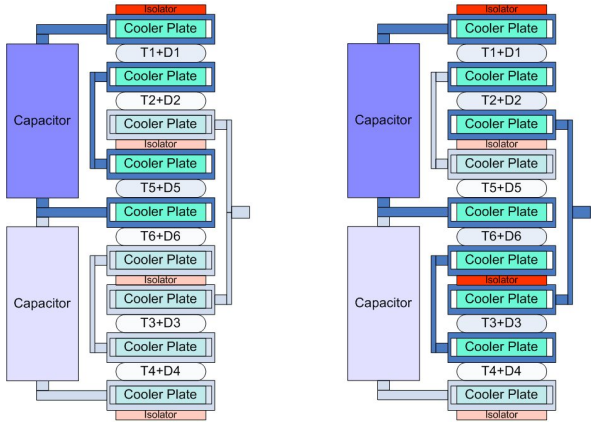

Fig. 7. Commutation paths of *Mode-I* (left) and *Mode-II* (right) for $v^*_{an}>0$ shown in the simplified structure of 3L-ANPC-VSC

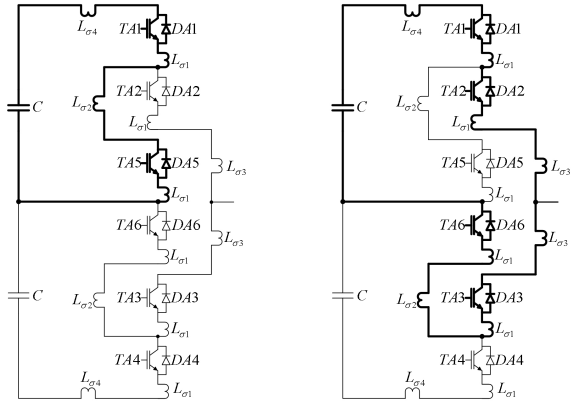

Fig. 8. Commutation paths of *Mode-I* (left) and *Mode-II* (right) for $v^*_{an}>0$ shown in the simplified circuit diagram of 3L-ANPC-VSC

B. Power Loss Modeling Approach

Along with the electrical VSC simulation outputs V_{CE}/V_{KA}, I_C/I_F, and duty cycles d; the power loss models utilize the switching energy loss functions derived as (6)-(8) with the

parameters given in Table V and the simplified conduction power loss functions at 25°C supplied by the manufacturer as given in (13) and (14) with the parameters $V_{T0,IGBT}$=1.81V, $r_{T,IGBT}$=1.33mΩ, $V_{T0,diode}$=2.43V, and $r_{T,diode}$=0.93mΩ [17].

$$P_{con,IGBT} = I_C(V_{T0,IGBT} + r_{T,IGBT} I_C) \quad (13)$$

$$P_{con,diode} = I_F(V_{T0,diode} + r_{T,diode} I_F) \quad (14)$$

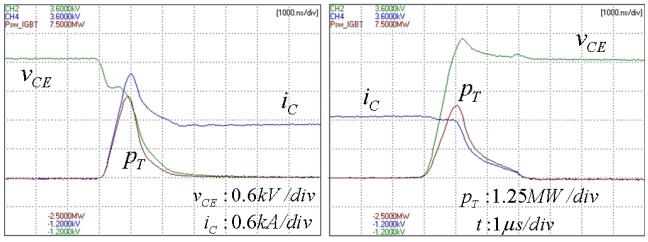

Fig. 9. IGBT switching voltage (green), current (blue), power loss (brown) waveforms during IGBT turn-on (left) and turn-off (right) for *Mode-I*

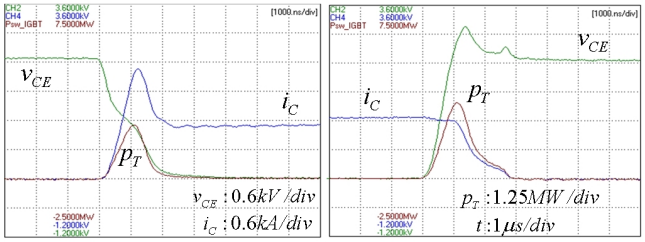

Fig. 10. IGBT switching voltage (green), current (blue), power loss (brown) waveforms during IGBT turn-on (left) and turn-off (right) for *Mode-II*

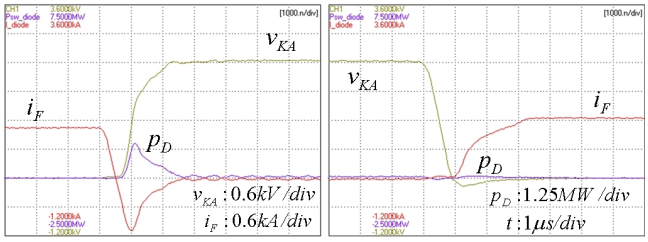

Fig. 11. Diode switching voltage (yellow), current (red), power loss (purple) waveforms during IGBT turn-on (left) and turn-off (right) for *Mode-I*

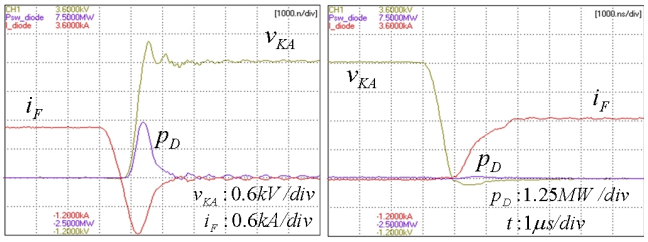

Fig. 12. Diode switching voltage (yellow), current (red), power loss (purple) waveforms during IGBT turn-on (left) and turn-off (right) for *Mode-II*

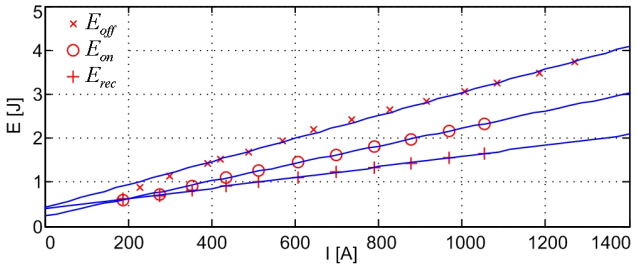

Fig. 13. Switching energy loss data and functions for *Mode-II*

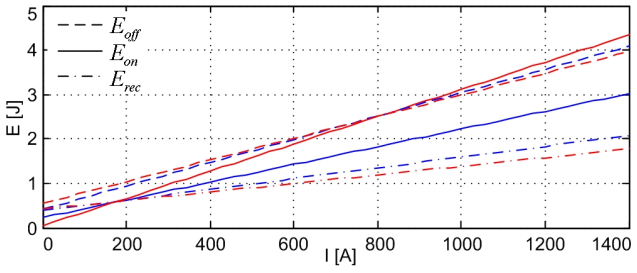

Fig. 14. Switching energy loss functions for *Mode-I* (red) and *Mode-II* (blue)

TABLE V
PARAMETERS OF THE SWITCHING LOSS FUNCTIONS FOR 3L-ANPC-VSC

	E_{on}			E_{off}			E_{rec}	
	Mode -I	*Mode -II*		*Mode -I*	*Mode -II*		*Mode -I*	*Mode -II*
a_0	0.24	0.18	b_0	0.11	0.15	c_0	0.42	0.38
a_1	2.35m	2.16m	b_1	3.68m	3.43m	c_1	0.96m	1.12m

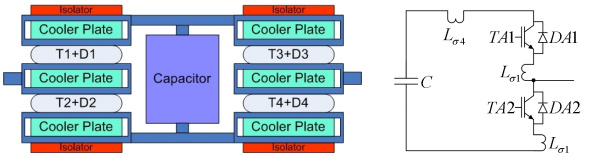

Fig. 15. Commutation paths in the simplified structure (left) and circuit (right) diagrams of 3L-HB-VSC

The power loss modeling approach can be illustrated by Fig. 16 for *TA1*'s E_{on} as follows. The switching voltage $V_{CE,TA1}$ is captured at the instant when d_{TA1} changes its state to '1'. At the next simulation instant (T_{sim} later), the switching current $I_{C,TA1}$ is captured and $E_{on,TA1}$ is calculated using (6) and Table V. For $E_{off,TA1}$ and $E_{rec,DA1}$, the same approach is followed. Similarly, the conduction losses are calculated for the simulation instants with non-zero IGBT/diode current and non-zero duty cycle of the corresponding IGBT/diode. Once the power loss figures for each simulation instant are obtained, they are averaged over an electrical cycle via (15) and (16). The averaged loss figures for each IGBT/diode are fed to the static thermal models. Without averaging, the loss figures can be directly applied to the dynamic thermal models.

$$P_{l,diode} = \frac{1}{T_e} \sum_{n=0}^{T_e/T_{sim}} (E_{rec}[n] + P_{con,diode}[n] \cdot T_{sim}) \quad (15)$$

$$P_{l,IGBT} = \frac{1}{T_e} \sum_{n=0}^{T_e/T_{sim}} (E_{on}[n] + E_{off}[n] + P_{con,IGBT}[n] \cdot T_{sim}) \quad (16)$$

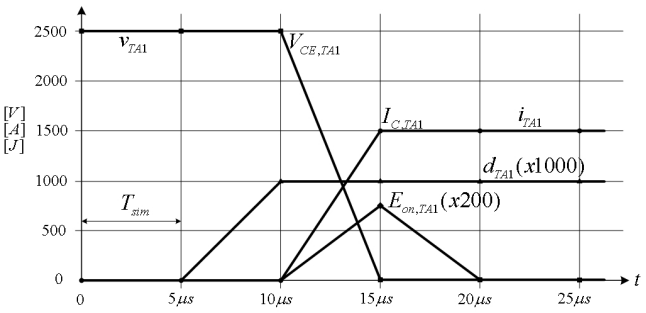

Fig. 16. Waveforms of *TA1* voltage v_{TA1}, current i_{TA1}, duty cycle d_{TA1}, turn-on energy loss $E_{on,TA1}$ during E_{on} calculation

IV. Static Thermal Modeling

Based on the physical placement of the press-pack devices (switch or IGBT-diode pair) and cooler plates shown in Fig. 7 and 15, the static thermal model is built as in Fig. 17 and applicable for both VSCs under study. Accounting for the power loss flow through each side of the press-pack device, the model represents the converter thermal behavior realistically. Table VI tabulates the thermal resistance values derived from the data supplied by the manufacturer [17], [18]. Moreover, the thermal model given in the figure can be mathematically represented for an IGBT-diode pair by (17)-(19) and the junction temperatures can be calculated by (20).

$$\begin{bmatrix} T_{j,T} \\ T_{j,D} \end{bmatrix} = A \begin{bmatrix} P_{l,T} \\ P_{l,D} \end{bmatrix} + B \begin{bmatrix} T_{ca,ck} \\ T_{ca,ea} \end{bmatrix} \tag{17}$$

$$\boldsymbol{T_{ca}} = C\boldsymbol{T_j} + DT_{com} \tag{18}$$

$$T_{com} = E\boldsymbol{T_{ca}} + FT_{amb} \tag{19}$$

$$\boldsymbol{T_j} = (I - B(I-DE)^{-1})^{-1}(A\boldsymbol{P_l} + B(I-DE)^{-1}DFT_{amb}) \tag{20}$$

where

$$A = \begin{bmatrix} \dfrac{R_{th,c}R_{th,e}}{R_{th,c}+R_{th,e}} & 0 \\ 0 & \dfrac{R_{th,k}R_{th,a}}{R_{th,k}+R_{th,a}} \end{bmatrix}, B = \begin{bmatrix} \dfrac{R_{th,e}}{R_{th,c}+R_{th,e}} & \dfrac{R_{th,c}}{R_{th,c}+R_{th,e}} \\ \dfrac{R_{th,a}}{R_{th,k}+R_{th,a}} & \dfrac{R_{th,k}}{R_{th,k}+R_{th,a}} \end{bmatrix},$$

$$C = \begin{bmatrix} \dfrac{R_{th,k}R_{th,co,ck}}{R_{th,CD1}} & \dfrac{R_{th,c}R_{th,co,ck}}{R_{th,CD1}} \\ \dfrac{R_{th,a}R_{th,co,ea}}{R_{th,CD2}} & \dfrac{R_{th,e}R_{th,co,ea}}{R_{th,CD2}} \end{bmatrix}, D = \begin{bmatrix} \dfrac{R_{th,c}R_{th,k}}{R_{th,CD1}} \\ \dfrac{R_{th,e}R_{th,a}}{R_{th,CD2}} \end{bmatrix},$$

$$E = \begin{bmatrix} \dfrac{6R_{th,cs}R_{th,co,ea}}{R_{th,EF}} & \dfrac{6R_{th,cs}R_{th,co,ck}}{R_{th,EF}} \end{bmatrix}, F = \dfrac{R_{th,co,ck}R_{th,co,ea}}{R_{th,EF}},$$

$$R_{th,CD1} = R_{th,c}R_{th,k} + R_{th,k}R_{th,co,ck} + R_{th,co,ck}R_{th,c},$$

$$R_{th,CD2} = R_{th,e}R_{th,a} + R_{th,a}R_{th,co,ea} + R_{th,co,ea}R_{th,e},$$

$$R_{th,EF} = R_{th,co,ck}R_{th,co,ea} + 6R_{th,cs}R_{th,co,ck} + 6R_{th,cs}R_{th,co,ea}.$$

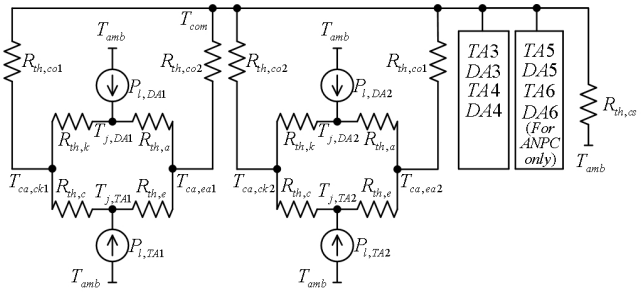

Fig. 17. Static thermal model of 3L-ANPC-VSC and 3L-HB-VSC

TABLE VI
Parameters of The Static Thermal Models

IGBT collector-side thermal resistance, $R_{th,c}$	13.9 K/kW
IGBT emitter-side thermal resistance, $R_{th,e}$	20.4 K/kW
Diode anode-side thermal resistance, $R_{th,a}$	42.6 K/kW
Diode cathode-side thermal resistance, $R_{th,k}$	23.2 K/kW
Cooler thermal res. for 2-cooler/1-device, $R_{th,co1}$	11.8 K/kW
Cooler thermal res. for 3-cooler/2-device, $R_{th,co2}$	13.6 K/kW
Cooling system thermal resistance, $R_{th,cs}$	0.25 K/kW
Water flow rate through cooler plates, v	10 *l*/min

V. Test Setup for Verification of The Power Loss and Static Thermal Models

The power loss and static thermal models can be verified via the single-phase full-scale 3L-ANPC-VSC (Fig. 18 and 19) with the parameters given in Table VII. In the VSC, single-phase power flow between the ANPC legs is formed by controlling the leg *b* as a voltage source and the leg *a* as a current source while the DC power supply compensates for only the system power loss [16]. For the operating conditions with various power flows, the simulated and measured case temperatures are compared for the model verification.

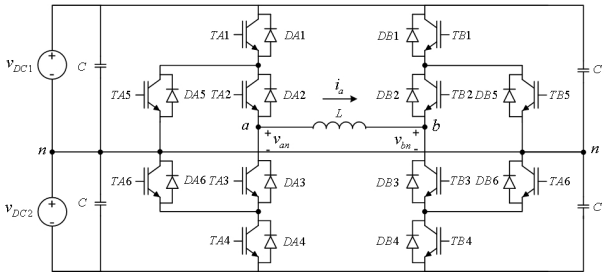

Fig. 18. Test setup power circuitry

TABLE VII
Parameters of The Test Setup

Phase-to-neutral output voltage	1.7kV$_{rms}$ (50Hz)
Power, P	2MW
DC bus voltage, V_{DC1}, V_{DC2}	2500V
Inductance, L	450μH (10%)
Capacitance, C	1.1mF
PWM frequency, f_{PWM}	1050Hz
Sampling time, T_S (double-update)	476.2μs
Dead time	10μs
IGBT-diode pair (Westcode)	T1800GB45A
Gate resistance, R_G	3Ω
Cooling plate (AlN-based)	XW180GN25A

Fig. 19. Test setup photo

VI. Simulation Results of The Three-Phase VSCs

The 6MW wind turbine grid connection with 3L-ANPC-VSC and 3L-HB-VSC are simulated via Ansoft-Simplorer using the parameters given in Table VIII and the parameters in the previous sections. The voltage and current output waveforms, which are almost identical for both VSCs, are given in Fig. 20 for P=6MW and PF=1 at the point of common coupling (PCC) with the grid. The switch current waveforms of the VSCs for this operating point illustrate the consecutive utilization of *Mode-I* and *Mode-II* (Fig. 21). The power loss distribution is illustrated in Fig. 22 for the three critical PFs of 1, 0.9 inductive (overexcited), and 0.9 capacitive (underexcited). It is observed that 3L-HB-VSC has almost homogenous power loss distribution among the IGBTs whereas the 3L-ANPC-VSC's power loss distribution can be more homogenized via a finer tuned mode sequence. It is seen that the diodes are quite lightly loaded due to high modulation index. Besides, the total power loss of each VSC varies around 45kW (η>0.99). The power losses are expected to be higher in practice because the simulation results are obtained with the power loss models built for $T_{j,max}$=25°C and the switching power losses tend to increase at higher junction temperatures.

TABLE VIII
Parameters of The Wind Turbine Connection System

Grid line-to-line voltage	10kV$_{rms}$ (50Hz)
Transformer turns-ratio, N (N_{inv}/N_{grid})	0.3 (1:3.33)
Turbine rated power, P_{out}	6MW
Power factor at PCC	0.9 *ind.* – 0.9 *cap.*
DC bus voltage, V_{DC}	2500V
Capacitance, C	1.1mF
Transformer leakage inductance (seen at converter side), L_{TR}	450µH (10%)
Grid inductance, L_S	2500µH (5%)
Filter inductor (at the grid side), L_F	5000µH (10%)
Filter capacitor (at the grid side), C_F	25µF (10%)
IGBT-diode pair (Westcode)	T1800GB45A
PWM frequency, f_{PWM}	1050Hz
Sampling time, T_S (double-update)	476.2µs
Deadtime, T_{dead}	10µs
Simulation time-step, T_{sim}	5µs

Corresponding to the power losses, the junction temperatures are shown in Fig. 23. For 3L-ANPC-VSC, there is a mismatch between the outer and inner IGBTs (TA1 and TA2) by almost 5°C for PF=1, however this mismatch can be diminished by means of a finer mode sequence. In contrast to 3L-ANPC-VSC, the temperature mismatch for 3L-HB-VSC is negligible. Also, the figure shows that the difference between the maximum junction temperatures $T_{j,max}$ is not more than 5°C.

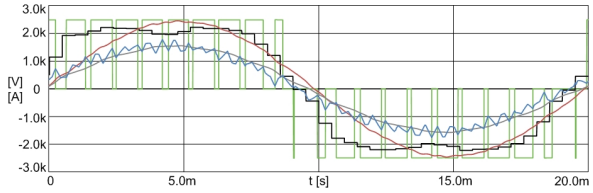

Fig. 20. The reference voltage v^*_a (black), inverter phase voltage v_a (green), inverter current i_a (blue), line voltage v_{sa} (red), and line current i_{sa} (grey) waveforms of phase-*a* for 3L-ANPC-VSC and 3L-HB-VSC at PF=1

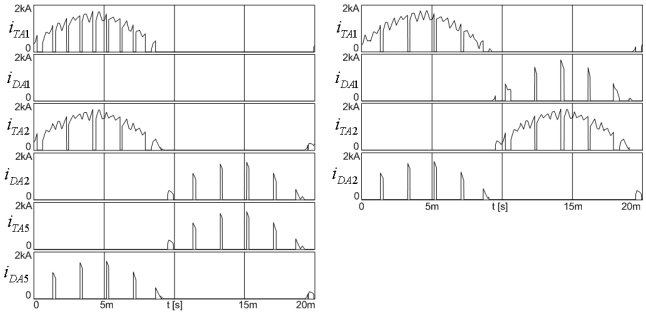

Fig. 21. IGBT (red) and diode (blue) current waveforms for the phase-*a* of 3L-ANPC-VSC (left) and 3L-HB-VSC (right) at PF=1

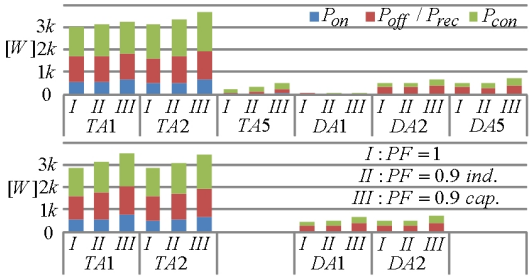

Fig. 22. Turn-on P_{on} (blue), turn-off/recovery P_{off}/P_{rec} (red), and conduction P_{con} (green) power losses of the phase-*a* IGBTs and diodes for 3L-ANPC-VSC (top) and 3L-HB-VSC (bottom)

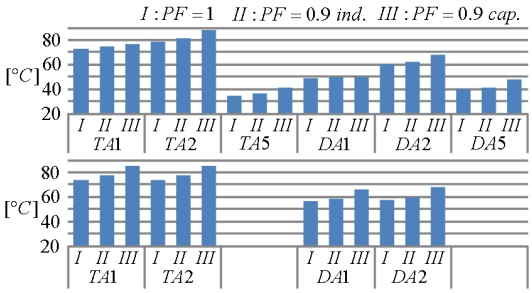

Fig. 23. Junction temperatures T_j of the phase-*a* IGBTs and diodes for 3L-ANPC-VSC (top) and 3L-HB-VSC (bottom)

VII. Discussions on Power Density and Reliability

The simulation results show that 3L-ANPC-VSC and 3L-HB-VSC under the given conditions perform very close electrically and thermally. Therefore, the power rating for both VSCs can be taken as the same. The 3L-ANPC-VSC thermal performance can be slightly enhanced by a finer mode sequence. For example, $T_{j,max}$ can be reduced from 78°C to 75°C at PF=1. Considering that both VSCs attain $T_{j,max}$=75-80°C at full-load, it can be stated that the IGBT lifetime due to junction temperature excursion, which is an indicator for reliability, is very close for each VSC.

Regarding semiconductors, IGBT gate drivers, and cooling plates, 3L-HB-VSC requires 33% fewer components than 3L-ANPC-VSC. According to the reliability calculation method using the failure rate λ of each individual VSC component [20], 3L-ANPC-VSC results in 50% more λ because the failure rates are summed up as given in (21) and (22) and therefore, 3L-HB-VSC has 50% more mean time between failures (MTBF=1/ λ).

$$\lambda_{ANPC} = 18\lambda_{IGBT/diode} + 18\lambda_{gatedriver} + 27\lambda_{cooler} \quad (21)$$

$$\lambda_{HB} = 12\lambda_{IGBT/diode} + 12\lambda_{gatedriver} + 18\lambda_{cooler} \quad (22)$$

Accounting only for the components mentioned above, 50% more power density of 3L-HB-VSC compared to 3L-ANPC-VSC (83.3kW/*l* vs. 55.5kW/*l* and assuming the power rating of 6MW) is expected. It should be noted that the power density of the experimental 3L-ANPC-VSC framed by the cabinet (Fig.19) is 7.5kW/*l*. It is expected that the 3L-HB-VSC framed by a similar cabinet (with the same capacitors) will have the approximate power density of 10kW/*l*, which means almost the 25% improvement.

VIII. Conclusion

In this study, the converter-structure based power loss and thermal models are developed for the medium voltage and full-scale 3L-ANPC-VSC and 3L-HB-VSC utilizing press-pack IGBT-diode pairs and interfacing a 6MW wind turbine to a medium voltage grid. For the experimental model verifications, a test setup with a single-phase full-scale 3L-ANPC-VSC is introduced. Using the power loss and thermal models, the switch junction temperatures are obtained on simulation and show that both converters perform very close thermally. Therefore, the VSCs' rated power and switch lifetimes are expected to be very close. Considering the counts and volumes of the press-pack devices, IGBT drivers, and cooling plates, the reliability and power density of 3L-HB-VSC is 50% better than 3L-ANPC-VSC. Including the VSC cabinet, the 3L-HB-VSC power density is expected to be 25% more than 3L-ANPC-VSC.

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