Grid Filter Design for a Multi-Megawatt Medium-Voltage Voltage Source Inverter

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***Abstract*—This paper describes the design procedure and performance of an LCL grid filter for a medium-voltage neutral point clamped (NPC) converter to be adopted for a multi-megawatt wind turbine. The unique filter design challenges in this application are driven by a combination of the medium voltage converter, a limited allowable switching frequency, component physical size and weight concerns, and the stringent limits for allowable injected current harmonics. Traditional design procedures of grid filters for lower power and higher switching frequency converters are not valid for a multi-megawatt filter connecting a medium-voltage converter switching at low frequency to the electric grid. This paper demonstrates a frequency domain model based approach to determine the optimum filter parameters that provide the necessary performance under all operating conditions given the necessary design constraints. To achieve this goal, new concepts such as virtual harmonic content and virtual filter losses are introduced. Moreover, a new passive damping technique that provides the necessary damping with low losses and very little degradation of the high-frequency attenuation is proposed.**

I. Introduction

Grid-connected converters are the interface for connecting distributed power generation systems to the new power system based on smart-grid technologies [1]. The most adopted approaches to reduce grid current harmonics injected by grid-connected converters are the use of tuned LC-filters, low-pass LCL-filters or a combination of the two [2]–[10]. In the first case, a group of "trap" filters acts on selective harmonics that need to be reduced. This solution has been adopted for line-commutated converters which exchange semi-square wave currents with the grid. The harmonic content of those currents is characterized by dominant low frequency harmonics and may be selectively filtered [11]. The LCL low pass filter acts on the whole harmonic spectrum and provides at least a 40 dB/dec attenuation above the resonance frequency. This solution has been typically adopted in the lower power range for grid connected pulse-width-modulated (PWM) converters because their harmonic spectrum exhibits no base band harmonics; only carrier band (or switching frequency) harmonics and groups of side band harmonics placed around multiples of the switching frequency [12]. If the switching frequency is high, the filter resonant frequency may be chosen low enough such that any significant side-band harmonics are above the resonant frequency; yet high enough that it will not present a challenge to the current control loop stability [13]–[16]. Hence the two filter types have been used for two different converter types, usually adopted for two different power levels; though some have suggested, using an LCL filter in conjunction with one or more tuned LC filters [6], [10].

Nowadays, the PWM converter has all but replaced the line-commutated converter in most applications, even those at high power and high voltage [17], [18]. But in these cases, the switching frequency is limited by the suitable semiconductor devices to about 1 kHz. Hence, for carrier-based modulation techniques, the first carrier band will be little more than one decade above the fundamental; making it next to impossible to place the resonant frequency above the control bandwidth but below significant side-band harmonics. Furthermore, the lower-frequency filter will necessarily be larger and more costly, placing an increased importance on the optimization process, a process that should also consider the impact of the filter component choice on the semiconductor rating, a dominant factor in multi-MW converters.

This paper discusses the grid filter design for a medium voltage multilevel VSI [18], [19] in a wind turbine application where volume and weight are critical [20], [21], but the process is equally valid for other applications relevant to the integration of distributed power generation systems, such as a large photovoltaic plant, wave energy system, STATCOM, FACTS and HVDC. The paper is laid out in the following manner: In Section II, the specific design constraints, such as the converter parameters and grid requirements are discussed. Section III presents the mathematical model for the LCL filter, where the forward-admittance transfer functions are regarded as the basis for the design of the filter. Section IV leads the reader through the design process; discussing the correlation between the design constraints and the filter parameters and demonstrating a step-by-step procedure to arrive at an optimal design. The final design is verified in Section V, through simulation results carried out over the range of power factors specified by the standards and recommendations valid for multi-MW wind turbines.

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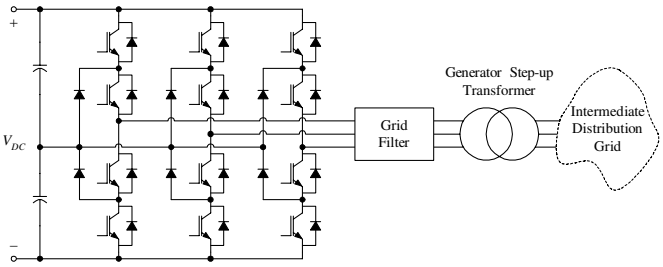

Fig. 1. Grid connected neutral point clamped voltage source inverter.

TABLE I
SYSTEM PER-UNIT BASE VALUES

Parameter		Formula	Value	
Power:	S_B	–	6.0	MVA
Voltage:	V_B	–	3.3	kV
Frequency:	f_B	–	50	Hz
Current:	I_B	$\frac{P_B}{\sqrt{3}V_B}$	1050	A
Radian freq.:	ω_B	$2\pi f_B$	314.16	rads/s
Impedance:	Z_B	$\frac{{V_B}^2}{P_B}$	1.815	Ω
Inductance:	L_B	$\frac{Z_B}{\omega_B}$	5.777	mH
Capacitance:	C_B	$\frac{1}{Z_B\omega_B}$	1754	μF

II. Filter Design Constraints

The relevant system schematic is shown in Fig. 1. The grid-side power converter is to be a neutral point clamped (NPC) VSI that is interfaced to the distribution network (which for the purposes of this paper, will be referred to as the *grid*) via a generator step-up transformer (GSU). The grid filter will be employed between the converter and the GSU.

The three-phase wind-turbine output is to be rated at 6.0 MVA, 3.3 kV line-to-line at 50 Hz. The converter must be capable of delivering full power at ± 0.9 power factor. Most of the analysis in this paper is presented on a per-unit (PU) basis. For the reader's reference, the corresponding base values are listed in Table I.

A. VDEW harmonic limits

It is a requirement that the wind-turbine meet the German VDEW standard for generators connected to a medium voltage network [22]. These limits are also described in a paper by Araujo et.al. [23]. Relevant to the filter design, this standard specifies limits for harmonic current injection based on the grid's short circuit ratio (SCR)–the ratio of grid's short-circuit current to the generator's rated current. Essentially, the base level harmonic limits are described by

$$I_{h_{\text{lim}}} = \frac{0.06}{h}\left(\frac{10\text{e}3}{V_B}\right)\left(\frac{P_B}{1\text{e}6}\right)\cdot \text{SCR},$$

which, for the per-unit definitions in Table I, can be written in per-unit as

$$I_{h_{\text{lim [PU]}}} = \frac{\sqrt{3}\,(0.0006)}{h}\cdot \text{SCR}. \qquad (1)$$

TABLE II
VDEW CURRENT LIMITS FOR ODD-INTEGER HARMONICS, $h \leq 25^{\text{TH}}$

h	$I_{h_{\text{lim}}}$/SCR	
	A/MVA @10 kVA	PU ($\times 10^{-3}$)
3, 5	0.115	1.992
7	0.082	1.420
9,11	0.052	0.900
13	0.038	0.658
15,17	0.022	0.381
19	0.018	0.312
21,23	0.012	0.208
25	0.010	0.173

At the present time, the limit for any integer harmonics above the 40th is relaxed to three times its base level. Below the 25th, the limits of the odd-ordered integer harmonics are relaxed according to Table II.

For the purpose of this paper, the SCR is assumed to be 20, which translates to a per-unit grid impedance of 5%. The VDEW current limits for the odd-ordered integer harmonics are indicated as the black line in Fig. 2. The grey dashed line indicates stricter limits for even harmonics and for non-integer harmonics below the 25th.

B. Converter Virtual Harmonic Spectrum

The harmonic voltage applied to the filter is of paramount importance in the filter design. The converter harmonic voltage depends on the converter topology and also on the modulation strategy. In this study, asymmetrical regular sampled (ASR) sine-triangle PWM with phase disposition (PD) carriers and 1/6 third-harmonic injection is employed. This method was chosen based on its popularity, suitability to digital implementation, high dc-link voltage utilization and superior harmonic performance [12]. For fixed frequency systems using this modulation technique, the best harmonic performance is achieved by setting the carrier frequency ω_c to an odd triplen multiple of the fundamental frequency, $\omega_c = \rho\ \omega_B$ where $\rho \in \{3, 9, 15, \ldots\}$. Such a carrier ratio restricts the resulting harmonics to odd non-triplen harmonic frequencies, thus avoiding the impact of the stricter limits for low-frequency even and non-integer harmonics of the VDEW standard, as indicated by the grey dashed line of Fig. 2.

Here, the converter will employ 4.5 kV, 1.3 kA integrated gate bipolar transistors (IGBTs). For this topology, the maximum switching frequency is limited to 1.2 kHz. The closest odd-triplen multiple of the fundamental frequency that does not exceed 1.2 kHz is 21, which results in a switching frequency of 1.05 kHz. Also as a result of this choice for switching device, the maximum total dc-link voltage is limited to approximately 5.5 kV (1.67 PU). In this application, the modulation index range will most likely be restricted from about 0.8 to 1.15. The inverter voltage harmonics were computed over the entire likely range of modulation index m_i and fundamental reference angle θ_1. With ASR PWM, the harmonics will differ with the angular offset of the reference

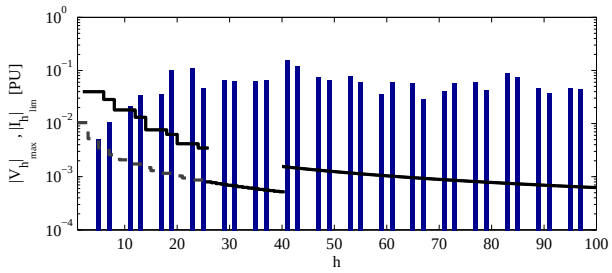

Fig. 2. Worst case per-unit voltage harmonic spectrum (ρ = 21, V_{DC}=1.67, $0.8 > m_i > 1.15$, $0 > \theta_1 > \pi/\rho$) plotted against the German VDEW harmonic current limits for generators connected to the medium-voltage network (SCR = 20). The dashed grey line indicates stricter limits for even and non-integer harmonics below the 25$^{\text{th}}$.

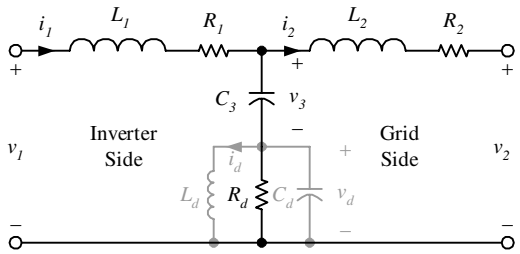

Fig. 3. Per-phase LCL filter schematic.

voltage. For a given modulation index, the harmonics begin to repeat once the angular offset of the reference voltage increases beyond one-half the carrier cycle. Hence, to ensure the worst case harmonics are realized for each modulation index, the fundamental reference angle must be swept over one half the carrier period (π/ρ). Then, for each harmonic, the worst-case voltage magnitude was extracted from the entire data set. This set of worst-case voltage harmonics was assembled into a *virtual* voltage harmonic spectrum (VVHS) which is shown in Fig. 2 for comparison purposes. The comparison of the *voltage* harmonics with the *current* limits in Fig. 2 gives an indication of the necessary filter admittance required to be able to meet the VDEW standard over all likely operating conditions. It should be emphasized that this spectrum is not for any particular modulation index or fundamental reference angle, but is a collection of the *worst-case* harmonic voltage magnitudes over the entire practical operating range. Its use, therefore, is restricted to comparisons in the frequency domain or to relative *virtual* comparisons such as the virtual loss computed in section IV-D where the compared data are all constructed from the VVHS. Since these harmonics never occur together as a group, no physically significant time-domain waveform can be re-constructed from the VVHS. Nonetheless, the VVHS is a valuable tool in gauging the filter performance over the entire operating range.

The VVHS in Fig. 2 suggests the use of tuned LC filters, which target individual harmonics, is largely impractical since, for such a low carrier frequency ratio ρ, the harmonics are relatively wide-band. The most restrictive VDEW current limits ($26 \leq \text{h} \leq 39$) are on the order of 10^{-3} PU, whereas the harmonic voltage at those frequencies is on the order of 10^{-1} PU. Hence, less than 1.5 decades above the fundamental frequency, the filter admittance must be less than 10^{-2} PU, clearly indicating the need for a filter with at least a second-order order admittance roll-off.

C. Converter Current Ripple

The LCL-filter design is not only constrained by the compliance with grid side specifications (harmonic limits) but also by converter-side ones. The initial converter specification, i.e. the topology and the voltage and current ratings, is devised to meet the output specification (i.e. power and harmonic performance). Then, the converter specification is adjusted, based on the availability of suitable semiconductors, since in the multi-megawatt medium-voltage realm, there are relatively few to choose from. Hence, the grid-filter design process is part of the exercise to determine whether the output specification can be met for the given converter specification.

For a given switching frequency and dc-link voltage, the ripple current, which contributes to the peak current flowing through the semiconductors, is a function of the filter admittance. However, the fundamental voltage drop across the filter, which contributes to the peak ac voltage that the converter must produce and is limited by the dc-link voltage, is a function of the filter impedance. Hence, the higher the filter impedance, the lower the ripple current but the higher the peak voltage the converter must produce. Therefore, for the given converter topology and choice of semiconductor, the maximum ripple current is limited by the semiconductor current rating (also considering semiconductor heating), whereas the minimum ripple current is limited by the dc-link voltage and thus, by the semiconductor voltage rating.

In an LCL-filter, the value of the maximum allowable current ripple has a deep impact on the cost and weight of the converter-side inductor. The current ripple dictates the choice of the magnetic material and the dimension and thickness of the lamination of the core in order to avoid magnetic saturation and to dissipate the heat produced by copper and core losses [24]. Hence, a lower current ripple would seem to lead to a smaller, cheaper converter-side inductor. However, the possible trade-off between the current limitation and voltage limitation is not yet understood. Hence, it is best to choose the maximum allowable current ripple as a starting point to get an idea of how close the design is to being voltage limited. Then, after the initial design process, when it is understood how much room there is for optimization, one can go back to try to minimize the current ripple. As previously mentioned, the semiconductor of choice is a 1.3 kA, 4.5 kV IGBT. The semiconductor current rating has been considered as starting point of the LCL-filter design and the consequent maximum ripple has been calculated to be limited to 25% of rated current (50% peak-to-peak).

III. LCL Filter Model

The LCL filter schematic is shown in Fig. 3, where v_1 and i_1 represent the inverter voltage and current, while v_2 and i_2 signify the grid voltage and current referred to the low-voltage side of the GSU. L_1 and R_1 represent the inverter side inductor and its equivalent series resistance (ESR), respectively. L_2 and

R_2 represent the combined impedance of the LCL grid side inductor, the GSU leakage and the grid; the later two of which are referred to the low-voltage side of the GSU. The shunt leg of the LCL filter is comprised of the filter capacitor C_3 in series with a damping impedance: the parallel combination of a resistor R_d, a capacitor C_d and an inductor L_d. In the initial analysis, C_d and L_d will be assumed to be zero and infinite, effectively removing them from the circuit. Their purpose is revisited later in Section IV-D. Furthermore, while it can be shown that the parallel combination of R_1 and R_2 also contribute to damping; as part of the main current path, their value is usually minimized to reduce losses. The presence of these small resistances slightly alter the model's effective pole-zero cancelation, but it does not significantly alter the shape or the attenuation of the transfer function. Thus they will be neglected in the analytical expressions, but are included in the computational analysis. For that purpose, it is assumed that the ESR is on the order of 0.5 % (0.005 pu), which is quite plausible for inductors at this power level.

The LCL filter can be considered as a two-port network with an "input" or inverter port and an "output" or grid port, each with a voltage and a current associated with it. The mathematical model of the LCL filter circuit can also be considered as a two-port network. However, from a modeling standpoint, the inputs should consist of the externally defined variables. In this case, the voltages are both defined, the grid voltage by the voltage and frequency at the point of common coupling and the inverter voltage by its dc-link, topology and modulation. Both the inverter current and grid current result from the relative phase and magnitude of these voltages, connected by the LCL filter. Hence, from a modeling point of view, the inverter and grid voltage are the inputs, and the inverter and grid currents are the outputs. The currents can be computed from the voltages via the state-space model for the LCL filter, in which the states are defined by the inductor currents and capacitor voltages.

A. LCL Filter State-Space Model

If L_d and C_d are neglected, the LCL filter model of Fig. 3 has three state variables, the inverter-side inductor current i_1, the grid-side inductor current i_2 and the shunt capacitor voltage v_3. Let $\mathbf{x}$ represent a vector of the circuit's state variables

$$\mathbf{x} = \begin{bmatrix} i_1 & i_2 & v_3 \end{bmatrix}^T . \tag{2}$$

As far as the rest of the system is concerned, the capacitor voltage is an internal state and is not considered an output. However, as it is an important design parameter, it too will be considered as an output of the model. Hence, the output vector will be equal to the state vector

$$\mathbf{y} = \mathbf{x} . \tag{3}$$

Let the input vector $\mathbf{u}$ be defined as

$$\mathbf{u} = \begin{bmatrix} v_1 & v_2 \end{bmatrix}^T , \tag{4}$$

where v_1 and v_2 represent the inverter and grid voltages, respectively. Carrying out the modeling process of writing the differential equations, converting to the frequency domain and solving for the states, the state-space model can be written as $\mathbf{Y}(s) = \mathbf{G}(s)\mathbf{U}(s)$, where $\mathbf{G}(s)$ is given as

$$\mathbf{G}(s) = \frac{\begin{bmatrix} \frac{1}{L_1}\left(s^2 + \frac{R_d}{L_2}s + \frac{1}{L_2C_3}\right) & \frac{-R_d}{L_1L_2}\left(s + \frac{1}{R_dC_3}\right) \\ \frac{R_d}{L_1L_2}\left(s + \frac{1}{R_dC_3}\right) & -\frac{1}{L_2}\left(s^2 + \frac{R_d}{L_1}s + \frac{1}{L_1C_3}\right) \\ \frac{1}{L_1C_3}s & \frac{1}{L_2C_3}s \end{bmatrix}}{s\left(s^2 + \frac{R_d}{L'} + \frac{1}{L'C_3}\right)} \tag{5}$$

where

$$L' = \frac{L_1L_2}{L_1 + L_2} . \tag{6}$$

The two components of the state-space model of most consequence in this analysis are the inverter voltage to inverter current transfer function which is referred to here as the *forward self-admittance* $Y_{11}(s)$, and the inverter voltage to grid current transfer function or the *forward trans-admittance* $Y_{21}(s)$, defined by (7) and (8) respectively

$$Y_{11}(s) = \frac{I_1(s)}{V_1(s)} = \frac{1}{L_1}\frac{s^2 + \frac{R_d}{L_2}s + \frac{1}{L_2C_3}}{s\left(s^2 + 2\zeta_p\omega_p\, s + {\omega_p}^2\right)} \tag{7}$$

$$Y_{21}(s) = \frac{I_2(s)}{V_1(s)} = \frac{R_d}{L_1L_2}\frac{s + \frac{1}{R_dC_3}}{s\left(s^2 + 2\zeta\omega_p\, s + {\omega_p}^2\right)} , \tag{8}$$

where the resonant pole frequency ω_p and the resonant pole damping factor ζ_p are defined as

$$\omega_p = \frac{1}{\sqrt{L'C_3}} \tag{9}$$

$$\zeta_p = \frac{R_d}{2}\sqrt{\frac{C_3}{L'}} . \tag{10}$$

The per-unit magnitude vs. frequency plot of both the forward admittance transfer functions is shown in Fig. 4. Attention is called to the effects of the individual parameters on the shape of each transfer function.

B. Forward Self-admittance

The forward self-admittance transfer function $Y_{11}(s)$ is shown as the thick solid line in Fig. 4. It has a set of complex-conjugate zeros, the corresponding frequency and damping factor of which are given by (11) and (12), respectively.

$$\omega_{z_{11}} = \frac{1}{\sqrt{L_2C_3}} = \omega_p\frac{1}{\sqrt{1+\frac{L_2}{L_1}}} \tag{11}$$

$$\zeta_{z_{11}} = \frac{R_d}{2}\sqrt{\frac{C_3}{L_2}} = \zeta_p\frac{1}{\sqrt{1+\frac{L_2}{L_1}}} \tag{12}$$

Since $\sqrt{1 + \frac{L_2}{L_1}}$ is always greater than 1, it will always be the case that $\omega_{z_{11}} < \omega_p$.

C. Forward Trans-admittance

In contrast to the self-admittance, the forward trans-admittance transfer function $Y_{21}(s)$ exhibits only a single zero;

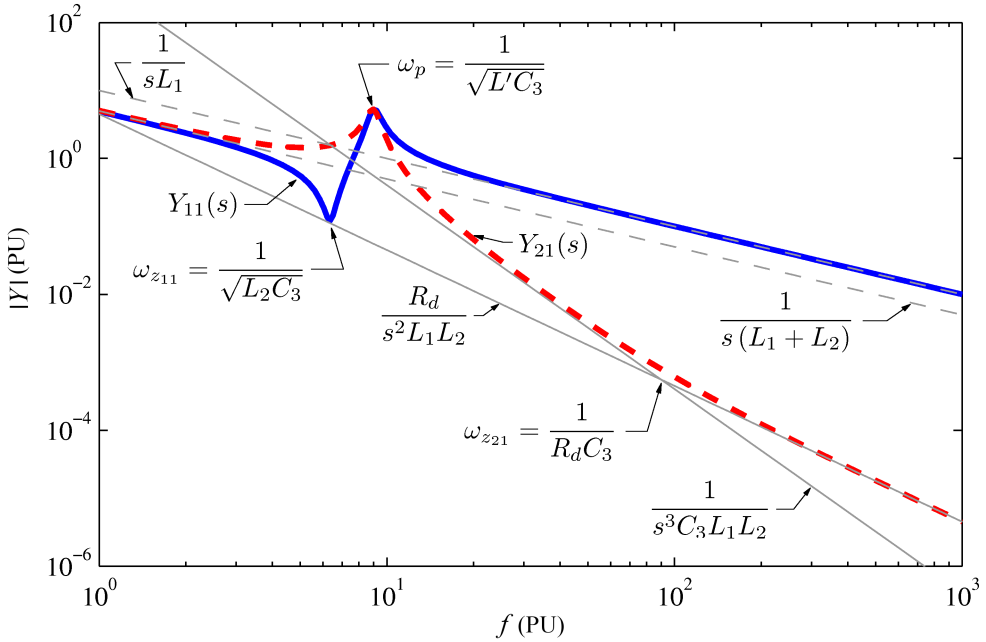

Fig. 4. LCL filter per-unit forward admittance transfer function magnitude plot; forward self-admittance $Y_{11}(s)$ (thick solid line) and forward trans-admittance $Y_{21}(s)$ (thick dashed line) versus normalized frequency, (L_1, L_2 = 0.1, ω_p = 9, ζ_p = 0.05). The relevant frequencies and asymptotes are indicated on the plot.

the frequency of which is determined by the RC time constant composed of the damping resistor and the shunt capacitor.

$$\omega_{z_{21}} = \frac{1}{\tau_{z_{21}}} = \frac{1}{R_dC_3} \ , \tag{13}$$

and from (9) and (10) it is not difficult to show that

$$\omega_{z_{21}} = \frac{\omega_p}{2\zeta_p} \ . \tag{14}$$

IV. LCL Filter Design Procedure

The traditional design procedure of an LCL grid filter is based on the following assumptions:

1) The filter in the low-frequency range (below resonant frequency) can be approximated as the sum of the overall inductance; and in the high frequency range, as the inverter side inductor alone. It is assumed that at high frequencies, the capacitor acts as a short circuit.
2) The resonance frequency is assumed to be well below that of the lowest significant low-frequency side-band harmonic.
3) The design is not constrained by the available dc-link voltage.

However, it has already been shown that for this case, the side-band harmonics are significant down to the 5$^{\text{th}}$ harmonic. Hence it is impossible to locate the resonant frequency well below this harmonic. The resonant pole must be located in the frequency range where significant side-band harmonics exist. Hence it is quite possible that a subset of harmonics will be amplified rather than attenuated, which may lead to higher than expected ripple current. In Section III, it was demonstrated that a resonant zero will exist below the resonant pole. Hence, it is likely that the control will have to accommodate necessary compensation. Finally, with a filter of this size and power-level, it is quite possible that the maximum dc-link voltage will play a role in limiting the filter size. The following subsections describe a step-by-step process by which an optimum filter design for such a system may be achieved.

A. Inverter-side Inductor Value

Since it is usually the case that the LCL resonant frequency is much lower than the switching frequency, it is common to consider the shunt capacitor impedance (or the entire shunt impedance) to be negligible at the frequencies at which significant harmonics exist. At these frequencies, the inverter will "see" only the impedance of L_1, so the rate of rise of the current is limited mainly by its value alone. Furthermore, because L_1 must endure these higher frequencies, it is typically a more expensive component than L_2 which is more of a line-frequency reactor. Consequently, the value of L_1 is usually minimized; selected specifically to limit the worst-case inverter ripple current to within a desired value.

An equation to compute the minimum inductor value for an LCL filter for a two-level inverter was given in [10] and developed in [25]. However, this equation is dependent on the converter topology and modulation algorithm used. Therefore, it is developed here explicitly for the three-level converter using ASR PWM, using essentially the same assumptions as in [25].

1) Initial Inductor Value Estimate: To determine the worst-case current ripple, one must consider the converter topology together with the modulation algorithm. Fig 5 shows as points in the hexagon, the 19 available phase voltage vectors for

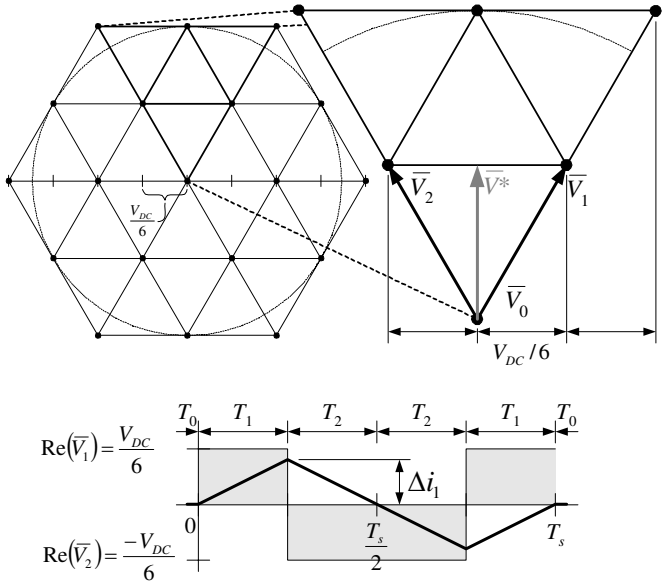

Fig. 5. Three-level NPC VSI voltage vectors showing case for worst-case current ripple

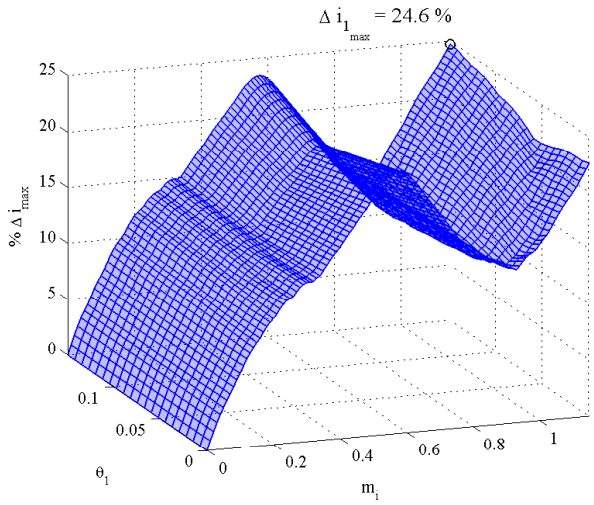

Fig. 6. Peak ripple current in percent rated vs. modulation index and fundamental angle for the LCL model (L_1, L_2 = 0.16, ω_p = 9, ζ_p = 0.05).

the NPC VSI. The instantaneous phase-to-neutral voltage of phase a, for example, is the projection of the selected voltage vector onto the horizontal axis. This instantaneous phase voltage can take on values from $-2V_{DC}/3$ to $+2V_{DC}/3$ in steps of $V_{DC}/6$. It is the purpose of the modulator to select the proper vectors in the proper sequence to produce, on average, the desired fundamental waveform.

It has been shown that ASR PWM with 3rd harmonic injection is almost identical to space vector modulation (SVM) in terms of voltage vector selection, except perhaps the placement (in time) of the zero voltage vector [12]. Both modulation strategies effectively resolve a voltage reference vector $\bar{V}^*$ into the three surrounding voltage vectors $\{\bar{V}_0, \bar{V}_1, \bar{V}_2\}$ such that they produce the desired voltage-second average. Using SVM to illustrate the process; at the beginning of the carrier cycle, the dwell times for each of the voltage vectors is computed such that

$$\bar{V}_0 \cdot T_0 + \bar{V}_1 \cdot T_1 + \bar{V}_2 \cdot T_2 = \bar{V}^* \frac{T_s}{2}. \tag{15}$$

Each of the voltage vectors is applied in turn (by means of the switch states) for the prescribed amount of time. Then, at $T_s/2$, a new volt-second average is computed for the second half of the switching cycle, in which the sequence of voltage vectors is then applied in reverse with the new set of computed dwell times.

The peak ripple current is defined by the difference between the peak volt-seconds and the average volt-seconds applied to the inductor over the switching period. The maximum will occur when the zero vector dwell time $T_0 = 0$ and the other two vector dwell times are equal $T_1 = T_2 = T_s/4$. This will be the case when the reference voltage vector is mid-way between $\bar{V}_1$ and $\bar{V}_2$, as illustrated in Fig 5, where the modulation index $m_i = 1/\sqrt{3}$ and the phase a voltage is crossing through zero. In this case, the peak volt-seconds applied to the inductor is

$$V_{L_1}\Delta_t = \frac{V_{DC}}{6}\frac{T_s}{4}, \tag{16}$$

while the average volt-seconds applied is zero. Assuming that the fundamental voltage is constant over the switching cycle, from (16) the minimum inductance value can be estimated by

$$L_{1_{\min}} = \frac{V_{DC}}{24\ \Delta i_{1_{\max}} f_s}\ , \tag{17}$$

where $\Delta i_{1_{\max}}$ is the maximum allowable peak ripple current and $f_s = 1/T_s$ is the switching frequency. For the per-unit values $V_{DC} = 1.67$, $\Delta i_{1_{\max}} = 0.25$ and $f_s = 21$, the estimated minimum value for $L_{1_{\min}} = 0.144$ PU (832 μH).

2) Refining the Inductor Value: The value of L_1 computed by (17) is based on the hypothesis outlined at the beginning of Section IV-A. Since the resonance and switching frequencies are particularly near it is worth verifying the effect of L_1 on Δi_1 using the full-order model of the LCL-filter (assuming ζ_p = 0.05, ω_p = 9 and L_1/L_2 = 1). Then one can apply the previously computed voltage harmonic spectrum to compute the ripple current for the LCL filter using the full state-space model. Because the ripple current is a time-domain phenomenon, the VVHS cannot be used. Instead, the current waveform is reconstructed from the complete voltage harmonic spectrum for each value of modulation index m_i and fundamental angle θ_1, together with the nominal grid voltage. This exercise indicates that for these conditions, the relation in (17) slightly underestimates the value of $L_{1_{\min}}$. Instead, a larger value of $L_1 = 0.16$ PU (924 μH) is required to limit the worst-case current ripple to below 25% (see Fig. 6), and it is not the case that this occurs at $m_i = 1/\sqrt{3}$, but rather at the maximum modulation index $m_i = 1.15$.

This seems to suggest that for the case where the switching frequency is low, a more complete model of the LCL filter should be used in conjunction with the voltage harmonic spectrum to refine the value of L_1, using (17) (or a similar relation developed for the particular topology and modulation algorithm) as a starting point. It is not difficult to estimate

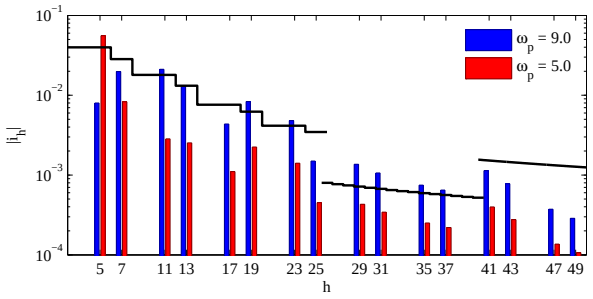

Fig. 7. Maximum per-unit grid current harmonics over the modulation index range $0.8 < m_i < 1.15$ (L_1, L_2 = 0.16, ζ_p = 0.05, ω_p = 9 and 5), compared to the German VDEW per-unit harmonic current injection limits (SCR = 20).

the necessary LCL parameters to a reasonable degree of accuracy to effectively refine the value of L_1. One may elect, however, to use a larger margin than the 0.4% (the difference between the computed maximum current ripple and the stated maximum limit) that is demonstrated here.

B. Resonant Pole Frequency

As mentioned before, it not possible to locate the resonant pole frequency well below the switching frequency or well above the control bandwidth. In this case, the placement is dominated by the need to achieve the necessary attenuation, but should be as high as possible to minimize the consequences on the control.

In Section IV-A, preliminary parameters for the LCL filter were selected; ω_p = 9, ζ_p = 0.05, L_1/L_2 = 1. The value of L_1 = 0.16 PU was determined as the minimum necessary to limit the current ripple to within the specified value. The current task is to see whether this LCL filter meets the specified grid harmonic limits over the entire operating range. This can be immediately accomplished by applying the VVHS (see Section II-B) to the forward trans-admittance transfer function (8).

If the resulting current harmonic spectrum does not meet the specification, then it will be necessary to reduce the trans-admittance transfer function. Equation (8) suggests that to decrease the trans-admittance, one may increase one or both of the inductor values and/or reduce the resonant pole frequency. But, because L_1 tends to be a more expensive component, increasing its value is avoided. One may elect to increase L_2, but as the resonant pole frequency has a squared effect, a slight shift in the pole frequency can have a significant effect on the trans-admittance. Furthermore, increasing L_2 can have other consequences, which is discussed in more detail in Section IV-C.

At this stage in the design, it is prudent to determine the resonant frequency at which the filter meets the specified harmonic limits. Fig. 7 indicates that the LCL filter with the parameters listed above does not meet the VDEW standard. It was necessary to reduce the resonant frequency to ω_p = 5, before all harmonics (except the 5th) met the standard with sufficient margin. The 5th harmonic fails, but this is because it coincides with the resonant frequency and, for the moment, there is almost no damping. However, the damping will not remain so low and is dealt with in Section IV-D.

C. Grid-side Inductor and Shunt Capacitor Selection

For a specific value of ω_p, an increase (or decrease) in L_2 must be accompanied by a corresponding decrease (or increase) in C_3. The possible range of values of these two components is evaluated with respect to their effect on the inverter voltage, the inverter losses and the component size, which is also related to component weight and cost.

1) Inverter voltage: As mentioned before, the VDEW limits in this paper are based on an assumed SCR of 20. This translates to a grid impedance of 5%. Furthermore, the filter is connected to the grid through the GSU. This transformer will have some leakage inductance associated with it as well; a typical value is somewhere around 5%. Hence, it is assumed that the minimum effective grid side inductance is 10%.

Now it remains to determine the upper bound. A typical power specification usually consists of a volt-amp (VA) rating accompanied by a power factor range. For example, it is common to require full-power operation to $\pm$0.9 power factor. One must ensure that the full operating range is attainable. The phasor relationships between the grid voltage and current and that of the inverter can be used to understand the effect of L_2 and C_3 in this regard. The phasor equations for the lossless LCL filter are given in (18) and (19).

$$\begin{aligned}\widetilde{V}_1 = &\left[1 - \tfrac{L_1}{L'}\left(\tfrac{\omega}{\omega_p}\right)^2\right]\widetilde{V}_2 \\ &+ j\omega\left(L_1 + L_2\right)\left[1 - \left(\tfrac{\omega}{\omega_p}\right)^2\right]\widetilde{I}_2\end{aligned} \tag{18}$$

$$\widetilde{I}_1 = \left[1 - \tfrac{L_2}{L'}\left(\tfrac{\omega}{\omega_p}\right)^2\right]\widetilde{I}_2 + j\frac{1}{\omega L'}\left(\tfrac{\omega}{\omega_p}\right)^2\widetilde{V}_2 \tag{19}$$

Equation (18) indicates that for the given values of L_1 and ω_p, and assuming the grid voltage magnitude $|V_2|$ does not vary significantly, the inverter voltage magnitude $|V_1|$ necessary to provide a given output power $S_2 = \widetilde{V}_2\widetilde{I}_2^*$ is directly proportional to the value of L_2.

The dc-link voltage of 1.67 PU is limited by the structure of the inverter and the voltage rating of the semiconductors. Furthermore, with ASR PWM modulation with 3rd harmonic injection, the maximum modulation index without going into over-modulation is 1.15. Assuming over-modulation is to be avoided in the steady-state, these parameters suggest that the maximum fundamental inverter voltage magnitude is limited to 1.174 PU

$$|V_1|_{\max} = m_{i_{\max}}\left(\frac{V_{DC_{\max}}}{2}\sqrt{\frac{3}{2}}\right) = 1.174.$$

Using (18) the fundamental inverter voltage magnitude $|V_1|$ required for each operating point over the full specified output power range was computed for a range of values of L_2. The results, shown in Fig. 8, suggest that for V_{DC} = 1.67 PU, L_1 = 0.16 PU and ω_p = 5, the grid side inductance must be below 0.25 PU to avoid over-modulation; limited by the case where the inverter is providing maximum output power at 0.9 PF sourcing.

Hence, the grid side inductance must be selected somewhere between 0.1 and 0.25 PU. This value is including the grid impedance and the transformer leakage inductance.

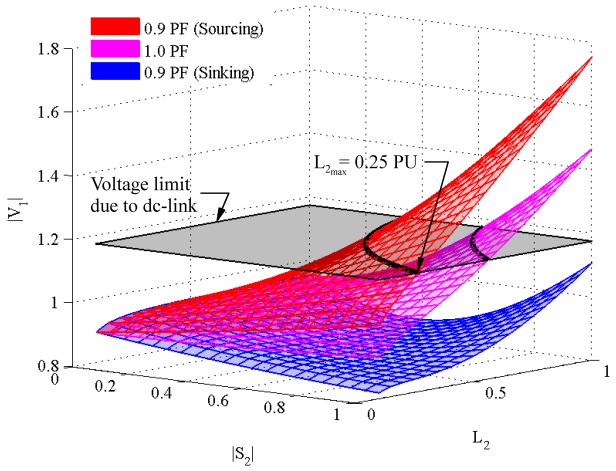

Fig. 8. Per-unit inverter voltage magnitude over the full specified output power range ($0 \leq S_2 \leq 1.0$ PU, ± 0.9 PF) vs. L_2, shown against the limit imposed by the maximum DC link voltage (L_1 = 0.16, ω_p = 5.0, V_{DC} = 1.67, $m_{i_{\max}}$ = 1.15).

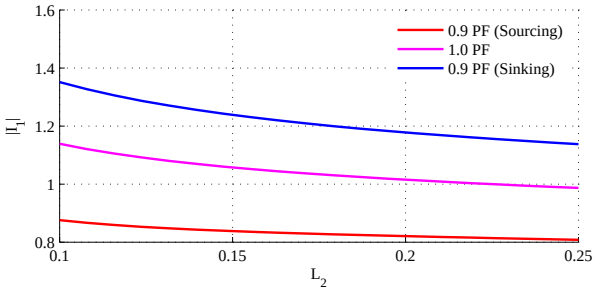

Fig. 9. Per-unit inverter current magnitude at full rated power over the range of specified power factor ($S_2 = 1.0$ PU, ± 0.9 PF) vs. L_2.

2) Inverter losses: The higher the inverter current necessary to supply the specified grid power, the greater the inverter losses. The trade-off between L_2 and C_3 can have a significant effect on the amount of reactive power that the inverter must source over the specified output power range. The phasor relationship in (19) can be used to calculate the corresponding effect on the inverter current. For a given ω_p, varying the value of L_2 (and thus L' as well) reflects the tradeoff between L_2 and C_3.

The magnitude of the inverter current necessary to supply the maximum specified grid power over the range of possible values of L_2 is shown in Fig. 9. The figure suggests that increasing the value of L_2 decreases the maximum inverter current necessary to provide the maximum output power. The current magnitude is highest when the power factor is 0.9 PF sinking, but the trend is the same over the entire power factor range.

3) Filter component size: Finally, it is worthwhile to investigate the relative size and weight of the filter due to the L_2-C_3 trade-off. The total energy stored in a component can be used as a relative measure of its size. Since the current through and voltage across each component can be computed from the state-space model, it is a simple matter to compute the maximum energy stored in the component per the following two relations,

$$\begin{aligned} U_{L_{\max}} &= \tfrac{1}{2} L I_{\max}^2 \\ U_{C_{\max}} &= \tfrac{1}{2} C V_{\max}^2 \ . \end{aligned} \tag{20}$$

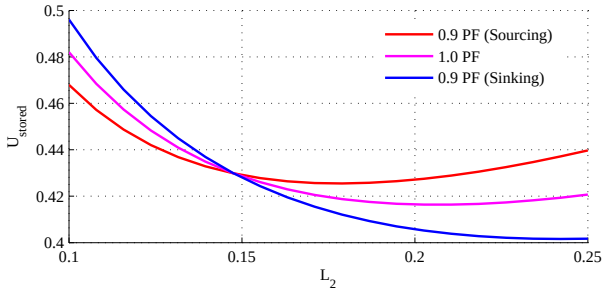

Fig. 10. Total per-unit stored energy in filter at maximum output power over the possible range of L_2.

The aggregate total energy stored in the filter components at the maximum output power over the specified power factor range and possible values of L_2 is shown in Fig. 10. This figure suggests that after L_2 increases past about 0.18 PU, the total energy stored in the filter begins to increase, suggesting a larger filter. Although not discernable from this figure, as the value of L_2 increases, the energy stored in both L_1 and C_3 continues to decrease. It is the increased energy stored in L_2 that is responsible for the overall increase in total stored energy. However, the portion of L_2 made up of the GSU leakage inductance and referred grid impedance should be taken into account since these will not contribute to the filter volume. For the purpose of this investigation, a value of L_2 = 0.2 PU (1.2 mH) was chosen as a compromise between filter volume and inverter losses. Then, for a resonant frequency of ω_p = 5 PU (250 Hz), a capacitor value C_3 = 0.45 PU ($\simeq$790 μF) results.

D. Passive Damping

High-order filters, like LCL-filters, have more state variables than the simple L-filter. The dynamics associated with these states may become unstable if they are triggered by a disturbance or by a sudden variation of the operating point; such as a change in the power transferred by the converter to the grid through the filter or a change in the grid voltage due to a voltage sag caused by a fault. The proper damping of these dynamics can be achieved by modifying the filter structure with the addition of passive elements or by acting on the parameters or on the structure of the controller that manages the power converter. The first option is referred to as passive damping while the second is referred to as active damping. Passive damping causes a decrease of the overall system efficiency because of the associated losses that are partly caused by the low frequency harmonics (fundamental and undesired pollution) present in the state variables and partly by the switching frequency harmonics [4], [5]. Moreover, passive damping reduces the filter effectiveness since it is very difficult to insert the damping in a selective way; only at those frequencies where the system is resonating due to a lack of impedance.

As a consequence, the passive damping is always present and the filter attenuation at the switching frequency and above is compromised [5]. Active damping consists of modifying the controller parameters or the controller structure [13], [26]; either cutting the resonance peak and/or providing a phase-lead around the resonance frequency range [27]. Active damping methods are more selective in their action, they do not produce losses but they are also more sensitive to parameter uncertainties [28], [29]. Moreover the possibility to control the potential unstable dynamics is limited by the controller bandwidth which is dependent on the controller sampling frequency. In [13] it has been demonstrated that the sampling frequency should be at least double the filter's resonance frequency to effectively perform active damping.

This paper only addresses issues related to the design of the filter, while control aspects are not treated. Hence only passive damping solutions are investigated here. Moreover, the selection of the best passive damping solution [10] is a very challenging task since the resonance frequency is very low and the damping has not only influence on the stability and on the filter attenuation, but also on the amplitude of the harmonics around the resonance frequency. This translates to an effect on the overall harmonic content and on the losses that those harmonics can cause.

The VVHS is used to compare three possible passive damping solutions; one defined as total damping and the other two as unique selective damping methods. *Total damping* consists simply of the damping resistor R_d in series with the shunt capacitor. It can be shown that resistances in series or parallel with any of the reactive filter elements contribute to damping in the same way as R_d; they provide damping over all the frequencies; hence, also where it is unnecessary [5]. Much of the work in this paper has considered only the effect of the series damping of the LCL-filter capacitor by R_d since losses would be quite high for resistors in series with the inductors.

The two selective damping solutions, differentiated here as *selective low-pass* damping and *selective resonant* damping, attempt to emulate with passive elements the selective effect of active damping. In the case of low-pass selective damping, an inductor is inserted in parallel with the damping resistor (indicated in grey as L_d in Fig. 3) in order to inhibit low-frequency losses where the inductor will act as a short circuit. It has been shown that the passive damping losses at low frequency can be as much as half of the overall filter losses [5]. Selective resonant damping, which places a parallel RLC circuit in series with C_3, seeks not only to mitigate the low frequency losses as mentioned above, but also to reduce the losses at the switching frequency and improve the high-frequency attenuation by again shorting the damping resistor R_d through the damping capacitor C_d at high frequencies.

The values of L_1, L_2 and C_3 were taken from the prior analysis and are set to 0.16, 0.2 and 0.45, respectively. In the case of the total damping method, the resistor value R_d was varied to achieve the variation of the damping coefficient according to (10). A value of ζ_p = 0.3, corresponding to a value of R_d = 0.267 PU (0.484 Ω) was chosen as a good compromise between damping and attenuation.

Then, for the two selective damping methods, the damping resistor R_d was set to that same value, and the other damping components were varied to achieve the variation in the damping coefficient. In the case of the selective low-pass solution, a value of L_d = 0.21 PU (1.2 mH) corresponded to an effective damping coefficient of $\zeta_p = 0.3$. In the case of the selective resonant solution, the damping circuit resonant frequency was constrained to be equal to the resonant frequency ω_p of the LCL filter. The value of the damping inductor was varied in conjunction with the damping capacitor C_d to achieve the variation in damping coefficient as determined by the ratio of the resonant pole's real component to its frequency. The values of L_d = 0.067 PU (389 μH) and C_d = 0.595 PU (1000 μF) resulted in an effective damping coefficient of ζ_p = 0.3.

Fig. 11 shows the bode plot for the forward trans-admittance $Y_{21}(s)$ (inverter voltage to grid current transfer function) for the three different damping solutions, all at $\zeta_p = 0.3$. Also shown, for comparison purposes, is the filter with almost no damping ($\zeta_p = 0.01$). All three damping solutions compromise the filter's high-frequency attenuation, but the selective resonant damping at least retains the third-order admittance roll-off characteristic of the undamped LCL filter.

Then, to determine the relative effect of the different damping solutions on the filter losses, the VVHS as defined in Section II-B was applied to each filter model and the losses were computed over the range of damping factor from 0.01 to 0.3. As was stated in Section II-B, the VVHS comprises the worst-case harmonic spectrum over the entire feasible operating range and does not indicate the true harmonic spectrum at any one operating point. Therefore the losses computed by the VVHS represent only a comparison of the losses (or virtual losses) between the damping methods and do not represent actual losses. The virtual losses vs. damping factor are shown in Fig. 12.

The bode plot for the total damping and the selective low-pass damping are very similar since, in both cases, the same value of R_d is used (0.267 PU) and the effect of L_d is only to by-pass the damping resistor at low frequencies. As Fig. 12 shows, this significantly reduces the losses incurred in the damping resistor, but results in the same high frequency attenuation degradation as the total damping solution. The filter with selective resonant damping also by-passes the damping resistor at the higher frequencies, resulting in even lower losses as well as improved high-frequency attenuation.

The resulting current harmonics from the application of the VVHS to each of the filter models is shown in Fig. 13. It demonstrates that for a damping coefficient of ζ_p = 0.3, the selective resonant solution is the only one that meets the VDEW limits for harmonic current injection. Of course, this solution requires extra damping components (L_d and C_d), but due to the relatively small current and voltage applied to the devices, one would not expect them to significantly affect the overall filter volume.

The performance of the LCL filter design with selective damping was computed using the VVHS as the input while the value of all components was swept between $\pm 10\%$ of nominal. Fig. 14 shows the variation in the bode plot for the forward trans-admittance transfer function and Fig. 15 shows the worst case current harmonics over the entire parameter

TABLE III
FINAL FILTER COMPONENT VALUES AND RATINGS

Component	PU Value	PU Rating	
		Voltage	Current
L_1	0.16	0.11	1.19
L_2	0.20	0.12	1.00
C_3	0.45	0.65	0.51
R_d	0.267	0.02	0.13
L_d	0.067	0.02	0.51
C_d	0.595	0.02	0.02

variation. The only harmonic which fails is the 29th harmonic and it was determined that this occurred at the point where all the parameter values were at -10% of nominal, a highly unlikely case. A further investigation showed that if the major components (L_1, L_2 and C_3) are held to within $\pm 5\%$ the limits are still met. Over the entire $\pm 10\%$ parameter variation the damping coefficient, nominally set to 0.3, varied between 0.21 to 0.37.

V. VERIFICATION OF FILTER EFFECTIVENESS

The final parameter values and ratings for the LCL circuit are given in Table III. The damping circuit parameters L_d, C_d and R_d result in a filter damping coefficient ζ_p of 0.3. It now remains to verify the design at the specification limits. In the simulation, the inverter is assumed lossless with a constant dc-link voltage of 1.67 PU (5.5 kV) and the primary referred grid voltage (at the filter output) is assumed to be a pure 50 Hz sinusoid at 3.3 kV line-to-line. The simulation was repeated for the maximum output power $|S_2|$ = 6.0 MVA (1 PU) at three power factor settings; 0.9 PF sourcing, 1.0 PF and 0.9 PF sinking. In each case, the resulting harmonic spectrum is compared to the German VDEW harmonic current injection limits (v_B = 3.3 kV, P_B = 6 MVA, SCR = 20).

Fig. 16 shows the simulated results at maximum leading

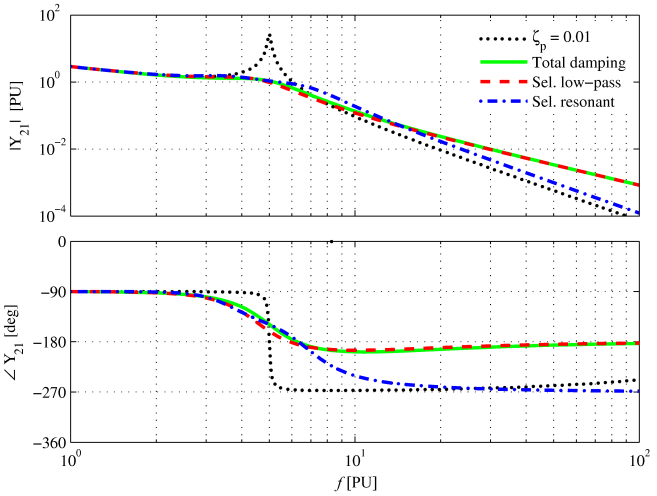

Fig. 11. Bode plot of the forward trans-admittance $Y_{21}(s)$ for the three damping solutions at $\zeta_p = 0.3$

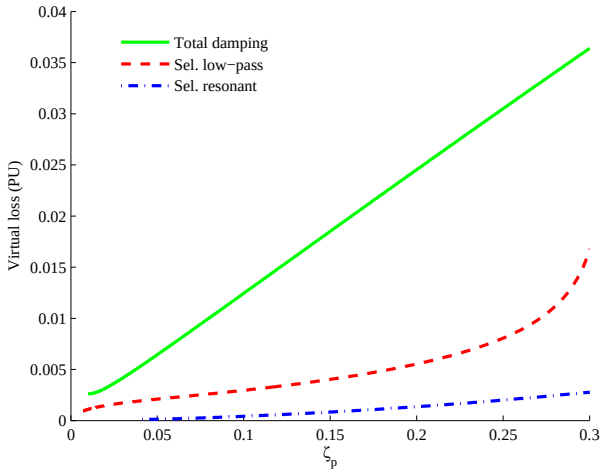

Fig. 12. Virtual losses versus the damping coefficient, ζ_p.

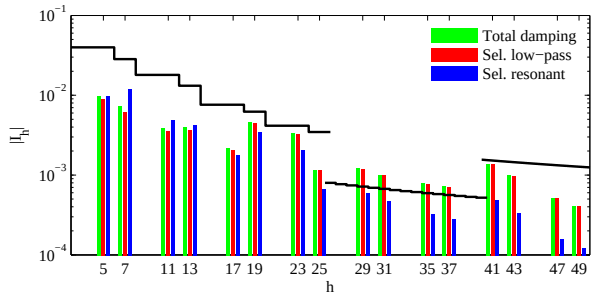

Fig. 13. Worst-case grid current harmonics for the three damping solutions at $\zeta_p = 0.3$ as compared to the VDEW standard limits

(sourcing) power factor. One will note that for this operating condition, the modulation index is near the maximum at $m_i = 1.10$. Hence, one would expect the worst case ripple current to occur here since in section IV-A, Fig. 6, it was shown that the maximum ripple current occurs at the maximum modulation index. The resulting peak current ripple is approximately 20% (40% peak-to-peak). The losses in the damping resistor at these conditions was computed to be about 9.5 kW per phase (0.005 PU).

Figs. 17 and 18 show similar results for unity and 0.9 power factor lagging (or sinking), respectively. The damping resistor losses in each of these cases was 7.8 kW (0.004 PU) and 6.5 kW (0.003 PU), respectively.

It may be tempting to think that since the design meets the standards by such margin in these three cases, the filter may be over designed. However, these simulations show only three specific cases. This demonstrates the benefit of designing the filter using the virtual voltage harmonic spectrum. Over the entire likely operating range, the margins will not be so large. Figs. 13 and 15, which show the harmonics based on the VVHS are better indicators in this regard.

VI. CONCLUSIONS

This paper has demonstrated a design procedure for a medium-voltage multi-megawatt grid connected LCL filter.

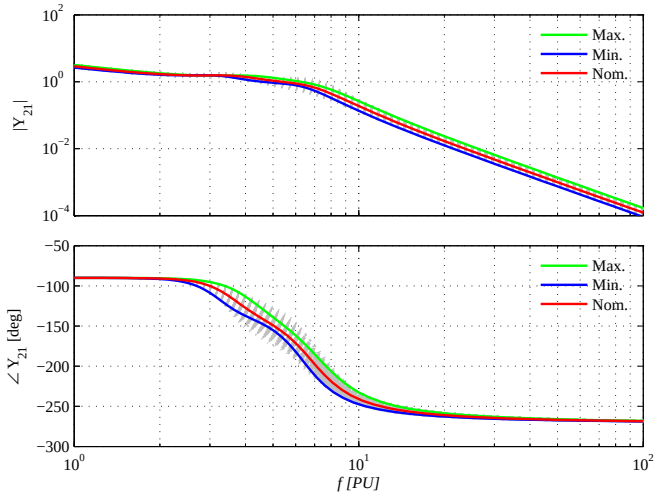

Fig. 14. Bode plots for LCL filter with resonant damping for all parameters swept within ±10% of nominal.

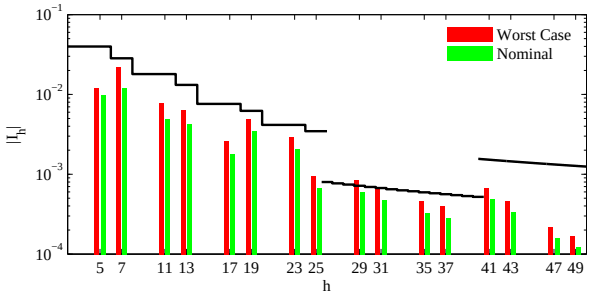

Fig. 15. Worst-case grid current harmonics over ±10% parameter variation as compared to the VDEW standard limits.

The procedure sought to ensure that the full specified output power and the limits for maximum injected harmonic currents and peak inverter ripple current could be met given the constraints on the inverter dc-link voltage and maximum switching frequency. The procedure centered on minimizing the most costly component, the inverter side inductor; and attempted to achieve the smallest, lightest, most-efficient design by placing the resonant frequency as high as possible, minimizing the maximum stored energy and the maximum inverter current and selecting the most efficient damping circuit.

The original contributions of the paper include: 1) The concept of the virtual voltage harmonic spectrum (VVHS), simplifying the filter performance assessment over the entire operating range. 2) The demonstration that the often cited method for computing the value of the inverter side inductor may underestimate the necessary value when the resonant frequency must be located where significant harmonics exist. 3) The idea of "selective resonant" damping which has been shown to both reduce losses and improve attenuation over the other damping methods discussed.

The performance of the final filter design was verified through simulation.

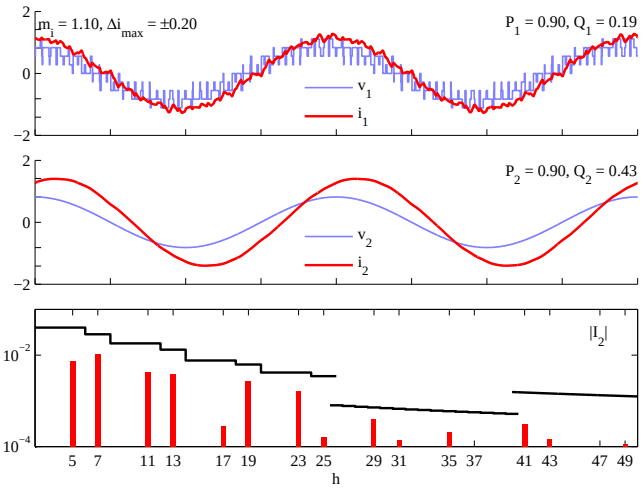

Fig. 16. Simulated converter waveforms for $S_2 = 1.0$ PU, 0.9 PF sourcing. Top: inverter voltage and current, Mid: grid voltage and current, Bot: grid current harmonics vs. VDEW standard.

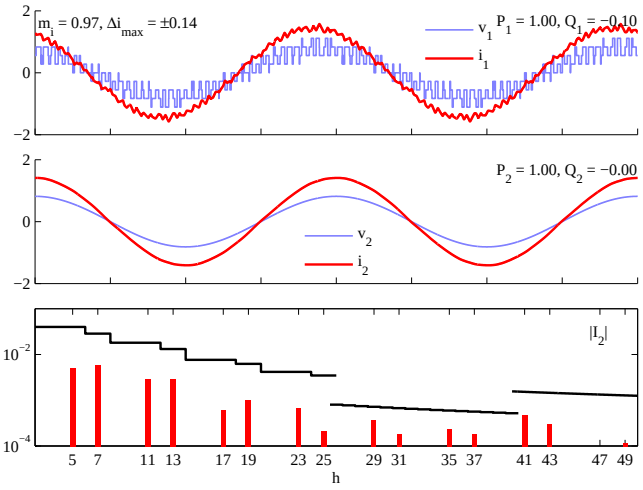

Fig. 17. Simulated converter waveforms for $S_2 = 1.0$ PU, 1.0 PF. Top: inverter voltage and current, Mid: grid voltage and current, Bot: grid current harmonics vs. VDEW standard.

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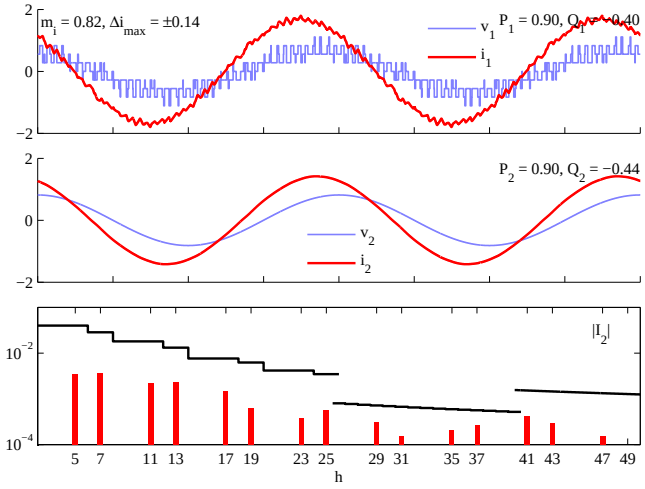

Fig. 18. Simulated converter waveforms for $S_2 = 1.0$ PU, 0.9 PF sinking. Top: inverter voltage and current, Mid: grid voltage and current, Bot: grid current harmonics vs. VDEW standard.

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