Providing an UWB-IR BAN wireless communications network and its application to design a low power transceiver in CMOS technology.

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I. Introduction

Ultra Wide-Band (UWB) communication techniques have received increasing attention since United States Federal Communications Commission (FCC) adopted a “First Report and Order” [1] in 2002. Unfortunately the regulations that appeared a few years latter didn't have the same level of commitment and had much tighter constraints. The FCC part. 15 power spectral density limitation is depicted in Fig. 1.

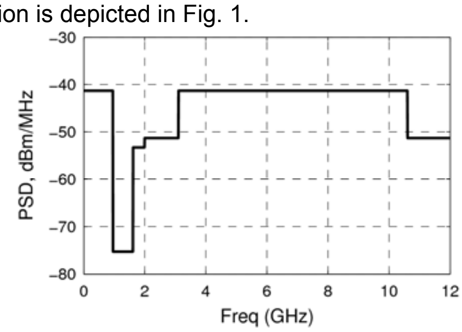


Figure 1. UWB Spectral Mask FCC part 15 regulations.

Although the word-wide common bandwidth is quite scarce (7.25 to 8.5 GHz), UWB still has its niche applications. Impulse Radio (IR) implementation of UWB systems has very interesting features such as low complexity, low power consumption, low cost, high data-rate, and the ability of coexistence with other radio systems [2].

II. UWB transceiver architecture

IR-UWB transceivers can be implemented with a coherent and non-coherent architecture. The non-coherent architecture uses a simpler transmitter and receiver, but has worse performance in both terms of datarate and immunity to noise and interferences. Thus, the coherent transceiver was chosen for the transceiver architecture.

The UWB transceiver was designed to provide a data link for medium to high speed datarates at low power consumption.

II.A. Receiver

To implement the receiver a full digital solution (known as *software radio*) can be used. As shown in Fig. 1a, the software radio receiver implementation uses a analog-to-digital converter (ADC) to sample the input RF signal and post-process it in the digital domain. Although this implementation is extremely flexible and the receiver can be reconfigured even on-line, the ADC requirements (sampling frequency) and the power consumption are very high. Therefore an alternative solution with reduced requirements is depicted in Fig. 1b, where a front-end mixer is used to reduce the sampling frequency of the ADC. This solution still has very high power consumption requirements. Therefore to implement the receiver with low power consumption an analog architecture is used, as shown in Fig. 1c.

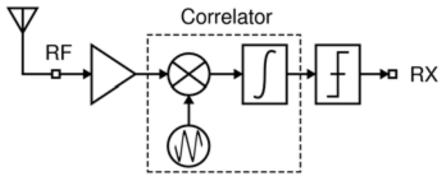


Figure 2. Architecture for the IR-UWB correlator-based receiver.

For the particular case of an IR-UWB receiver, this latter architecture is slightly changed into the one presented in Fig. 2. This receiver architecture is based on a correlator. The correlator consists of a mixer, a template generator and an integrator.

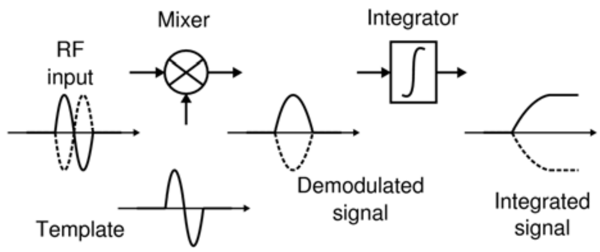
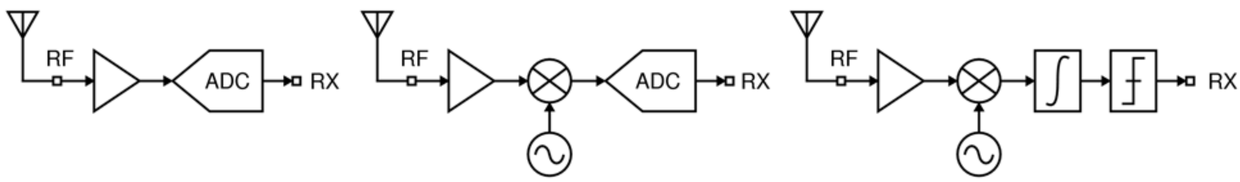


Figure 3. Impulse radio correlator operation.

The principle of operation of the correlator is depicted in Fig. 3. The RF input signal is combined with the template into the mixer, then this signal is integrated and the output bit is decided upon looking at the output amplitude using a comparator. The optimal template signal produced by the template generator depends on the expected RF signal at the input, the modulation scheme used, etc. Using a sub-optimal template leads to some extra SNR losses in the receiver [3].

II.B. Transmitter

For the transmitter architecture an all digital software radio solution can be used, although just like in the case of the receiver its power consumption



(a) (b) (c)

Figure 1. Receiver architecture for (a) software radio (b) software radio with reduced requirements and (c) superheterodyne architecture.

requirements make it unsuitable for a low power consumption implementation.

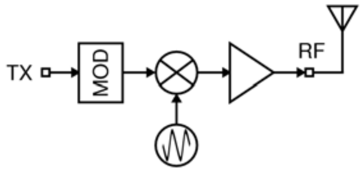


Figure 4. Architecture for the UWB impulse radio transmitter.

The analog transmitter architecture used in the transceiver is depicted in Fig. 4. It uses a template generator and a mixer to modulate and generate the UWB output pulse.

III. Measurements

The transceiver was implemented in a 0.18 μm 1P6M CMOS technology. A microphotography of the fabricated chip is shown in Fig. 5. The chip dimensions are 1525x1525 μm^2.

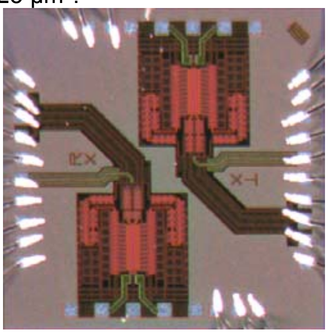
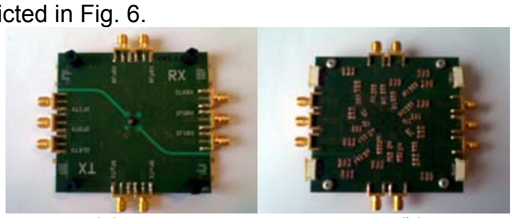


Figure 5. Chip microphotography.

To carry out the measurements the chip was directly connect to a PCB (Chip-on-board, CoB), as depicted in Fig. 6.



(a) (b)

Figure 4. Hybrid PCB photographs (a) front and (b) back

The PCB was implemented in a four layer process. The upper layer was designed with a high frequency substrate to route the input and output RF signals, while the other layers were used for the chip biasing.

The transceiver was measured wirelessly with a pair of UWB antennas, as shown in Fig. 7.

The IR-UWB transceiver was characterized up to 560 Mbps at a distance of 30 cm between the antennas. The total power consumption (combining the transmitter and receiver) was just 42 mW, thus the efficiency of the transceiver was 75 pJ/b. The measured bit error rate (BER) was lower than 10^{-4}.

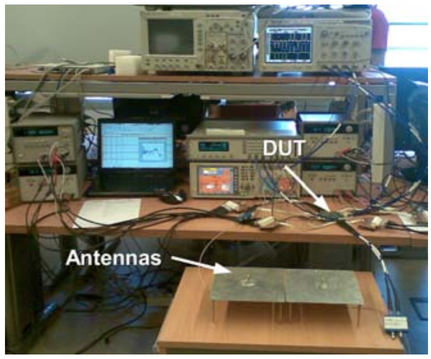


Figure 7. Measurements testbench setup.

The datagram of the transmitted bits and the demodulated signals at the receiver is shown in Fig. 8. When compared to other UWB transceivers, such as [4], this work has better performance in terms of energy efficiency, datarate, die area and interferences robustness.

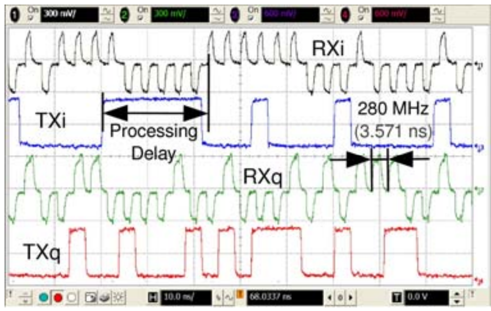


Figure 8. Datagram measurements of the transmitted bits and the demodulated signals at 560 Mbps.

IV. Acknowledgments

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V. References

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