Design of Reconfigurable RF circtuits for self-compensation

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I. Introduction

The aggressive scaling of CMOS technology has allowed the use of CMOS transistors for RF applications. Unfortunately, the unpredictability of the manufacturing process is increasing with every new generation [1]. This increase in variability requires the designer to extend the overdesign margins if production yield needs to be maintained, or a decrease in yield is obtained if design margins are kept [2]. Although this challenge is not new for digital designers [3], it is not until now that RF and analog designers enter in sub-100nm nodes pressed by the market. Little work can be found in the literature about yield enhancement in RF CMOS [4,5]. In this paper we will show how a combination of design choices allows for the design of a PVT robust RF front-end with minimum area, power and nominal specifications penalty.

II. Reference Design

The reference design is shown in figure 1 (only I path shown for simplicity), it comprisses a Common-Source degenerated Low Noise Amplifier biased with low overdrive (moderate inversion) for low power consumption, a couple of charge-injected (also known as current bleeding) Gilbert Mixers [6] for increased gain and on-chip bias circuitry (a bandgap cell-untrimmed- and a modified constant-gm). Its nominal specs are shown in table 1, it also shows the supply and temperature sensitivity .

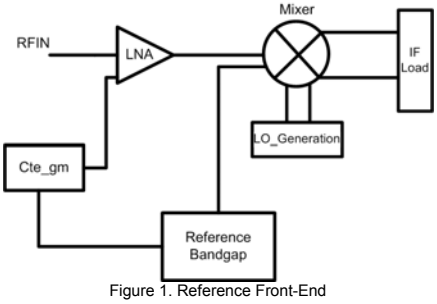

Figure 1. Reference Front-End

VDD+/-10%,Temp=-45ºC,85ºC	Min	Typ(VDD=1.2V, Temp=27ºC)	Max	Δ
Gv(dB)	30.73	35.85	40.08	9.35
NF(dB)	6.034	8.131	10.64	4.606
IIP3(dBm)	-29.23	-26.41	-24.94	4.29
S11(dB)	-15.71	-18.8	-22.09	6.38
PDC(uW)	0.50	1.11	1.88	1.38

Table 1. Specifications for Reference Design

As can be seen the reference design suffers from a great sensitivity to voltage and temperature, for example the great voltage gain variation will need a higher than desirable overdesign of noise and linearity in subsequent stages.

Next table shows the results of 1000 montecarlo runs and the individual and multicondional yields for main specs with the following constraints NF<10,34.2<Gv<37.5,s11<-10,IIP3>-28:

	mean	Std dev	Yield(%)
Gv(dB)	31.75	3.87	24.4
NF(dB)	10.43	2.43	56.1
IIP3(dBm)	-25.74	3.19	76.2
S11(dB)	-17.2	5.35	91.8
Total			11.3

Table 2. Montecarlo results for Reference Design

Comparing tables 2 and 1 its obvious that the design is not well centered (i.e. mean and typical values are quite different) that causes a big spread of values that translates to a low total yield.

III. PVT tolerant RF-Front End

To solve the problems associated with the reference design we propose the following PVT tolerant RF-Front End that comprisses a Current-Reuse LNA a Folded Micromixer , the same on-chip biasing scheme used in the reference design and two OTAs for Supply compensation.

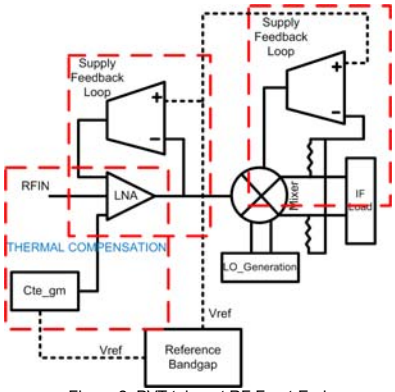

Figure 2. PVT tolerant RF Front-End

III.A. PVT tolerant LNA

The LNA implemented follows a triple strategy for PVT compensation: variability aware choice of design bias point of the transistors for process compensation [7], a negative feedback loop for supply voltage immunity and an open loop bias for temperature compensation. Its worth noting that the use of a current-reuse topology allows the use of two separate bias path thus simplifying the design of Voltage and Temperature compensation strategy; as a matter of fact the PMOS transistor perform a dual function: transconductot and part of a LDO(with the DC feedback loop of figure 2). Similarly the NMOS transistor performs also a dual function: transconductor and Temperature compensation.

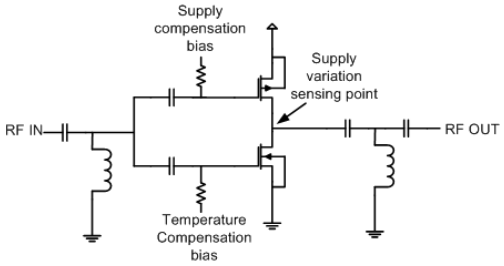

Figure 3. Current-Reuse LNA schematic

III.B. PVT tolerant Mixer

As pointed in [5] in a bleeding Gilbert cell main contributors to variability are the PMOS bleeding transistors, one solution to reduce varibiality is obviously to eliminate them but unfortunately with low supply voltages a conventional Gilbert Mixer fails to meet gain specifications [8]. A sensible solution is a topological change to achieve the specs, in [9] a MicroMixer was presented; that cell is inherently more robust to process variations since gain doesn't depend on injected current ; unfortunately its isolation is lower so in this work a folded structure is used. Figure 4. shows its schematic. PVT tolerance its guaranteed with two techniques: in the transconductor stage a DC feedback loop its used for DC gate bias stability(this technique could also be used in the transconductor of the MicroMixer), in the switching stage a CMFB loop controls the current so that switching transistors are always in the best possible bias point.

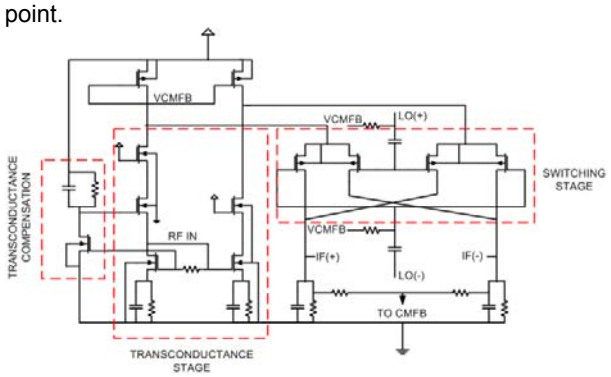

Figure 4. Folded MicroMixer Schematic

III.C. Results for the PVT tolerant Front-End

VDD+/-10%,Temp=-45ºC,85ºC	Min	Typ(VDD=1.2V, Temp=27ºC)	Max	Δ
Gv(dB)	31.09	34.3	35.53	4.44
NF(dB)	8.624	9.127	10.85	2.226
IIP3(dBm)	-21.08	-19.74	-18.56	2.52
S11(dB)	-15.24	-19.76	-23.98	8.74
PDC(mW)	0.41	0.87	1.425	1.015

Table 3. Specifications for PVT tolerant design

As can be seen comparing tables 3 and 4 the PVT tolerant Front-End suffers a reduced Voltage and Temperature sensitivity for all parameters of interest except in input matching; nevertheless worst input matching is only 0.5dBs less than in reference design. Next table shows the results of 1000 montecarlo runs and the individual and multicondional yields for main specs with the following constraints NF<11,32.65<Gv<35.95,s11<-10,IIP3>-21.33 :

	mean	Std dev	Yield(%)
Gv(dB)	33.14	1.85	60.4
NF(dB)	9.53	1.11	89.5
IIP3(dBm)	-20	1.71	78.6
S11(dB)	-15.15	5.64	79.6
Total			40.5

Table 4. Montecarlo results for PVT tolerant design

As can be seen applying the same safety margins over the nominal values the proposed design shows a much greater total yield, being input matching the only worst specification limit (nevertheless it could be improved using calibration that could also help to improve voltage gain yield).

IV. Conclusions

In previous sections we have shown how a combination of strategies allows to reduce PVT spread in a low-power front-end without sacrificing nominal performances and without increasing power consumption with only minimal additional hardware overhead.

V. Acknowledgments

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VI. References

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