Variations-Aware Circuit Designs for Microprocessors

Author: Marc Pons, Thesis Advisors: Francesc Moll and Jaume Abella

I. Introduction

The evolution of integrated circuits industry is based on technology scaling. For every new technology node, the critical dimension that can be printed in a circuit layout becomes smaller. This scaling allows the increase of the number of elements that can be included in a single chip and therefore to implement more complex functions.

However, integrated circuit manufacturers are facing the increasing manufacturing costs associated to this technology scaling. Printing smaller critical dimensions for each technology node is becoming unaffordable [1].

Lithography processes used for manufacturing that involve resolution enhancement techniques are computationally expensive for large circuits with arbitrary layout patterns. That is why design time and therefore the time-to-market are increased.

A new trend that is becoming dominant is to improve layout regularity so that the layouts to be printed are more repetitive and easy to manufacture.

Our proposal is to push to the limit layout regularity to minimize manufacturing costs.

In section II we will explain in more detail our design proposal that is called Via-Configurable Transistor Array (VCTA). In section III we will show the regularity improvement of our layouts when compared to the conventional layouts. Finally in section IV we provide the conclusion.

II. VCTA design proposal

Integrated circuit layouts are composed by devices (transistors) that perform the functions and by interconnects to transport the signals involved. VCTA focus on maximizing layout regularity for both levels. It is based on the repetition of a single basic cell that can implement different functions depending on the configuration of vias and contacts. Fig. 1 shows the VCTA structure that is explained in next subsections. For more details please refer to [2].

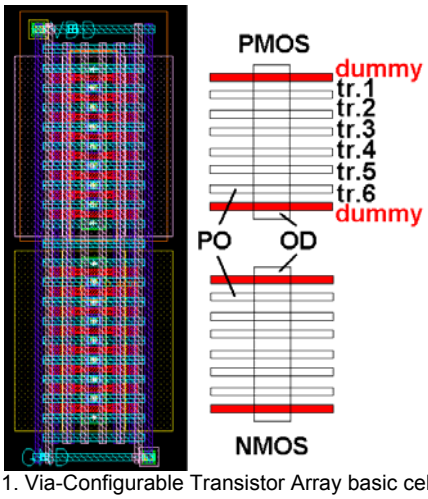

Figure 1. Via-Configurable Transistor Array basic cell (OD=Oxide Diffusion, PO=Polysilicon).

II.A. Maximizing layout regularity at device level: the transistor array

VCTA is based on the use of a single basic cell containing one array of PMOS transistors and one array of NMOS transistors. In order to force maximum transistor layout regularity, all transistors have the same width and the minimum channel length.

II.B. Maximizing layout regularity at interconnect level: the via-configurable structure

In order to ensure interconnect regularity VCTA uses a regular interconnect grid of parallel metal lines. The lines alternate from horizontal to vertical direction from one layer to the next.

III. Regularity improvement

The regularity improvement of our VCTA layouts has been demonstrated using a two dimensional Fourier Transform of the polysilicon layer for VCTA circuits and conventional design. The peaks in the VCTA FFT represent the spatial frequency of repetition of our regular layouts. However, for the conventional design no clear peaks of repetition can be observed.

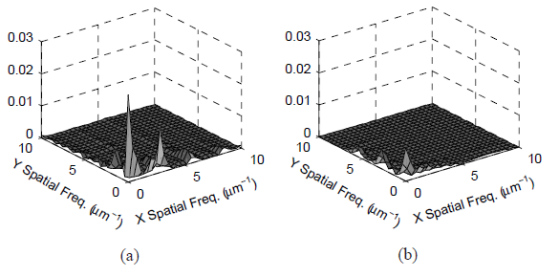

Figure 1. 2-dimensional normalized FFT of the polysilicon layer for: (a) VCTA layout (b) conventional layout.

IV. Conclusion

To face the arising issues associated to technology scaling, we have proposed a new regular layout design fabric called VCTA. Compared to the conventional layout style, we have demonstrated its regularity using the visual inspection of the two dimensional FFT. Therefore manufacturing costs can be reduced.

V. Acknowledgments

This work has been supported by Intel Corporation, EU-FEDER funds, TEC2008-01856, TIN2007-61763, ENIAC MODERN (Spanish MICINN PLE2009-0024), AGAURSGR1497, FPU AP2007-04125, 2009SGR1250, TIN2007-60625 and Beatriu Pinós 2009 BP-B 00260.

VI. References

[1] B. Wong et al, Nano-CMOS Design for Manufacturability: Robust Circuit and Physical Design for Sub-65 nm Technology Nodes. John Wiley & Sons, 2009.

[2] M. Pons et al, “VCTA: A Via-Configurable Transistor Array Regular Fabric,” 18th IEEE/IFIP International Conference on VLSI and System-on-Chip, VLSI-SoC, 2010.

This page intentionally left blank